Safia Reazi

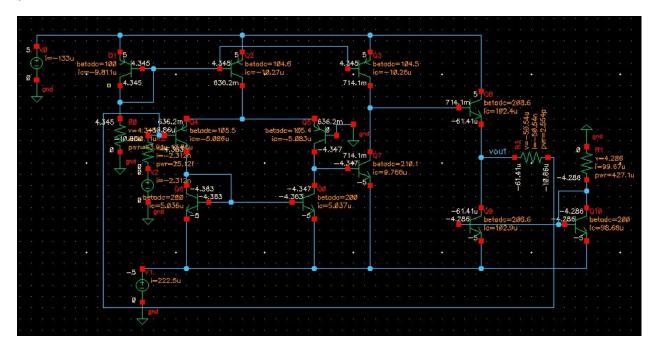
170LC

Lab 6

ID: 21415003

6/2/2020

SIM 1



- All transistors are in forward active since Vce = 4.4V which is higher than Vce(sat) = 0.2V.
- The simulated values for the collector currents are similar to the actual values of $10\mu A$ and $100\mu A$. The simulated values are $10.27\mu A$ and $102.9\mu A$.
- The simulated values for the DC voltages are close to zero with V- = 0V and Vout = $-61\mu V$
- Resistor in 1st stage:
 - $\circ \quad Rref = 4.3V/10\mu A = 430k\Omega$
- Resistor in 2nd stage:
 - $\circ \quad Rref2 = 4.3V/100\mu A = 43k\Omega$

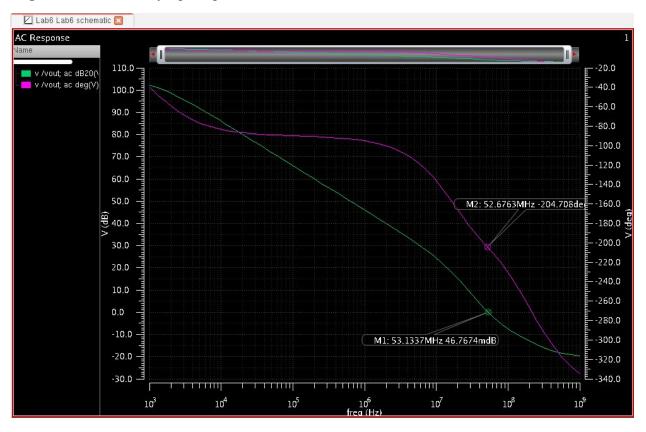
SIM 2



• The output is oscillating which indicates that the circuit is unstable.

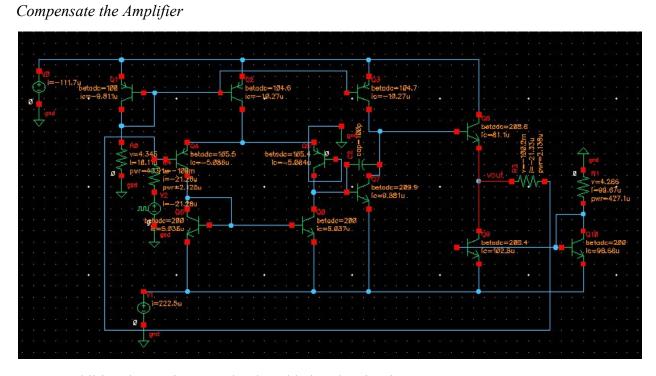
SIM 3

Magnitude and Phase of Op-Amp

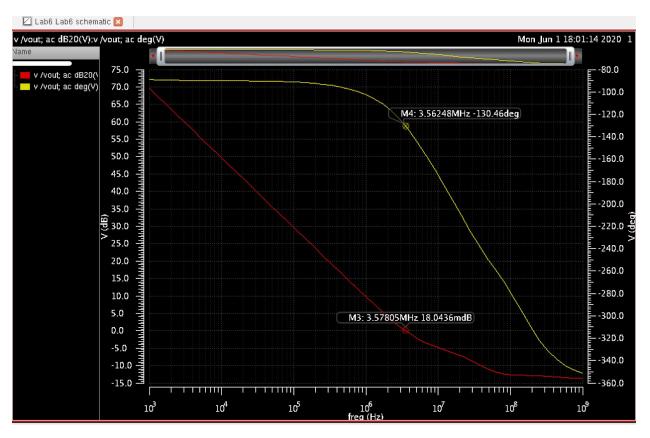


- Unity gain frequency (near 0dB): **53.12MHz**
- Phase (near 53.12MHz): **-204.7**°
- Phase Margin: $-204.7^{\circ} (-180^{\circ}) = -24.7^{\circ}$
 - Since the phase margin is negative the circuit is unstable.

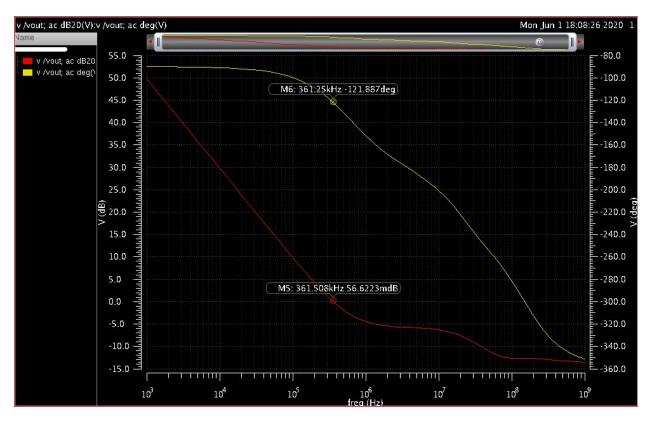
SIM 4



- Additional capacitors need to be added to the circuit
 - \circ Cc = 10pF
 - O Dominant Pole:
 - Pc = 1/rout*Cc(1+A2)
- Phase Margin: phase(wo) $(-180^\circ) = 60^\circ$
 - \circ PM = -120° (theoretical value)

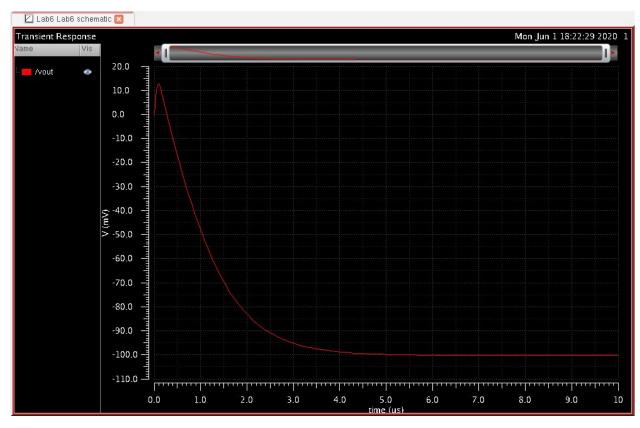


- Phase Margin: $-130.4^{\circ} (-180^{\circ}) = 49.6^{\circ}$
 - Although the phase margin is now positive and the circuit is stable, it is not at 60°. In order for there to be a 60° phase margin, the value of the capacitor needs to be increased.



- Cc = 100pF
- Phase Margin: $-121.8^{\circ} (-180^{\circ}) = 58.2^{\circ}$
 - \circ This value is close to the 60° phase margin.

SIM 5



 After compensation, there is no oscillation in the circuit which means the circuit is now stable. Since Vpulse is added to the input, the transient response increases to about 14mV and flat lines around -100mV due to the negative feedback.

Conclusion

In this circuit we were asked to design inverting amplifiers to observe the transient response of the op-amps. When capacitors are not present in the circuit the output waveform is oscillating, meaning the circuit is unstable. We used two different inputs, Vpulse and Vac to prove that the circuit is unstable. We looked at the magnitude and phase plots to determine the phase margins. A negative phase margin indicates that the circuit is unstable. After adding capacitors to the circuit, we see that the phase margin becomes positive. However, in order to get a 60° phase margin the value of the capacitor needs to be increased. We increased the values of the capacitor from 10pF to 100pF. Through compensation, the circuit becomes stable.