

Safia Reazi

170LC

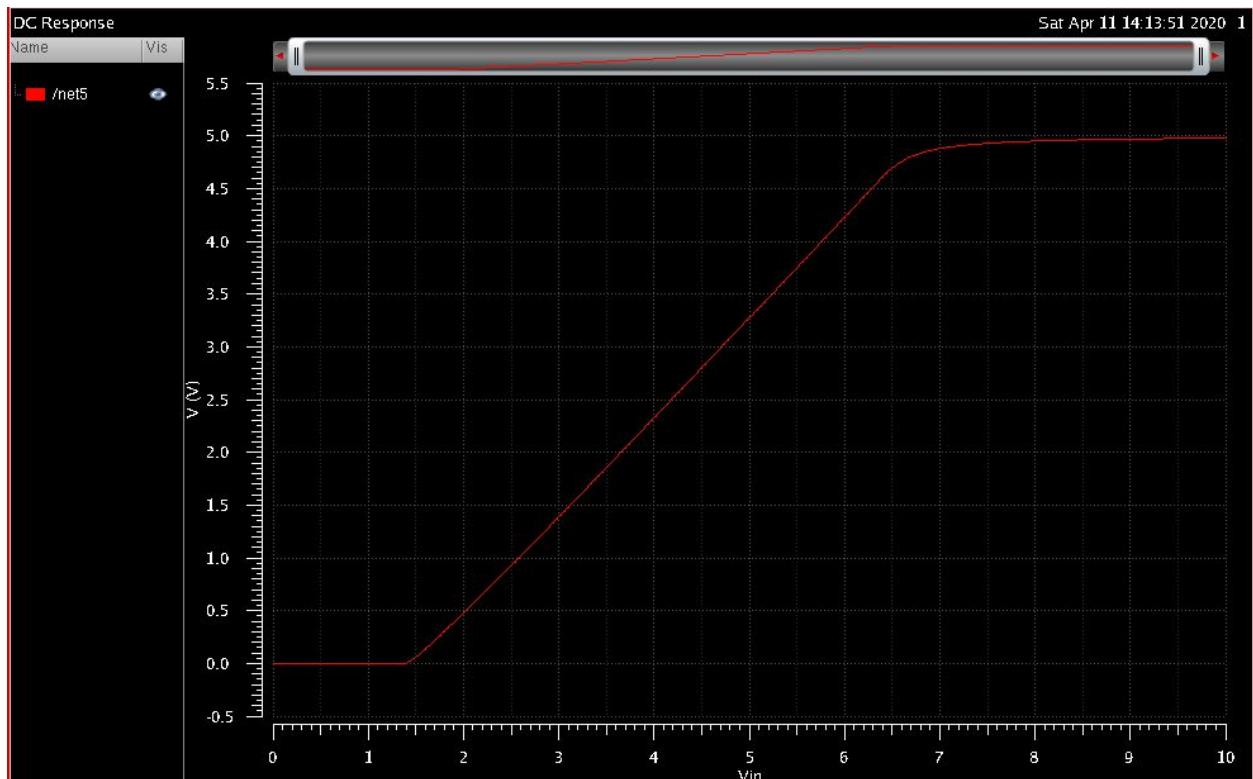
Lab 1

4/14/2020

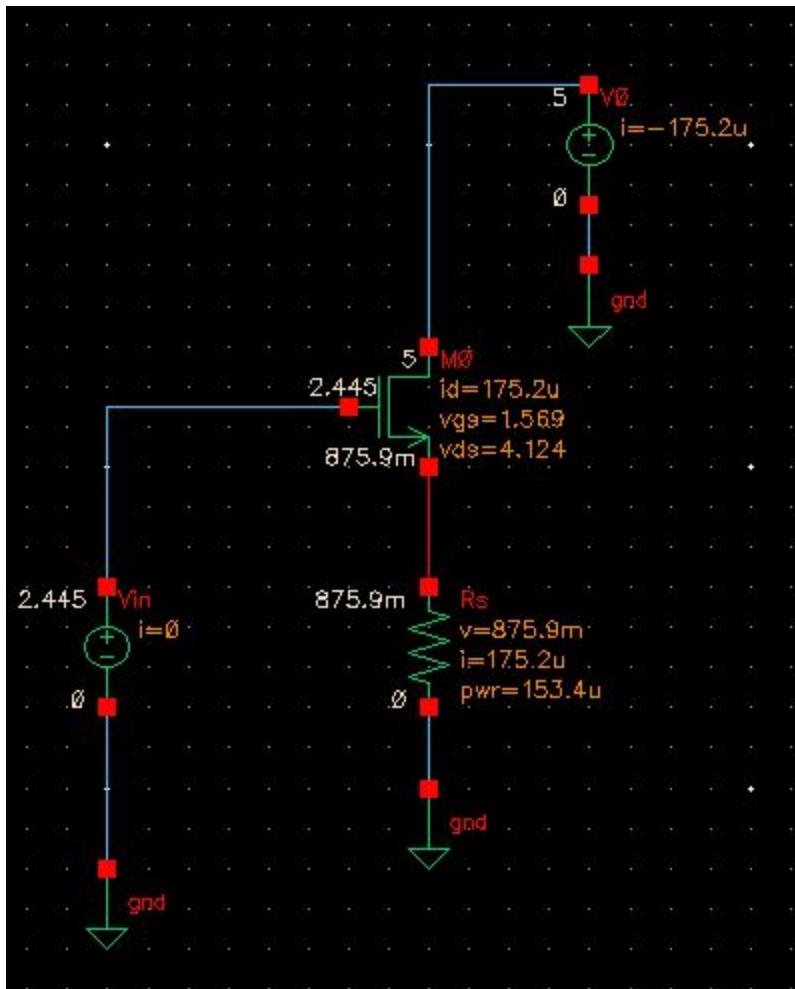
## Problem 1

A.

$V_{out}$  vs.  $V_{in}$



- $V_{in} = V_{in(eq1)}$ ;  $\frac{6.33V - 1.44V}{2} = 2.445V$
- Region of operation (from bottom to top of graph): 1) cutoff, 2) saturation, 3) triode

**B.***DC Operating Point Analysis***C.**Calculations

Small signal parameters from simulation:

- $gm = 2.072n$
- $ro = 1.11 M\Omega$

Calculated small signal parameters

- $gm = \frac{2Id_s}{V_{gs} - V_t} = 2.061n$ 
  - $Id_s = k' / 2(W/L)(V_{gs} - V_t)^2 \Rightarrow 175.2u = 0.6m / 2(200u/10u)(V_{gs} - V_t)^2$
  - $V_{gs} = \sqrt{(175.2u/6m)} + 1.4 = 1.57V$

- $r_o = \frac{1}{\lambda I_{ds}} = 1/(0.005)(175.2\mu) = 1.14 \text{ M}\Omega$

Percent error:

- gm % error =  $2.072n - 2.061n / 2.072n * 100\% = 0.53\%$
- $r_o$  % error =  $|1.11\text{M}\Omega - 1.14\text{M}\Omega|/1.11\text{M}\Omega * 100\% = 2.7\%$

## D.

### Comparing AC and DC components of Vin and Vout



- DC input level: 2.445V
- DC output level: 0.876V
- Amplitude\_Vin: 20mV
- Amplitude\_Vout: 885 mV - 866 mV = 19mV
- Gain = Amp\_Vout/Amp\_Vin = 20/19 = 1.05
- DC and AC output levels decrease when adding a sine wave input and the gain is small.

E.

Increase  $V_{in}(eq1)$  by 10mV

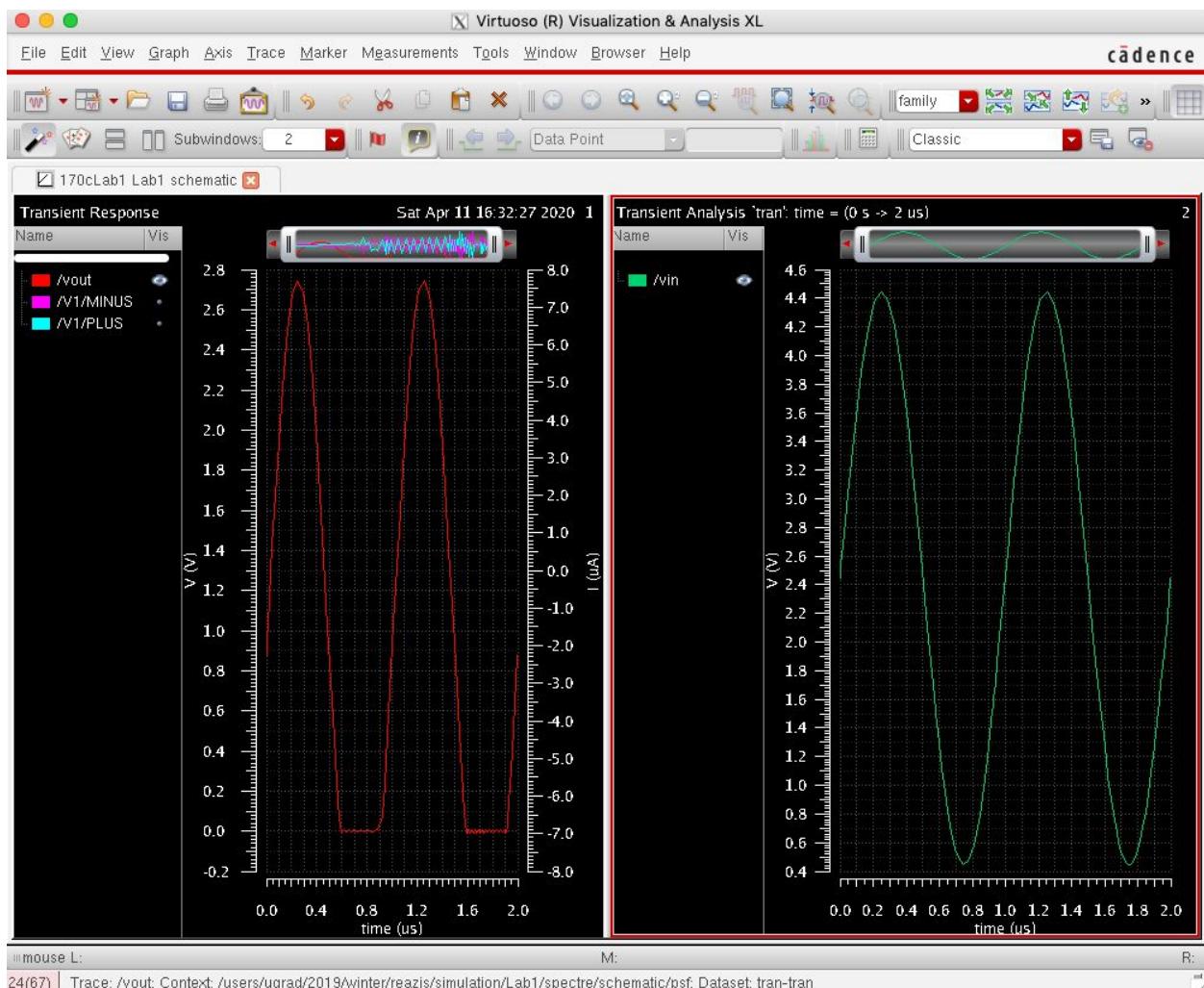


Fig. 1

- Since this is a buffer circuit, increasing  $V_{in}$  by 10mV will have no effect on the amplitude. However, increasing the amplitude from 10mV to 2V, which would be the maximum value, shows that  $V_{out}$  will start to clip (Fig.1). On the other hand, if  $V_{in}$  is increased significantly the output does not clip but the input does at around 14.4V (Fig. 2).

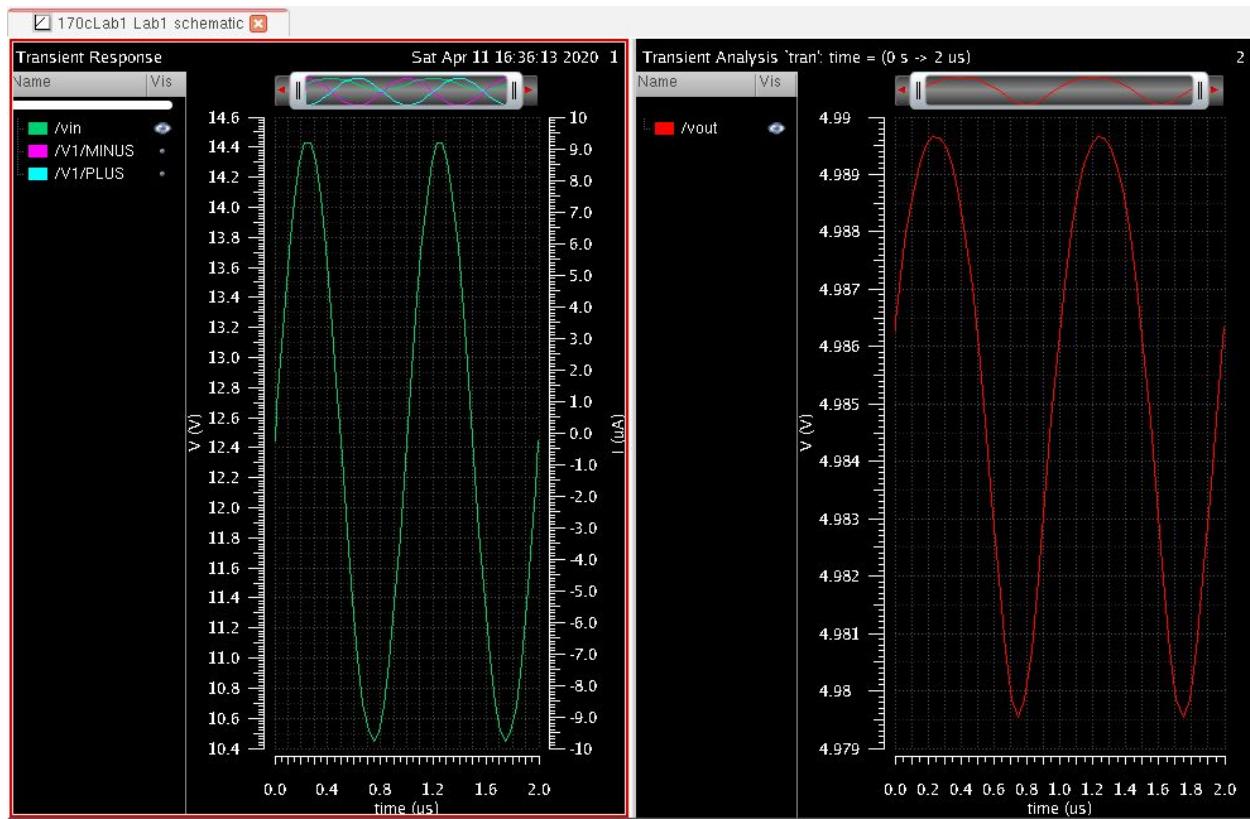


Fig.2

## Problem 2

A.

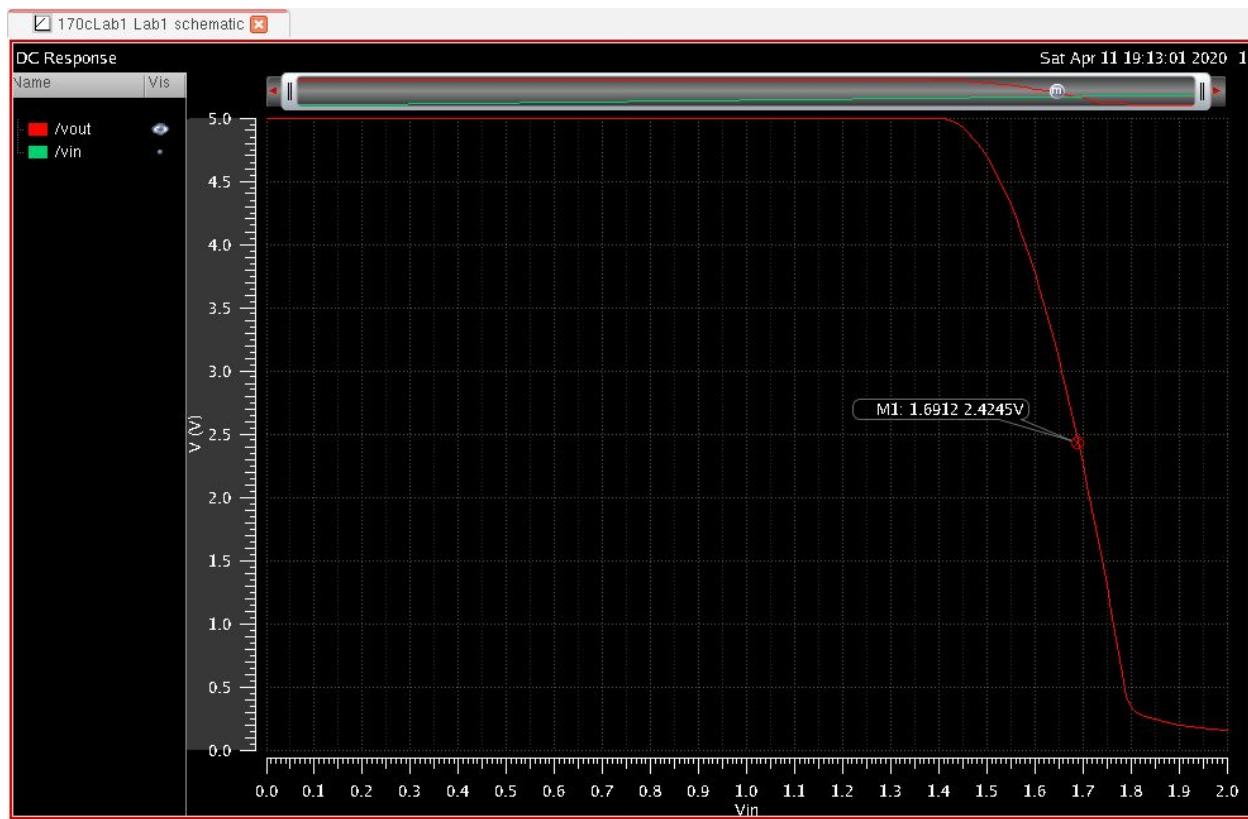
$V_{out}$  vs.  $V_{in}$



- Region of operation (from top to bottom of graph): 1) cutoff, 2) saturation, 3) triode

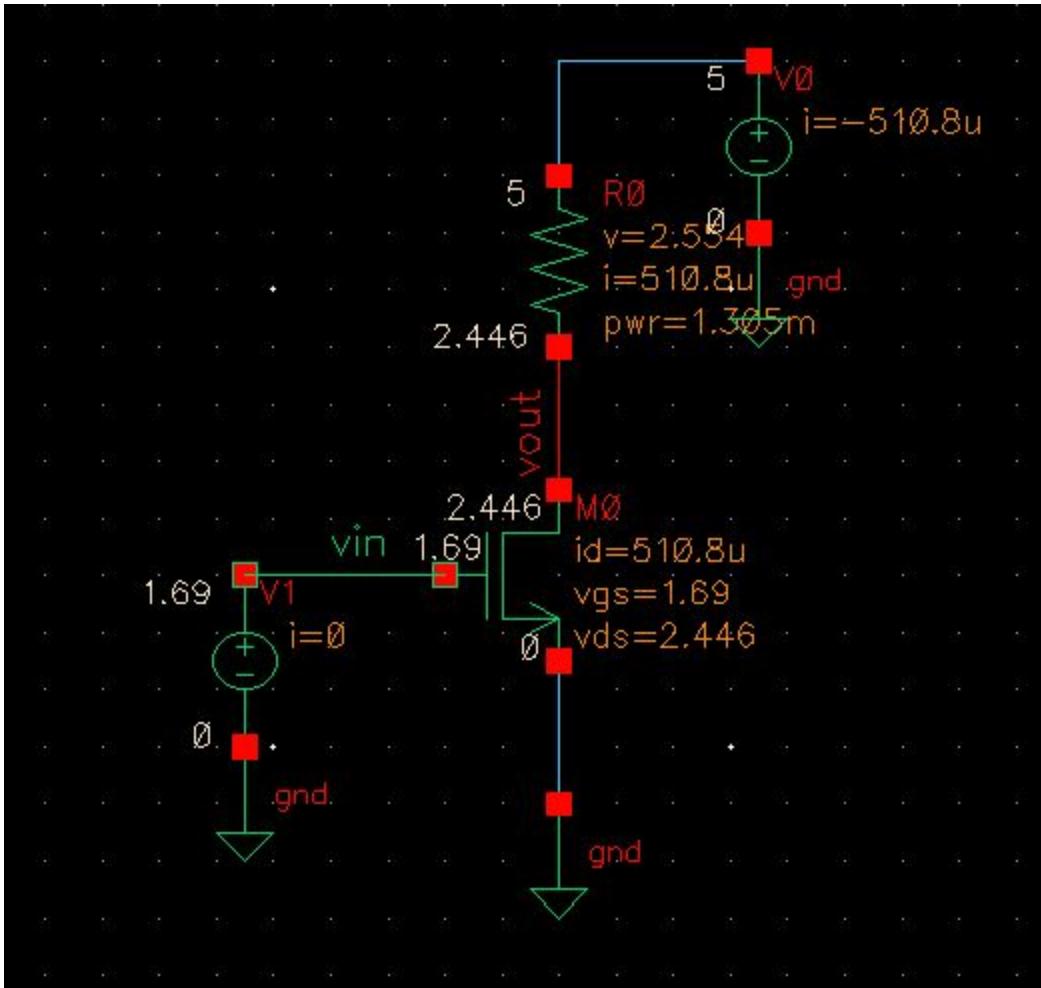
**B.**

$$V_{in} = V_{in(eq2)}$$



- $V_{out} = 1.69V$
- $V_{in} = V_{in(eq2)}: \frac{5V - 0.155V}{2} = 2.422V$

### DC Operating Point Analysis



- The transistor is operating in saturation mode since  $V_{ds} \geq V_{gs} - V_t$ .
  - $2.446V \geq 1.69V - 1.4V$

C.

### Calculations

Small signal parameters from simulation:

- $g_m = 3.523m$
- $r_o = 0.386 M\Omega$

Calculated small signal parameters

- $g_m = \frac{2I_{ds}}{V_{gs}-V_t} = 3.517m$ 
  - $I_{ds} = k'/(2(W/L)(V_{gs}-V_t)^2) \Rightarrow 510.8\mu A = 0.6m/(2(200\mu/10\mu)(V_{gs}-V_t)^2)$
  - $V_{gs} = \sqrt{(510.8\mu/6m)} + 1.4 = 1.69V$

- $r_o = \frac{1}{\lambda I_{ds}} = 1/(0.005)(510.8\mu\text{A}) = 0.392 \text{ M}\Omega$

Percent error:

- gm % error =  $3.523\text{n}-3.517\text{n}/3.523\text{n} * 100\% = 0.17\%$
- $r_o$  % error =  $|0.386\text{M}\Omega - 0.392\text{M}\Omega|/0.386\text{M}\Omega * 100\% = 1.5\%$

## D.

Gain for common source circuit

- $A = gm * (R_d \parallel r_o)$ , Accepted gain: 17.3
- Slope  $(5-0.311)/(1.8-1.43) = 12.64$
- Calculated gain:  $A = 3.523\text{m} * (4.9\text{k}) = \underline{17.26}$
- $r_o = 1/gds = 1/2.586\mu\text{A} = \underline{386\text{k}}$

Gain percent error:

$$17.3 - 17.26 / 17.3 * 100\% = \underline{0.23\%}$$

## E.

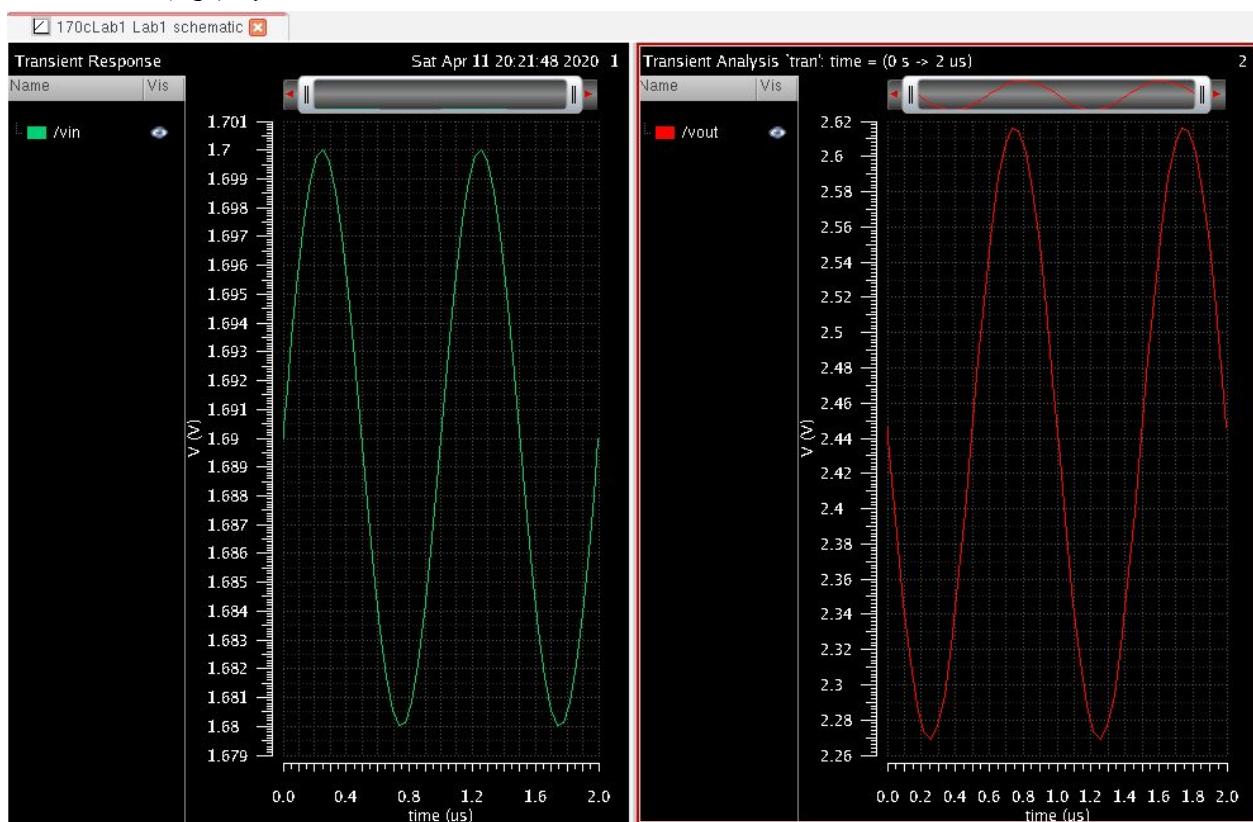
*Comparing AC and DC components of Vin and Vout*



- DC input level: 1.69V
- DC output level: 2.45V
- Amplitude\_Vin  $1.691 - 1.689 = 2\text{mV}$
- Amplitude\_Vout  $2.4631 - 2.4284 = 34.7\text{mV}$
- Gain = Amp\_Vout/Amp\_Vin =  $34.7/2 = 17.35$
- DC and AC output levels increase when adding a sine wave input and the gain is high.

## F.

Increase Vin(eq2) by 10mV

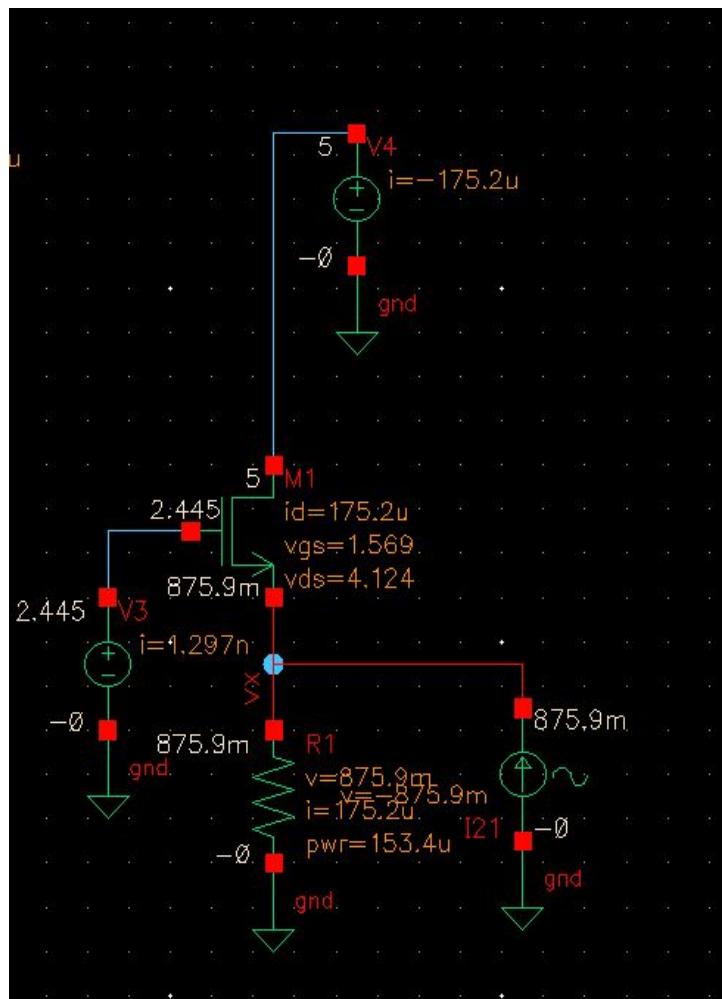


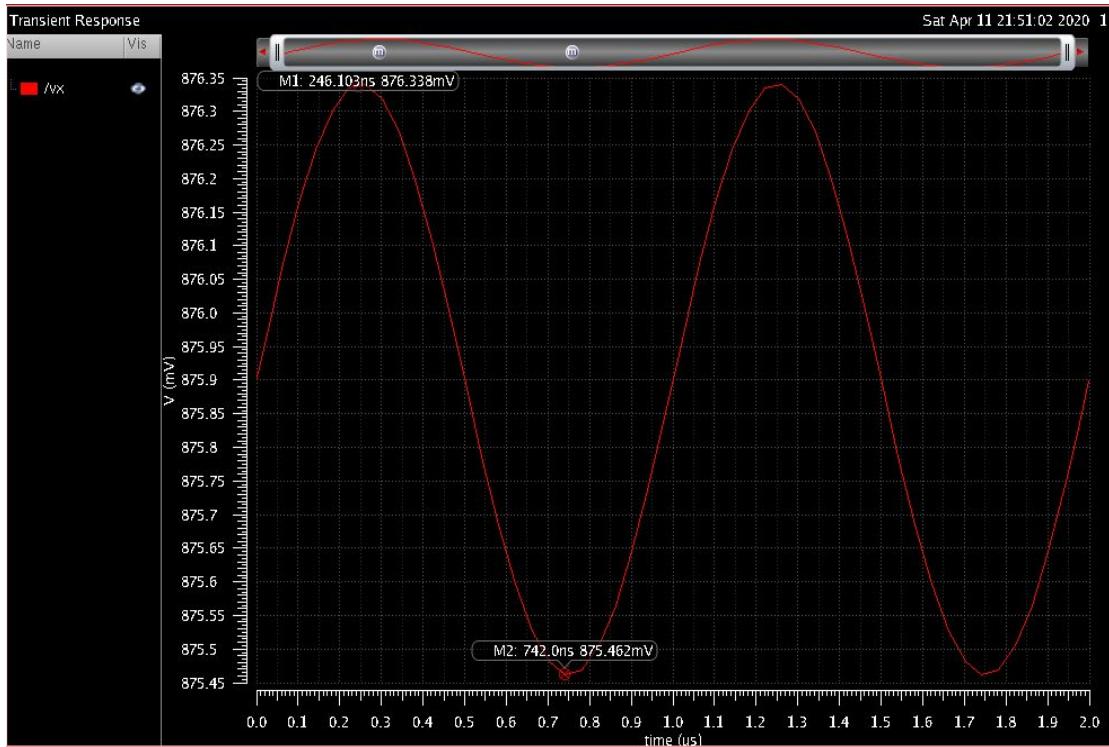
- Increasing Vin(eq2) by 10 mV increases the amplitude of the output to 347 mV.

### Problem 3

A.

Calculate  $R_{out}$  for a common source circuit

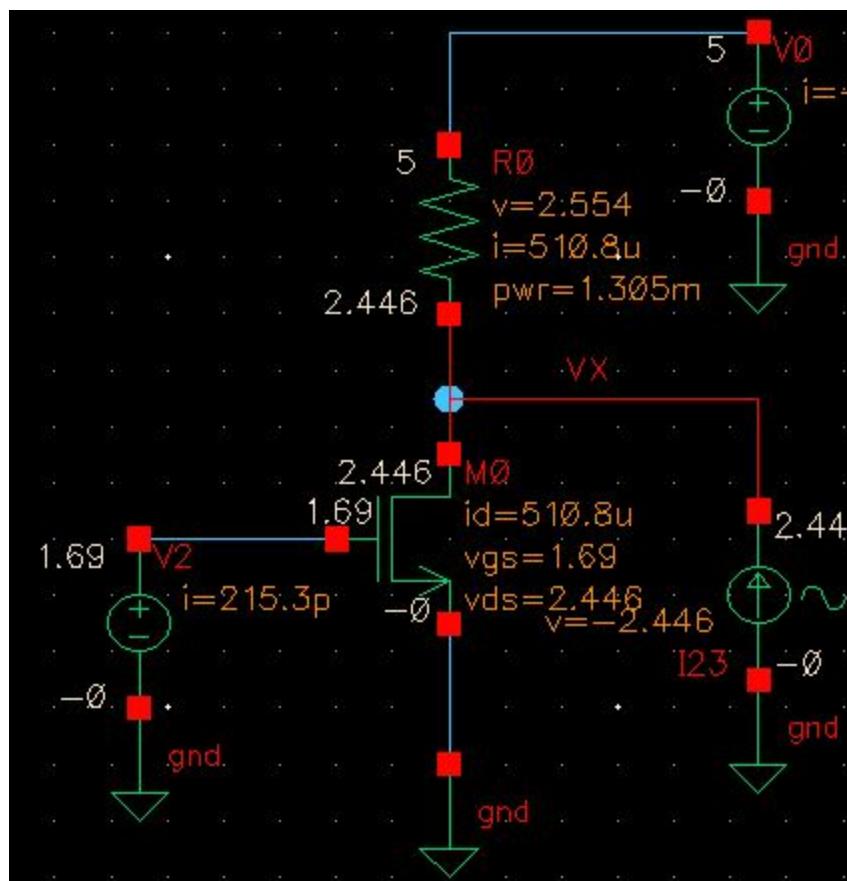


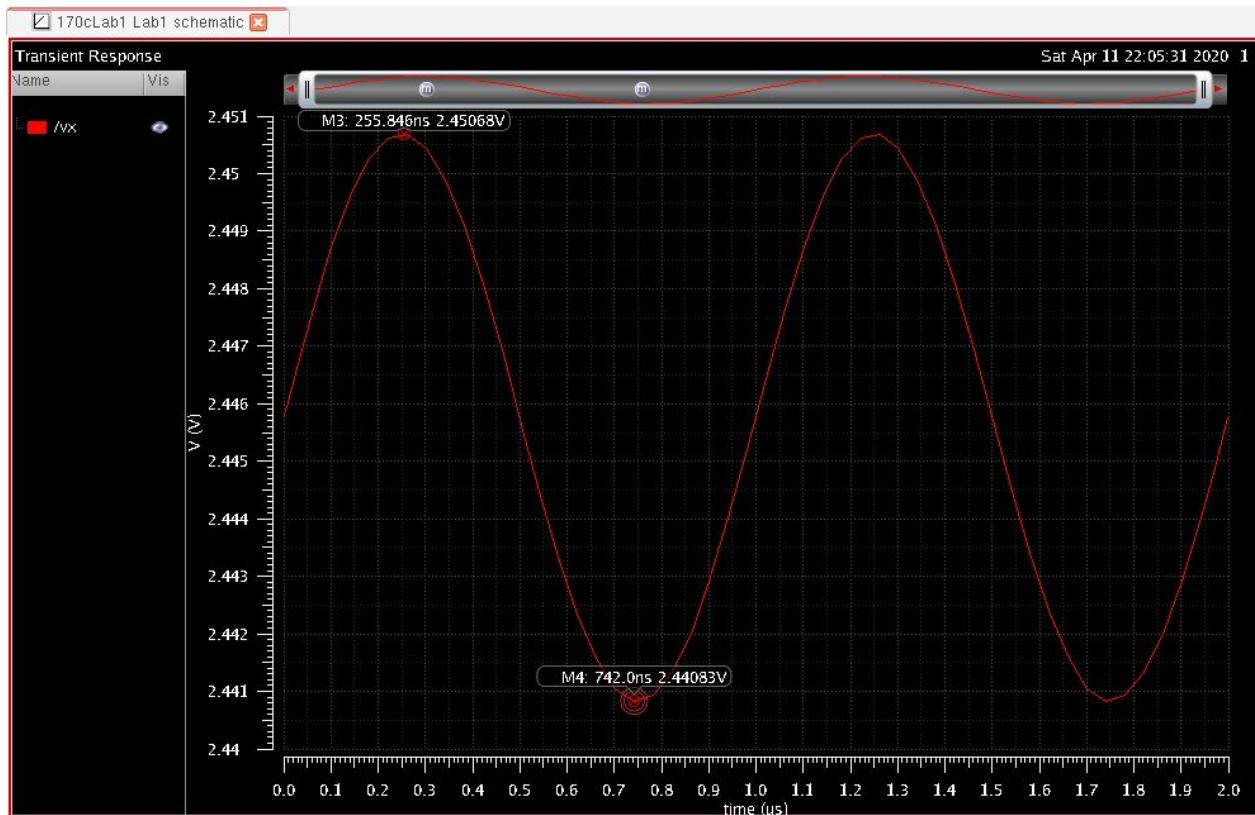


- $R_{out} = \text{Amp\_vx}/\text{Amp\_ix}$
- $\text{Amp\_Vx} = 876.3 - 875.4 \text{ mV} = 0.9 \text{ mV} = 900 \mu\text{V}$
- $\text{Amp\_Ix} = 2 \mu\text{A}$
- $R_{out} = 900 \mu\text{V}/2 \mu\text{A} = \underline{450 \text{ ohm}}$

**B.**

Calculate  $R_{out}$  for common drain



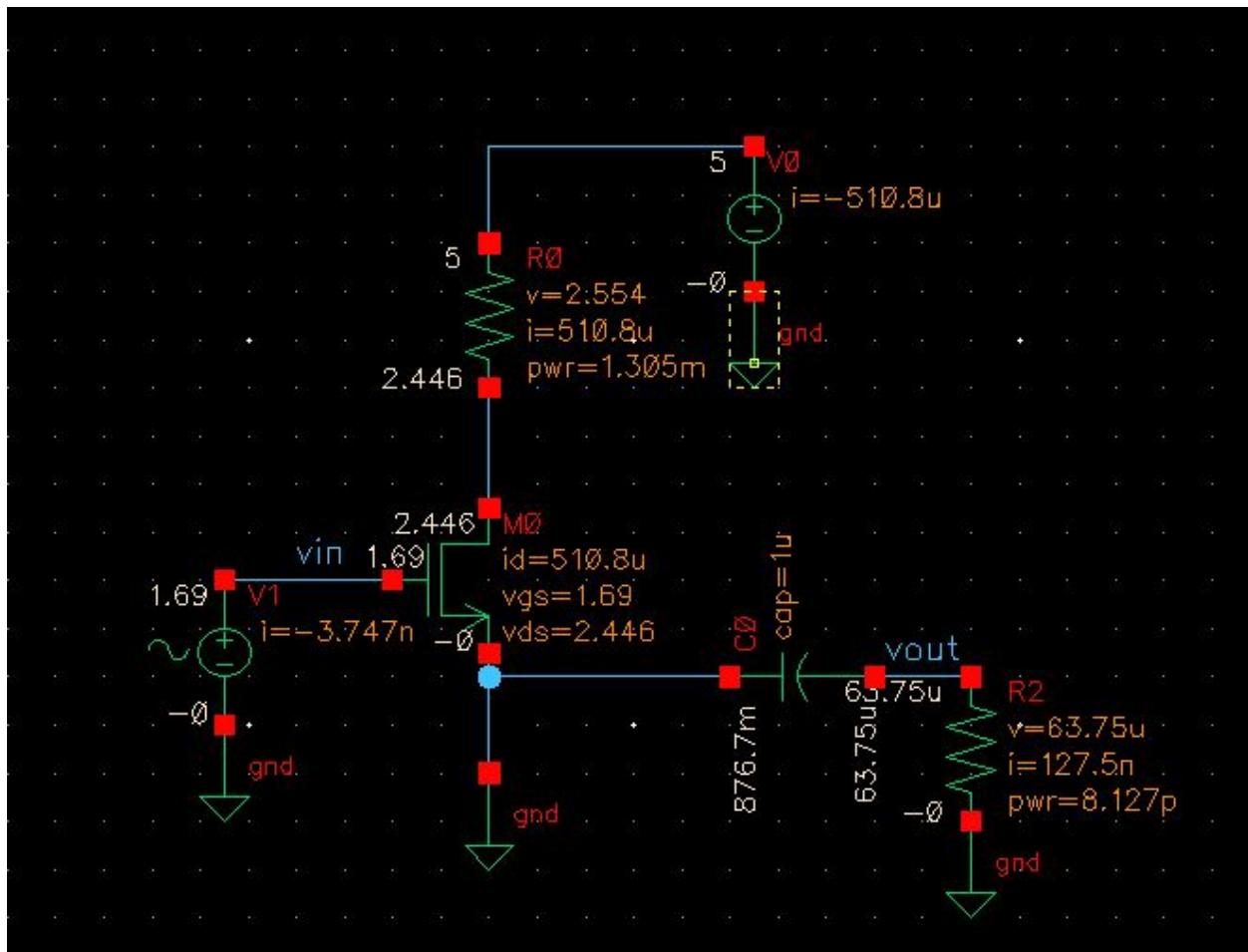


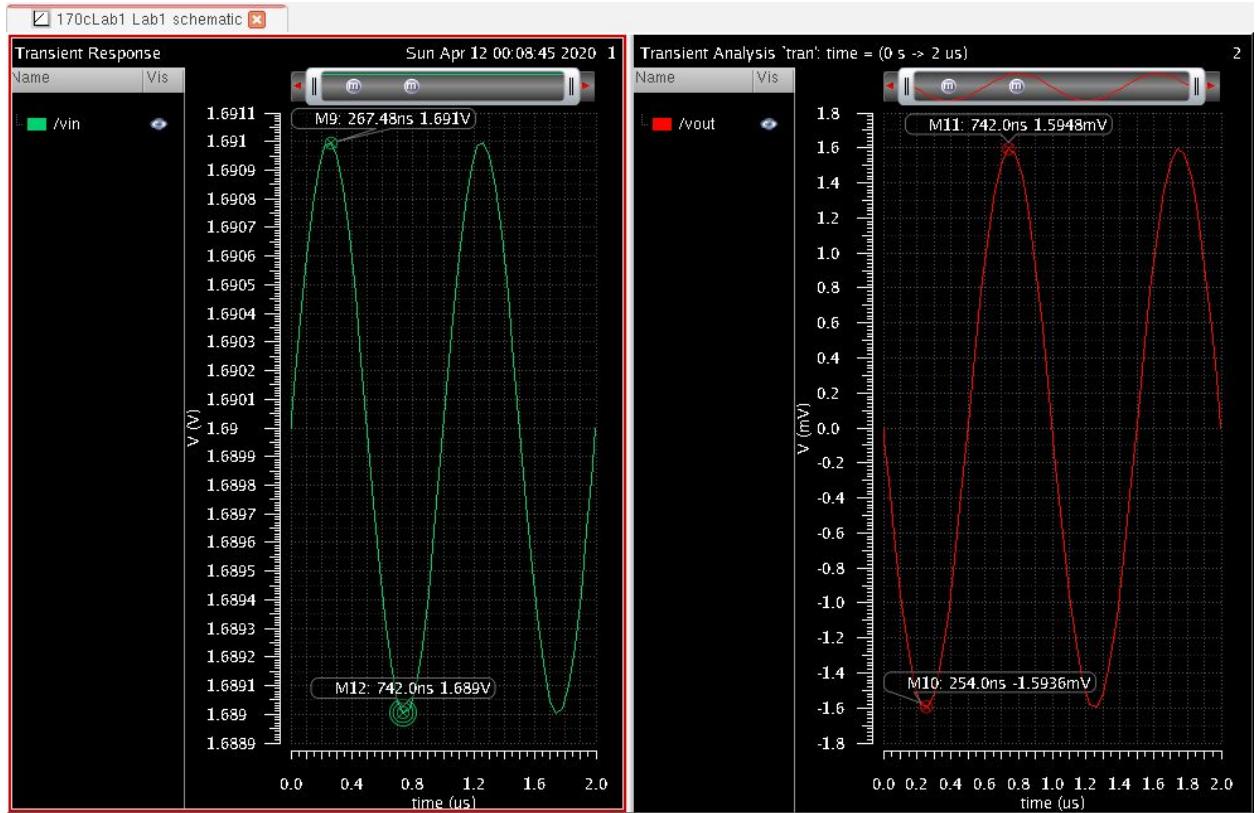
- $R_{out}$ : Amp vx/Amp\_ix
- $Amp\_Vx = 2.45V - 2.44V = 0.01V = 10mV$
- $Amp\_Ix = 2\mu A$
- $R_{out} = 10mV/2\mu A = 5k$

## Problem 4

A.

Small-signal gain  $V_{out}/V_{in}$  for one stage amplifier

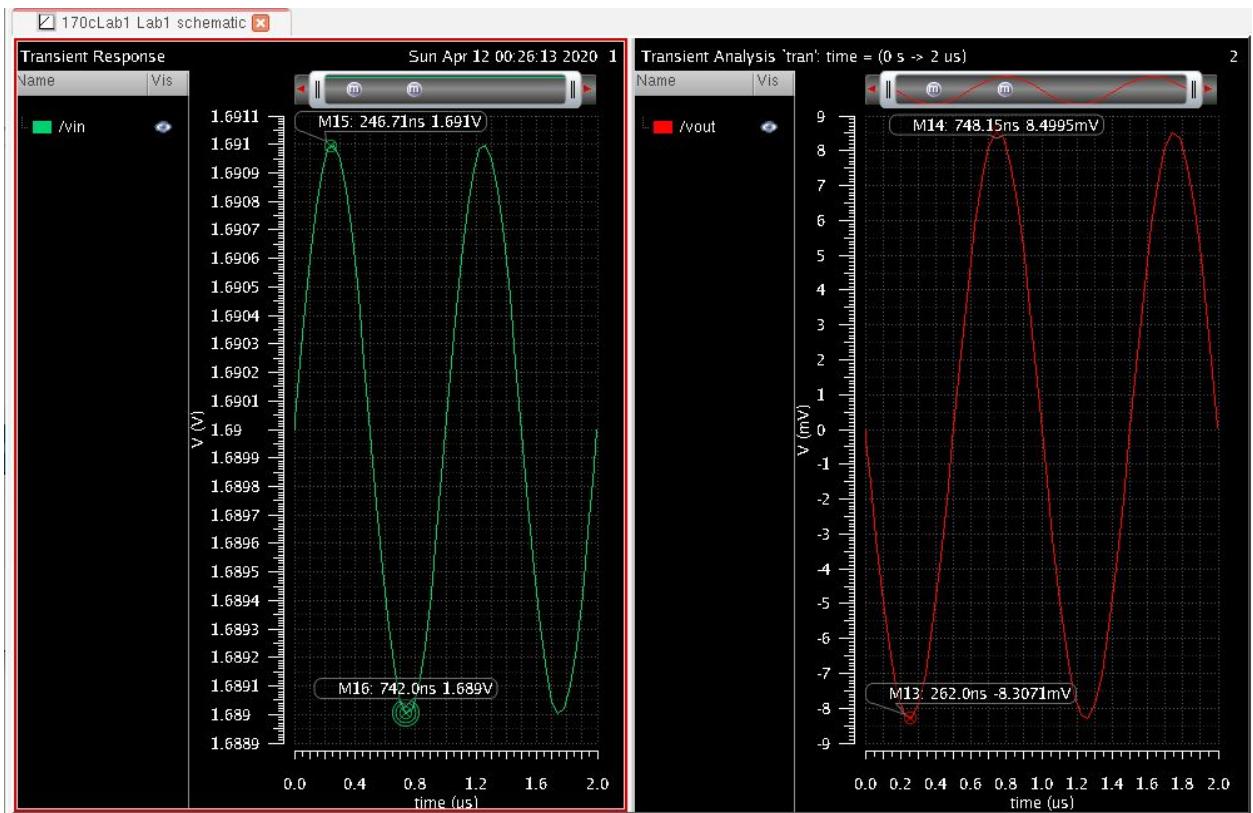
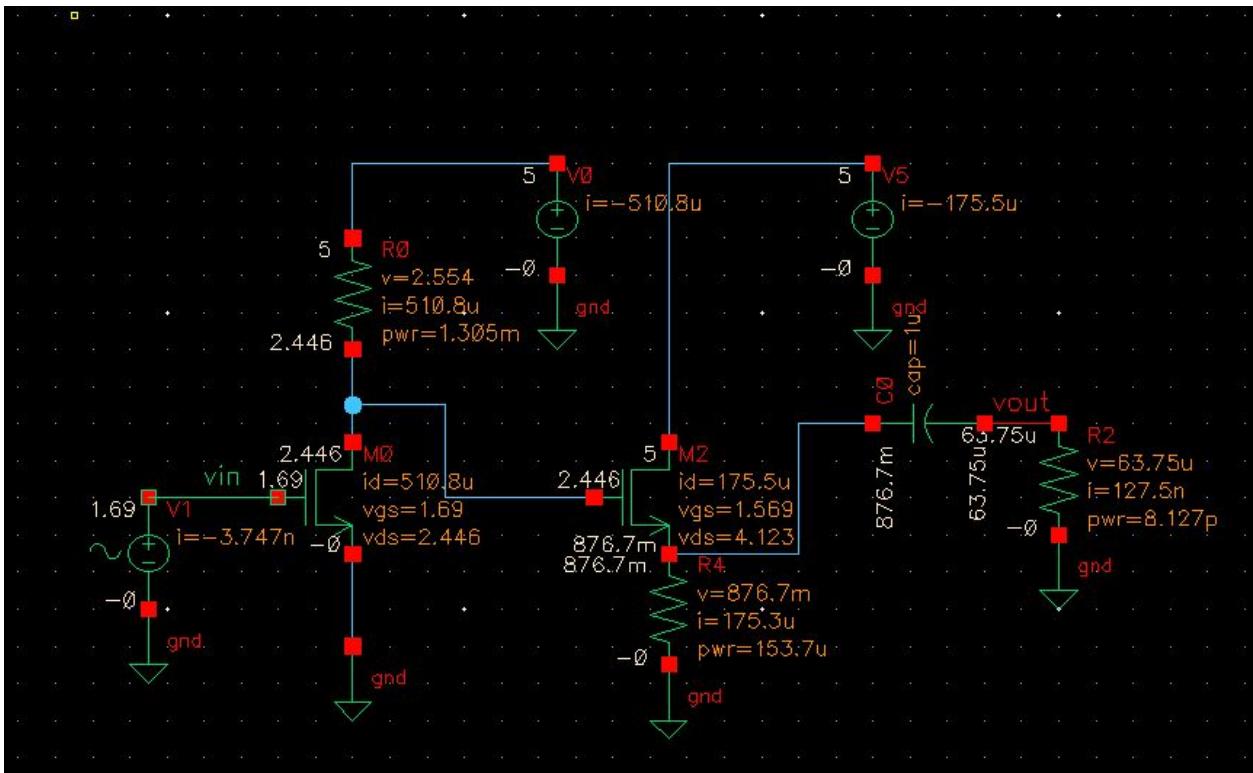




- $A = gm^* (R_d \parallel r_o \parallel R_l) = gm^*(R_d \parallel R_l)$ . Since  $r_o$  is large it goes to 0.
- $A = gm^*(R_l)$ . Since  $R_d$  is a lot smaller than  $R_l$ , it goes to 0. This will decrease the gain.
- $Amp_{vout} = 1.59mV$
- $Amp_{vin} = 2mV$
- DC output level is 0 because we are looking at  $V_{out}$  after the capacitor.
- Gain =  $Amp_{vout}/Amp_{vin} = \underline{0.795}$ . Small!

B.

*Small signal gain Vout/Vin for two stage amplifier*



- Gain = A1 \* A2
- A1 = gm \*Rd
- A2 =  $(Rs||RI / (1/gm + Rs||RI))$
- Gain = gm\*Rd <- expecting higher gain
- A\_vout=8.4mV
- A\_vin=2mV
- Gain = Amp\_vout/Amp\_vin = 4.2 which is a lot higher than previous the one-stage amplifier

## Conclusion

The simulations given produced the results as expected. In the common drain and common source circuit, the correct plots along with the calculations for Vin(eq1) and Vin(eq2), gm, and ro were determined. The percent error between the actual and calculated values for gm and ro were small. In the circuits, Rout was calculated by putting a current source on the source and drain, respectively. To consider the effects of loading on the common source and common drain circuit, a capacitor was connected to the circuit. In the circuit with one transistor, the gain is small but when there are two transistors connected together, the gain is a lot higher thus making the circuit more robust.

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Lab 2

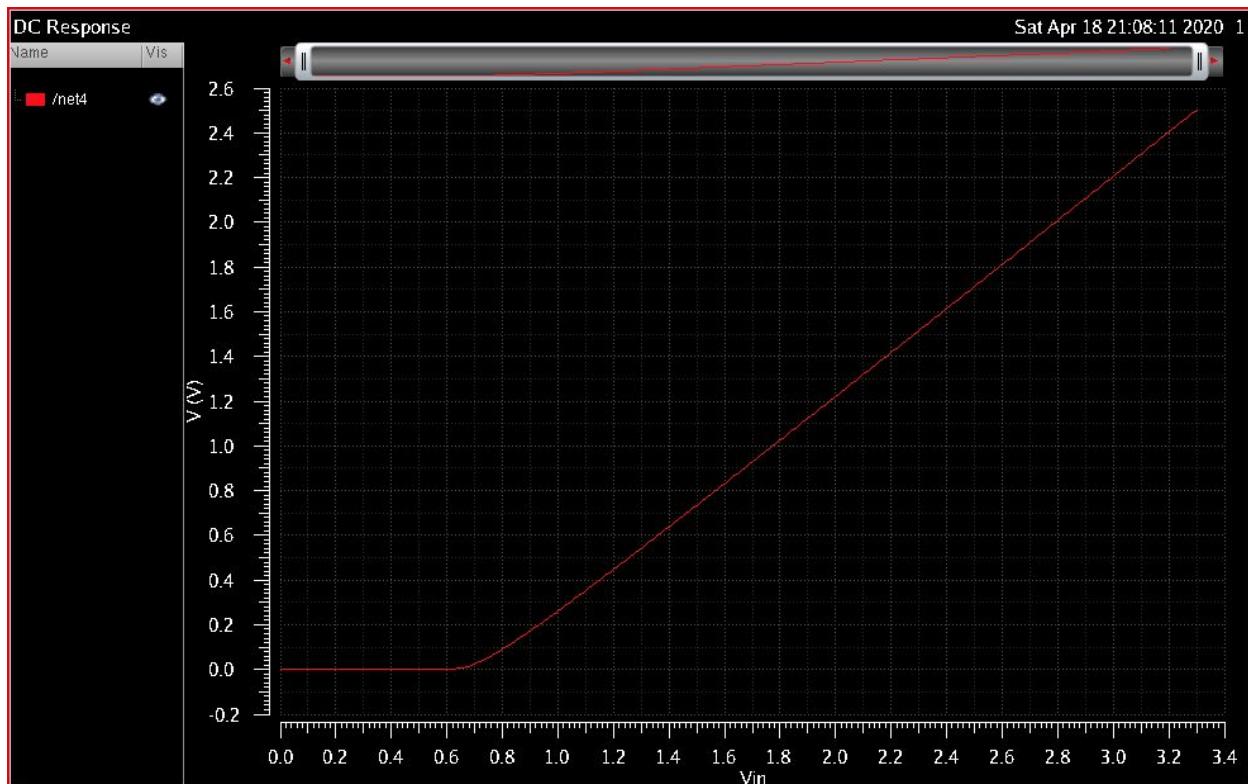
4/21/2020

## Problem 1

### Common Collector

A.

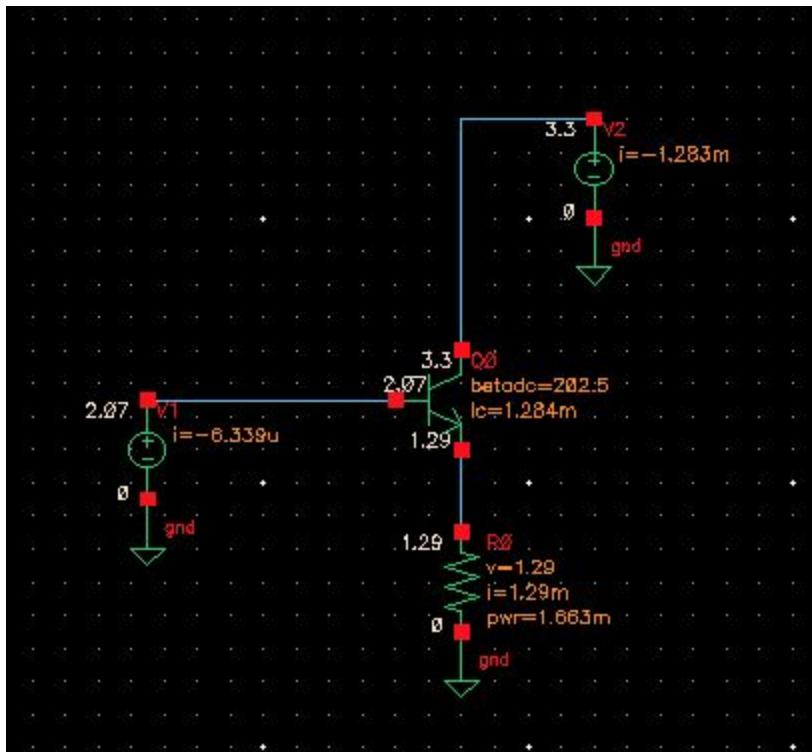
$V_{out}$  vs.  $V_{in}$



- $V_{in} = V_{in(eq1)}: \frac{3.3V - 0.706V}{2} = 1.297V$
- Region of operation (from bottom to top of graph): 1) cutoff, 2) forward active

## B.

### DC Operating Point Analysis



## C.

### Calculations

Small signal parameters from simulation:

- $gm = 49.61m$
- $ro = 78.87k\Omega$

Calculated small signal parameters

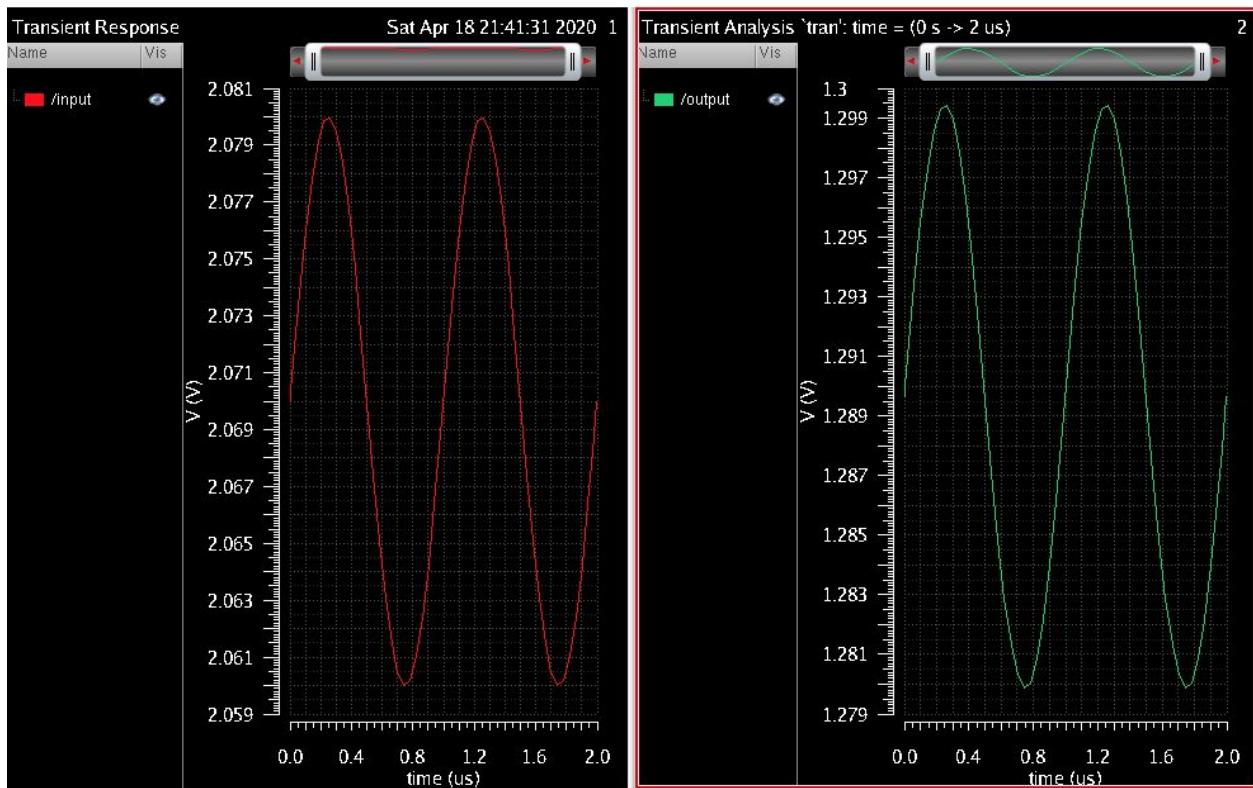
- $gm = \frac{I_c}{V_T} = (1.284/26) = 49m$
- $ro = \frac{V_A}{I_c} = (100/1.284) = 77.88k\Omega$

Percent error:

- $gm \% \text{ error} = 49.61m - 49m / 49.61m * 100\% = 1.23\%$
- $ro \% \text{ error} = 78.87 k\Omega - 77.88 k\Omega / 78.87 k\Omega * 100\% = 1.25\%$

## D.

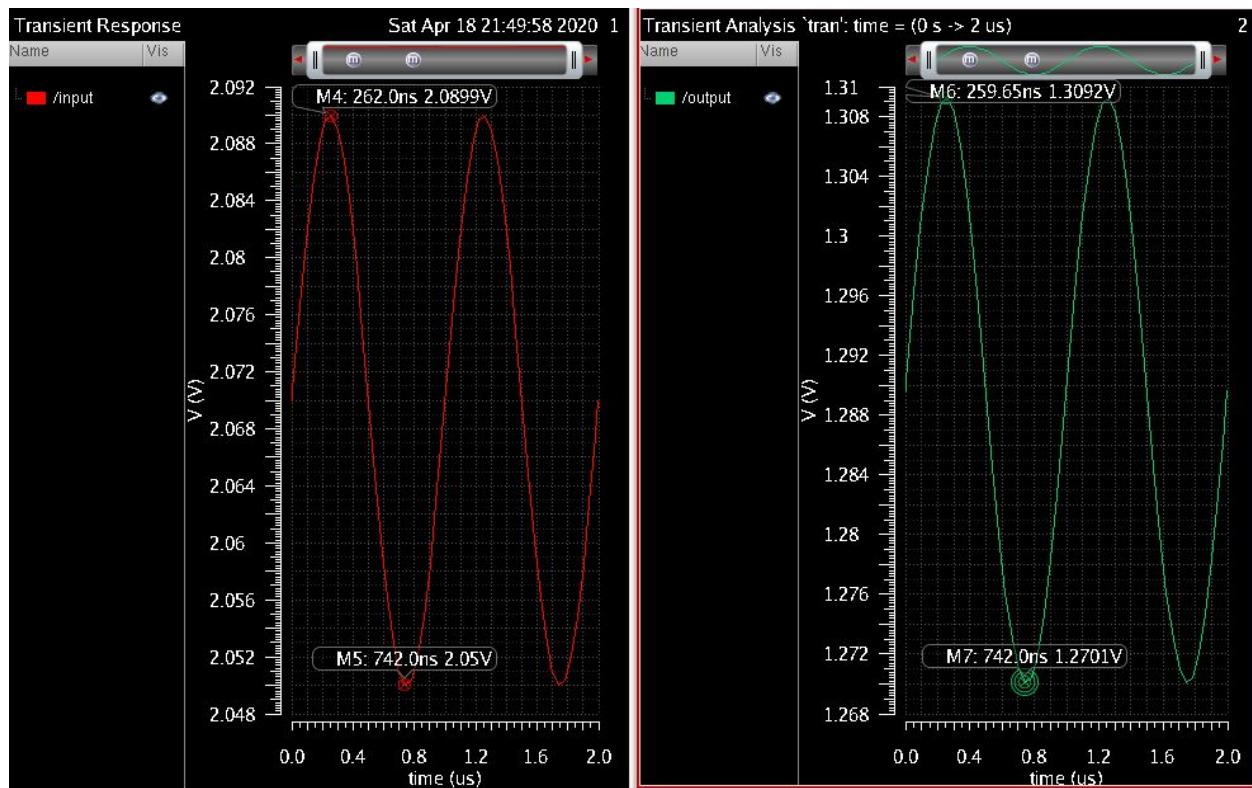
Comparing AC and DC components of Vin and Vout



- DC input level: 2.07V
- DC output level: 1.289V
- Amplitude\_Vin: 19.96mV
- Amplitude\_Vout: 19.56mV
- Gain = Amp\_Vout/Amp\_Vin =  $19.56/19.96 = 0.98$
- DC and AC output levels decrease when adding a sine wave input and the gain is small.

E.

Increase  $V_{in}(eq1)$  by 10mV



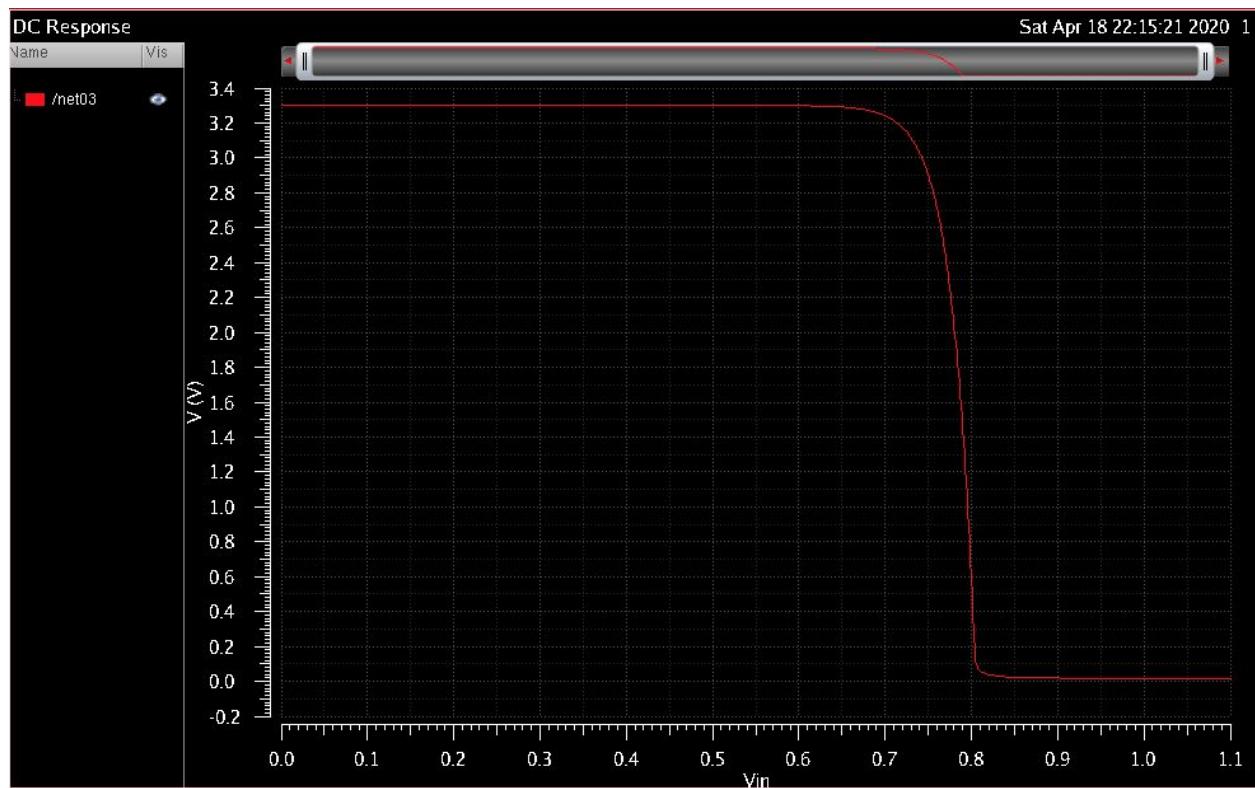
- Increasing the amplitude by 10mV causes the input and output amplitude levels to also increase to 39.92mV and 39.12 mV, respectively. The DC levels remain the same.

## Problem 2

### Common Emitter

**A.**

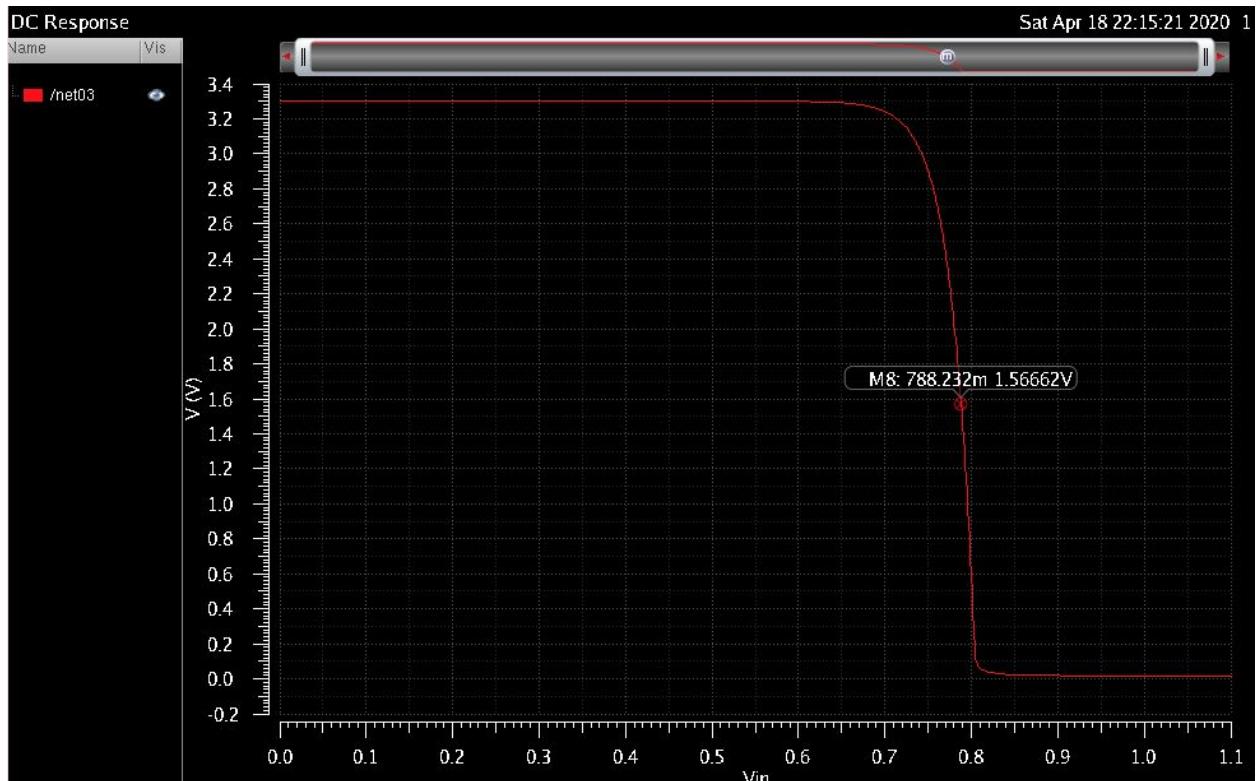
*Vout* vs. *Vin*



- Region of operation (from top to bottom of graph): 1) cutoff, 2) forward active, 3) saturation

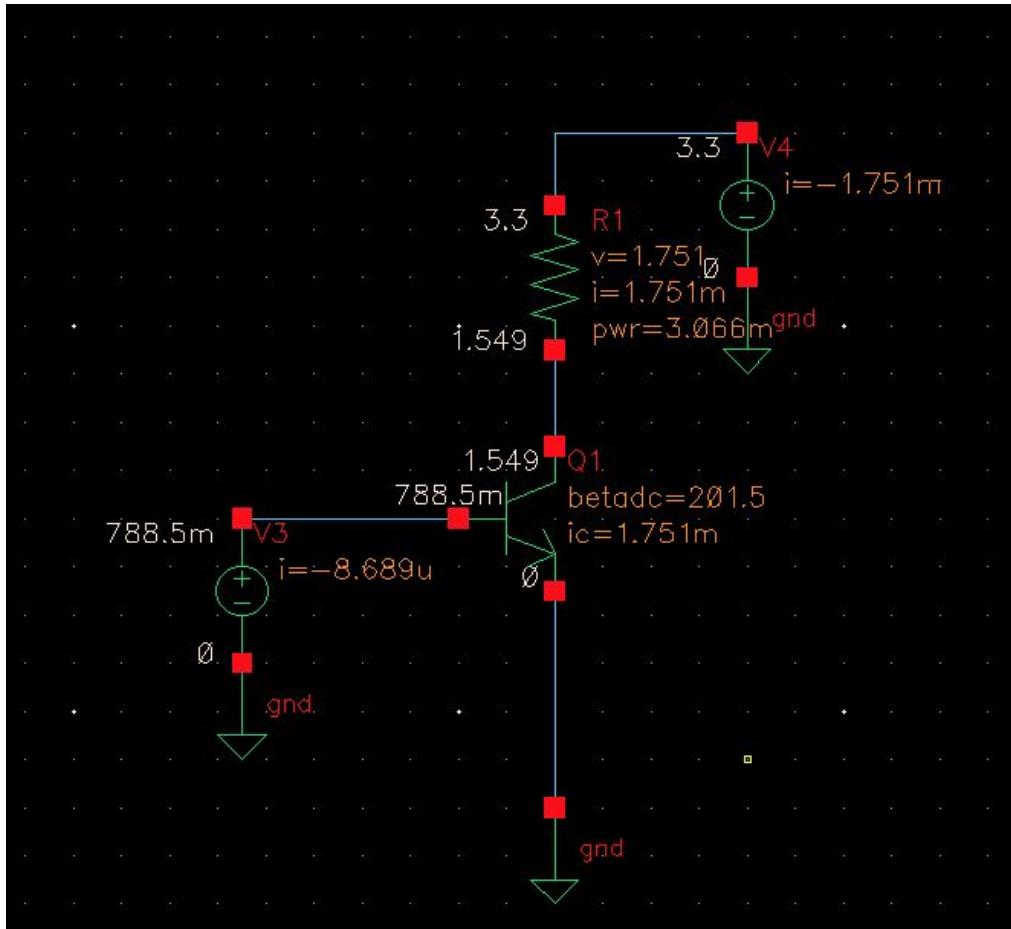
**B.**

$$V_{in} = V_{in(eq2)}$$



- $V_{out} = 1.56V$
- $V_{in} = V_{in(eq2)}: \frac{3.3V - 0.18V}{2} = 1.56V$

### DC Operating Point Analysis



- The transistor is operating in the forward active region since  $I_b > 0$  and  $V_{ce} > 0$ .

### C.

#### Calculations

Small signal parameters from simulation:

- $gm = 67.68m$
- $ro = 57.55k\Omega$

Calculated small signal parameters

- $gm = \frac{I_c}{V_T} = (1.751/26) = 67m$
- $ro = \frac{V_A}{I_c} = (100/1.751) = 57.11k\Omega$

Percent error:

- $gm \% \text{ error} = 67.68m - 67m / 67.68m * 100\% = 1\%$
- $ro \% \text{ error} = 57.55 k\Omega - 57.11 k\Omega / 57.55 k\Omega * 100\% = 0.76\%$

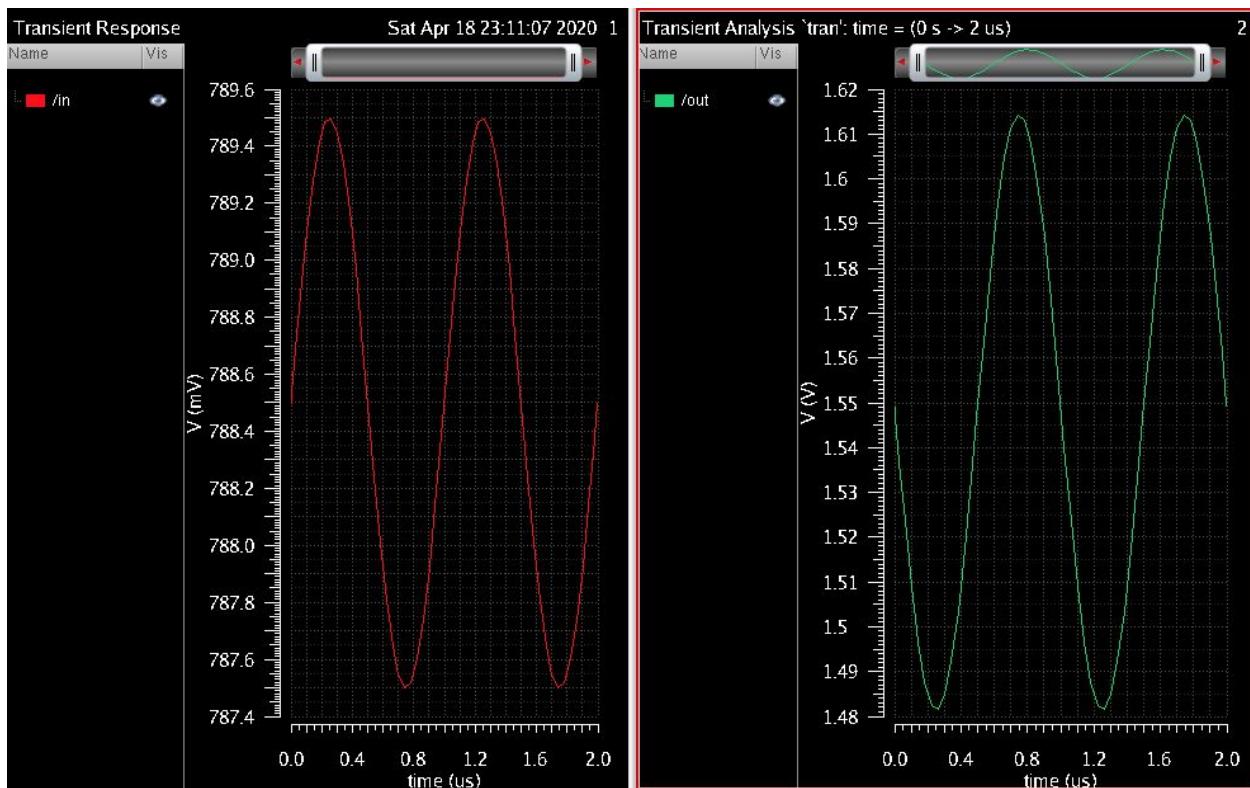
## D.

Gain for common emitter circuit

- $A = -gm \cdot R_c = 67.68m \cdot 1k = \underline{-67.68}$
- Slope  $(3.24-0.136)/(0.698-0.806) = \underline{-28.74}$

## E.

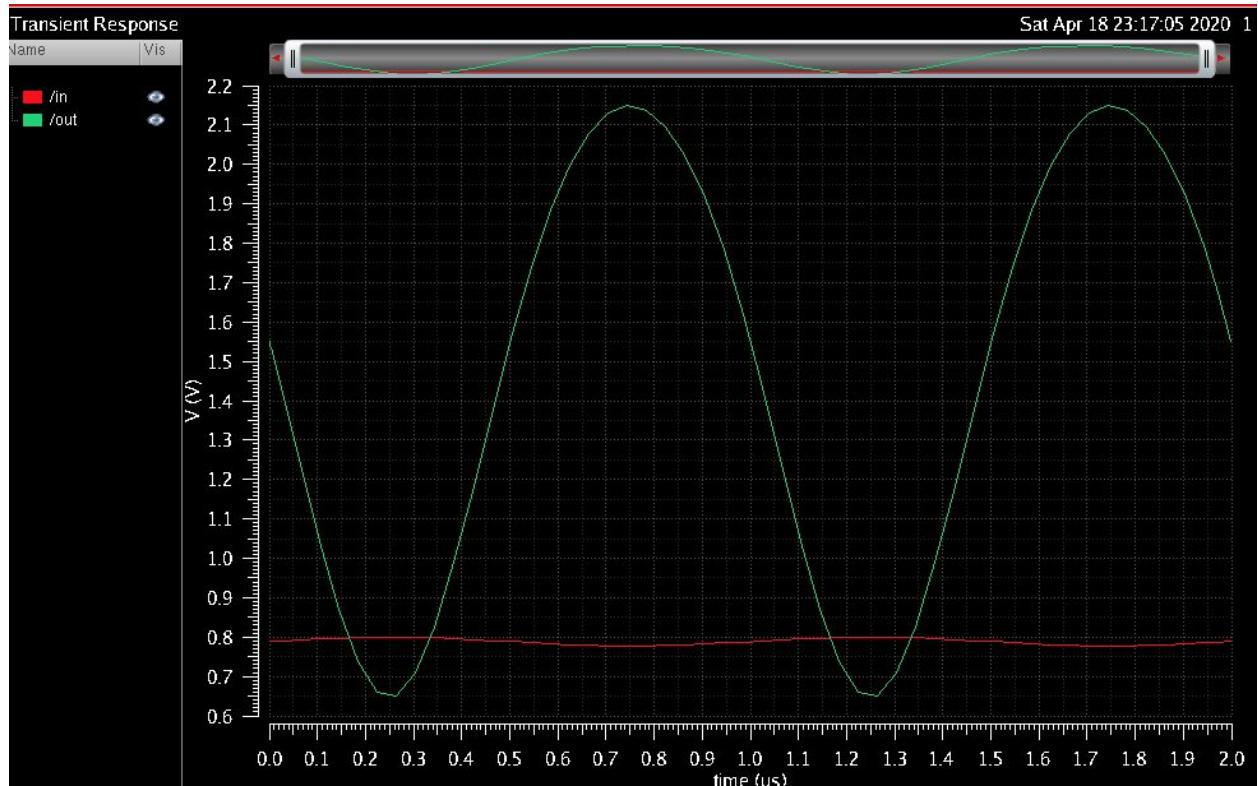
*Comparing AC and DC components of Vin and Vout*



- DC input level: 788.5 mV
- DC output level: 1.54V
- Amplitude\_Vin: 1.996 mV
- Amplitude\_Vout: 132.8mV
- Gain = Amp\_Vout/Amp\_Vin =  $132.8/1.996 = \underline{66.5}$
- DC and AC output levels increase when adding a sine wave input and the gain is high. The amplitude of the input signal is very low compared to the output signal.

## F.

Increase  $V_{in}(eq2)$  by 10mV

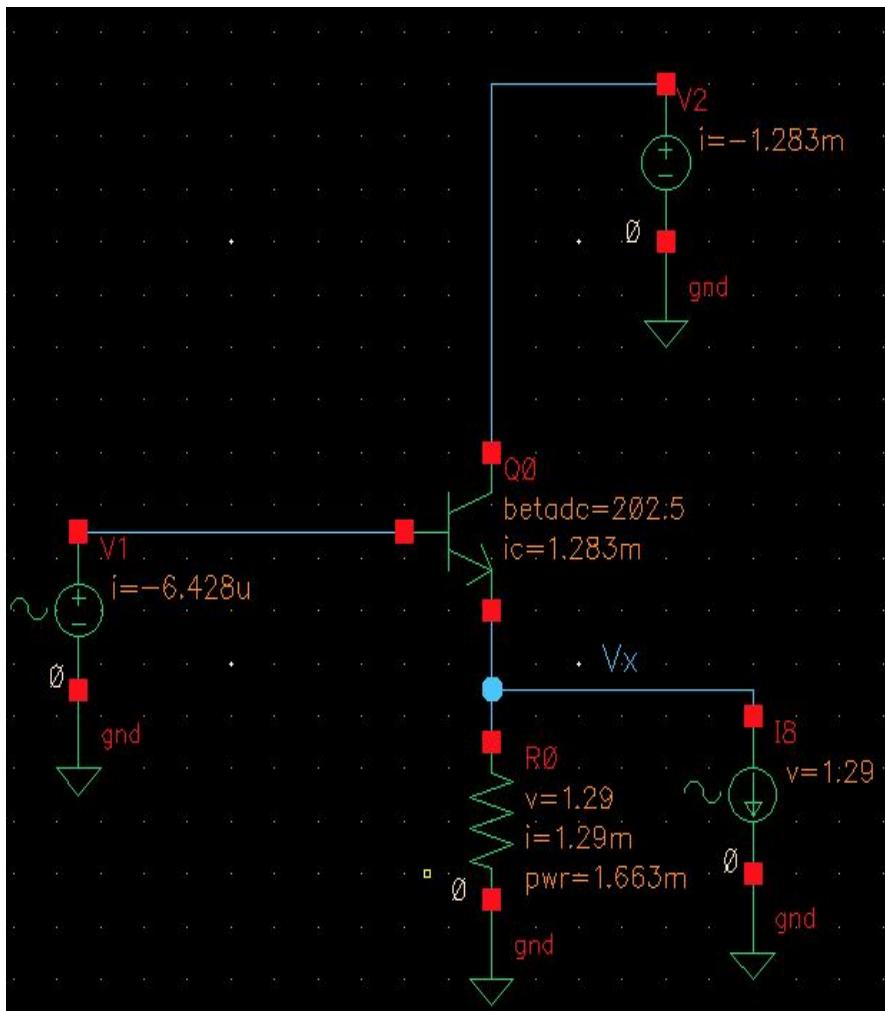


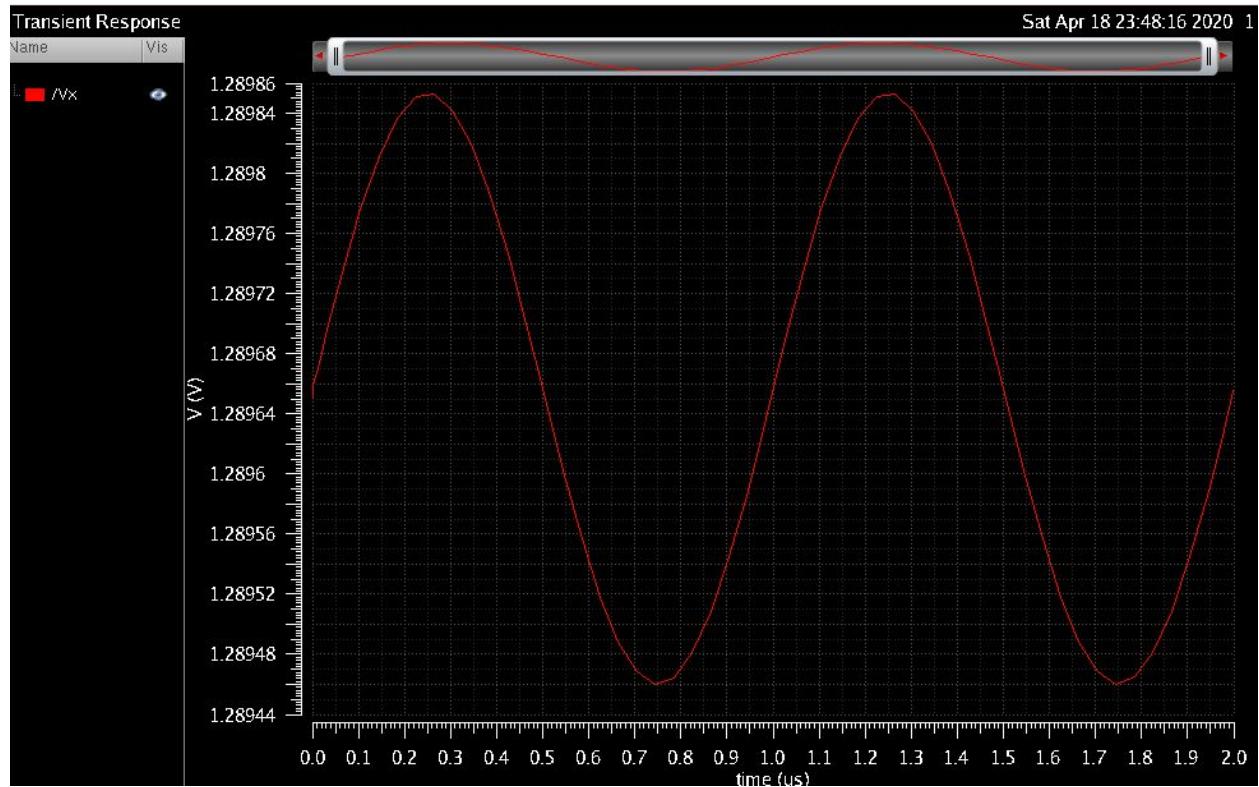
- Increasing the amplitude by 10mV causes the amplitude of the input and output levels to increase. The input amplitude is 21.96mV and output amplitude is 1.499V. The gain is increased to 71.3.

### Problem 3

A.

Calculate  $R_{out}$  for a common collector circuit

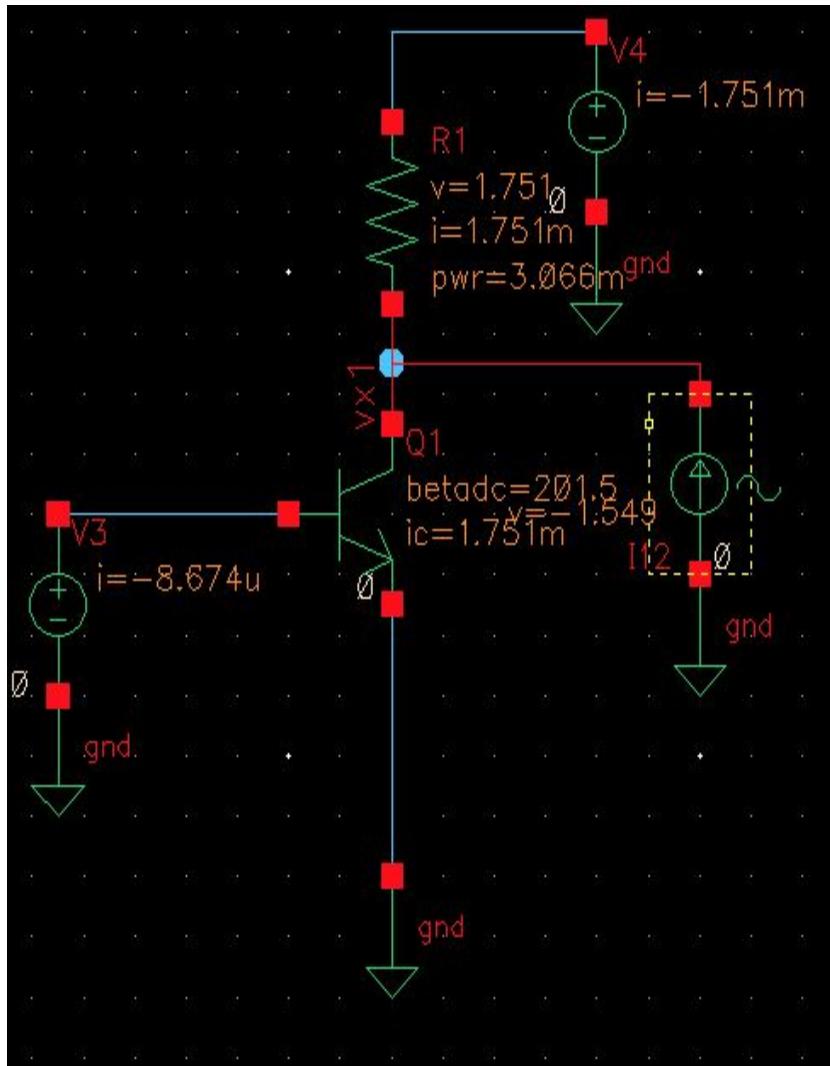


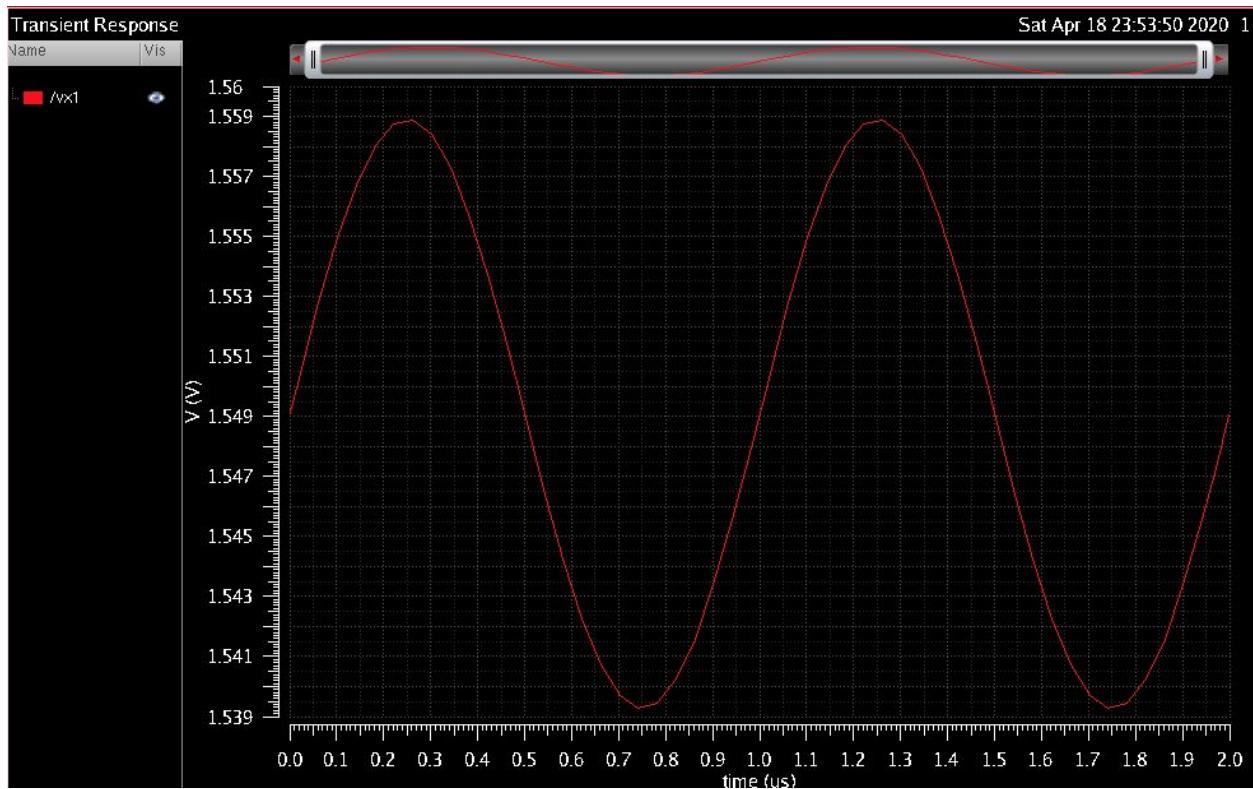


- Rout: Amp\_vx/Amp\_ix
- Amp\_Vx = 392.3u
- Amp\_Ix = 20u
- Rout =  $392.3\text{uV}/20\text{u} = \underline{19.61\Omega}$

**B.**

Calculate  $R_{out}$  for common emitter circuit



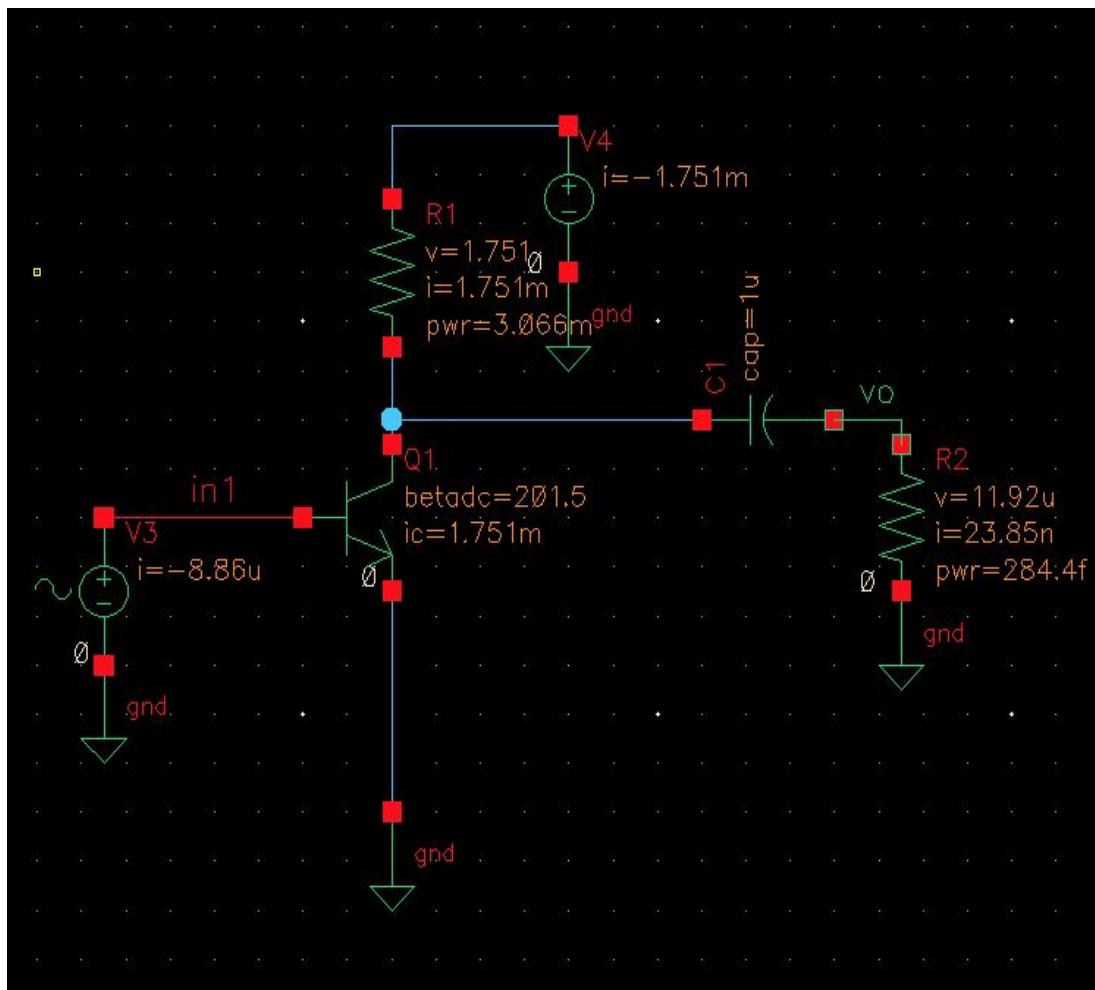


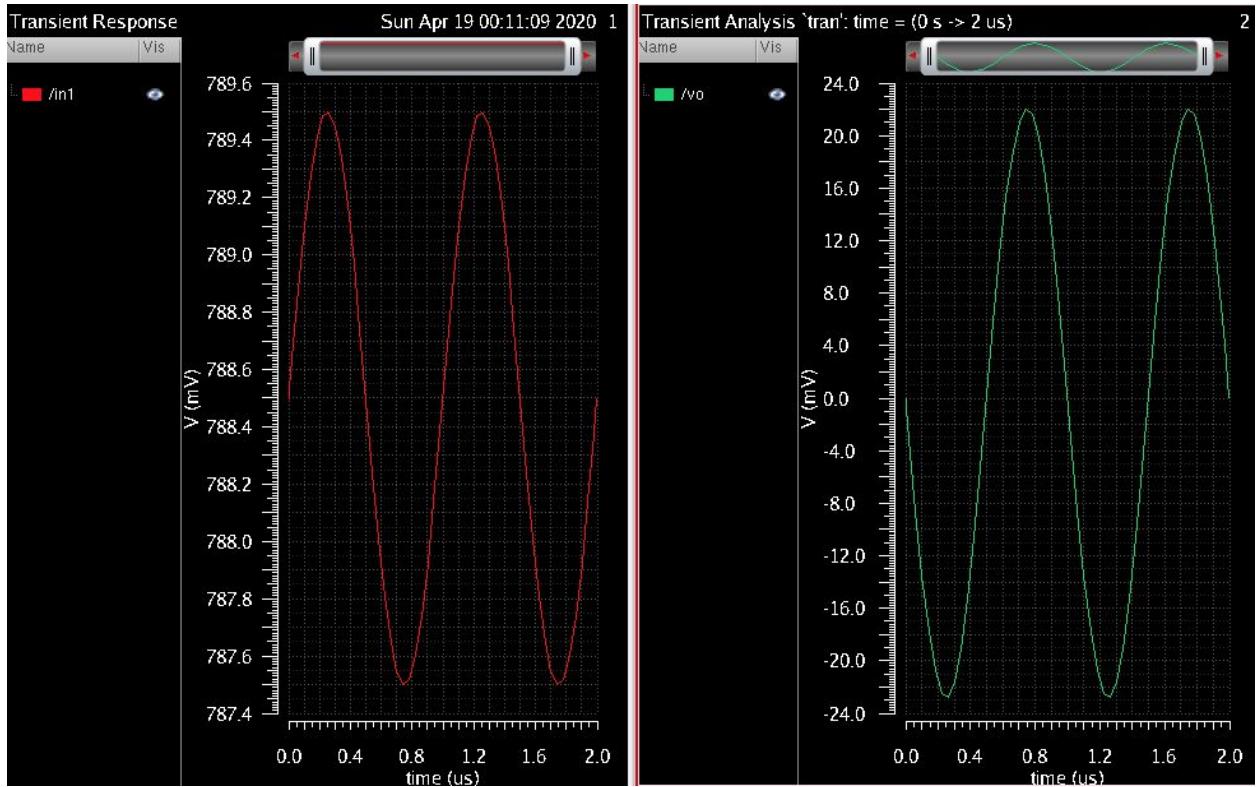
- Rout: Amp vx/Amp\_ix
- Amp\_Vx = 19.62mV
- Amp\_Ix = 20uA
- Rout = 19.62mV/20uA = 981k

## Problem 4

A.

Small-signal gain  $V_{out}/V_{in}$

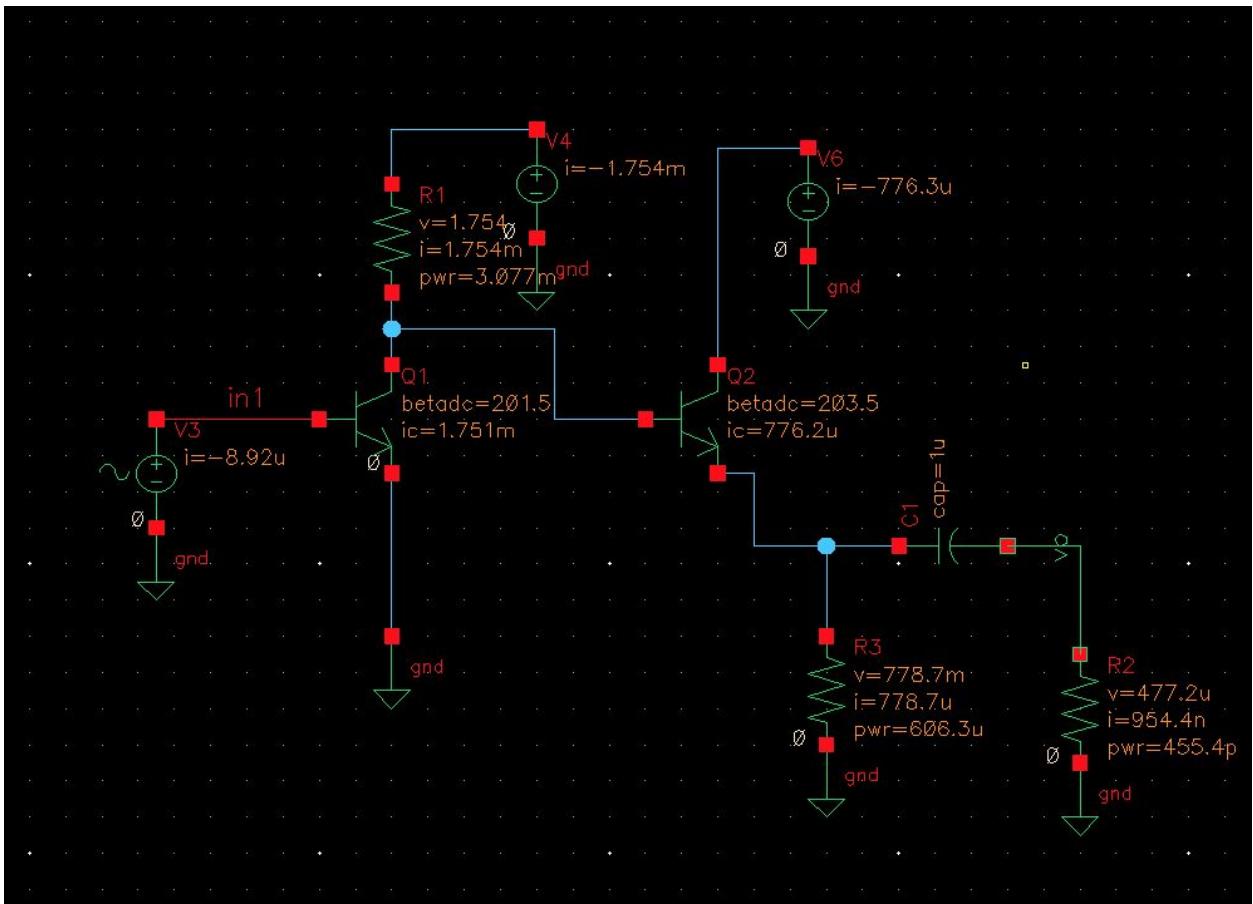


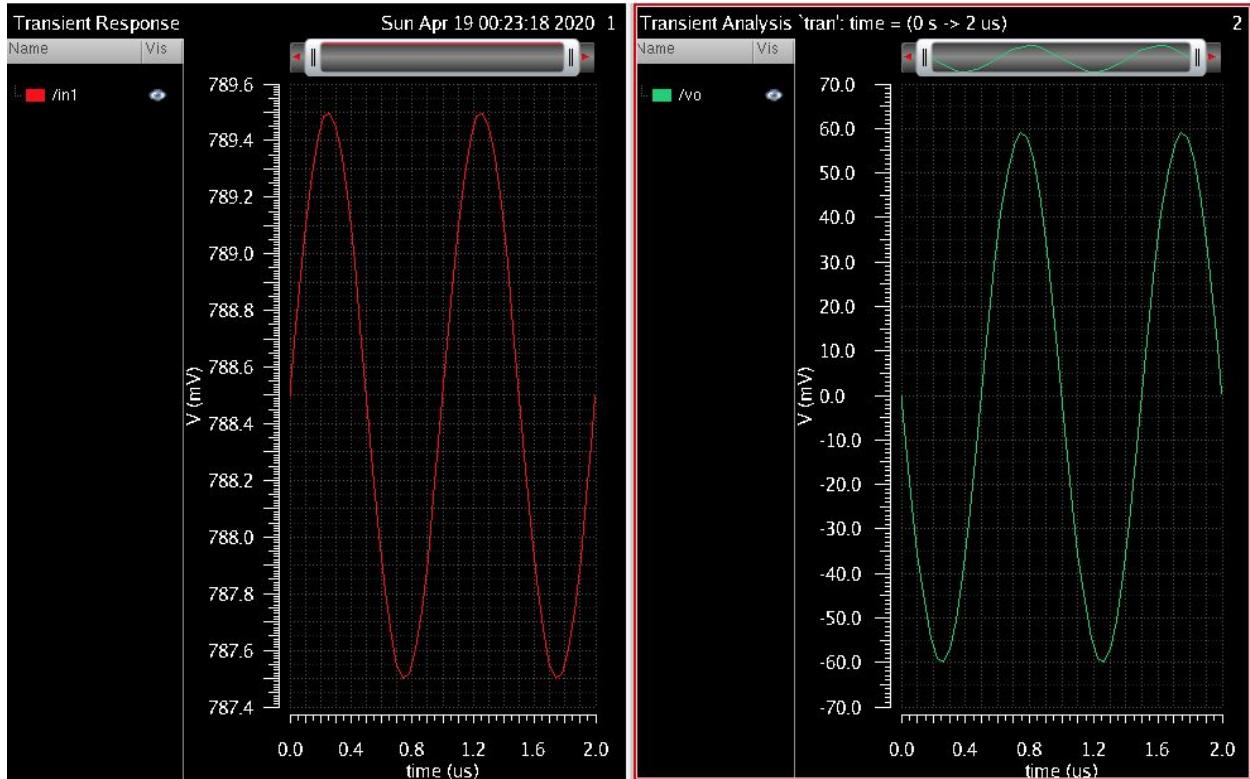


- $A = gm^* (R_C \parallel R_o \parallel R_L)$
- $Amp_{vout} = 44.78\text{mV}$
- $Amp_{vin} = 1.996\text{mA}$
- $A = 44.78\text{mV}/1.996\text{mA} = \underline{\underline{22.43}}$

B.

*Small signal gain  $V_{out}/V_{in}$  for two stage amplifier*





- $A_{vout}=119\text{mV}$
- $A_{vin}=1.996\text{mA}$
- Gain =  $119\text{mV}/1.996\text{mA} = \underline{59.6}$  which is a lot higher than previous one-stage amplifier

## Conclusion

The effects of each circuit were observed with both DC and AC sources. With the DC sources, the operating point was determined along with the calculations for the small-signal parameters. Adding an AC source demonstrates what happens to the input and output levels. For the common collector, the DC and AC output levels decreased when adding a sine wave input and the gain is small. On the other hand, the common emitter had increased output levels when adding a sine wave input and the gain is high. For both circuits, increasing the amplitude increases the gain. The value of  $R_{out}$  is determined by adding a test source to the output and calculating the peak to peak value of the test voltage and current. For the last part, a capacitor was added to observe the gain of a one stage and two stage amplifier. Compared to the one stage amplifier, the gain in the two stage amplifier is almost tripled. This is due to the buffer stage in the circuit which prevents  $R_L$  from loading the amplifier.

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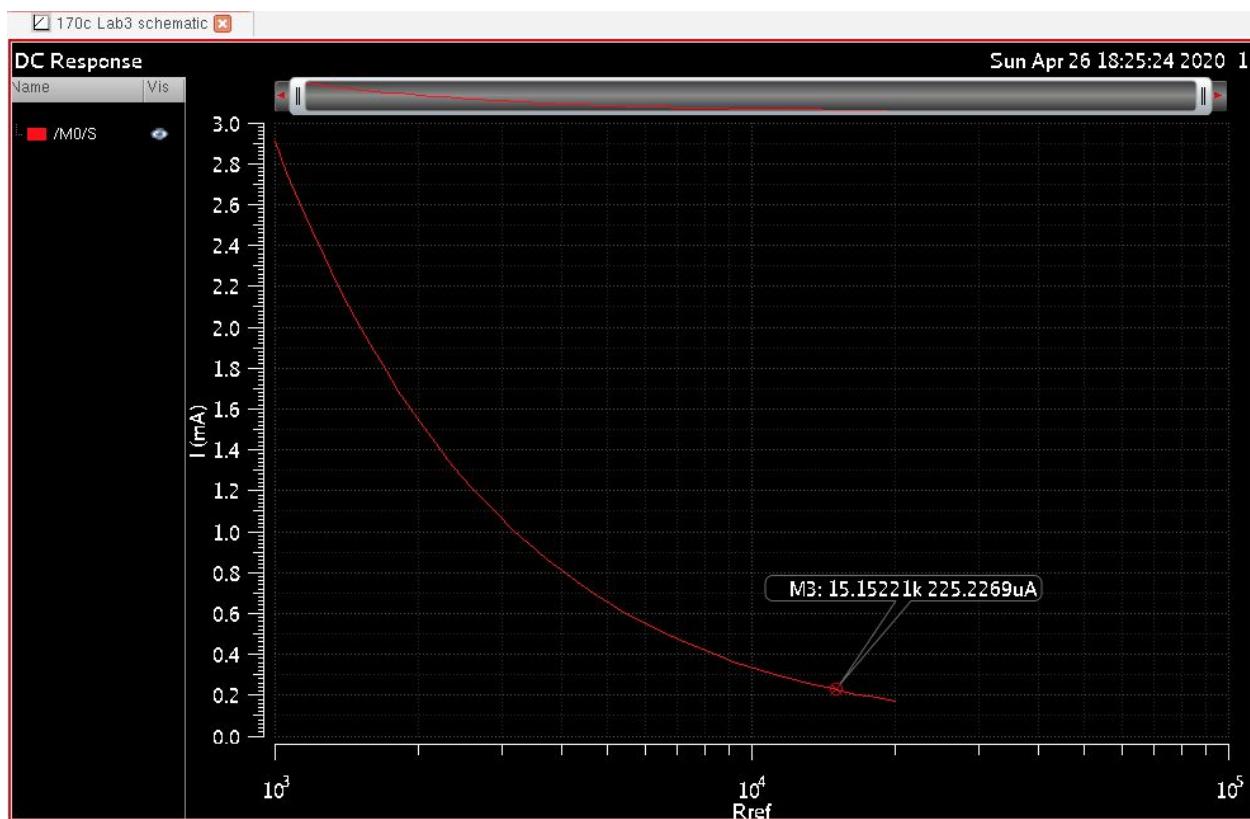
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Lab 3

4/28/2020

## SIM 1

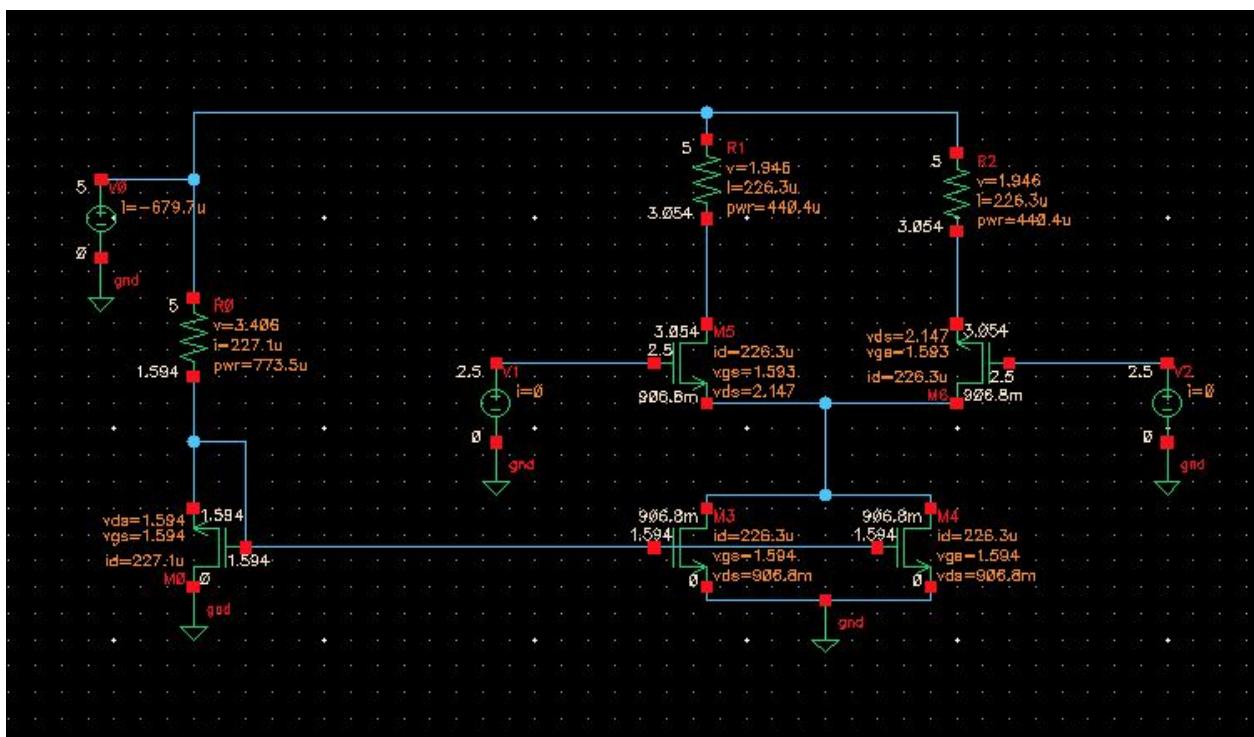
*Rref Sweep*



Calculations before simulation:

- $I(M_d) = \frac{1}{2} \mu C_{ox} (W/L) (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$ 
  - $225\mu A = \frac{1}{2} (0.6e-3)(200\mu m/10\mu m)(V_{gs}-1.4)^2(1+0.005V_{gs})$ 
    - **$V_{gs} = 1.6V$**
- $I(M_d) = V_{dd} - V_{gs}/R_{ref}$ 
  - $V_{dd} = 5V$
  - $5V - 1.6V/R_{ref}$ 
    - **$R_{ref} = 15.1k\Omega$**

- Transistor is in saturation
  - $V_{ds} > V_{gs} - V_t$
  - $V_d - V_s > 2.5V - V_s - 1.4V$ 
    - $V_d > 1.1V$
- DC operating point
  - $V_{out(dc)} = [V_{dd} + V_d(\min)]/2 \rightarrow (5V + 1.1V)/2$ 
    - $V_{out(dc)} = 3.05V$
- $R_d$  value
  - $(5V - 3.05V)/225\mu A$ 
    - $R_d = 8.66k\Omega$



Calculations after simulation:

- Differential Mode Gain =  $-gmR_d = -2IdR_d/V_{gs}-V_t$ 
  - $[-2(226.3\mu A)(8.66k\Omega)]/(1.593-1.4)$ 
    - $Adm = -20.16$

- Common Mode Gain =  $- \frac{gmR_d}{1+gmro} = - \frac{(2IdR_d/V_{gs}-V_t)}{(1+(2Id/V_{gs}-V_t)(1/\lambda Id))} = - \frac{(2IdR_d/V_{gs}-V_t)}{(1+(2/V_{gs}-V_t)(1/\lambda))}$ 
  - $- 20.30/1037$

**■  $A_{cm} = -0.019$**

## SIM 2



- Input voltage range: -113mV to 112mV
- Output voltage range: 4.87V to 1.24V
- Slope (Green curve):  $y_2-y_1/x_2-x_1 = (4.87-1.22)/(0.112+0.113) = 16.22$
- Slope (Red curve):  $y_2-y_1/x_2-x_1 = (1.24-4.87)/(0.111+0.112) = -16.27$
- The values for the slope were close to the calculated value for differential-mode gain.
  - Calculated Value: **-20.16**

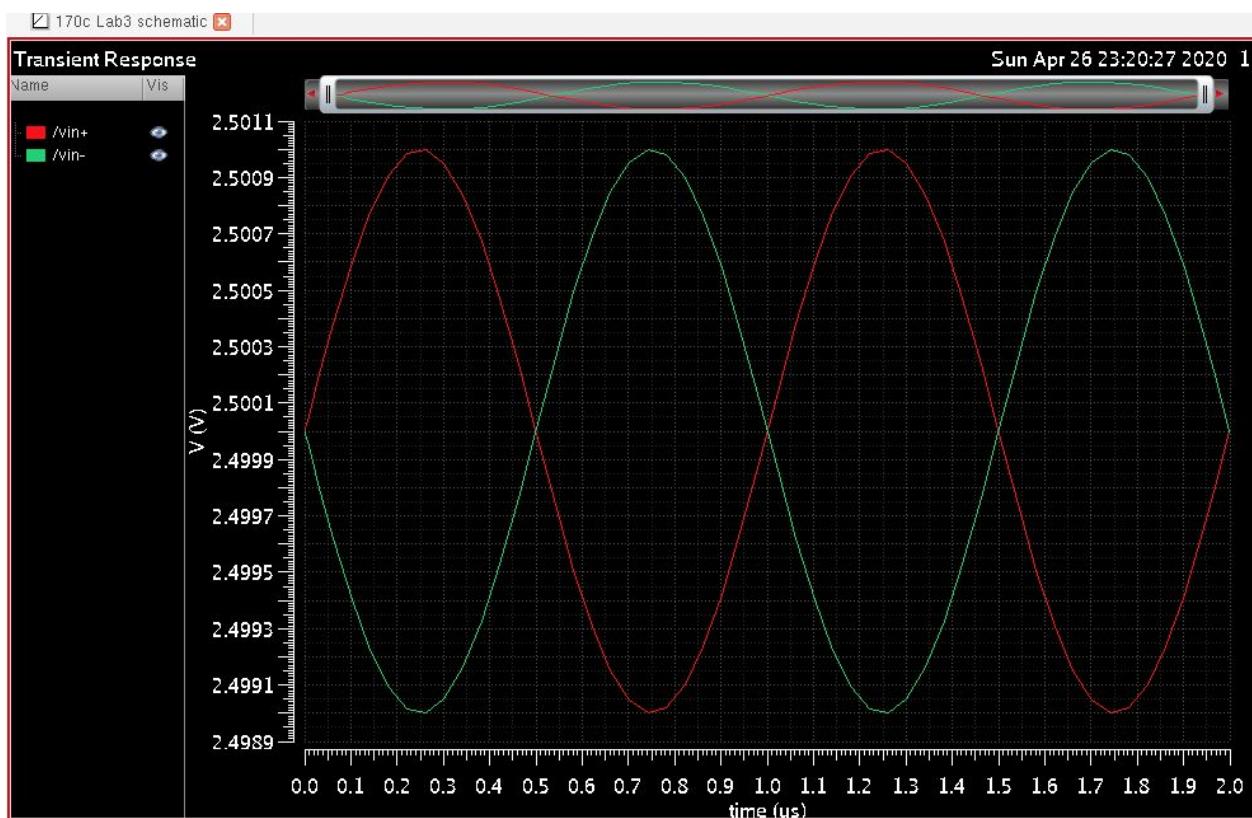
### SIM 3



- Input voltage range: -999mV to -696mV
- Output voltage range: 4.64V to 3.06V
- Slope (Green curve):  $y_2-y_1/x_2-x_1 = (3.06-4.64)/(-0.696+0.999) = -5.21$
- Slope (Red curve):  $y_2-y_1/x_2-x_1 = (3.06-4.64)/(-0.712+0.999) = -5.50$
- The values for the slope were significantly lower than the common-mode gain that was calculated.
  - Calculated Value: **-0.019**

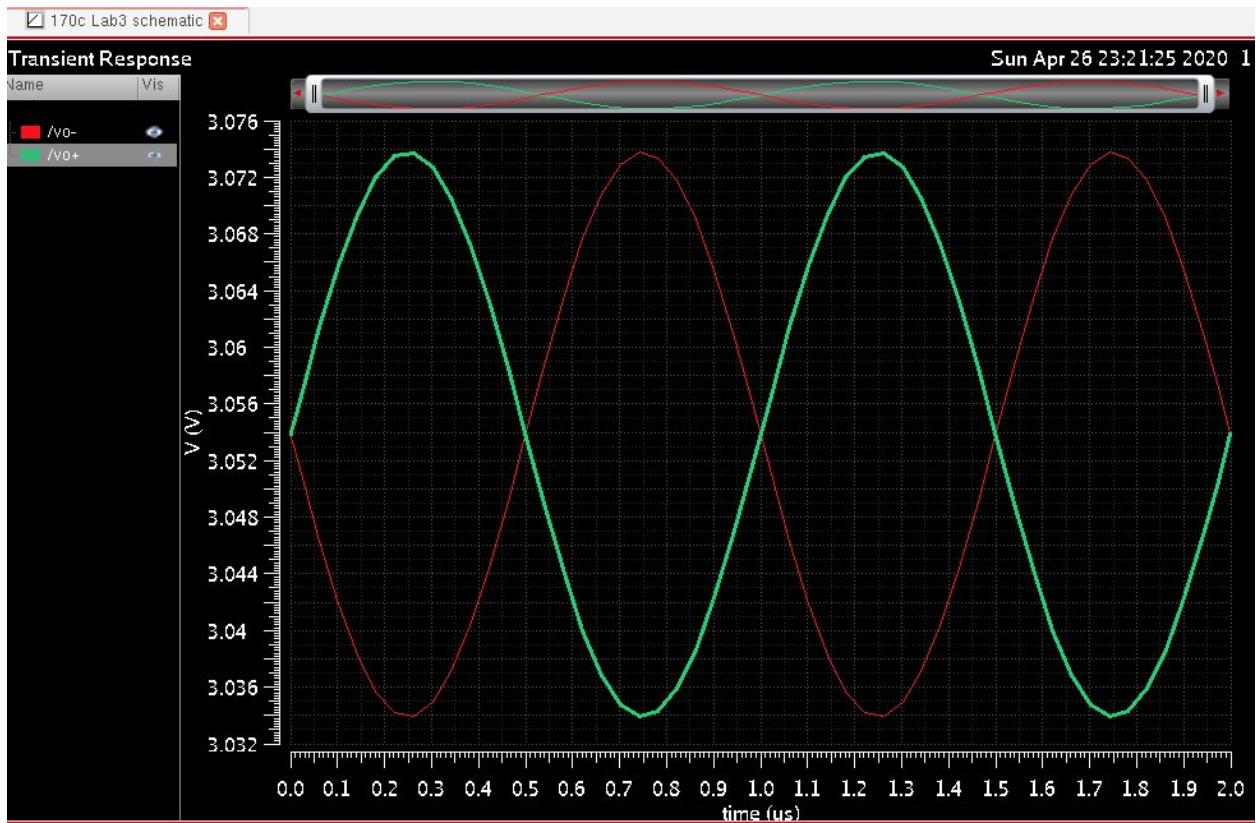
## SIM 4

### Differential Inputs



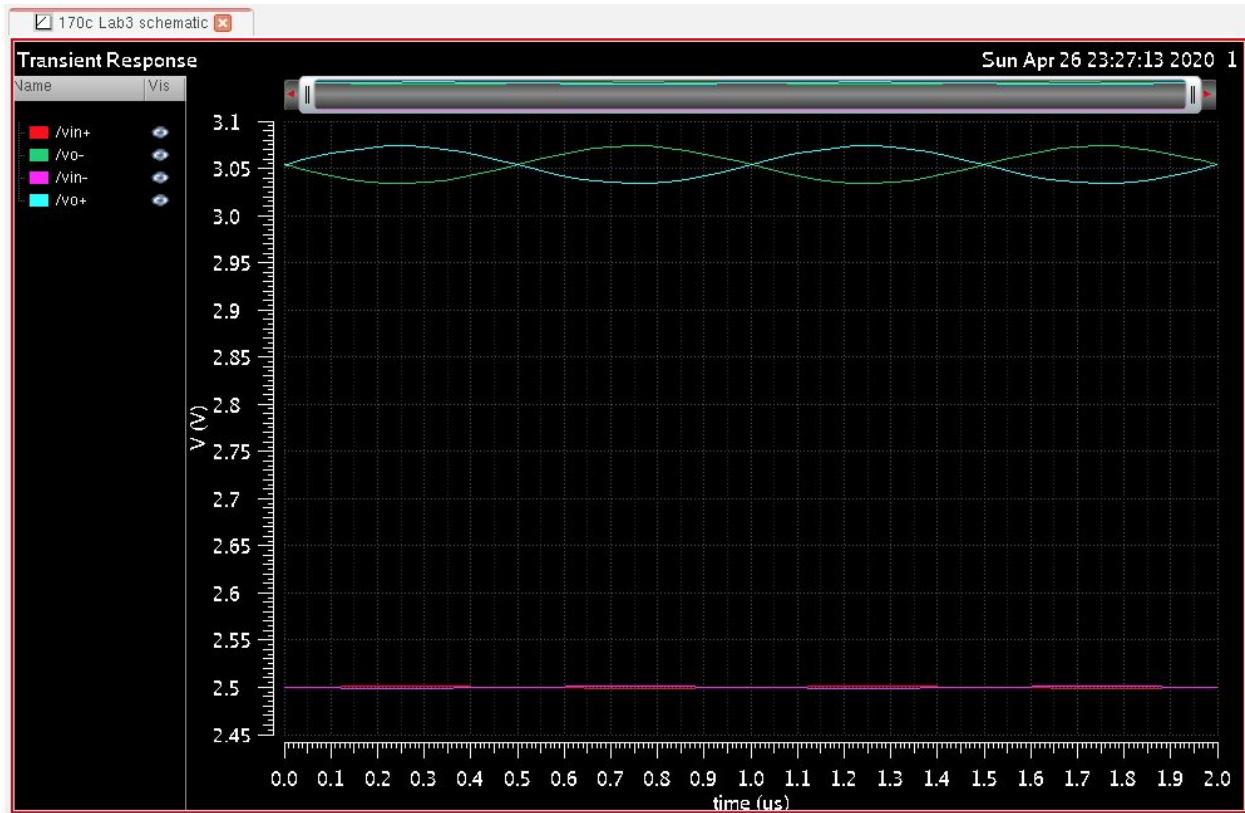
- DC value at 2.5 V

## Differential Outputs



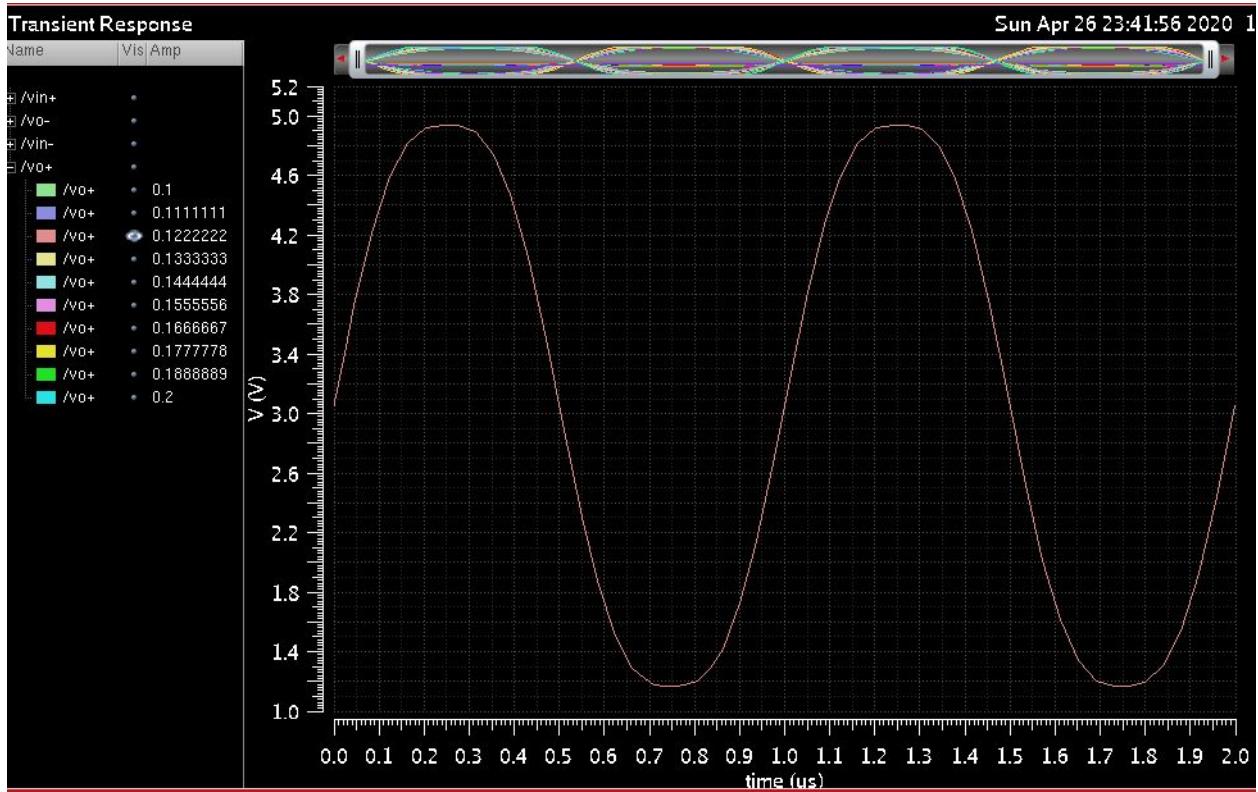
- DC value at 3.05V

## Differential-mode Input and Output



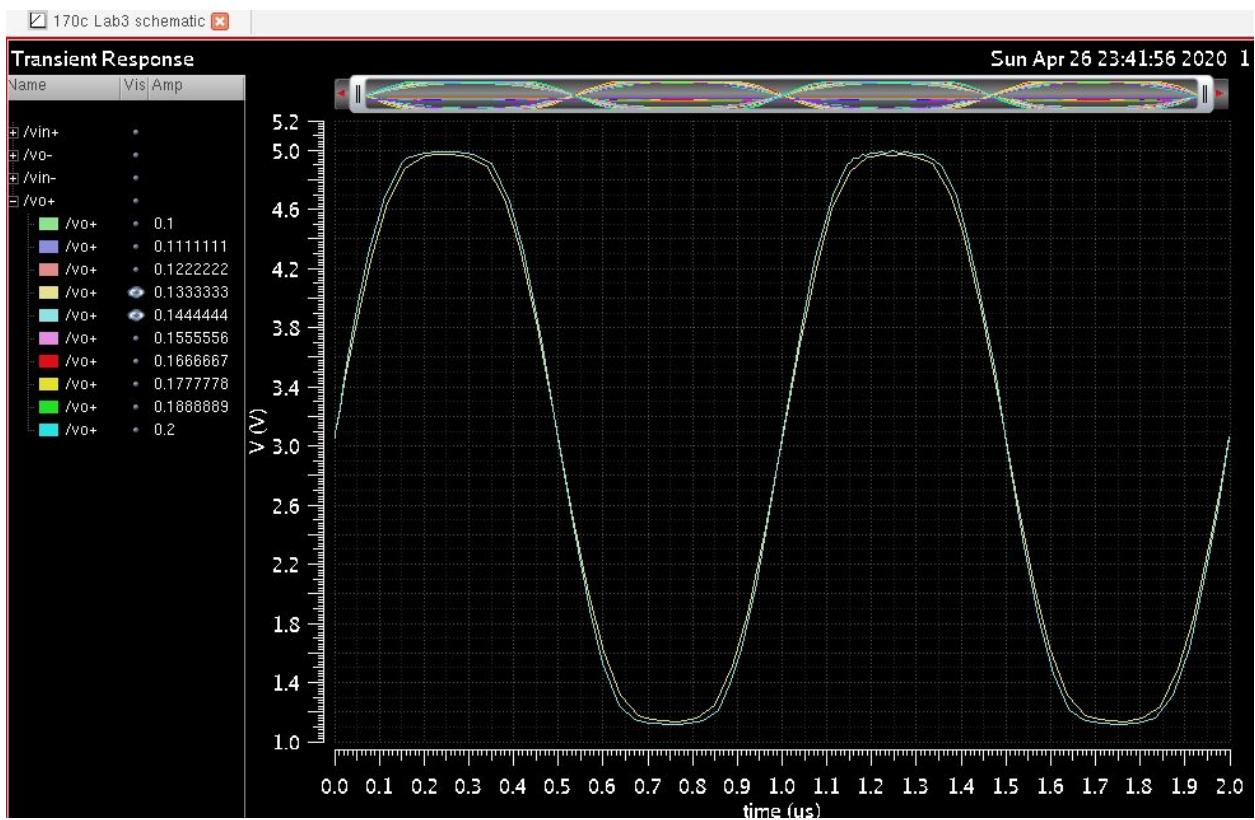
- Differential output gain is significantly higher than the input gain.

## Maximum Amplitude



- The maximum amplitude for which the differential mode output looks sinusoidal is at 122mV.

## Increasing Amplitude



- When the amplitude is increased higher than its maximum value, the output waveform starts to clip. This means the transistor is no longer in the saturation region.

## Conclusion

In this lab, we were asked to design a CMOS differential amplifier. The reference resistor value was determined from  $I(M_d)$ ,  $V_{dd}$ , and  $V_{gs}$ . The DC operating point was determined from the maximum and minimum values that kept the transistor in saturation. The value of  $R_d$  was calculated from the DC operating point. Differential and common mode gains were calculated and confirmed with simulation results. The slope for the differential-mode input and output was close to the calculated value however, the calculated value for the common mode gain was significantly higher than the slope. Adding a differential sine wave to the inputs produced outputs with much higher gain. The output waveform begins to clip when the amplitude is above 122mV. This implies the region of operation has changed in the transistor.

Safia Reazi

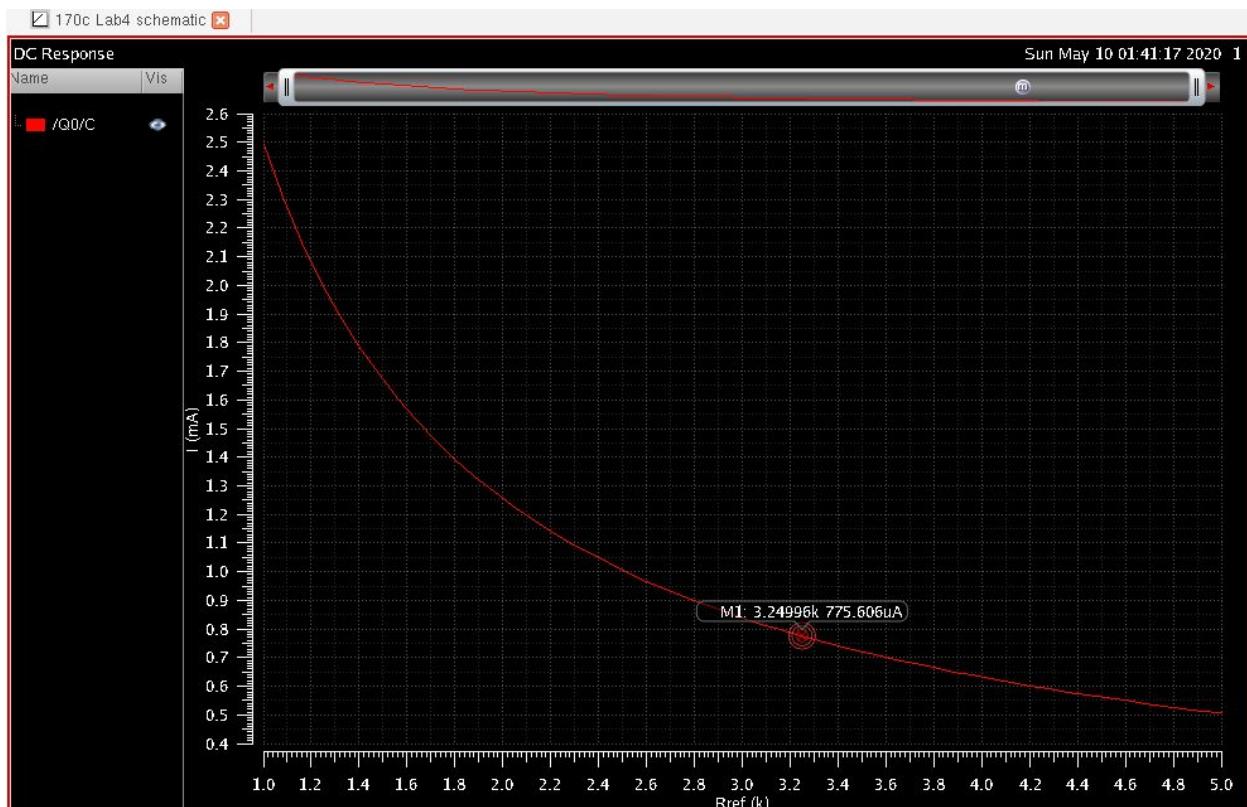
170LC

Lab 4

5/12/2020

## SIM 1

### Rref Sweep



Calculations before simulation:

- $I_c = \frac{1}{2} * I_{ee}$ 
  - $\frac{1}{2} * 1.5\text{mA}$ 
    - **$I_c = 0.75 \text{ mA}$**
- $R_{ref} = V_{cc} - V_{be(on)} / I_c$ 
  - $V_{cc} = 3.3\text{V}$
  - $3.3\text{V} - 0.7\text{V} / 0.75\text{mA}$ 
    - **$R_{ref} = 3.5\text{k}\Omega$**

- Emitter Voltage
  - $V_e = V_b - V_{be}$
  - $1.5V - 0.7V$

■  **$V_e = 0.8V$**

- Transistor is in forward active
  - $V_{ce} \geq V_{ce,sat}$
  - $V_{ce,sat} = 0.2V$
  - $V_c - V_e \geq 0.2V; V_c=V_o$
  - $V_o - 0.8V \geq 0.2V$

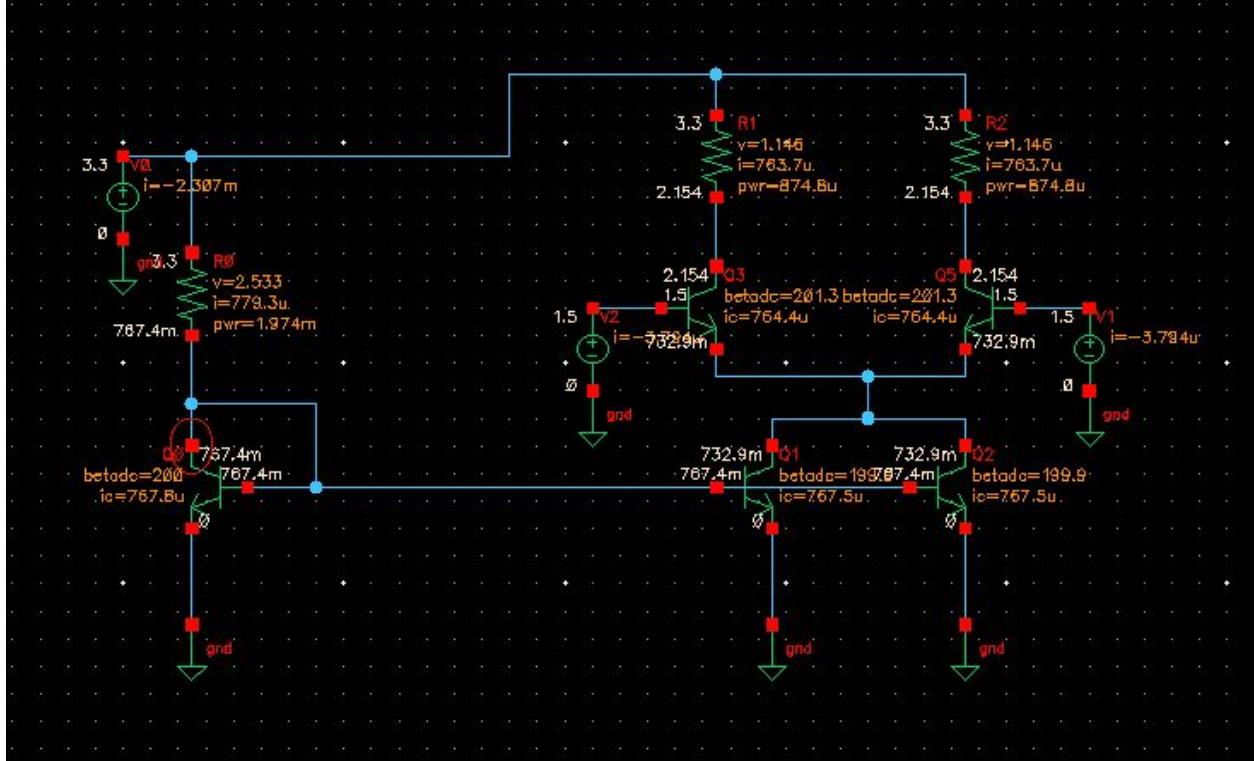
■  **$V_o > 1V$**

- DC operating point
  - $V_{out(dc)} = [V_{dd} + V_o]/2 \rightarrow (3.3V + 1V)/2$

■  **$V_{out(dc)} = 2.15V$**

- $R_c$  value
  - $(3.3V - 2.15V) / 0.75mA$

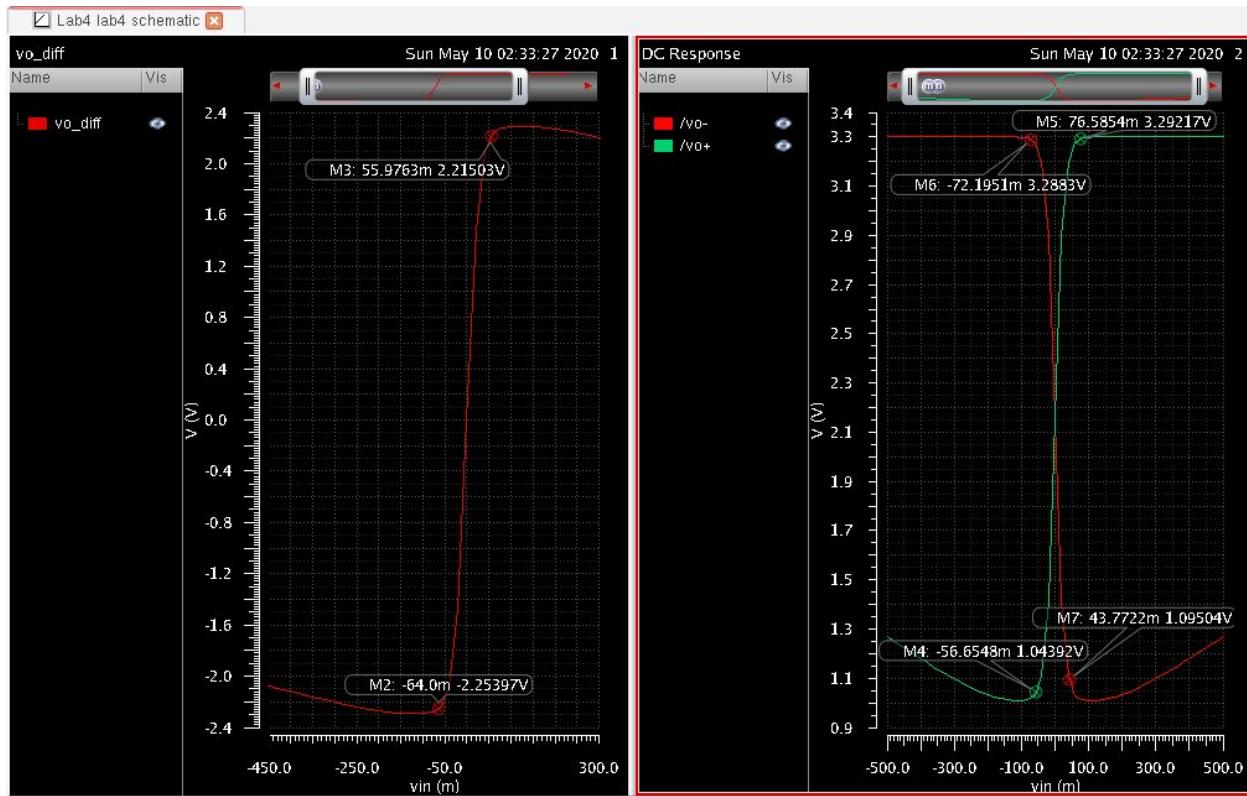
■  **$R_c = 1.5k\Omega$**



Calculations after simulation:

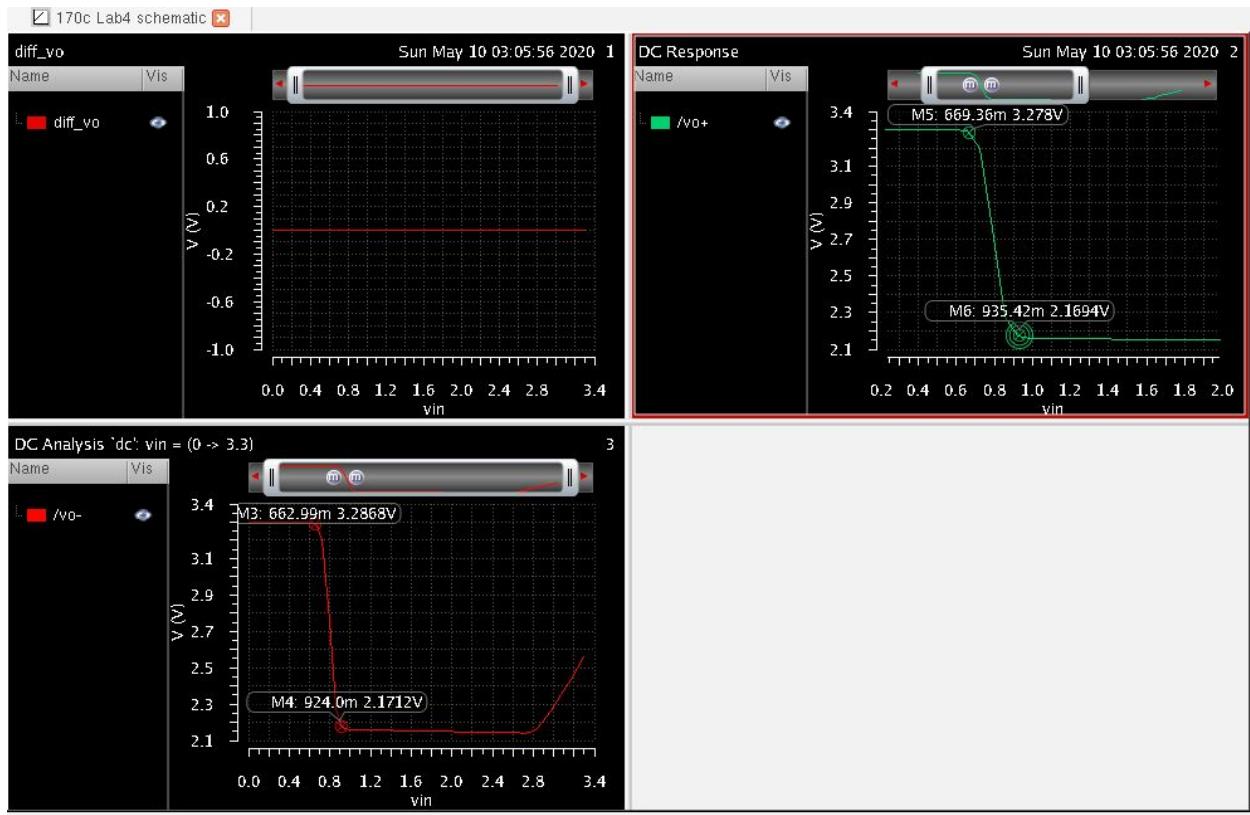
- Differential Mode Gain =  $-gmRc$ 
  - $(-29.55mS)(1.5k\Omega)$ 
    - **Adm = -44.3**
- Common Mode Gain =  $- gmRc/1+gmRee = - gmRc/1+gmro$ 
  - $(-29.55mS)(1.5k\Omega)/1 + (29.55mS)(130.2k\Omega)$ 
    - **Acm = -0.011**

## SIM 2



- Input voltage range: -56.65mV to 76.58mV
- Output voltage range: 3.28V to 1.09V
- Slope (vo\_diff):  $y_2-y_1/x_2-x_1 = (2.21V+2.25V)/(55.97mV+64mV) = 37.17$
- The value for the slope is slightly different from the calculated value for differential-mode gain.
  - Calculated Value: **-44.3**

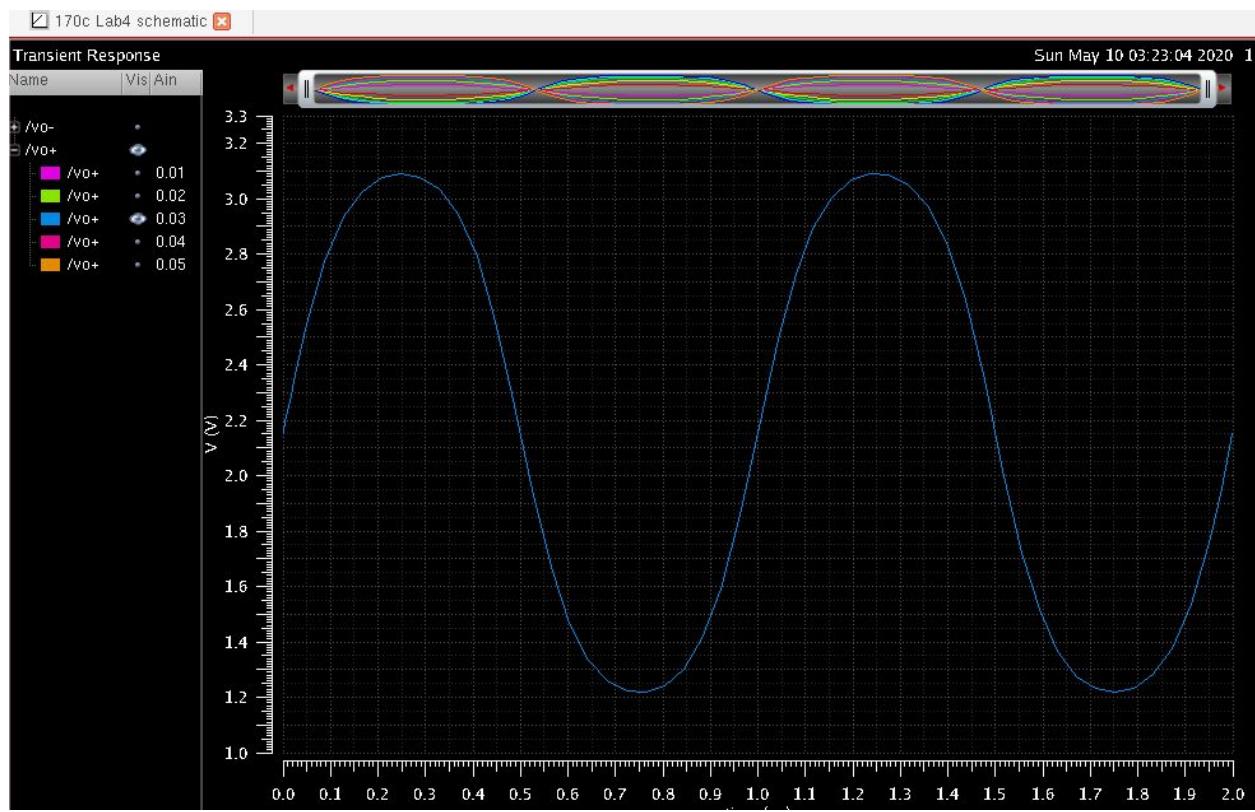
### SIM 3



- Input voltage range: 669.3mV to 935.4mV
- Output voltage range: 3.28V to 2.17V
- Slope (diff<sub>-</sub>vo):  $y_2 - y_1 / x_2 - x_1 = 0$
- The value for the slope is close to the calculated value for the common-mode gain.
  - Calculated Value: **-0.011**

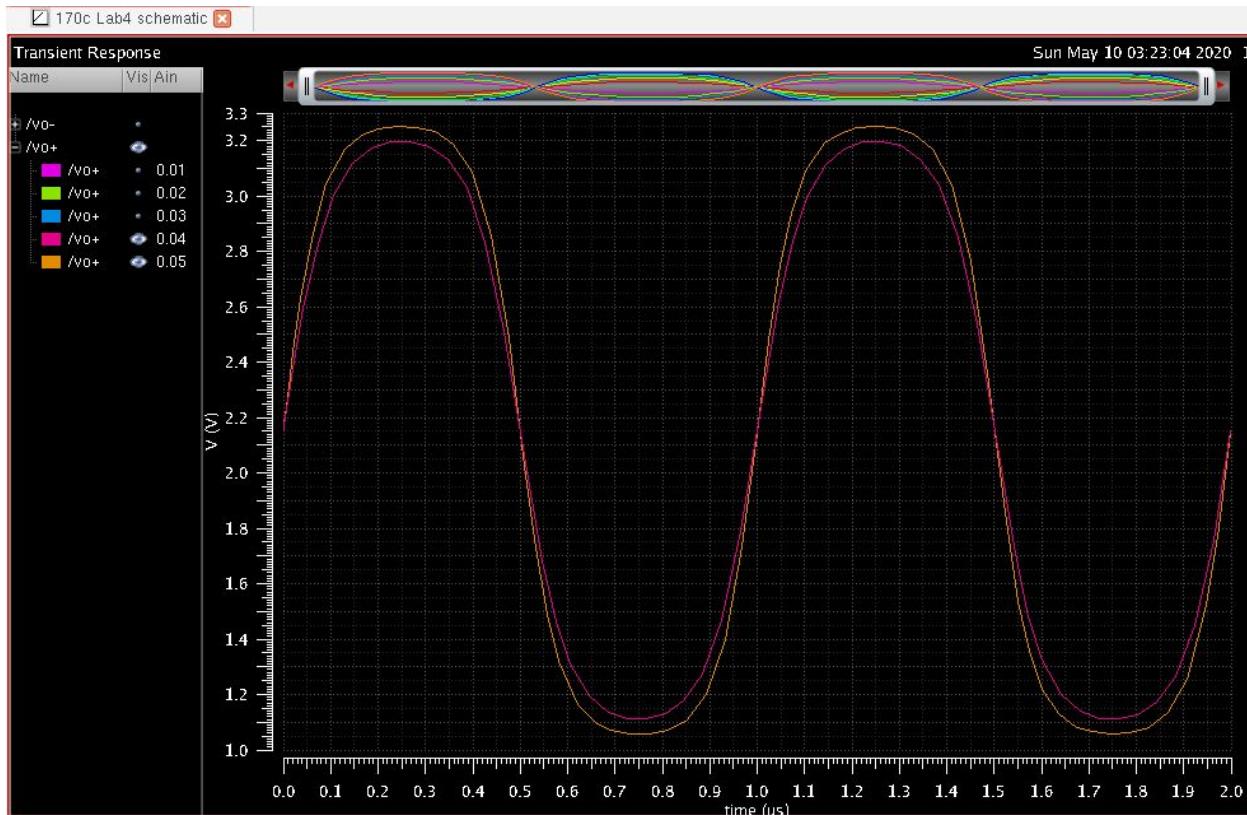
### SIM 4

### *Maximum Amplitude*



- The maximum amplitude for which the differential mode output looks sinusoidal is at 30V.

### *Increasing Amplitude*



- When the amplitude is increased higher than its maximum value, the output waveform starts to clip and looks more like a square wave.

## Conclusion

In this lab, we were asked to design a BJT differential amplifier. The reference resistor value was determined from  $I_c$ ,  $V_{cc}$ , and  $V_{be(on)}$ . The DC operating point was determined from the maximum and minimum values that keep the transistor in forward active. The value of  $R_C$  was calculated from the DC operating point. Differential and common mode gains were calculated and confirmed with simulation results. The slope for the differential-mode was somewhat close to the calculated value however, the calculated value for the common mode gain was more precise. Adding a differential sine wave to the inputs allowed us to determine the maximum amplitude for which the output looks sinusoidal. The output waveform begins to clip when the amplitude is above 30V and begins to look more like a square wave.

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Lab 5

5/26/2020

## SIM 1

*Value of Rd*

- $R_d = (V_{dd} - V_{out})/I_d$ 
  - $R_d = (5V - 2.5V)/200 \mu A$ 
    - **$R_d = 12.5k\Omega$**

*Transistor width*

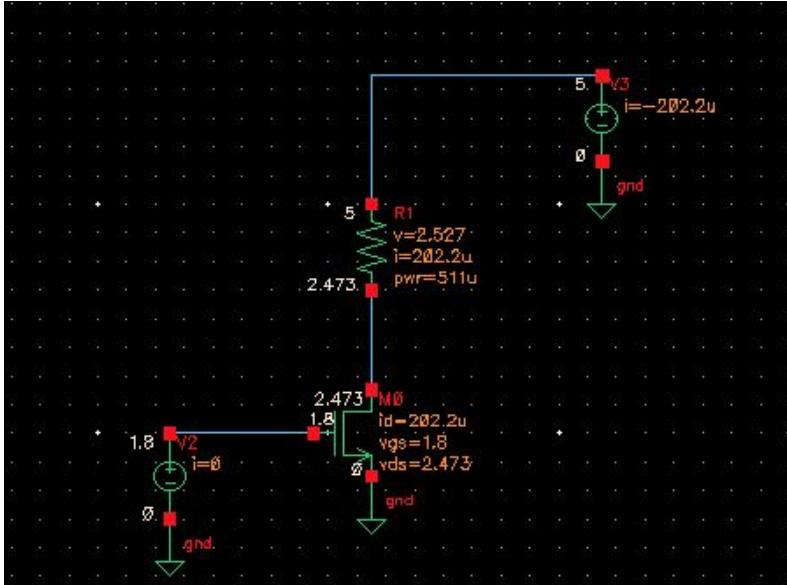
- $I_d = \frac{1}{2} \mu C_{ox}(W/L)(V_{gs}-V_t)^2$ 
  - $200 \mu A = \frac{1}{2} (0.6m)(W/L)(1.8V-1.4V)^2$
  - $L = 2 \mu m$
  - $W/L = 4.16 \mu m$ 
    - **$W = 8.32 \mu m$**

*DC input voltage*

- $g_m = 2I_d/(V_{gs}-V_t) \Rightarrow V_{gs} - V_t = 2I_d/g_m \Rightarrow V_{gs} = 2I_d/g_m + V_t$ 
  - $g_m = 1mS, V_t = 1.4V$
  - $V_{gs} = 2(200 \mu A)/1mS + 1.4V$ 
    - **$V_{in} = V_{gs} = 1.8V$**

## SIM 2

## DC Operating Point Analysis

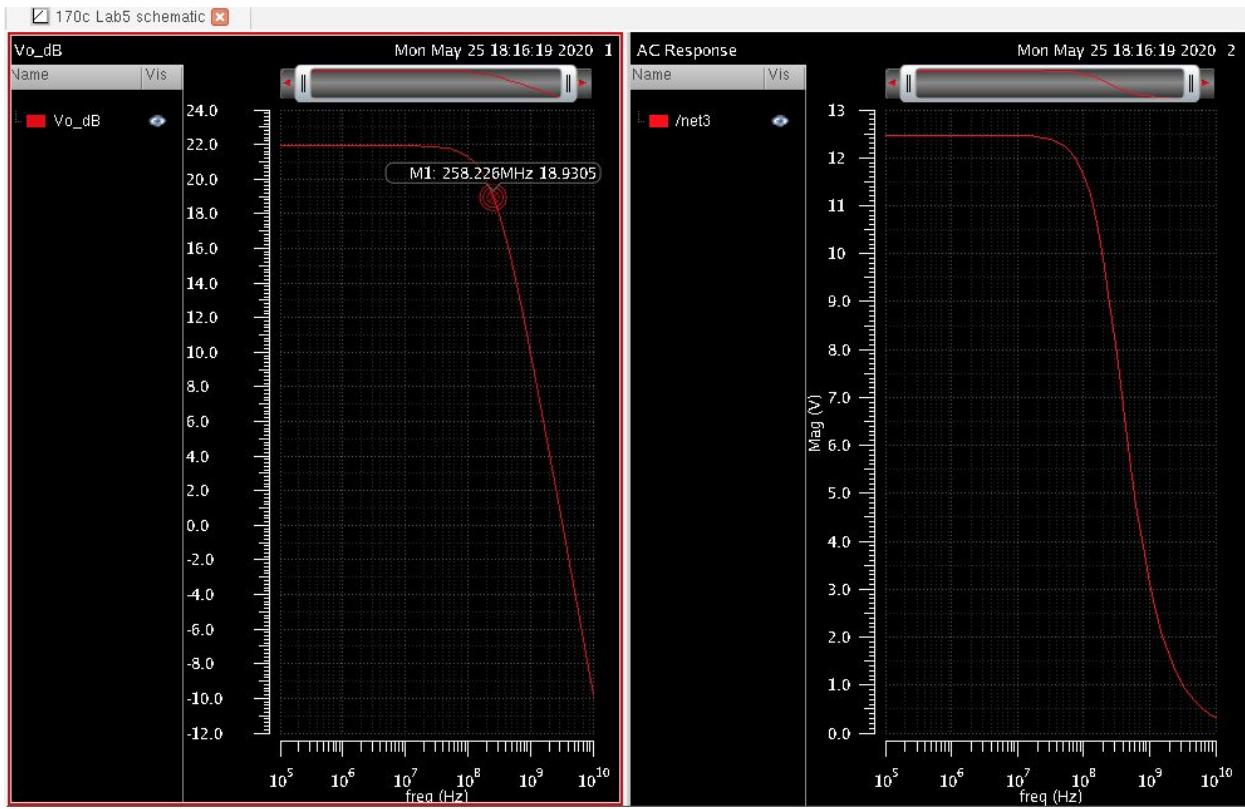


### Dominant pole of amplifier

- From the results window on Cadence:
  - $C_{bd} = 49.44\text{fF}$
  - $C_{bs}, C_{gd} = 0\text{F}$
  - $C_{gd} = 287.3\text{aF}$
  - $C_{gs} = 4.118\text{fF}$
- $C_{gs}$ :  $\tau_1 = C_{gs} \cdot R_1 = 0$
- $C_{bd}$ :  $\tau_2 = C_{bd} \cdot (r_o // R_d)$
- $C_{gd}$ :  $\tau_3 = C_{gd} \cdot (r_o // R_d)$
- $\tau(\text{total}) = \tau_1 + \tau_2 + \tau_3$ 
  - $(C_{bd} + C_{gd})(r_o // R_d)$
- Frequency Pole:  $f_{p1} = 1/2\pi \cdot \tau(\text{total}) = 1/2\pi[(C_{bd} + C_{gd})(r_o // R_d)]$ 
  - $1/2\pi[(C_{bd} + C_{gd})(r_o // R_d)]$
  - $r_o = 1/g_{ds} = 1/1.024 \mu S = 0.976\text{M}\Omega$
  - $r_o // R_d = 1.23\text{e}4\Omega$
  - $1/2\pi[(49.44 + 0.28) \cdot 1\text{e}-15\text{F} \cdot (1.23\text{e}4\Omega)]$
  - $f_{p1} = 250\text{MHz}$

**SIM 3**

### 3dB Frequency Point



- Calculated frequency: 250MHz
- Simulation Frequency: 258MHz
- Percent Error: 3.1%

### SIM 4

*Value of Rs*

- $Rs = (V_{out} - Vs)/Id$ 
  - $Rd = (2V - 0V)/200 \mu A$ 
    - **$Rs = 10k\Omega$**

*Transistor width*

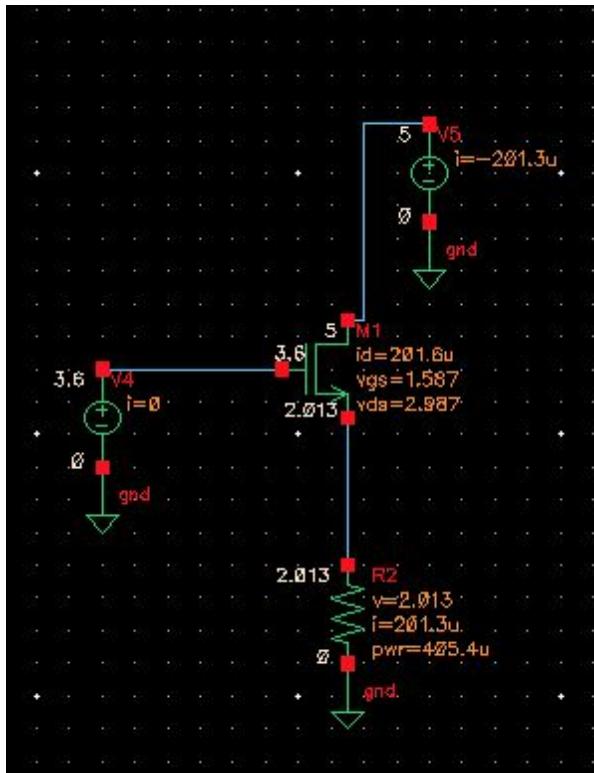
- $Id = \frac{1}{2} \mu Cox(W/L)(V_{gs} - V_t)^2$ 
  - $200 \mu A = \frac{1}{2} (0.6m)(W/L)(1.6V - 1.4V)^2$
  - $L = 2 \mu m$
  - $W/L = 16.6 \mu m$ 
    - **$W = 38 \mu m$**

### DC input voltage

- $gm = 2Id/(Vgs - Vt) \Rightarrow Vgs - Vt = 2Id/gm \Rightarrow Vgs = 2Id/gm + Vt$ 
  - $gm = 2mS$ ,  $Vt = 1.4V$
  - $Vgs = 2(200 \mu A)/2mS + 1.4V = 1.6V$ 
    - $Vin = Vgs + Vout = 1.6V + 2V = 3.6V$

### SIM 5

#### DC Operating Point Analysis

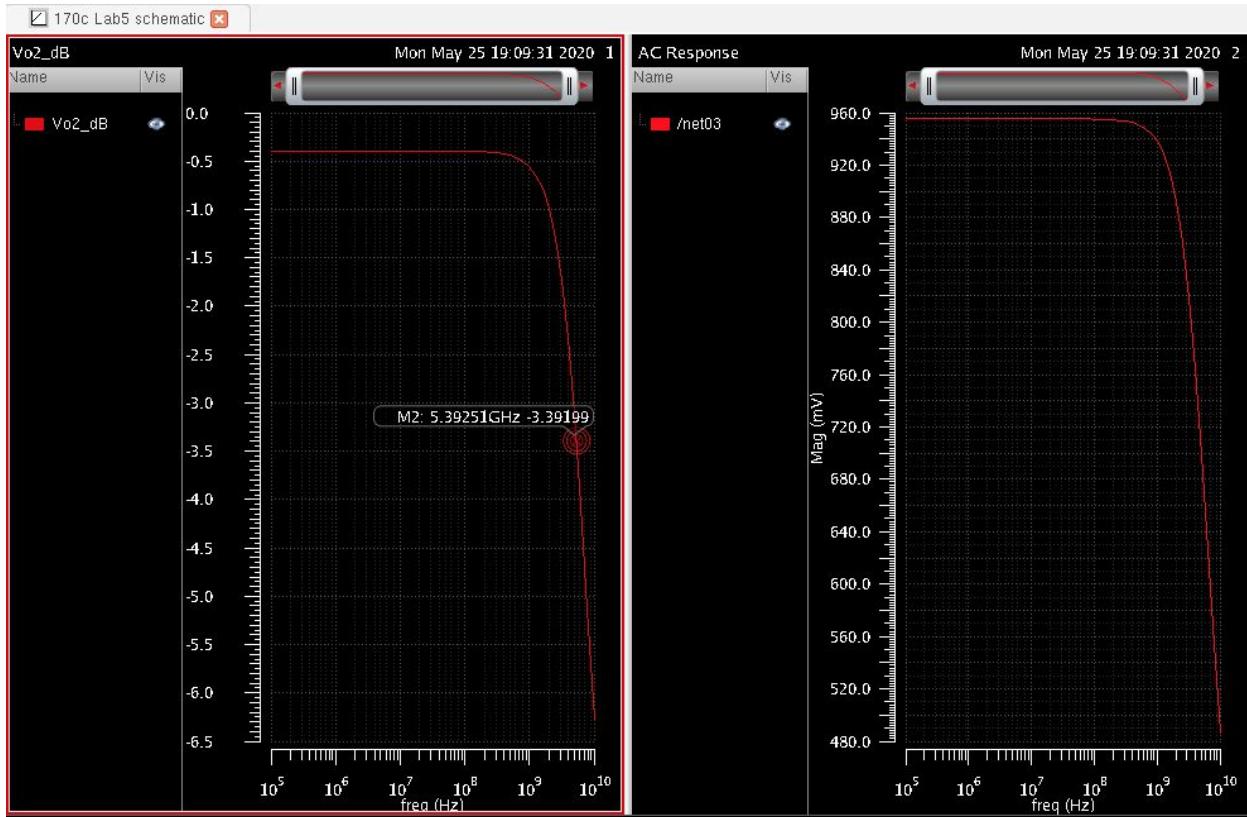


- From the results window on Cadence:
  - $C_{bd} = 37.14fF$
  - $C_{bs} = 53.33fF$
  - $C_{gd} = 1.312f$
  - $C_{gs} = 18.81fF$
- $C_{gs}: \tau_1 = C_{gs} * (R_s // r_o // 1/gm)$
- $C_{bs}: \tau_2 = C_{sb} * (R_s // r_o // 1/gm)$
- $C_{gd}: \tau_3 = C_{gd} * (R_{gd}) = 0$

- $\tau(\text{total}) = \tau_1 + \tau_2 + \tau_3$ 
    - $(C_{gs} + C_{bs})(R_s // r_o // 1/gm)$
  - Frequency Pole:  $f_{p1} = 1/2\pi * \tau(\text{total}) = 1/2\pi[C_{gs} + C_{bs})(R_s // r_o // 1/gm)]$ 
    - $1/2\pi[(C_{gs} + C_{bs})(R_s // r_o // 1/gm)]$
    - $r_o = 1/gds = 1/1.023 \mu S = 0.976 M\Omega$
    - $gm = 2mS \Rightarrow 1/gm = 500\Omega$
    - $R_s // r_o // 1/gm = 495\Omega$
    - $1/2\pi[(18.81 + 53.33)*1e-15F*(495\Omega)]$
- **$f_{p1} = 4.46\text{GHz}$**

## SIM 6

### 3dB Frequency Point



- Calculated frequency: 4.46GHz
- Simulation Frequency: 5.39GHz
- Percent Error: 17.2%

## Conclusion

In this simulation we were asked to design a common-drain and common-source CMOS amplifier. For the circuits we determined the resistor value, transistor width, and dc input voltage. The circuits were simulated with the design constraints and the calculated values were compared to the simulation results. The dominant pole was determined using the capacitor values given in Cadence. After the DC operating point analysis, an AC analysis was performed to calculate the 3dB frequency point and compare it with the estimated values. For the common-drain circuit there was a 3.1% error and for the common-source it was 17.2%.

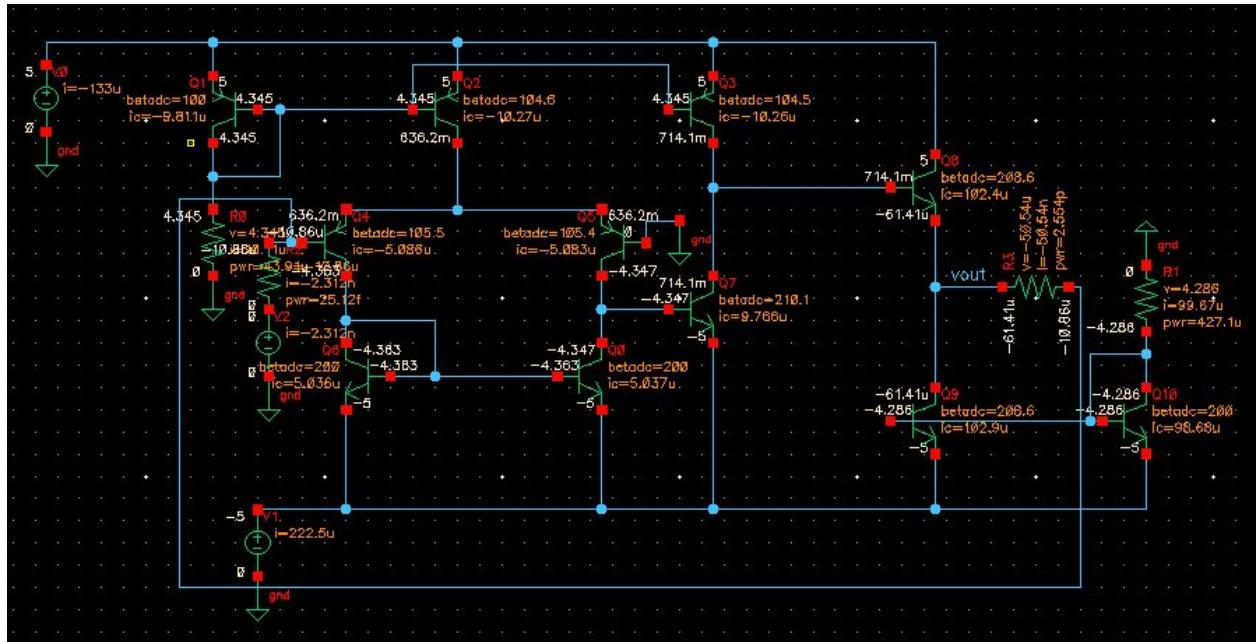
Safia Reazi

170LC

Lab 6

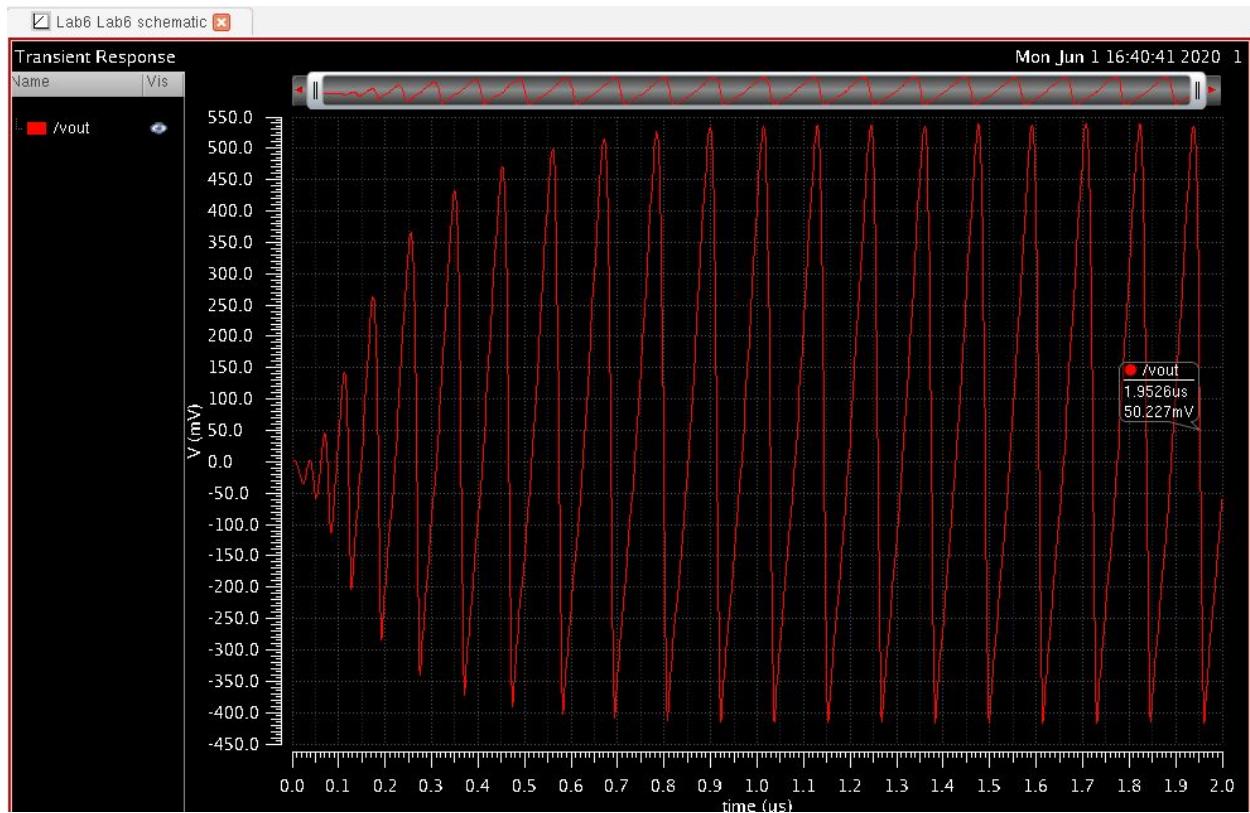
6/2/2020

## SIM 1



- All transistors are in forward active since  $V_{ce} = 4.4\text{V}$  which is higher than  $V_{ce(sat)} = 0.2\text{V}$ .
- The simulated values for the collector currents are similar to the actual values of  $10\mu\text{A}$  and  $100\mu\text{A}$ . The simulated values are  $10.27\mu\text{A}$  and  $102.9\mu\text{A}$ .
- The simulated values for the DC voltages are close to zero with  $V_- = 0\text{V}$  and  $V_{out} = -61\mu\text{V}$
- Resistor in 1st stage:
  - $R_{ref} = 4.3\text{V}/10\mu\text{A} = 430\text{k}\Omega$
- Resistor in 2nd stage:
  - $R_{ref2} = 4.3\text{V}/100\mu\text{A} = 43\text{k}\Omega$

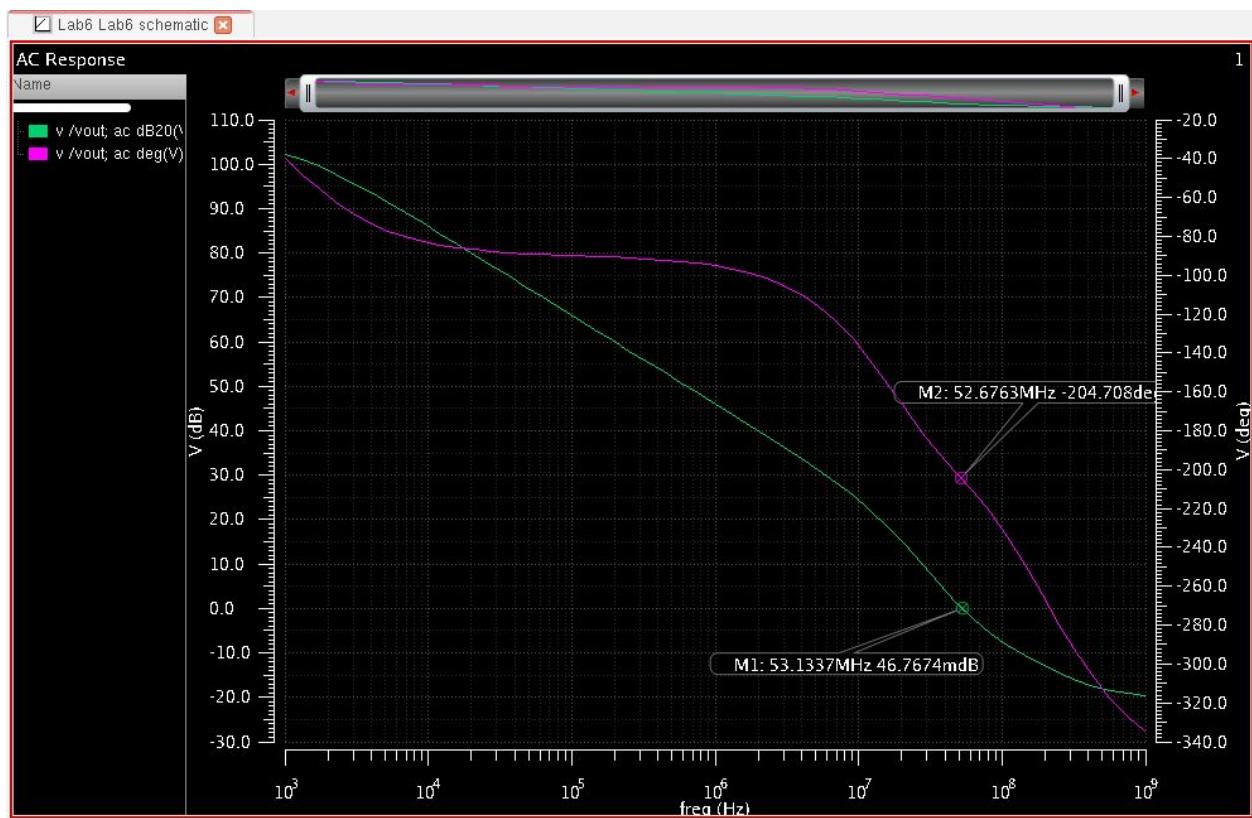
## SIM 2



- The output is oscillating which indicates that the circuit is unstable.

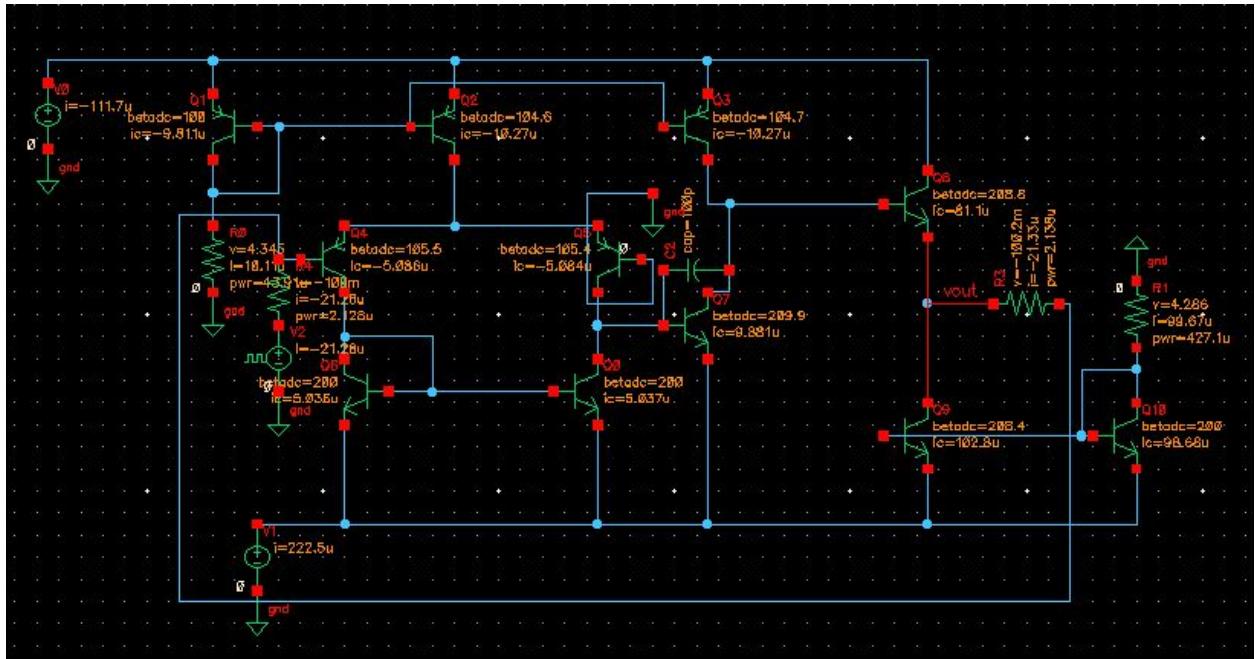
### SIM 3

## Magnitude and Phase of Op-Amp

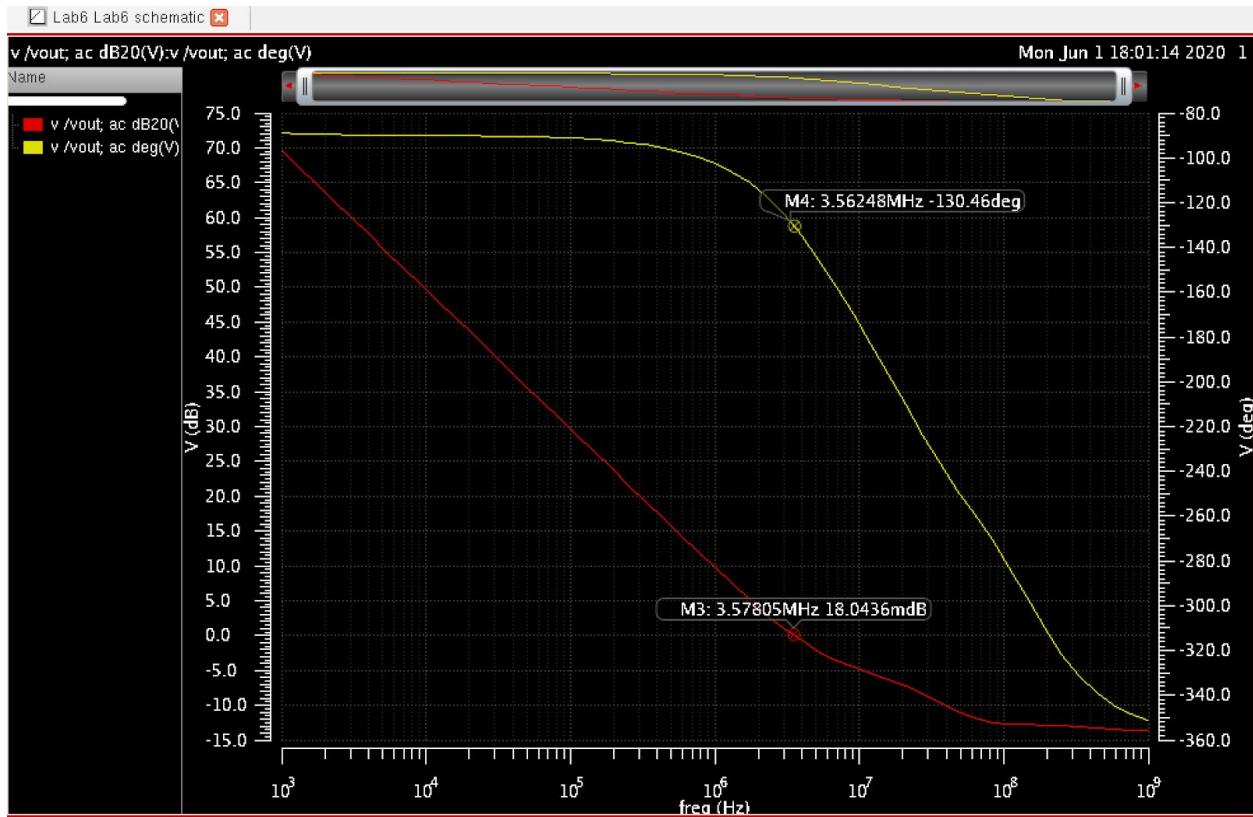


- Unity gain frequency (near 0dB): **53.12MHz**
- Phase (near 53.12MHz): **-204.7°**
- Phase Margin:  $-204.7^\circ - (-180^\circ) = -24.7^\circ$ 
  - Since the phase margin is negative the circuit is unstable.

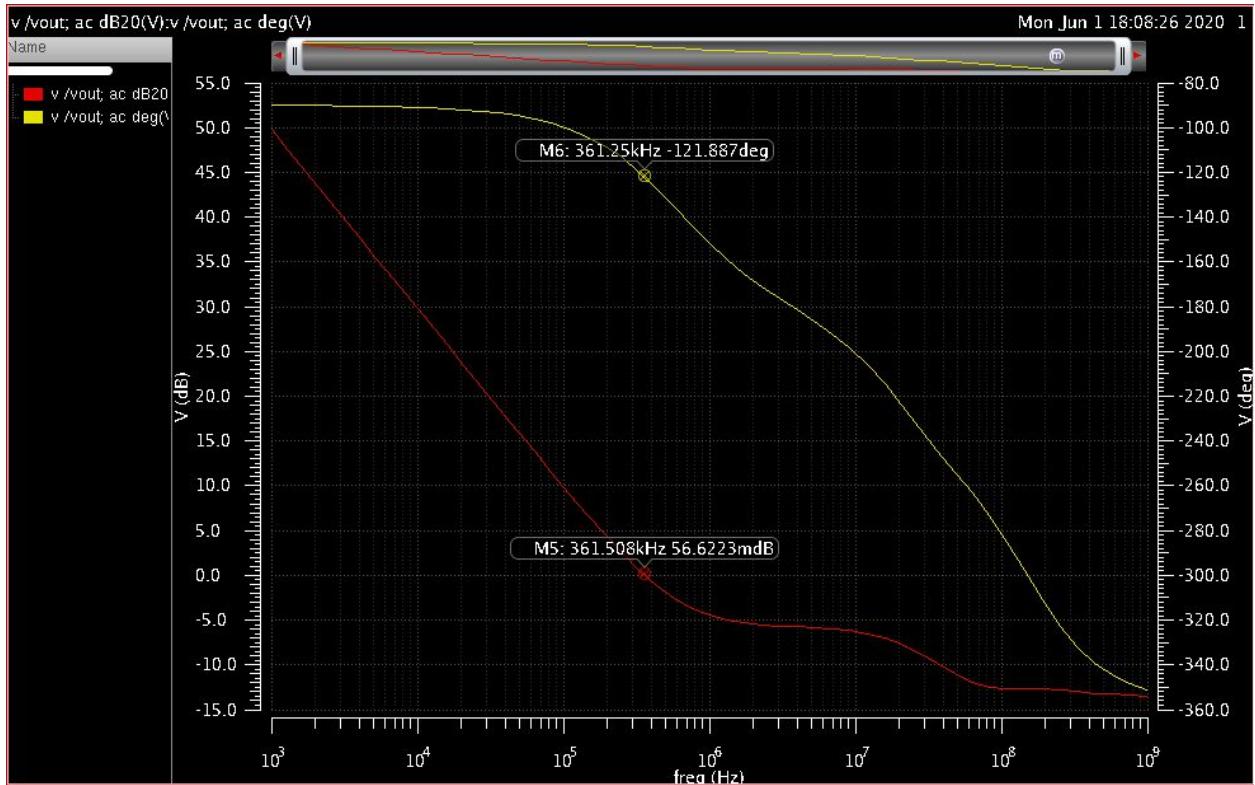
## Compensate the Amplifier



- Additional capacitors need to be added to the circuit
  - $C_c = 10\text{pF}$
  - Dominant Pole:
    - $P_c = 1/r_{out} \cdot C_c(1+A_2)$
- Phase Margin:  $\text{phase}(w_0) - (-180^\circ) = 60^\circ$ 
  - PM = **-120°** (theoretical value)

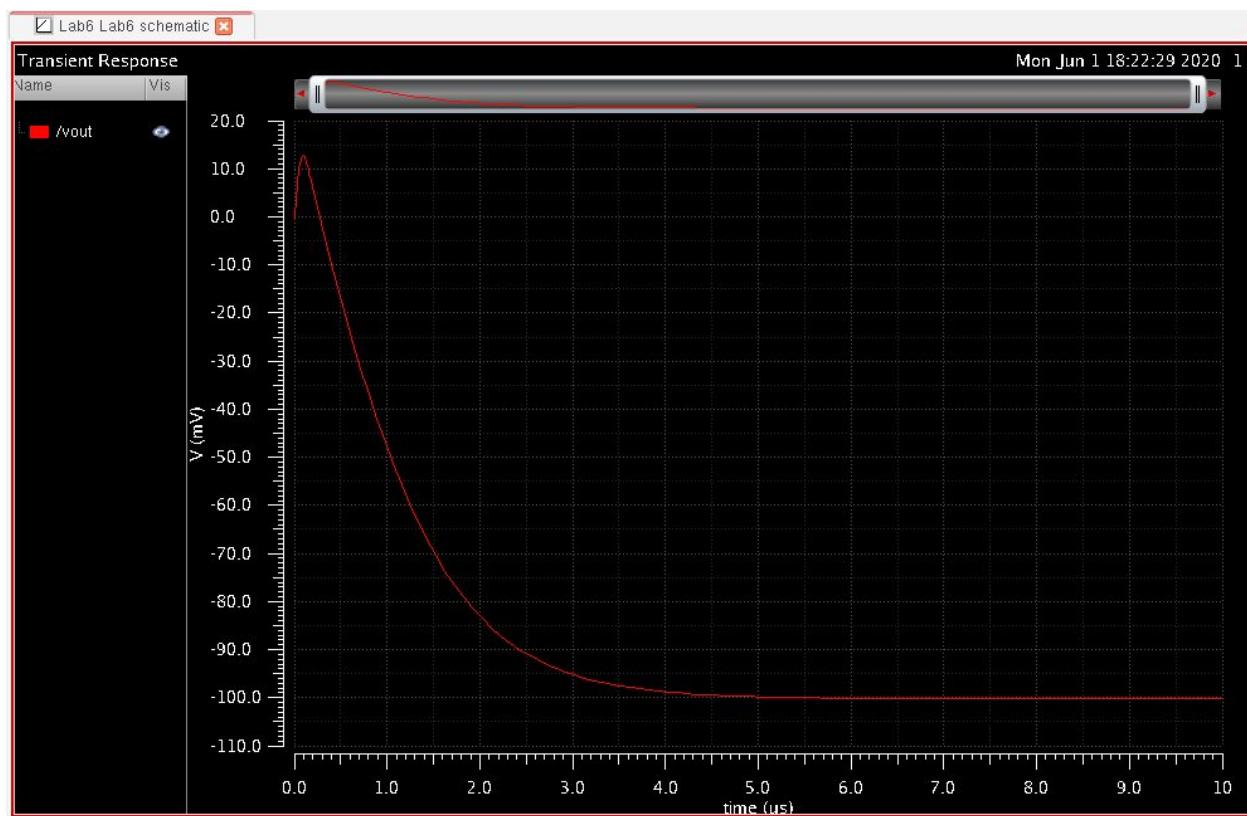


- Phase Margin:  $-130.4^\circ - (-180^\circ) = 49.6^\circ$ 
  - Although the phase margin is now positive and the circuit is stable, it is not at  $60^\circ$ . In order for there to be a  $60^\circ$  phase margin, the value of the capacitor needs to be increased.



- $C_c = 100\text{pF}$
- Phase Margin:  $-121.8^\circ - (-180^\circ) = 58.2^\circ$ 
  - This value is close to the  $60^\circ$  phase margin.

## SIM 5



- After compensation, there is no oscillation in the circuit which means the circuit is now stable. Since  $V_{pulse}$  is added to the input, the transient response increases to about 14mV and flat lines around -100mV due to the negative feedback.

## Conclusion

In this circuit we were asked to design inverting amplifiers to observe the transient response of the op-amps. When capacitors are not present in the circuit the output waveform is oscillating, meaning the circuit is unstable. We used two different inputs,  $V_{pulse}$  and  $V_{ac}$  to prove that the circuit is unstable. We looked at the magnitude and phase plots to determine the phase margins. A negative phase margin indicates that the circuit is unstable. After adding capacitors to the circuit, we see that the phase margin becomes positive. However, in order to get a  $60^\circ$  phase margin the value of the capacitor needs to be increased. We increased the values of the capacitor from 10pF to 100pF. Through compensation, the circuit becomes stable.