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Lab 5

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SIM 1

Value of Rd

- Rd = (Vdd - Vout)/Id
    - Rd = (5V - 2.5V)/200 μ*A*
        - **Rd = 12.5kΩ**

Transistor width

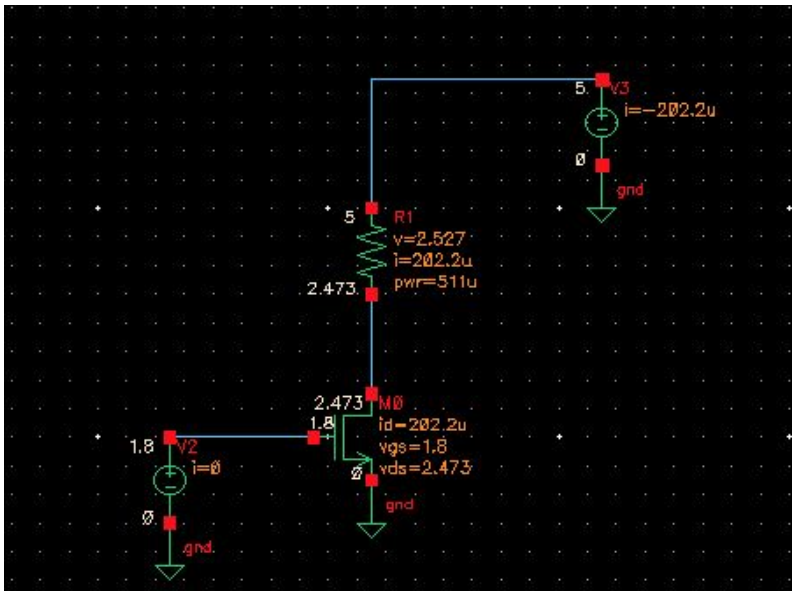
- Id = ½ μCox(W/L)(Vgs-Vt)^2
    - 200 μ*A* =½ (0.6m)(W/L)(1.8V-1.4V)^2
    - L = 2 μ*m*
    - W/L = 4.16 μ*m*
        - **W = 8.32** μ*m*

DC input voltage

- gm = 2Id/(Vgs-Vt) => Vgs - Vt = 2Id/gm => Vgs = 2Id/gm + Vt
    - gm = 1mS, Vt = 1.4V
    - Vgs = 2(200 μ*A*)/1mS + 1.4V
        - **Vin = Vgs = 1.8V**

SIM 2

DC Operating Point Analysis

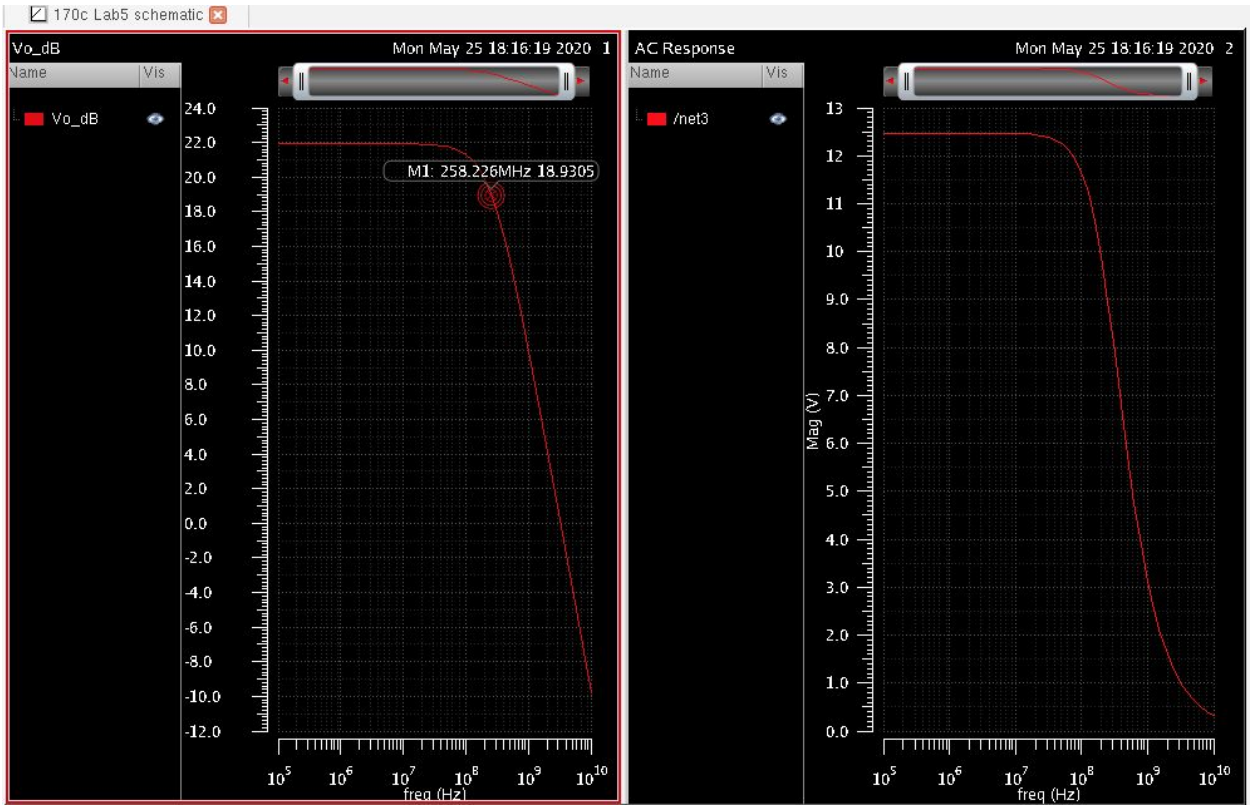


Dominant pole of amplifier

- From the results window on Cadence:
  - Cbd = 49.44fF
  - Cbs, Cgd = 0F
  - Cgd = 287.3aF
  - Cgs = 4.118fF
- Cgs: $\tau 1 = Cgs*R1 = 0$
- Cbd: $\tau 2 = Cdb*(ro \,//\, Rd)$
- Cgd: $\tau 3 = Cgd*(ro \,//\, Rd)$
- $\tau(total) = \tau 1 + \tau 2 + \tau 3$
  - $(Cbd + Cgd)(ro \,//\, Rd)$
- Frequency Pole: $fp1 = 1/2\pi*\tau(total) = 1/2\pi[(Cbd + Cgd)(ro \,//\, Rd)]$
  - $1/2\pi[(Cbd + Cgd)(ro \,//\, Rd)]$
  - $ro = 1/gds = 1/1.024\ \mu S = 0.976M\Omega$
  - $ro \,//\, Rd = 1.23e4\Omega$
  - $1/2\pi[(49.44 + 0.28)*1e\text{-}15F*(1.23e4\Omega)]$
    - **fp1 = 250MHz**

SIM 3

3dB Frequency Point



- Calculated frequency: 250MHz
- Simulation Frequency: 258MHz
- Percent Error: 3.1%

SIM 4

Value of Rs

- Rs = (Vout-Vs)/Id
    - Rd = (2V - 0V)/200 μA
        - **Rs = 10kΩ**

Transistor width

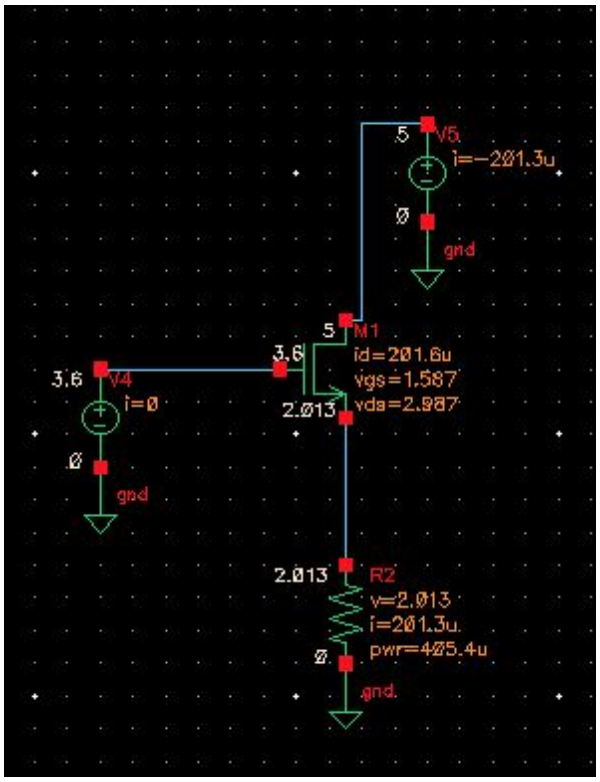
- Id = ½ μCox(W/L)(Vgs-Vt)^2
    - 200 μA =½ (0.6m)(W/L)(1.6V-1.4V)^2
    - L = 2 μm
    - W/L = 16.6 μm
        - **W = 38** μm

DC input voltage

- gm = 2Id/(Vgs-Vt) => Vgs - Vt = 2Id/gm => Vgs = 2Id/gm + Vt
    - gm = 2mS, Vt = 1.4V
    - Vgs = 2(200 μA)/2mS + 1.4V = 1.6V
        - **Vin = Vgs + Vout = 1.6V + 2V = 3.6V**

SIM 5

DC Operating Point Analysis

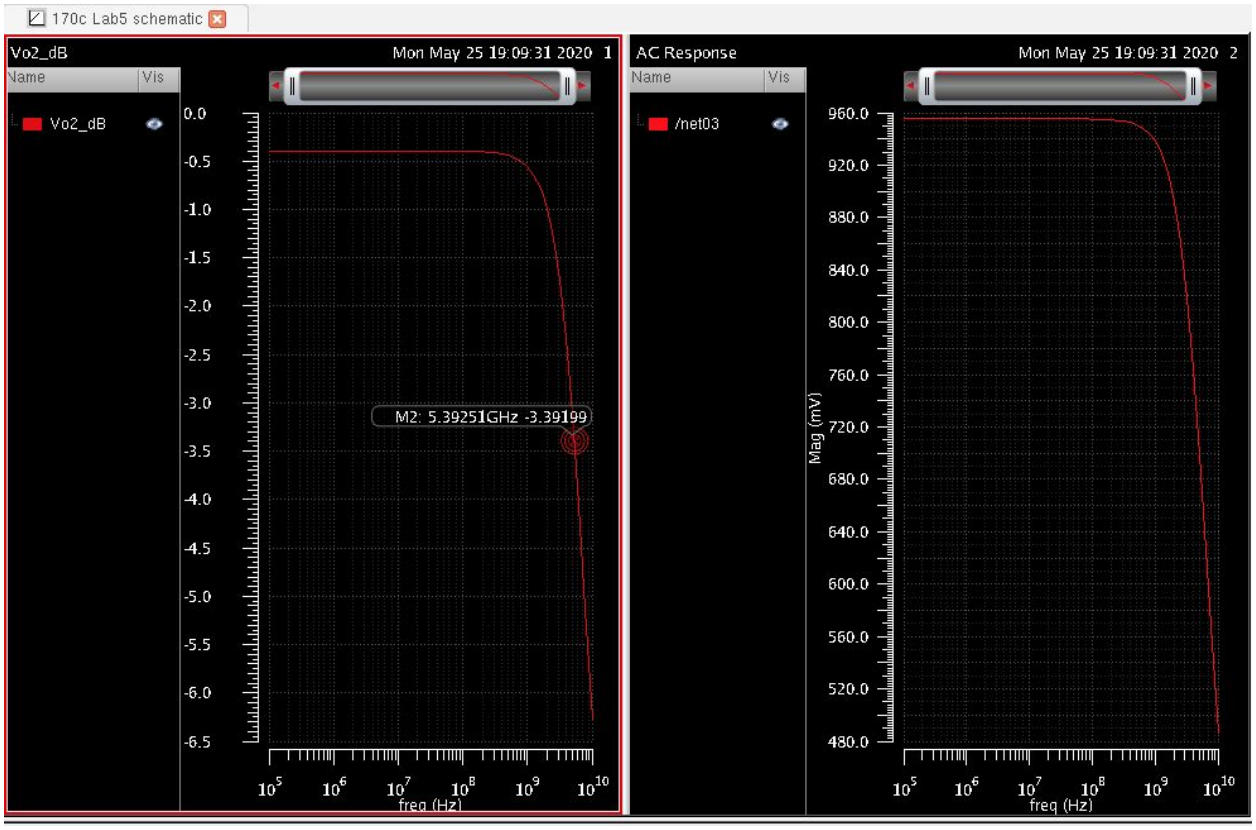


- From the results window on Cadence:
    - Cbd = 37.14fF
    - Cbs = 53.33fF
    - Cgd = 1.312f
    - Cgs = 18.81fF
- Cgs: $\tau 1$ = Cgs*(Rs // ro // 1/gm)
- Cbs: $\tau 2$ = Csb * (Rs // ro // 1/gm)
- Cgd: $\tau 3$ = Cgd*(Rgd) = 0

- τ(total) = τ1 + τ2 + τ3
    - (Cgs + Cbs)(Rs // ro // 1/gm)
- Frequency Pole: fp1 = 1/2π*τ(total) = 1/2π[Cgs + Cbs)(Rs // ro // 1/gm)]
    - 1/2π[(Cgs + Cbs)(Rs // ro // 1/gm)]
    - ro = 1/gds = 1/1.023 μS = 0.976MΩ
    - gm = 2mS => 1/gm = 500Ω
    - Rs // ro // 1/gm = 495Ω
    - 1/2π[(18.81 + 53.33)*1e-15F*(495Ω)]
        - **fp1 = 4.46GHz**

SIM 6

3dB Frequency Point



- Calculated frequency: 4.46GHz
- Simulation Frequency: 5.39GHz
- Percent Error: 17.2%

Conclusion

In this simulation we were asked to design a common-drain and common-source CMOS amplifier. For the circuits we determined the resistor value, transistor width, and dc input voltage. The circuits were simulated with the design constraints and the calculated values were compared to the simulation results. The dominant pole was determined using the capacitor values given in Cadence. After the DC operating point analysis, an AC analysis was performed to calculate the 3dB frequency point and compare it with the estimated values. For the common-drain circuit there was a 3.1% error and for the common-source it was 17.2%.