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A PROCESS MODEL OF STRATEGIC BUSINESS EXIT: IMPLICATIONS FOR AN EVOLUTIONARY PERSPECTIVE ON STRATEGY

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The process model of strategic business exit (SBE) maps the activities of different levels of management onto the business and corporate levels of strategy making involved in Intel Corporation's exit from its core dynamic random access memory (DRAM) business. The SBE process model contributes to the development of an evolutionary process theory of strategy making by conceptualizing the pattern of managerial activities through which resources and corporate competencies are internally redirected toward more viable business opportunities, and the strategic context of a core business dissolves. The SBE process model corroborates the usefulness of the Bower–Burgelman process model for conceptualizing strategy making in complex organizations.

INTRODUCTION

In this paper I examine the pattern of managerial activities involved in the strategic process through which an established high-technology firm exited from a core business in a fast-growing industry without destroying valuable corporate competencies. Relatively little is currently known about managing strategic business exit (SBE). In strategic management, the most extensive literature related to exit concerns portfolio planning, corporate restucturing, and divestiture (e.g., Hoskisson, Johnson, and Moesel, 1994). Other strategic management research has focused on exit in terms of product-market positioning in declining industries (e.g., Porter, 1980; Harrigan, 1981; Baden-Fuller, 1989; Lieberman, 1989). One previous field study (Gilmour, 1973) has provided data on the divestment decision process. In organization theory, rich literatures exist on disbandings (e.g., Hannan and Freeman, 1989), organizational decline (Sutton, 1990), permanently failing organizations (Meyer and Zucker, 1989), and escalation (e.g., Staw and Ross, 1987) and de-escalation (Simonson and Staw, 1992) processes. Research specifically focusing on organizational exit, however, is relatively rare. Ross and Staw, for instance, in their recent study of escalation and exit concerning the Shoreham nuclear power plant note that 'prior research provided few leads about the exit of organizations from losing causes of action' (1993: 724).

The SBE process examined in this paper concerns Intel Corporation's exit in the mid-1980s from the dynamic random access memory (DRAM) business which had been its core business during the 1970s. The data on Intel's exit from DRAMs are part of an ongoing longitudinal field study of the evolution of Intel's corporate strategy. Earlier work based on this research has provided insight in the intraorganizational ecological processes that shape strategy making in complex organizations and make various forms of adaptation possible (Burgelman, 1991). More recently, this research has yielded a process theory of strategic business exit that combines industry-level and firm-level forces to explain Intel's exit from DRAMs (Burgelman, 1994).

The present paper's main purpose is to provide

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a conceptualization of the *intra-firm* pattern of managerial activities involved in the strategic process that led Intel to exit from its core DRAM business but also allowed the company to preserve valuable corporate competencies which could be redeployed in its other businesses. *Process* is defined as the pattern of activities of differentially positioned managers that, together, produce outcomes such as strategic business exit. I adopt the Bower–Burgelman process model (Bower, 1970; Bower and Doz, 1979; Burgelman, 1983b)—a matrix-like framework consisting of levels of management (operational, middle, top) by levels of strategy making (business, corporate)—to conceptualize the SBE process. The Bower–Burgelman process model elucidates the 'generative mechanisms' (Pondy, 1976) of corporate strategy making by showing how the activities of individuals combine to produce strategic outcomes at the level of the corporation, as well as how forces at the level of the corporation influence the activities of these individuals (Burgelman, 1983b). The level of analysis addressed by the Bower–Burgelman process model is the firm; the unit of analysis is the strategic process associated with particular types of outcomes, such as strategic capital investments, internal corporate ventures, and SBEs. Managerial activities are assumed to be boundedly rational, purposeful, and driven by managers' perceptions of their and the firm's interests. Because it conceptualizes the simultaneous involvement of differentially positioned managers, the Bower–Burgelman process model can document how well these managerial activies are aligned.

The process model of SBE presented in this paper elucidates the generative mechanisms of effective strategic business exit. It conceptualizes the behavior of Intel's senior and top management and the corporate-level contextual forces that prevented escalation of commitment to the failing DRAM business and the preservation and redeployment of key corporate competencies. I use qualitative pattern matching to distinguish the SBE generative mechanisms from those involved in new entry through internal corporate venturing (Burgelman, 1983b). The paper thus combines, to some extent, testing of existing theory and building of new theory. I show that the same intraorganizational ecological processes, but involving different managerial activities, influence the creation of new resource combinations *and* the creative destruction of old ones. This provides insight in the link between strategy making and corporate 'capability' (Teece, Pisano, and Shuen, 1990), and additional insight in the role of strategy-making processes in firm evolution. It also contributes additional empirical content to the resource-based view of the firm which examines how firm-specific resource combinations may become sources of competitive advantage. Finally, by focusing on the fine-grained detail of the managerial activities involved in the actual processes through which a major change—from an old core business to new ones and from certain technologies to others—took place, I provide some evidence supporting the need to critically examine the universal applicability of the punctuated model of organizational change (e.g., Tushman and Romanelli, 1985; Gersick, 1991; Romanelli and Tushman, 1994).

The paper is organized as follows. A description of the longitudinal field study is provided in the Appendix. The next section presents the process model of SBE. The discussion section summarizes the key findings, relates the process model of SBE to process models of other substantive areas of strategy making, and explores how the findings may contribute to an evolutionary process theory of strategy making in established firms. The final section presents implications and conclusions.

PROCESS MODEL OF SBE

Case studies and chronology of key events

Data were drawn from the field research described in the Appendix to write three case studies concerning the DRAM exit decision, its implementation, and its implications for Intel's other businesses (Cogan and Burgelman, 1990, 1991; Graham and Burgelman, 1991). To assure that the data were internally valid and reliable, these case studies were reviewed by all the managers who participated in the study. The cases have been taught for senior managers at Intel, and they have also been used in several executive programs in which former Intel managers were participants. Invariably these managers have confirmed the DRAM story as told in the cases. The DRAM data were also used to establish a chronology of key events in the evolution of DRAMs at Intel in the period 1970–85. These events are reported in Table 1 and numbered **E1–E38**.

Table 1. Key events in the evolution of DRAMs at Intel: 1970–85

1970	**E1**. Intel introduced the first 1K (kilobit) dynamic random access memory (DRAM) in volume. The product used the new metal-oxide semiconductor (MOS) process technology. This process technology was relatively slow but less power consuming than the standard bipolar process technology. Intel was the first successful mover in DRAMs.
1972–74	**E2**. Intel introduced 4K DRAMs. Intel captured more than 80% of the 4K DRAM market in 1974. **E3**. The first competitive challenge came from Mostek, a new startup. Mostek focused on user-friendliness of DRAMs in the 4K DRAM generation.
1976–77	**E4**. Intel introduced a standard 16K DRAM. Intel captured more than 35% of the 16K DRAM market in 1976. **E5**. The competitive challenge from Mostek and others continued. By 1979, Intel's market share in standard 16K DRAM was less than 5%. **E6**. High demand for EPROMs created a shortage in Intel's manufacturing capacity. For the first time, DRAM manufacturing capacity was shifted toward the higher-margin EPROM products.
1979	**E7**. Intel introduced the first 5-volt 'single-power-supply' 16K DRAM. Single-power supply greatly simplified the user's design and production tasks. In 1979, Intel was the only supplier of single-power-supply 16K DRAMs and captured a price premium of double the industry average for three-power-supply 16K DRAMs. **E8**. Intel expected the 64K DRAM generation to be introduced later and to be based on single power supply. Fujitsu introduced a standard 64K DRAM in 1979 and captured a large market share. **E9**. The single-power-supply 16K DRAM remained a small-niche product. **E10**. Intel fell behind in manufacturing yields relative to top Japanese producers of DRAMs (Prestowitz, 1988: 46).
1982	**E11**. Intel's 64K DRAM with 'redundancy' entered production. Redundancy involves adding an extra column of memory elements so that, in the event of a process-induced defect, the auxiliary column could be activated. This allows a defective memory chip (at testing) to be reprogrammed before shipment and to increase yields. Intel expected that 'redundancy' would help overcome its disadvantage in manufacturing yields relative to the Japanese, and that the 256K DRAM generation would be based on the redundancy process technology. **E12**. However, Fujitsu and Hitachi entered with a standard 256K DRAM in 1982 and captured a large market share. **E13**. Intel was now far behind in manufacturing competence relative to the Japanese.
Mid-1982	**E14**. The manager of fabrication sites (Fabs) 4, 5 and 8 proposed to align the memory components division (MCD), which was part of Intel's Components Group, with a dedicated DRAM manufacturing capability in fabrication site 5 (Fab 5), in Oregon. **E15**. This proposal was not accepted by top management.
1983–84	**E16**. Intel decided to produce a 'complementary metal-oxide semiconductor' (CMOS) 256K DRAM. CMOS had the advantage of very low power consumption. **E17**. Responding to capacity constraints, Intel decided to cancel the standard n-channel (NMOS) 256K DRAM effort and to allocate the capacity to other, more profitable products. DRAM manufacturing was now down to one fab out of a network of seven. **E18**. In 1984, Intel introduced first a 64K CMOS DRAM and then a 256K CMOS DRAM and was the only supplier of CMOS DRAMs. Intel hoped to offset its manufacturing cost disadvantage with a technically superior product, expecting that customers would pay a price premium for the CMOS version. Intel expected that CMOS would become the standard for 256K and later DRAM generations. But it did not for the 256K generation. Intel's market share in 64K DRAMs in 1984 was less than 2% and less than 1% in 256K DRAMs by 1985. Prices for CMOS DRAMs turned out to be far lower than Intel expected.
Spring 1984	**E19**. The manager of Fab 5 proposed an investment of approximately $80 million for a DRAM-exclusive facility in Oregon. The proposal was based on simple, standard process technology and manufacturing vs. Intel's 'process technology leadership' approach. **E20**. Top management denied the investment.
Mid-1984	**E21**. The manager of static random access memory (SRAM) and microprocessor process technology decided to stop one of two SRAM process technology development projects which was important for maintaining a competitive position in commodity memories, including DRAMs. **E22**. The DRAM process technology group was working on the 1 Meg (megabit) DRAM and focused on an advanced capability in 'thin dielectrics'. Thin dielectrics allow reduction

Table 1. Continued

	of minimum feature size to 1 μm instead of changing the entire DRAM cell design. The DRAM process technology group estimated their design was 2 years ahead of the competition. The estimated budget for DRAM process technology for 1985 was estimated to be around $65 million, roughly the same level as for EPROMs and microprocessors.
October 1984	**E23**. Intel decided to close one of its three process technology sites, but was not quite sure which one to close: Fab 5 process technology in Oregon (DRAM), Fab 3 process technology in Livermore (microprocessors), or Fab 1 process technology in Santa Clara (non-volatile memory, including EPROM). Fab 5 process technology (Oregon) was estimated to be 12 months ahead in developing 1 μm linewidth technology.
November 1984	**E24**. Top management decided not to proceed with 1 Meg DRAM production. **E25**. The DRAM process technology group (Fab 5) petitioned to be allowed to develop prototypes in order to demonstrate functionality for the 1 Meg DRAM. The morale of the Fab 5 group sank as their mission was now unclear.
December 1984	**E26**. Intel decided to close the Fab 3 process technology (Livermore) site and to move the 1 μm 80386 microprocessor development project to the Fab 5 process technology group in Oregon. Fab 5 process technology had the strongest linewidth reduction competence at Intel. The 1 μm 80386 project was transferred quickly to Fab 5 (early 1985) to avoid 'not invented here' and further distractions to the manufacturing of 1.5 μm 80386 products at Fab 3 in Livermore.
Early 1985	**E27**. The head of DRAM operations (product design, sales and marketing, customer service) in the Memory Components Division proposed to subcontract 256K CMOS DRAM to a Japanese firm.
March 1985	**E28**. The first batch (of final five) of 1 Meg DRAM prototypes yielded functional die. A total of five batches of prototypes were processed through Fab 5, before further developments on the 1 Meg DRAM were completely halted. **E29**. The General Manager of the Components Group continued to feel that retaining DRAMs as a core business of Intel was important. He felt it was difficult to get top management to discuss the issue. **E30**. COO Andy Grove felt strongly that the burgeoning logic (microprocessor) business needed to get more resources.
Mid-1985	**E31**. In light of its history of DRAM manufacturing problems, Fab 5 manufacturing sought to show it was capable of producing state-of-the-art products. Fab 5 produced primarily 256K DRAMs but wanted to show an ability to second source current-generation microprocessor products currently produced at Fab 3. Initial yield results were good.
Summer 1985	**E32**. An evaluation of Japanese/Korean DRAM production alternatives took place under impulse of the General Manager of the Components Group who was in charge of overseeing the implementation of Intel's exit from DRAMs. Implementation lingered on. **E33**. At the last moment, the plan to source DRAMs was turned down by top management due, in part, to Intel's concern about giving a competitor access to its distribution channels. There was little support from Fab 5 manufacturing for this subcontracting alternative in the first place. Without the prospect of a partner, the head of DRAM operations recommended exit from DRAMs. **E34**. The General Manager of the Components Group stepped down and was reassigned to another business area. Andy Grove assumed direct operational control over the DRAM exit process. He assigned two senior managers to immediately and fully implement the DRAM exit decision.
October 1985	**E35**. The decision was reached to close Fab 5 for DRAM production. Fab 5 was to be transformed into a process technology site for microprocessors. Animosity and mistrust between manufacturing and process technology personnel flared at Fab 5. **E36**. Andy Grove went to Portland to speak to the group: 'Welcome to the Mainstream Intel'. That is, Intel the 'microcomputer company'.
December 1985	**E37**. After completing the 'end-of-life build' of DRAMs at record high yields, approximately 250 production supervisors and operators at Fab 5 received their final paychecks and left Intel. Most of Fab 5's technicians and engineers were absorbed by the new Logic (microprocessor) process technology effort. Most of the personnel of the Memory Components Division were absorbed by other divisions; several DRAM designers left Intel. **E38**. Intel top management reconsidered the routines for process technology–manufacturing integration. Top management reasserted responsibility for strategic planning and articulated a new corporate strategy based on architectural leadership in microprocessors, becoming vendor of preference (sole source) for customers, and becoming a world class manufacturer.

Process model conceptualization of SBE

Grounded theorizing consciously avoids data interpretation that is prematurely influenced by existing theoretical frameworks (Glaser and Strauss, 1967). This approach was used in earlier work based on the field research described in the Appendix (Burgelman, 1991, 1994). The present paper, however, draws on the process model of internal corporate venturing (ICV) (Burgelman, 1983b) to construct a process model of SBE. The construction of the SBE process model involved an iterative approach of qualitative pattern matching, moving back and forth between the ICV process model and the DRAM exit data. Qualitative pattern matching suggested that the overall structure of the ICV process model was useful to conceptualize the strategy making involved in SBE. Qualitative pattern matching also revealed, however, that the managerial activities involved in SBE, and the linkages between them, were quite different. This effort yielded new categories to conceptualize the managerial activities involved in SBE. This is shown in Figure 1.

The SBE process model presented in Figure 1 shows the business and corporate levels of strategy making and depicts the sequential and simultaneous activities of different levels of management in each of these levels of strategy making. The *definition* part of the process model maps the managerial activities that made exit from DRAMs a definite thrust at the business level. The *impetus* part of the process model maps the managerial activities that gave the business-level thrust to exit from DRAMs its force. The *strategic context* part of the process model maps the managerial activities that stimulated a reconsideration of the role of the DRAM business in Intel's corporate strategy. Finally, the *structural context* part of the process model maps the selective forces associated with the rules governing resource allocation and strategic debate, and the managerial activities involved in attempts to change the rules. The structural context and strategic context parts of the process model constitute the internal selection environment within which the business-level parts took shape, and through which the corporate-level strategic issues associated with the exit from the DRAM business were brought into focus.

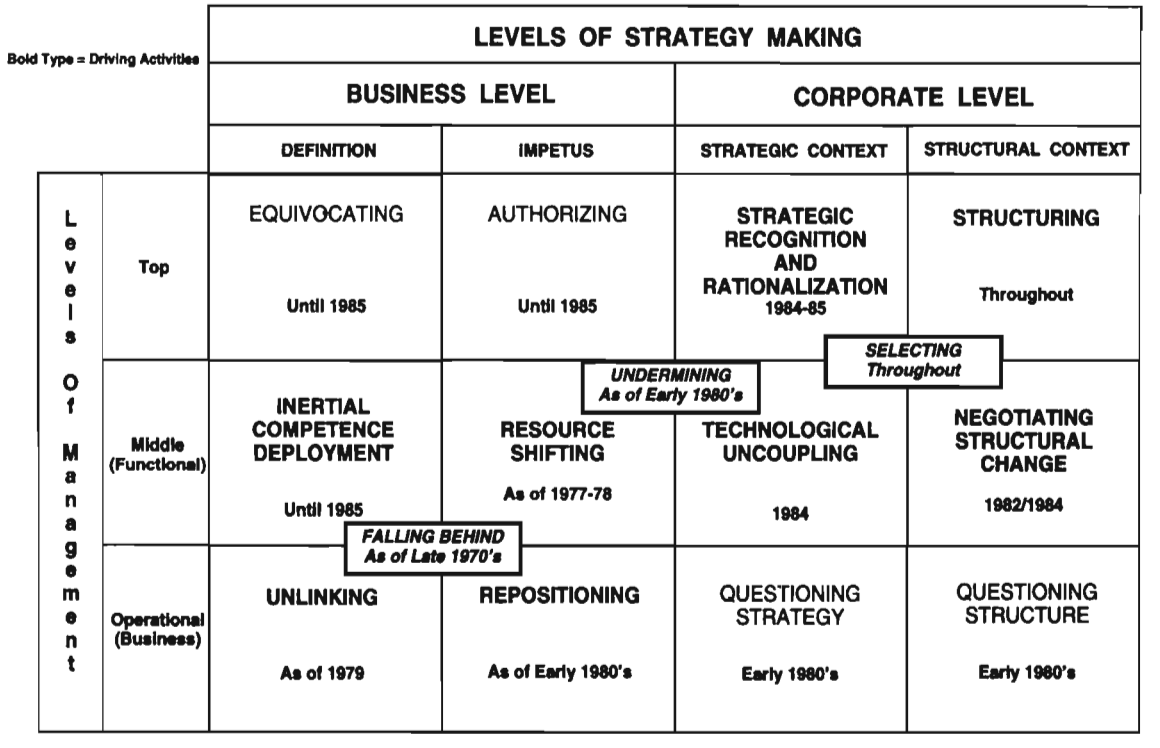

Figure 1. Managerial activities in a process model of SBE

Figure 1 shows that each part of the SBE process model involved top, middle, and operational-level managerial activities. The relations between the operational and middle levels are viewed in terms of responsibilities rather than hierarchy. Intel was a multibusiness firm, but its organization structure maintained a strong functional dimension with managers of the different product divisions needing to obtain R&D and manufacturing support for their products from the functional units. This is reflected in Figure 1: operational managers were business managers who interacted with the product-market environment and were primarily concerned with business strategy-level issues; middle managers were functional managers primarily concerned with maintaining and developing the firm's distinctive technological competencies and with resource allocation issues. Top managers, on the other hand, were primarily concerned with corporate strategy-level issues. Some activities—shown in bold characters—were stronger in driving the SBE process than others. Figue 1 also indicates the time period within which the activities took place.

Figure 2, which can be superimposed on Figure 1, shows how the different managerial activities affected each other, forming a pattern. The arrows indicate the dominant direction of influence among the key managerial activities. The relative importance of activities is indicated by the different types of line segments. The rough sequential and simultaneous flow of the activities in this pattern is indicated by the numbers in Figure 2.

The solid lines in Figure 2 identify the activities that were strongest in driving the SBE process. Inertial competence deployment of middle-level managers (1) led to unlinking of market needs and Intel DRAM products. Operational and middle-level managerial activities at the business level (3, 4) responded to the selective pressures of the structural context (1′) favoring other businesses and to DRAMs falling behind (2) in the market. At the corporate level, the undermining of the DRAM business (7) resulting from the resource shifting, combined with the continued selective pressures from the structural context (8), set the stage for middle managers' technological uncoupling activities and top management's strategic recognition and rationalization of the exit from DRAMs (9, 10). The undermining of the DRAM business was unsuccessfully countered by

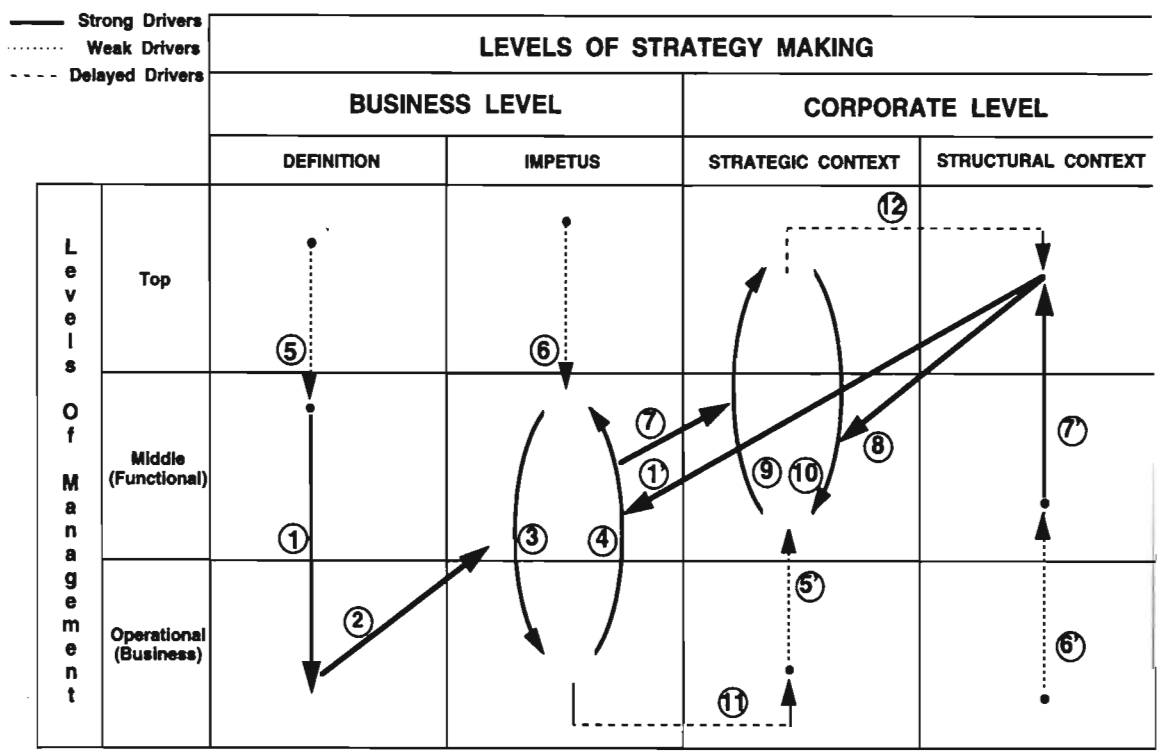

Figure 2. Flow of activities in a process model of SBE

efforts of some DRAM middle-level managers to negotiate changes in Intel's structural context (7′).

The finely dotted lines in Figure 2 represent the set of activities that were weak drivers of the SBE process. At the business strategy level, top management's equivocation about the importance of DRAMs for Intel (5) led them to continue to invest heavily in DRAM R&D, which reinforced the inertial competence deployment of middle-level managers (definition). On the other hand, top management authorized (6) incremental shifting of scarce manufacturing resources from DRAMs to other businesses (impetus). At the corporate strategy level, operational managers associated with the DRAM business questioned Intel's business strategy in DRAMs (5′) (strategic context). Operational level managers also questioned some aspects of the structural context, in particular the resource allocation rule, as shifts in resource allocation were made and authorized (6′).

The broken line segments in Figure 2 indicate two delayed effects in the SBE process. First, a last ditch, unsuccessful effort was launched by a DRAM business manager to change the strategic context of the DRAM business in 1985 (11). Second, the decision to exit from DRAMs led top management to reconsider some aspects of Intel's structural context (12).

Below, the case data on the DRAM exit and the chronology of key events listed in Table 1 are analyzed in terms of the SBE process model. The analysis is organized around the four parts of the process model. The primary focus of the analysis is on the bold-faced key activities shown in Figure 1. The analysis breaks the chronological order of Table 1 in order to examine, together, the activities of differentially positioned managers involved in the key parts of the SBE process model and the links between them. Where appropriate, the analysis is keyed to the numbers associated with key events in Table 1.

Definition

The DRAM case data indicate that the definition part of the SBE process was not driven by clear corporate or business-level strategic intent and involved managerial activities that were not well articulated across hierarchical levels. There was no clear corporate-level exit decision until the exit from DRAMs was virtually a *fait accompli*.

The definition part of the SBE process took several years to complete. During that time, top management was divided and equivocal in its support for DRAMs. Some top managers continued to view Intel as a 'memory' company and DRAMs as the 'technology driver' on which the company's learning curve depended. Top management continued to invest in DRAM R&D at the same level as for its other, far more successful, businesses and avoided the difficult decision to consider exiting from DRAMs (**E22**). This reluctance was underscored by Andy Grove, COO at the time, and by Ed Gelbach who was VP of sales at the time. Andy Grove said (Graham and Burgelman, 1991: 1):

> Don't ask managers, 'What is your strategy?' Look at what they do! Because people will pretend . . . The fact is that we had become a non-factor in DRAMs, and we had been for several years with 2–3% market share. The DRAM business just passed us by! Yet, in 1984, many people were still holding on to the 'self-evident truth' that Intel was a memory company.

And the VP of Sales recalled (Cogan and Burgelman, 1990: 13):

> In board meetings, the question of DRAMs would often come up. I would support them from a market perspective, and Gordon [Moore] would support them because they were our technology driver. Andy [Grove] kept quiet on the subject. Even though it wasn't profitable, the board agreed to stay in it on the face of our arguments.

Inertial competence deployment

Middle-level functional managers contributed to the definition part of the SBE process through inertia in their deployment of Intel's distinctive competence in the business strategy of DRAMs. Semiconductor memories required three types of technical competencies (Burgelman, 1994): (i) design (can we design it?); (ii) process technology (can we make it?); and (iii) large-scale precision manufacturing (can we make it in large volumes with high initial yields?). Intel's initial success in the 1K (kilobit) DRAM (1971–73) was due to the ability of its technologists to come up with a process technology that allowed production yields sufficiently high to beat magnetic core memory, which was the industry standard of the day, in the market (**E1**). Process

technology was therefore viewed by Intel management as the firms' 'distinctive competence' (Selznick, 1957) on which its ability to differentiate its products and get a premium price depended (**E7**, **E11**, **E18**, **E22**). Having maintained leadership in the 4K DRAM generation (1972–76) (**E2**, **E3**), Intel's process technologists came up with the first 5-volt single-power-supply 16K DRAM in 1979. Intel process technologists decided to focus on the single-power-supply 16K DRAM because they projected a relatively long life cycle for the 16K generation due to the technological challenges posed by the 64K generation (**E18**). They also believed that the single-power-supply process would eventually dominate the memory industry. They considered it too risky to tackle both the 64K DRAM generation and the single power supply in the same product.

While it is usually difficult to observe distinctive competence independent of the successful product with which it is associated, and the risk of tautology is high, Intel's pattern of strategic actions offers the opportunity to make independent observations. When changes in the DRAM industry structure shifted the basis of competition from process technology to large-scale precision manufacturing, Intel *continued* to rely on process technology to compete in four successive product generations. The first independent observation concerned the 16K DRAM generation. But, as documented below, inertial deployment of process technology competence was also observed in the 64K, 256K, and 1 Meg (megabit) product generations. Paradoxically, the distinctive competence that provided Intel with its initial competitive advantage became a source of failure later on.

Unlinking

Intel was sole supplier in the single-power-supply market segment and captured a price premium of double the industry average for the standard three-power-supply 16K DRAMS. On the other hand, Intel had lost share in the mainstream market with their earlier standard three-power-supply 16K product offerings (1976–79) (**E4**, **E5**). And, the single-power-supply 16K DRAM remained a small niche product (**E9**). In 1979, the worldwide shipments of three-power-supply (standard) 16K DRAMs totalled 70 million units; Intel's shipments for the single-power-supply 16K DRAM totalled only 150 thousand. In 1981, the total units shipped worldwide were 215 million for the standard 16K DRAM and 5.7 million for Intel's single-power-supply 16K DRAM (Cogan and Burgelman, 1990). Thus, by marketing and selling the single-power-supply 16K product, Intel's DRAM business managers allowed the company to get started on a course that unlinked its DRAM products from the mainstream DRAM customer base. This unlinking, unintentionally, provided a definite thrust to exit from DRAMs.

Impetus

The impetus part of the SBE process, too, was not driven by clear corporate or business-level strategic intent. This part of the process concerned managerial activities that gave force to the thrust to exit from DRAMs in the late 1970s to early 1980s. Top management's primary role in the impetus part of the process lay in authorizing resource allocation decisions made by middle managers who responded to competitive pressures encountered in the DRAM market and internal financial performance pressures from Intel's structural context that favored other products over DRAMs.

Resource shifting activates the impetus process

Intel's initial success as a startup company was primarily based on DRAMs, but it soon developed a new type of memory products, EPROMs, as well as logic products based on the microprocessor. EPROMs and logic products were unplanned products (Cogan and Burgelman, 1990), but became fast-growing businesses that competed for Intel's resources, especially scarce manufacturing capacity. Manufacturing capacity at Intel had to be shared by product divisions. Sharing was possible because fabrication sites could be fairly easily converted from DRAM to EPROM or microprocessor production. It was necessary because in boom times Intel's fabrication facilities would be running at capacity, requiring allocation of production between products. Deciding which type of product to put on a wafer at the start of the sequence of production steps was a key decision. Manufacturing capacity was therefore allocated based on the maximize margin-per-wafer start rule. The maximize mar-

gin-per-wafer start rule, which involved a complex calculation (Cogan and Burgelman, 1990), was consistent with Intel's profit orientation. The VP of Finance at the time pointed out that managers could deviate from profit maximization only if they could justify it for strategic reasons. Sometimes DRAM managers would be asked to write a symbolic check to bearer—'to support customers'—for the amount of margin foregone when DRAMs would bump a higher margin product (Cogan and Burgelman, 1990).

The maximize margin-per-wafer start rule guiding manufacturing resource allocation seemed to capture a great amount of information about the internal and external conditions. It was clear that high margins did reflect competitive advantage in the EPROM and microprocessor product offerings. But the application of the rule also started a vicious circle for DRAMs. Within those manufacturing plants capable of producing different types of products, the allocation rule led to a gradual mix change in favor of EPROMs and microprocessors. This process of incremental decommitment to DRAMs started with the 16K generation (**E6**) and continued throughout the boom period of late 1983 to early 1984. In 1984 DRAM production was restricted to one fabrication site (in Oregon) out of a network of seven plants (Cogan and Burgelman, 1990).

Falling behind reinforces the impetus process

Falling behind in the market made it difficult for the DRAM business managers to compete with Intel's other businesses for resources. Business managers had tried to reposition Intel's single-power-supply 16K DRAM as a niche product that would fetch a higher unit price ('2x'). They had expected that eventually the whole 16K market would have to go for single-power-supply. This did not happen for the 16K generation, however, and further impetus for exit was gained when the strategy to reposition Intel's DRAMs as niche products failed (**E9**; Cogan and Burgelman, 1990).

Repositioning

Intel was already late in the 64K generation and Japanese companies had entered the DRAM market in 1979. In addition, Intel's 64K product design was flawed and expected to result in uncompetitive low manufacturing yields (**E10**). The DRAM process technology group responded by introducing a new process technology called 'redundancy', as a way to overcome the low yield problem (**E11**). This new process, however, had a major defect which showed up late in its development. Intel introduced its 64K DRAM with redundancy only in 1982. These delays were fatal for Intel's strategic position in the 64K generation. A former General Manager of the Memory Components Division (during the early 1980s) said that he took a 1-week trip to see the Intel sales engineers and explain that Intel would be late. He said (Cogan and Burgelman, 1990: 15):

> The sales force was very disappointed in the company's performance. Any sales force wants a commodity line. It's an easy sell and sometimes it's a big sell. That trip was perhaps the most difficult time in my whole career. When I announced we would be late with the product, the implication was that Intel would not be a factor in the 64K generation.

Having assessed that they were behind in the 64K generation, the DRAM process technology group took another gamble. They had come up with yet another innovative process technology—complementary metal-oxide semiconductor (CMOS)—which was to eventually supersede the standard n-channel MOS (NMOS) technology. They decided to apply the CMOS technology to a new 64K DRAM product as well as in the 256K generation (**E16**). This raised the difficult question for the memory components division about how to effect the transition from NMOS to CMOS. The NMOS products had been made at the Chandler (Arizona) facility, but that capacity had been shifted to microcontrollers based on the maxmize margin-per-wafer start rule. In early 1984, the decision was made to phase out the NMOS line (**E17**).

The former General Manager of the Memory Components Division (during the early 1980s) said that the new business strategy was to reposition Intel in DRAMs. The idea was to create a niche market with premium pricing for 64K and 256K CMOS products, so that Intel could maintain a memory presence while accelerating back into an overall leadership position at the 1 Meg (Megabit) generation. But for both the 64K and 256K DRAM products, the innovative solution

did not produce competitive advantage. The large majority of customers for the 64K generation were looking for standard products of high quality (few defect devices) at low prices. Japanese companies provided what customers wanted at very low prices. The Japanese had introduced standard 256K DRAMs in 1982 (**E12**), and Intel had fallen far behind the Japanese in manufacturing yields (**E13**). Intel entered with its CMOS 256K product only in 1984, and it remained a small niche product. The former General Manager of the Memory Components Division (during the early 1980s) said that standard DRAMs were being sold at less than half of the price Intel was asking, and the improved performance of the CMOS chips just wasn't worth it to most customers. Intel's repositioning effort resulted in completely losing strategic position in the DRAM market. Intel's market share shrunk from more than 80 percent in the 4K DRAM generation in 1974 to less than 1 percent in the 256K DRAM generation in 1984 (Cogan and Burgelman, 1990). Repositioning thus failed to reestablish Intel as a key player in the industry. Also, prices for the niche products were lower than expected, making it harder for DRAMs to compete with other products for Intel's scarce manufacturing resources.

The Director of Technology Development observed that Intel's DRAM business had entered a 'death spiral'. In the face of strong competition from Japanese manufacturers, business managers' focus on the more profitable products and technology development's preoccupation with leading-edge processes contributed to missing the DRAM mainstream market. This led to cutbacks in manufacturing capacity and budgets which made it even more difficult to compete. This manager, in an interview in October 1988, anticipated a similar vicious circle ('death spiral') for EPROMs, which had also become a commodity product, and correctly foresaw the decision to exit from EPROM manufacturing, which happened in 1991.

Strategic context

For Intel's top management, the strategic context of DRAMs had always been very clear. DRAMs had very strong legitimacy. DRAMs was the business that 'made Intel', as one senior manager put it, and some top managers, including the CEO, viewed DRAMs as a core business and one that served as technology driver on which the learning curve of the company depended. It was not easy for top management to admit that the legitimacy of DRAMs was vanishing. And it was difficult to decide to exit from DRAMs even though objective analysis seemed to suggest that this was the appropriate course of action in light of Intel's strategic alternatives.

Undermining activates strategic context dissolution

The dissolution of the strategic context of the DRAM business took several years. It happened gradually with the incremental decommitment in allocation of manufacturing resources at the business level. Intel's VP of finance (in 1984–85) pointed out that until 1984 the allocation of scarce manufacturing capacity decisions, while strategic in their implications for the DRAM business, were not considered 'strategic' by top management. They were viewed simply as short-term profit-maximizing responses in the face of a limiting production constraint. In 1984, however, when DRAMs were down to one production site and the challenge of the 1 Meg DRAM required new fabrication facilities, top management was forced to face up to the dissolving strategic context for DRAMs. When it became clear, in November 1984, that the proposal to regain leadership in the 1 Meg DRAM generation implied a capital investment decision of several hundred million dollars for new fabrication facilities, top management decided against it.

Technological uncoupling solidifies strategic context dissolution

To some extent Intel was lucky that its distinctive competencies in design and process technology had generated new business opportunities—EPROMs and microprocessors—that provided unplanned alternatives to the DRAM business. In 1984, however, the new corporate strategy of Intel the 'microcomputer company' had not yet been explicitly stated. Yet, some middle-level managers made technological choices that helped define the strategic context for the microprocessor business at Intel, while further dissolving that of the DRAM business. A critical decision in 1984 involved a technological choice that uncoupled commodity Static Random Access Memory

(SRAM) process technology from process technology development for microprocessors (**E21**). Process technology development for the new 80386 microprocessor was taking place in parallel with process technology development for both a new, high-volume commodity-type SRAM and a specialty SRAM under the direction of the same middle-level functional manager. The specialty SRAM process was applicable to the 80386 microprocessor; the commodity SRAM process was not. This manager decided in mid-1984 to drop the commodity SRAM process. He said: 'Basically, we sacrificed the high-volume SRAM for the 386.' The manager pointed out that Intel 'bet the company' on the 80386 and compounded the risk by changing many things at once—both design and process. He was under great pressure to come up with a very advanced process and was determined to consolidate the SRAM effort with the microprocessor effort. His decision, however, had repercussions for Intel's participation in commodity memories, including DRAMs. In an interview in Ocober 1988, Andy Grove recalled:

> By mid '84, some middle-level managers had made the decision to adopt a new process technology which inherently favored logic (microprocessor) rather than memory advances, thereby limiting the decision space within which top management could operate. The faction representing the ×86 microprocessor business won the debate even though the 386 had not yet become the big revenue generator that it would eventually become.

The uncoupling of DRAM and microprocessor technology development created a dilemma for top management: DRAMs were still viewed as a key *technology* for Intel, but the DRAM *business* was highly unprofitable and further investments seemed hard to justify. This dilemma triggered a debate about the strategic importance of DRAM technology. A former General Manager of the Memory Components Division (1983–85) reported that there was an argument that eventually all DRAM would be integrated on to the microprocessor chip and that the ability to produce state-of-the-art memory would lead to a competitive advantage in microprocessors. He also said, however, that other technical arguments indicated that the chip size would have to be too large to make such a device, so that in the foreseeable future the two technologies would not be integrated. The latter argument won.

The debate concerning the importance of DRAM process technology was nested in a broader debate about the scope of Intel's core technologies. In the period October to December 1984, Intel top management considered closing one of its three process technology sites (**E23**). The VP of Finance pointed out that there were a series of critical process technologies (DRAMs in Oregon, EPROMs in Santa Clara, SRAM and microprocessors in Livermore), and the question Intel faced was how many of these technologies it could do well. He said, 'The question is what do you need to look like if you want to win? How do you avoid spending on all and losing on all?' This manager also said that the critical factor in Intel's choice was the evolution of protection of intellectual property. Intel had cross-licensed everything in DRAMs, but had not yet done this for logic. So the company could still protect microprocessor technology. A former general manager of the memory components division (early 1980s) pointed out that in the background of the decision to exit DRAMs was the sense that more corporate technological resources needed to be focused on logic development. This manager described the DRAM process technology group as the best corporate resource available. Several other managers reported that Andy Grove was a strong proponent of moving the DRAM process technology group to microprocessor development (**E30**). Grove was able to separate the product–market (business) aspect of the DRAM exit from the competence (technology) aspect. He realized that product-market exit did not necessarily mean losing all of the key competencies currently associated with DRAMs. In December 1984, Intel decided to close the Livermore site and to consolidate microprocessor process technology with the DRAM group in Oregon (**E26**). The DRAM process technology group, however, successfully petitioned top management to be allowed to continue to develop prototypes of the 1 Meg DRAM in order to demonstrate functionality (**E25**).

Strategic recognition completes strategic context dissolution

Strategic recognition came in two steps: Intel's top management recognized what it did *not* want the company to become before it recognized what it *did* want the company to become.

Midde-level managers associated with the

DRAM business wanted Intel top management to recognize the fact that the company was competing in two different businesses—a commodity business (DRAMs) and a specialty business (microprocessors)—and to reorganize accordingly. As early as mid-1982, the manager of several fabrication sites, including the fabrication plant effectively dedicated to DRAMs in Oregon, had proposed to realign his fabrication facility with the memory component division to create a coherent, dedicated DRAM organization (**E14**). Top management did not approve the reorganization (**E15**), and DRAM wafer starts continued to be pressured by the contribution margin decision rule. In early 1984, the manager of the DRAM fabrication plant in Oregon proposed an investment of $80 million for an upgrade of the facility (**E19**). His plan was to create a state-of-the-art, dedicated DRAM facility that was cost competitive with any other facility in the world. This manager thought the battle for DRAMs should be fought in the manufacturing arena, focusing on manufacturability and cost, rather than on the leading-edge process technology. But the investment plan was not approved by top management (**E20**). These proposals, however, helped top management recognize that they did *not* want Intel to become a supplier of commodity products.

Intel's decision in November 1984 not to invest in new fabrication facilities for the 1 Meg DRAM was a *de facto* exit decision (**E24**). This decision reflected top management's strategic recognition that Intel was not equipped to compete in the commodity business that DRAMs had become. The completion of the exit process, however, took almost a year. During 1985, the company continued to manufacture 64K and 265K DRAMs in its Portland facility, the last remaining DRAM fab. Also, since it was unclear what to do with the Portland-based DRAM technology development group, top management had allowed the group to keep working on prototypes of the 1 Meg DRAM and these efforts continued until March 1985 (**E25**, **E28**). Furthermore, DRAM business managers and the General Manager of the Components Division were still looking, in 1985, for ways to stay in the business. But they were not able to come up with a new strategy that would not require heavy capital investment. One final effort to salvage Intel's product–market presence in DRAMs involved the head of DRAM Memory Components (in 1985), who proposed a strategic alliance with a Japanese partner to trade Intel's CMOS 256K DRAM design and process technology for manufacturing by the partner (**E27**). This proposal was supported by the general manager of the components division, who reported directly to COO Andy Grove (**E29**, **E32**). At the last moment, in late summer 1985, this proposal was rejected by top management (**E33**). By then, there was great tension and confusion within the organization about what to do about DRAMs. Asked, in an interview in January 1989, how the situation was finally resolved, Andy Grove said that in the summer of 1985 he went to see CEO Gordon Moore and asked him what would happen if new top management were brought in. Grove said that Moore told him that new management would probably want to exit from DRAMs. Grove then suggested to Moore 'that we go through the revolving door, come back in, and just do it ourselves.' Grove then took personal charge of the implementation of the DRAM exit and reassigned the general manager of the components division (**E34**).

The VP of Finance pointed out that the 1985 semiconductor recession forced Intel to examine which of its fabrication sites could be closed. The Portland fab was a clear candidate, given the losses that Intel was incurring in DRAMs. Closing the Portland fab, however, was no longer a question of capacity allocation but rather one of deciding whether or not to keep the capabilities associated with DRAMs. Intel made the decision, in October 1985, to close the fabrication plant in Oregon (**E31**, **E35**, **E37**). This concluded the strategic exit from DRAMs. By then, top management had come to recognize that the future of Intel lay in becoming a leading microcomputer company. This was the message Andy Grove delivered when he went to address the Oregon group in October 1985 (**E36**).

Rationalization produces organizational learning

The case data indicate that looking back at the DRAM experience, Intel top management realized that, on balance, the strategic business exit from DRAMs had worked well for Intel. This allowed Andy Grove to go around the company and retroactively rationalize the strategic exit from DRAMs. Grove reportedly told groups of Intel managers that the DRAM business had supported

the company for over 10 years, had been well managed, had developed key corporate resources which were redeployed when needed most, and was a business that Intel exited at just the right time.

In several interviews in early 1989, Andy Grove pointed out that Intel had learned from the DRAM experience to raise questions about the scope of the company's technology strategy. Grove pointed out that top management realized it needed to look at its various technologies (associated with different businesses), ask 'Am I the best in the technology?' and then decide what to fight for. He said 'If it is my best technology, I will fight tooth and nail.' He pointed out that the belief, in 1984–85, that DRAM technology was critical for Intel's future was erroneous. The technical competencies deployed in DRAMs—especially linewidth reduction—*were* critical, but these could be preserved and redeployed in microprocessor technology which really was Intel's best. Grove noted that, in 1989, top management faced a similar decision with EPROM technology. He said that he anticipated perhaps only one more generation of EPROMs as a separate technology at Intel. Asked how he reconciled this anticipation with having to convince people to keep working on it in the meantime, he said:

> Not very well! It is a very ambiguous, sensitive deal. You need to be able to be ambiguous in some circumstances. You dance around it a bit, until a wider and wider group in the company becomes clear about it. That's why continued argument is important. Intel is a very open system. No one is ever told to shut up, but you are asked to come up with better arguments. People are allowed to persist.

Referring back to EPROMs, Grove said that '"X" (a manager assigned to study and make recommendations for Intel's memory businesses in 1986 who had emphasized the importance of EPROM technology for a new type of semiconductor called "Flash") will work even harder to show you wrong (in getting out of EPROMs).'

Structural context

Selecting

From the start, Intel had a strong profit-oriented culture. Earlier I described the powerful selective consequences of the maximize margin-per-wafer start rule used to allocate manufacturing capacity for the DRAM business. This rule reflected the different competitive reality facing Intel's memory ('commodity') and microprocessor ('specialty') businesses. The strong selective consequences of this rule for DRAMs were not fully anticipated and sometimes not quite liked by some top managers. Nevertheless, these top managers abided by the rule that they had established. They did not undo the capacity allocation decisions made by middle-level managers that undermined the strategic context of DRAMs. The VP of finance said that there was some dissatisfaction on the part of the DRAM business managers about the allocation rule being biased against DRAMs, but that in the capacity allocation decision processes about 80 percent of the allocated costs were not at all argued about, 10 percent yielded 'shrugged shoulders,' and 10 percent elicited a 'those jerks' comment from the memory managers. Hence, the questioning of the allocation rule on the part of operational-level managers had little impact.

Negotiating structural change

Another important element of Intel's structural context was the encouragement of open debate. The prevailing rule, established by top management, was that knowledge power should not be dominated by position power (Grove, 1983) and that there should be open debate about the business and technical merits of any proposal. As reported earlier, Andy Grove maintained that Intel was a very open system where no one was ever told to shut up, and where decisions were made based on the force of argument. This culture supporting unfettered debate made it possible for middle-level managers associated with the DRAM business to challenge the way Intel was pursuing the business and to propose a major reorganization. And, simultaneously, for other middle managers to make decisions that undermined the idea of Intel as a memory company and pushed the company further toward becoming a microcomputer company.

Structuring and restructuring

The dissolution of the strategic context of DRAMs had been accompanied by rising tensions among middle managers and top management.

Top management had begun to recognize that there was an imbalance between technology investments in DRAM and capacity allocation, and that this was symptomatic of a more fundamental decoupling of strategy and action. Top management was now asking: why are we investing so much in DRAM process technology (one third of all process technology investments budgeted for 1985 were for DRAMs) if DRAMs are so unprofitable and if we have more profitable alternatives? This made them realize that a major source of the difficulty came from the fact that technology development decisions and the capacity decisions were made in different parts of the organization. They began to reconsider other aspects of the structural context than simply the resource allocation rule. They asked: is our organizational structure not designed to compete effectively in a commodity business? Or is it a bad business to begin with? These questions reflected their strategic recognition, reported earlier, that Intel had become a microcomputer company and that a new corporate strategy and some changes in the structural context were necessary (**E38**).

DISCUSSION

Limitations

The limitations of the field research on which this paper is based have been discussed in earlier work (Burgelman, 1991, 1994). The process model of SBE presented in this paper has several additional limitations. First, the process model of SBE does not aim to cover the entire range of issues associated with SBE. The study reported here focuses on the intrafirm pattern of managerial activities associated with SBE. Also, the process model of SBE presented here is the result of qualitative pattern matching using the Bower–Burgelman process model. While this pattern matching has been done carefully and objectively, the patterns found necessarily reflect the conceptual lens used. The process model presented here is an attempt at bounding the set of managerial activities involved in SBE but must be verified through further research. Finally, process models show the pattern of managerial activities through which a strategic outcome such as SBE comes about, but do not seek to explain variation in this pattern (Mohr, 1982; Burgelman, 1985). Further research involving large samples is needed to identify the contingency factors that might explain variance in the SBE process across different types of organizations in different types of environments. Such research may indicate which managerial activities are missing or redundant in the present SBE process model, and whether the pattern of sequential and simultaneous activities as depicted here needs to be modified, and how.

Substantive theoretical insights

Process models of substantive areas of strategy making such as SBE provide windows into the 'black box' of strategy making in complex organizations. Their approach is positive-descriptive and they help identify and explain paradoxes, vicious circles, dilemmas, and tensions in the strategy making process that derive from the activities of managers that are differentially situated in the organization and respond to different external and internal pressures. For instance, the process model of SBE shows how the process technology competence that allowed Intel to be the first successful mover in DRAMs paradoxically also bore the seeds of its failure in DRAMs later on. It explains how a vicious circle ('death spiral') in resource allocation to DRAMs resulted from some middle-level managers' inertial deployment of process technology competence, which failed to meet competitive challenges in DRAMs, while others responded to the internal pressures of the structural context by moving scarce manufacturing capacity away from DRAMs. The model helps explain how top management's uncertainty about the importance of DRAM technology created a dilemma on their part in deciding whether or not to exit from the DRAM business, and how middle-level managers contributed to resolving the dilemma by making technology choices that favored microprocessors over memories. And, it explains how managerial factions aligned with DRAMs, EPROMs, and microprocessors created tensions associated with competition for resources in the corporate context, and how this led top management to change elements of the structural context.

Developing a grounded process model for a substantive area such as SBE helps produce categories and concepts that are somewhat rudimentary and evocative but are closely tied to the phenomenon and enrich the repertoire for concep-

tualizing it. In this respect, the present study has identified unlinking and repositioning; resource shifting and technological uncoupling; and strategic recognition and structuring as key categories of managerial activity, performed by different levels of management, that shaped the SBE process. The study has also shown how these activities brought about the dissolution of the strategic context of a core business of the firm. Linked together in the process model these categories and concepts depict the complex pattern of managerial activities and organizational forces associated with the SBE phenomenon in a parsimonious way and show the underlying order and sources of rationality in a process that, at the surface, looks chaotic.

Comparing the process model of SBE to process models of other substantive areas of strategy making provides additional insight. The SBE process was different in several respects from the process of ICV (Burgelman, 1983b). New business development through ICV was structurally separated from the mainstream operations through the use of a new venture division. This purposefully protected new businesses for some time from internal competition for resources and provided some leeway for operational-level product championing and middle-level organizational championing activities. Strategic context determination for a new venture was expected to involve a positive, upward spiral of growth. SBE, in contrast, took place in an integrated organizational structure where the DRAM business (and later EPROMs) could not escape the internal competition for resources with other businesses. Strategic context dissolution of memory businesses involved negative, downward spirals of decline. This made product championing and organizational championing for memory businesses impossible tasks, like swimming against an overwhelmingly strong tide.

The SBE process was also different from the divestment process (Gilmour, 1973). Gilmour's study of the divestment process suggested that impetus preceded definition in the process model. He also found that the divestment process was more driven from the top than the strategic capital investment process (Ackerman, 1970; Bower, 1970). The divestment decisions studied by Gilmour were of the portfolio planning type with little need to consider competence linkages between the divested business and the remaining ones. Gilmour's study also did not examine the antecedents of the performance discrepancies that triggered the divestment process. The study of Intel's exit from DRAMs suggests a more complex picture because there were competence linkages among businesses and inertial competence deployment was an important antecedent to the performance discrepancies. The present study provides some support for Gilmour's finding that the impetus process started before the definition process. But it was the unlinking of customer needs and Intel DRAM products in the 16K generation that initiated the definite thrust to exit, led to the falling behind of DRAMs in the market, and reinforced the impetus part of the process which had already been activated by the shifts in resource allocation away from DRAMs. The comparison with the divestment process model also corroborates the importance of distinguishing between the impetus and strategic context parts of the process model. This distinction, which was not available to Gilmour, allowed the study of SBE to disentangle the manufacturing capacity allocation decisions from the strategic choices concerning core technologies. While the former provided impetus for exit, it was the latter that dissolved the strategic context of DRAMs and convinced top management that DRAMs were no longer a core business.

The process model of SBE supports theory that views the notion that top management defines the strategy which is then expeditiously implemented as an incomplete representation of strategy making and enactment processes (e.g., Mintzberg, 1978; Mintzberg and Waters, 1985; Quinn, 1978; Weick, 1979) and of organizational change more broadly defined (e.g., Grinyer and McKiernan, 1990; Pettigrew, 1990; Levinthal, 1991). The process model of SBE underscores the difficulty of establishing who the relevant 'actor' is (Allison, 1971) when considering strategic interaction involving complex organizations, and it provides additional insight in the internal sources of inertia in strategic response and the myopia of organizational learning (Levinthal and March, 1993). The SBE process models also help see why the application of formal theories of competitive interaction, such as game theory (e.g., Camerer, 1991; Saloner, 1991), is problematical when complex players like Intel are involved.

Intel was able to exit effectively from DRAMs and preserve and redeploy important corporate

competencies without having to rely on extraordinary foresight on the part of top management. Three key factors contributed to this. First, top management had created an internal selection environment that led differentially positioned managers to take competitive reality into consideration when allocating scarce resources and put the burden of proof on those managers who wanted to forego profits for 'strategic' reasons. Second, the company's tradition of open debate made sure that those managers could, in fact, make their arguments. And, third, top management's strategic recognition capacity led them to draw decisive conclusions concerning, at first, what Intel *should not* become and, later, what it *should* become. These three factors, together, may help clarify what some have called organizational 'capability' (e.g., Teece *et al.*, 1990). One important manifestation of corporate capability is a company's ability to adapt without having to rely on extraordinary top management foresight.

The SBE process model documents one manifestation of corporate capability. Matrixing levels of management by levels of strategy making helped elucidate the interplays between business-level and corporate-level strategy making. Conceptualizing the complete process—depicting simultaneous as well as sequential managerial activities and contextual forces–also helped illuminate the difficulties in establishing when exactly the strategic exit decision was made and when strategic business exit had actually occurred. The process model of SBE thus can be useful for practitioners. As a diagnostic tool it may draw top management's attention to business-level strategic activities that are already clearing the road to exit but of which the corporate-level strategic implications have not yet been fully realized, and vice versa. It may also help top management assess more carefully the evolving links between business-level product market issues and corporate-level competence issues.

Toward an evolutionary process theory of strategy making

Grounded theory about substantive areas of strategy making establishes the foundation for formal theory building (Glaser and Strauss, 1967). Linking substantive research in strategic management to discipline-based intellectual traditions in organization theory and organizational economics may offer the best opportunity for developing cumulative knowledge (for an alternative view see Bartlett and Goshal, 1993). Earlier work has proposed that the process model of ICV could be subsumed under the framework of evolutionary organization theory (Burgelman, 1983a). The process model of SBE, too, can be fruitfully linked to evolutionary organizational theory. SBE was found to be shaped by intraorganizational ecological processes that determined the ascendance (microprocessors) and decline (DRAMs) of different businesses in the firm's internal selection environment. The ICV and SBE process models show that the Bower–Burgelman process model continues to be a useful conceptual tool to depict the pattern of activities of managers involved in these intraorganizational ecological processes. It augments the tool kit of a theoretical perspective that shifts the locus of selection from the firm as a whole to classes of strategic action inside the firm and views managing intraorganizational ecological processes as a means by which the firm can achieve the learning benefits of both external and internal selection (Burgelman, 1991, 1994; Rumelt, Schendel, and Teece, 1994; Barnett, Greve, and Park, 1994).

Process models of strategy making using the Bower–Burgelman approach help illuminate the working of internal selection processes. In particular, documenting the multilevel interplays of managerial activities involved in strategic context determination and dissolution elucidates the subtle intertwining of internal selection and coordination, and the value-added activities of middle-level managers. In the case of ICV, strategic building and organizational championing were value-added activities of middle-level managers because they provided a rationale for continuing to move resources into new businesses and thereby helped determine the strategic context for these businesses in the corporation (Burgelman, 1983b). In the case of SBE, resource shifting and technological uncoupling were value-added activities because they released scarce resources from businesses in which the company's strategic position was weak and thereby helped dissolve the strategic context of those businesses within the corporation. ICV and SBE may thus both be viewed as part of the Schumpeterian process within the firm that materially changes its resource allocation pattern (Burgelman, 1983c). Documenting the intrafirm Schumpeterian process

also informs the resource-based view of the firm which examines how firm-specific resource combinations become sources of competitive advantage.

The ICV and SBE process models can also be connected to the literatures on escalation and exit and institutionalization and deinstitutionalization (e.g., Ross and Staw, 1993), and permanently failing organizations (Meyer and Zucker, 1989). Research on ICV discovered that successful strategic forcing—gaining a significant market share with a new product—was necessary to start the process of escalation of commitment to a new venture (Burgelman, 1983b, 1988). The SBE study found that if the structural context comprises a resource allocation rule that reflects competitive reality, like the maximize margin-per-wafer start at Intel, escalation of commitment to a losing business is less likely. Intel's structural context forced internal shifts of resources from unsuccessful to successful businesses and thus prevented the company from getting stuck in the pattern of low performance associated with permanently failing organizations. While the ICV study found that managerial activities involved in determining the strategic context for a new venture were an instance of 'institutionalization' (Burgelman, 1988), the SBE study suggests that managerial activities leading to dissolving the strategic context of DRAMs were an instance of 'deinstitutionalization'. The latter findings corroborate Ross and Staw's proposition that 'Efforts to deinstitutionalize a project, or separate it from the actual goals and purposes of an enterprise, can reduce organizational determinants of commitment, thereby increasing the propensity for withdrawal' (1993: 728), but they go beyond it by documenting in more detail the pattern of managerial activities resulting in deinstitutionalization/strategic context dissolution.

By elucidating the internal selection processes, process models of strategy making also contribute to the debate concerning the prevalence of punctuated equilibrium models of strategic change (e.g., Tushman and Romanelli, 1985; Gersick, 1991; Romanelli and Tushman, 1994). Intel's transformation from memory into microcomputer company seems at first to have been a rather abrupt organizational-level change taking place in the 1984–85 time frame. A closer look at the strategy-making processes that played out in the late-1970s to mid-1980s time frame, however, reveals that the organizational-level change was the culmination of gradual replacement of memories by microprocessors as the core business of Intel—a change that took top management a relatively long time to come to grips with. The process model thus calls into question the universal applicability of the punctuated equilibrium model and may help establish more precisely how and when strategic change takes place. Strategic change may take place before it is recognized or acknowledged as such by top management.

IMPLICATIONS AND CONCLUSIONS

For more than 25 years, process model research has made useful contributions to our understanding of strategy making in a variety of substantive areas and in a variety of firm types. The process model of SBE presented in this paper is another modest contribution in that intellectual tradition. It provides additional insight into how the activities of differentially positioned managers add value in the firm's strategic processes, and underscores the importance of studying the role of middle-level managers in strategic management. It also shows that the Bower–Burgelman process model continues to serve as a useful tool to conceptualize the patterns of strategic managerial activities associated with the evolution of large, complex firms.

In the evolution of large, complex firms, new forms of organization labeled as 'nonhierarchical,' 'network,' 'boundaryless,' 'virtual,' and the like, have recently emerged. Several research questions derive from the Bower–Burgelman process model that can shed light on strategy making in these new organization forms. For instance, how is the strategic context for alliance formation determined or dissolved within each of the participating organizations in a network? What is the role of differentially positioned managers in favoring or opposing strategic alliances? How do operational and/or middle-level managers from one organization cross organizational boundaries to affect the strategic context determination/dissolution process to the network's advantage, or to that of their own organization? And so on. Addressing these sorts of research questions would enrich the literature on strategic management and our understanding of these new forms of organization. Such research could provide deeper insight into the

limits of effective managerial hierarchies and provide some guidance for the restructurings, currently in vogue, of organizations that have extended their managerial hierarchy beyond those limited.

Conclusions

Intel Corporation's transformation from memory to microcomputer company suggests that firms continue to exist, in part, because old product-market strategies get replaced by new ones, and old distinctive competencies give way to new ones. SBE plays a key role in these evolutionary processes. Surviving firms effectively substitute, to some extent, internal selection for external selection. That is, in surviving firms, resource allocation and reallocation, and competence deployment and redeployment, are effectively governed by internal selection processes. In large, complex organizations, these internal selection processes involve the combined activities of differentially positioned managers. This is why evolutionary theories of the firm must take strategy-making processes seriously, and why resource-based views of the firm must take managerial action seriously.

The process model of SBE presented in this paper also provides some evidence that the internal selection processes, which sometimes produce corporate transformations, are both more continuous and less centrally driven than the punctuated equilibrium model of organizational change seems to suggest. The process model of SBE is therefore a potentially useful building block in theory about the role of internal selection processes in firm evolution.

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APPENDIX: RESEARCH METHOD

Research setting

The research was carried out at Intel Corporation, a major high-technology firm. Intel was founded in 1968, and was the first company to specialize in making large-scale integrated circuit memory products. The company's strategy in 1968 was to build semiconductor memory products for mainframe computers in competition with the 'core memory' standard of the day. In 1984–85, when Intel decided to exit from the DRAM business, the company had reached a sales volume of about $1.5 billion and was already well established. In 1991, the time when the research reported here ended, Intel was a leading microcomputer company that had survived for more than 20 years as an independent company in an extremely dynamic industry. The firm grew from $1 million in sales in 1968 to $4.8 billion in 1991. Profits rose from a loss of $2 million in 1969 to over $800 million in 1991.

Research design

The study was based on a longitudinal, two-stage, nested case study design within one corporate setting (e.g., Yin, 1984; Leonard-Barton, 1990). While concentrating on one organization with more than 20 years of continuity in leadership limits generalizability of the findings, it also made it possible to gain access to sources with intimate knowledge of the details of the firm's evolution. The research capitalized on the opportunity to gain understanding of 'the manager's temporal and contextual frame of reference' (Van de Ven, 1992: 181). It also capitalized on the possibility to reconstruct the SBE with input from people at the different levels of management involved in the SBE process. This provided a basis for triangulation and may alleviate some of the concerns associated with retrospective data (e.g., Golden, 1992).

Archival and interview data were collected on the evolution of two semiconductor memory businesses—DRAM and EPROM—and the microprocessor business at Intel. These cases were selected for theoretical reasons as an intentional sample (Glaser and Strauss, 1967; Eisenhardt, 1989). The selection criterion was strategic importance to the firm. DRAMs was the business that had made Intel successful during the early 1970s. EPROMs, during the mid-1980s, still accounted for about 15 percent of Intel's business. Microprocessors had become Intel's largest source of revenue by 1982 and grew rapidly during the mid-1980s.

The research was carried out in two stages. The first stage, from fall 1988 through spring 1989, focused on the decision to exit DRAMs during 1984–85. The second stage of the research, from fall 1990 through spring 1991, focused on the implementation of the DRAM exit decision. It sought to document the difficulties that Intel encountered in getting the organization to stop all activity in DRAMs. During this stage of the research, Intel top management also made important decisions regarding EPROMs and microprocessors.

Data collection

Interview and archival data were collected. All data collection was longitudinal. For DRAM, data were historical, covering the period 1971–85. For EPROMs and microprocessors, historical data were combined with current data obtained during the research period.

Interview data

Twenty-seven key Intel managers were formally interviewed, many of them repeatedly, yielding close to 200 pages of written interview notes. Seventeen of these managers were interviewed during the first stage of the research. Some top managers who had previously left the company were included as well. Managers from different levels, different functional groups, and different businesses who had been involved in or affected by the decision were asked to discuss the causes of Intel's exit decision. Ten additional managers, most of whom were at lower and middle levels in the organization in the mid-1980s, were formally interviewed during the second stage of the research. These interviews provided a more detailed account of how the DRAM exit decision was perceived and experienced by front-line managers. Many of the managers previously interviewed were contacted again to clarify differences

and discrepancies. Throughout the research period, informal discussions with current and former Intel employees were used to corroborate data obtained from the formal interviews. The head of R&D of one of the leading Japanese photolithography equipment suppliers was also interviewed. This company had had an important impact on the evolution of the DRAM industry, and the interviewee had had significant experience with DRAMs in another major U.S. semiconductor company earlier in his career. Table A1 lists the managers who were formally interviewed, with the job they held in 1984–86 and the number of times they were interviewed.

The interviews lasted between 1 and 2 hours and were open-ended. Follow-up interviews were semistructured, for clarification about key events, people, and issues that had been identified. Key events centered primarily around the introduction of successive generations of products in each of the businesses, because these introductions drove and were driven by the competitive dynamics in the industry. Key people were individuals or groups from different functional areas or different hierarchical levels who made critical decisions, or made proposals that, while not necessarily implemented, triggered high-level reconsideration of strategic issues. Key issues included the importance of DRAMs as a technology driver at Intel; the importance of DRAMs in Intel's product market strategy; the allocation of scarce manufacturing capacity; the allocation of R&D resources to different businesses; the integration of process technology development and manufacturing; the retention and deployment of key talent, and, more generally, Intel's ability to compete in commodity businesses. No tape recorder was used, but the interviewers made extensive notes. I conducted

Table A1. Interviewees

	Job in 1984–86 period (except as stated)	Number of interviews
1.	Chief Executive Officer	2
2.	Chief Operating Officer	4
3.	Chief Financial Officer	1
4.	Senior VP and GM, Components Division	2
5.	Senior VP and GM, Systems Division	2
6.	Director, Assembly/Test	3
7.	Director, Technology Development (TD)	3
8.	Director, Memory Components Division (early 1980s)	2
9.	Director, Memory Components Division (July 1983 to early 1985)	1
10.	Head, DRAM Memory Operations—supervised design, marketing/sales, and customer support	1
11.	Head, Fab 5 TD (DRAM)	3
12.	Head, Fab 3 TD (Logic/SRAM)	1
13.	Head, Fabs 4, 5, 8 (Manufacturing)	1
14.	Head, Fab 5 Manufacturing	1
15.	Proj. Manager, Fab 5 TD—1 μm DRAM	1
16.	Supervisor Fab 3, of TD and manufacturing—group leaders; brought in to make TD and manufacturing integrate their efforts for the 1.5 μm 80386 microprocessor	1
17.	Fab 3 Manufacturing (group leader)	1
18.	Fab 3 Manufacturing—group leader; associated with Component Contracting in 1991	1
19.	Head of Component Contracting in 1991	1
20.	DRAM designer	1
21.	Responsible for closing Barbados assembly and Puerto Rico test facilities in 1986	1
22.	General Manager for Application Specific Integrated Circuits in the Microcomputer Division in 1988	1
23.	Development Manager, Microcomputer Division in 1988	1
24.	Responsible for Intel's Computer Aided Design group throughout the 1980s	1
25.	Product Development Manager for the i860 (RISC) microprocessor in 1988	1
26.	Manager assigned to study and make strategic recommendations for Intel's memory businesses in the mid-1980s	1
27.	Personal Assistant to Andy Grove in 1988	2
28.	Senior VP and Chief Technical Officer, Nikon Precision Inc. in 1991	2

15 of the interviews with a research associate. Transcripts of the research associate's notes, when compared with mine, showed consistent agreement on the substantive content of the interview. This provided some confidence that the data were valid and reliable.

Archival data

Archival data, such as documents describing the company's history, annual reports, and reports to financial analysts, were obtained from Intel. The company also provided a statement on the evolution of Intel's approach to the development of computer-aided design tools throughout the 1980s, written specifically for this research. Additional archival data were obtained from Dataquest and from written materials, such as industry publications, and financial analysts' reports and business press articles about Intel and the semiconductor industry. These archival data made it possible to construct a quantitative picture of the evolution of the semiconductor industry and Intel's evolving strategic position in major segments. The archival data could be juxtaposed to the interview data to check for potential systematic biases in retrospective accounts of past strategy (Golden, 1992). Discrepancies between interview data and archival data discovered in the course of the research raised a number of questions that guided further data collection and analysis. Jelinek and Schoonhoven's (1990) study of the innovation process at Intel was a fortuitous source of additional data as well as a validity check for the new data collected in this study. Data collection was concluded when a level of saturation was reached (Glaser and Strauss, 1967).

Data analysis

In earlier work, the data on the evolution of Intel's corporate strategy was analyzed using the methodology of grounded theorizing (Glaser and Strauss, 1967). The analysis of the DRAM and EPROM cases using the 'constant comparison method' suggested several partly overlapping stages in the chronological development of strategic business exit: (1) Initial success, (2) emergence of external competition, (3) internal competition for resources, (4) growing doubts about the viability of the business, (5) strategic exit decision and implementation, and (6) articulation of new corporate strategy and internal creative destruction of obsolete routines.

Further analysis of the stages of strategic business exit generated a conceptual framework comprising external and internal forces that formed the basis for the articulation of a process theory of strategic business exit (Burgelman, 1994). The present paper uses the Bower–Burgelman process model (Bower, 1970; Burgelman, 1983b) to analyze the intrafirm pattern of managerial activities associated with strategic business exit.