DAY-3 DESIGN LIBRARY CELL USING MAGIC LAYOUT AND NGSPICE CHARACTERIZATION.

1. CMOS inverter ngspice simulations

1: Spice deck

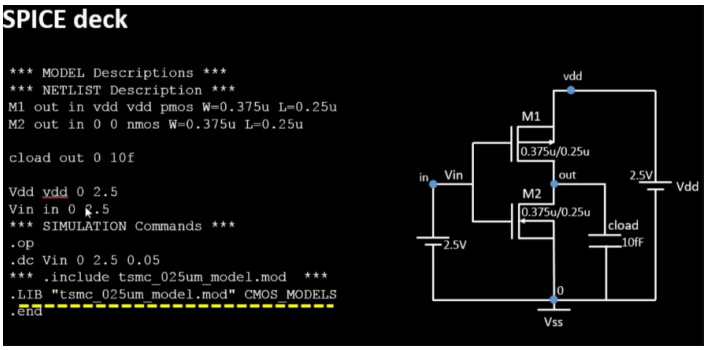
- This image shows a SPICE deck (simulation input file) and a CMOS inverter circuit used for analog simulation.
  Left Side – SPICE Deck:

- Netlist Description:
  - M1 is a PMOS transistor (W=0.375µm, L=0.25µm).
  - M2 is an NMOS transistor (same dimensions).

- Capacitive Load: cload of 10fF between output and ground.
- Voltage Sources:
  - Vdd provides 2.5V to power rail.
  - Vin is the input voltage source swept from 0V to 2.5V in steps of 0.05V.

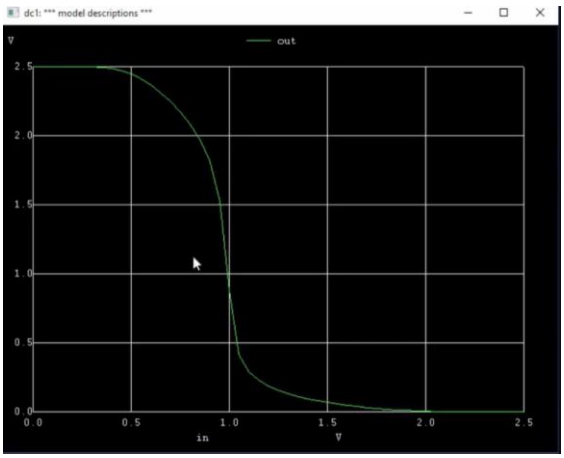
- Simulation Commands:
  - .op: Operating point analysis.
  - .dc: DC sweep of Vin.

  Right Side – Circuit Diagram:
- CMOS inverter using:
  - M1 (PMOS) on top, connected to Vdd.
  - M2 (NMOS) at the bottom, connected to Vss.
- Output (out) node connected to a 10fF capacitor (cload).
- Vin drives the gates of both transistors.

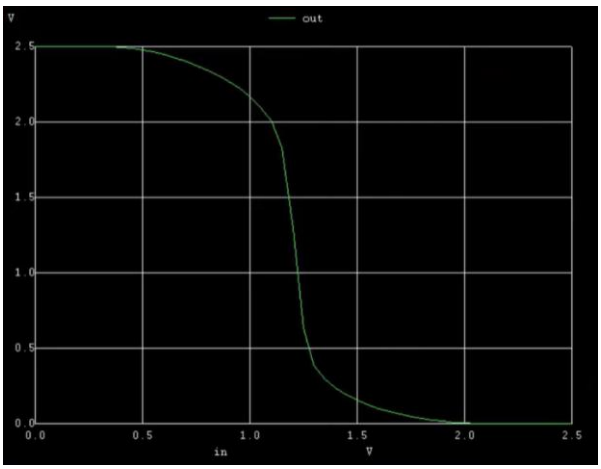


2: Spice Simulation & Switching Threshold

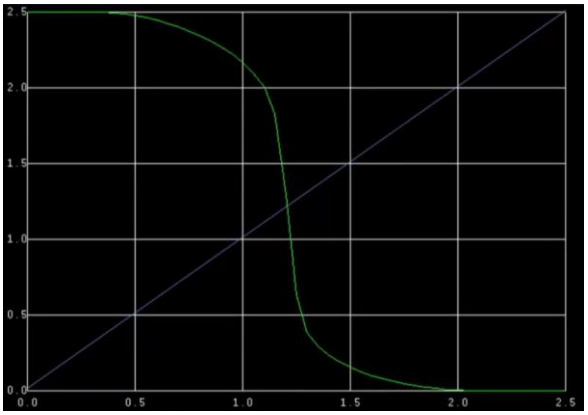
- Where both the nmos and pmos are of equal width.



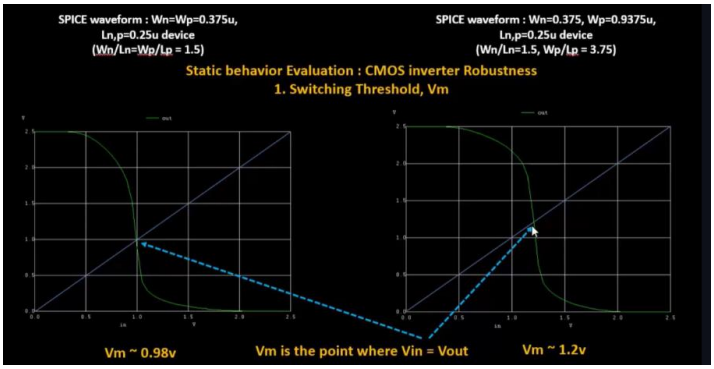
- When width of pmos is thrice to nmos



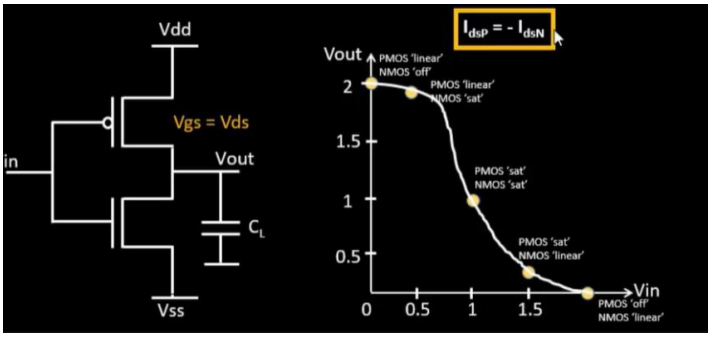
- Switching Threshold is the point where the straight line and the curve meets it determines the ON and OFF for transistors.



- Switching Threshold of two graphs

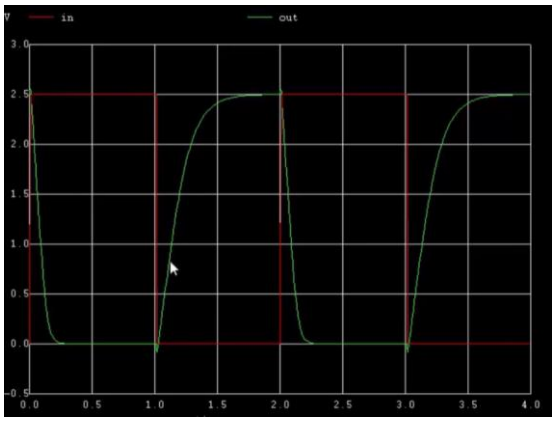


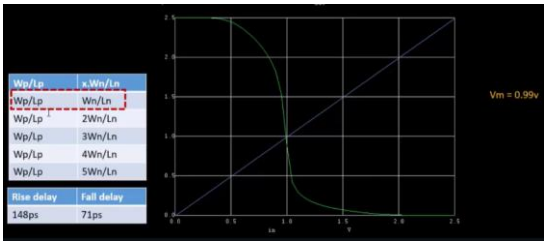
- DC characteristics of nmos and pmos.



3: Spice Simulation & Switching Threshold

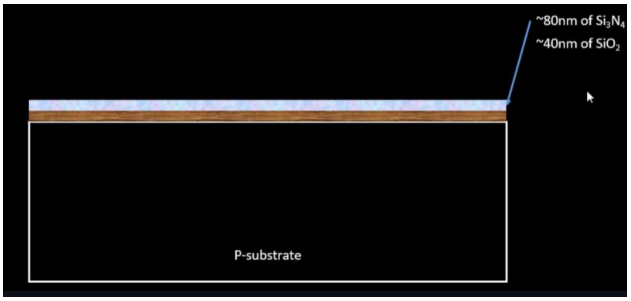
- The graph Time vs Voltage will be plotted here from where we can calculate the rise and fall delay

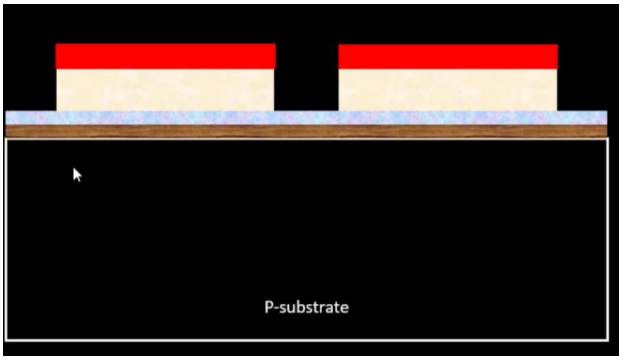


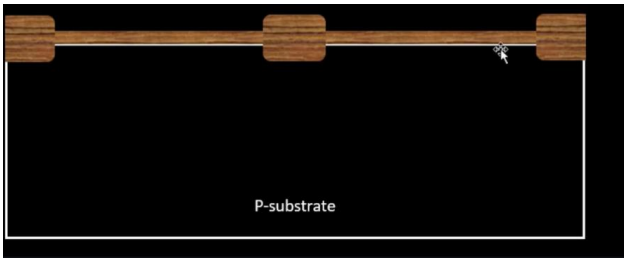


2. Inception of Layout and CMOS fabrication process

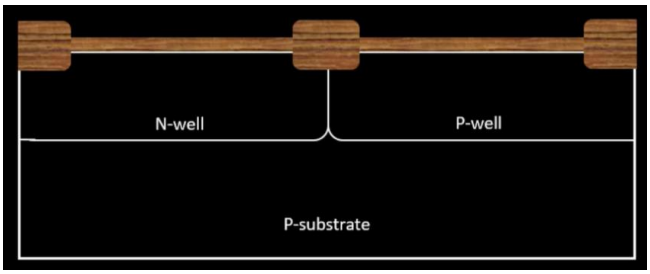
- At each step changes are done such that to achieve a proper fabrication process and make it ready for the further step.
- We select a p type substrate creating a region for nmos and pmos.
- We use Sio2 and Si3N4 layer for isolation
- A photoresist is used which is a light-sensitive material applied to a silicon wafer to define patterns for subsequent processing steps such as etching or doping.
- UV rays are used to etch the area which is exposed.
- We use n type and p type doing substances for creating the well.
- Create Active regions



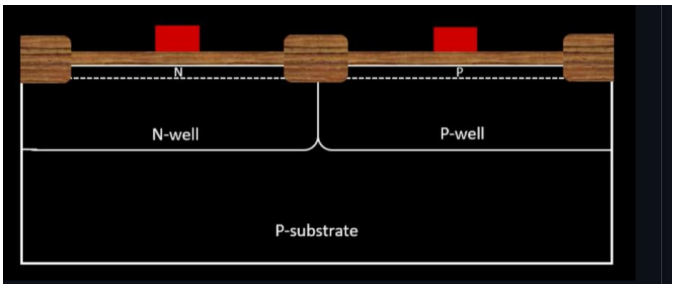




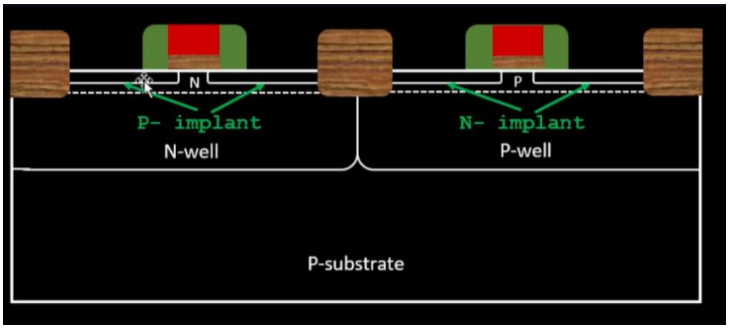
- Formation of N-well and P-well



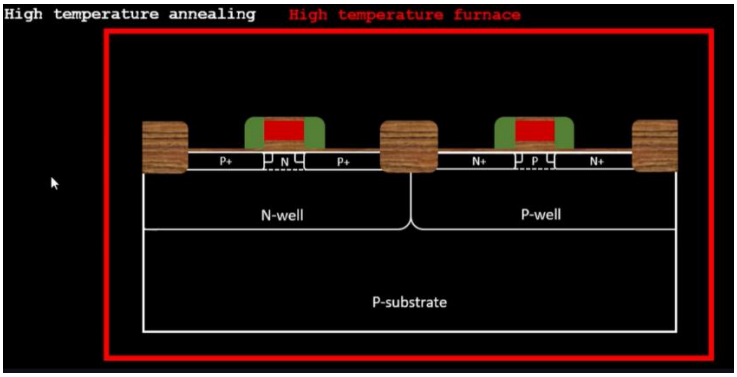
- Formation of gate terminal



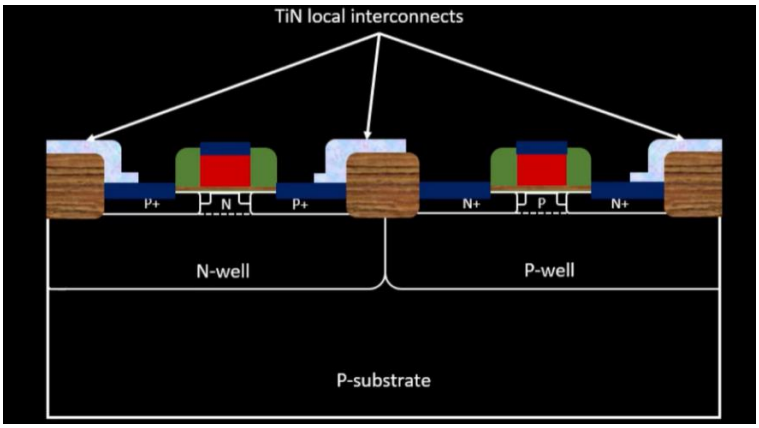
- Lightly doped drain (LDD) formation



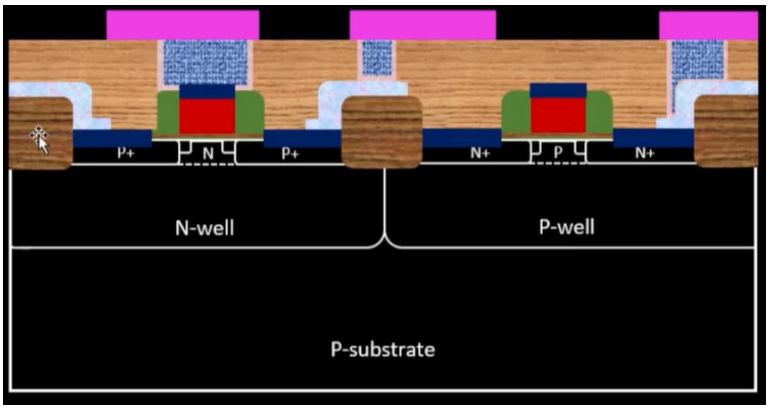
- Source and drain formation



- Local interconnect formation



- Higher level metal formation



- Final fabrication of cmos is as below