A project report on

Design and Analysis of Sense Amplifier in a Pulse Generator of a Cardiac Pacemaker

Submitted in partial fulfilment for the award of the degree of

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CERTIFICATE

This is to certify that the project report entitled "Design and Analysis of Sense Amplifier in a Pulse Generator of a Cardiac Pacemaker" being submitted by the students **Ch. Sree Deepak (20A81A1403), M. Chaitanya Komali (20A81A1432), G. Bhargavi (21A85A1401), J.V.R. Nanaji (21A85A1402), P. Naveen (21A85A1405)** in partial fulfilment for award of the degree of **Bachelor of Technology** in **Electronics and Communication Technology** from **Sri Vasavi Engineering College (Autonomous),** Tadepalligudem, affiliated to the Jawaharlal Nehru Technological University Kakinada (JNTUK), is a record of bona-fide work carried out by them under my guidance and supervision.

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We further declare that the work reported in this project have not been submitted either in part or in full, for the award of any other degree in any other institute or University.

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NOMENCLATURE

BPM	Beats per minute
SA Node	Sino atrial node
ECG	Electro cardio gram
Op – amp	Operational Amplifier
VOA	Voltage mode Operational Amplifier
AAB	Analog Active Block
CCII	Second Generation Current Conveyor
CCCII	Second Generation Current Controlled Current Conveyor
DVCC	Differential Voltage Current Conveyor
OTA	Operational Trans conductance Amplifier
DVCCTA	Differential Voltage Current Conveyor Trans conductance Amplifier
CMOS	Complementary Metal Oxide Semi-conductor
INA	Instrumentation Amplifier
VMIA	Voltage Mode Instrumentation Amplifier
CMIA	Current Mode Instrumentation Amplifier
CMRR	Common Mode Rejection Ratio
SIFO Filter	Single Input Five Output Filter
BPF	Band Pass Filter
LPF	Low Pass Filter
HPF	High Pass Filter

ABSTRACT

Cardiac Pacemakers play a vital role in the emerging medical field, as people are suffering from arrhythmia this pacemaker helps in monitoring cardiac activity. The Pulse Generator is the heart of the Pacemaker which comprises of sense amplifier, timing unit, and logic control unit. Sense amplifiers can be designed using an analog active block DVCCTA (Differential Voltage Current Conveyor Trans conductance Amplifier). The DVCCTA comprises the advantages of both the active blocks DVCC and OTA. The main aspects of a pacemaker are sensing and pacing. The sense amplifier consists of an instrumentation amplifier, band pass filter, and comparator that are used to detect the R wave from the cardiac signal. Based on the sense amplifier's output the timing and logic control unit decides whether pacing to be done or not. This can be stimulated with the help of Cadence Virtuoso 180nm technology.

Keywords: Sense Amplifier, DVCCTA, Instrumentation Amplifier, Pacemaker, Arrhythmia

CHAPTER 1
INTRODUCTION

1.1 Introduction

With the emerging technology, electronic devices demand low power consumption, high speed and better performance. Cardiac pacemaker is among those devices which plays a crucial role during arrhythmia (irregular heartbeat) for a longer lifetime. The main aspect of pacemaker is sensing and pacing. A pacemaker or heart's electrical system is used to increase or control the heartbeat. The normal heart rate of a human being is 72 beats per minute (bpm). If the heart rate is less than normal heart beat typically less than 60bpm it leads to tachycardia. During such fatal conditions pacemaker is implanted in the body to pace the heart by generating electrical impulses as per the patient's requirement. Pacemaker consists of a pulse generator and leads. Pulse generator has sense amplifier as the frontend design and digital part which is Logical and Timing control unit as the backend design.

Pacemakers are classified based on the rate of pacing. The major ones among these are fixed-rate pacing and demand pacing. In fixed-rate pacing the pacemaker generates the electrical signals at regular intervals regardless of whether the heart's natural pacemaker is functioning properly or not. But in demand pacing it monitors the activity of the heart and intervenes only when it's required.

The demand pacemaker requires a sense amplifier to monitor the condition of heart. The sense amplifier is implemented using Differential Voltage Current Conveyor Trans conductance Amplifier (DVCCTA). DVCCTA is an analog active block which has an advantage of electronic tuning over Differential Voltage Current Conveyor (DVCC) active block and conventional op-amp. Also DVCCTA has low power consumption and higher gain hence it is used as replacement of DVCC and conventional op-amp. Instrumentation Amplifier, Band Pass Filter and Comparator circuits in a sense amplifier has been designed using DVCCTA. Instrumentation amplifier is used to amplify the weak QRS complex of the cardiac signal. Band pass filter is used to filter unwanted P-wave and T-wave in the cardiac signal. Comparator compares the received QRS complex with the reference signal and generates digital output. Logic and Timing control unit will do pacing based on the sense amplifier's

output. It will implement the control algorithm based on the programmed mode of the pacemaker. It will decide the pacing rate based on various parameters and the timing constraints.

1.2 Objective

To create a robust sense amplifier using DVCCTA technology for precise R wave detection in a pacemaker's pulse generator. It employs Cadence Virtuoso to optimize design and simulation, aiming to improve arrhythmia monitoring and pacing accuracy.

1.3 Organization of Thesis

Thesis has been organized into six chapters in a sequence. Chapter 1 includes the introduction of the cardiac pacemaker and its importance. Also, its implementation using DVCCTA analog active block. Chapter 2 explains about the literature survey on pacemaker, pulse generator, cardiac cycle and some other active blocks which were included in the references. Chapter 3, Chapter 4 and Chapter 5 deals with the implementation of sense amplifier and its components using conventional op-amp, DVCC and DVCCTA active blocks respectively. Chapter 6 gives the conclusion and scope for future research in the field.

CHAPTER 2

LITERATURE SURVEY

2. LITERATURE SURVEY

2.1 Cardiac Cycle

Cardiac events that occur at the beginning of each heartbeat until the beginning of next are called the cardiac cycle. These events involve atrial and ventricle contraction, shots of autorhytmic fibers, opening and closing valves, at the cellular level involves depolarization for appropriate heart function. Human heart has four chambers two atria and two ventricles. The atria receive the blood flow from the external body parts. Ventricles pump out the blood to the other body parts. Deoxygenated blood returns to the heart via the superior vena cava and inferior vena cava into the right atrium and further flows to the right ventricle. The right ventricle pumps the deoxygenated blood to the lungs through the pulmonary artery. In the lungs, blood picks up oxygen and releases carbon dioxide. Oxygenated blood returns to the heart via the pulmonary veins into the left atrium. From the left atrium, blood flows into the left ventricle. The left ventricle, being the strongest chamber, pumps oxygen-rich blood to the rest of the body through the aorta. This cycle of blood flow repeats continuously, ensuring that all cells in the body receive the oxygen and nutrients they need to function. The anatomy of the heart is represented in figure 2.1.

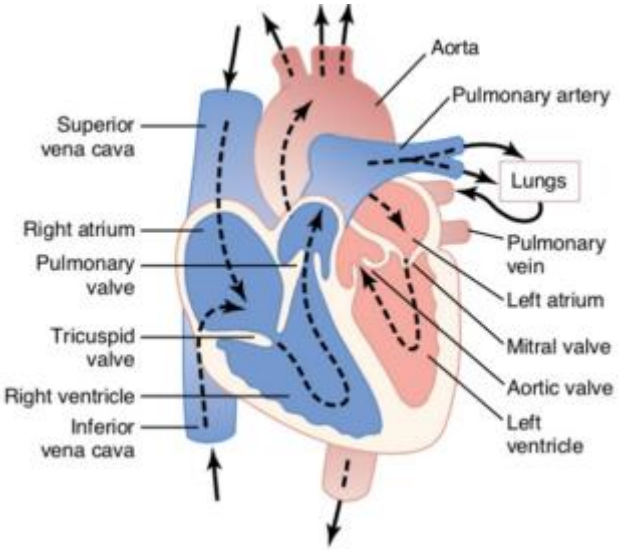

Fig. 2.1. Heart's anatomy

The Sino atrial node which acts like built-in pacemaker and generates electrical impulses that initiates hearts contraction. The heart is a pump that performs 72 beats per minute (bpm) equivalent to 1.2 Hertz, which each beat lasts around 0.830 ms (milliseconds) to boost the blood circulation that transports and distributes nutrients and oxygen, maintains the balance of fluids and body temperature. If heart beat is less than normal beat it leads to bradycardia (<60 bpm) and heavy heart rate leads to tachycardia (>100 bpm). The cardiac cycle is represented in figure 2.2.

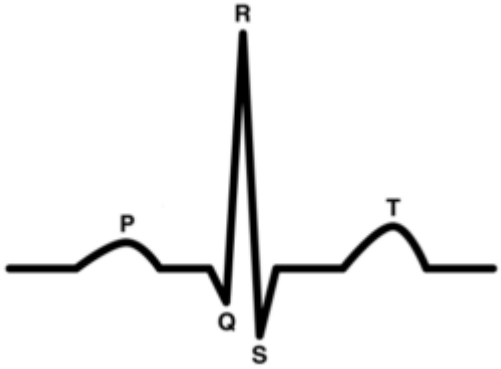

Fig. 2.2. Cardiac cycle

Diastole (relaxation) and Systole (contraction) are the two phases of cardiac cycle. When atria fill with blood SA node trigger to generate electrical pulses and simulates atria to contract. Atrial contraction is represented by P-wave when pressure in ventricles exceed atria, SLV opens allowing blood into pulmonary artery which results in the formation of QRS complex or R-wave. Then the blood flow from atria to ventricle which results in the formation of T-wave. The functioning of human heart and overview of the cardiac cycle have been presented in [1].

2.2 Evolution of Pacemakers

Nowadays pacemakers are the active implantable devices which are being used abundantly. Since the first artificial pacemaker was introduced in 1932, much has changed and will continue to change in future. The complexity and reliability in modern pacemakers has increased drastically mainly due to developments in integrated circuit and batteries. Pacemakers play a crucial role to help in the control for heart rhythms. To improve cardiac function and prevent cardiac rhythm disturbances with the use of artificial pacemakers, several pacing modes evolved during the 1960s.

Pacemakers and implantable cardioverter defibrillators (ICDs) have revolutionized cardiology by providing life-saving interventions for patients with cardiac rhythm disturbances. Pacing the heart is an effective treatment for people suffering from bradycardia caused by sinus node dysfunction or atrioventricular (AV) block, and electronic pacing has saved countless lives since its introduction into clinical practice. AV synchronization is the typical cycle of atrial depolarization and contraction followed by ventricular depolarization and contraction. The continuation of this cycle leads to appropriate ventricular filling and cardiac output. By contrast, the failure of the cycle results in AV asynchrony, which may result in heart failure. Cardiac resynchronization treatment (CRT) involves using customized pacemakers with or without implantable cardioverter defibrillators and tries to resynchronize the failing heart by enhancing myocardial contraction without increasing energy consumption. This review delves into the extensive journey of pacemakers and ICDs in the field of cardiology. It highlights the transformative impact of these devices on patient care and quality of life, emphasizing technological advancements, clinical applications, and prospects. This comprehensive review aims to provide insights into the dynamic landscape of cardiac rhythm management.

2.3 Classification of Pacemakers

Pacemakers are classified based on the rate of pacing. The major ones among these are fixed-rate pacing and demand pacing. The article on the history of the development of artificial pacemakers with the evolution of the various power sources needed for the designing of the pacemaker as well as the classification of the pacemakers have been presented in [2] and [3].

In fixed-rate pacing the pacemaker generates the electrical signals at regular intervals regardless of whether the heart's natural pacemaker is functioning properly or not. Hence it is known as asynchronous pacemaker and thus it leads to larger power consumption which is a disadvantage of this model. But in demand pacing it monitors the activity of the heart and intervenes only when it’s required. It maintains synchronization with the heart rhythm and consumes less power comparatively. The placement of implantable pacemaker inside patient’s heart is shown in figure 2.3.

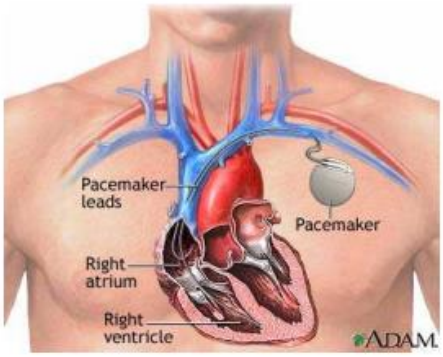

Fig. 2.3. Pacemaker inside patient's heart

2.3.1 Single chamber pacemaker

In single-chamber pacing, either the right atrium or the right ventricle is paced. It requires a single lead and is implanted either in atrium or ventricle, depending on the chamber to be paced and sensed. The pacemaker senses electrical activity in atrium or ventricle and determines whether pacing is needed or not. The placement of pacemaker in a single chamber is shown in figure 2.4.

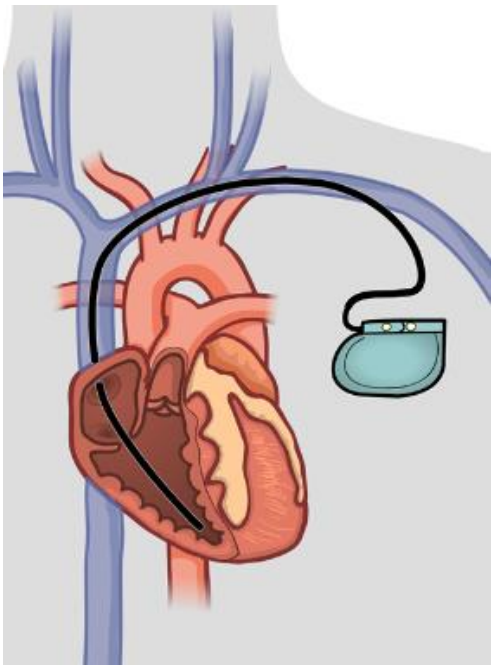

Fig. 2.4. Single chamber pacemaker

2.3.2 Dual chamber pacemaker

In dual chamber pacing, the pacemaker senses electrical activity in both the atrium and the ventricle and determines whether or not pacing is needed. Dual chamber pacemakers help the upper and lower chambers of heart to beat in their natural sequence and it requires two leads. The placement of pacemaker in dual chamber is shown in figure 2.5.

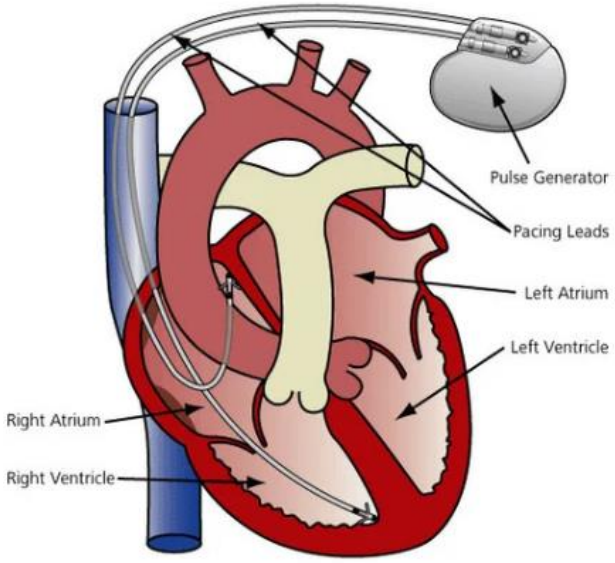

Fig. 2.5. Dual chamber pacemaker

2.3.3 Biventricular pacemaker

This type is also called a cardiac resynchronization pacemaker. These are often used to treat people with heart failure and slow heartbeat. It has three leads and used in the condition where left and right ventricles do not contract simultaneously.

2.4 Pulse Generator

Pulse Generator is the heart of the pacemaker comprises of sense amplifier, timing and logic control unit. Sense amplifier is the front end, logic and timing control unit is the backend of the pacemaker. Sense amplifier is responsible for sensing and comprises of instrumentation amplifier, band pass filter and a comparator. Based on sense amplifier's output digital unit i.e., timing and logic control unit determines whether pacing is required or not. A cardiac pulse generator is a device having a power source and electronic circuitry that produce output stimuli. Functionally, at its simplest, current sourced by the device's battery travels through a connecting pathway to

stimulate the heart and then flows back into the pacemaker to complete the circuit. Although numerous and varied designs of cardiac pacemakers are available, all have the same basic components:

- A power source in the form of a battery
- Circuitry (output, sensing, microprocessor and memory)
- A metal casing welded shut to keep out fluids
- A means of connecting a pacing lead to the header of the pacemaker
- Sensors like acceleration, vibration and impedance

Analysis of the pulse generator in the pacemaker represented in [4] which covers the analog part and digital part of the pacemaker.

2.4.1 Sense Amplifier

Sense amplifier in a pulse generator of a cardiac pacemaker helps in sensing the QRS complex of the ECG signal. Basically, sense amplifier comprises of an instrumentation amplifier, band pass filter and a comparator. Based on the output, Timing and Logic control unit decides whether pacing is required or not. Sense amplifier can be designed using conventional voltage mode operational amplifier and current mode analog active blocks. The instrumentation amplifier which is used to amplify the low voltage cardiac signals (ECG signals) i.e. QRS complex signal. Band pass filter is used to filter out the unwanted P wave or R wave received from instrumentation amplifier. Comparator is used to compare the QRS complex with some threshold value based on the patient's condition. The input ECG signal compared with threshold value, can decide the presence of QRS complex. The detail analysis of sense amplifier in a cardiac pacemaker has been presented in [5]. Implementation and analysis of sense amplifier using conventional op-amp and Differential Voltage Current Conveyor (DVCC) has been discussed in [6].

2.4.2 Logic and Timing Control Unit

Based on the operations performed by the pacemaker the modes of the pacemaker have been standardized by The North American Society of Pacing and Electrophysiology (NASPE) and British Pacing and Electrophysiology Group (BPEG). It is known as NBG coding. It is revised in 2002 and it has five positions which refer to the pacemaker function. They are presented in the following table.

The NASPE/BPEG Generic code (NBG Code)					
Position	I	II	III	IV	V
Category	Chamber(s) Paced	Chamber(s) Sensed	Response to sensing	Rate Modulation	Multisite Pacing
Letters used	O-None A-Atrium V-Ventricle D-Dual(A+V)	O-None A-Atrium V-Ventricle D-Dual(A+V)	O-None I- Inhibited T-Triggered D-Dual(T+I)	O-None P-Simple Programmable M-Multi Programmable R-Rate Modulation	O-None A-Atrium V-Ventricle D-Dual(A+V)

Table 1. Operations performed by the pacemaker (NBG coding)

Position I - Position-I shows which chambers are to be paced. Letter 'A' refers Atrium and 'V' refers to Ventricle. If there is need of pacing of both chambers then 'D' dual is used. Whereas 'O' stands for none or asynchronous pacing.

Position II– Position-II is similar to Position I. It shows which chambers are to be sensed.

Position III – Position-III shows what kind of response is generated for a sensed event inhibited or restricted response. If it is 'O' then there is no response to sensed event, if it is 'I' it indicates that pacemaker will inhibit pacing in response to sensed event, if it is 'T' then it refers to triggers an impulse in response to sensed event. Whereas 'D' is for the dual chamber system and to provide both triggered and inhibited function.

Position IV – Position IV show the presence or absence of rate responsive pacing. If it is 'R', it means pacemaker is integrated with some other sensors which sense the physiological conditions. If it is 'O', it stands for no any rate responsive program.

Position V - Position V indicates whether multisite pacing is present or not. If it is 'O', then it indicates that there is in none of the cardiac chambers. If it is 'A', it means multisite pacing is present in one or both atria and if it is 'V' multisite pacing is present in one or both ventricles. Where as if it is 'D', it indicates both atria and ventricle pacing. The modes of pacemaker were presented in [6].

2.5 Analog Active Blocks

Analog active blocks emerged as a specialized alternative to operational amplifiers (op-amps) due to their ability to provide tailored functionality and improved performance in certain applications. While op-amps offer versatility and simplicity in many circuit designs, they may not always meet the specific requirements of more complex systems or niche applications. Analog active blocks address this limitation by offering customized solutions with enhanced features and performance characteristics. For instance, op-amps have inherent limitations in terms of bandwidth, slew rate, and input/output impedance, which may constrain their suitability for high-frequency applications or those requiring precise signal conditioning. Analog active blocks, on the other hand, can be designed to optimize these parameters, providing superior performance in specialized domains such as high-speed data communication, radio frequency (RF) circuits, or sensor interfacing. Moreover, active blocks can incorporate additional functionalities such as frequency synthesis, signal modulation, or power amplification, extending their utility beyond basic signal processing tasks. By leveraging advanced semiconductor technologies and innovative circuit topologies, analog active blocks offer engineers greater flexibility and control in designing circuits tailored to specific application requirements, ultimately driving advancements in electronics across various industries.

Searching for novel active circuit elements for analog signal processing which would operate on completely different circuit principles than present-day operational amplifiers (op-amps) is going hand to hand with research into new circuit structures employing these elements for linear and nonlinear signal processing. It looks like an apparent paradox in the era of advanced technologies of IC manufacturing that the “old” but proven op-amp circuit principles persist on the production programmed of world-leading factories, whereas the series production of electronic components, working on modern principles, cannot be put through. On the other hand, for example, one cannot fully utilize the claimed advantages of the current mode in comparison to the voltage mode when implementing the application circuits from discrete components. This lecture illustrates the above problem on an example of emulating memristors, memcapacitors, and meminductors, promising circuit elements which represent an extension of the set of conventional R, C, and L elements, via a combination of analog passive and active elements. It is shown that special mutators can serve as effective

tools for such emulation, and that the second-generation current conveyors (CCIIs) can play an important role in their synthesis. On the other hand, such emulators should be small enough and supplied by individual mini-batteries. It leads to a requirement of low-voltage low-power building blocks. This lecture describes prototyping of these emulators via today's off-the-shelf integrated circuits. In the second step, a comparison with other implementations is made on the assumption that some till this time hypothetical active elements are available in the market. The analysis of analog active block has been presented in [7].

2.6 Operational Amplifier

The Operational Amplifier (op – amp) is primarily one of the voltages amplifying device which is designed using the external component feedback devices such as resistors and capacitors between its outputs and input terminals. These feedback components determine the output of the op – amp by the virtue of the different feedback configurations whether resistive or capacitive. The op – amp can perform various operations and more over the growth of the rapid growth in portable applications demand to low voltage and low power consumption. Here there is a presentation of the CMOS op-amp which is operating at 2V power supply and 1 uA input current at 0.8 um technology using the non – conventional mode of MOS transistors and the input current is dependent on bias current. There is a unique behavior of the MOS transistors in the sub threshold region, which enables the circuit designers to work at low input bias current. This condition allows the circuit to operate at low voltage. When the device is operated at weak inversion. It results in low power dissipation. But this results in degradation of dynamic range. Optimum balance in dynamic range and power dissipation results when the op – amp operates at moderate inversion. As a result in the comparison with the reported low power, low voltage op – amp at 0.8 um technology. This circuit has very low stand by power consumption and high driving capacity and operated at low voltage. As the above-mentioned properties are more advantageous. These operational amplifiers are used extensively in signal processing and filtering or to perform mathematical operations like addition, subtraction, integration and differentiation. It is discussed in [8].

2.6.1 Instrumentation Amplifiers in Op-Amps

Instrumentation amplifiers are tailored for precision signal amplification in measurement and sensor applications. They feature adjustable gain, enabling accurate

amplification of small differential signals. With a high CMRR, they effectively reject common-mode signals, crucial for maintaining accuracy in noisy environments. These amplifiers prioritize precision, boasting low offset voltage, drift, and noise. They also offer high input impedance, minimizing loading effects on the measured circuit, and often provide single-ended output for simplified interfacing. Temperature stability is another hallmark, ensuring accuracy across varying operating conditions.

2.6.2 Filter in Op-Amp

Filters are essential components in electronics, serving to selectively pass or reject certain frequency components within a signal. Operational amplifiers (op-amps) are versatile devices commonly used in filter circuits due to their high gain, low output impedance, and ease of implementation. By combining op-amps with passive components like resistors, capacitors, and inductors, various types of filters can be realized. Whether it's a low-pass filter allowing frequencies below a cutoff point, a high-pass filter passing frequencies above a cutoff point, a band-pass filter isolating a specific range of frequencies, or a band-stop filter attenuating a particular frequency range, op-amp-based filter circuits offer flexibility and precision in signal conditioning and processing applications. Each filter type has distinct characteristics and design considerations, enabling engineers to tailor the filter response to meet specific requirements for noise reduction, signal extraction, or interference rejection.

2.7 Differential Voltage Current Conveyor (DVCC)

The differential voltage current conveyor (DVCC) is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith [9]. Recently, the CCII has been realized using MOS transistors, with the intention to integrate the different CCII circuit applications on one chip [10]. The CCII proves to be a versatile building block that can be used to implement a variety of high-performance circuits which are simple to construct. The CCII has a disadvantage that only one of the input terminals has a high input impedance (the Y terminal). This disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of an instrumentation amplifier. The design of such an amplifier requires two or more CCIIs. A basic section used in realizing floating input applications from CCIIs is given. Using

such a circuit to realize an instrumentation amplifier results in an amplifier structure that has the advantage of a high CMRR (even at high frequencies) without the need for an accurately matched resistor network. The circuit given uses two CCIIs and a floating resistor to provide floating input handling capability. Moreover the floating resistor is connected between the X terminals of the two CCIIs. As each X terminal has an output resistance R, the effective resistance between the two X terminals is R + 2R, which is the error caused by the nonzero X terminal resistance is doubled.

The differential voltage current conveyor (DVCC) building block is proposed. The DVCC is a novel building block specially defined to handle differential signals. It is a versatile building block for applications demanding floating inputs. DVCC is used to realize an instrumentation amplifier, MOS Trans conductor and a current mode MOSFET C filter. The details are presented in [11].

2.7.1 Instrumentation amplifier using DVCC

Instrumentation amplifier (INA) is the basic one and widely used to amplify the useful differential signals and to suppress any unwanted common mode signals. On the other hand, several applications like medical instrumentation, read out integrated circuits for biosensors, data acquisition systems, electrocardiography, etc. have been reported that pronounce the importance of INA. Initially, numerous voltage INA structures have been depicted using well-known operational amplifier (op-amp) but suffers from the following draw-back such as narrow bandwidth, uses excess number of passive components, limited gain bandwidth product, high power consumption, low slew rate, and dynamic range. Although resistors present in INA should be matched to attain high common mode rejection ratio (CMRR), voltage gain-dependent CMRR and many more in comparison to the current mode active blocks. As an attractive strategy to overcome the limitations associated with the conventional op-amp based INA, an alternate scheme based on current mode instrumentation amplifiers (CMIA) came into existence using current mode active blocks such as current conveyors (CC), second-generation current conveyor (CCII), and second-generation current controlled current conveyor (CCCII).

The instrumentation amplifier which is used to amplify the low voltage cardiac signals has been implemented using Differential Voltage Current Conveyor (DVCC). The

differential mode gain has been calculated and this implementation was discussed in [12].

2.7.2 Bi quadratic Filter using DVCC

The differential voltage current conveyor (DVCC) was proposed in 1997 and it enjoy the advantages of CCIIs such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power-consumption and high input impedance. Moreover, it has two high input voltage terminals. A high-input impedance voltage-mode universal bi quadratic filter with one-input and five-outputs is presented. The proposed circuit uses three plus-type differential voltage current conveyors (DVCCs), two grounded capacitors and three resistors and offers the following features: the realization of all the standard filter functions, that is, high-pass, band-pass, low-pass, notch, and all-pass filters, orthogonal control of ωo and Q, the use of only grounded capacitors, high-input impedance and low active and passive sensitivities.Bi quadratic Filter has been implemented using DVCC. Filter has been implemented using single DVCC. This design is presented in [13].

2.8 Differential Voltage Current Conveyor Trans conductance Amplifier

Current-mode active building blocks have been receiving considerable attention owing to their larger dynamic range, greater linearity, wider bandwidth and low power consumption with respect to operational amplifier-based circuits. Moreover, analogue signal processing in low supply voltages can be best accomplished in the current-mode and hence low voltage current mode active building blocks operating in the current-mode and their applications are important in sinusoidal oscillators. In 2009, a new active building block for analogue signal processing, namely, differential voltage current conveyor trans conductance amplifier (DVCCTA), was introduced. DVCCTA device is obtained by cascading of the differential voltage current conveyor (DVCC) with the operational trans conductance amplifier (OTA) in monolithic chip for compact implementation of analogue function circuits. As a result, DVCCTA has a trans conductance stage at its back end and hence it provides the feature of electronic tuning to the circuit parameters, while also reducing the number of resistors by one. Recently, a voltage-mode DVCCTA based quadrature sinusoidal oscillator is constructed. This circuit employs a single DVCCTA, two grounded capacitors and two grounded resistor and offers the advantages of (i) independent control of condition of oscillation (CO)

and frequency of oscillation (FO), (ii) voltage mode quadrature signals with 90° phase difference, and (iii) low active and passive sensitivities. In this paper, the authors also propose another electronically controllable DVCCTA based quadrature sinusoidal oscillator. The proposed circuit has all of the advantages by Lahiri et al. in addition to one more advantage of two explicit high-output impedance sin currents with a 90° phase difference. Both current-mode and voltage-mode quadrature signals can be simultaneously obtained in the proposed circuit. Sinusoidal oscillators which produce both current-mode and voltage-mode quadrature signals are useful for their versatility. Since the proposed circuit consists of single DVCCTA and all grounded passive components thus it is more suitable for integrated circuit implementation.

2.8.1 Instrumentation amplifier using DVCCTA

The instrumentation amplifier which is used to amplify the low voltage cardiac signals has been implemented using Differential Voltage Current Conveyor Trans conductance Amplifier (DVCCTA). The differential mode gain has been calculated and this implementation was discussed in [14].

2.8.2 SIFO Filter using DVCCTA

Single Input Five Output Filter (SIFO) Filter has been implemented using DVCCTA. The high pass filter, low pass filter, band pass filter, all pass filter and band reject filter has been implemented using single DVCCTA. This design is presented in [15].

2.8.3 Comparator using DVCCTA

Comparator has been implemented using DVCCTA. It incorporates single DVCCTA block and a single resistor. It compares the analog signal at input and produces the digital output. CMOS internal implementation of comparator is same as that of INA.

CHAPTER 3

SENSE AMPLIFIER USING OP-AMP

3. Implementation of Sense Amplifier using Conventional Op-Amp

Sense amplifier has been implemented using conventional voltage mode op-amp. In conventional op-amp based design sense amplifier, instrumentation amplifier consists of an active device op-amp and a resistive network of seven resistors. Active band pass filter comprises of an active high pass filter followed by active low pass filter. BPF is a second order active filter comprises of op-amp and a second order reactive network. Comparator is the third stage of a sense amplifier used to detect the QRS complex by generating a digital pulse signal.

3.1 Block diagram of a Sense Amplifier

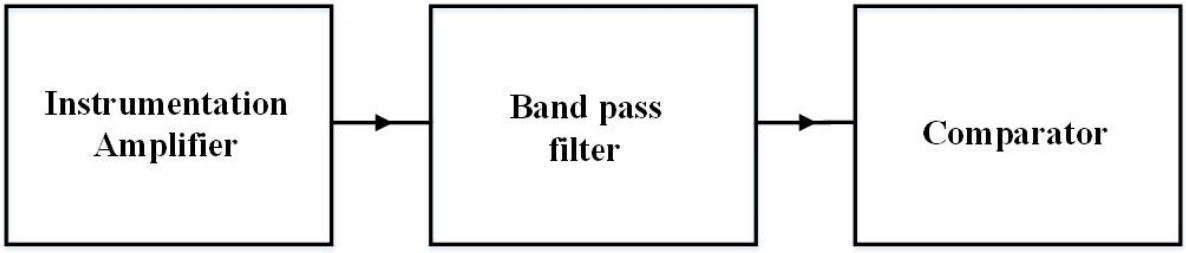

Fig. 3.1. Block diagram of a sense amplifier

The primary function of the pacemaker circuit is to amplify the signals coming from the heart through the sensing leads (electrodes). Now need to analyse the ECG signal so as to filter out the R-wave or the QRS complex of the cardiac signal. So, a sense amplifier is used to detect the cardiac activity of the heart. It is used to detect the R-wave or the QRS complex. The sense amplifier mainly comprises of three components namely instrumentation amplifier, band pass filter and comparator. To tap the ECG signal an instrumentation amplifier can be used. The ECG signal is of very low amplitude (20-30 mv) and having a frequency range of 1-100Hz which is of very low frequency. Hence, require a robust filter with less roll-off- factor to achieve accurate results. Thereby can filter the QRS complex from the cardiac signal.

Now in order to detect the R-wave or the QRS complex, can have a comparator with some threshold value. This threshold value may vary depending upon the condition of

the patient. By comparing the input signal with the threshold value, can decide the presence of the QRS complex. This forms the input to the next stage whether to pace the heart or not. Timing and logic control unit is the next stage which generates electrical impulses based on the sense amplifier's output. The block diagram of sense amplifier can be seen in figure 3.1.

3.2 Circuit Analysis

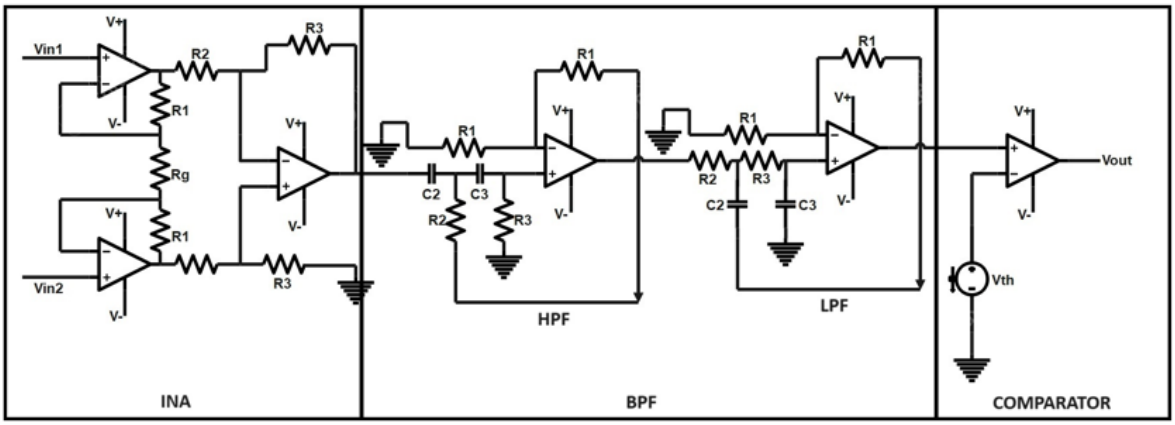

Fig. 3.2. Circuit of Op-amp based sense amplifier

3.2.1 Instrumentation Amplifier:

Instrumentation amplifier is a kind of differential amplifier which amplifies the difference of two input signals. These amplifiers are used where long-term accuracy and stability are desired. The circuit converts a differential signal to a single-ended output signal. It has three stages; first stage is the input stage which takes the difference of two input signals. Second stage is the gain stage which amplifies the differential signal and gain is determined by the resistive network. Third stage is the output stage which provides a buffered and amplified output voltage to ensure low output impedance. It has very high gain, high CMRR and high input impedance. It plays a vital role in amplifying the cardiac signals which are of very low magnitude.

Instrumentation amplifier is the first stage of a sense amplifier. It is designed with an active network of three op-amp and a passive network of seven resistors. The value of resistors in a network is given by $R_1 = R_2 = R_3 = 10K\Omega$, $R_g = 2.2\ K\Omega$ and it can be adjustable. The implementation of an instrumentation amplifier is shown in figure 3.2.

Voltage gain of an instrumentation amplifier is calculated by using the formula as follows

$$Av = (1 + \frac{2\ R2}{Rgain})(\frac{R4}{R3})$$

3.2.2 Band Pass Filter (BPF)

Active band pass filter is the second stage of a sense amplifier. It comprises of high pass filter (HPF) followed by a low pass filter (LPF). BPF is used to allow a certain band of frequencies of range around 100Hz and to reject unwanted signals. The amplified ECG signal from the instrumentation amplifier is applied as an input to the band pass filter. It filters the incoming ECG signal to eliminate noise and other unwanted components that may contained therein, for example, the low-frequency P-wave and T-wave. The implementation of band pass filter is shown in figure 3.2.

Second order active high pass filter consists of one active component op-amp which acts as an amplification and gain control factor and a passive network of four resistors and two capacitors. The values of a passive network is given by R_1 = 3.5k, R_2 = R_3 = 10k, C_1 = C_2 = 31.8uF with a cut-off frequency of around 0.5Hz. The cut-off frequency of band pass filter is determined by

$$f_c = \frac{1}{2\pi RC}.$$

Second order active low pass filter consists of one active component op-amp which acts as an amplification and gain control factor and a passive network of four resistors and two capacitors. The values of a passive network are given by R_1 = 3.5k, R_2 = R_3 = 10k, C_2 = C_3 = 0.159uF with a cut-off frequency of around 100Hz. The cut-off frequency of band pass filter is determined by

$$f_c = \frac{1}{2\pi RC}.$$

3.2.3 Comparator

The comparator is implemented using conventional op-amp. The threshold can be programmable. It is varied based on various parameters like the age of the person, his health condition etc. which are too monitored prior and then the threshold is fixed. The threshold can be fixed based on the previous values when special cases like random pulses occur. It should be able to differentiate the QRS from the P - wave and the T-wave. The threshold voltage is given here is around 80 mV. The implementation of comparator is shown in figure 3.2.

The final output of the sense amplifier will be a digital signal. The pulse indicates the presence of QRS complex. This will be the driving input for the timing circuit. If the pulse is detected then no need of artificial pacing or else the pulse generator sends the artificial pulses to the heart. Thus, the Sense Amplifier forms an important part of the Demand pacemaker where it could reduce the power consumption as the other circuitry need not be active all the time. It gets activated only when's required.

3.3 Simulations

The simulations have been performed in Cadence OrCAD Pspice. The input as well as the outputs of the Sense Amplifier have been simulated and plotted in this section. The figure 3.3 shows the input test cardiac signal used for the simulation. The figure 3.4 shows the output transient response of the first stage instrumentation amplifier. The figure 3.5 and figure 3.6 shows the transient and AC response of the Band pass filter. The figure 3.3 shows the response of the Comparator which is the final output of the Sense Amplifier.

3.3.1 Input test cardiac signal

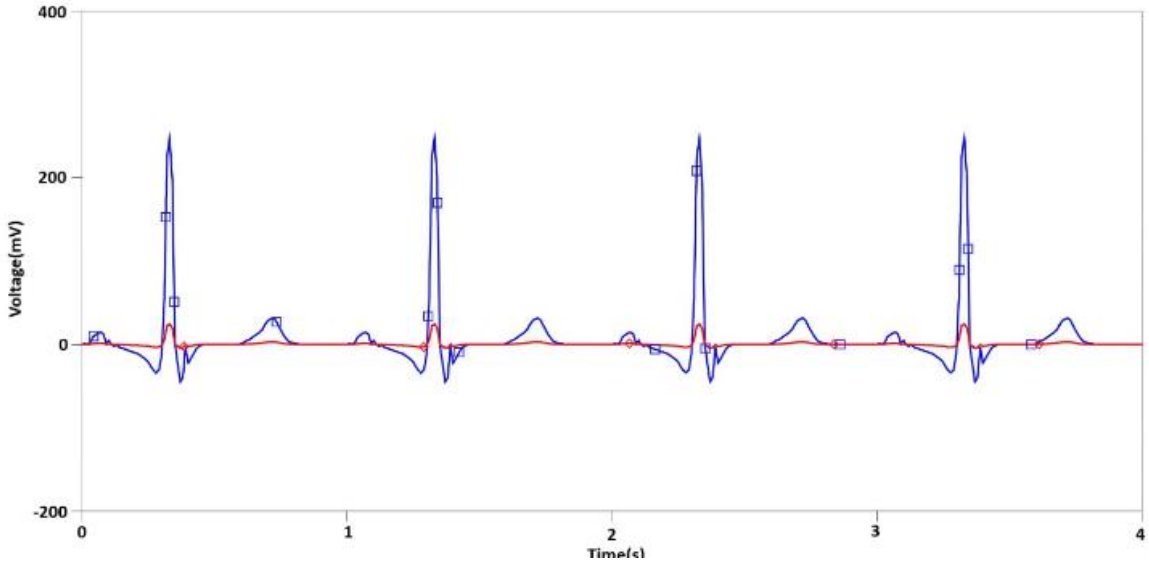

Fig. 3.3. Test Input ECG signal

The input cardiac signal is of very less magnitude. It has two full cycles each of 0.8 sec approximately. All the P-wave, QRS complex and the T-wave can be seen in the figure 3.3. The peak value of QRS complex is 24 mv.

3.3.2 Output waveform of the Instrumentation Amplifier

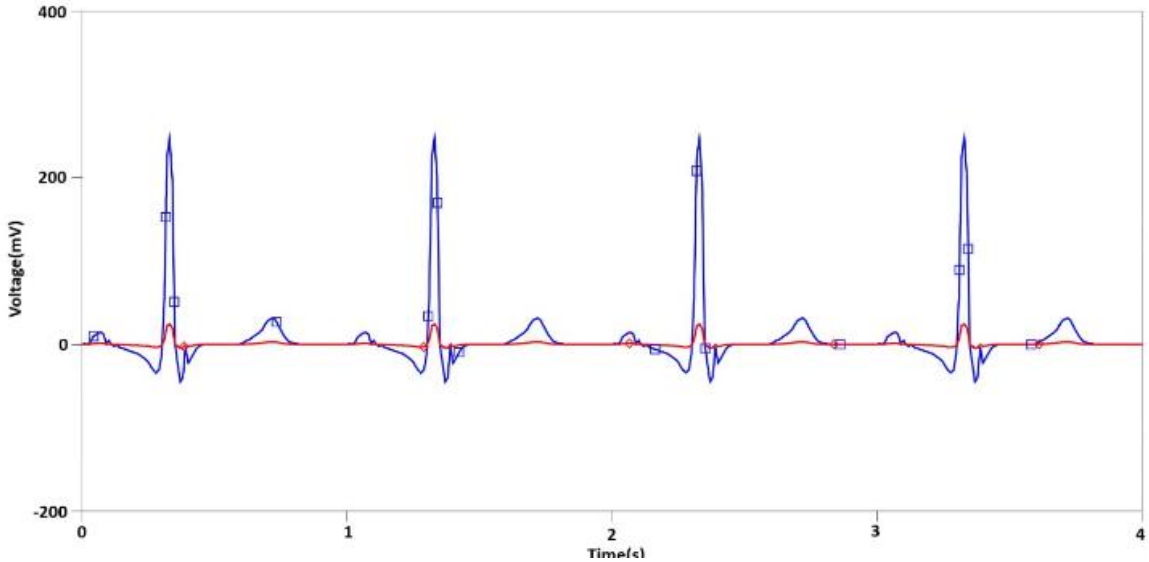

Fig. 3.4. Output of INA

The differential gain is around 20.07 db. The delay between input and output waveforms is found around 30 ns for a test pulse signal. The peak value of the QRS complex is around 240 mv.

Output and gain of an instrumentation amplifier can be controlled by R_g. Relation between the outputs voltages obtained for different adjustable gain resistor is shown in table 2.

Input voltage (Vin)	Resistor Gain (Rgain)	Output voltage (Vo)	Voltage gain (Av)
24mV	1Kohm	510mV	26.44db
24mV	2.2Kohm	240mV	20.07db
24mV	4.7Kohm	120mV	14.4db

Table 2. Differential gain obtained for different Rg

3.3.3 Transient response of the Band pass filter

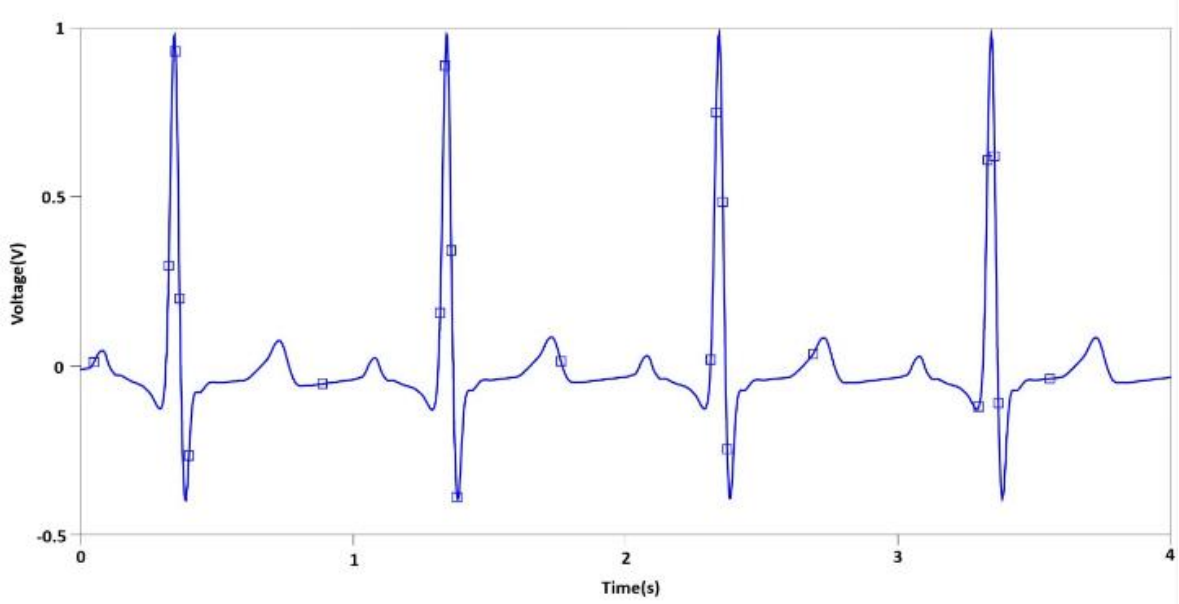

Fig. 3.5. Transient response of BPF

The Band pass filter is designed such that it filters out only the QRS complex which is evident from figure 3.5. The AC response of high pass filter and low pass filter is shown in figure 3.6 and figure 3.7 respectively.

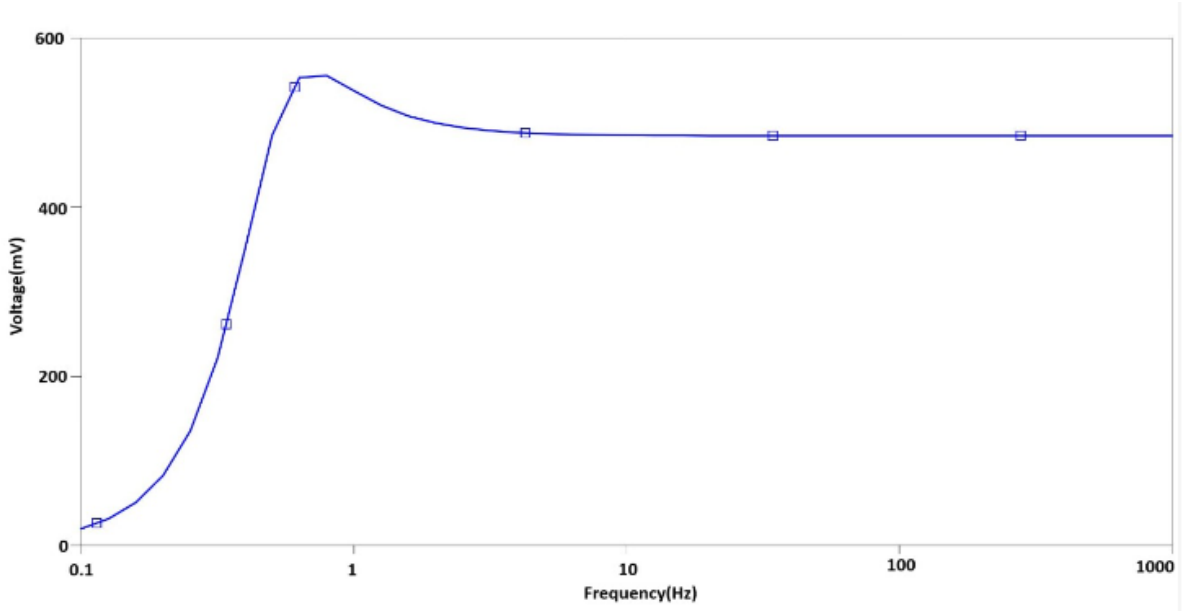

Fig. 3.6. AC response of HPF

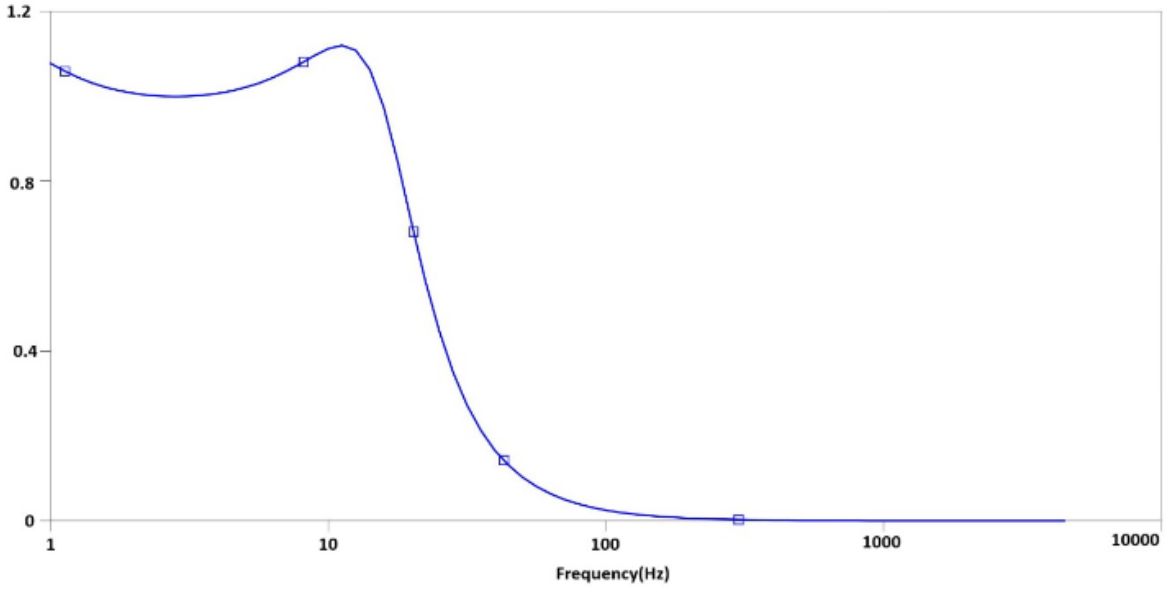

Fig. 3.7. AC response of LPF

3.3.4 Final Output of Sense Amplifier

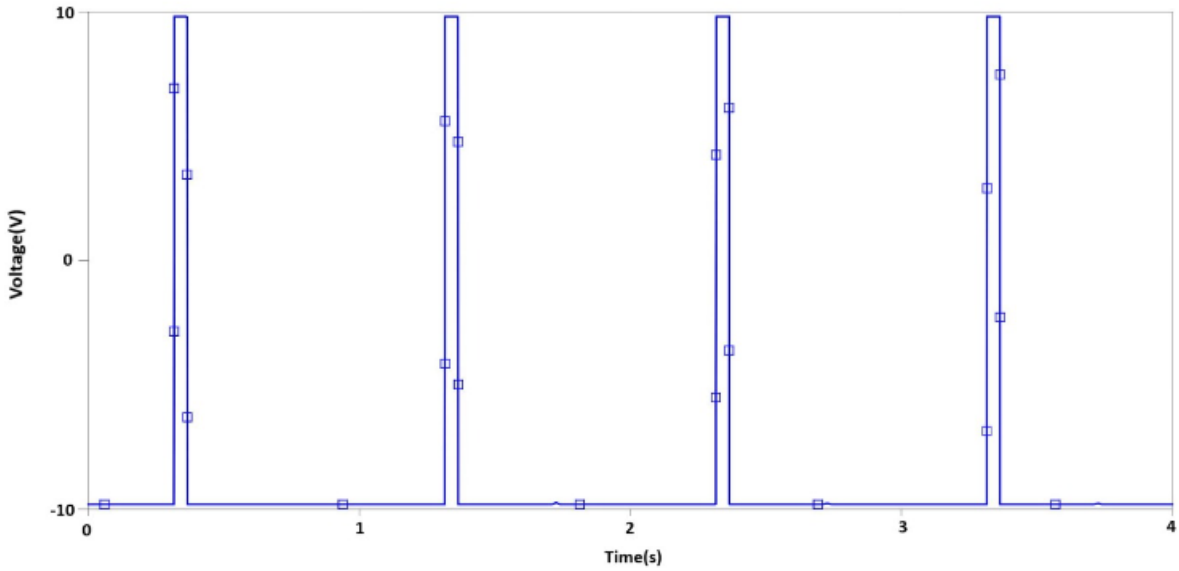

Fig. 3.8. Comparator Output

The output of the comparator can be seen in figure 3.8. The threshold provided to the comparator varies depend on the person. A digital waveform having a dynamic range from +10V to -10V has been obtained which are the saturation voltages of the comparator respectively. The pulse indicates the presence of QRS complex.

3.4 Conclusion

The voltage mode operational amplifier based sense amplifier design has the input as test cardiac ECG signal and the output obtained at comparator of sense amplifier is digital pulses. This sense amplifier design comprises of an instrumentation amplifier of 3 active element of op-amp and network of seven resistors. Filter comprises of 2 active op-amp and a reactive network of 8 resistors and 4 capacitors. Comparator comprises of a single active element and a reference voltage. The power consumption of voltage mode sense amplifier for op-amp based design is around 20.8mW. So to decrease the power consumption and circuit complexity and to increase the efficiency current mode analog active blocks were used which uses the technique of current mirror.

CHAPTER 4

SENSE AMPLIFIER USING DVCC

4. Implementation of Sense Amplifier using DVCC

Sense amplifier has been implemented using Differential Voltage Current Conveyor (DVCC). In DVCC based design sense amplifier, instrumentation amplifier consists of an analog active block DVCC and employs two MOSFETs which act as a resistive network. Active band pass filter comprises of single active block DVCC and a reactive network of two resistors and two capacitors. Comparator employs a single active block DVCC and a single MOSFET which detects the QRS complex by generating a digital pulse signal as output.

4.1 Differential Voltage Current Conveyor (DVCC):

Differential Voltage Current Conveyor (DVCC) is an analog active building block. These circuits are powerful building blocks, especially for applications demanding differential instrumentation amplifiers. They are useful building blocks for analog circuits, especially for applications demanding differential input. They can be directly used with MOS transistors operating in ohmic region to implement require analog functions. The DVCC was first proposed by Elwan. An ideal DVCC port characteristic will be as follows,

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}$$

From the port relations it implies that the voltage at the X-terminal follows the difference of voltages at Y_1 and Y_2 terminals. The current at Z-terminal replicates at X-terminal and also the current at Y_1 as well as at Y_2 terminals is zero since the impedance at these two terminals is very high.

$$I_{Y1} = I_{Y2} = 0$$

$$V_X = V_{Y1} - V_{Y2}$$

$$I_Z = I_X.$$

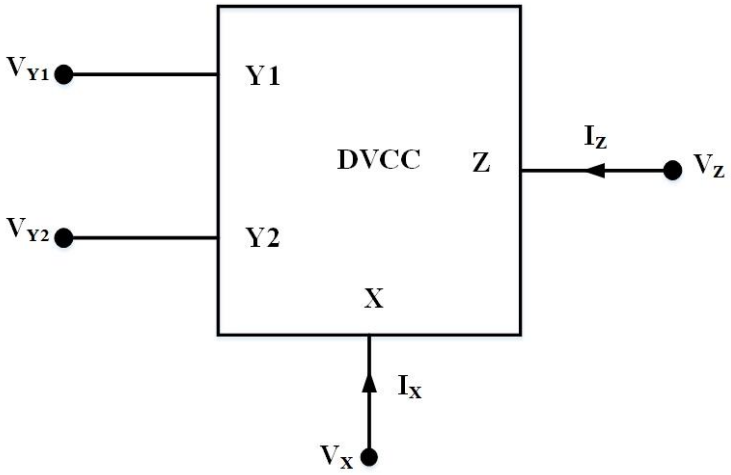

Fig. 4.1. DVCC Block

The circuit symbol of the DVCC block is shown in the figure 4.1. The internal structure of the DVCC i.e. the CMOS realization of the DVCC is shown in figure 4.2. It totally has 9 NMOS and 5 PMOS. The supply voltages $V_{dd} = -V_{ss} = 1.25V$. The biasing voltages are $V_{b1} = -450mV$ and $V_{b2} = 300mV$. The aspect ratios of the MOSFET's can be seen in Table-3.

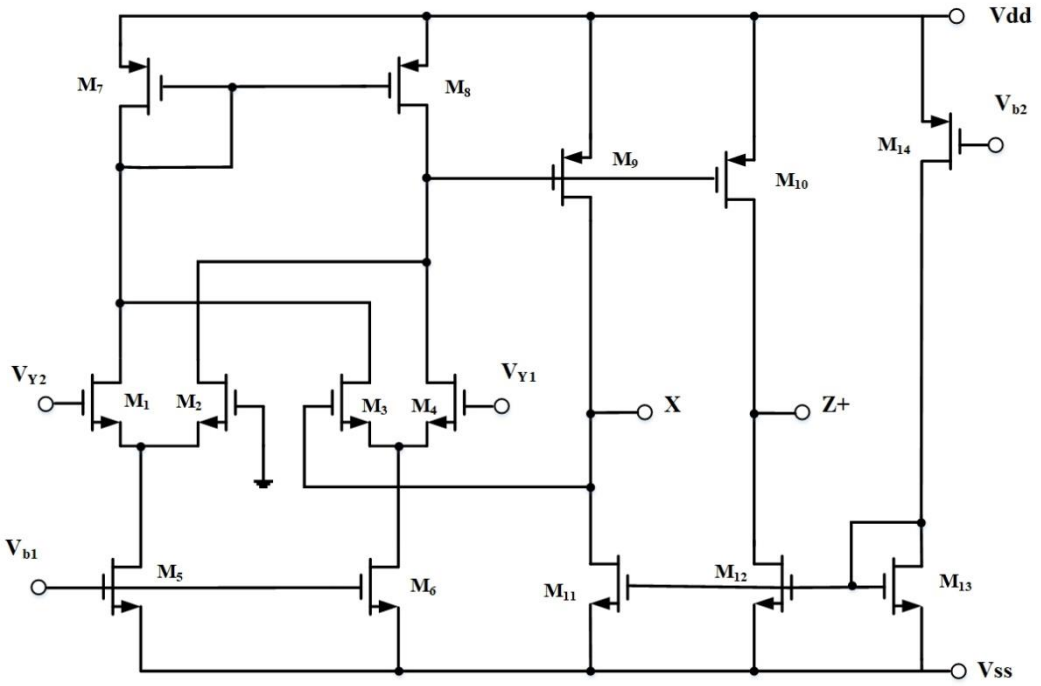

Fig. 4.2. Implementation of CMOS based DVCC

The practical equivalent circuit of DVCC deviates from the ideal characteristics of DVCC and possess current transfer gain (α), voltage transfer gain (βi) with the following port characteristics

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}$$

Aspect Ratios for the MOSFETs:

MOSFET	**W/L(um)**
M_1-M_6	4.5/0.9
M_{11}-M_{13}	4.5/0.9
M_7-M_{10}, M_{14}	9/0.9

Table 3. Aspect ratios for the CMOS transistors in DVCC

4.2 Circuit Analysis

4.2.1 Instrumentation Amplifier

The instrumentation amplifier is constructed from the DVCC by employing two more external MOSFETs to provide the required differential gain. It is shown in figure 4.3.

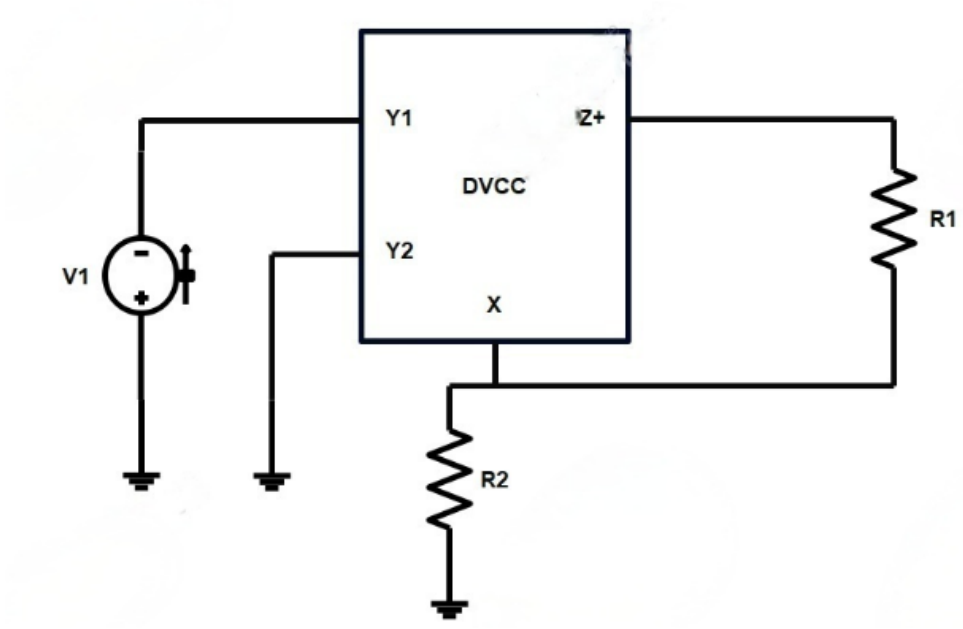

Fig. 4.3. Instrumentation Amplifier using DVCC

All the parameters are same as that shown in the Table 3. R1 and R2 values are 10KΩ and 0.25Ω respectively. The differential gain of the instrumentation amplifier is given by

$$A_d = 1 + \left(\frac{\alpha}{\alpha + 1}\right)\left(\frac{R_2}{R_1}\right)$$

If non- ideal characteristics are taken, then the output response for the VMIA can be rewritten by keeping β1 = β2 = 0 as

$$Vout = (1 + \left(\frac{\alpha}{\alpha+1}\right)\left(\frac{R_2}{R_1}\right))(Vin1 - Vin2) \quad \rightarrow(1)$$

The differential mode gain (Ad) for VMIA is given as

$$A_d = \frac{\text{Vout}}{\text{Vin1}-\text{Vin2}} = 1 + \left(\frac{\alpha}{\alpha+1}\right)\left(\frac{R_2}{R_1}\right) \rightarrow(2)$$

4.2.2. Single Input Multi Output Filter

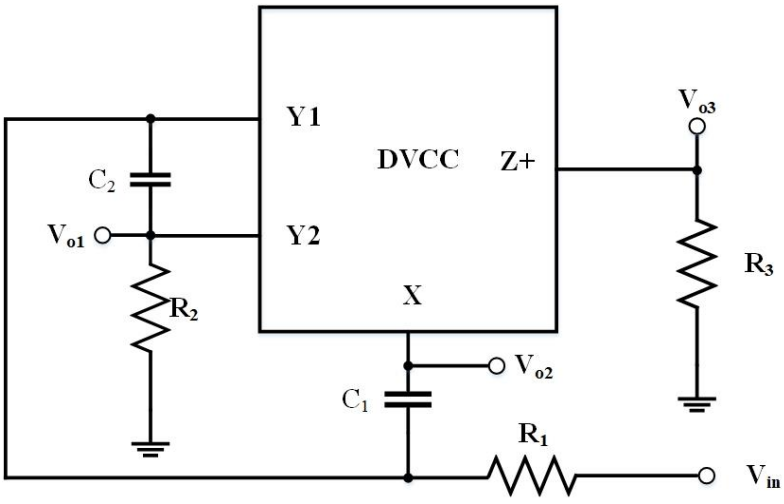

Fig. 4.4. Voltage-mode multifunction biquadratic filter

This is implemented using plus type DVCC which is same as the DVCC except for the M_{13} and M_{14} shown in Figure 3.12. The corresponding R, C values are R_1 = 100KΩ, C_1 = 159nF, R_2 = 275KΩ, C_2 = 25nF for a centre frequency of 25Hz. The bandwidth of the filter is around 30Hz.The V_{dd} = - V_{ss} = 0.9V and V_b = -500mV.

By the corresponding nodal equations, we can derive the transfer functions at the three ports V_{o1}, V_{o2}, V_{o3}. We can achieve a non-inverting band pass filter, a non-inverting low pass filter and an inverting high pass filter at V_{o1}, V_{o2}, and Vo3 respectively.

The transfer functions are given by the following equations:

$$\frac{V_{01}}{V_{in}} = \frac{sC_2G_1}{s^2C_1C_2 + sC_2(G_1 + G_2) + G_1G_2}$$

$$\frac{V_{02}}{V_{in}} = \frac{G_1G_2}{s^2C_1C_2 + sC_2(G_1 + G_2) + G_1G_2}$$

$$\frac{V_{03}}{V_{in}} = -\frac{G_1}{G_3}\frac{s^2C_1C_2}{s^2C_1C_2+sC_2(G_1+G_2)+G_1G_2}$$

The resonant frequency of the filter is given by,

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}$$

Aspect ratio of plus type DVCC:

MOSFET	**W/L(um)**
M_1-M_4	8.75/0.35
M_5-M_6, M_{11}-M_{12}	8.75/0.18
M_7-M_{10}	17.5/0.18

Table 4. Aspect ratios of CMOS transistors in plus type DVCC

4.2.3 Comparator

Using DVCC, a comparator is implemented to detect the QRS complex in the ECG signal by shorting the X- terminal to the ground. Then the current at X-terminal enters to saturation which is mathematically,

$$I_X = I_m \tanh \beta(V_{Y1} - V_{Y2})$$

where β is the open-loop gain of the comparator and $\pm I_m$ is the saturated output current level(s) of the DVCC and are decided by the bias current of the DVCC, which in turn is governed by the bias voltage V_{BB}, where g is the trans conductance gain from the

input voltage ports Y_1 and Y_2 to the output current port X and $\pm V_m$ are the biasing voltages of the DVCC-based comparator. This current from X-terminal will be replicated at Z-terminal.

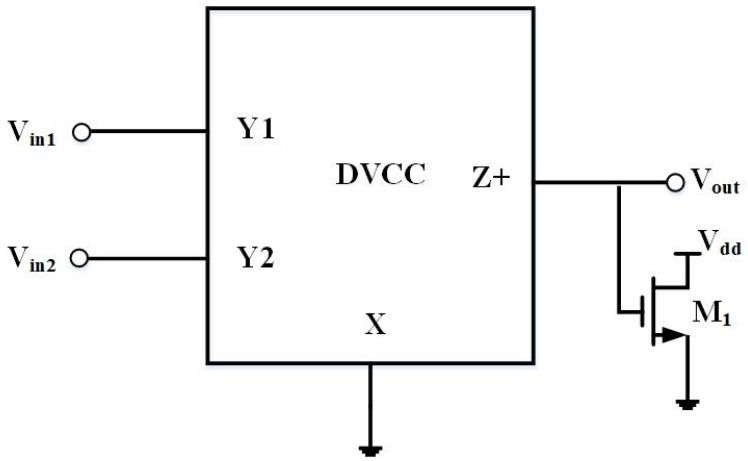

Fig. 4.5. Implementation of Comparator using DVCC

The comparator is implemented using the DVCC plus. The aspect ratios are similar to that of filter. Bias voltages are $V_{dd} = -V_{ss} = 0.9$ V. The threshold can be programmable. It is varied based on various parameters like the age of the person, his health condition etc. which are too monitored prior and then the threshold is fixed. The threshold can be fixed based on the previous values when special cases like random pulses occur. It should be able to differentiate the QRS from the P - wave and the T-wave.

The final output of the sense amplifier will be a digital signal. The pulse indicates the presence of QRS complex. This will be the driving input for the timing circuit. If the pulse is detected then no need of artificial pacing or else the pulse generator sends the artificial pulses to the heart. Thus, the Sense Amplifier forms an important part of the Demand pacemaker where we could reduce the power consumption as the other circuitry need not be active all the time. It gets activated only when required.

4.3 Simulations

All the simulations have been performed in Cadence using TSMC 180nm technology. The input as well as the outputs of the Sense Amplifier have been simulated and plotted in this section. The figure 4.6 shows the input test cardiac signal used for the simulation. The figure 4.7 shows the output transient response of the first stage Instrumentation Amplifier. The figure 4.8 shows the Magnitude response of the Band pass filter. The

figure 4.9 shows the output transient response of the Band pass filter. The figure 4.10 shows the response of the Comparator which is the final output of the Sense Amplifier.

4.3.1. Input test cardiac signal

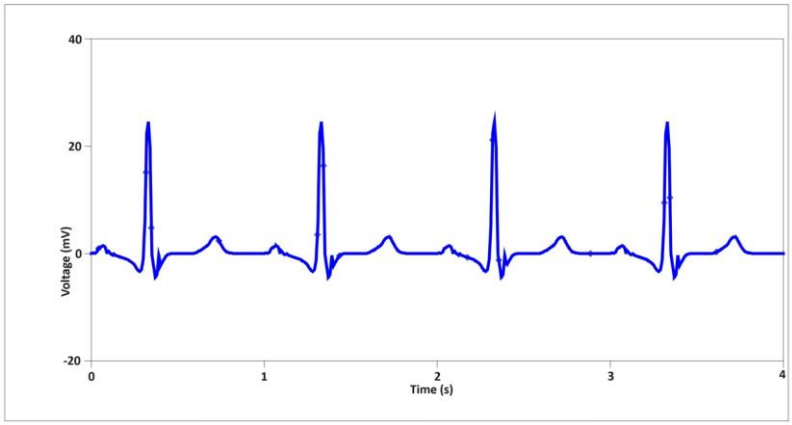

Fig. 4.6. Input test cardiac signal

The input cardiac signal is of very less magnitude. It has two full cycles each of 0.8 sec approximately. All the P-wave, QRS complex and the T-wave can be seen in the figure 4.6. The peak value of QRS complex is 24 mv.

4.3.2. Output waveform of the Instrumentation Amplifier

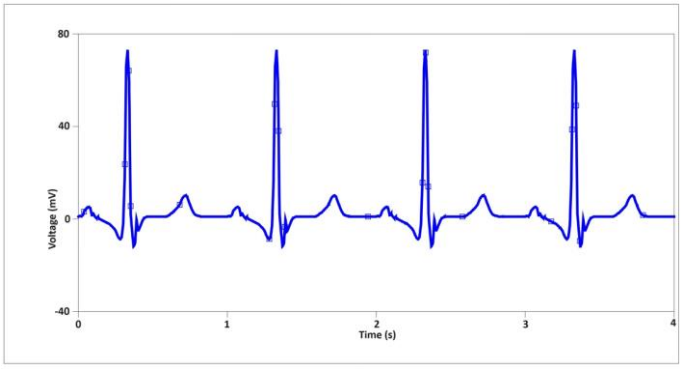

Fig. 4.7. Output of the Instrumentation Amplifier

The differential gain is around 20.65dB. The peak value of the QRS complex is around 300 mv.

4.3.3. Frequency response of the Band pass filter

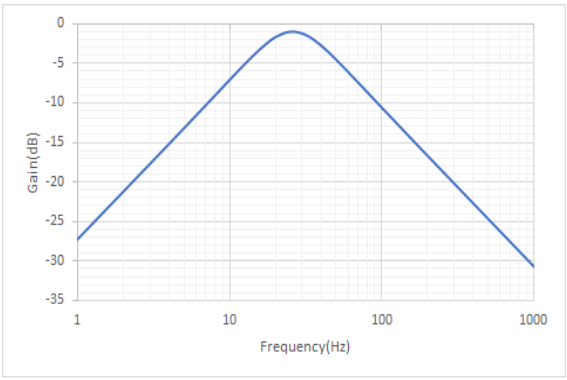

Fig. 4.8. Frequency response of the band pass filter

The corresponding R, C values are R_1 = 100 KΩ, C_1 = 159nF, R_2 = 275KΩ, C_2 = 25nF for a centre frequency of 25Hz. The bandwidth of the filter is around 30Hz.

4.3.4. Output of the Band pass filter

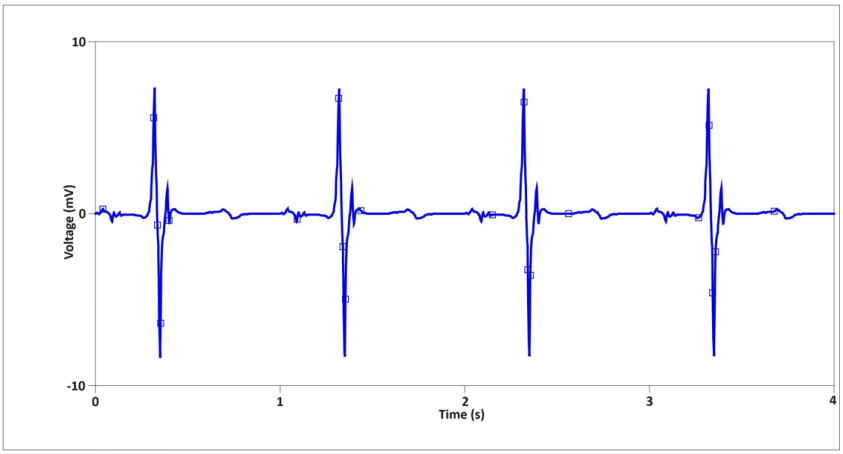

Fig. 4.9. Output of Band pass filter

The Band pass filter is designed such that it filters out only the QRS complex which is evident from figure 4.9. The magnitude level of the P-wave has attenuated much compared to the input P-wave and clamping is reduced which resolves the issue of false detections.

4.3.5. Output of the Sense Amplifier

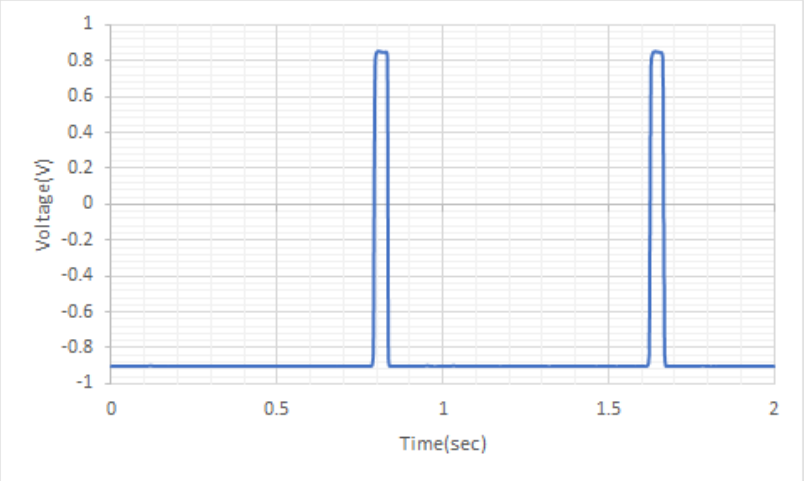

Fig. 4.10. Output of Sense Amplifier

The output of the comparator can be seen in figure 4.10. The threshold provided to the comparator varies depend on the person. A digital waveform having a dynamic range from +0.9 to -0.9V has been obtained which are the V_{dd} as well as V_{ss} of the comparator respectively. The pulse indicates the presence of QRS complex.

4.4 Conclusion

The DVCC based sense amplifier design has the input as test cardiac ECG signal and the output obtained at comparator of sense amplifier is digital pulses. This sense amplifier design comprises of an instrumentation amplifier of a single analog active block and two resistors. Filter also comprises of a single analog active block and a reactive network of 3 resistors and 2 capacitors. Comparator comprises of a single analog active block and a resistor. The power consumption of DVCC based sense amplifier is around 4.8 mW. Therefore in comparison with voltage mode sense amplifier, DVCC based sense amplifier has less circuit complexity and less power consumption. To increase further efficiency and to increase performance by electronic tunability of bias current and trans conductance (gm), another current mode analog active block DVCCTA was used.

CHAPTER 5

SENSE AMPLIFIER USING DVCCTA

5. Implementation of Sense Amplifier using DVCCTA

Sense amplifier has been implemented using Differential Voltage Current Conveyor Trans Conductance Amplifier (DVCCTA). In DVCCTA based design sense amplifier, instrumentation amplifier consists of a single analog active block DVCCTA and employs two resistors. Active band pass filter comprises of a single active block DVCCTA and a reactive network of three resistors and two capacitors. Comparator employs a single active block DVCCTA and a single resistor which detects the QRS complex by generating a digital pulse signal as output. In DVCCTA based sense amplifier DVCC acts at an input stage and OTA at an output stage.

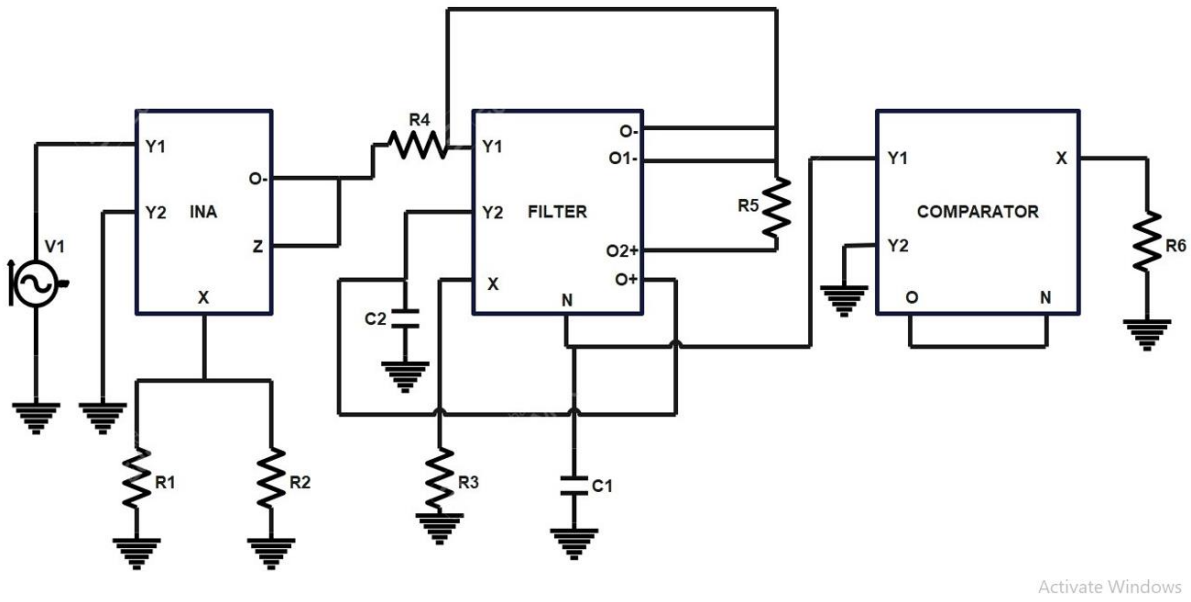

Fig. 5.1. Implementation of Sense Amplifier using DVCCTA

5.1 Differential Voltage Current Conveyor Trans conductance Amplifier (DVCCTA):

The active element referred to as a DVCCTA is an electronic tunable element in an analog signal processing blocks such as instrumentation amplifier, bi quad filter, Schmitt trigger, versatile modulator, and oscillator and in other analog applications. DVCCTA is a combination of two analog active blocks DVCC and OTA. DVCC is an input stage followed by OTA at an output stage. The DVCCTA block form

representation is shown in figure 5.1 which has three input ports among them two having high impedance (Y_1 and Y_2) and remaining one having low impedance (X). Beside it, Z is auxiliary output port whose voltage is transferred to current at trans-conductance type high impedance output ports (O-).

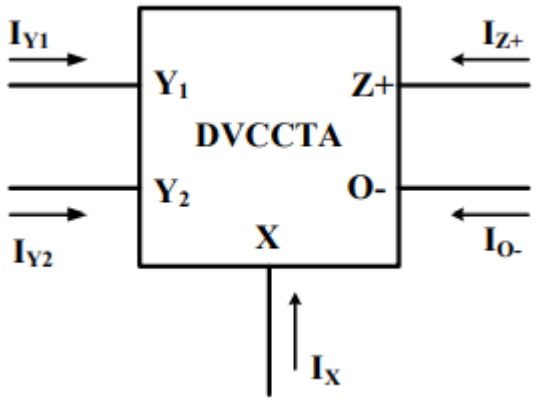

Fig. 5.2. DVCCTA Block

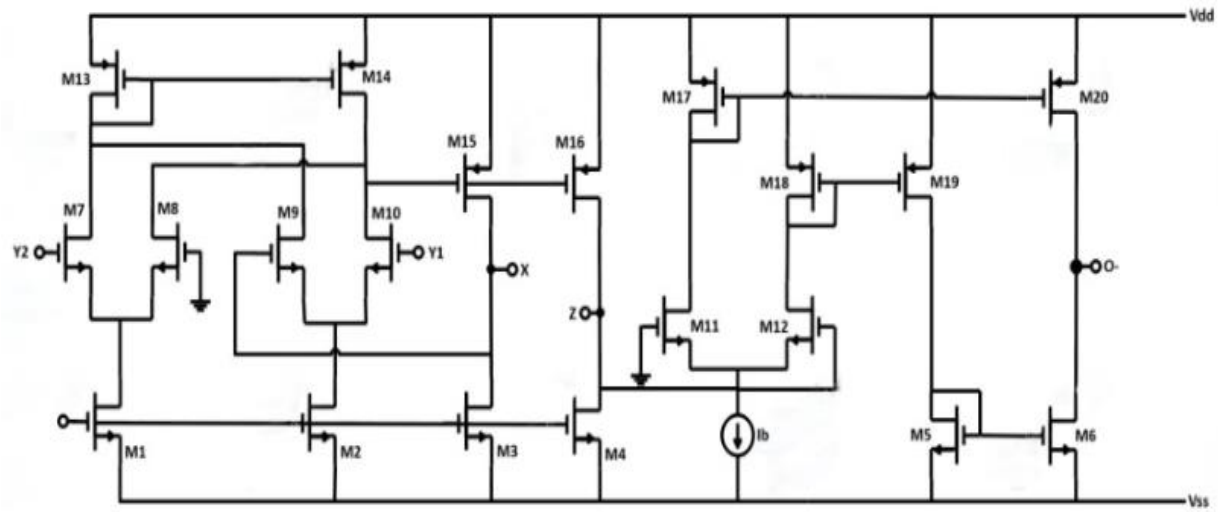

Fig. 5.3. Implementation of CMOS based DVCCTA

Internal relation of input and output ports of DVCCTA can be characterized by the following matrix equation. Characteristic equations or terminal equations of DVCCTA block is given by

$$I_{Y1} = I_{Y2} = 0$$

$$V_X = V_{Y1} - V_{Y2}$$

$$I_Z = I_X$$

$$I_O = -g_m V_{Z+} \qquad \rightarrow (1)$$

$$\begin{bmatrix} Iy1 \\ Iy2 \\ Vx \\ Iz \\ Io \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & \beta 1 & -\beta 2 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm gm \end{bmatrix} \begin{bmatrix} Ix \\ Vy1 \\ Vy2 \\ Vz \end{bmatrix}$$

DVCCTA is an electronically adjustable using as external biasing current (I_B) and is given by

$$g_m = \sqrt{\mu n \, cox \, (\frac{W}{L}) IB} \qquad \rightarrow (2)$$

The aspect ratio of MOS Transistors is given as in the following table:

MOS Transistors	**W/L(μm)**
$M_1 – M_6$	3/0.25
$M_7 – M_{10}$	1/0.25
$M_{11} – M_{12}$	5/0.18
$M_{13} – M1_6$	15/0.25
$M_{17} – M_{20}$	5/0.25

Table 5. Aspect ratios for the CMOS transistors in DVCCTA

Based on the regular analysis of the design, the current measured at the X terminal is calculated as

$$I_X = I_{R1} + I_{R2} = \frac{Vx}{R1} + \frac{Vx}{R2} \qquad \rightarrow (3)$$

Here the currents passing through the terminals Z and O are equal because of the short circuit connection between them.

$$I_Z = I_O \qquad \rightarrow (4)$$

From the port relation ($I_Z = I_X$) given in equation (1), can substitute the above equations (3) and (4) in this and get the following expression as:

$$I_O = \frac{Vx}{R1} + \frac{Vx}{R2} \qquad \rightarrow (5)$$

Again, from port relation, $I_{Y1} = I_{Y2} = 0$, $V_X = V_{Y1} - V_{Y2}$, $I_Z = I_X$, $I_O = -g_m V_{Z+}$, then

Equation (5) can be rewritten as

$$g_m \, Vout = (Vin1 - Vin2)\left(\frac{1}{R1} + \frac{1}{R2}\right) \rightarrow (6)$$

Equation (6) can be rewritten as

$$\frac{Vout}{(Vin1 - Vin2)} = \frac{1}{gm}\left(\frac{R1+R2}{R1\,R2}\right) \qquad \rightarrow (7)$$

By substituting R_1=R_2=R, Then the voltage mode IA's differential gain (A_{dm}) is written as follows

$$A_{dm} = \frac{Vout}{Vin1 - Vin2} = \frac{2}{Rgm} \qquad \rightarrow (8)$$

By utilizing trans conductance parameter (gm) of the DVCCTA and adjusting the external biasing current (I_B), the gain of INA can be electronically adjusted as per the above differential gain equation. However, it is important to note that the non-ideal characteristics of the DVCCTA may have an impact on the gain.

5.2 Circuit Analysis

5.2.1 Instrumentation Amplifier

Instrumentation amplifier incorporates single DVCCTA block and two grounded resistors. The differential voltage inputs applied at input terminals Y_1 and Y_2 and output is obtained at O- terminal. The aspect ratio of instrumentation amplifier is same as that of DVCCTA. The values of resistors are given by $R_1 = R_2 = 0.6K\Omega$, supply voltage $V_{dd} = -V_{SS} = 1.25V$, $V_B = -0.61V$ and $I_B = 10\mu A$. The internal CMOS implementation of DVCCTA based instrumentation amplifier is shown in figure 5.4. Implementation of DVCCTA based instrumentation amplifier is shown in figure 5.5.

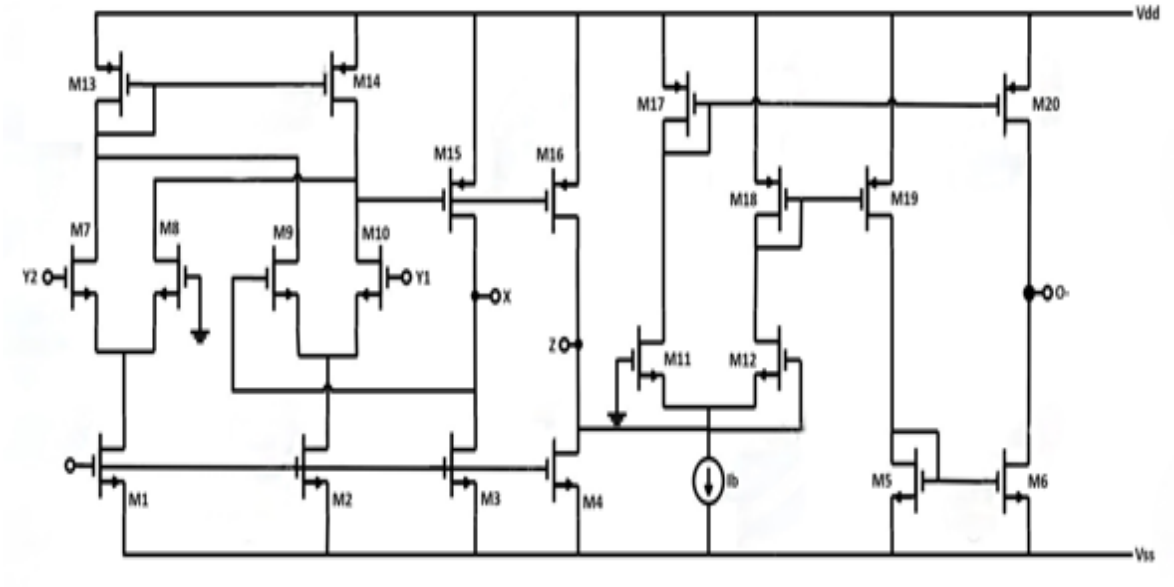

Fig. 5.4. Implementation of CMOS based INA

The differential gain of an IA is calculated by

$$A_{dm} = \frac{2}{Rgm} .$$

Where, $g_m = \sqrt{\mu n \, cox \, (\frac{W}{L}) 11{,}12 \;\; IB}$

$$\mu n = 327.3736992$$

$$C_{OX} = \frac{\epsilon ox}{Tox} = 8.422*10^{-7}$$

$$I_B = 10\mu A$$

$$g_m = 0.000276$$

$$A_{dm} = \frac{2}{0.6*1000*0.000276} = 12 = 25dB$$

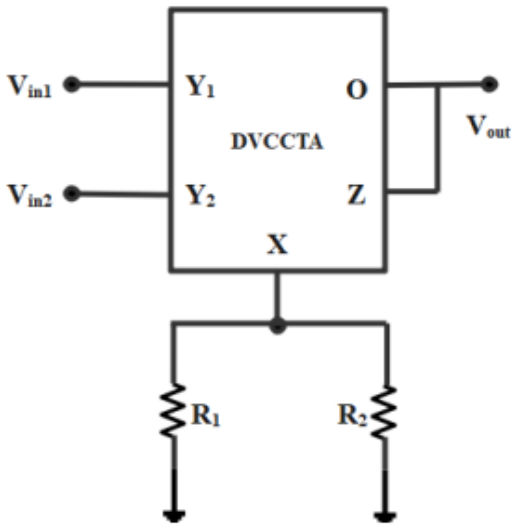

Fig. 5.5. DVCCTA based INA

5.2.2 Band Pass Filter:

Filter is used to remove the unwanted signals obtained from the IA output. Filter is the second stage of sense amplifier. Filter is implemented using DVCCTA and passive components of three resistors and two grounded capacitors. In the proposed various filter responses can be obtained like V_{HP}, V_{LP}, V_{BP}, V_{AP}, $V_{BR.}$ DVCCTA based filter block is shown in figure 5.6.

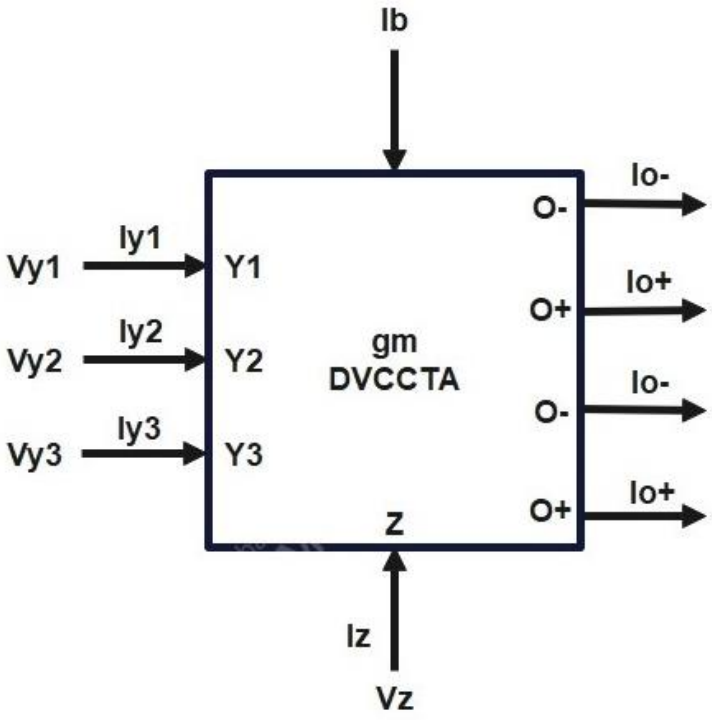

Fig. 5.6. DVCCTA block filter

The values of resistive and capacitive network is given by $R_1 = 1K\Omega$, $C_1 = C_2 = 0.835\mu F$, $g_m = 0.000276$. The cut-off frequency for band pass filter is around 100Hz and is given by

$$w_o = \sqrt{\frac{gm}{C1\ C2\ R1}}.$$

CMOS internal implementation of DVCCTA based filter is shown in figure 5.7 and DVCCTA based filter is shown in figure 5.8.

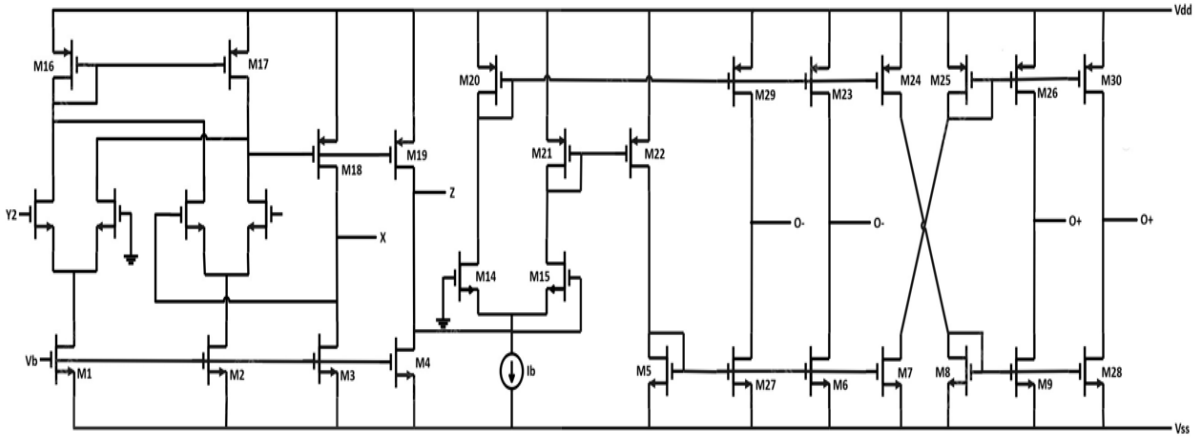

Fig. 5.7. Internal implementation of DVCCTA based filter

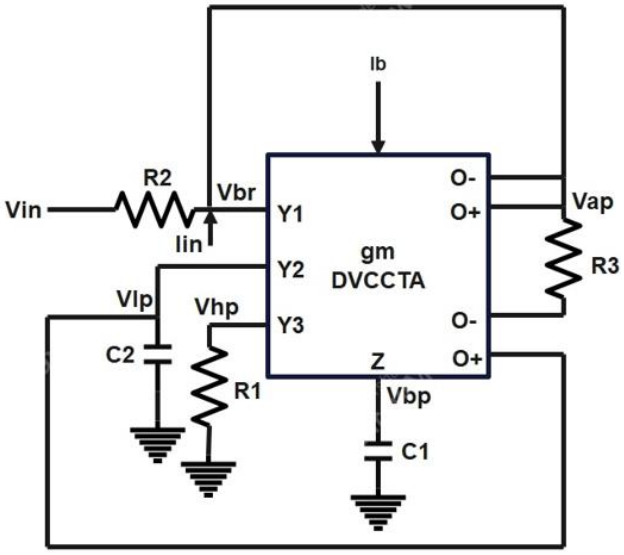

Fig. 5.8. DVCCTA based filter

Internal relation of input and output ports of DVCCTA can be characterized by the following matrix equation. Characteristic equations or terminal equations of DVCCTA block is given by

$$I_{Y1} = I_{Y2} = 0$$

$$V_X = V_{Y1} - V_{Y2}$$

$$I_Z = I_X$$

$$I_{O+} = g_m V_{Z+}$$

$$I_{O-} = -g_m V_{Z+}$$

$$\begin{bmatrix} Iy1 \\ Iy2 \\ Vx \\ Iz \\ Io+ \\ Io- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & \beta 1 & -\beta 2 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & +gm \\ 0 & 0 & 0 & -gm \end{bmatrix} \begin{bmatrix} Ix \\ Vy1 \\ Vy2 \\ Vz \end{bmatrix}$$

DVCCTA is an electronically adjustable using as external biasing current (I_B) and is given by

$$g_m = \sqrt{\mu n \, cox \, (\frac{W}{L}) 14{,}15 \;\; IB}$$

The aspect ratio of MOS Transistors is given as in the following table:

MOS Transistors	W/L(µm)
$M_1 - M_9, M_{27} - M_{28}$	4.32/0.36
$M_{10} - M_{13}$	1.44/0.36
$M_{14} - M_{15}$	21.6/0.36
$M_{16} - M1_9$	21.6/0.36
$M_{20} - M_{26}, M_{29} - M_{30}$	7.2/0.36

Table 6. Aspect ratios for the CMOS transistors in DVCCTA Filter

5.2.3 Comparator:

Comparator is the third stage of Sense Amplifier. It detects the QRS complex of the ECG signal by shorting O and X terminals together. It incorporates single DVCCTA block and a single resistor. It compares the analog signal at input and produces the digital output. CMOS internal implementation of comparator is same as that of INA. The input voltage inputs applied at input terminals Y_1 and Y_2 and output is obtained at Z terminal. The resistor connected at X terminal and is given by R=30KΩ. It should be able to differentiate QRS complex from the P-wave and T-wave.

The saturation voltage of a comparator can be controlled by the bias voltage $V_{b.}$ The aspect ratio of comparator is similar to INA. The supply voltage $V_{dd} = -V_{ss} =$ 1.25V and bias current is given by I_B = 10µA.

The transfer function of comparator is given by

$$\frac{Vz}{Vy1-Vy2} = \left(\frac{1}{R}\right)\left(\frac{1}{\pm Rgm}\right)$$

The final output of the sense amplifier is the digital signal and it indicates the presence of QRS complex. Depending on the comparator output pacing is determined. If the pulse obtained at comparator at particular intervals of time pacing is not required, else demand pacing is required. Implementation of DVCCTA based comparator is shown in figure 5.9.

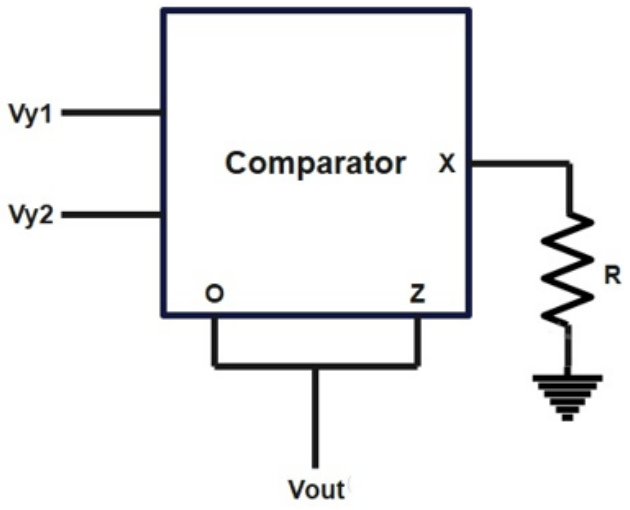

Fig. 5.9 Voltage mode DVCCTA based Comparator

Following are the characteristic equations that define the analog block:

$$Iy1 = Iy2 = 0;$$

$$V_X = Vy1 - Vy2;$$

$$I_{Z+} = Ix;$$

Here the currents passing through the terminals Z and O are equal because of the short circuit connection between them.

$$I_Z = I_O \quad \rightarrow (1)$$

The current at the terminal x is a product of trans-conductance (gm) and voltage

$$Ix = \pm gm\ V_Z \quad \rightarrow (2)$$

Now according to the ohms law based on that equation can be arranged as

$$\frac{Vx}{R} = \pm gm.\ Vz \quad \rightarrow (3)$$

From the port relations as $V_X = Vy1-Vy2$ now substitute it in the V_X in equation 3

$$\frac{Vy1-Vy2}{R} = \pm g_m V_Z \quad \rightarrow (4)$$

Now to acquire the relation $\frac{Vout}{Vin}$ as from the block diagram $V_{out} = V_Z$ and V_{in} is the difference between two inputs $V_{in} = Vy1-Vy2$

$$\frac{Vy1-Vy2}{Vz} = \pm g_m R \quad \rightarrow (5)$$

But $\frac{Vout}{Vin}$ is the equation requires so the equation will be as follows

$$\frac{Vz}{Vy1-Vy2} = \frac{1}{\pm gm.R} \quad \rightarrow (6)$$

5.3 Simulations

All the simulations have been performed in Cadence using TSMC 180nm technology. The input as well as the outputs of the Sense Amplifier have been simulated and plotted in this section. The figure 5.10 shows the input test cardiac signal used for the simulation. The figure 5.11 shows the output transient response of the first stage Instrumentation Amplifier. The figure 5.12 shows the Magnitude response of the Band pass filter. The figure 5.13 shows the output transient response of the Band pass filter. The figure 5.14 shows the response of the Comparator which is the final output of the Sense Amplifier.

5.3.1. Input test cardiac signal

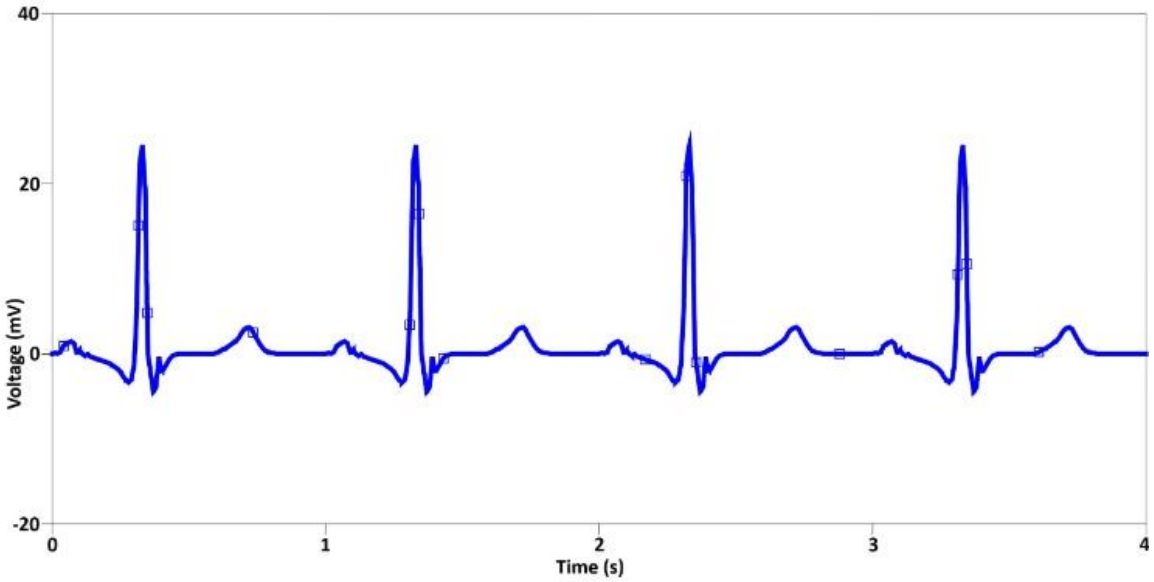

Fig. 5.10. Input test cardiac signal

The input cardiac signal is of very less magnitude. It has two full cycles each of 0.8 sec approximately. All the P-wave, QRS complex and the T-wave can be seen in the figure 5.10. The peak value of QRS complex is 24 mv.

5.3.2. Output waveform of the Instrumentation Amplifier

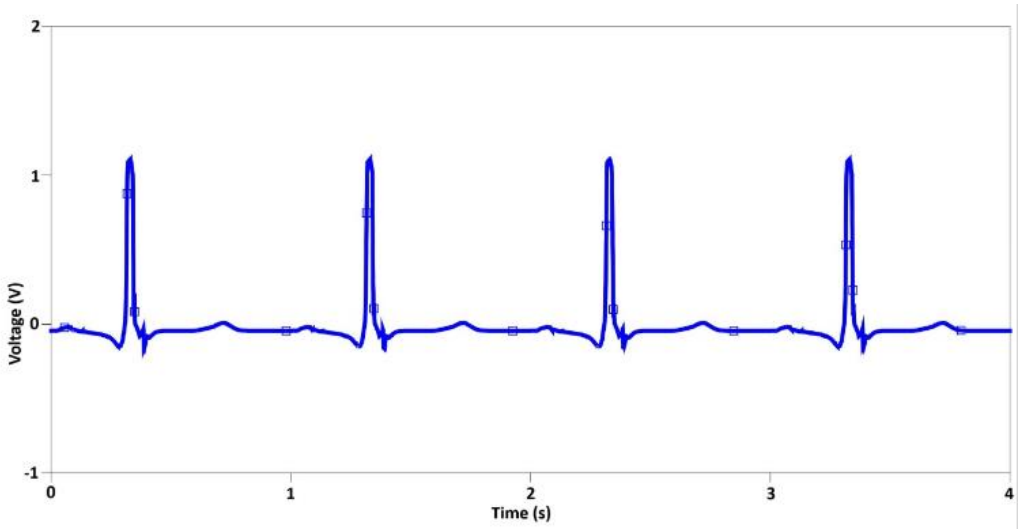

Fig. 5.11. Output of the Instrumentation Amplifier

The differential gain is around 24 db. The peak value of the QRS complex is around 1V.

Differential gain and output voltage obtained for different bias currents is as follows in the following table:

Bias Current I_B (µA)	Input Voltage V_{in} (mV)	Output Voltage V_{out} (mV)	Gain (dB)	
			Theoretical	Practical
10	24	1000	21	25
20	24	930	18.59	20
30	24	540	16.83	16.889
40	24	250	15	14.99
50	24	144	13.7	13.482

Table 7. Differential gain at different IB

5.3.3. Frequency response of the Band pass filter

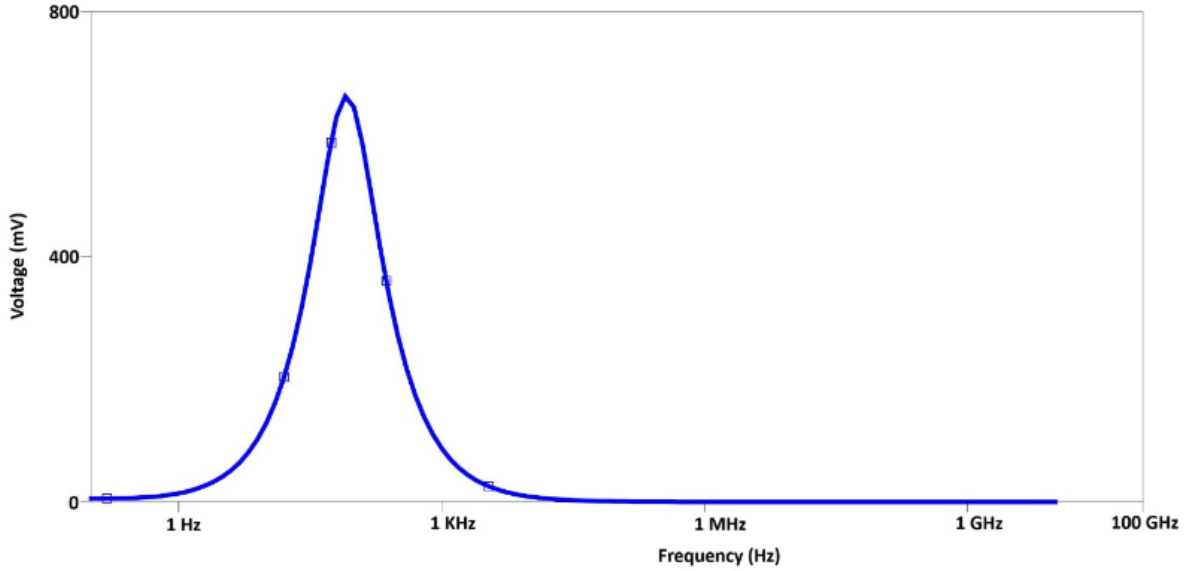

Fig. 5.12. Frequency response of the band pass filter

The corresponding R, C values are R_1 = 100 KΩ, C_1 = 159nF, R_2 = 275KΩ, C_2 = 25nF for a centre frequency of 25Hz. The bandwidth of the filter is around 30Hz.

5.3.4. Output of the Band pass filter

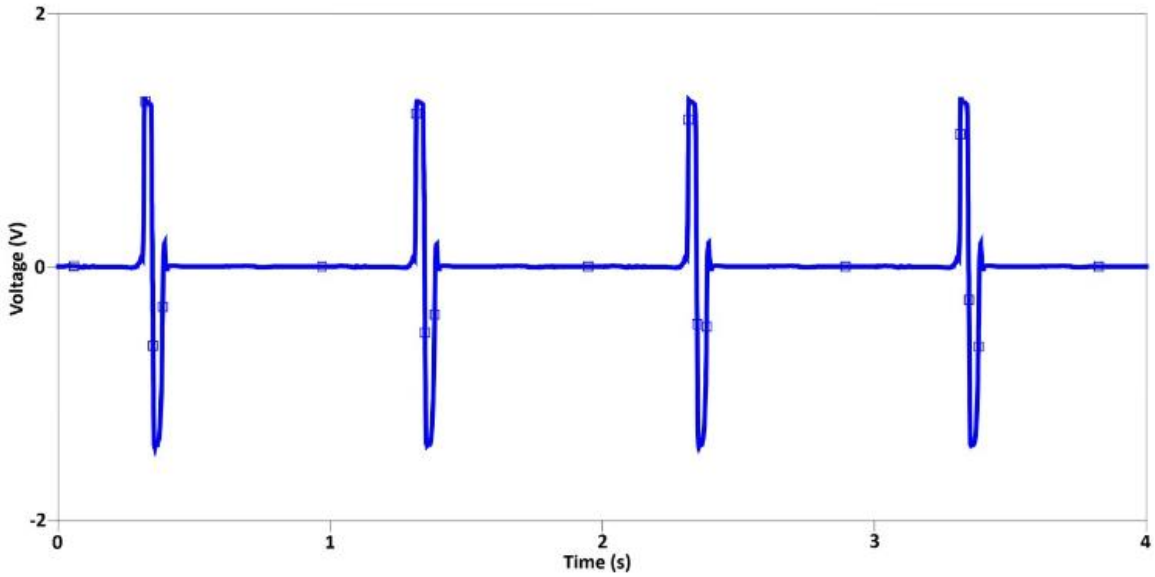

Fig. 5.13. Output of Band pass filter

The Band pass filter is designed such that it filters out only the QRS complex which is evident from figure 5.13. The magnitude level of the P-wave has attenuated much compared to the input P-wave and clamping is reduced which resolves the issue of false detections.

5.3.5 Output of the Sense Amplifier

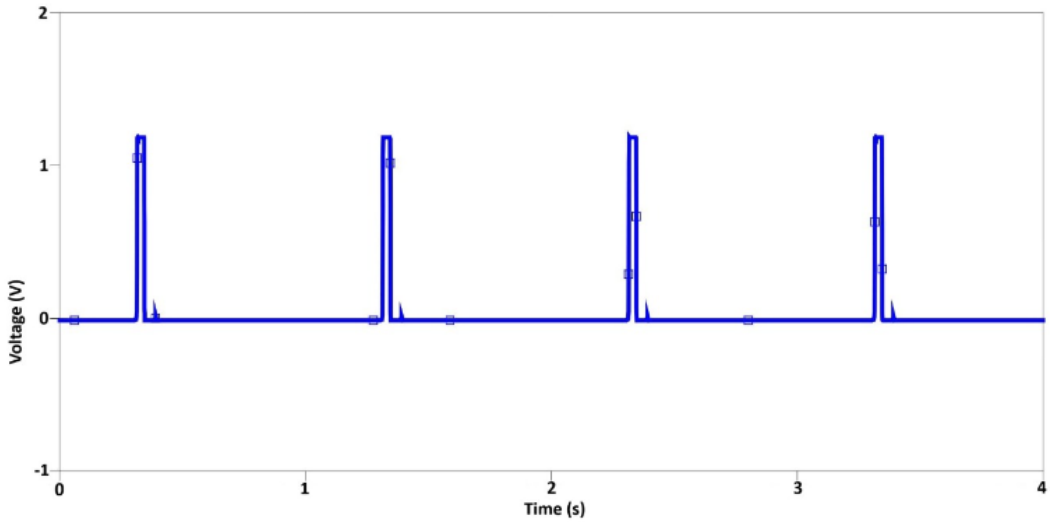

Fig. 5.14. Output of Sense Amplifier

The output of the comparator can be seen in figure 5.14. The threshold provided to the comparator varies depend on the person. A digital waveform having a dynamic range from +0.9 to -0.9V has been obtained which are the V_{dd} as well as V_{ss} of the comparator respectively. The pulse indicates the presence of QRS complex.

5.4 Conclusion

The DVCCTA based sense amplifier design has the input as test cardiac ECG signal and the output obtained at comparator of sense amplifier is digital pulses. This sense amplifier design comprises of an instrumentation amplifier of a single analog active block and two resistors similar to DVCC. Filter also comprises of a single analog active block and a reactive network of 3 resistors and 2 capacitors. Comparator comprises of a single analog active block and a resistor. The power consumption of DVCCTA based sense amplifier is around 3.3 mW. Therefore in comparison with DVCC based sense

amplifier, DVCCTA based sense amplifier has low power consumption and higher gain by electronic tunability of adjusting bias current and trans conductance (gm).

5.5 Comparison of VOA vs DVCC vs DVCCTA

Feature	Op-amp	DVCC	DVCCTA
Number of components in an instrumentation amplifier	3 active blocks 7R	1 active block 2R	1 active block 2R
Number of components in band pass filter	2 active blocks 8R, 4C	1 active block 3R, 2C	1 active block 3R, 2C
Number of components in comparator	1 active block Vth	1 active block 2R	1 active block 1R
Gain of INA	20.07db	20.65db	24db
Power consumption	20.6mW	4.8mW	3.3mW
Circuit Complexity	Difficult	Easy	Easy
Electronic Tunability	No	No	Yes

Table 8. Comparison of VOA vs DVCC vs DVCCTA

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

The motive of this work is to develop a model that can depict the functionality of a real time Cardiac Pacemaker. This is a device which has many critical parameters and their improper tuning may be life threatening. We have considered few of them that are related to our present work and tried to optimize them to the possible extent.

The front end design of the Sense Amplifier has been implemented in Cadence using TSMC 180 nm technology. The simulations have been generated and verified with the real time behavior. A power reduction of about 10 times has been observed with the DVCCTA based Sense Amplifier compared to that of the Op-amp based sense amplifier and DVCC based sense amplifier. The sense amplifier is designed by cascading the instrumentation amplifier, band pass filter and comparator.

This DVCCTA is an analog active block which comprises the features of two blocks DVCC and OTA. The OTA has a special feature of electronic tunability by tuning the bias current (I_B) and trans conductance (gm) can have control over the gain.

The advancement in the VLSI technology is largely helpful in scaling of the device to achieve much more efficiency. It should be made compatible with the leads, battery, antennas for communication. It can be interfaced with IOT so that the doctors as well as patients can have an easy access to the data.

6.2 Future scope

- Implement the peripheral for the transmission of the data related to the pacing.
- Integrating the front end and back end in a single integrated unit.
- Real time implementation by using FPGA.
- Dual Sensor Approach for the rate responsive pacing and further optimization of the algorithms.
- Optimize the power dissipation by reducing it.

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