Sai Sreenivas K

Indian Institute of Technology, Madras

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Education

Program	Institution	% (or) CGPA
Dual Degree in CSE	Indian Institute of Technology, Madras	8.24 (Major: 8.41)
XII	Pratibha Jr.College, Hyderabad	91.3
X	Gowtham Model School, Hyderabad	91.6

Scholastic Achievements

- All India Rank 402 in IIT-JEE 2008, among top 0.1%.
- Top 0.15% in AIEEE 2008 & Eamcet 2008.
- District 5th in *Matrusri* talent search exam.

Key Courses

- Graph Theory, Machine Learning, Design & Analysis of Algorithms, Software Engineering, Probability & Stochastic processes, Natural Language Processing, Modern Compilers: Theory & Practice, Kernel Methods for pattern analysis, Parallel Computer Architecture, Language Translators, VLSI Design Automation Algorithms, Distribued Computing, Operating Systems

Interests

- Performance oriented programming, Machine Learning & Algorithms.
- Probability & Statistics.

Skills

- **Languages:**
  - C, C++, Java & Objective-C
  - Python, MATLAB & bash scripting
  - Common Lisp, Prolog & Verilog
  - LaTeX
- **Linux Operating System**
  - Familiar with Unix BSD sockets & pthreads libraries.
  - Unix tools: Flex, Yacc, Git, Vim & Eclipse.
- **Large Software Frameworks**
  - LLVM Compiler for C++
  - Jikes-RVM a java virtual machine

Master's Thesis

- **Machine Learning techniques for Tuning Java-RTE**
  Guide: Dr.Shankar Balachandran *August 2012 - May 2013*
  - Architecture specific tuning in Java-RTE.
  - Automatic construction of compiler heuristics using statistical analysis.
  - Worked on java research framework *Jikes-RVM*.

Internships

- **IBM-HPC Labs** Bangalore
  Mentor: Seshasayee V Subramanian *May 2012 - July 2012*

- Parallel Algorithms for Big data Analytics
- Implemented parallel version for *K-Means clustering* algorithm on *MR-MPI* frameworks
- Scaleup & Scaleout is measured across several data upto 5 high compute nodes

- **Juniper Networks** Bangalore
  Mentor: Uday Kishore *May 2011 - July 2011*
  - Analysis & Recommendations for migration of centralized database to distribued file systems & databases

Experience

- **Kiwi Inc.** Bangalore
  July 2013 - Present
  - Working on cross-platform game developement for iOS & android.
  - Worked on both client and server side development for the game application.

Past projects

- **Strength reduction of python loops to Map, Reduce & Filter**
  Instructor: Dr.Shankar Balachandran *Aug 2011 – Nov 2011*
  - Designed and implemented Control & Data flow analyses for python programs.
  - Implemented to handle *for* loops and *nested for* loops
  - Transformations are implemented as pass structure.
  - Experimented with real time program: *Association rule mining*
- **Spam Filter**
  Instructor: Dr.Sutanu Chakraborti *Aug 2011 – Nov 2011*
  - Designed and implemented *Bayesian Spam filter* for spam classification
- **VLSI Automation algorithms**
  Instructor: Dr.Shankar Balachandran *Jan 2011 – April 2011*
  - Implemented placement heuristics for VLSI chips to minimize the chip area & the total wire length.
  - Achieved promising results on IBM benchmarks.
- **Pint-OS**
  Instructor: Dr.Krishna Sivalingam *Aug 2010 – Nov 2010*
  - Pint-OS a partially developed kernel.
  - Implemented priority scheduling, system calls & demand paging.
- **Compiler for Pascal**
  Instructor: Dr.Siva Ram Murty *Aug 2010 – Nov 2010*
  - Developed compiler for Pascal language, starting from syntax analyzer till the generation of intermediate code in C.
  - Implemented using Unix tools Flex, Yacc & C languague.
- **Dead block detection in cache**
  Instructor: Dr.Madhu Mutyam *Aug 2010 – Nov 2010*
  - Simulated dead block detection & eviction in using cache burst techniques.
  - Implemented using M5 simulator.
- **Computational Biology**
  Guide: Dr.Ashish V Tendulkar *May 2010 – July 2010*
  - Protiens represented as graphs, task is to extract various graph properties.
  - Implemented various graph algorithms in C++.
- **Case Based Reasoning**
  Instructor: Dr.Sutanu Chakraborti *Jan 2012 – April 2012*
  - Implemented *Case Based Reasoning System for Genre classification* in MATLAB.

- **4-Bit Processor**
  Instructor: Dr.Madhu Mutyam *Aug 2009 – Nov 2009*
  - Designed and implemented various components of processor such as ALU, instruction decoder, & register files.
  - Implemented in Verilog-HDL.

Positions of Responsibility

- Events core team member for Exebit-2012.
- Coodinator for workshop on *Parallel programming* for Exebit-2011.
- Design coordinator for Exebit-2010.