Implementing a Bang Bang Phase Detector in 28nm CMOS Technology

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***Abstract*—In this paper the design and implementation of a bang bang phase detector(BBPD) in 28 nm CMOS technology is discussed. This is a binary phase detector unlike the conventional phase frequency detector.**

***Index Terms*—bang bang phase detector(BBPD), Phase locked loop(PLL), frequency synthesizers.**

I. Introduction

The basic operation of a phase detector is to take in two input signals(reference and clock), compare them and generate two other output signals(Up and down) and determine which one of the two input signals lead/lags the other. Depending upon the kind of application intended, there are different topologies of phase detectors. Broadly they are classified into linear and non-linear phase detectors based on the gain of the phase detector. The gain of a phase detector is given by Eq.1.

$$Gain\ of\ PD = \frac{Duty\ cycle\ of\ output}{phase\ difference\ of\ input} \tag{1}$$

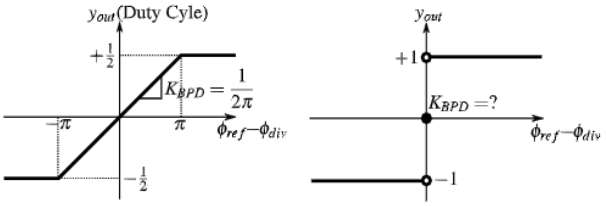

Fig. 1. (a). Gain of linear phase detector (b). Gain of binary phase detector

II. Design Architecture

Fig. 2 shows the circuit of alexander phase detector which gives the output pulses which are proportional to the sign of the phase difference between the given input signals. Due to this binary nature of the phase detector it is termed as bang bang phase detector(BBPD). This phase detector takes the reference and divider output signals, sample them with positive and negative edge of the clock respectively and then synchronized them using flip-flops. The output of the first flip-flop(Q1) and output of the fourth flip-flop(Q4) are XOR-ed to give the UP signal, similarly the output of the second flip-flop(Q2) and flip-flop(Q4) are XOR-ed to get the DOWN signal. This phase detector is most commonly used in CDR applications where the clock and data rates are nearly equal i.e, same frequency.

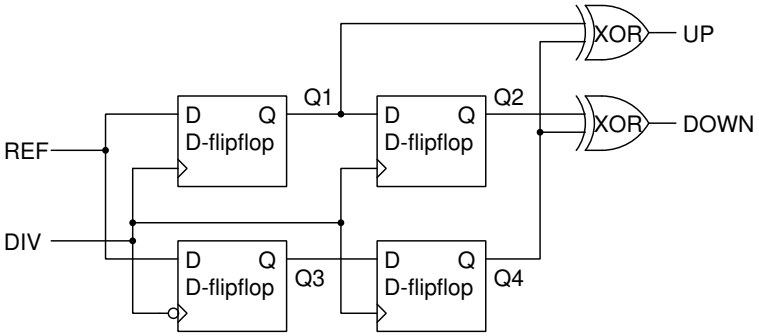

Fig. 2. Alexander phase detector

III. Simulation results

Fig.3 shows the output of the alexander phase detector for the two cases - (a) clock leads the data signal and (b) clock lags the data signal.

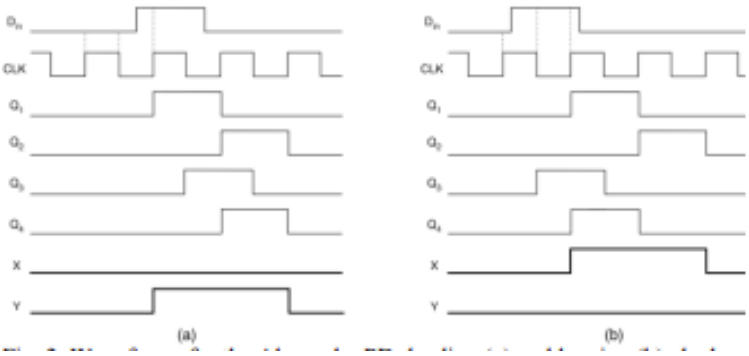

Fig. 3. Output waveform of the Alexander phase detector (a)Clock leads data (b)Clock lags data

References

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