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1. a). clock cycle time equal to slowest individual stage and it is 350 ps.

For non-pipeline processor is 250 + 350 + 150 + 300 + 200 = 1250 ps

b). lathency of pipeline is still the same.

so total latency = 5. (cycle time)

= 5. 350 = 1750 ps.

lathency of none-pipeline is still 1250 ps.

c). split ID stage since it has highest lathency. Then MEM has highest lathency, which make the pipeline lathency is 300 ps. This is the new cycle cycle time.

d). if no stall or hazard, ultization of data memory is 20% (load) + 15% (store) = 35%.

e). if no stall or hazard, ultization of write-reg is 45% (ALU) + 20% (load) = 65%

8).

2). a). without forwarding: $t_1 = 25n \cdot t_{cycle}$

$= 5 \cdot 250 \cdot 5n$

$= 6250n\,ps$

with forwarding: $t_2 = 1.05n \cdot t_{cycle}$

$= 1575n\,ps$

$Speedup = \frac{6250}{1575} = \underline{3.968}$

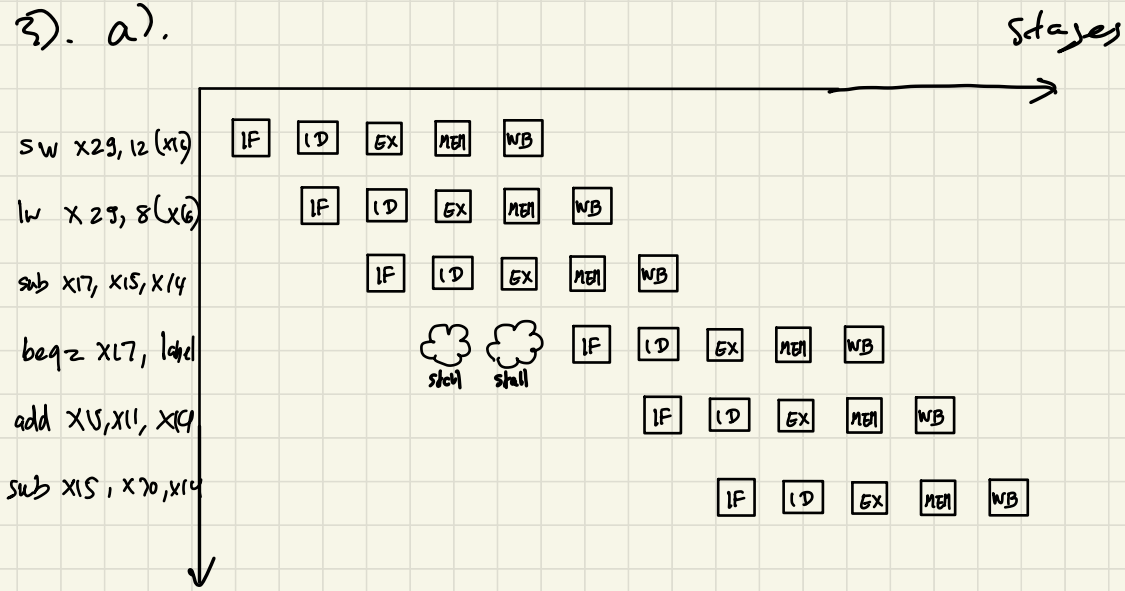
b). K: extra stall

$t = (n+1+K) \cdot 5.300 <= t_1$

$K <= 3.167n$

There can have 3.17 extra nop instructions.

3). a).



b). No, structure hazard can be improved by proper hardware.

c). No, they must be fetched from the instruction memory. To avoid this we need to use proper hardware the keep the instruction memory distinct from data memory.

4). a. Before iteration:

Mem	ALU	Cycle
li X12, 0		0
	Jal ENT	1
	bne X12, X13, TOP	2
	slli X5, X12, 3	3

first iteration

Mem	ALU	Cycle
	add x6, x10, x5	4
lw x7, 0(x6)		5
lw x29, 4(x6)		6
		7
	sub x30, x7, x29	8
	add x31, x11, x5	9
sw x30, 0(x31)	addi x12, x12, 2	10
	bne x12, x13, TOP	11
	slli x5, x12, 3	12

b). one-issue processor : cycle = 10n

two-issue processor : cycle = 9n

$$Speedup = \frac{10}{9} = 1.11$$

c). Move slli x5, x12, 3 out from the loop, we have

```
slli x13, x13, 3
add  x6, x13, x10
add  x31, x13, x11
beq  x1, x10, exit
TOP:
lw   x7, 0(x6)

lw   x29, -4(x6)
```

```
sub  x30, x29, x7
sw   x30, 4(x31)
addi x6, x6, 8
addi x30, x30, -8
blt  x6, x10, TOP
Exit:
```

d).

```
slli x13, x13, 3
add  x6, x14, x10
add  x31, x14, x11
beq  x1, x10, exit
TOP:
    lw x7, 0(x6)
    addi x31, x31, -8
    lw   x29, -4(x6)
    addi x6, x6, -8
    sub  x30, x29, x7
    sw   x30, 4(x31)
    blt  x6, x10, TOP
    Exit:
```

e).

MEM	ALU	cycle
lw x7, 0(x6)	addi x13, x13, -8	1
lw x29, -4(x6)		2
	addi x6, x6, -8	3
	sub x30, x29, x7	4
sw x30, 4(x31)	bne x6, x10, TOP	5

$$\text{Speedup} = \frac{8}{6} = 1.428$$