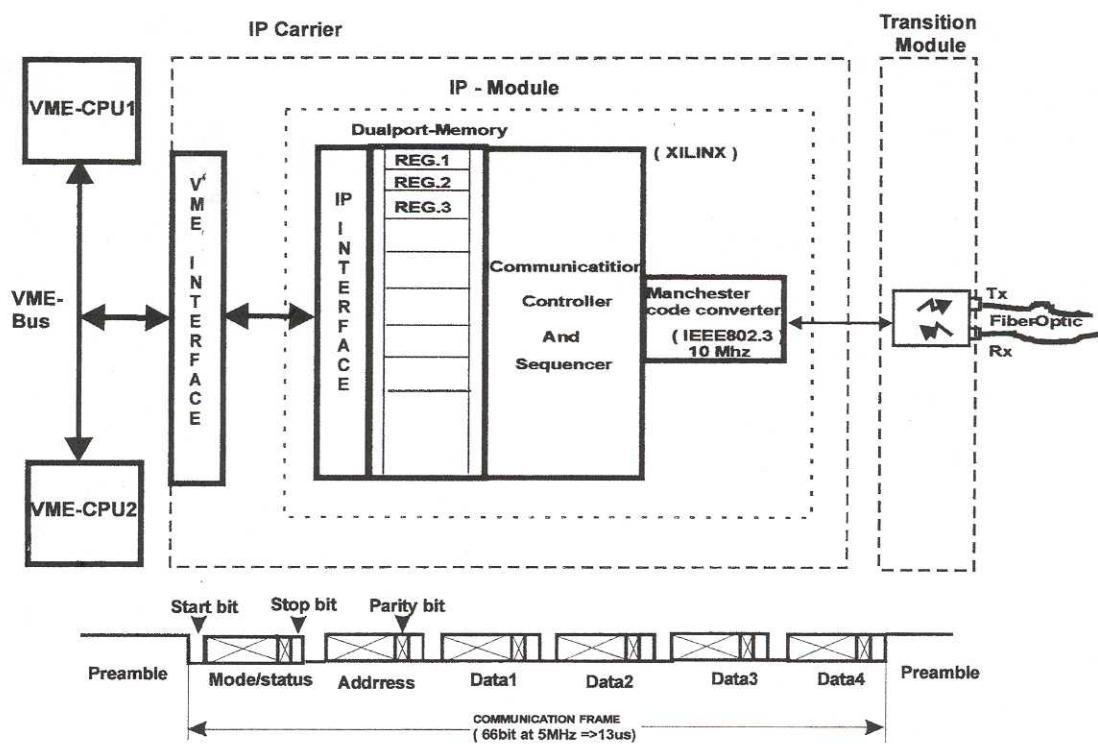
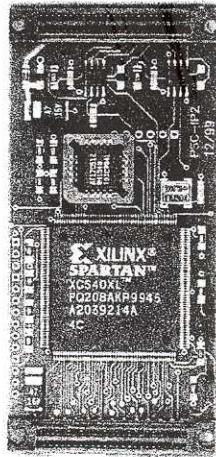


SLS

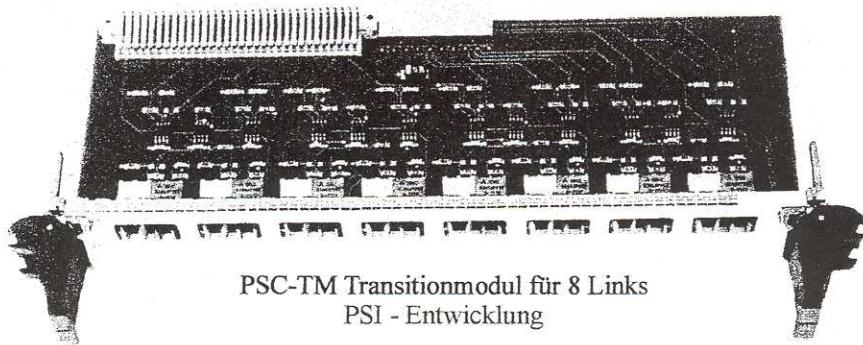
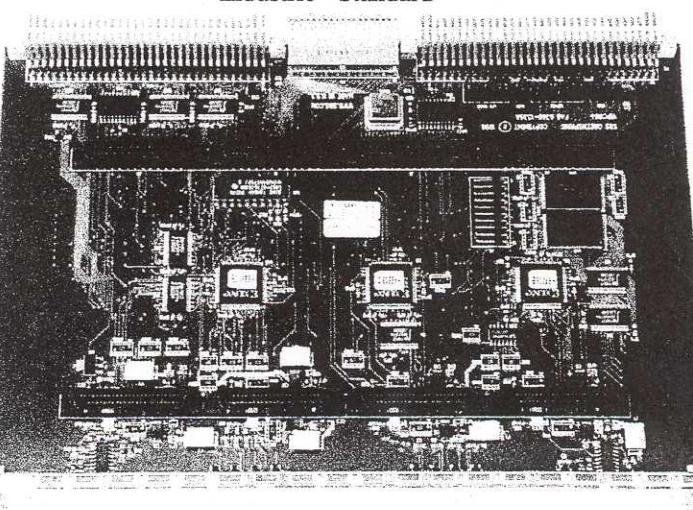
OPTICAL FIBRE LINK VME-INTERFACE FUER POWER SUPPLY CONTROLLER



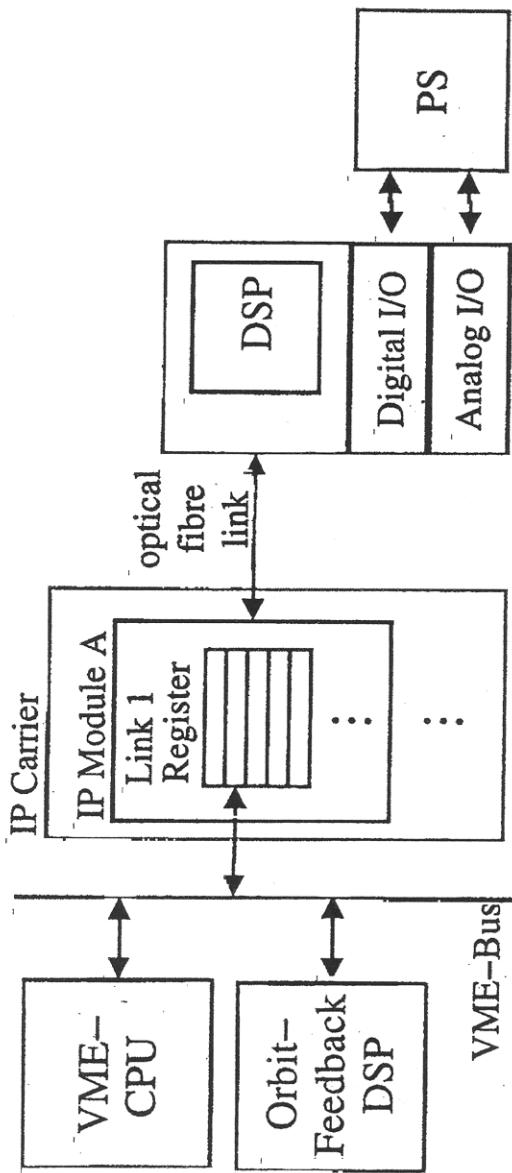
PSC-IP2
Industriepack für 2 Links
PSI - Entwicklung



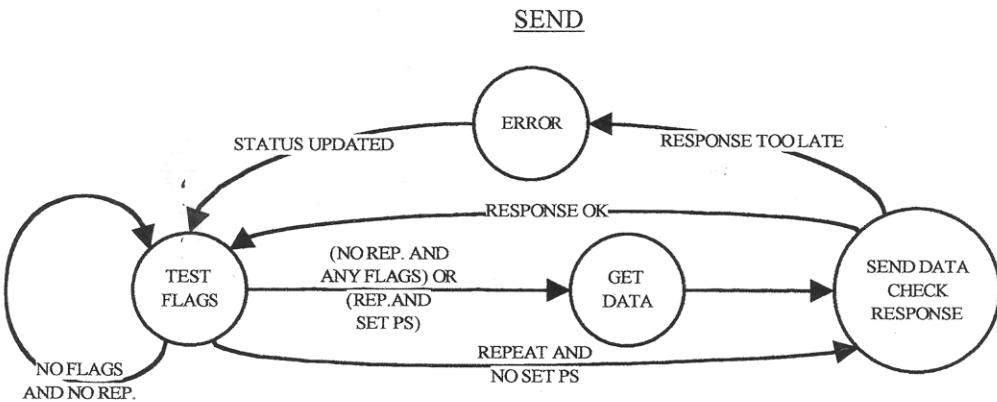
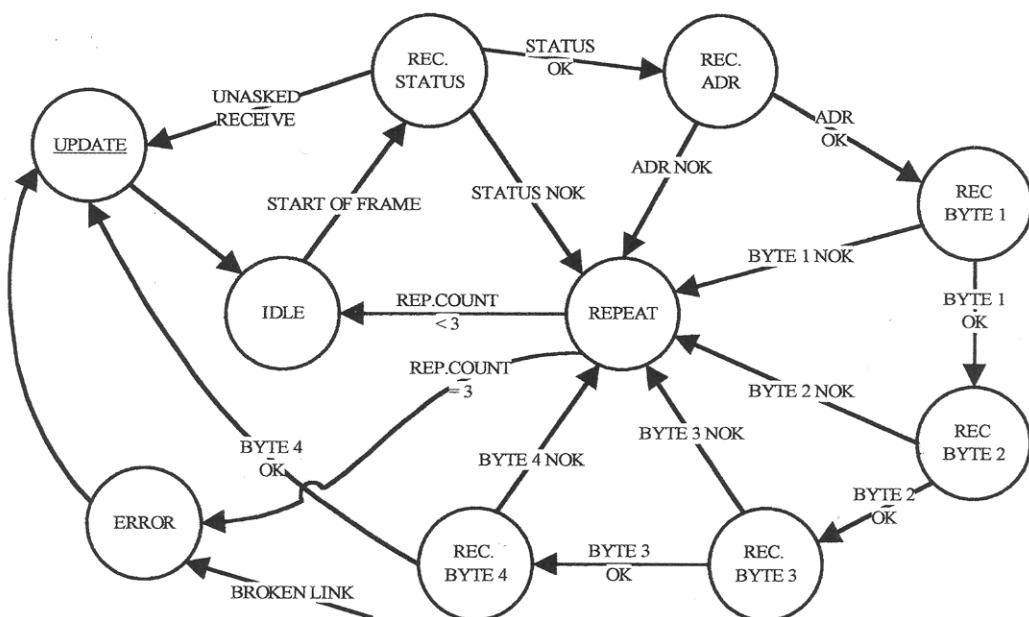
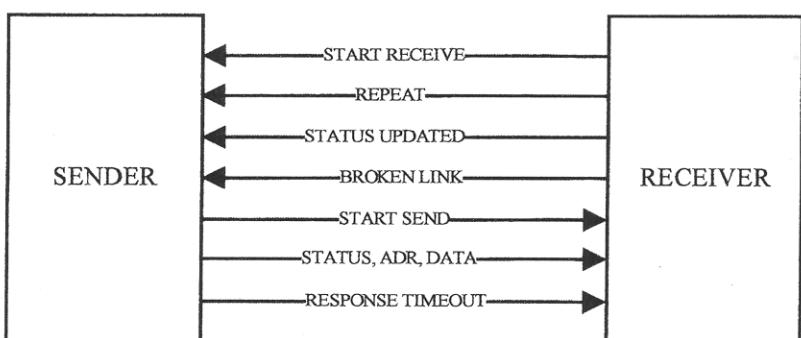
VIPC664 Carrierboard für 4 PSC-IP2 max. 8 Links
Industrie - Standard



PSC-TM Transitionmodul für 8 Links
PSI - Entwicklung



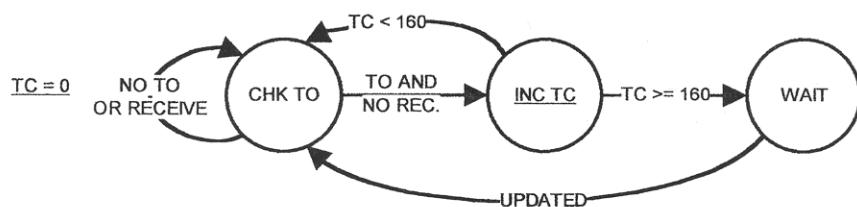
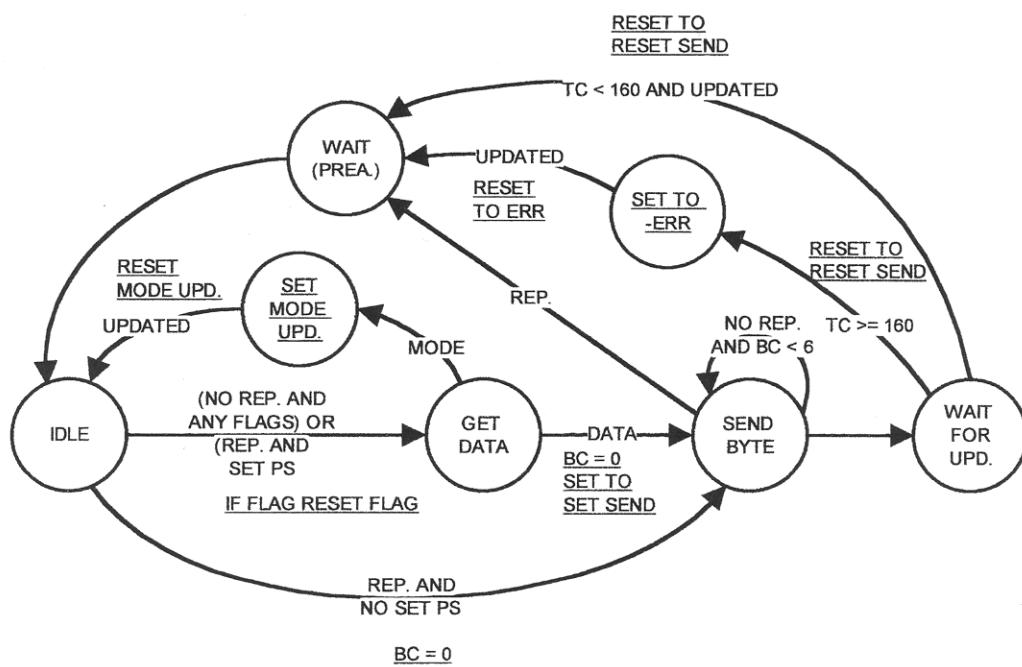
Picture 1: Overview of the planned SI S power supply control

RECEIVEINTERCONNECTION

SLS Point to Point Link

SEND State Transition Diagramm

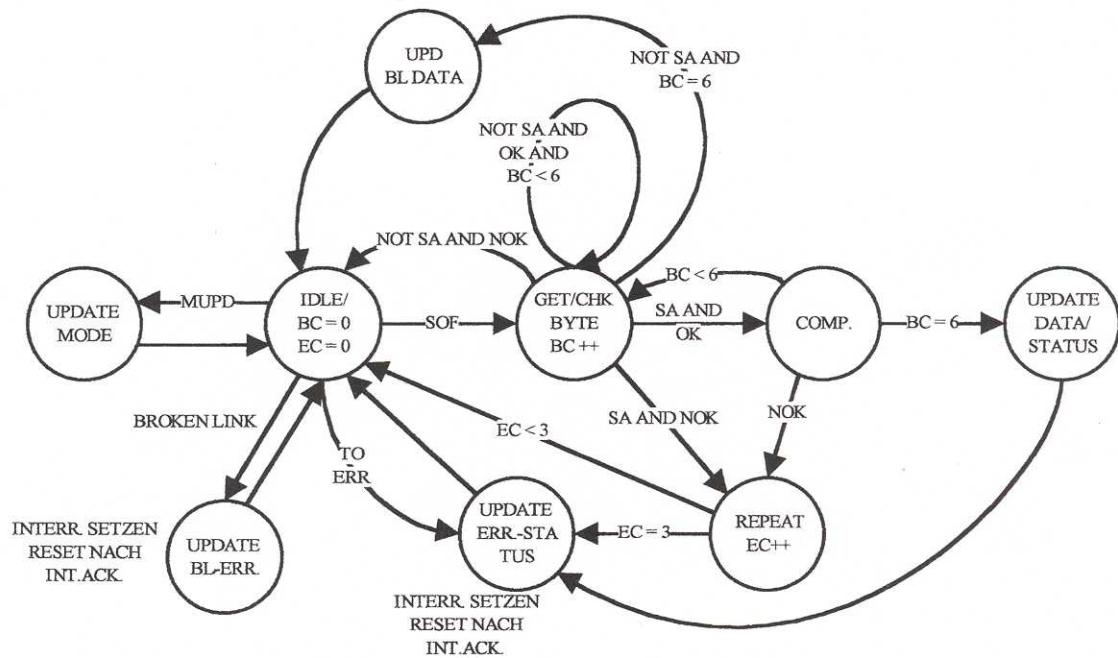
BC = BYTECOUNT **TO** = TIMEOUT **TC** = TIMER COUNTER **REP** = REPEAT CLOCK = 8 MHZ



SLS Point to Point Link

RECEIVE State Transition Diagramm

SOF = START OF FRAME **BC** = BYTECOUNT **EC** = ERRORCOUNT **BL** = BROKEN LINK ERROR **MUPD** = MODE UPDATE VON VME
SA = SEND AKTIV CLOCK = 8 MHz



I/O Memory – Mapping / Bitbelegungen

Default I/O base address: 0x6000 (konfigurierbar)

Offset IP A Link 1 0x0000, Link 2 0x0040

Offset IP B Link 3 0x0100, Link 4 0x0140

Offset IP C Link 5 0x0200, Link 6 0x0240

Offset IP D Link 7 0x0300, Link 8 0x0340

		write registers	read registers																
		high byte low byte	high byte low byte																
base+0	high priority write (set PS current)	<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care	
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don't care																			
base+8	write word	<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care	
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don't care																			
base+16	read word	<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care	
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don't care																			
base+24	write waveform	<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care	
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base+32	read waveform	<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care	
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base+40	broken Transmit		<table border="1"> <tr><td>status</td><td>address</td></tr> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (lower word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	status	address	data (higher word)		data (lower word)		don't care									
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base+48	FPGA Status	<table border="1"> <tr><td>data (high word)</td><td></td></tr> <tr><td>data (mid word)</td><td></td></tr> <tr><td>data (low word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	data (high word)		data (mid word)		data (low word)		don't care		<table border="1"> <tr><td>data (higher word)</td><td></td></tr> <tr><td>data (mid word)</td><td></td></tr> <tr><td>data (low word)</td><td></td></tr> <tr><td>don't care</td><td></td></tr> </table>	data (higher word)		data (mid word)		data (low word)		don't care	
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base+56	register status		<table border="1"> <tr><td>data</td><td></td></tr> </table>	data															
data																			
base+58	interrupt vector	<table border="1"> <tr><td>don't care</td><td>vector</td></tr> </table>	don't care	vector															
don't care	vector																		

Register – Status

Bit	Funktion	1	0
15	Fehlerdiagnose	Fehler	kein Fehler
14 .. 5	keine		
4	read waveform	ausgeführt	in Arbeit oder idle
3	write waveform	ausgeführt	in Arbeit oder idle
2	read word	ausgeführt	in Arbeit oder idle
1	write word	ausgeführt	in Arbeit oder idle
0	write current	ausgeführt	in Arbeit oder idle

FPGA – Status

write

Bit	Funktion	1	0
high word			
15	Fehlerzähler	clear	dont'care
14 .. 1	keine		
0	Mode	loopback	normal
mid word	keine		
low word	keine		

read

Bit	Funktion	1	0
high word			
15 .. 8	Fehlerzähler	Zählerstand	Zählerstand
7	link down	error	ok
6	transmit error	error	ok
5 .. 1	keine		
0	Mode	loopback	normal
mid word			
15	keine		
14	parity	error	ok
13	break	error	ok
12	framing	error	ok
11	compare	error	ok
10	timeout	error	ok
9 .. 5	wie set current	error	ok
4 .. 0	wie set current	error	ok
low word			
15 .. 10	keine		
9 .. 5	wie set current	error	ok
4 .. 0	wie set current	error	ok
			write waveform
			read waveform

MEMORANDUM

Date: 30. July 1999

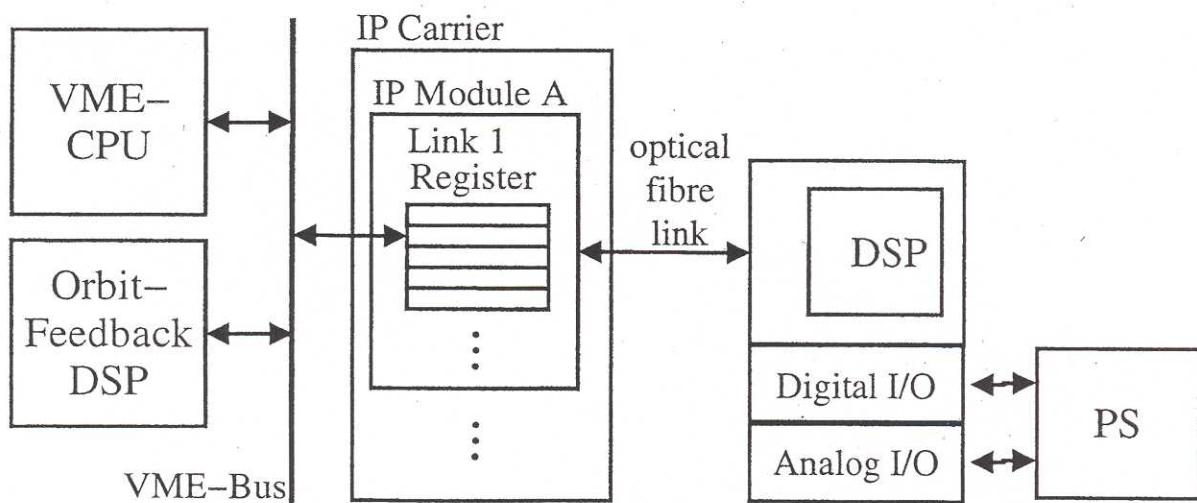
From: Andreas Lüdeke
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To: Martin Emmenegger, Guido Janser, Felix Jenni, Ivo Jirousek
cc: Steve Hunt, Hans-Ullrich Boksberger, Albin Wrulich

SLS Power Supply Control: Optical Fibre Link VME Interface Design Draft 1.3

1. Overview

The following picture 1 shows an overview of the planned SLS power supply control:



Picture 1: Overview of the planned SLS power supply control

The VME-CPU will write in memory mapped registers of an IndustryPack module. This causes the module to write over the optical fibre link to the power supply controller. The answer from the controller comes back across the fibre link and will be written in the corresponding read register. An interrupt will tell the CPU that new data has arrived. In the orbit-feedback mode the feedback DSP will write directly into a set-PS-current register. The CPU must not write in this register as long as the DSP is in this mode. Other read/write commands could be done simultaneously by the CPU.

2. Memory space of the IndustryPack modules

The links on an IndustryPack module are implemented with FPGAs. A FPGA has 64 bytes write-only memory and 64 bytes read-only memory in the VME I/O memory space. They will be memory mapped to the same VME address space. I.e. a byte-write to the base address will affect the write-register status byte and not the read register status. The read registers can only be written by the FPGA.

Table 1 shows the definition of the I/O memory-space for each link as defined in reference 2.

The value for 'base' adds up from the base address of the carrier board (default 0x6000), the offset for each module (0x100) and the offset of the link in the module (two links per module, offset 0x40). The offsets for the eight possible links are:

IP Module A Link 1: 0x0000, IP Module A Link 2: 0x0040, IP Module A ID: 0x0080,

IP Module B Link 3: 0x0100, IP Module B Link 4: 0x0140, IP Module B ID: 0x0180,

IP Module C Link 5: 0x0200, IP Module C Link 6: 0x0240, IP Module C ID: 0x0280,

IP Module D Link 7: 0x0300, IP Module D Link 8: 0x0340. IP Module D ID: 0x0380,

A maximum of seven links per carrier board are allowed due to limited space on the transition module which connects the carrier board with the optical fibre link, link 8 cannot be used therefore.

The memory is grouped in six registers of six bytes each (in the following just called "register"), a two byte register-status which is read-only from the CPU and one byte write-only for the interrupt vector. If an address is not specified in the table 1 than it has no function and is disregarded by the FPGA.

For each of the registers an interrupt will be given if they are ready to be written or when new data has arrived in the read register. The register-status word determine with flag bits, which register is ready to be read or to be written into. The register-status will be updated by the FPGA before raising an interrupt. The FPGA can raise an interrupt if he detects an error with the same procedure than for the registers.

All registers have big-endian byte order i.e. the least significant bits of a word are in the byte with the higher address. This is the Byte order of the VME Bus, the byte order of the protocol of the optical fibre link is little-endian.

3. Access modes

The communication between the EPICS process database and the FPGA will be done by an interrupt handler. There are five different forms of access to the power supply controller. They correspond to the first five registers of the FPGA and will be described in the following sections.

The set-PS-current, read and write rates are all limited to 10 kHz each by the power supply controller. The FPGA will take care that these rates will not be exceeded. That implies that a write to the data field of any register will not necessarily handled immediately by the FPGA.

The FPGA will react to a write in the higher word of a register data field. He will send the data together with the address to the PS controller. When he received the answer from the PS controller he check it for transmission errors. In case of an error he will repeat the sending up to three times. If it fails the third time he will just write the return status to the status field of the corresponding register and set the error flag.

The FPGA will raise interrupts to communicate with the CPU. The interrupt vector for each link will be set by the CPU at boot time by an initialisation routine. The register-status word will be set by the FPGA before raising the interrupt. The interrupt handler will read this word. Depending on the bits set, several tasks will be informed (by flushing a corresponding semaphore) that they has to handle new data. The FPGA will clear the register-status word automatically after it was read.

All five access forms are equal for the FPGA. Just the priority is decreasing with the register address, i.e. if more than one registers are written while the FPGA is busy, the next transmission will be the first in the sequence "Set-PS-ref.-current", "write-word", "read-word", "write-waveform", "read-waveform". The repeating due to transmission errors will be handled like new requests in respect to the priorities of the register. I.e. a set-PS-current access will delay the

The PS-controller has one waveform-download procedure for all types of waveforms. Only one waveform can be downloaded to the controller at a time. For every download the write-waveform task will do several steps:

- 1) send a "0" to the *data-counter* channel-address.
- 2) send the block-length to the *block-data* channel address.
- 3) send the block-identifier to the *block-data* channel address.
- 4) send the waveform data, one word after another, to the *block-data* channel address.
- 5) read the *data-counter* channel-address and compare it to the expected data length.
- 6) write the block-identifier to the *copy-data* channel address.

After step 6 the DSP compares block-length and block-identifier written to the *data-channel* with the *data-counter* channel and the block-identifier written to the *copy-data* channel. If both are identical, the data will be copied to the destination given by the block-identifier. If not the *copy-data* channel address will be written in the refused-commands buffer (see also Reference 1.)

The addresses for '*data-counter*', '*block-data*' and '*copy-data*' will be the same for all waveform-downloads. In the case of a reference-current-waveform download the new waveform will be activated with an extra *toggle* channel. The new ramp will be active after a "1" is send to this channel-address, but only if the old ramp is not still running. In the case it is running the new ramp will activated immediately after the old ramp has finished. Therefore "activated" means, that the ramp will be used with the next trigger signal.

The waveform will be written from the EPICS process database to an buffer in the RAM of the CPU card. The write-waveform-task write this buffer down to the write waveform register, four data bytes of data per interrupt. A new interrupt will be raised when a data word is successfully written to the power supply controller by the FPGA or when the third try fails, identical to the write word access. Bit 3 in the register-status word is used for this access. As long as one waveform is in the process, no other waveform could be written.

The write-waveform-task will read the waveform *data-counter* from the PS-controller after writing the complete waveform. The ref_current_waveform will not be toggled to the new ramp if the number does not match the length of the written data. Instead the written data will be cleared by writing a "0" to the *data-counter* channel-address.

3.6 Read-waveform access

The read-waveform access would be similar to write-waveform access. It is yet not clear if any read-waveform access will be supported by the PS-controller.

3.7 FPGA Status Register

The FPGA status register is for debugging purposes and reflects the error status of the FPGA. The functionality of this register, as defined in reference 2, is listed in the tables 4 and 5.

Table 4: Write to FPGA status register

Word	Bit	Functionality	meaning of '1'	meaning of '0'
high	15	Error-counter	clear	don't care
	1...14	none		
	0	loopback mode	on	off
mid	0...15	none		
low	0...15	none		



Memorandum

Refiled 1999

Date: March 31, 1999

From: Th. Schilcher / F. Jenni
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 felix.jenni@psi.ch

To: A. Wrulich, L. Rivkin, S. Hunt
 cc: H.U. Boksberger, G. Irminger, I. Jirousek,
 T. Korhonen

Data-Link Control System (EPICS VME crate) - Power Supply Controller

With this memo the link and data structure for the communication between the EPICS VME crate and the power supply controller are defined. The presented structure reduces the time critical load on the DSP drastically, giving it more time for its control task. A part of the software expenses for the communication is shifted from the DSP to the VME crate. Therefore, the device driver becomes more sophisticated, simple memory mapping is no more possible.

The functionality of the driver software will be independent of this hardware specifications. They will be defined in a second stage.

Hardware

The communication works with two optical links as was agreed before, one for each direction:

- Transmitter: HFBR-1528
- Receiver: HFBR-2528
- Optical fiber: HFBR-RUD055
- Optical connectors: HFBR-4506

Block, word, byte and bit pattern

The communication is always organised in identical blocks as shown in the figure. Each block starts with a 'preamble', followed by 8 bits, the 'address byte'. Following are 32 bit data transmitted in four bytes. The length of a block with preamble, start, parity and stop bits is 67 bits.

In all cases bytes have to be transmitted atomic (to improve the quality of the error detection.)

Preamble: The preamble identifies the begin of a new block. Its data corresponds with the data in the idle state of the transmission. The preamble is a 'high' signal for the duration of 12 bits or longer.

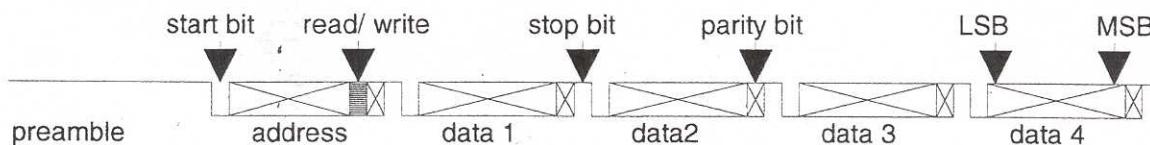
Address byte: The last bit transmitted, the MSB of the address byte, determines whether the whole cycle is a write or read cycle. MSB=1: write; MSB=0: read. The address of the data is specified by the remaining 7 bits which allows the addressing of 127 read and write channels ('registers').

Data word: Every data word consists of four times 8 bit, i.e. 4 bytes. In a read request the content of these 4 bytes will be neglected (in the present).

Start, stop and parity bits: The sequence in each byte is a start bit (logical 0), LSB...MSB, a parity bit (odd parity) and it ends with a stop bit. It is the common structure of the recommended standards.

Bit pattern of a full block:

(logical 1)



Data rate

The nominal baud rate (frequency of the single bits) on both links shall be 5MHz with a precision of 10^{-3} . Two more baud rates: 10 MHz and 115.2 kHz shall be implemented as options.

Loop back, auto echo

Written data are echoed by the receiver byte by byte with start, parity and stop bits (not bit by bit!). This allows the sender to perform a check of the correct transmission.

A read request is not echoed. It is answered by the address of the requested data with the MSB=0 and the data itself. The writing of the answer can already begin while the transmission of the read request is still in progress (data bytes of the read request are not used, but checked!).

Every write or read cycle has to be terminated before starting a new one.

Data check, error detection

Every byte has to be checked with the parity bit. A detected parity error leads to abortion of the whole data by the receiver. After detecting a parity error the receiver will send a start bit only to the sender. After that the link goes to the idle state for at least 12 bits, respectively until it receives a new preamble. This sequence can be detected as a parity error together with a block end.

Data high for more than the length of the preamble (12 bits) within a block are interpreted as the begin of a new block. The incomplete block is discarded.

Data low for more than 30 bits are interpreted as a break of the link. In this case data has to be set low on the other link too: master and slave know that the link is down.

An additional check can be done by the sender with the echoed data. Data sent after a read request can be verified with the parity check. This leads to a high reliability of the link.

Master slave structure

Though the communication has to be identical for both directions the EPICS VME crate shall be the master of the communication in the present.

Yours sincerely,

Thomas Schilcher

Felix Jenni

Completion / comments to the memorandum to A. Wrulich, L. Rivkin, S. Hunt
from February 10 by Th. Schilcher and F. Jenni:
"Data-Link Control System (EPICS VME crate) - Power Supply Controller"

Following the discussions, completions and clarifications to the above memo are made:

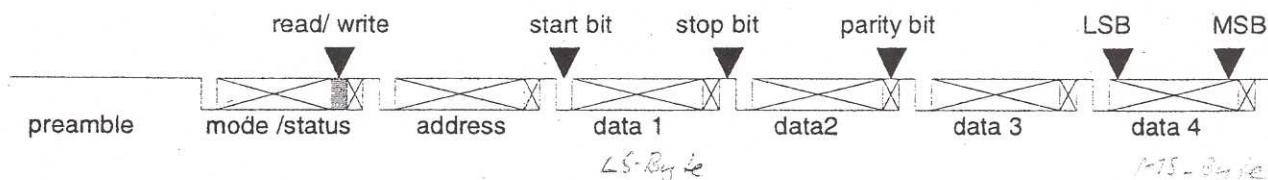
1. To avoid distortions at high baud rates, caused by dc components in the signal, differential biphase level (manchester encoding) is applied at the 5 MHz baud rate. (On the power supply this differential biphase level can be activated for every baud rate).
2. No signal on a link for more than 30 bits is interpreted as a break of the link. If this case is detected it is communicated to the other side with an error bit in the mode/status byte. In this case the slave writes to the master without being asked. The remaining 5 bytes will send back address and content of a memory location. This memory location will be defined in system parameter.
Periodisch

3. The data block is extended by an additional status / mode byte, preceding the address byte. The 8 bits are used as follows:

bit 7: 0: read cycle;	1: write cycle; (as it was defined for the MSB of the address byte)
bit 6: 0: write cycle / read request;	1: write-echo / send of requested data.
bit 5: 0: input buffer not full;	1: input buffer full (as an echo of a not accepted data write)
bit 4: 0: DSP running;	1: DSP stopped
bit 3: 0: PS controlled by the control system; 1: PS controlled local (RS232-port)	
bit 2: 0: link ok;	1: link down"
bit 1: spare	
bit 0: spare	"

4. The former read/ write bit in the address-byte is used as additional address bit.

The mode/status byte and the address byte together are treated as a 16 bit address on the power supply. With a 'mask-word' (hardware parameter) the bits used for the communication can be masked out. Therefore, the address space can be extended.



- In case of an error, three attempts to correct it shall be made.
- The number of reception errors are stored in a memory location. This location can be read and written via the link.
- After a reset, the input buffer is set to zero.

Opto-Link „EPICS VME – Power suply“ 5 Mhz, Manchester code, IEEE 802.3 – Decoder (30.3.99;I.J)

1.) Synchronisation:

Nach PowerOn sendet „VME“ Preamble „1“ so, dass nach empfangenen 12 „1“ mit der Data-Transmission begonnen werden kann d.h., „Bypass“ für Preamble in „power suply“ sonst link „dunkel“.

Error-Status: - No Sync: keine Preamble empfangen (Link „dunkel“)

- No Message Sync.: weniger als 12 „1“ zwischen Messagen („0“-Detektion)

- No Byte Sync.: mehr/weniger bits im Byte

2.) Byte : Start b., 8 Data, (Par.b.), 1Stop b. -> 11 Bits \Rightarrow 2,2 us

3.) Message: min 12 „1“ – Preamble b., (Function B.), Address B., 4 Data B., CRC B., min 12 „1“ – Preamble b. (2,4 us) + (2,2us) + (2,2us) + (8,8us) + (2,2us) + (2,4us) \Rightarrow 19,2us

15,4us

-- Setpoint WR 10 KHz, d.h. je 100us

-- RDs' mit höchste Frequenz möglich ??

-- Command WR ??

-- Timeout für Reply (2us vorgeschlagen ?, wann wird der „Message Check“ gemacht ?)

Error-Status:

-- oben beschriebene Synchronisations Error (No Sync., No Message Sync., No Byte Sync.)

-- Parity Error

-- Message Error (mehr/wenig Byte in der Message)

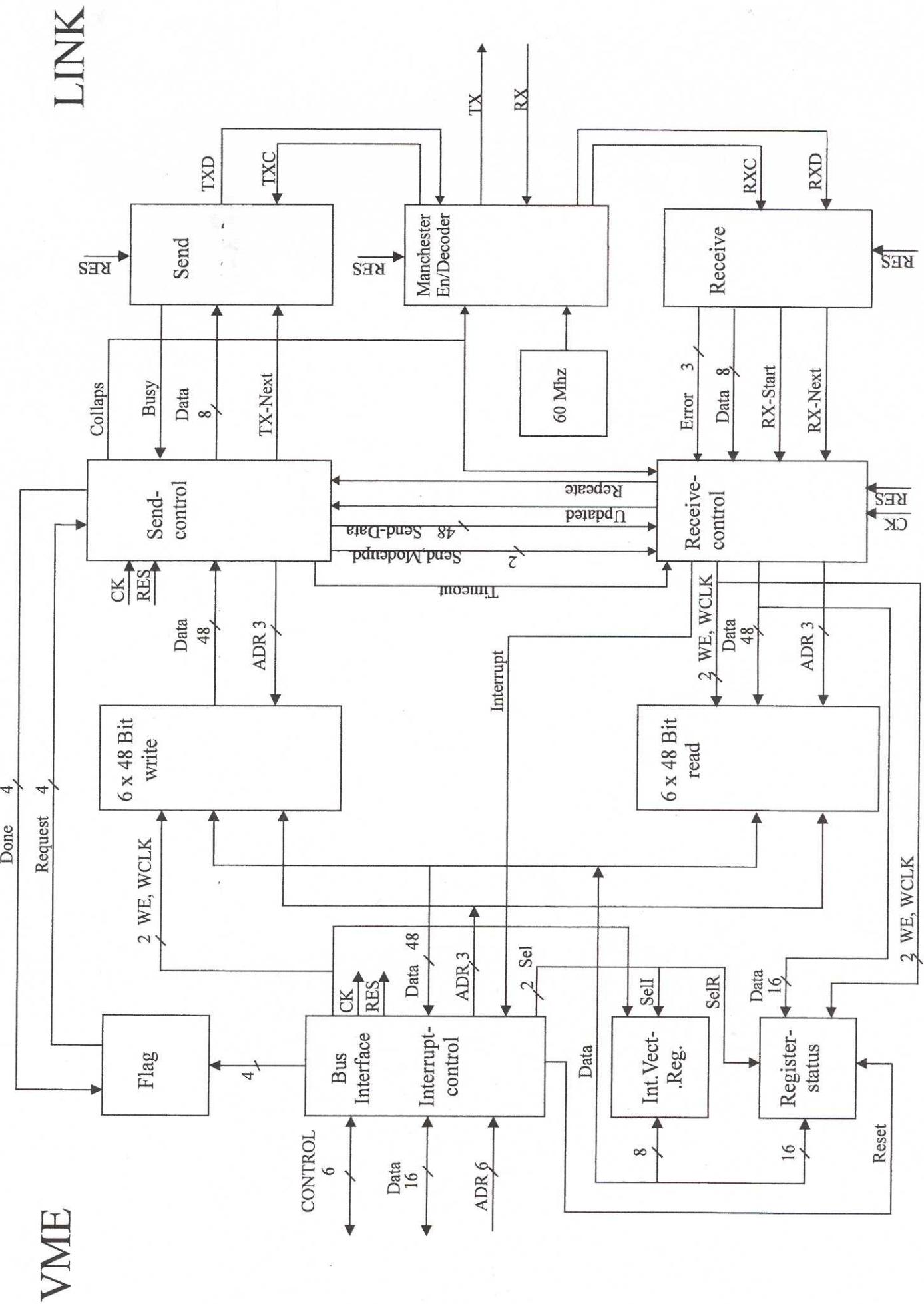
-- etc..

Die Fehlerhafte Messagen werden ignoriert (P.S.Controller) und und Error in Reply – Message zurück gemeldet:

Positive/negative acnowledge-Bit im Funktion-Byte mit Deteildiagnose im Data-Byte (s'), Address-Byte wird kopiert.

So können die „Fehlerhafte- Messages“ **unmittelbar** wiederholt werden (WRds' ?, max.3 mall)

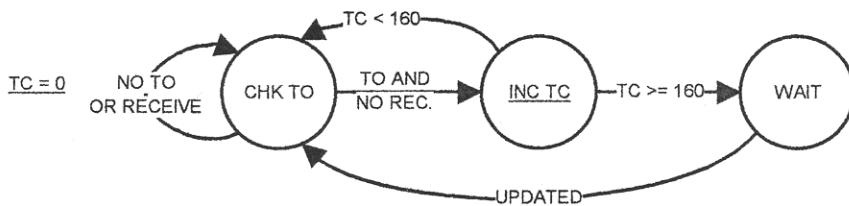
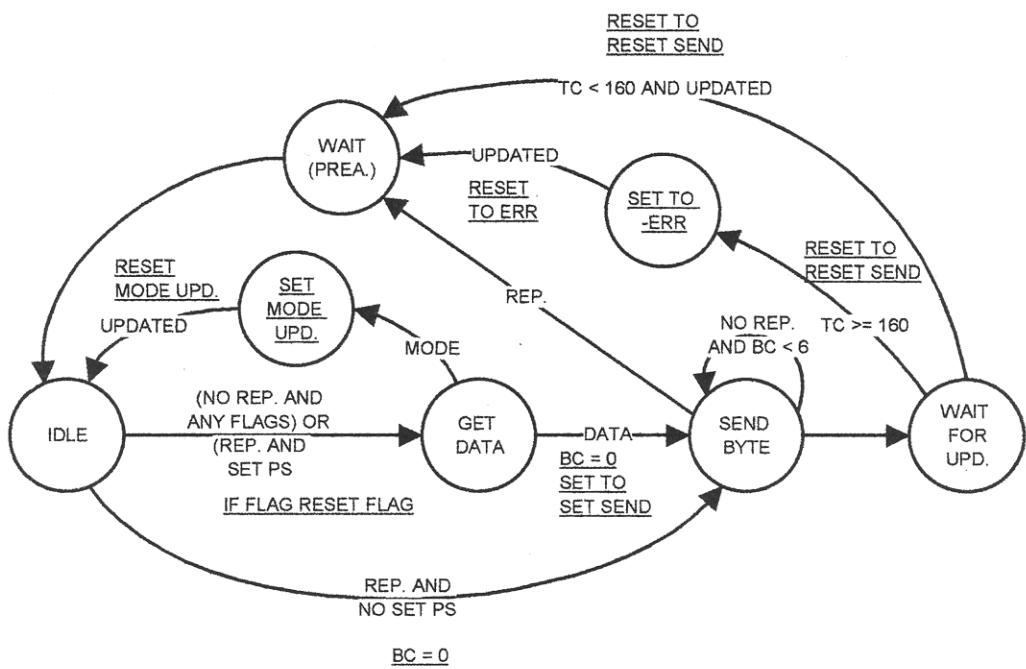
SLS Point to Point Link Industry Pack Blockschema 0.3.00 JG85



SLS Point to Point Link

SEND State Transition Diagramm

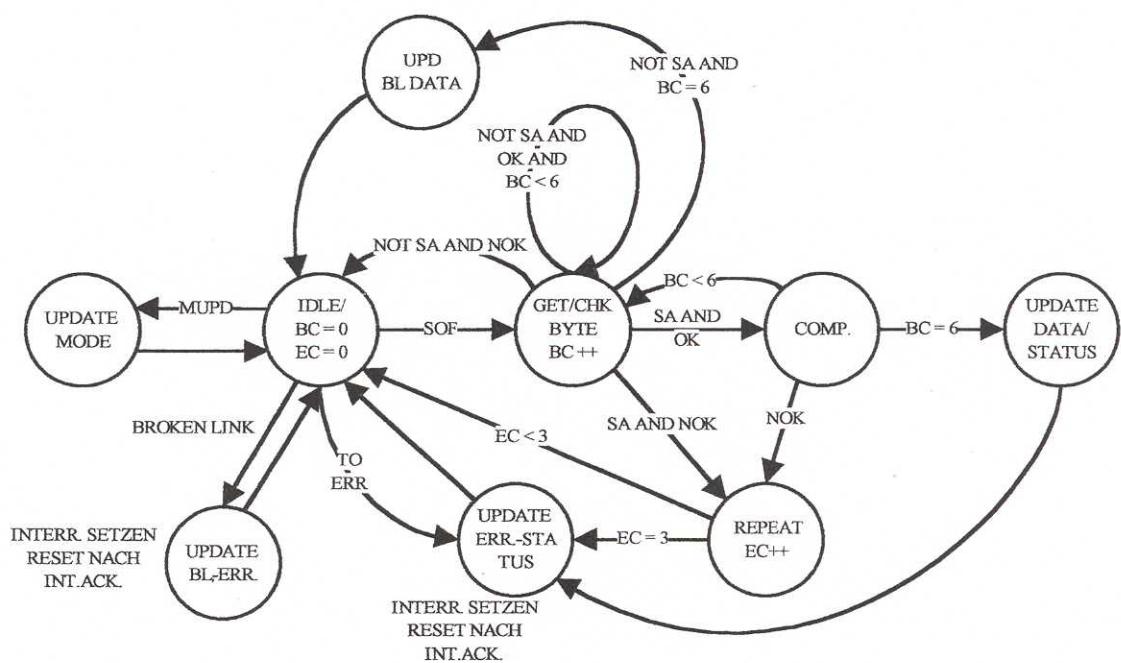
BC = BYTCOUNT TO = TIMEOUT TC = TIMER COUNTER REP = REPEAT CLOCK = 8 MHZ



SLS Point to Point Link

RECEIVE State Transition Diagramm

SOF = START OF FRAME **BC** = BYTECOUNT **EC** = ERRORCOUNT **BL** = BROKEN LINK ERROR **MUPD** = MODE UPDATE VON VME
SA = SEND AKTIV CLOCK = 8 MHZ

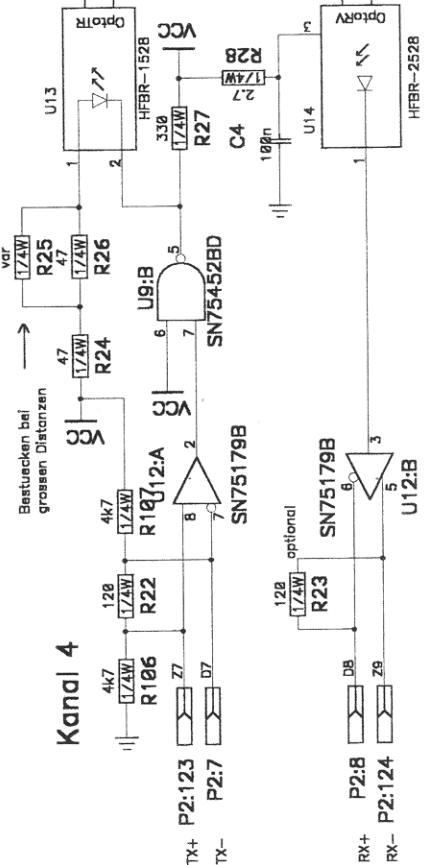
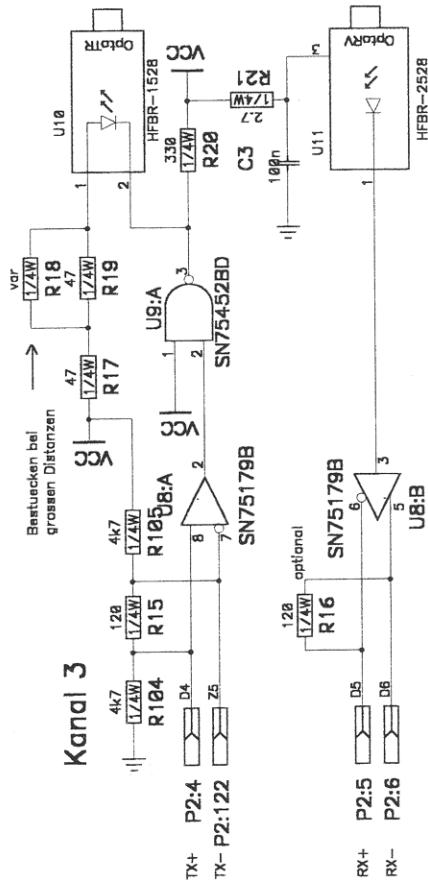
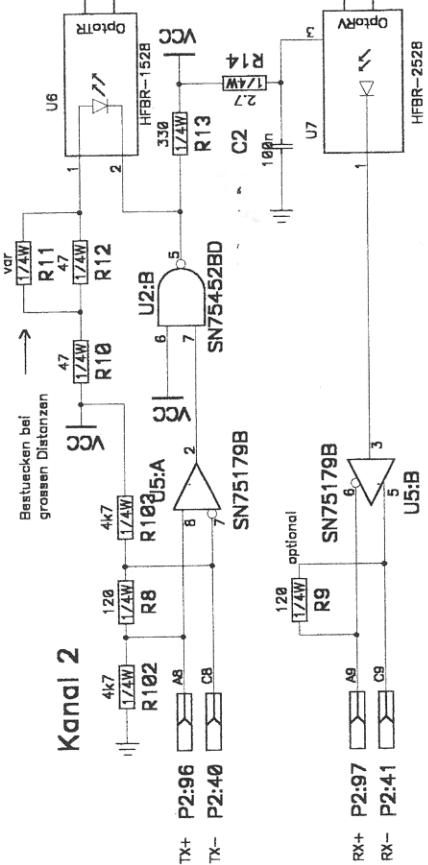
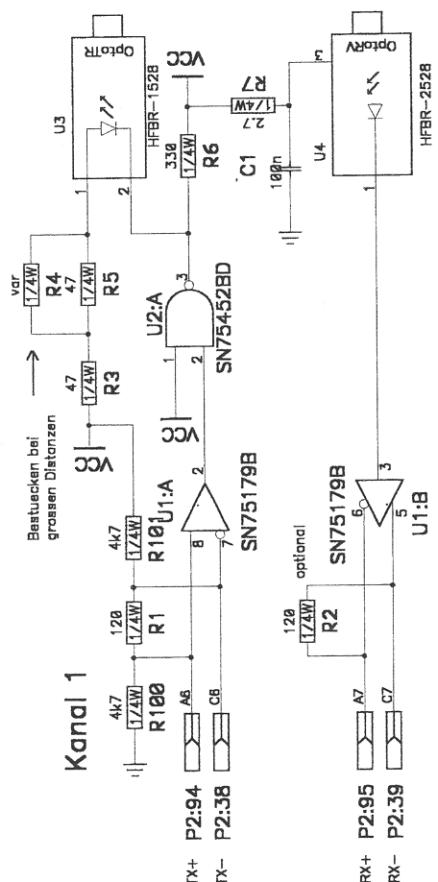


A

B

C

D



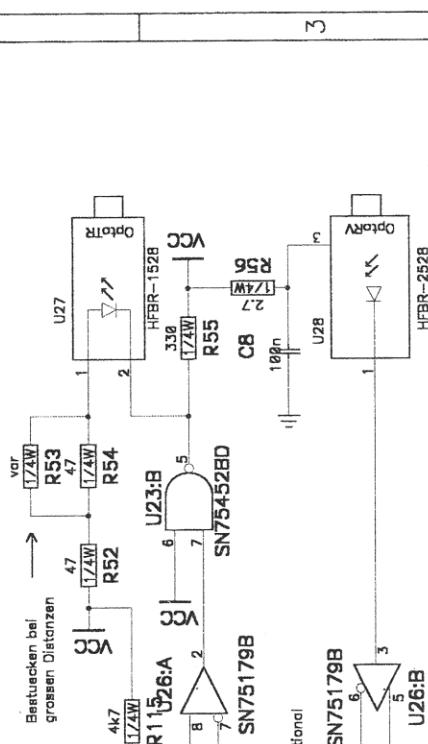
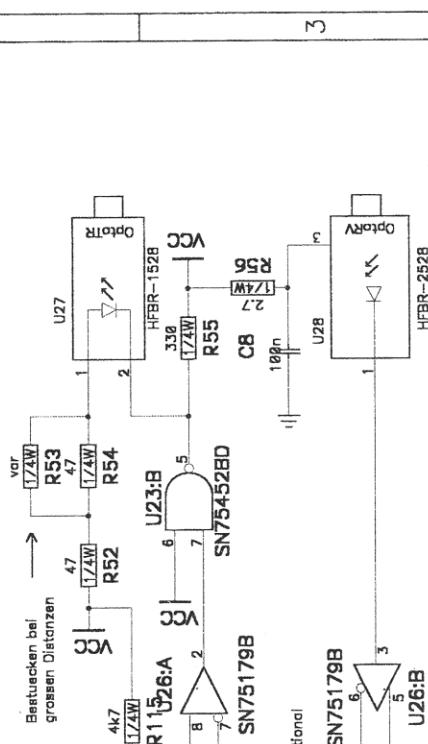
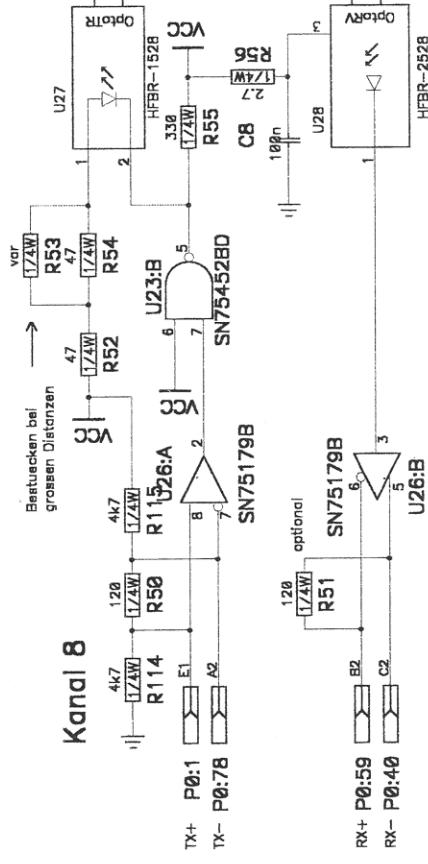
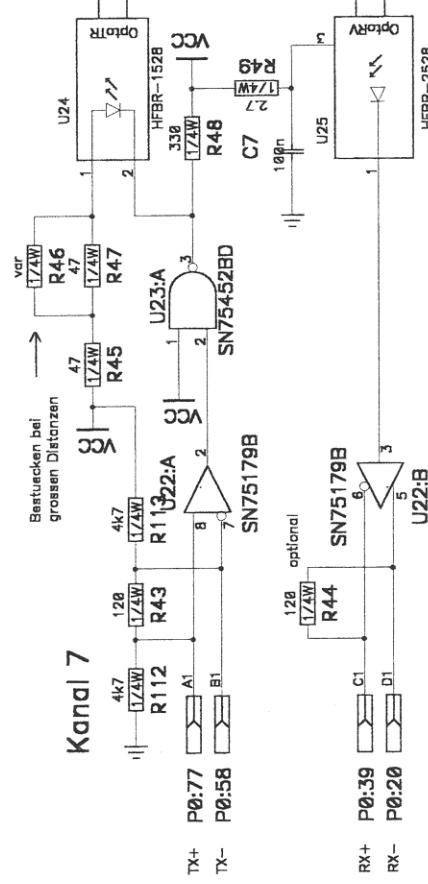
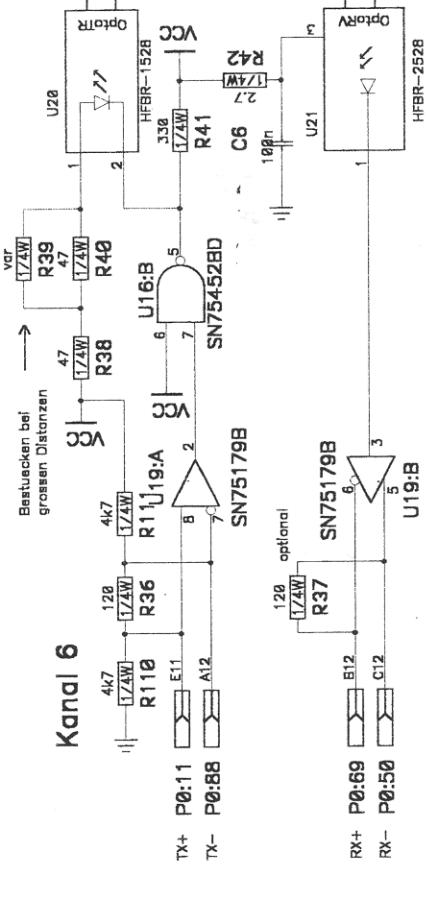
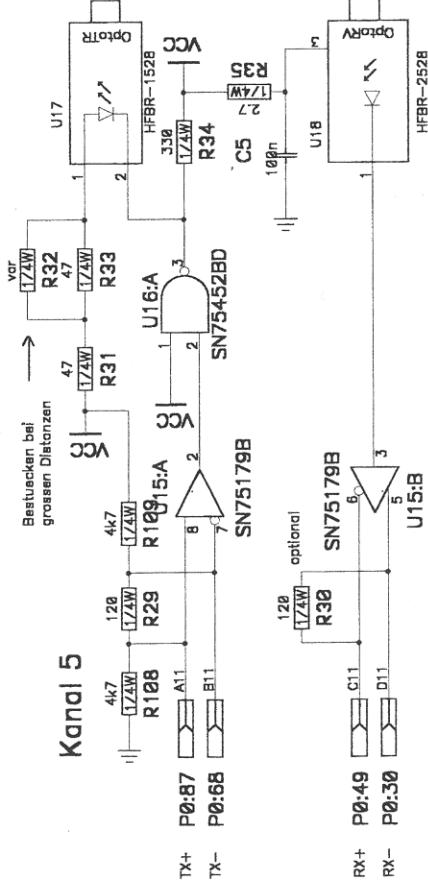
PSC - TM		SLS Point to Point Link	
	PSI System-Hilfe 8582 Steier- und Kärntentele 5122 Leoben/TG	Kanal 1 - 4	Rev 2.0
Date 07.01.00 Filename pac-trnisch	Drawn by G.Janser Sheet 2 of 3	D	

A

B

C

D



PSC-TM	SLS Point to Point Link	Rev
FuS Sonderrechnung Ressort und Kontrollbericht S21-Variante	Kanal 5 - 8	2.0
Date 07.01.00 Filename pac-tm.sch	Drawn by G.Janssen	Sheet 3 of 3

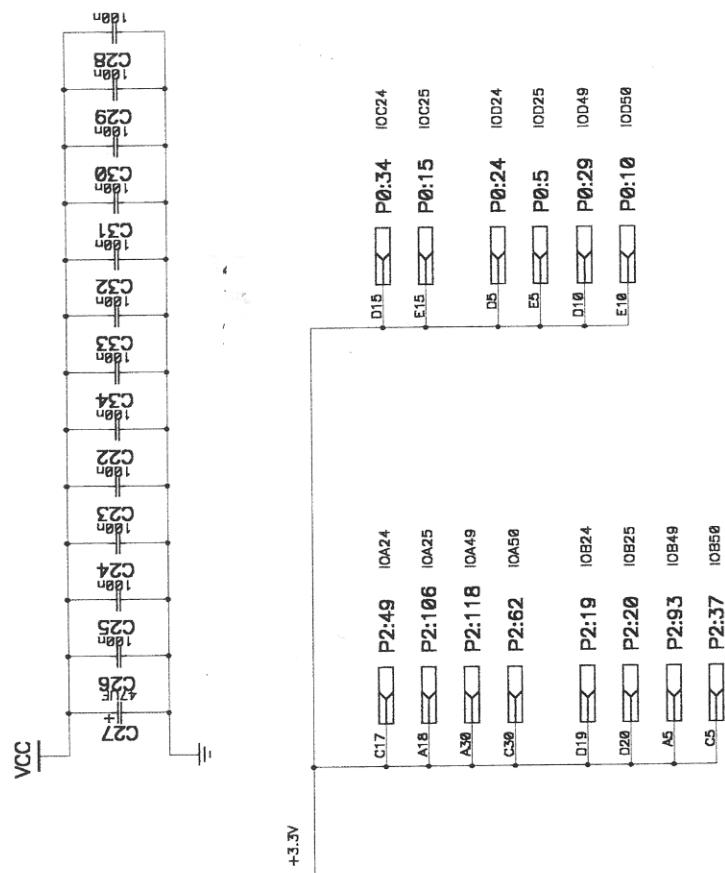
A

C

B

D

Power Table			
Ref	Des	Device(Type)	Packag e
P0	VME_P0_TRANS_PRVME_P0_PRESS	VCC	GND
		F1,F2,F3,F4,F5,F6,F7, F8,F9,F10,F11,F12, F13,F14,F15,F16,F17, F18,F19	
P2	EURO160F_TRANS	EURO160F	B2,B1,B3,B31,B32,A12 Z6,Z5,Z16,Z12,Z14, Z16,Z18,Z20,Z22,Z24, Z26,Z28,Z30,Z32
U1	SN75179B	S08	4
U2	SN75452BD	S08	4
U3	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U4	HFBR-152B	HFBR-152B/252B/2.4.5.6	
U5	SN75179B	S08	4
U6	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U7	HFBR-252B	S08	4
U8	SN75179B	S08	4
U9	SN75452BD	S08	4
U10	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U11	HFBR-252B	HFBR-152B/252B/2.4.5.6	
U12	SN75179B	S08	4
U13	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U14	HFBR-252B	HFBR-152B/252B/2.4.5.6	
U15	SN75179B	S08	4
U16	SN75452BD	S08	4
U17	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U18	HFBR-252B	HFBR-152B/252B/2.4.5.6	
U19	SN75179B	S08	4
U20	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U21	HFBR-252B	HFBR-152B/252B/2.4.5.6	
U22	SN75179B	S08	4
U23	SN75452BD	S08	4
U24	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U25	HFBR-252B	HFBR-152B/252B/2.4.5.6	
U26	SN75179B	S08	4
U27	HFBR-152B	HFBR-152B/252B/3.4.5.6	
U28	HFBR-252B	HFBR-152B/252B/2.4.5.6	



3

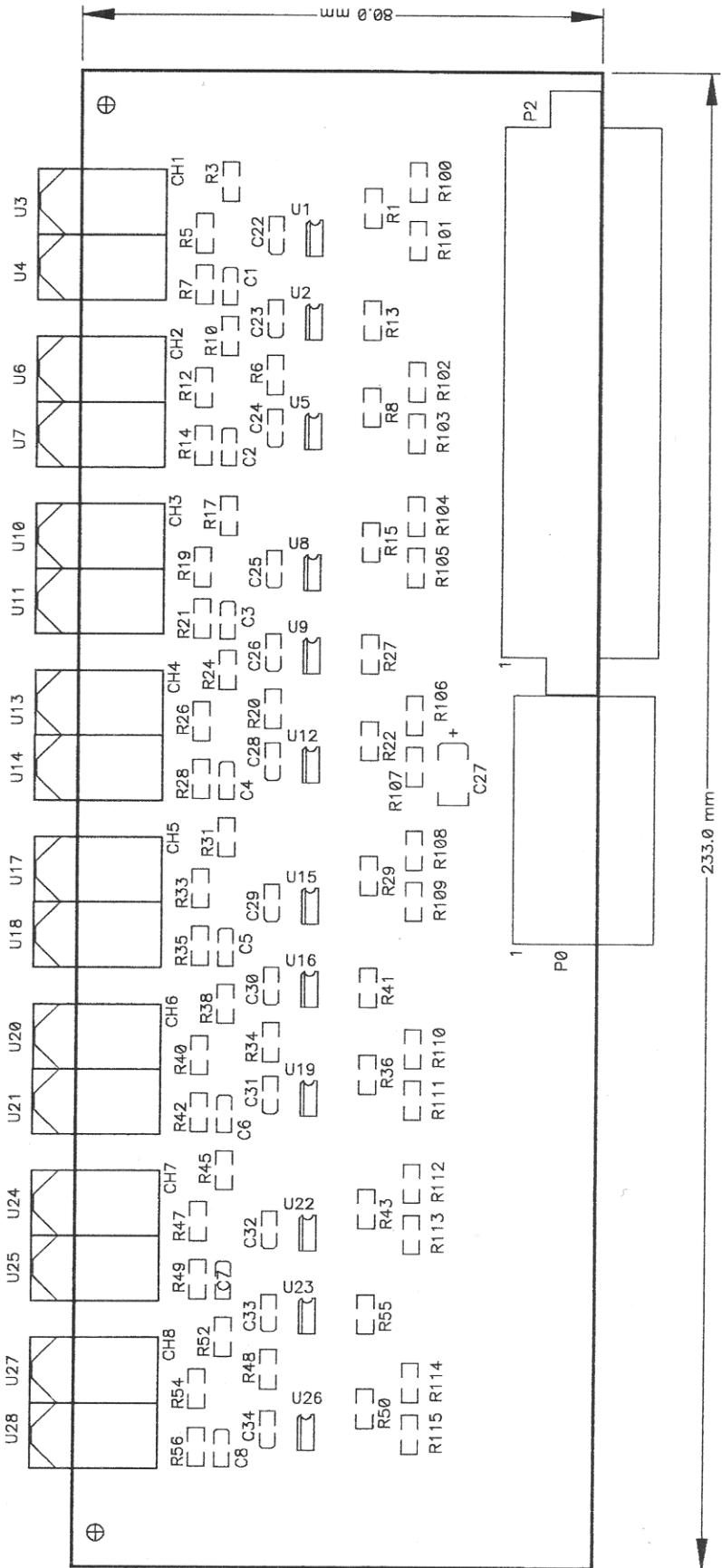
2

1

4

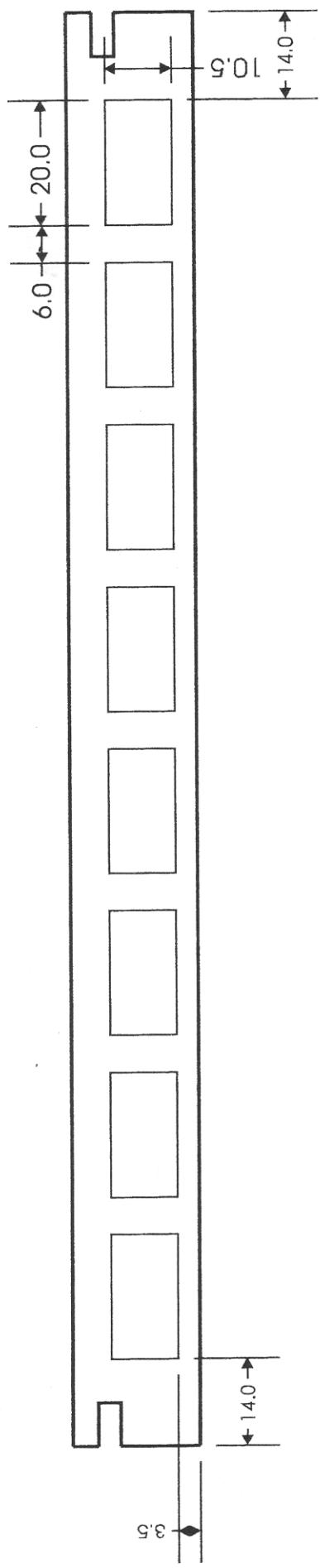
PSC-TM		SLS Point to Point Link	
 FSE Software System- und Komponenten S22-19793		Speisung	Rev 2.0
		Drawn by G.Janssen	
		Sheet 3 of 3	
		D	

PSC-TM TOPSILK
14.01.00
PSI G.Janssen 5232 Villigen PSI Tel 056 310 34 10

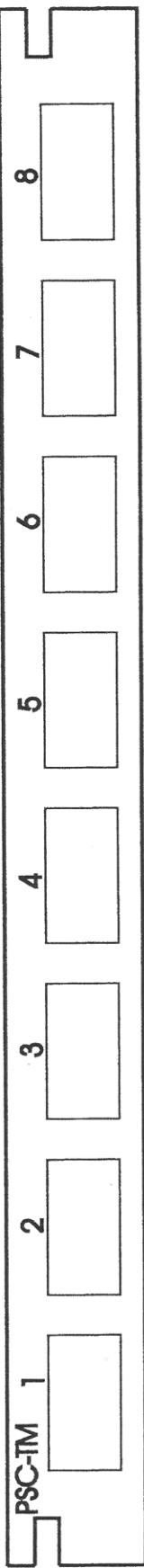


PSC-TM Frontplatte 4.2.00 JG85

Ansicht von vorne, 8 Aussparungen, Radius 1.5 In den Ecken



Beschriftung



Anzahl	Komponent	RefDes	Wert/Nr.	Leistung	Dimension	Lieferant
20	Kondensator	C1	100n		3.2 X 1.6	ELFAB
	Kondensator	C2	100n			
	Kondensator	C3	100n			
	Kondensator	C4	100n			
	Kondensator	C5	100n			
	Kondensator	C6	100n			
	Kondensator	C7	100n			
	Kondensator	C8	100n			
	Kondensator	C22	100n			
	Kondensator	C23	100n			
	Kondensator	C24	100n			
	Kondensator	C25	100n			
	Kondensator	C26	100n			
	Kondensator	C28	100n			
	Kondensator	C29	100n			
	Kondensator	C30	100n			
	Kondensator	C31	100n			
	Kondensator	C32	100n			
	Kondensator	C33	100n			
	Kondensator	C34	100n			
1	Tantal-Elko	C27	47UF		42.190.0470	PSI
8	Widerstand	R7	2.7	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R14	2.7	1/4W		
	Widerstand	R21	2.7	1/4W		
	Widerstand	R28	2.7	1/4W		
	Widerstand	R35	2.7	1/4W		
	Widerstand	R42	2.7	1/4W		
	Widerstand	R49	2.7	1/4W		
	Widerstand	R56	2.7	1/4W		
16	Widerstand	R100	4k7	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R101	4k7	1/4W		
	Widerstand	R102	4k7	1/4W		
	Widerstand	R103	4k7	1/4W		
	Widerstand	R104	4k7	1/4W		
	Widerstand	R105	4k7	1/4W		
	Widerstand	R106	4k7	1/4W		
	Widerstand	R107	4k7	1/4W		
	Widerstand	R108	4k7	1/4W		
	Widerstand	R109	4k7	1/4W		
	Widerstand	R110	4k7	1/4W		
	Widerstand	R111	4k7	1/4W		
	Widerstand	R112	4k7	1/4W		
	Widerstand	R113	4k7	1/4W		
	Widerstand	R114	4k7	1/4W		
	Widerstand	R115	4k7	1/4W		

8	Widerstand	R5	39	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R12	39	1/4W		
	Widerstand	R19	39	1/4W		
	Widerstand	R26	39	1/4W		
	Widerstand	R33	39	1/4W		
	Widerstand	R40	39	1/4W		
	Widerstand	R47	39	1/4W		
	Widerstand	R54	39	1/4W		
8	Widerstand	R3	47	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R10	47	1/4W		
	Widerstand	R17	47	1/4W		
	Widerstand	R24	47	1/4W		
	Widerstand	R31	47	1/4W		
	Widerstand	R38	47	1/4W		
	Widerstand	R45	47	1/4W		
	Widerstand	R52	47	1/4W		
8	Widerstand	R1	120	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R8	120	1/4W		
	Widerstand	R15	120	1/4W		
	Widerstand	R22	120	1/4W		
	Widerstand	R29	120	1/4W		
	Widerstand	R36	120	1/4W		
	Widerstand	R43	120	1/4W		
	Widerstand	R50	120	1/4W		
8	Widerstand	R6	330	1/4W	3.2 X 1.6	ELFAB
	Widerstand	R13	330	1/4W		
	Widerstand	R20	330	1/4W		
	Widerstand	R27	330	1/4W		
	Widerstand	R34	330	1/4W		
	Widerstand	R41	330	1/4W		
	Widerstand	R48	330	1/4W		
	Widerstand	R55	330	1/4W		
1	Stecker	P2	0204.160.1101		160 polig	Harting
8	HFBR-1528	U3	Optotransmitter			Dätwyler
	HFBR-1528	U6				
	HFBR-1528	U10				
	HFBR-1528	U13				
	HFBR-1528	U17				
	HFBR-1528	U20				
	HFBR-1528	U24				
	HFBR-1528	U27				
8	HFBR-2528	U4	Optoreceiver			Dätwyler
	HFBR-2528	U7				
	HFBR-2528	U11				
	HFBR-2528	U14				
	HFBR-2528	U18				
	HFBR-2528	U21				
	HFBR-2528	U25				
	HFBR-2528	U28				

8	SN75179B	U1	IC			EBV
	SN75179B	U5				
	SN75179B	U8				
	SN75179B	U12				
	SN75179B	U15				
	SN75179B	U19				
	SN75179B	U22				
	SN75179B	U26				
4	SN75452BD	U2	IC			EBV
	SN75452BD	U9				
	SN75452BD	U16				
	SN75452BD	U23				
1	Stecker	P0	10.064.784		95 polig	Erni
1	Leiterplatte		PSC-TM			ELFAB
1	Frontplatte		3685.532			Rittal
1	Bestückung					ELFAB

Stückliste PSC-TM 17.4.00 JG85

Anzahl	Komponent	RefDes	Wert/Nr.	Leistung	Dimension	Lieferant	Preis	Total	Bestand
20	Kondensator	C1	100n		3.2 X 1.6	ELFAB	0.10	2.00	
	Kondensator	C2	100n						
	Kondensator	C3	100n						
	Kondensator	C4	100n						
	Kondensator	C5	100n						
	Kondensator	C6	100n						
	Kondensator	C7	100n						
	Kondensator	C8	100n						
	Kondensator	C22	100n						
	Kondensator	C23	100n						
	Kondensator	C24	100n						
	Kondensator	C25	100n						
	Kondensator	C26	100n						
	Kondensator	C28	100n						
	Kondensator	C29	100n						
	Kondensator	C30	100n						
	Kondensator	C31	100n						
	Kondensator	C32	100n						
	Kondensator	C33	100n						
	Kondensator	C34	100n						
1	Tantal-Elko	C27	47UF	42.190.0470	PSI		0.50	0.50	40
8	Widerstand	R7	2.7	1/4W	3.2 X 1.6	ELFAB	0.05	0.40	
	Widerstand	R14	2.7	1/4W					
	Widerstand	R21	2.7	1/4W					
	Widerstand	R28	2.7	1/4W					
	Widerstand	R35	2.7	1/4W					
	Widerstand	R42	2.7	1/4W					
	Widerstand	R49	2.7	1/4W					

	Widerstand	R56	2.7	1/4W				
16	Widerstand	R100	4k7	1/4W	3.2 X 1.6	ELFAB	0.05	0.80
	Widerstand	R101	4k7	1/4W				
	Widerstand	R102	4k7	1/4W				
	Widerstand	R103	4k7	1/4W				
	Widerstand	R104	4k7	1/4W				
	Widerstand	R105	4k7	1/4W				
	Widerstand	R106	4k7	1/4W				
	Widerstand	R107	4k7	1/4W				
	Widerstand	R108	4k7	1/4W				
	Widerstand	R109	4k7	1/4W				
	Widerstand	R110	4k7	1/4W				
	Widerstand	R111	4k7	1/4W				
	Widerstand	R112	4k7	1/4W				
	Widerstand	R113	4k7	1/4W				
	Widerstand	R114	4k7	1/4W				
	Widerstand	R115	4k7	1/4W				
8	Widerstand	R5	39	1/4W	3.2 X 1.6	ELFAB	0.05	0.40
	Widerstand	R12	39	1/4W				
	Widerstand	R19	39	1/4W				
	Widerstand	R26	39	1/4W				
	Widerstand	R33	39	1/4W				
	Widerstand	R40	39	1/4W				
	Widerstand	R47	39	1/4W				
	Widerstand	R54	39	1/4W				
8	Widerstand	R3	47	1/4W	3.2 X 1.6	ELFAB	0.05	0.40
	Widerstand	R10	47	1/4W				
	Widerstand	R17	47	1/4W				
	Widerstand	R24	47	1/4W				
	Widerstand	R31	47	1/4W				
	Widerstand	R38	47	1/4W				
	Widerstand	R45	47	1/4W				

8	Widerstand	R52	47	1/4W				
8	Widerstand	R1	120	1/4W	3.2 X 1.6	ELFAB	0.05	0.40
	Widerstand	R8	120	1/4W				
	Widerstand	R15	120	1/4W				
	Widerstand	R22	120	1/4W				
	Widerstand	R29	120	1/4W				
	Widerstand	R36	120	1/4W				
	Widerstand	R43	120	1/4W				
	Widerstand	R50	120	1/4W				
8	Widerstand	R6	330	1/4W	3.2 X 1.6	ELFAB	0.05	0.40
	Widerstand	R13	330	1/4W				
	Widerstand	R20	330	1/4W				
	Widerstand	R27	330	1/4W				
	Widerstand	R34	330	1/4W				
	Widerstand	R41	330	1/4W				
	Widerstand	R48	330	1/4W				
	Widerstand	R55	330	1/4W				
1	Stecker	P2	0204.160.1101	160 polig	Harting	39.15	39.15	70
8	HFBR-1528	U3	Optotransmitter		Dätwyler	9.35	74.80	550
	HFBR-1528	U6						
	HFBR-1528	U10						
	HFBR-1528	U13						
	HFBR-1528	U17						
	HFBR-1528	U20						
	HFBR-1528	U24						
	HFBR-1528	U27						
8	HFBR-2528	U4	Optoreceiver		Dätwyler	12.90	103.20	550
	HFBR-2528	U7						
	HFBR-2528	U11						
	HFBR-2528	U14						
	HFBR-2528	U18						
	HFBR-2528	U21						

	HFBR-2528	U25							
	HFBR-2528	U28							
8	SN75179B	U1	IC		EBV	0.50	4.00	1100	
	SN75179B	U5							
	SN75179B	U8							
	SN75179B	U12							
	SN75179B	U15							
	SN75179B	U19							
	SN75179B	U22							
	SN75179B	U26							
4	SN75452BD	U2	IC		EBV	0.35	1.40	270	
	SN75452BD	U9							
	SN75452BD	U16							
	SN75452BD	U23							
1	Stecker	P0	10.064.784	95 polig	Erni	8.21	8.21	70	
1	Leiterplatte		PSC-TM		ELFAB	52.80	52.80	2	
1	Frontplatte		3685.532		Rittal	28.41	28.41	70	
1	Bestückung				ELFAB	18.50	18.50		

Preis total

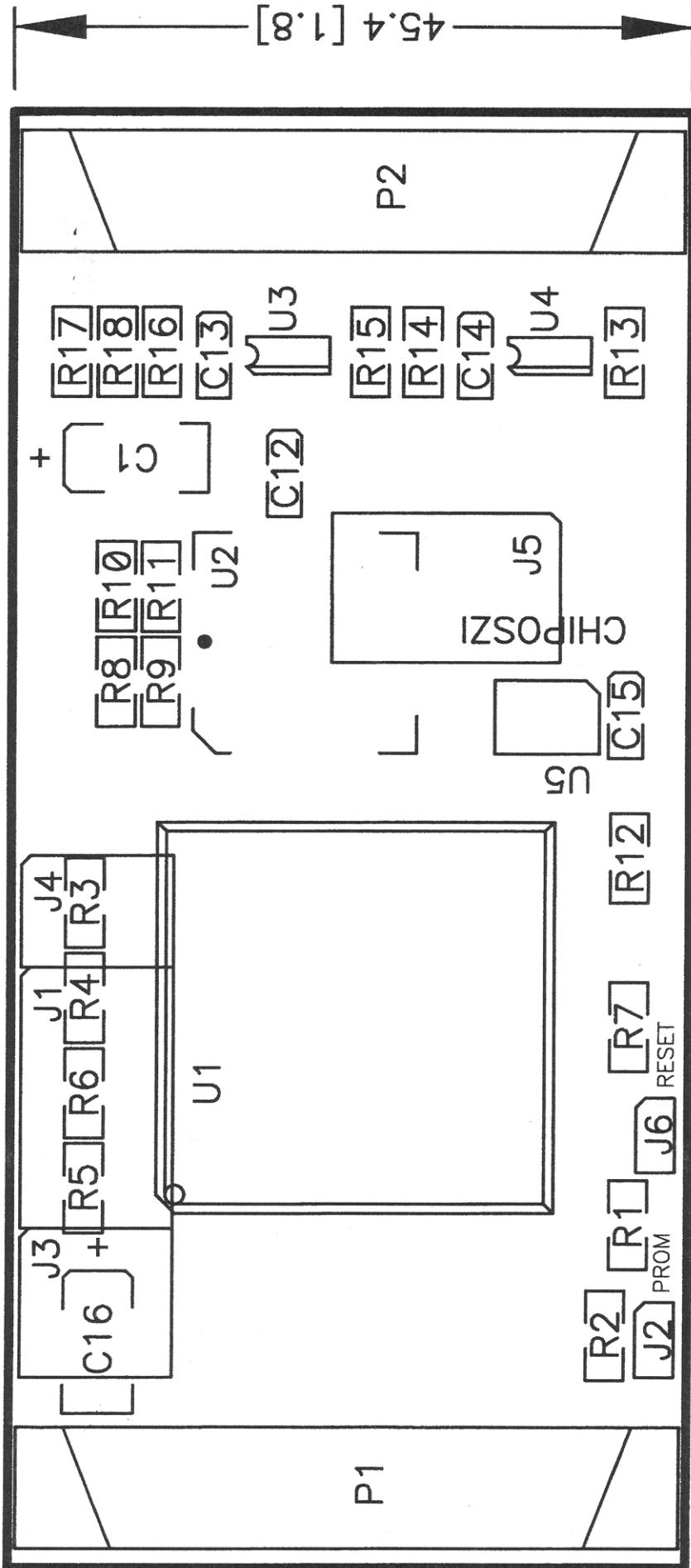
335.77

Preis pro Kanal

41.97

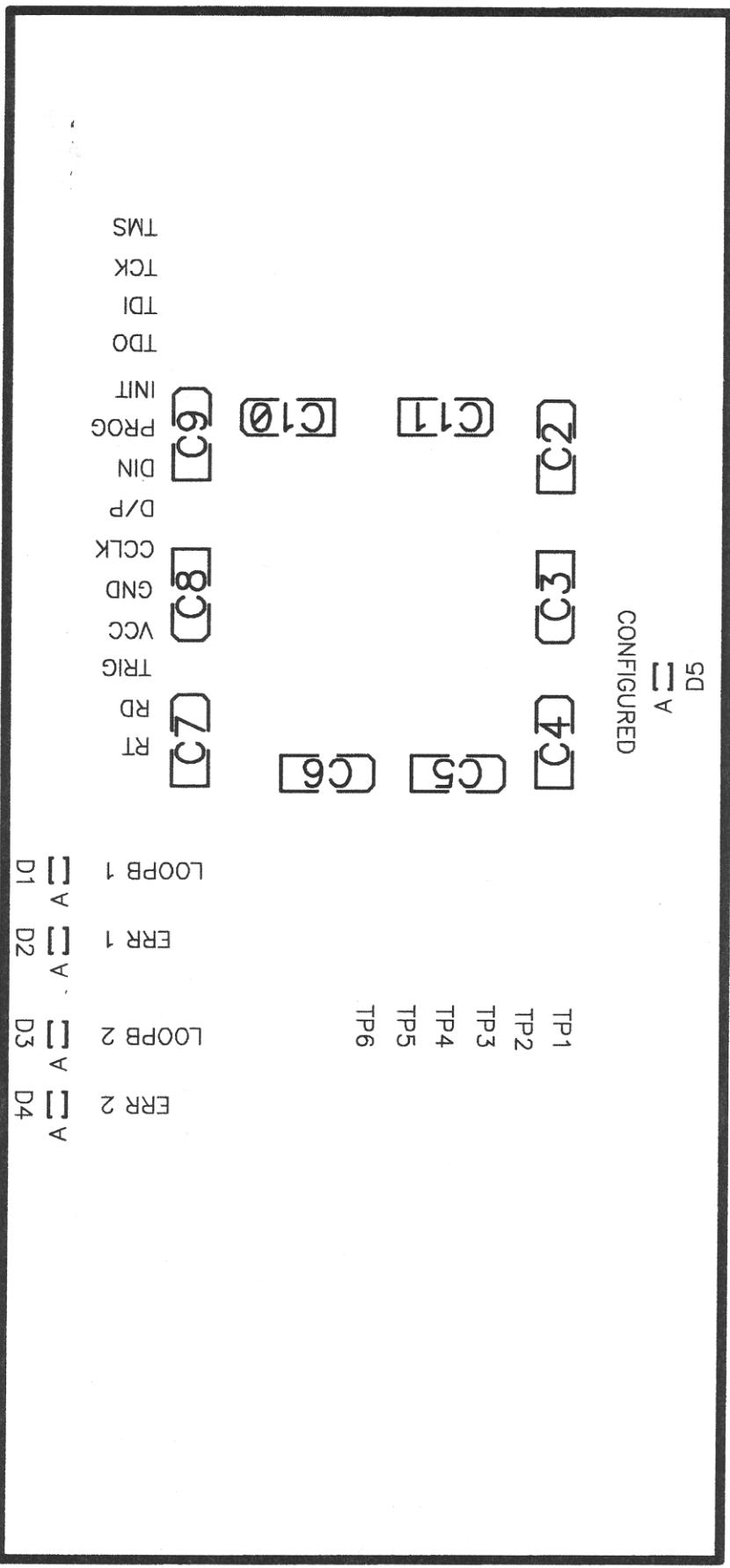
PSC-IP2 Bestueckung top

J1, J3, J4, J5, R13, R15, R18 nicht bestuecken, Pins fuer J2 und J6 6 mm vorstehend auf Best. Seite



PSC-IP2 Bestueckung bottom

[e.3] 1.66



Anzahl	Komponent	RefDes	Wert/Art.Nr.	Leistung	Dimension	Lieferant
1	AT17C512-10JC	U2	IC			Anatec
14	Kondensator	C2	100N		3.2 x 1.6	ELFAB
		C3				
		C4				
		C5				
		C6				
		C7				
		C8				
		C9				
		C10				
		C11				
		C12				
		C13				
		C14				
		C15				
2	Tantal Elko	C1	47UF		42.190.0470	PSI
		C16				
5	CHIPLED	D1	253177			Distrelec
		D2				
		D3				
		D4				
		D5				
1	Chiposzillator	U5	715151	KS5750HBE	60MHz	Quarz AG
2	Stecker	P1	333591	AMP 173279-3		Spörle
		P2				
1	Widerstand	R17	0	1/4W	3.2 x 1.6	ELFAB
6	Widerstand	R1	1K	1/4W	3.2 x 1.6	ELFAB
		R2				
		R3				
		R4				
		R5				
		R6				
1	Widerstand	R7	10K	1/4W	3.2 x 1.6	ELFAB
2	Widerstand	R14	120	1/4W	3.2 x 1.6	ELFAB
		R16				
5	Widerstand	R8	330	1/4W	3.2 x 1.6	ELFAB
		R9				
		R10				
		R11				
		R12				
1	XCS40XL-4PQ208C	U1	IC	FPGA		Memec
2	Jumper	J2	CAB4G01	F1		Astrel
		J6				
2	SN75179BD	U3	IC	SO8		EBV
		U4				

1	IC-Sockel	U2	650474	PLCC	20 Pin	Distrelec
1	Leiterplatte		VME-IP2			ELFAB
1	Bestückung					ELFAB
0.12	Stiftleiste	J2,J6	*	36 polig	44.040.0804	PSI

Stückliste PSC-IP2

17.4.00 JG85

Anzahl	Komponent	RefDes	Wert/Art.Nr.	Leistung	Dimension	Lieferant	Preis	Total	Bestand
1	AT17C512-10JC	U2		IC					
14	Kondensator	C2	100N		3.2 x 1.6	Anatec ELFAB	16.40 0.10	16.40 1.40	270
		C3							
		C4							
		C5							
		C6							
		C7							
		C8							
		C9							
		C10							
		C11							
		C12							
		C13							
		C14							
		C15							
2	Tantal Elko	C1	47UF		42.190.0470	PSI	0.50	1.00	40
		C16							
5	CHIPLED	D1	253177			Distrelec	0.50	2.50	1600
		D2							
		D3							
		D4							
		D5							
1	Chiposzillator	U5	715151	KS5750HBE	60MHz	Quarz AG	3.10	3.10	270
2	Stecker	P1	3333591	AMP 173279-3		Spörle	5.00	10.00	460
1	Widerstand	R17	0	1/4W	3.2 x 1.6	ELFAB	0.05	0.05	
6	Widerstand	R1	1K	1/4W	3.2 x 1.6	ELFAB	0.05	0.30	
		R2							

	R3								
	R4								
	R5								
	R6								
1	Widerstand	R7	10K	1/4W	3.2 x 1.6	ELFAB	0.05	0.05	
2	Widerstand	R14	120	1/4W	3.2 x 1.6	ELFAB	0.05	0.10	
		R16							
5	Widerstand	R8	330	1/4W	3.2 x 1.6	ELFAB	0.05	0.25	
		R9							
		R10							
		R11							
		R12							
1	XCS40XL-4PQ208C	U1	IC	FPGA		Memec	37.85	37.85	0
2	Jumper	J2				Astrel	0.20	0.40	
		J6							
2	SN75179BD	U3	IC	SO8		EBV	0.50	1.00	1100
		U4							
1	IC-Sockel	U2	650474	PLCC	20 Pin	Distrelec	0.80	0.80	420
1	Leiterplatte		VME-IP2			ELFAB	14.00	14.00	7
1	Bestückung					ELFAB	13.50	13.50	
0.12	Stiftleiste	J2,J6	*	36 polig	44.040.0804	PSI	5.00	0.60	0

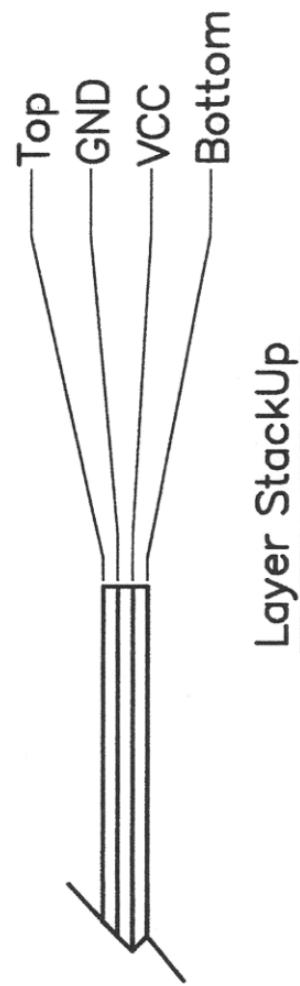
103.30

Preis pro Kanal

51.65

* 2 Pin in Jumper bis Anschlag, abschneiden -> minimale Bauhöhe

PSC-IP2 Drill Table, Layer Stackup



Drill Table

Hole Dia (mm)	Symbol	Quantity	Plated
0.457	+	124	Yes
0.864	X	126	Yes
2.540	Y	7	Yes