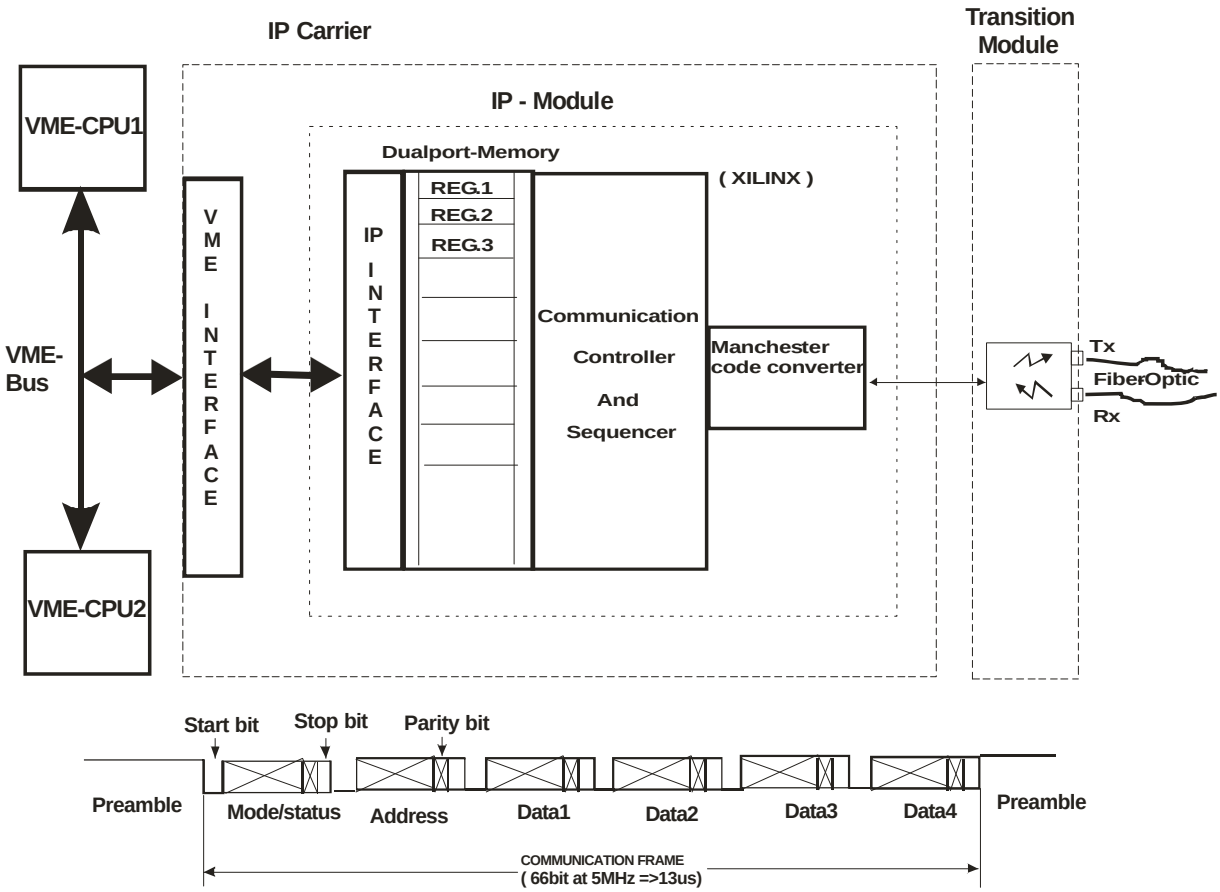
PSCIP2
Industrypack for Powersupply control



1. Overview

The PSCIP2 provides control of two Powersupplies. The VME-CPU will write in memory mapped registers of the PSCIP2 module. This causes the module to write over the optical fibre link to the power supply controller. The answer from the controller comes back across the fibre link and will be written in the corresponding read register. An interrupt will tell the CPU that new data has arrived.

2. Memory space

The links on PSCIP2 module are implemented with an FPGA. The FPGA has 64 bytes write-only memory and 64 bytes read-only memory in the VME I/O memory space. They will be memory mapped to the same VME address space. I.e. a byte-write to the base address will affect the write-register status byte and not the read register status. The read registers can only be written by the FPGA.

Table 1 shows the definition of the I/O memory-space for each link.

Table 1: IP-Module I/O memory space

		write registers		read registers	
		high byte	low byte	high byte	low byte
base+0	high priority write	Status	address	status	address
base+2	(set PS current)	data (higher word)		data (higher word)	
base+4		data (lower word)		data (lower word)	
base+8	write word	Status	address	status	address
base+10		data (higher word)		data (higher word)	
base+12		data (lower word)		data (lower word)	
base+16	read word	Status	address	status	address
base+18		data (higher word)		data (higher word)	
base+20		data (lower word)		data (lower word)	
base+24	write waveform	Status	address	status	address
base+26		data (higher word)		data (higher word)	
base+28		data (lower word)		data (lower word)	
base+32	read waveform	Status	address	status	address
base+34		data (higher word)		data (higher word)	
base+36		data (lower word)		data (lower word)	
base+40	broken transmit			status	address
base+42				data (higher word)	
base+44				data (lower word)	
base+48	FPGA Status	data (high word)		data (higher word)	
base+50		data (mid word)		data (mid word)	
base+52		data (low word)		data (low word)	
base+56	register status			data	
base+58	interrupt vector	don't care	vector		

Table 2: Status

Bit	***Functionality***	***meaning of '1'***	***meaning of '0'***
7	write / read	write cycle	read cycle
6	echo	write echo / send of requested data	write cycle / read request
5	input buffer	full	not full
4	DSP	stopped	running
3	remote / local	PS controlled local	PS contr. by the contr. system
2	link	link down	link ok
1	don’t care		
0	don’t care		

Table 3: Reading the register-status word

Bit	*reg.no.*	*Functionality*	*meaning of '1'*	*meaning of '0'*
15	-	Error flag	error	ok
5...14	-	none		
4	4	read waveform	ready	in proccess or idle
3	3	write waveform	ready	in proccess or idle
2	2	read word	ready	in proccess or idle
1	1	write word	ready	in proccess or idle
0	0	set-PS-ref.-current	ready	in proccess or idle

Table 4: IP-Module ID memory space

	Form I ID ("IPAC")				M-ID	Modul	Rev.	res.	driver ID		length	CRC
base+0x80+	0x01	0x03	0x05	0x07	0x09	0x0B	0x0D	0x0F	0x11	0x13	0x15	0x017
	0x49	0x50	0x41	0x43	0x0B	0x1B	0xA1	0x00	0x00	0x00	0x0C	0xAF

The ID memory space is defined according to the IndustryPack VITA standard. The manufacturer ID "M-ID" is choosen to be 0x0B as a development ID. The module ID is choosen to be 0x1B. The routine to calculate the CRC is according to the IndustryPack VITA standard.

The value for 'base' adds up from the base address of the carrier board, the offset for each module (0x100) and the offset of the link in the module (two links per module, offset 0x40). The offsets for the eight possible links are:
IP Module A Link 1: 0x0000, IP Module A Link 2: 0x0040, IP Module A ID: 0x0080,
IP Module B Link 3: 0x0100, IP Module B Link 4: 0x0140, IP Module B ID: 0x0180,
IP Module C Link 5: 0x0200, IP Module C Link 6: 0x0240, IP Module C ID: 0x0280,
IP Module D Link 7: 0x0300, IP Module D Link 8: 0x0340. IP Module D ID: 0x0380,

The memory is grouped in six registers of six bytes each (in the following just called "register"), a two byte register-status which is read-only from the CPU and one byte write-only for the interrupt vector. If an address is not specified in the table 1 than it has no function and is disregarded by the FPGA. For each of the registers an interrupt will be given if they are ready to be written or when new data has arrived in the read register. The register-status word determine with flag bits, which register is ready to be read or to be written into. The register-status will be updated by the FPGA before raising an interrupt. The FPGA can raise an interrupt if he detects an error with the same procedure than for the registers.
All registers have big-endian byte order i.e. the least significant bits of a word are in the byte with the higher address. This is the Byte order of the VME Bus, the byte order of the protocol of the optical fibre link is little-endian.

3. Access modes

There are five different forms of access to the power supply controller. They correspond to the first five registers of the FPGA and will be described in the following sections.
The set-PS-current, read and write rates are all limited to 10 kHz each by the power supply controller. The FPGA will take care that these rates will not be exceeded. That implies that a write to the data field of any register will not necessarily handled immediately by the FPGA.
The FPGA will react to a write in the lower word of a register data field. He will send the data together with the address to the PS controller. When he received the answer from the PS controller he check it for transmission errors. In case of an error he will repeat the sending up to three times. If it fails the

third time he will just write the return status to the status field of the corresponding register and set the error flag.
The FPGA will raise interrupts to communicate with the CPU. The interrupt vector for each link will be set by the CPU at boot time by an initialisation routine. The register-status word will be set by the FPGA before raising the interrupt. The interrupt handler will read this word. Depending on the bits set, several tasks will be informed (by flushing a corresponding semaphore) that they has to handle new data. The FPGA will clear the register-status word automatically after it was read.
All five access forms are equal for the FPGA. Just the priority is decreasing with the register address, i.e. if more than one registers are written while the FPGA is busy, the next transmission will be the first in the sequence "Set-PS-ref.-current", "write-word", "read-word", "write-waveform", "read-waveform". The repeating due to transmission errors will be handled like new requests in respect to the priorities of the register. I.e. a set-PS-current access will delay the repeating of a read or write access. The third successive transmission error will abort all pending requests at the FPGA.
In normal operation the status and address field in the set-PS-ref.-current register will be written only once with the hex 0x80 for a write access and the ref.-current channel-address of the power supply controller. The FPGA always uses the value in the Status / Address word, written last.

4. FPGA Status Register

The FPGA status register is for debugging purposes and reflects the error status of the FPGA. The functionality of this register is listed in the tables 5 and 6.

Table 5: Write to FPGA status register

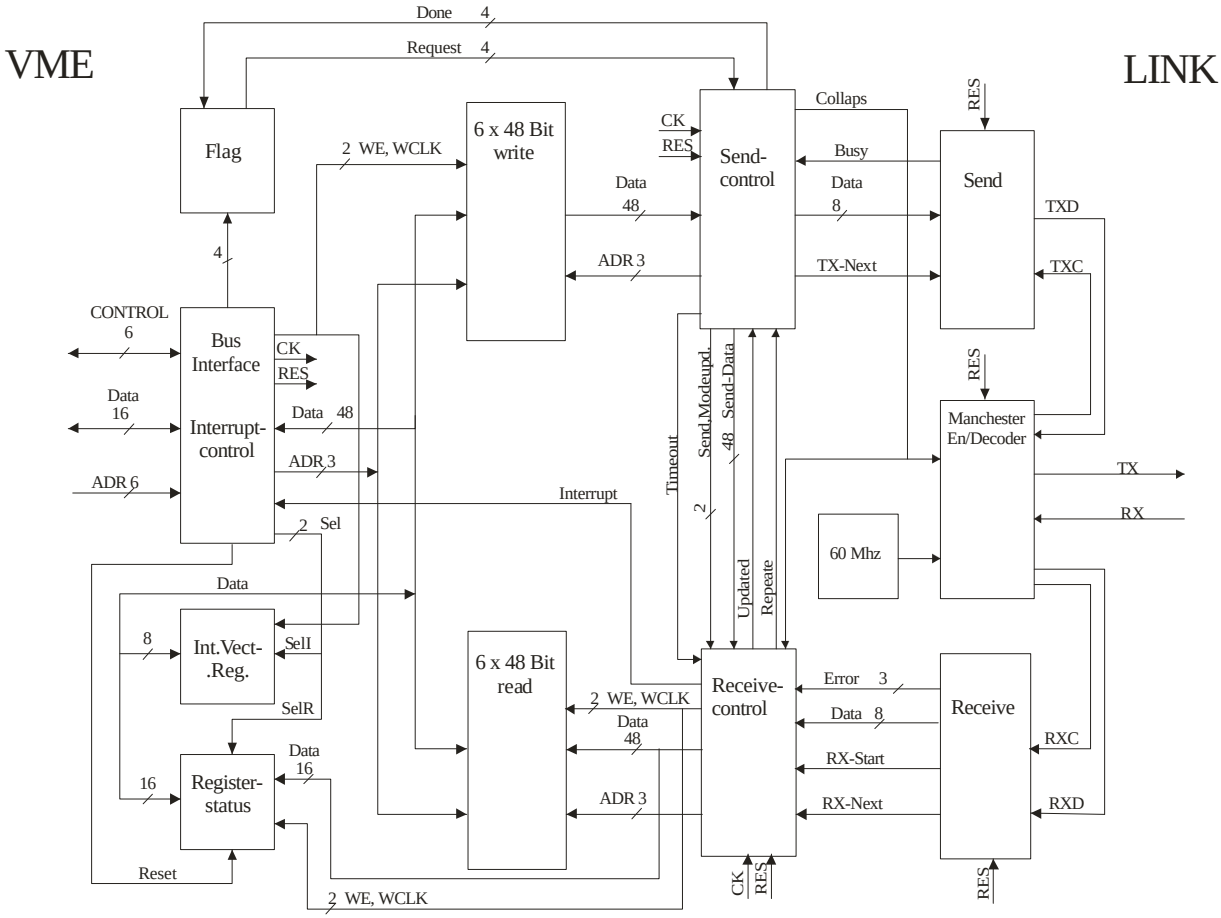
Word	***Bit***	***Functionality***	***meaning of '1'***	***meaning of '0'***
high	15	Error-counter	clear	don't care
	1...14	none		
	0	loopback mode	on	off
mid	0...15	none		
low	0...15	none		

Table 6: Read FPGA status register

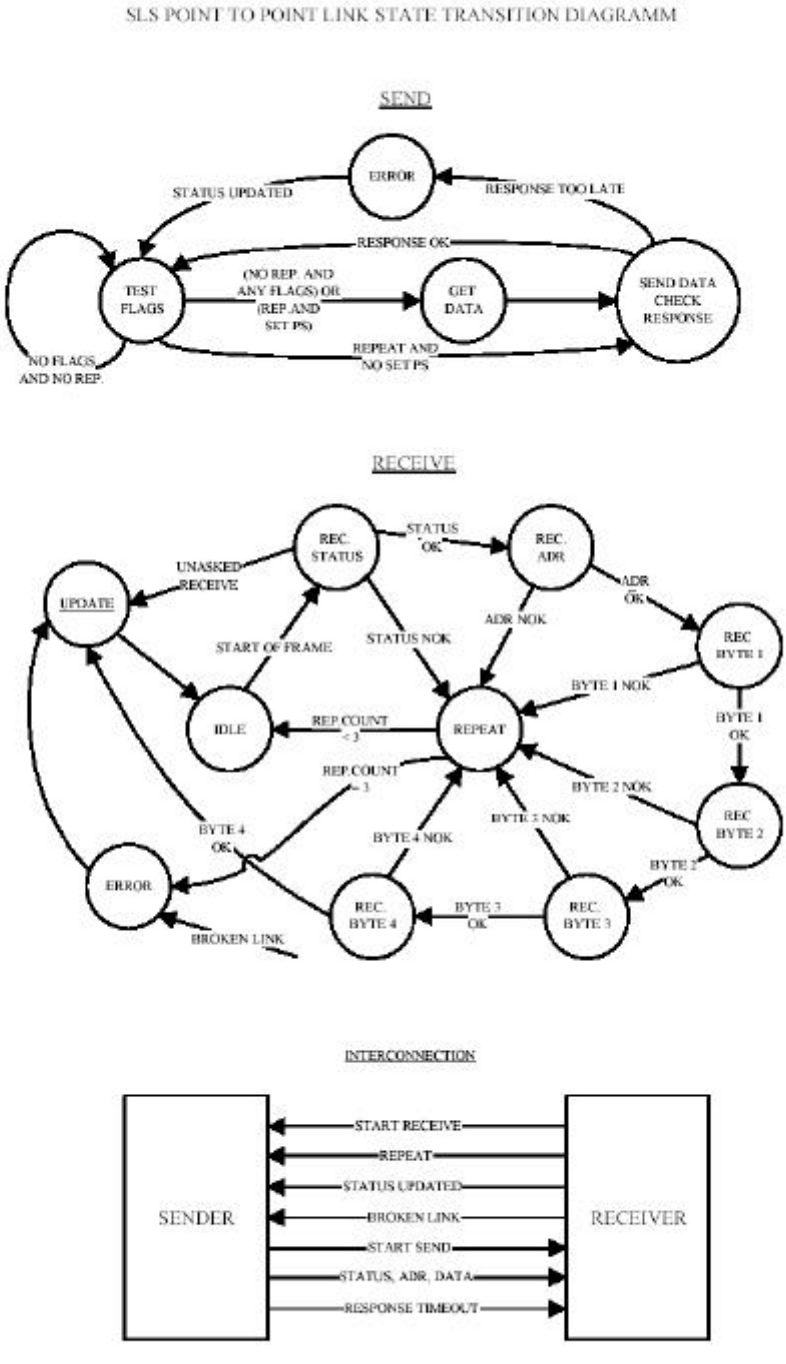
Word	***Bit***	***Functionality***	***meaning of '1'***	***meaning of '0'***
high	8...15	Error-counter	number of errors	number of errors
	7	link down	error	ok
	6	transmit error	error	ok
	1...5	none		
	0	loopback mode	on	off
mid	15	none		
	14	parity error of high priority write (reg 0)	error	ok
	13	break error of reg 0	error	ok
	12	framing error of reg 0	error	ok
	11	compare error of reg 0	error	ok
	10	timeout error of reg 0	error	ok
	5...9	like reg 0 for reg 1		
	0...4	like reg 0 for reg 2		
low	10...15	none		
	5...9	like reg 0 for reg 3		
	0...4	like reg 0 for reg 4		

5. FPGA Blockschematic

Point to Point Link Industry Pack PSCIP2 Blockschematic

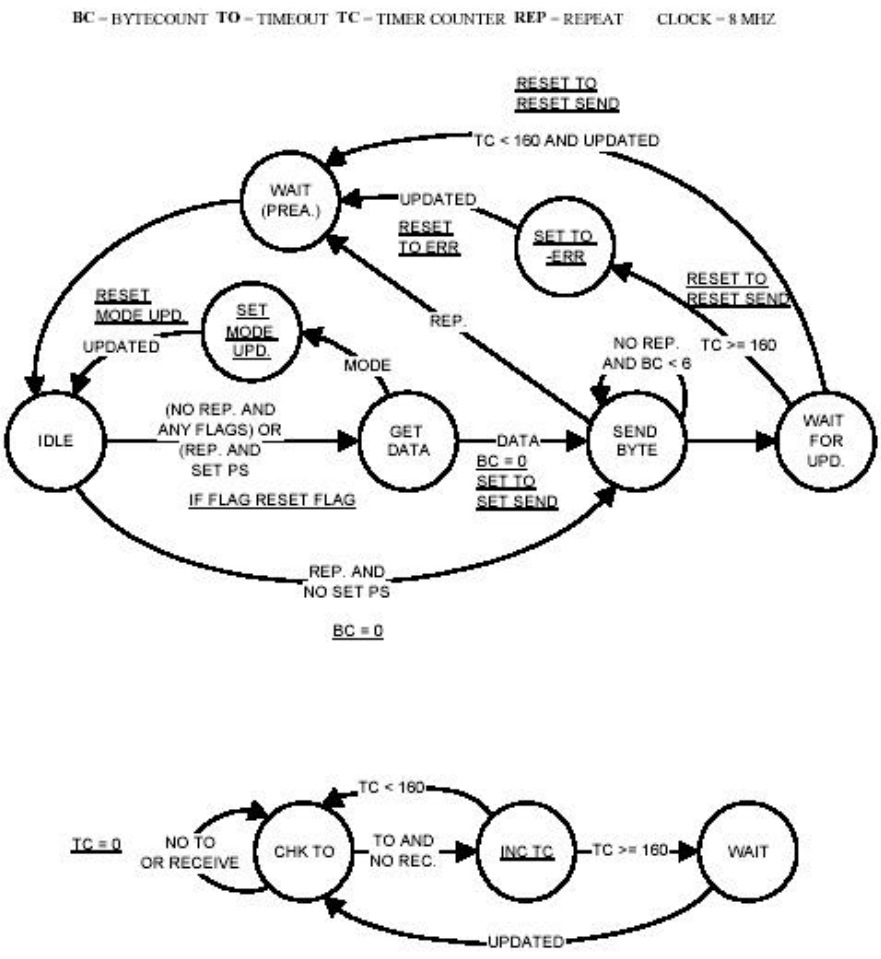


5.1 State transition diagrams



Point to Point Link

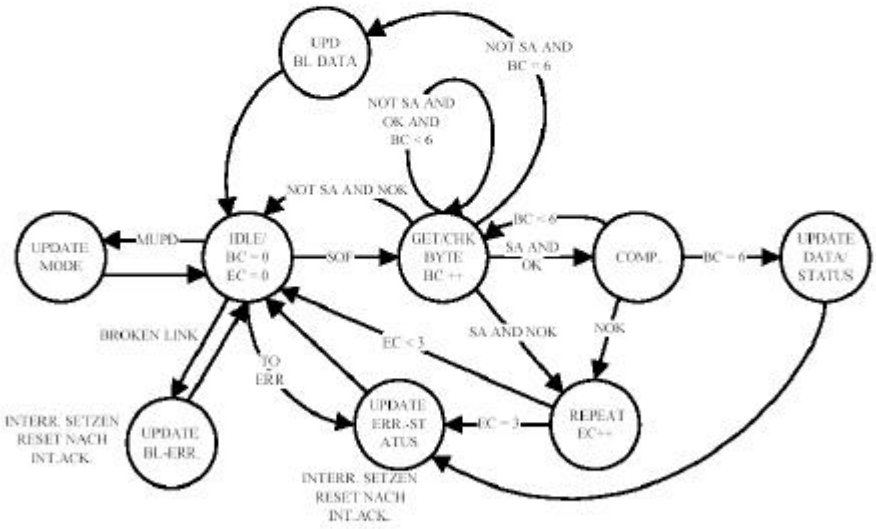
SEND State Transition Diagramm



Point to Point Link

RECEIVE State Transition Diagramm

SOF = START OF FRAME **BC** = BYTECOUNT **EC** = ERRORCOUNT **BL** = BROKEN LINK ERROR **MUPD** = MODE UPDATE VON VME
SA = SEND AKTIV CLOCK = 8 MHZ



References:

1) Andreas Lüdeke, “SLS Power Supply Control: Optical Fibre Link VME Interface Design Draft 1.5”
2) Felix Jenni, 28.05.99: "Power Supply Controller: Block-Daten-download (Programm-, Parameter- und current-waveform etc.)"
3) VITA Standards Organization, 10229 North Scottsdale Road, Scottsdale AZ 85253: "IP-Module Draft Standard VITA 4-1995"