Unit-5

Transmission of Binary Data in Communication Systems

- Digital Codes
- Principles of Digital transmission
- Transmission Efficiency

Modern concepts & Methods
- FSK
- BPSK
- Error detection & correction

Digital Codes →

* In telecommunication, a line code (also called digital baseband modulation, also called digital baseband transmis - sion method) is a code chosen for use within a communication s/s for base band transmission purposes
* Line coding is often used for digital data transport.
* As the coding is done to make more bits to transmit on a single signal, the bandwidth used is much reduced.
* Error detection is done & the bipolar too has a correction capability
* A line code is the code used for data transmission of a digital signal over a transmission line.
* This process of coding is chosen so as to avoid overlap and distortion of signal such as inter-symbol interference.
* There are 3 types of line coding.
    1. Unipolar
    2. Polar
    3. Bi-polar

Unipolar :-

* Unipolar is also called as On-off keying or simply OOK
* the presence of pulse represents a 1 & the absence of pulse represents a 0.
* There are two variations in Unipolar
  1. Non Return to Zero (NRZ)
  2. Return to Zero (RZ)

Polar :-

* They are two methods of polar
  1. Polar NRZ
  2. Polar RZ

Bipolar :-

* This is an encoding technique which has three voltage levels namely +, - & 0. Such a signal is called as duo-binary signal.
* They are two types
  1. Bipolar NRZ
  2. Bipolar RZ

* The codes are broadly categorized into following types
  1. Weighted Codes
  2. Non-Weighted Codes
  3. Binary Coded Decimal
  4. Alpha Numeric Codes
  5. Error Detecting codes
  6. Error Correcting codes

Principles of Digital Transmission →

* Data can be transmitted in two ways
  1. Parallel
  2. Serial
* Data transfers in long-distance communication systems are made serially.

* In a serial transmission, each bit of a word is transmitted one after another.
* Parallel data transmission is not practical for long-distance communication

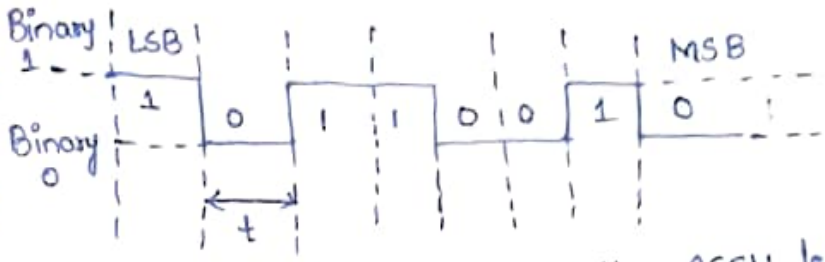


Fig: Serial transmission of the ASCII letter M

Serial Transmission:-

* Expressing the serial Data Rate
* The speed of data transfer is usually indicated as number of bits per second (bps or b/s)
* Another term used to express the data speed in digital communication s/s is baud.
* Baud rate is the number of signaling elements or symbol that occur in a given unit of time.
* A signaling element is simply some change in the binary signal transmitted.

→ Digital transmission is the transfer of data from one point to another.

Advantages:-

1. Noise immunity
2. Encryption
3. Bandwidth efficiency
4. Ability to use repeaters for long distance transmission.

Bit rate = Baud x N

↓

number of bit in one symbol

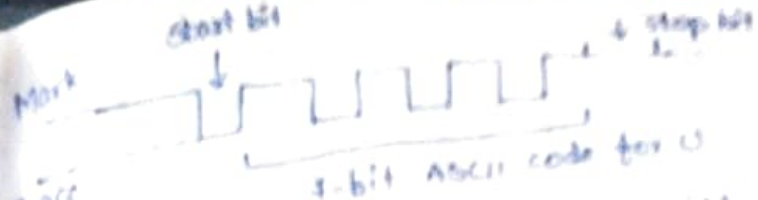


Fig: Asynchronous transmission with start & stop bits

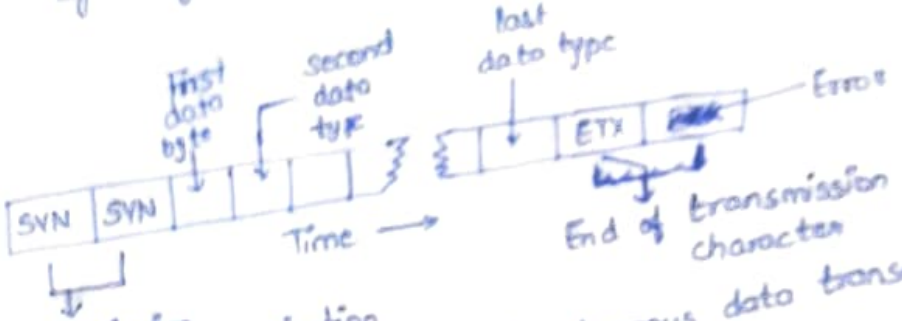


Fig: Synchronous data transmission

Transmission Efficiency →

Hartley's Law :-

* The amount of information that can be sent in a given transmission is dependent on the bandwidth of the communi-cation channel & the duration of transmission.
* Mathematically, Hartley's law is

$$C = 2B$$

where C is the channel capacity (bps) & B is the channel bandwidth

* Hartley's law for multiple coding levels

$$C = 2B \log_2 N$$

↓ number of different encoding levels per time interval

Transmission medias & Bandwidth :-

* The two types of wire cable
  1. Coaxial cable
  2. Twisted pair cable

* Coaxial cable has a center conductor surrounded by an insulator over which is a braided shield. The entire cable is covered with a plastic insulation

* A twisted pair cable is two insulated wires twisted together

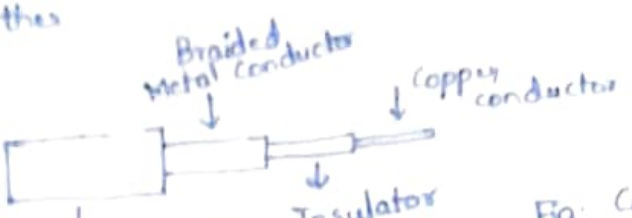


Fig: Coaxial Cable

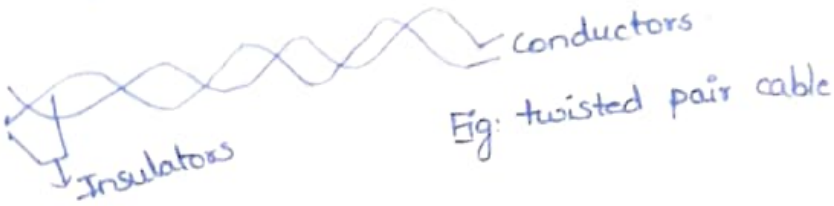
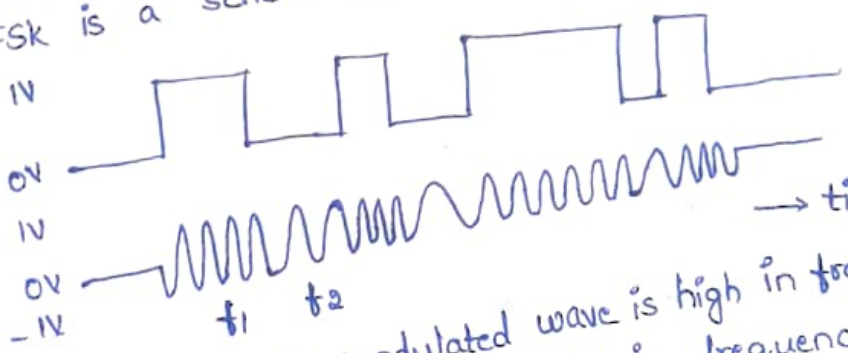


Fig: twisted pair cable

Frequency shift keying (FSK) →

* FSK is the digital modulation technique in which the frequency of the carrier signal varies according to the discrete digital changes.
* FSK is a scheme of frequency modulation.



* The o/p of a FSK modulated wave is high in frequency for a binary HIGH input and is low in frequency for a binary LOW input.
* General expression for FSK is

$$V_{fsk}(t) = V_c \cos\left[2\pi (f_c + V_m(t)\,\Delta f)t\right]$$

Where

$V_{fsk}(t)$ → binary FSK waveform

V_c → peak analog carrier amplitude

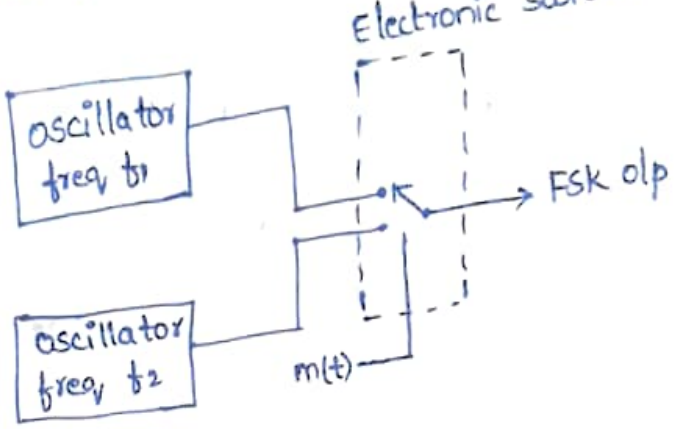
f_c → analog carrier center frequency

f → peak change in the analog carrier frequency

$v_m(t)$ → binary i/p signal

* FSK is analogous to FM where frequency of carrier signal varies in accordance with the base band signal (DATA)

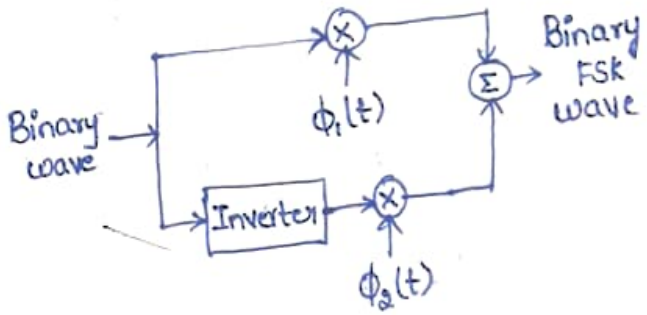
* In FSK, two sinusoidal carrier waves of same amplitude Ac, but different frequencies f_1 & f_2 are used to represent two symbols



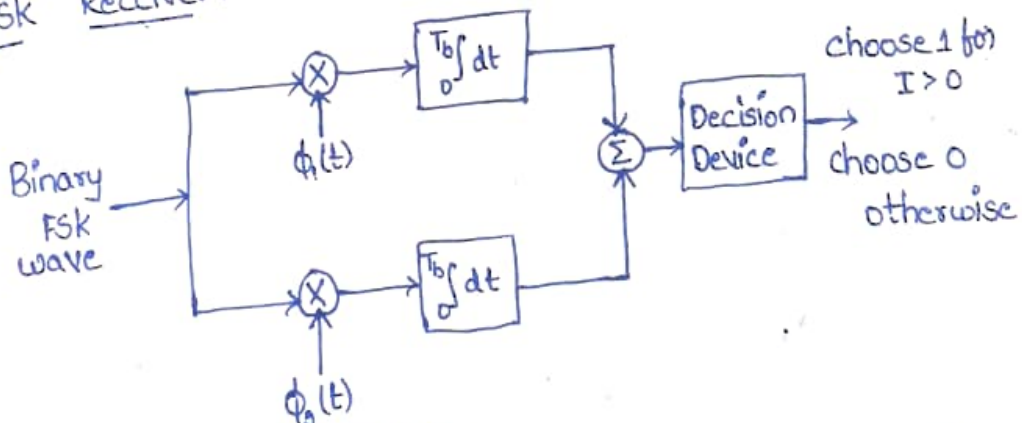
FSK transmitter:-

$$\phi_1(t) = \sqrt{\frac{2}{T_b}} \cos 2\pi f_1 t$$

$$\phi_2(t) = \sqrt{\frac{2}{T_b}} \cos 2\pi f_2 t$$



FSK Receiver:-

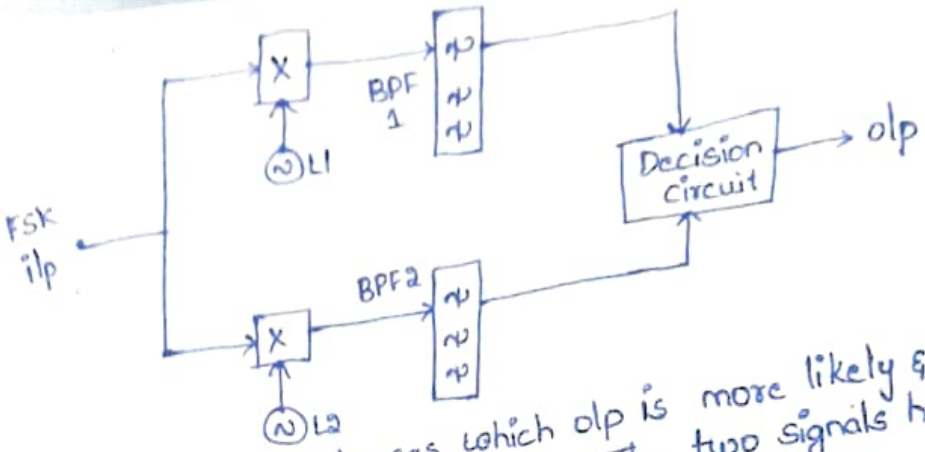


Synchronous FSK Detector:-

* The FSK signal i/p is given to the two mixers with local oscillator circuits.

* These two are connected to two band pass filters.

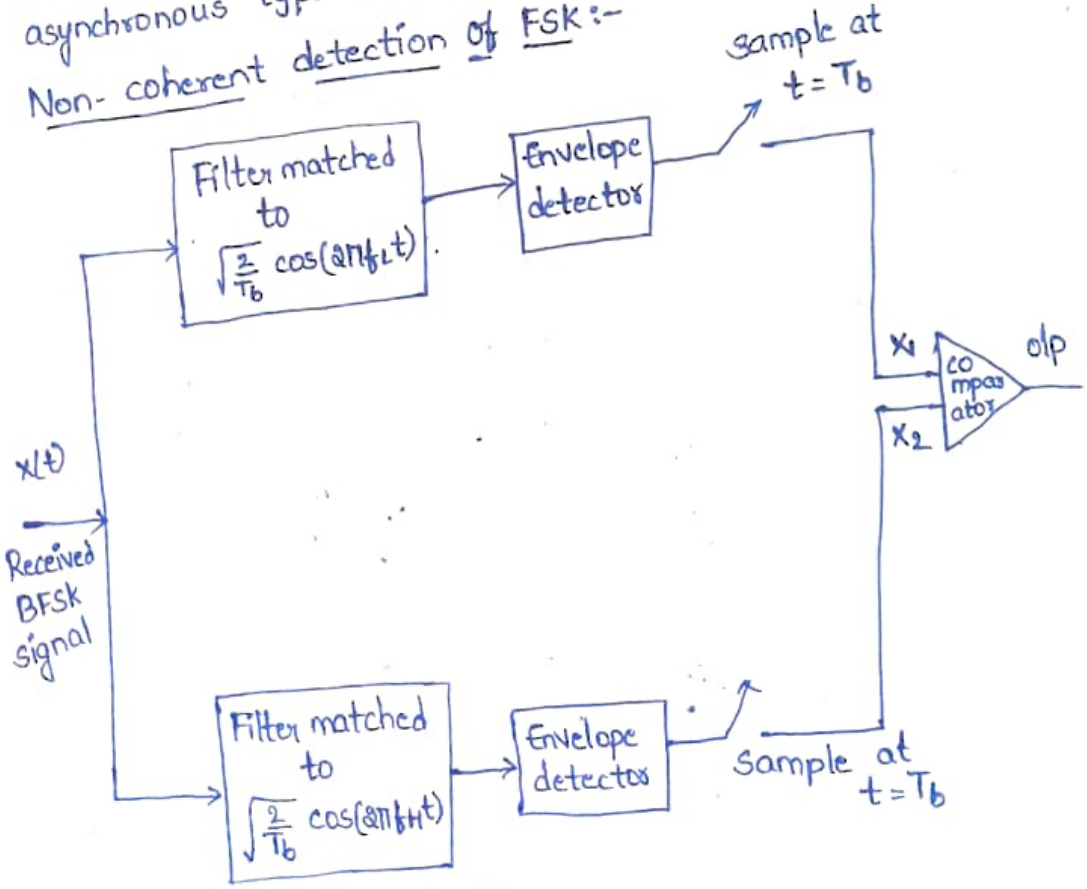
These combinations act as demodulators.



* Decision circuit chooses which olp is more likely & selects it from any one of the detectors. The two signals have a minimum frequency separation.
* For both of the demodulators, the bandwidth of each of them depends on their bit rate.
* This sychronous demodulator is a bit complex than asynchronous type demodulators

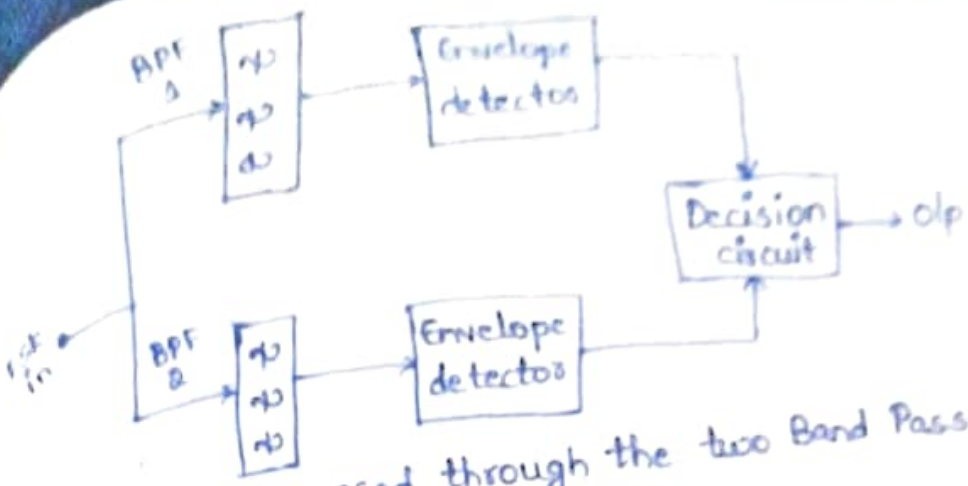
explanation in last

Non-coherent detection of FSK:-

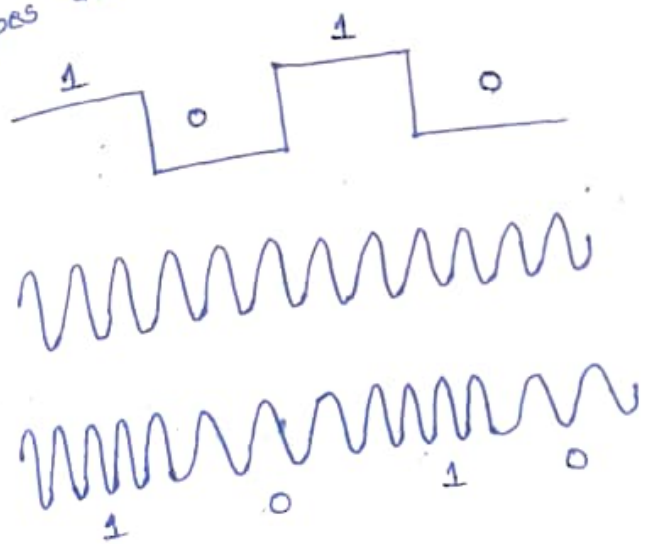


Asynchronous FSK Detector:-

* The block diagram of Asynchronous FSK detector consists of two band pass filters, two envelope detectors & a decision circ.



* FSK signal is passed through the two Band Pass filters tuned to space & mark frequencies.
* The o/p from these two BPF's look like Ask signal, which is given to the envelope detector
* The signal in each envelope detector is modulated asynchronously.
* The decision circuit chooses which o/p is more likely and selects it from any one of the envelope detectors. It also re-shapes the waveform to a required one.



Advantages:-

1. Constant envelope hence not too sensitive to varying attenuation.
2. Detection based on frequency changes, so not sensitive to frequency shifts of channel.
3. Simple implementation possible for low bit rates.

Disadvantages :-

1. Less bandwidth efficient than ASK
2. Requires higher BW

Applications :-

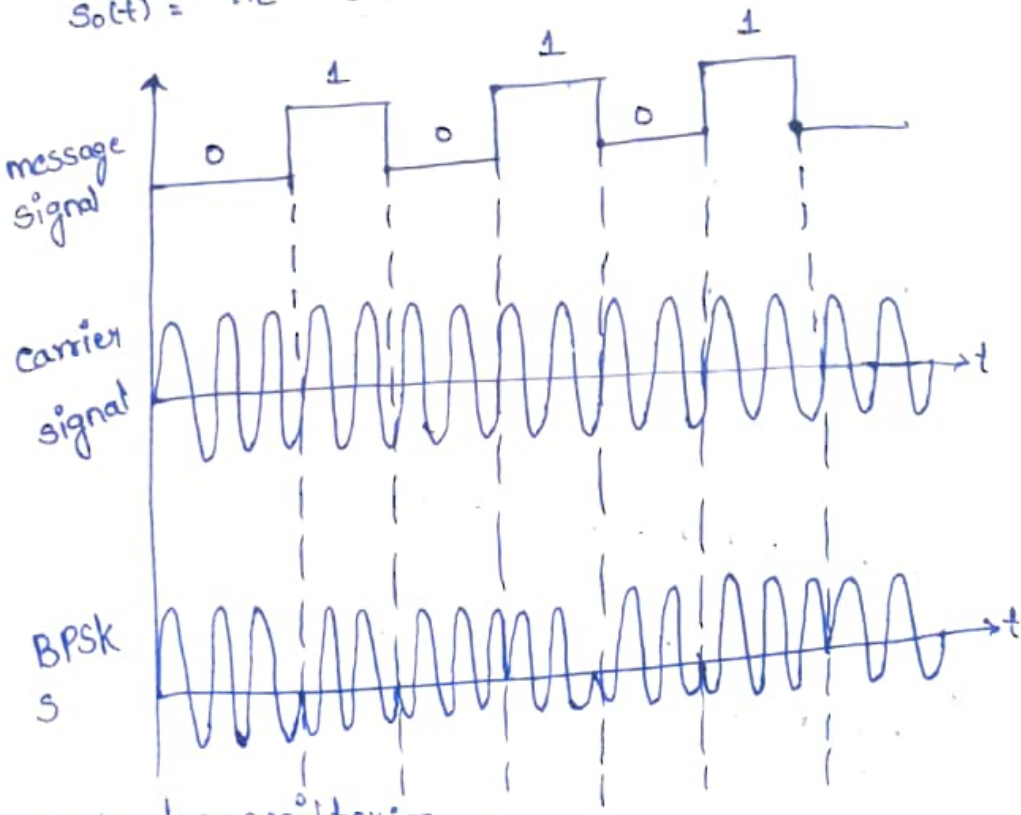
1. Over voice lines in HF radio transmission

Binary Phase shift keying →

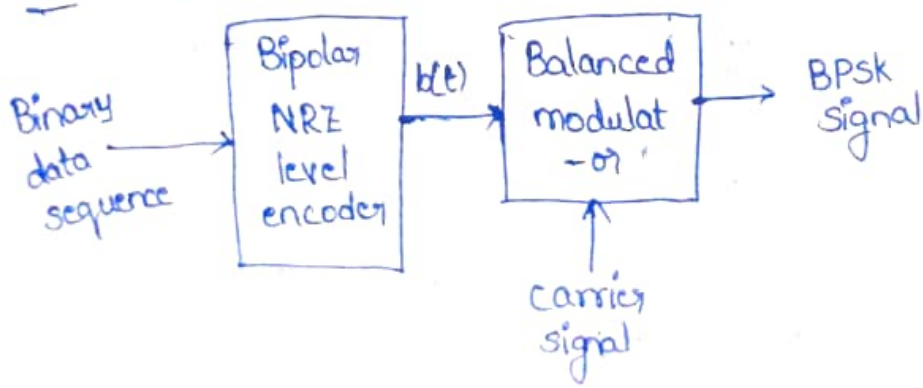
* BPSK is a two phase modulation scheme, where the 0's & 1's in a binary message are represented by two different phase states in the carrier signal: for binary 1 and for binary 0

$$S_1(t) = A_c \cos(2\pi f_c t) \; ; \quad 0 \le t \le T_b \text{ for binary 1}$$

$$S_0(t) = A_c \cos(2\pi f_c t + \pi) \; ; \quad 0 \le t \le T_b \text{ for binary 0}$$



BPSK transmitter :-



* The BPSK signal can be generated by applying carrier signal to the balanced modulator. The baseband signal b(t) is applied as a modulating signal generator to the balanced. The NRZ level encoder converts the binary data sequence into bipolar NRZ signal.

* In BPSK, binary symbol '1' & '0' modulate the phase of the carrier.

Let, the carrier be

$$S(t) = A_c \cos(2\pi f_0 t) \rightarrow (1)$$

* A represents peak value of sinusoidal carrier. In the standard 1 ohm load register, the power dissipated will be

$$P = \frac{1}{2} A^2$$

$$A = \sqrt{2P} \rightarrow (2)$$

* When the symbol is changed, then the phase of the carrier is changed by 180 degrees.

Consider, for example

symbol '1' $\rightarrow$ $S_1(t) = \sqrt{2} P \cos(2\pi f_0 t) \rightarrow (3)$

symbol '0' $\rightarrow$ $S_2(t) = \sqrt{2} P \cos(2\pi f_0 t + \pi) \rightarrow (4)$

Since $\cos(\theta + \pi) = -\cos\theta$

$\therefore$

$$\text{ab } S_2(t) = -\sqrt{2} P \cos(2\pi f_0 t) \rightarrow (5)$$

$$S(t) = b(t) \sqrt{2} P \cos(2\pi f_0 t) \rightarrow (6)$$

Here, $b(t) = +1$ when binary '1' is transmitted

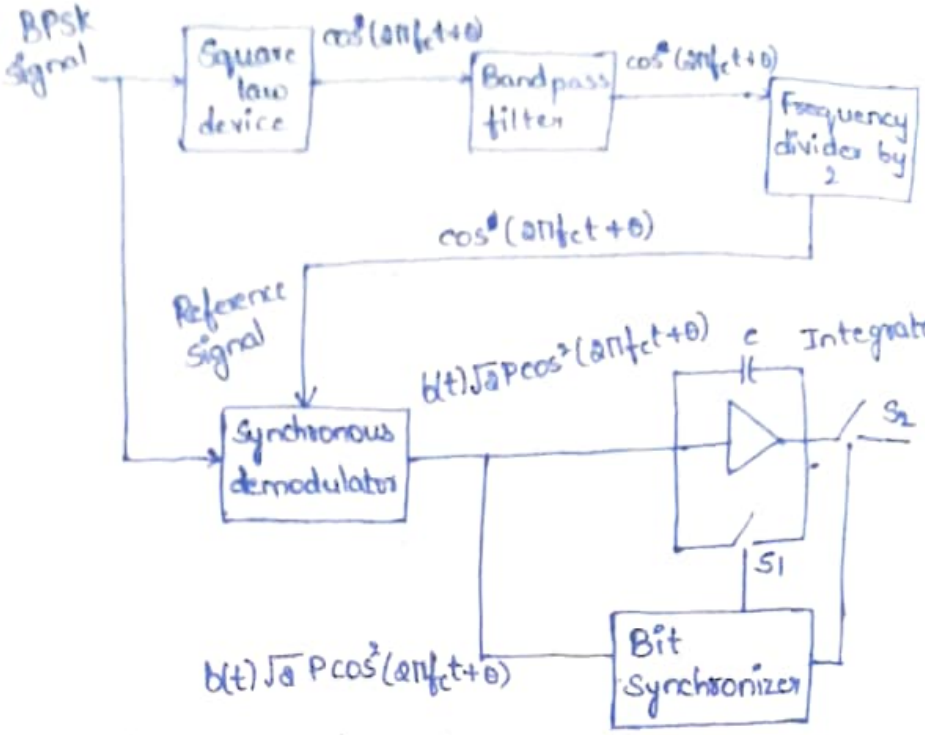
$= -1$ when binary '0' is transmitted

BPSK Receiver:-

Phase shift in received signal:-

* This signal undergoes the phase change depending upon the time delay from the transmitter to receiver.

* This phase change is normally fixed phase shift in the transmitted signal. Let the phase shift be θ. Therefore the signal at the input of the receiver is,



$$S(t) = b(t)\sqrt{2}P\cos(2\pi f_c t+\theta) \rightarrow (1)$$

Square law device :-

* Now from this received signal, carrier is separated since this is coherent detection, the received signal is passed through a square law device.
* At the o/p of the square law device the signal will be, $\cos^2(2\pi f_0 t+\theta)$.
* We have neglected the amplitude, because we are only interested in the carrier of the signal.

We know that, $\cos^2\theta = \frac{1+2\cos\theta}{2}$

$$\therefore \cos^2(2\pi f_0 t+\theta) = \frac{1+\cos 2(2\pi f_0 t+\theta)}{2}$$

$$= \frac{1}{2}+\frac{1}{2}\cos 2(2\pi f_0 t+\theta)$$

Here $\frac{1}{2}$ represents D.C level.

Band Pass filter :-

* This signal is then passed through a band pass filter whose pass band is centered around $2f_0$.
* Band pass filter removes the D.C level of $\frac{1}{2}$ and at its output we get,

cos 2(2πf₀t + θ) has a frequency of 2f₀

Frequency divider :-

The above signal is passed through a frequency divider by two.

∴ At the o/p of frequency divides we get a carrier signal whose frequency is f₀ i.e., cos (2πf₀t + θ).

Synchronous demodulator :-

The synchronous demodulator multiplies the input signal and the recovered carrier.

At the o/p of multiplier we get,

$$b(t)\sqrt{2}P\cos(2\pi f_0 t)\cos(2\pi f_0 t+\theta) = b(t)\sqrt{2}P\cos^2(2\pi f_0 t+\theta)$$

$$= b(t)\sqrt{2}P\left[\frac{1}{2}+\frac{1}{2}\cos 2(2\pi f_0 t+\theta)\right]$$

$$s(t) = b(t)\sqrt{\frac{P}{2}}\left[1+\cos 2(2\pi f_0 t+\theta)\right] \rightarrow (8)$$

Bit Synchronizer & Integrator :-

The above signal is then applied to the bit synchronize & integrator. The integrator integrates the signal over one bit period.

The bit synchronizes takes care of starting & ending times of a bit

Generation & detection of Coherent BPSK :- explanation last

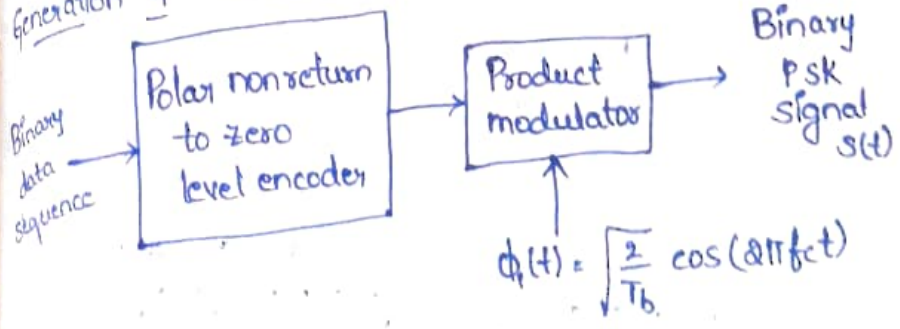


Fig: block diagram of BPSK transmitter

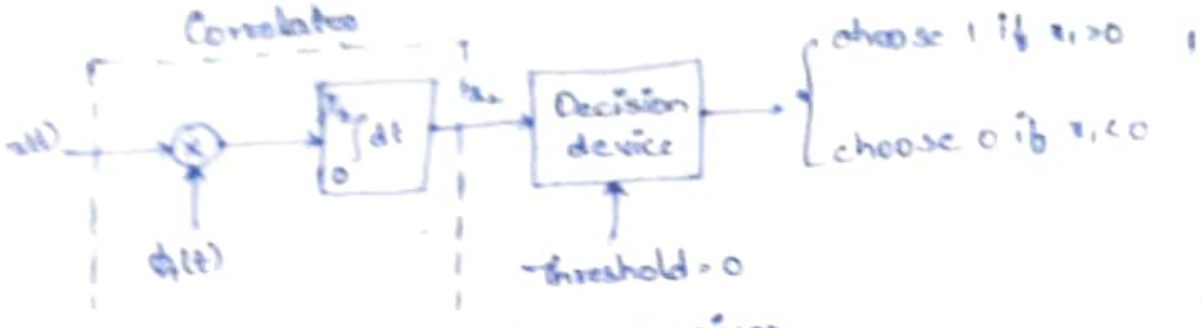


Fig: Coherent BPSK receiver

Advantages:-

1. Bandwidth is less than FSK
2. Perform best in the presence of noise out of all the 3 types of modulation techniques
3. High immune to noise.

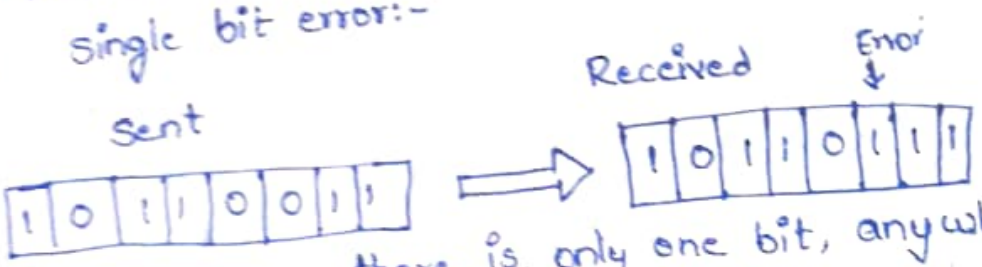
Disadvantages:-

1. Recovered signal is unchanged even if the ip signal has changed its sign.
2. Possibility of overlapping

Error detection & correction →

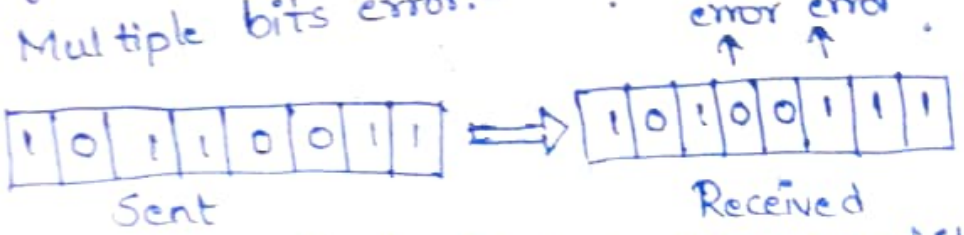
* There are three types of errors:

1) single bit error:-



* In a frame, there is only one bit, anywhere though, which is corrupt.

2) Multiple bits error:-



* Frame is received with more than one bits in corrupted state

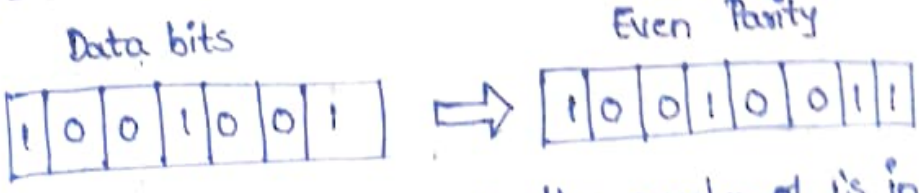
* Frame contains more than 1 consecutive bits corrupted
* Error control mechanism may involve two possible ways:
  1) Error detection
  2) Error correction

Error detection:-

* Errors in the received frames are detected by means of Parity check and cyclic Redundancy check (CRC). In both cases, few extra bits are sent along with actual data to confirm that bits received at other end are same as they were sent. If the counter check at receiver end fails, the bits are considered corrupted.

Parity check:-

* One extra bit is sent along with the original bits to make number of 1's either even in case of even parity, or odd in case of odd parity
* The sender while creating a frame counts the number of 1's in it. For example, if even parity is used and number of 1's is even then one bit with value 0 is added. This way number of 1's remains even. If the number of 1's is odd, to make it even a bit with value 1 is added.



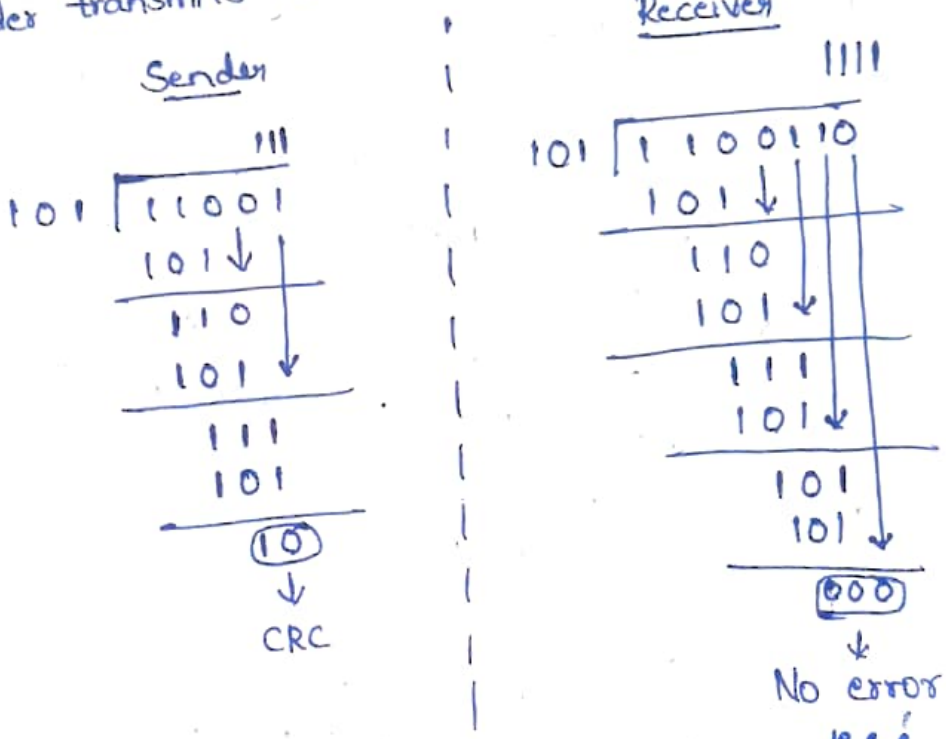
* The receiver simply counts the number of 1's in a frame. If the count of 1's is even & even parity is used, the frame is considered to be not-corrupted & is accepted. If the count of 1's is odd and odd parity is used, the frame is still not corrupted

* If a single bit flips in transit, the receiver can detect it by counting the number of 1's. But when more than one bits are erroneous, then it is very hard for the receiver to detect the error

Cyclic Redundancy Check (CRC):-

* CRC is a different approach to detect if the received frame contains valid data. This technique involves binary division of the data bits being sent. The divisor is generated using polynomials. The sender performs a division operation on the bits being sent and calculates the remainder.

* Before sending the actual bits, the sender adds the remainder at the end of the actual bits. Actual data bits plus the remainder is called a code word. The sender transmits data bits as code words.



* At the other end, the receiver performs division operation on code words using the same CRC divisor. If the remainder contains all zeros the data bits are accepted, otherwise it is considered as there some data corruption occured in transit.

Error Correction →

* In the digital, error correction can be done in two

ways

1. Backward Error Correction:- When the receiver detects an error in the data received, it requests back the sender to retransmit the data unit.

2. Forward Error Correction:- When the receiver detects some error in the data received, it executes error correcting code which helps it to auto recover and to correct some kinds of errors.

Hamming code:-

* Hamming code is a block code that is capable of detecting upto two simultaneous bit errors and correcting single-bit errors.

* The procedure used by the sender to encode the message encompasses the following steps.

step 1: Calculation of the number of redundant bits.

step 2: Positioning the redundant bits.

step 3: Calculating the values of each redundant bit

Eg: If the 7-bit hamming code word received by a receiver is 1011011. Assuming the even parity state whether the received code word is correct or wrong. If wrong locate the bit having error.

Sol:

D_7	D_6	D_5	P_4	D_3	P_2	P_1
1	0	1	1	0	1	1

P_4 D_5 D_6 D_7 → total no of 1's

1 1 0 1 → 3 (odd)

$P_4 = 1$

P_2 D_3 D_6 D_7 → 2 (even)

1 0 0 1

$P_2 = 0$

P_1 D_3 D_5 D_7 → 3 (odd)

1 0 1 1

$P_1 = 1$

P_4 P_2 P_1

1 0 1 = $(5)_{10}$

5th bit is having error

D_7	D_6	D_5	P_4	D_3	P_2	P_1
1	0	0	1	0	1	1

↙ correct code

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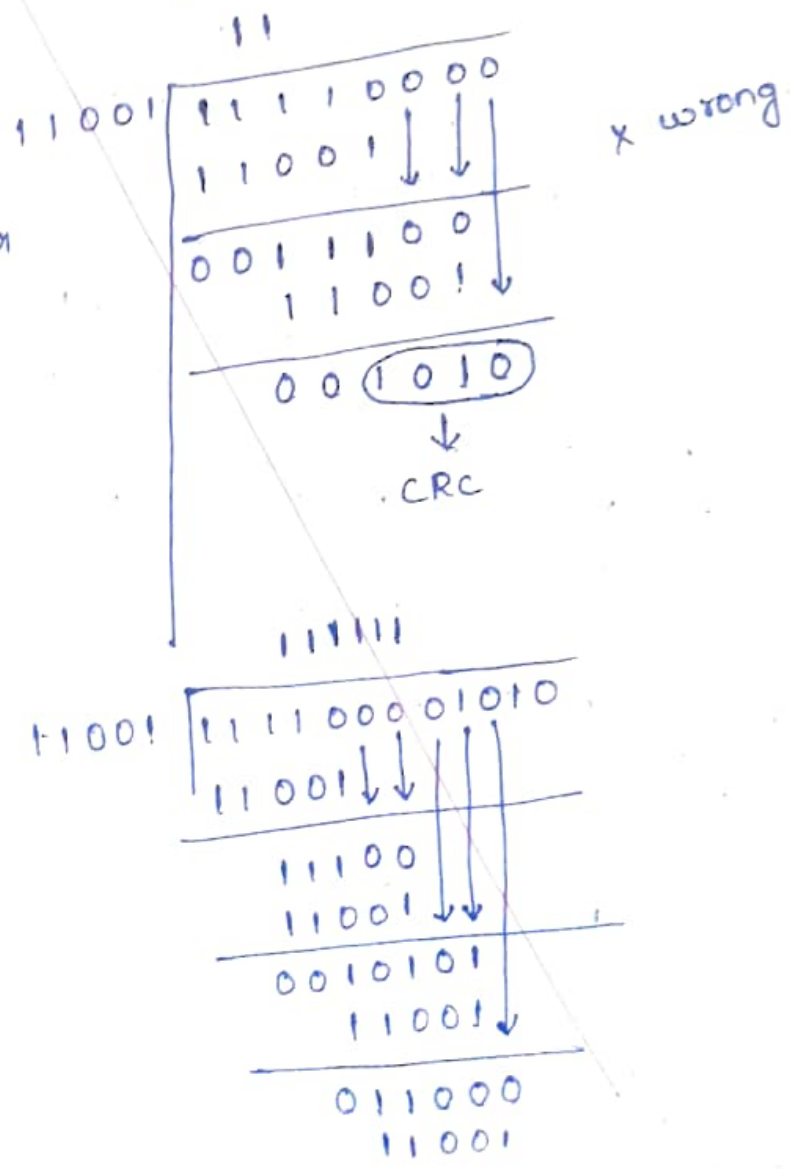
* If generating polynomial for CRC code is x^4+x^3+2 & message word is 11110000, determine check bits and code word.

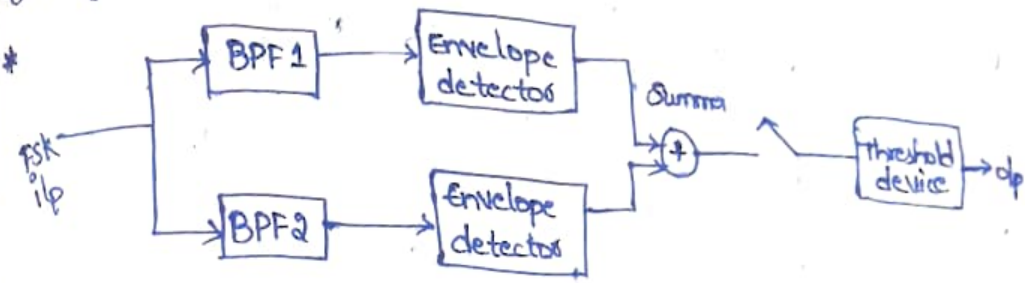
4	3	2	1	0
1	1	0	0	1

Sol: $x^4+x^3+2 \Rightarrow$



Non coherent detection of FSK →

* Requires no reference wave; does not exploit phase reference information.
* Non coherent detection is less complex than coherent detection
* The modulated FSK signal is forwarded from the bandpass filter 1 & 0 with cut off frequencies equal to the space and mark frequencies
* So, the unwanted signal components can be eliminated from the BPF & the modified FSK signals are applied as input to the two envelope detectors
* This envelope detector is a circuit having a diode (D).
* Based upon the ilp to the envelope detector it delivers the olp signal.
* This envelope detector used in the amplitude demodulation process. Based upon its ilp it generates the signal & then it is forwarded to the threshold device.
* This threshold device gives the logic 1 & 0 for the different frequencies. This would be equal to the original binary ilp sequence.



Generation & detection of Coherent BPSK →

Generation:-

* To generate the BPSK, we build on the fact that the BPSK signal is a special case of DSB-SC modulation.
* Specifically, we use a product modulator consisting of two components.

i. Non return to zero level encoder: the ilp binary data sequence is encoded inpolar form with symbol 1 & 0

represented by the constant amplitude

ii. Product modulator: which multiplies the level encoded binary wave by the sinusoidal carrier of amplitude to produce the BPSK signal. The timing pulses used to generate the level encoded binary wave & the sinusoidal carrier wave are usually, but not necessarily, extracted from a common master clock.

Detection:-

* To detect the original binary sequence of 1's & 0's, the BPSK signal at the channel o/p is applied to a receiver that consists of four sections.

i. Product modulator: which is also supplied with a locally generated reference signal that is replica of the carrier wave.

ii. low-pass filter: designed to remove the double-frequency components of the product modulator o/p & pass the zero frequency components.

iii. Sampler: which uniformly samples the o/p of the low pass filter at where; the local clock governing the operation of the sampler is synchronized with the clock responsible for bit-timing in the transmitter.

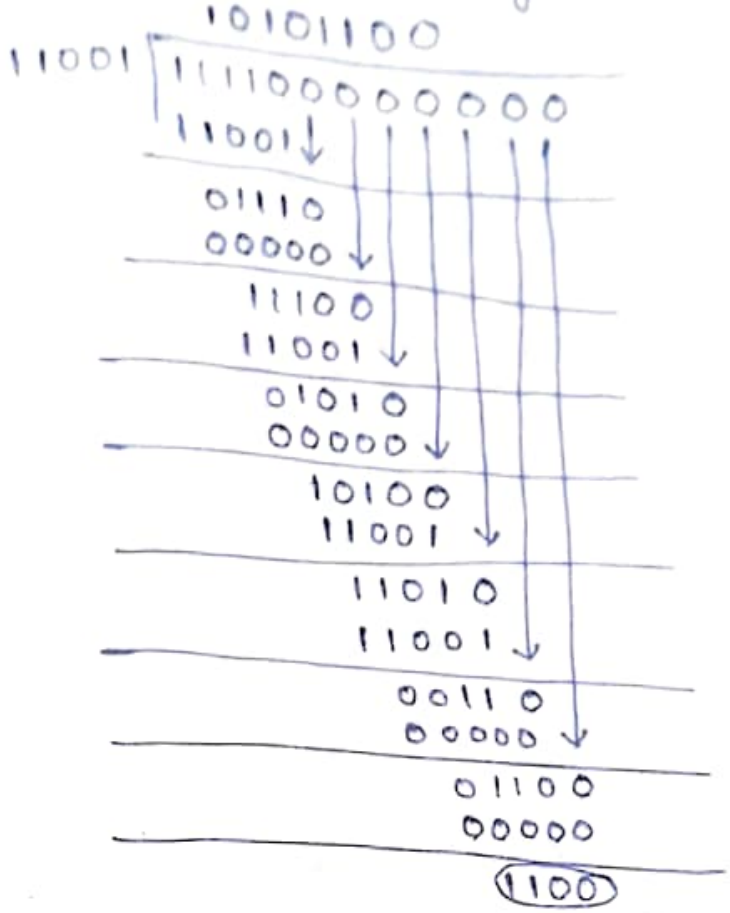
iv. Decision making device: which compares the sampled value of the low-pass filters o/p to an externally supplied threshold, every seconds. If the threshold is exceeded, the device decides in favor of symbol 1; otherwise; it decides in favor of symbol 0 levels.

* If generating polynomial for CRC code is x^4+x^3+1 & message word is 11110000, determine check bits & code word.

Sol.

$x^4 + x^3 + 1 \Rightarrow 11001$

add 4 zeroes to message word i.e., 11110000



Add this check bits to message word. If remainder is zero i.e., no error. If remainder is not zero there is error in specific position.