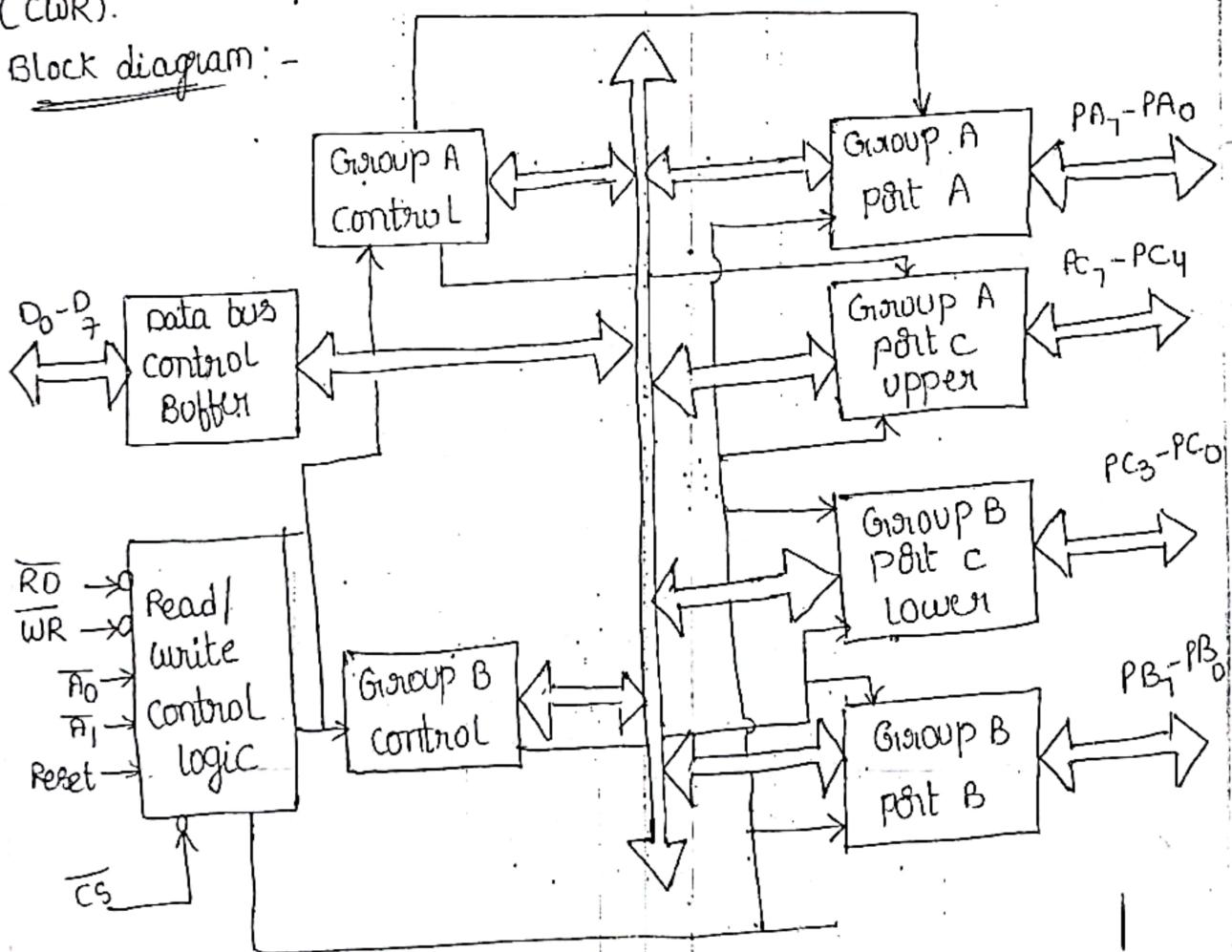


PIO 8255 (Programmable input-output port) :- (PPI)

The parallel input-output port chip 8255 is also known as programmable peripheral input-output port. It has 24 Input/output lines which may be individually programmed in two Groups of twelve lines each or three groups of eight lines. The two groups of I/O pins are named as group A and group B. Thus Group A contains an 8-bit port A along with a 4-bit port C (upper). ($PA_0 - PA_7$ & $PC_4 - PC_7$) Similarly, Group B contains an 8-bit port B, containing lines 8-bit port B ($PB_0 - PB_7$) along with a 4-bit port C ($PC_0 - PC_3$). All these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).

Block diagram:-



Block diagram of 8255 internal architecture.

The 8-bit data bus buffer is controlled by the read / write control logic. The read / write control logic manages all of the internal and external transfer of both data and control words. RD, WR, A₁, A₀ and reset are the inputs, provided by the microprocessor to the read / write control logic of 8255.

The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus. This buffer receives & transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

Input					
RD	WR	CS	A ₁	A ₀	Read cycle
0	1	0	0	0	Port A to data bus.
0	1	0	0	1	Port B to data bus.
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus.
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR
X	X	1	X	X	Data bus tri-stated
1	1	0	X	X	Data bus tri-stated.

} Read operation.

} Output

} Write cycle.

Modes of operation of 8255:-

There are two basic modes of operation of 8255 -

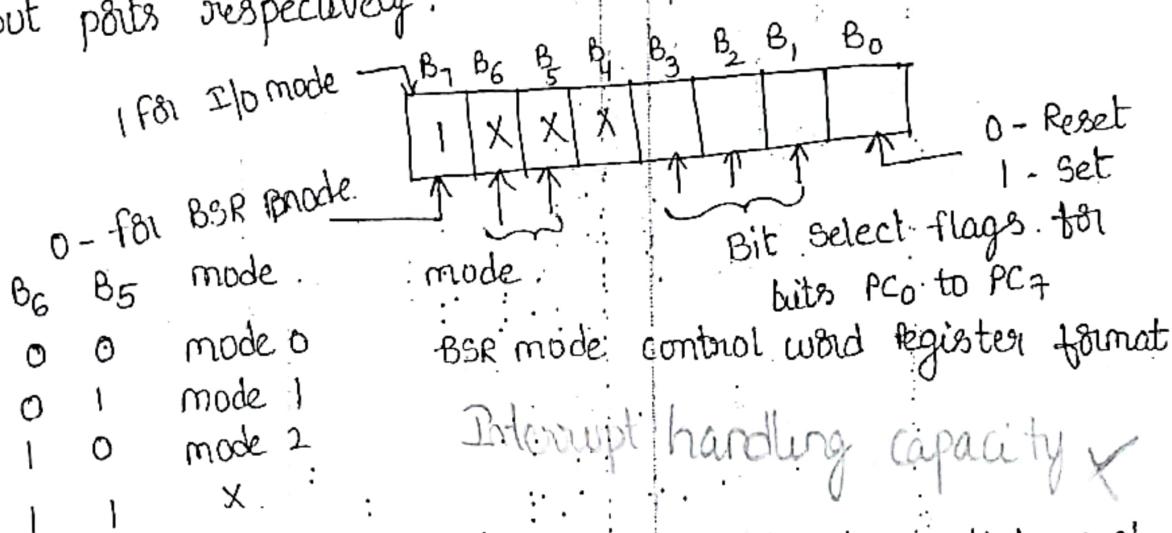
I/O mode and Bit Set-Reset mode. In the I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (P_{C0} - P_{C7}) can be used to set or reset its individual port bits. Under the I/O mode of operation, further there are three modes of operation of 8255, so as to

Support different types of applications mode 0, mode 1 and mode 2.

→ BSR mode :- In this mode, any of the 8-bits of port C can be set or reset depending on B0 of the control word. The bit to be set or Reset is selected by bit Select flags B₃, B₂ and B₁ of the CWR. The CWR format

→ I/O modes :- This mode is also known as basic input / output mode. This mode provides with simple input and output capability using each of three ports. Data can be simply read from and written to the input & output ports respectively.

B ₃	B ₂	B ₁	Selected bits of Port C
0	0	0	B ₀ (PC ₀)
0	0	1	B ₁ (PC ₁)
0	1	0	B ₂ (PC ₂)
0	1	1	B ₃ (PC ₃)
1	0	0	B ₄ (PC ₄)
1	0	1	B ₅ (PC ₅)
1	1	0	B ₆ (PC ₆)
1	1	1	B ₇ (PC ₇)



mode 1 (strobed I/O mode) :- This mode is also called as strobed input / output mode. In this mode the handshaking signals control the input & output action of the specified port. Port C lines PC₀ - PC₂ provides strobe & handshake lines for port B. Then PC₀ - PC₂ is called as Group B for strobed data input / output similarly port C lines PC₃ - PC₅ provides strobe lines for port A. Then PC₃ - PC₅ is called as Group A for strobed data input / output.

interv ✓

Input control signals.

(STB) - If (strobe input). If this line falls to logic low level, the data available at 8-bit input port is loaded into input latches.

IBF (input Buffer full) :- If this signal rises to logic 1, it indicates that data has been loaded into the latches it works as an acknowledgement.

INTR (Interrupt Request) :- This active high output signal can be used to interrupt the CPU whenever an input device request the service.

Output control signals:-

OBF (Output buffer full) :- This status signal, whenever falls to logic low, indicates that the CPU has written data to the specified output port.

ACK (Acknowledge input) :- ACK signal acts as an acknowledgement to be given by an output device.

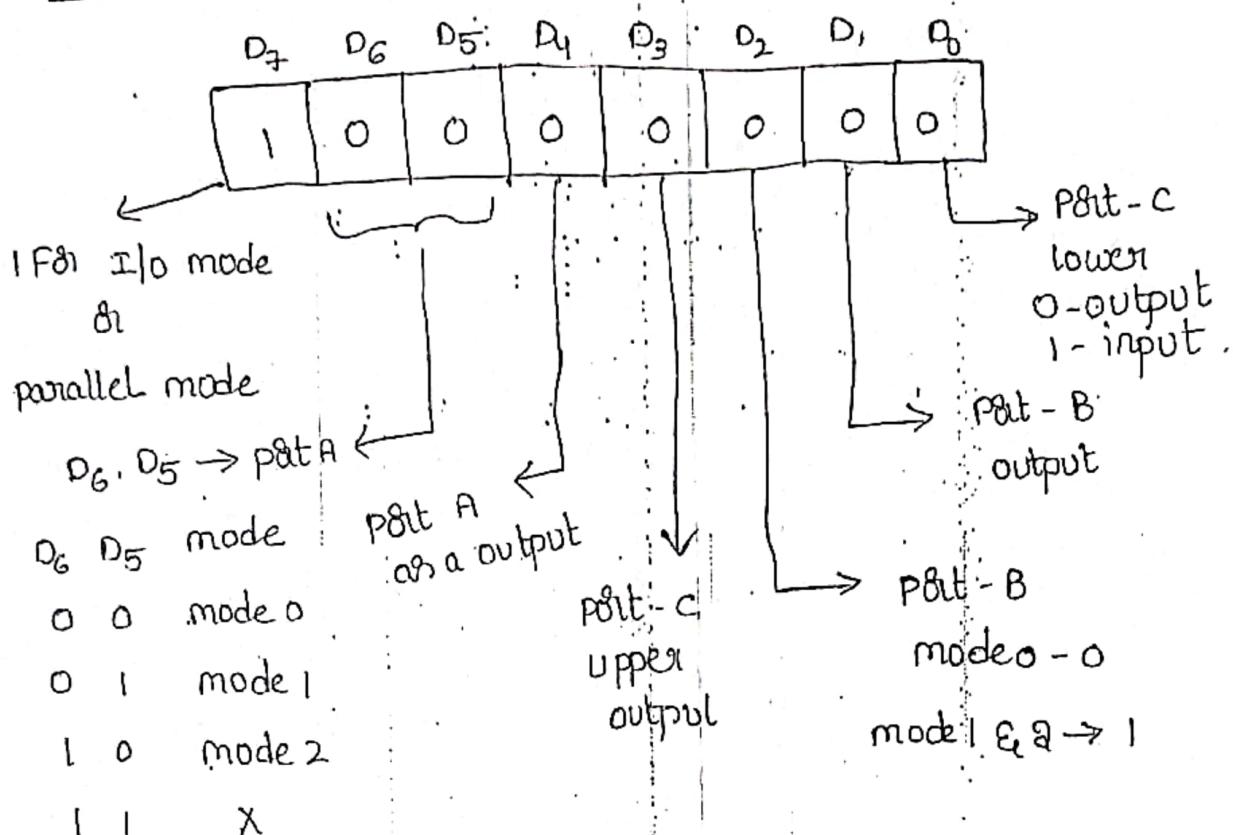
INTEI (interrupt request) :- Thus an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from the CPU.

mode 2 (strobed, bidirectional I/O) :- This mode of operation provides 8255 with an additional feature for communicating with a peripheral device on an 8-bit data bus. hand-shaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver.

control signals for output operation :- OBF, ACK, INTEI

Control signal for input operation :- STB, IBF.

parallel I/O mode :- (I/O mode)



I/O mode control word Register format.

Port	mode 0	mode 1	mode 2	BSR mode
Port A	✓	✓	✓	X
Port B	✓	✓	X	X
Port C	✓	X(HS)	X(HS)	✓

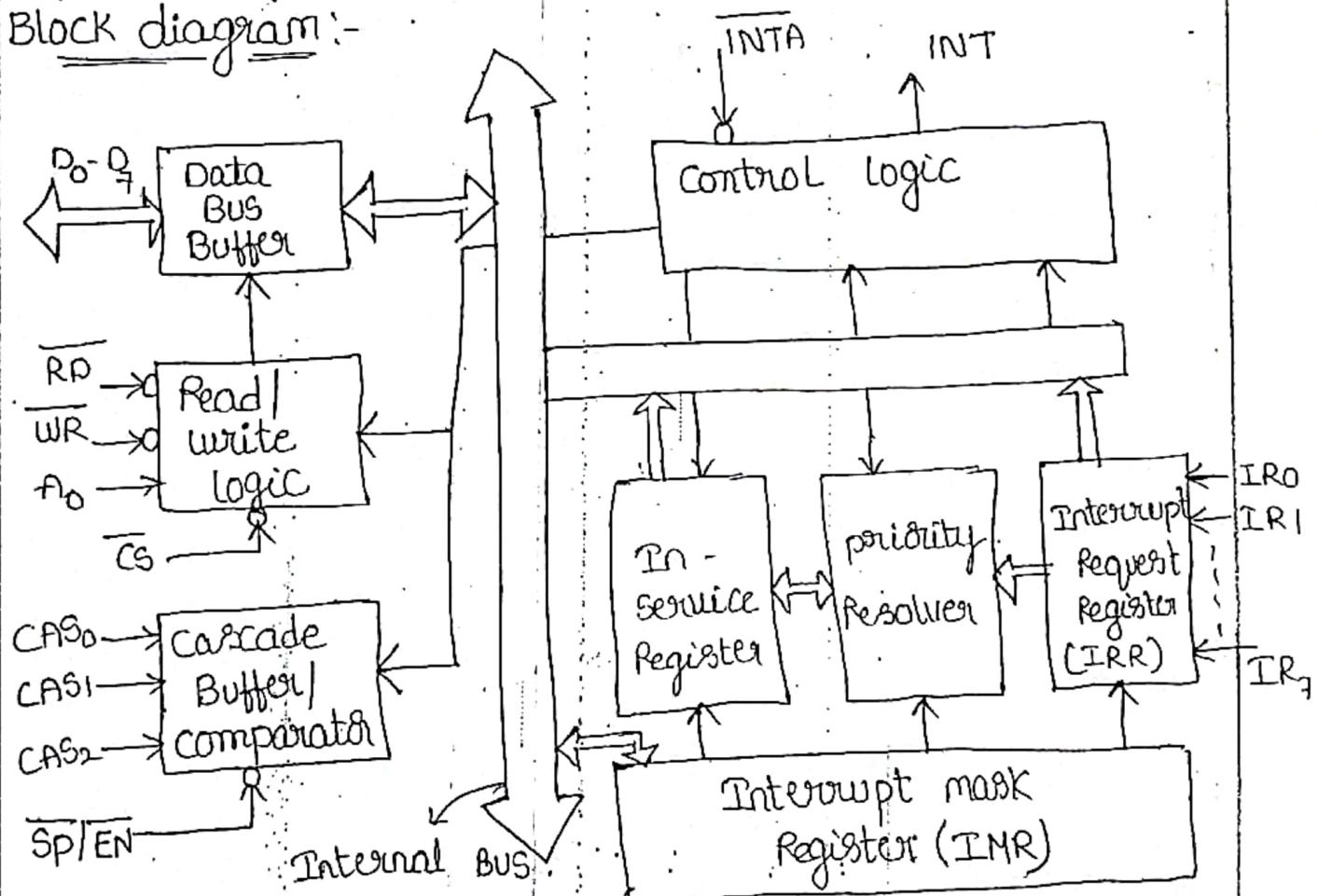
programmable Interrupt controller (8259A).

The processor 8085 had five hardware interrupt pins. Out of these five interrupt pins, four pins were allotted fixed vector addresses but the pin INTR was not allotted any vector address, rather an external device was supposed to hand over the type of interrupt to the microprocessor. Consider an application, where a number of I/O devices connected with a CPU desire to transfer data using interrupt driven data transfer mode. In these types of applications, more number of interrupt pins are required.

than available in a typical microprocessor. In these multiple interrupt systems, the processor will have to take care of the priorities for the interrupts, simultaneously occurring at the interrupt request pins.

To overcome all these difficulties, we require a programmable interrupt controller which is able to handle a number of interrupts at a time. This controller takes care of a number of simultaneously appearing interrupt requests along with their types and priorities.

Block diagram:-



Block diagram of 8259A.

Data bus buffer:- This tri-state bidirectional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information.

Control logic :- This Block has an input and an output line. If the 8259A is properly enabled the interrupt request will cause the 8259A to assert its INT output pin high. If this pin is connected to the INTR pin of an 8086 and if the 8086 interrupt flag is set, then this high signal will cause the 8086 to respond INTR.

SP/EN (slave program / enable buffer) :-

The SP/EN Signal is tied high for the master, it is grounded for the slave.

Interrupt Sequence :-

1. one or more of the interrupt request lines (IR0 - IR7) are raised high, setting the corresponding IRR bits.
2. The priority resolver checks three registers (IRR, IMR & ISR). It resolves the priority and sets the INT high when appropriate.
3. The CPU acknowledges the INT and responds with an INTA pulse.
4. Upon receiving an INTA from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset.
5. The priority modes can be changed or reconfigured dynamically at any time during the main program.
6. The 8086 will initiate a second INTA pulse. 8259A releases a 8-bit pointer (interrupt type) onto the data bus where it is read by the CPU.
7. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

pass through data buffer during read or write operations.

Read / write Control logic :- This circuit accepts and decodes commands from the CPU. This block also allows the status of the 8259A to be transferred on to the data bus.

Cascade Buffer / Comparator :- This block stores and compares the I/Os of all the 8259A's used in the system. The three I/O pins CASO - A are outputs when the 8259 is used as a master. The same pins act as inputs when 8259 is in the slave mode. The 8259A in the master mode, sends the ID of the interrupting slave device on these lines. The slave thus selected, will send its pre-programmed vector address on the data bus during the next INTA pulse.

Interrupt request Register (IRR) :- The IRR is used to store all the interrupt levels which are requesting service. The eight interrupt inputs set corresponding bits of the Interrupt Request Register.

Priority Resolver :- The priority resolver determines the priorities of the bits set in the IRR. The bit corresponding to the highest priority interrupt input is set in the ISR during the INTA input.

Interrupt Service Register (ISR) :- The interrupt service Register (ISR) stores all the levels that are currently being serviced.

Interrupt mask Register (IMR) :- Interrupt mask Register (IMR) stores the masking bits of the interrupt lines to be masked. This register can be programmed by an OCW. An interrupt which is masked by software will not be recognized and serviced even if it set the corresponding bits in the IRR.

Priority modes

(FNM)

→ 1) Fully Nested mode :- It is called as default mode. The 8259 continues to operate in the fully nested mode until the mode is changed through operation command words. In this mode, IR0 has highest priority and IR7 has lowest priority. The bit in the ISR will remain set until an EOI command is issued by the microprocessor at the end of interrupt service routine. But if FEOI bit is set, the bit in the ISR resets at the trailing edge of the last INTA.

→ 2) Special Fully Nested mode (SFNM) :-

The special fully nested mode is used to avoid the drawbacks in FNM. It is similar to the FNM except for the following differences:

i) When an interrupt request from a slave is being serviced, the slave is allowed to place further requests. These interrupts are recognized by the master and it initiates interrupt requests to the CPU.

ii) Before exiting from the interrupt service routine, a non-specific EOI must be sent to the slave and its ISR must be read to determine if it was the only interrupt to the slave. If the ISR is empty, a non-specific EOI command can be sent to the master. If it is not empty, it implies that the same IR level input to the master is to be serviced again due to more than one interrupt being presented to the slave, and an EOI must not be sent to the master.

→ 3) Rotating priority mode :- The rotating priority mode can be set in i) automatic rotation, ii) specific rotation.

i) Automatic Rotation :- In this mode, a device, after being serviced, receives the lowest priority. Assuming that IR3 has just been serviced, it will receive the seventh priority.

IR ₀	IR ₁	IR ₂	IR ₃	IR ₄	IR ₅	IR ₆	IR ₇
4	5	6	7	0	1	2	3

ii) specific Rotation :- In the automatic rotation mode, the interrupt request last serviced is assigned the lowest priority, whereas in the specific rotation mode, the lowest priority can be assigned to any interrupt input (IR₀ to IR₇) thus fixes all other priorities.

For example if the lowest priority is assigned to IR₂, other priority are as shown below

IR ₀	IR ₁	IR ₂	IR ₃	IR ₄	IR ₅	IR ₆	IR ₇
5	6	7	0	1	2	3	4

d) special mask mode :-

If any interrupt is in service then the corresponding bit is set in ISR and the lower priority interrupts are inhibited. Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control, for example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion. In these case we have to go for special mask mode.

e) poll mode :- In this mode the INT output is not used.

The microprocessor checks the status of interrupt requests by issuing poll command. The microprocessor reads contents of 8259A after issuing poll command. During this read operation the 8259A provides polled word and sets ISR bit of highest priority active interrupt request format

I = 1 = one or more interrupt requests activated

I = 0 = No interrupt request activated

I	X	X	X	X	w ₂	w ₁	w ₀
---	---	---	---	---	----------------	----------------	----------------

w₂, w₁, w₀ = Binary code of highest priority active interrupt request.

Command words of 8259A

The command words of 8259A are classified in two groups.

i) Initialization command words (ICWs)

ii) Operation command words (OCWs)

iii) Initialization command words :-

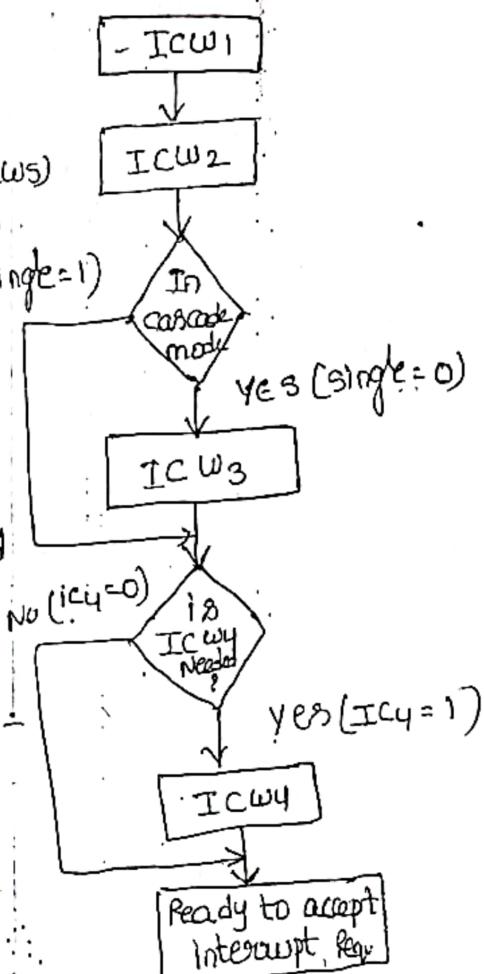
Before it starts functioning, the 8259A must be initialized by writing two or four command words into the respective command word registers. These are called as initialization command words.

Initialization command word 1 (ICW1) :-

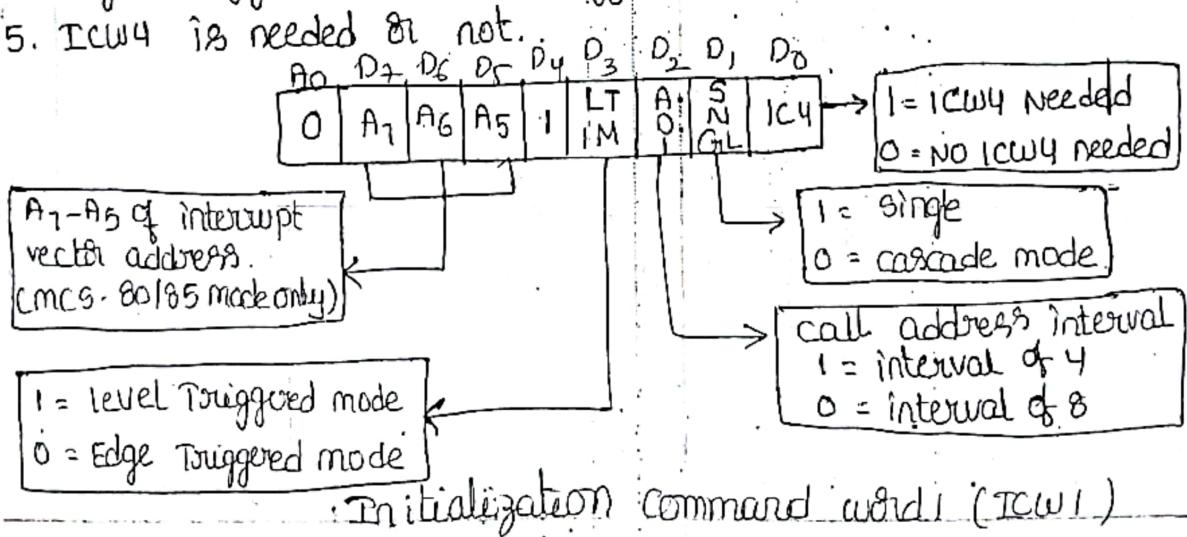
A write command issued to the 8259 with $A_0 = 0$ and $D_4 = 1$ is interpreted as ICW1, which starts the initialization sequence.

It specifies:-

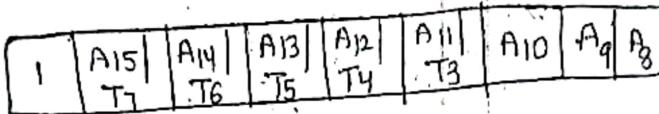
1. Single or multiple 8259 As in the system.
2. 4 or 8 bit interval between the interrupt vector locations.
3. The address bits A_7-A_5 of the call instruction.
4. Edge triggered or level triggered interrupts.
5. ICW4 is needed or not.



Initialization sequence of 8259A.



Initialization command word 2 (ICW2) :- A write command ICW1, with $A_0 = 1$ is interpreted as ICWA. This is used to load the high order byte of the interrupt vector address of all the interrupts.



A₁₅-A₈ of interrupt vector address (mcs80/85 mode).

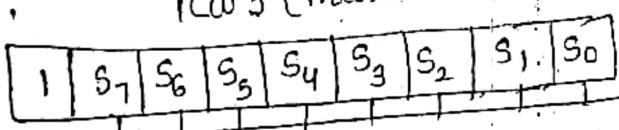
T₇-T₃ of interrupt vector address (8086/8088 mode).

Initialization command word 2 (ICWA)

Initialization command word 3 (ICW3) :-

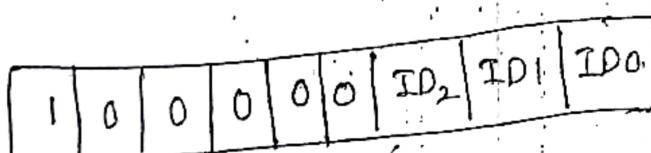
ICW3 is required only if there is more than one 8259 in the system and if they are cascaded. An ICW3 operation loads a slave register in the 8259. The format of the byte to be loaded as an ICW3 for a master or a slave. For master each bit in ICW3 is used to specify whether it has a slave 8259 attached to it on its corresponding IR input. For slaves, bits D₀-D₂ of ICW3 are used to assign a slave identification code to the 8259.

ICW3 (master device)



1 = IR input has a slave
0 = IR input does not have a slave

ICW3 (slave device)



Initialization command word 3 (ICW3).

Initialization command word 4 (ICW4) :-

It is loaded only if the D₀ bit of ICW1 (IC4) is set. The format of ICW4 is shown in below figure.

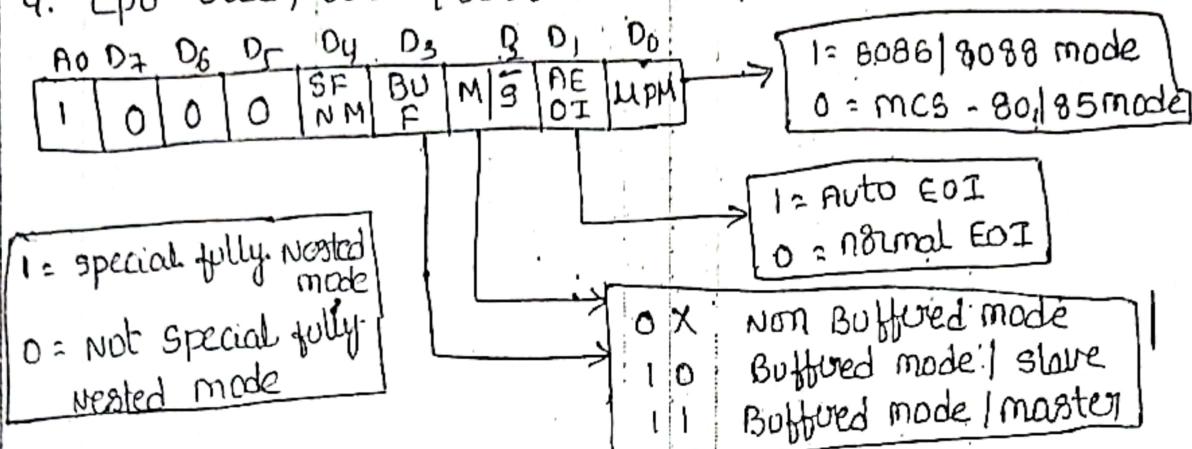
It specifies:-

- 1) whether to use special fully nested mode, & non special fully nested mode.

Slave ID

000	0	100	4
001	1	101	5
010	2	110	6
011	3	111	7

- whether to use buffered mode or non buffered mode.
- whether to use automatic EOI or normal EOI.
- CPU used, 8086 | 8088 & 80810.

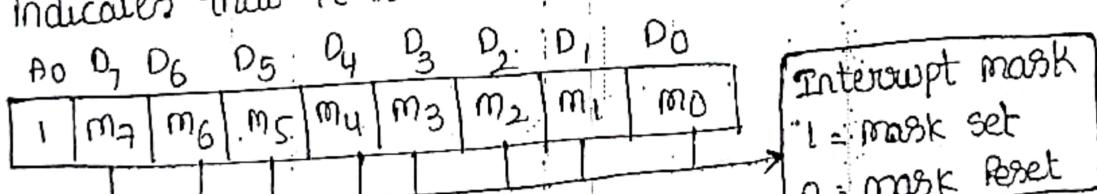


initialization command word 4 (ICW4):

After initialization, the 8259 is ready to process interrupt requests. However, during operation, it might be necessary to change the mode of processing the interrupts. Operation command words (OCWs) are used for this purpose. They may be loaded anytime after the 8259's initialization to dynamically alter the priority modes.

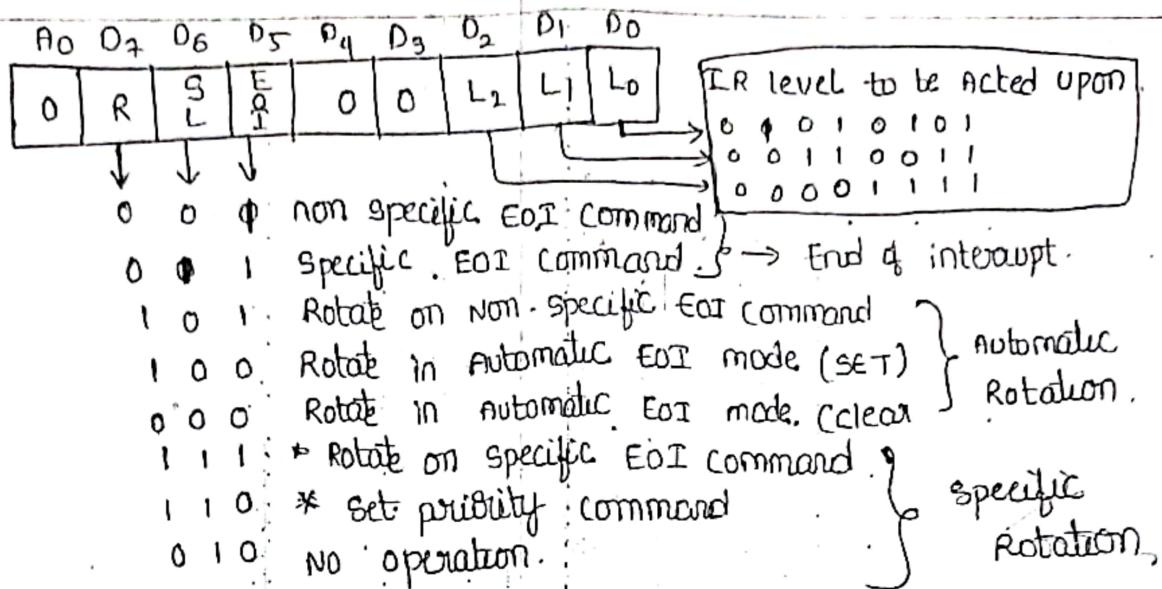
operation command word 1 (OCW1): - A write command to the 8259 with A0 = 1 (after ICW1a) is interpreted as OCW1. OCW1 is used for enabling or disabling the recognition of specific interrupt requests by programming the IMR.

M=1 indicates that the interrupt is to be masked.
M=0 indicates that it is to be unmasked.

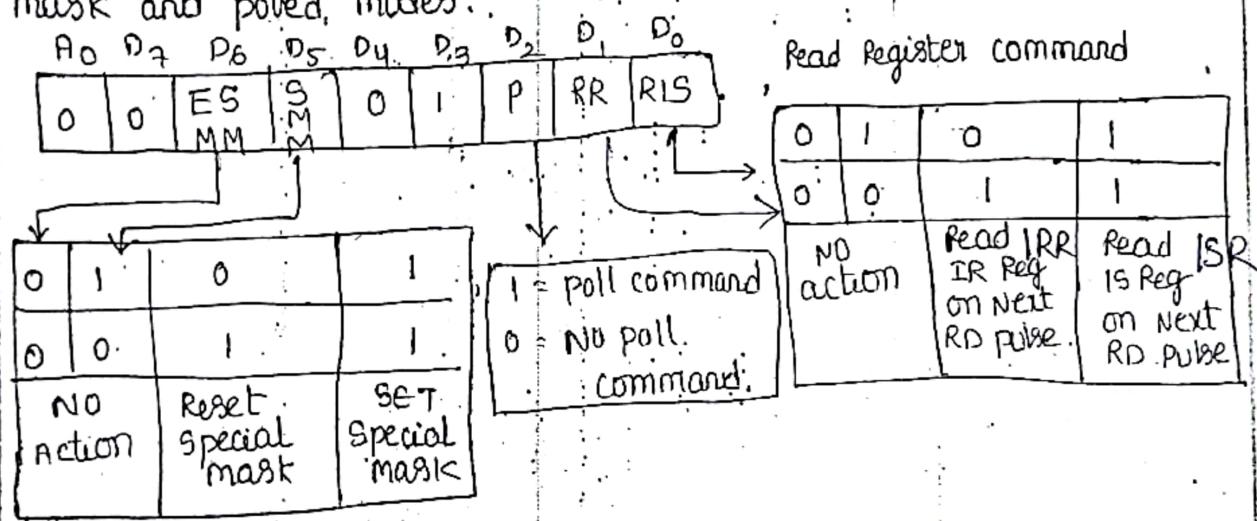


operation command word 2 (OCW2):

A write command with A0 = 1 and D4-D3 = 00 is interpreted as OCW2. The R (rotate), SL (select-level), EOI bits control the Rotate and End of interrupt modes and comb of the two L2-L0 are used to specify the interrupt level to be acted upon when the SL bit is active.

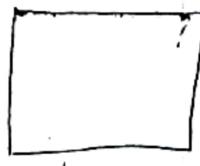
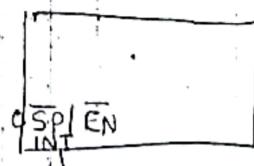
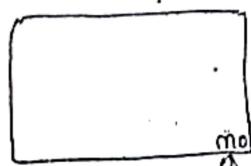


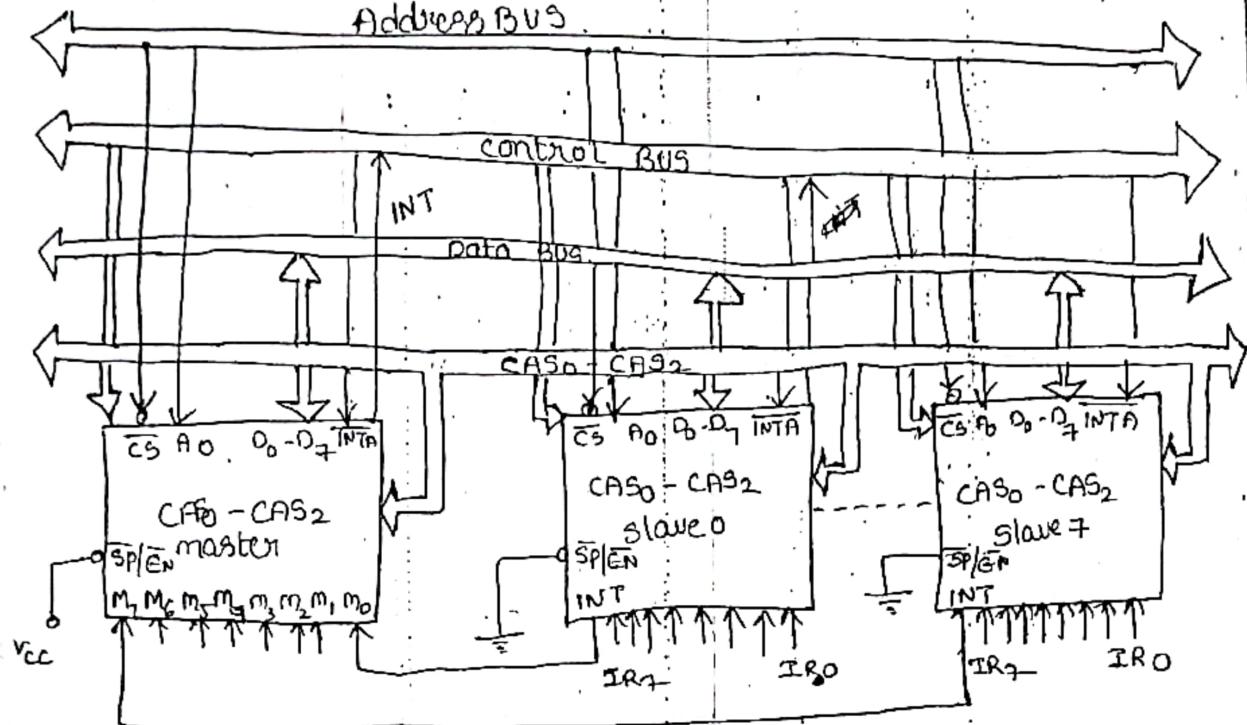
operation command word 3 (OCW3) :- OCW3 is used to read the status of the Registers, and to set or reset the special mask and polled modes..



8259 in cascaded mode :-

ix





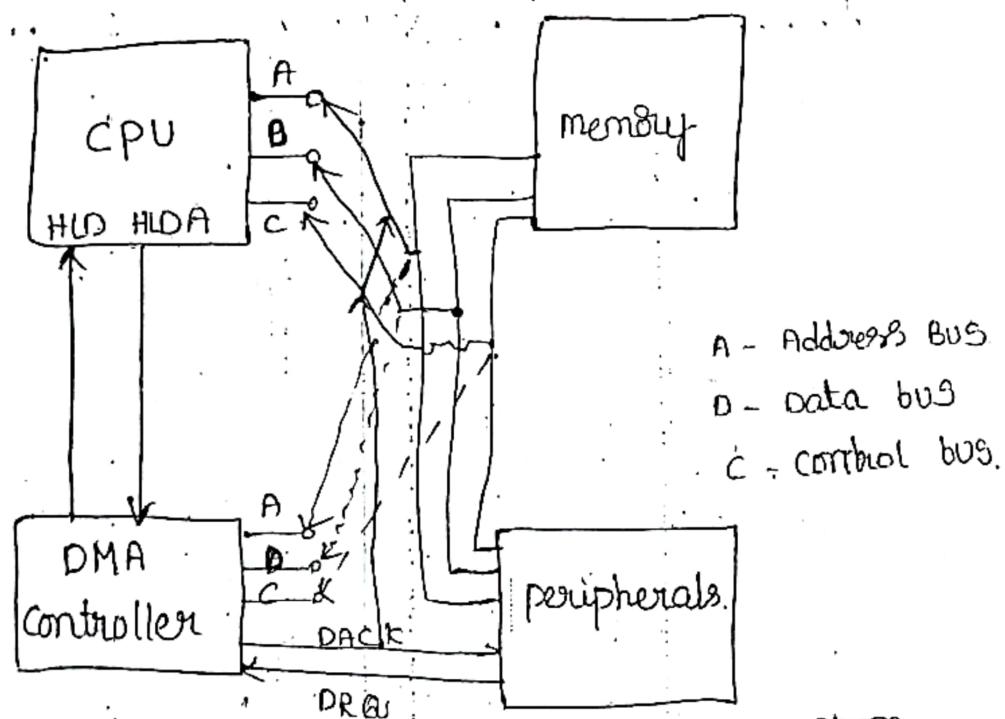
8259A cascaded mode

cascade mode :- The 8259A can be connected in a system containing one master and eight slaves (maximum) to handle upto 64 priority levels. The master controls the slaves using $CAS_0 - CAS_2$ which act as chip select inputs for slaves.

In this mode, the slave INT outputs are connected with master IR inputs. When a slave request line is activated and acknowledged, the master will enable the slave to release the vector address during the second pulse of \overline{INTA} sequence. The cascade lines are normally low and contain slave address codes from the trailing edge of the first \overline{INTA} pulse to the trailing edge of the second \overline{INTA} pulse. The EOI command must be issued twice, one for master and the other for the slave.

DMA Controller :-

The Direct memory Access or DMA mode of data transfer is the fastest amongst all the modes of data transfer. In this mode, the device may transfer data directly to / from memory without any interference from the CPU. The device requests the CPU (through a DMA controller) to hold its data, address and control bus, so that the device may transfer data directly to / from memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

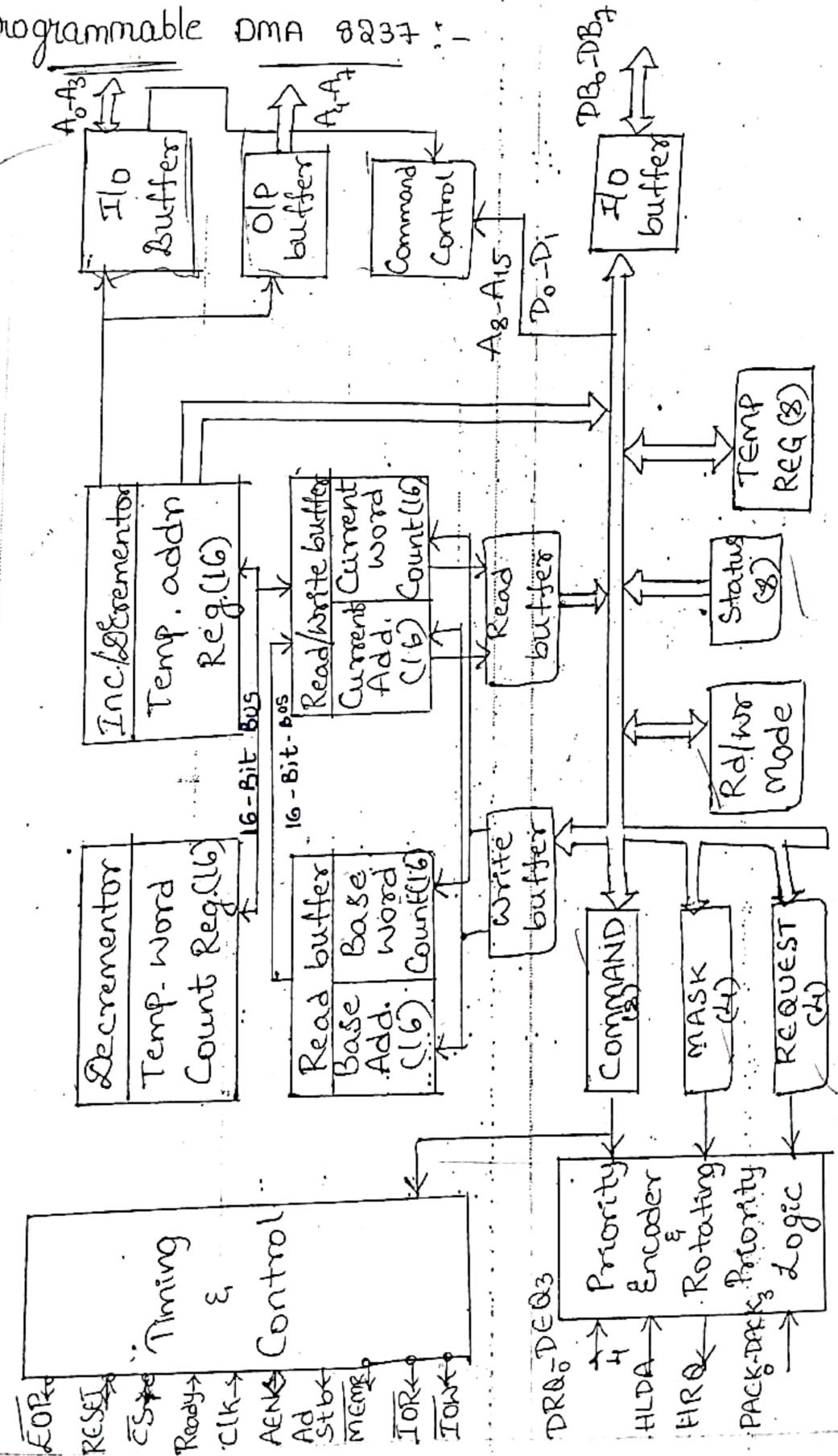


A Typical DMA Controller with a system.

Once a DMA controller is initialized by a CPU properly, it is ready to take control of the system bus on a DMA request, either from a peripheral or itself. The DMA controller sends a HOLD request to the CPU and waits for CPU to assert the HLDA signal. Once the HLDA signal goes high, the DMA controller activates the ACK signal.

to the requesting peripheral and gains the control of the system bus. The DMA controller is the sole master of the bus till the DMA operation is over.

programmable DMA 8237 :-



An Advanced programmable DMA controller 8237, which provides a better performance, compared to 8257. This is capable of transferring a byte or a byte of data between system memory and peripherals in either direction. memory to memory data transfer facility is also available in this peripheral. The 8237 also supports four independent DMA channels which may be expanded to any number by cascading more number of 8237.

The Internal Block diagram of 8237 is shown in the figure. The 8237 contains three basic blocks of its operational logic.

- The program command control block decodes the various commands given to the 8237 by the CPU before servicing a DMA request. It also decodes the mode control word used to select the type of the programmed DMA Transfer.
- The timing and control block generates the internal timings and external control signals.
- The priority encoder block resolves priority between the DMA channels requesting and services simultaneously.

Register organisation of 8237:-

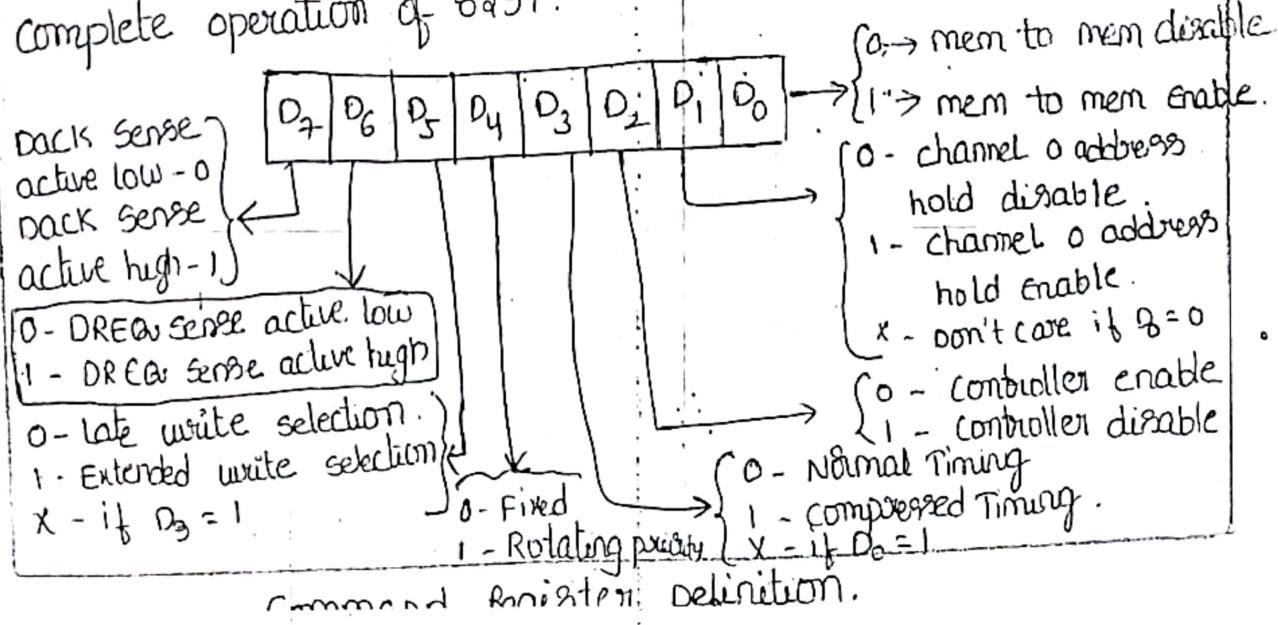
8237 houses a set of twelve types of registers. Some of these registers are present in each of the four channels while the remaining are common for all the channels. Considering the multiple existence of the registers, there are 25 registers in 8237 which are described below.

Current address Register:- Each of the four DMA channels of 8237 has a 16-bit current address register that holds the current memory address, being accessed during the DMA Transfer. The address is automatically incremented or decremented after each transfer and the resulting address value is again stored in the current address register. This can be byte-wise programmed by the CPU, lower byte first and the higher byte later.

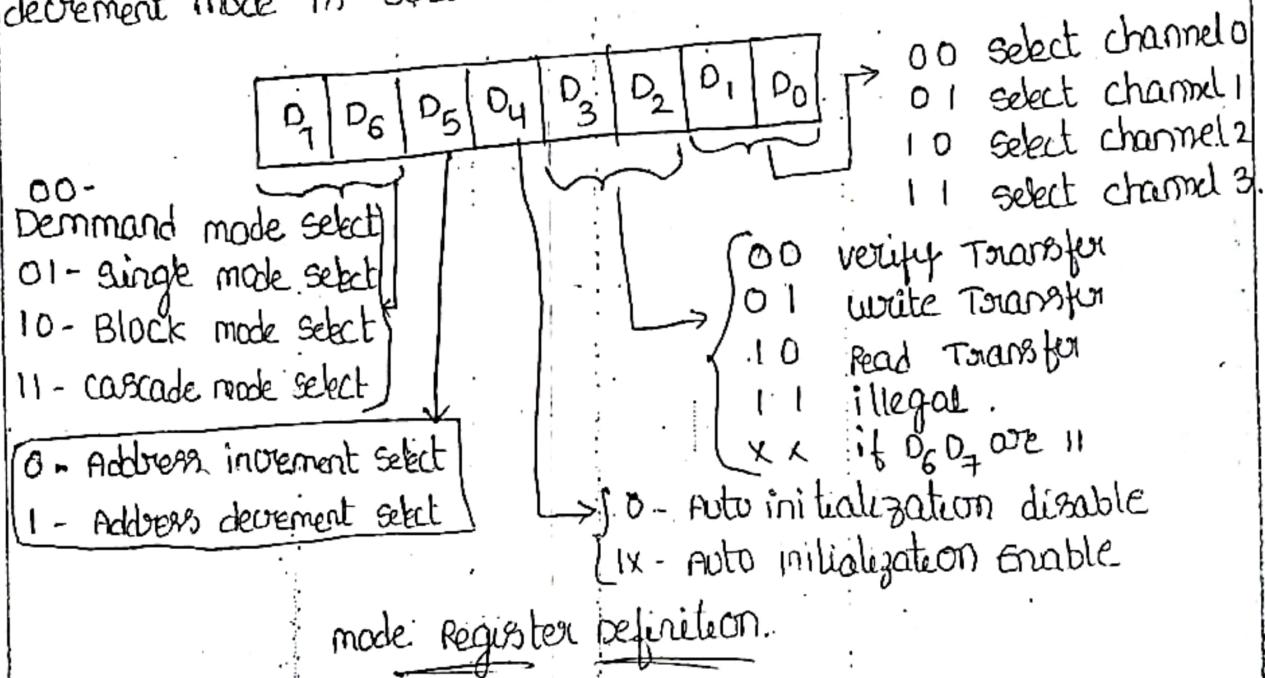
Current word Register:- Each channel has a 16-bit current word register that holds the number of data bytes transferred to be carried out. The word count is decremented after each transfer and the new value is again stored back to the current word register. When the count becomes zero an EOP signal will be generated. This can be written in successive bytes by the CPU, in program mode.

Base address and Base word count Registers:- Each channel has a pair of these registers. These maintain an original copy of the respective initial current address register and current word register (before incrementing or decrementing), respectively.

Command Register:- This 8-bit register controls the complete operation of 8237.

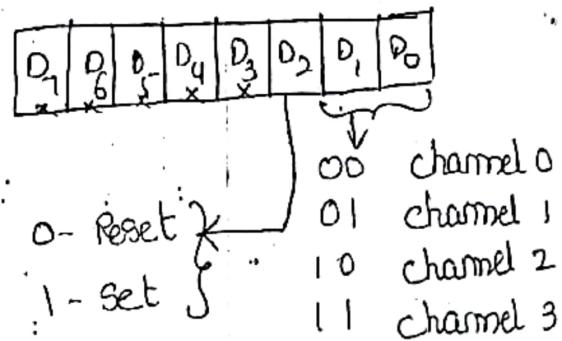


Mode register :- Each of the DMA channel has an 8-bit mode register. This is written by the CPU in program mode. Bits 0 and 1 of the mode register determine which of the four channel mode register is to be written. The bits 2 and 3 indicates the type of DMA Transfer. Bit 4 of the mode register indicates whether auto-initialization is selected or not. While bit 5 indicates whether address increment or address decrement mode is selected.



Request Register :-

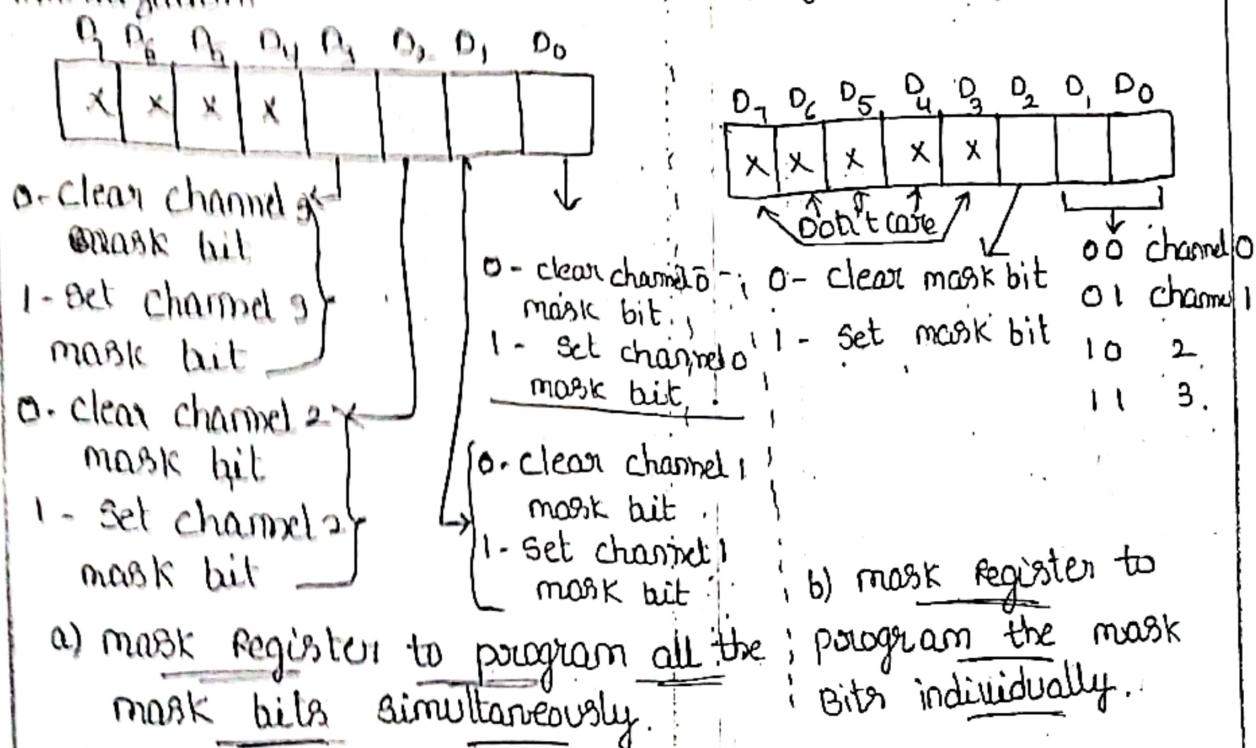
Each channel has a request bit associated with it, in the request register. These are non-maskable and subject to prioritization by the priority resolving network of 8237.



Request Register.

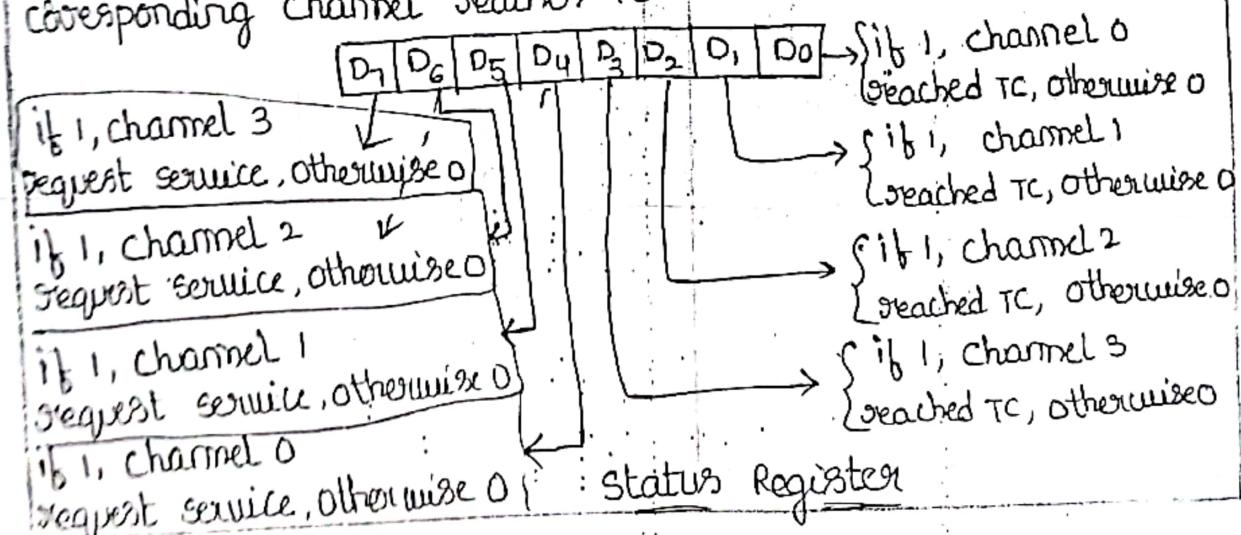
Mask Register :- Sometimes it may be required to disable a DMA request of a certain channel. Each of the four channel has a mask bit which can be set under program control to disable the incoming DREQ Requests at the specific channel.

This bit is set when the corresponding channel produces an EOP signal, if the channel is not programmed for auto-initialization.



Temporary Register :- The temporary register holds data during memory-to-memory data transfers. After the completion of the transfer operation, the last word transferred remains in the temporary register till it is cleared by a reset operation.

Status Register :- The status register keeps the track of all the DMA channel pending requests and the status of their terminal count. The D₀-D₃ are updated every time, the corresponding channel reaches TC or an external EOP occurs.



Transfer modes of 8237 :- If the CPU acknowledges the hold request on HLDA, the 8237 enters an active cycle. In the active cycle, the actual data transfer takes place in one of the following transfer modes, as is programmed.

Single Transfer mode :- In this mode, the device transfers only one byte per request. The word count is decremented and the address is decremented or incremented after each such transfer. The terminal count (TC) state is reached, when the count becomes zero. For each transfer, the DREQ must be active until the DACK is activated, in order to get recognized.

Block Transfer mode :- In this mode, the 8237 is activated by DREQ to continue the transfer until a TC is reached or a block of data is transferred. The transfer cycle may be terminated due to EOP which forces terminal count (TC).

Demand Transfer mode :- In this mode, the device continues the transfer until a TC is reached or an external EOP is detected or the DREQ signal goes inactive. Thus, a transfer may exhaust the capacity of data transfer of an I/O device.

Cascade mode :- In this mode, more than one 8237 can be connected together to provide more than four DMA channels. The HREQ and HLDA signals from additional 8237s are connected with DREQ and DACK pins of a channel of the host 8237 respectively.

Memory to memory Transfer :- To perform the transfer of a block of data from one set of memory address to another one, this transfer mode is used. Programming the corresponding mode bit in the command word, sets the channel 0 and 1 to operate as source and destination channels, respectively.

Intel 8251 USART :- (universal synchronous asynchronous Receiver and transmitter).

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To implement serial communication in up system we need basically two devices. 1) parallel to serial converter and 2) serial to parallel converter.

To transmit byte data it is necessary to convert byte into eight serial bus. This can be done by using the parallel to serial converter. Similarly at the reception these serial bits must be converted into parallel 8 Bit data. The serial to parallel converter is used to convert serial data bits into the parallel data.

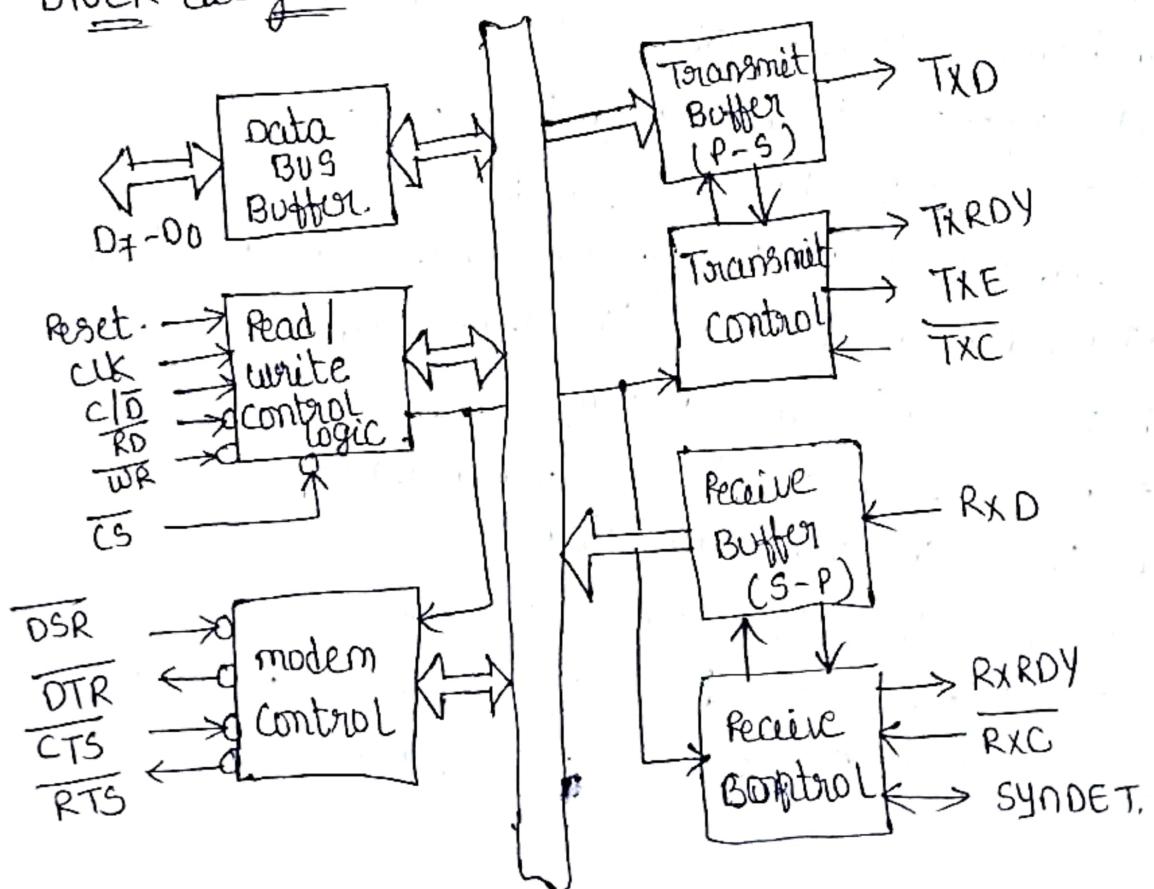
The devices are designed for this purpose are called universal synchronous Asynchronous receiver and transmitter. UART \rightarrow 8250, USART \rightarrow 8251.

Features :-

1. The intel 8251A is an universal synchronous and asynchronous communication controller.
2. It supports standard Asynchronous protocol with.
 - a). 5 to 8 Bit character format.
 - b) odd, even or no parity generation and detection.
 - c) Baud rate from DC to 19.2 k baud.
 - d) False start bit detection.
 - e) Automatic break detect and handling.
 - f) Break character generation.
3. It has built in baud rate generator.
4. It supports standard synchronous protocol with a) 5 to 8 Bit character format.

- b) internal or external character synchronization.
 - c) automatic sync insertion.
 - d) Baud rate from DC to 64 k baud.
5. It allows full duplex transmission and reception.
6. It provides double buffering of data both in the transmission selection and the receiver section.
7. It provides error detection logic, which detects parity, overrun and framing errors.
8. It has modem control logic, which supports basic data set control signals.
9. It provides separate clock inputs for receiver and transmitter.
10. It is compatible with an extended range of Intel microprocessors.
11. It is fabricated in 28 pin DIP package

Block diagram :-



The Block diagram of 8251 it includes: Data bus Buffer, Read/Write control logic, modem control, Transmit Buffer, Transmit Control, Receiver Buffer and Receiver Control.

Data Bus Buffer:- This tri-state, bi-directional, 8-Bit Buffer is used to interface 8251 to the system data bus (up) along with the data, control word, command words and status information are also transferred through the Data Bus Buffer.

Read/write control logic:- This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the Control word register and Command word register that stores the various control formats for the device functional.

Transmit Buffer:- The transmit buffer accepts parallel data from the CPU, adds the appropriate framing information, serializes it, and transmits it on the TxO pin on the falling edge of TxC.

It has two registers - a Buffer register to hold eight bits and an output register to convert eight bits into a stream of serial bits.

In the synchronous mode the transmitter always adds start bit, it also adds an optional even or odd parity bit, and either 1, 1½ or 2 stop bits. In synchronous mode there is no parity, start and stop bits.

Transmit control:-

It manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally.

TxDY (Transmit Ready) :- This output signal indicates CPU that buffer register is empty and the USART is ready to accept a data character. This signal is reset when a data byte is loaded into the buffer register.

TXE (Transmitter Empty) :- This is an output signal. A high on this line indicates that the output buffer is empty.

TxC (Transmitter clock) :- This clock controls the rate at which characters are transmitted by USART. In the synchronous mode TxC is equivalent to the baud rate, and is supplied by the modem.

Receiver Buffer :- The receiver accepts serial data on the RXD line, converts the serial data to parallel format.

8251 is in the asynchronous mode and it is ready to accept a character, if looks for a low level on the RXD line.

- when it receives the low level, it assumes that it is a start bit and enables an inter counter.
- After successful reception of a start bit the 8251 receives data, parity and stop bits and then transfers the data on the receiver input register. The data is then transferred into the receiver buffer register.

In the synchronous mode the receiver simply receives the specified number of data bits and transfers them to the receiver input register and then to the receiver buffer register.

Receiver control :- It manages all receiver-related activities. Along with data reception, it does start bit detection, parity error detection, framing error detection, synch detection and break detection.

RXRDY (Receiver ready) :- This is an output signal. It goes high when the USART has a character in the Buffer register and is ready to transfer it to the CPU.

RXC (Receiver clock) :- This clock controls the rate at which the character is to be received by USART in the synchronous mode. RXC is equivalent to the baud rate. In asynchronous mode RXC is 1, 16 or 64 times the baud rate.

modem control :- The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any modem.

DSR :- Data set ready :- This input may be used as a general purpose one bit inverting input port. This is normally used to check if the data set is ready when communicating with a modem.

DTR :- (Data terminal Ready) :- This output may be used as a general purpose one bit inverting output port. This is used to indicate that the device is ready to accept data when the 8251 is communicating with a modem.

RTS :- (Request to send data) :- This signal is used to communicate with a modem. This output may be used as a general purpose one bit inverting output port that can be programmed low to indicate the modem the device (receiver) is ready to receive a data byte from the modem.

CTS :- (Clear to send) :- If the clear to send the input line is low, the 8251 A is enabled to transmit the serial data, provided the enable bit in the command byte is set to '1'.

SYNDET / BD :- (Sync detect / Break detect) :- In the synchronous mode for detecting sync characters and may be used as either input or output.

→ 8251 control words :-

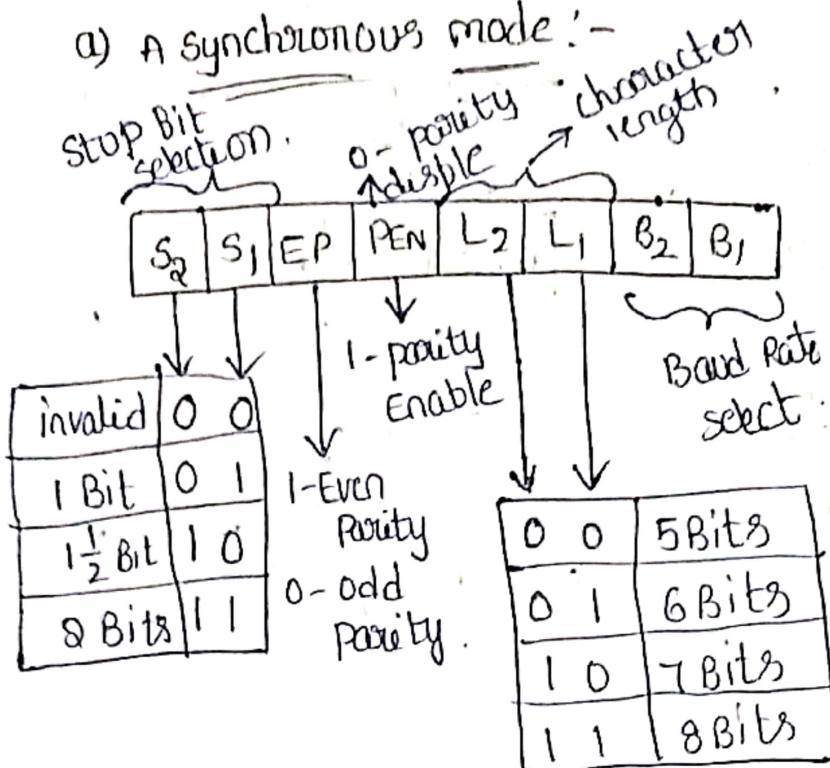
The control words of 8251 A are divided into two functional types:-

1. mode instruction control word.
2. command instruction control word.

1. mode instruction control word :-

The 8251 A can be programmed to operate in its various modes using its mode control words.

a) A synchronous mode :-

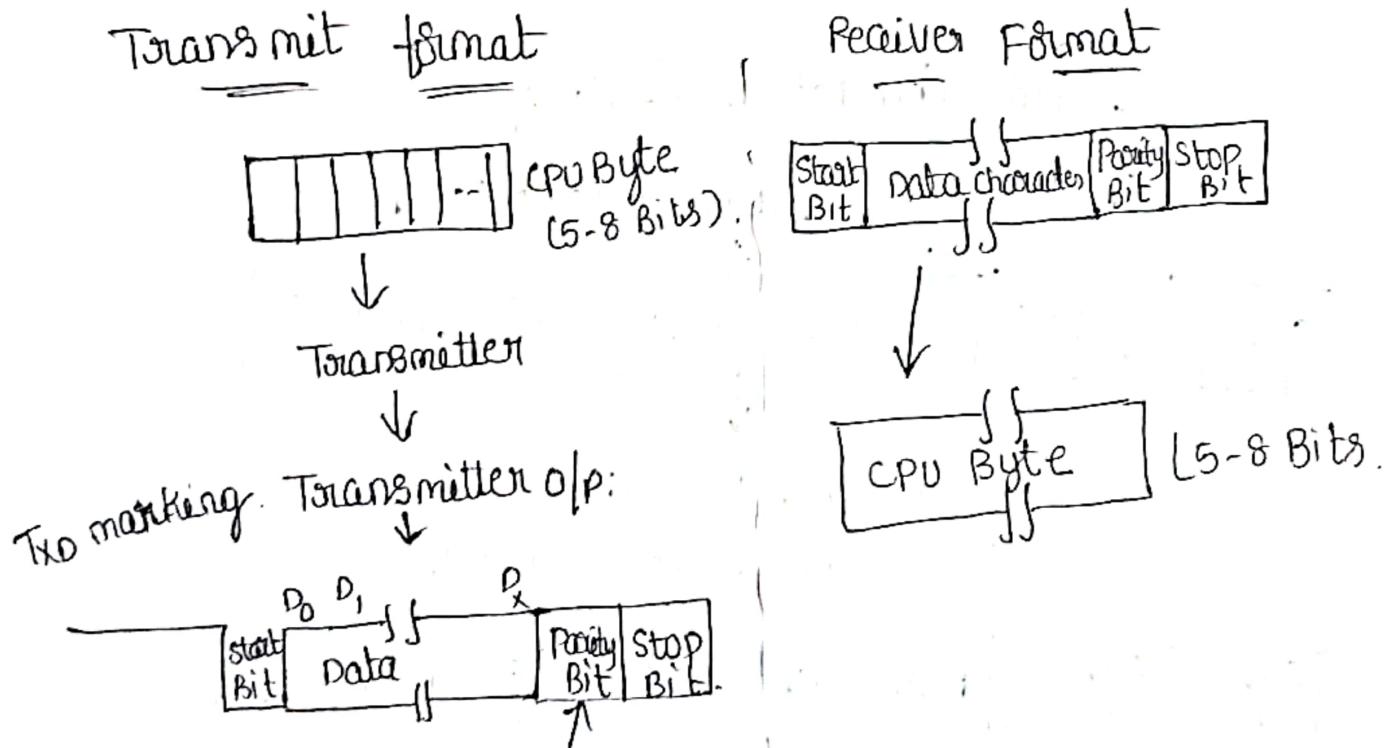


B₂ B₁

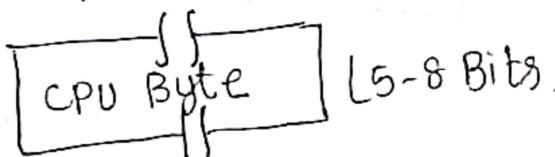
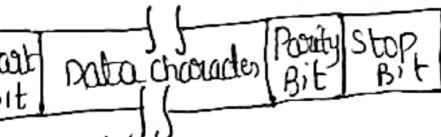
0 0	Synchronous mode
0 1	1x Asynchronous
1 0	16x Asynchronous
1 1	64x Asynchronous

A synchronous mode Transmit and receive Format

Transmit format

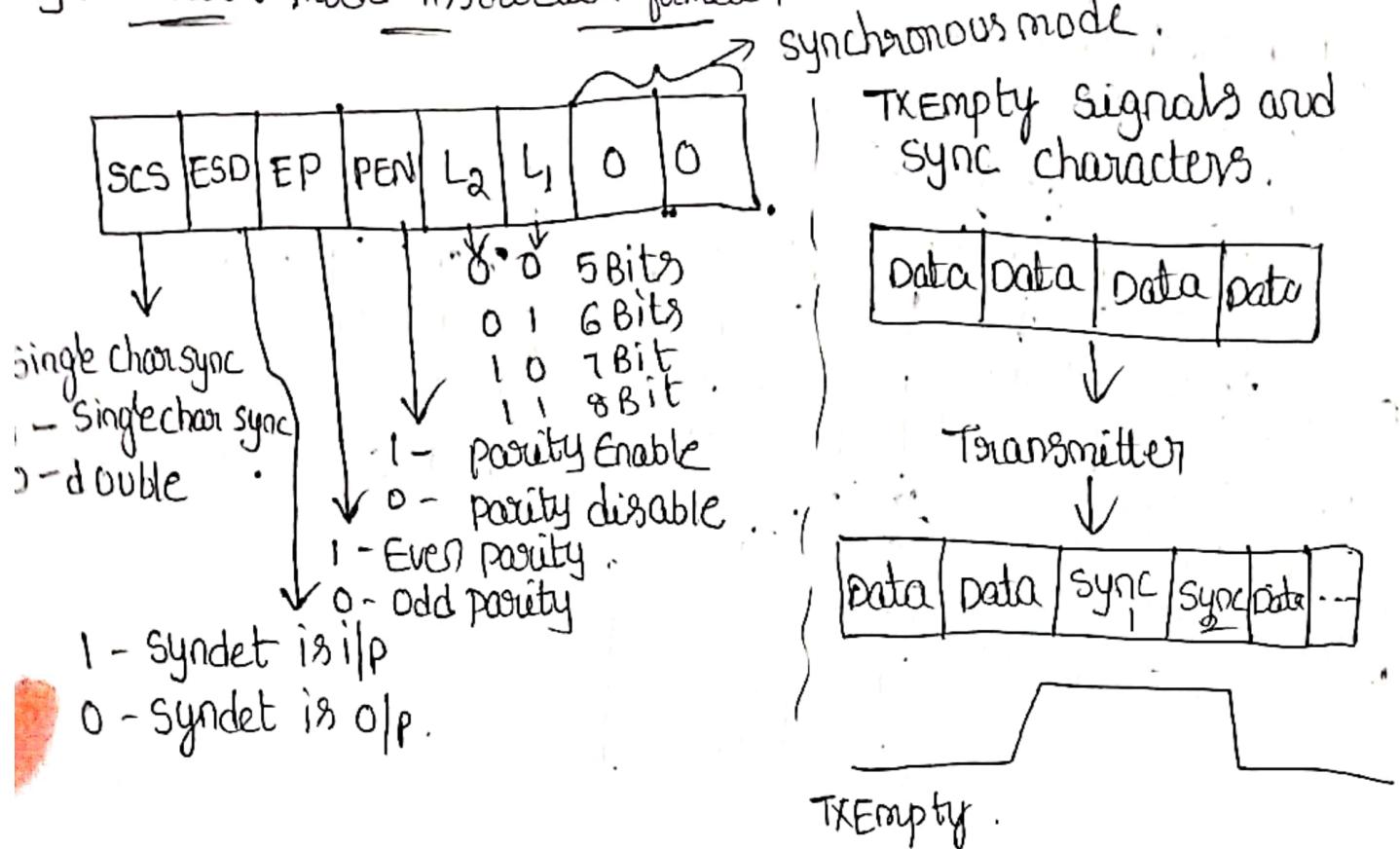


Receiver Format

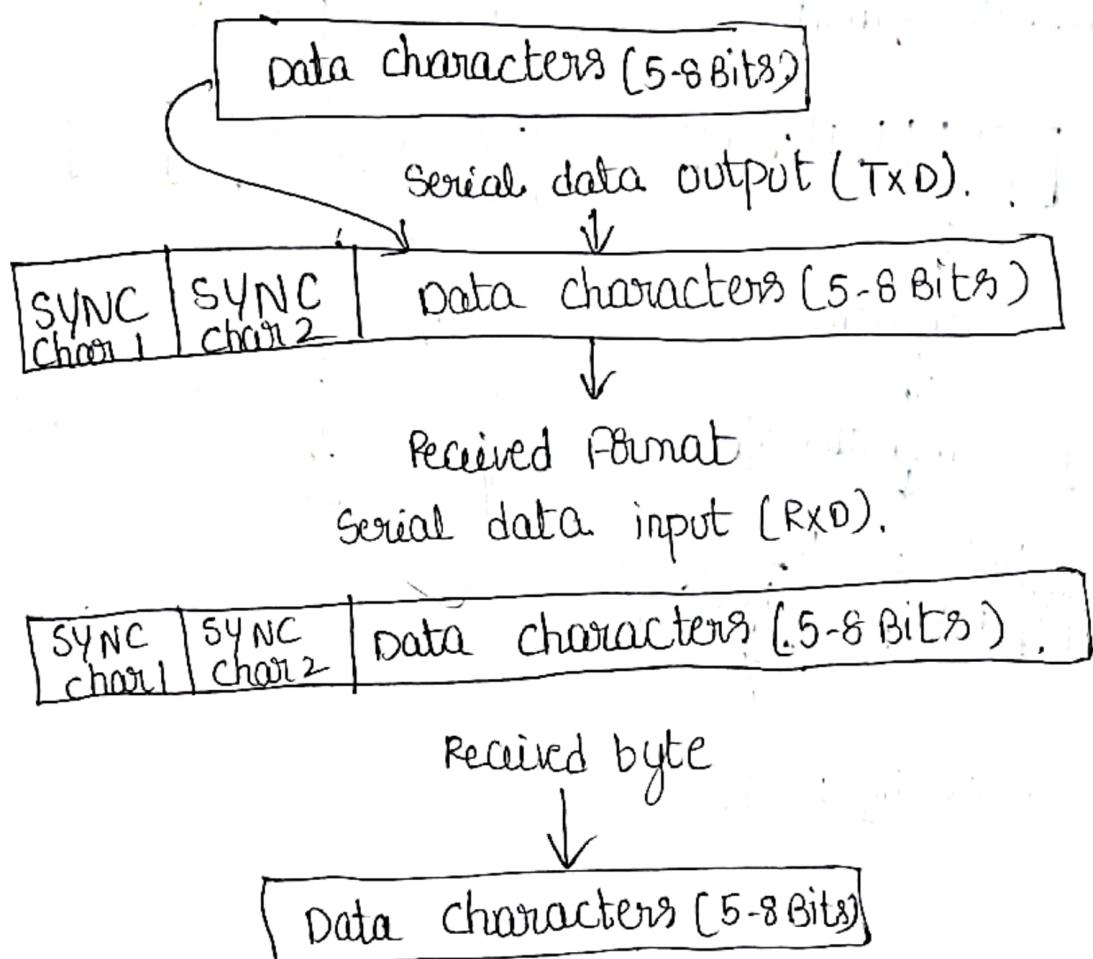


Generate by 8251.

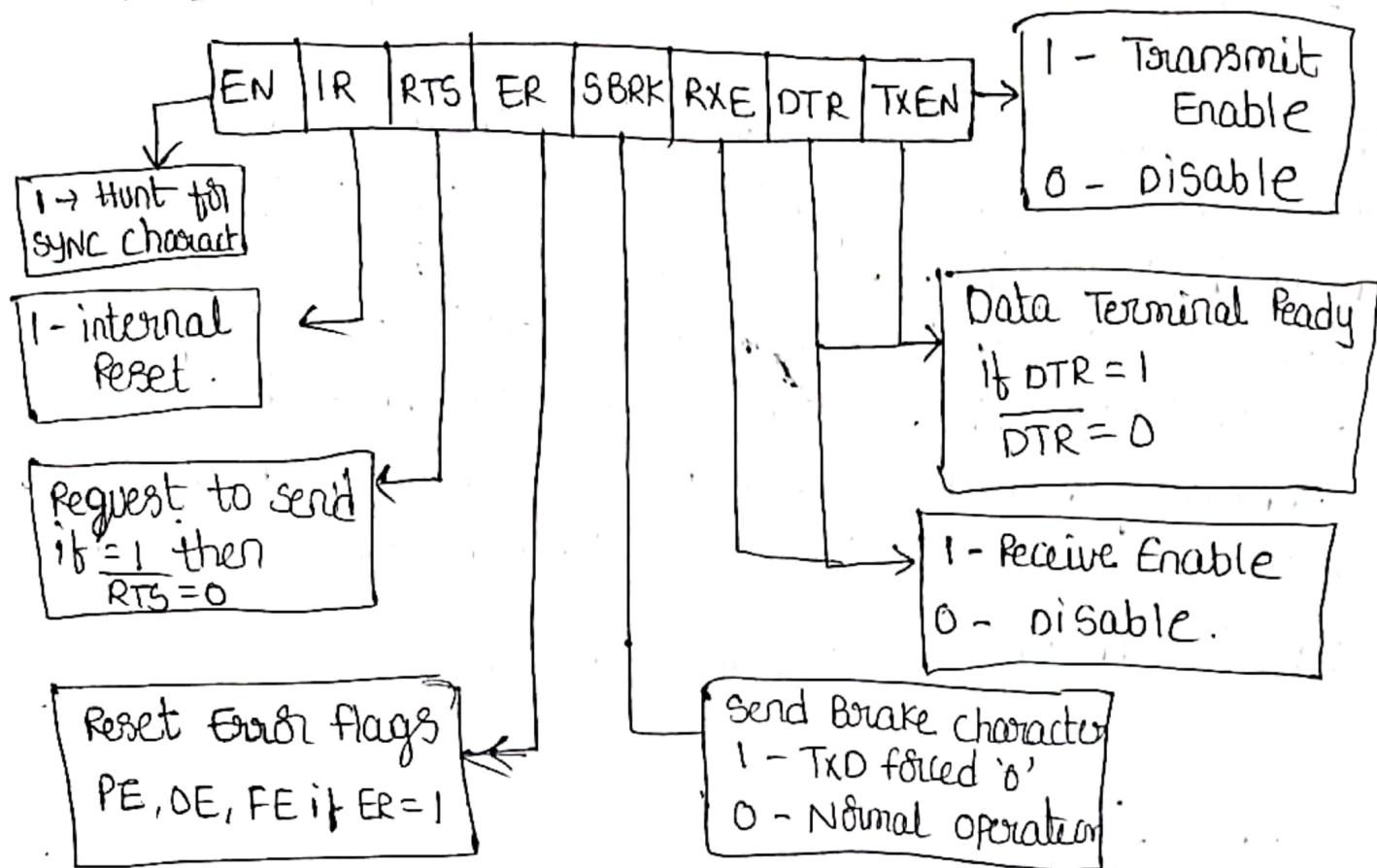
Synchronous mode instruction format :-



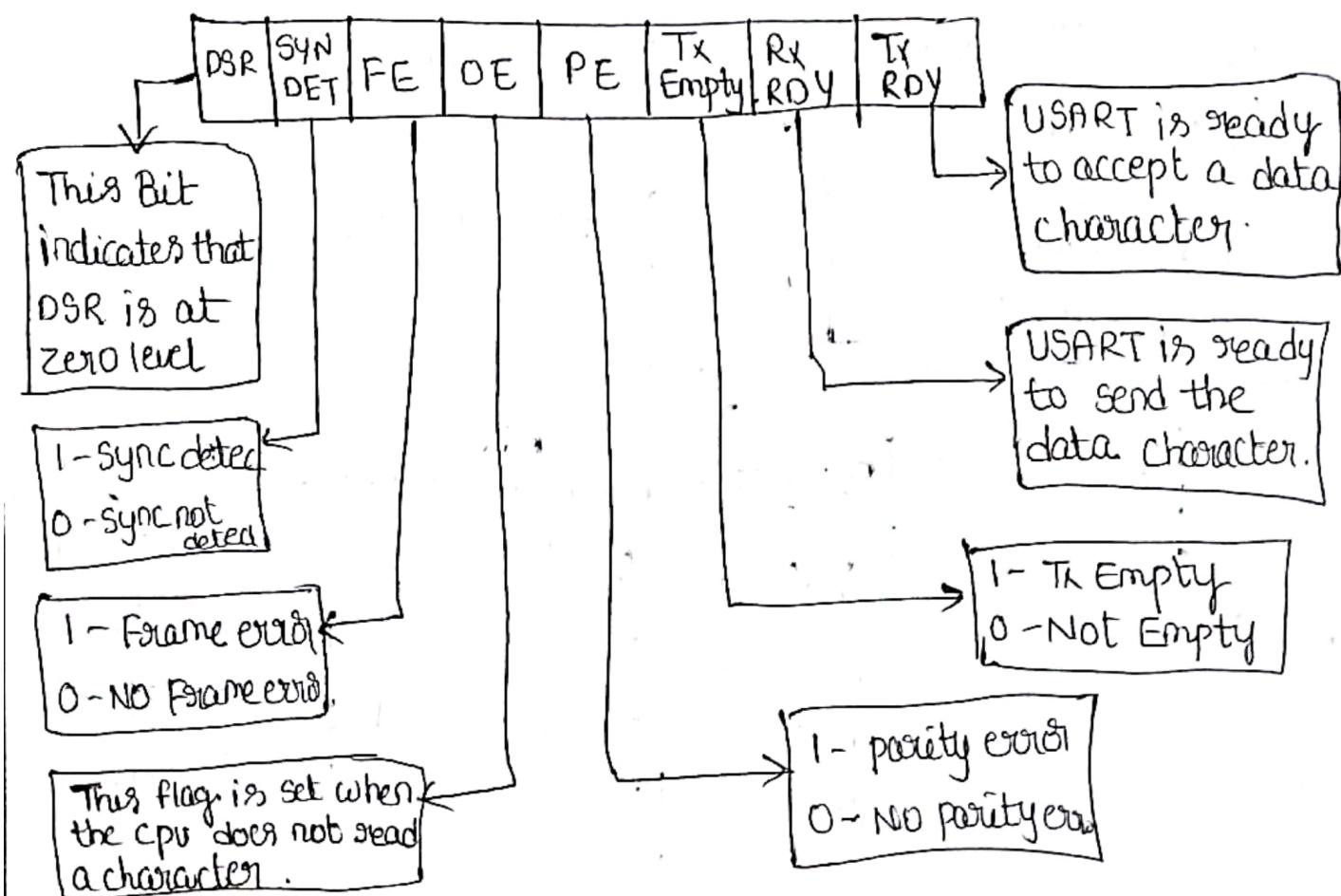
Synchronous mode Transmit and Receive Format



Command instruction format :-



Status read instruction Format

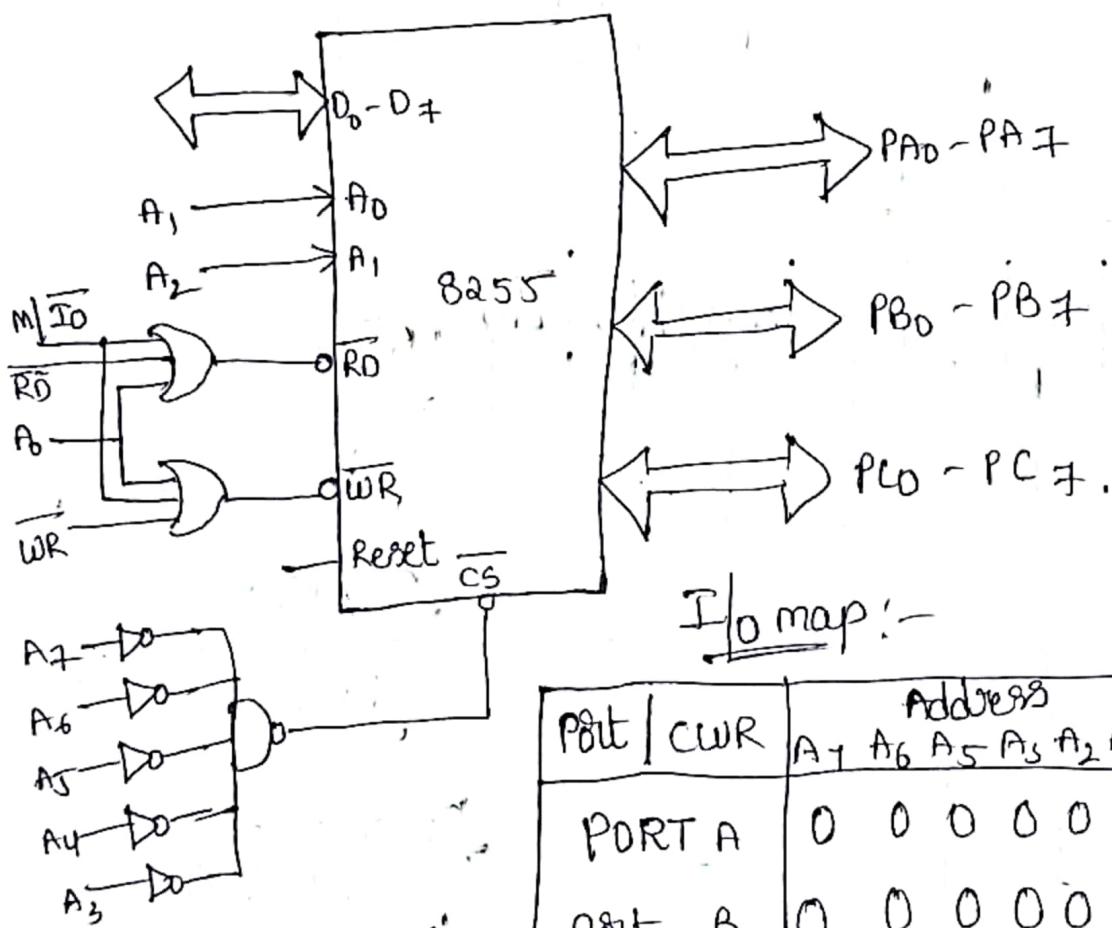


Interfacing:-

Interfacing 8255 to 8086 :- (I/O mapped I/O).

The 8086 has four special instructions IN, INS, OUT and OUTS to transfer data through the Input/Output ports in I/O mapped I/O system. M/I_O signal is used to generate separate addresses for memory and Input/Output. Only 256 (2^8) I/O addresses can be generated when direct addressing method is used. By using indirect address method this range can be extended upto $65536^{(2^{16})}$ addresses.

Direct addressing :- (I/O mapped I/O)



Port / CWR	Address A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ , A ₀	Address
PORT A	0 0 0 0 0 0 0	00H
PORT B	0 0 0 0 0 1 0	02H
PORT C	0 0 0 0 1 0 0	04H
CWR	0 0 0 0 1 1 0	06H