UNIT-V
PART-1 : INTRODUCTION TO PROGRAMMABLE DSPs

INTRODUCTION

- A digital signal processor (DSP) is a specialized microprocessor designed specifically for digital signal processing, generally in real time computing.
- They contain special architecture and instruction set so as to execute computation-intensive DSP algorithms more efficiently.
- The programmable digital signal processors are designed with features that are specifically required for DSP applications.
- Low power requirement, cost, real time I/O capability, availability of high speed on-chip memories.

TYPES OF PDSPs

1. **General purpose DSPs:**

- These are basically high speed microprocessors with architecture and instruction sets optimized for DSP operations.
- They include
  - Fixed point processors such as Texas instruments TMS320C5X, TMS320C54X and
  - Motorala DSP563X and
  - Floating point processors such as Texas instruments

    TMS320C4X, TMS320C67XX, and analog devices ADSP21XXX.

2.Special purpose DSPs:

- This type of processors consist of hardware

  (i) designed for specific DSP algorithms such as FET,

  (ii) designed for specific applications such as PCM and filtering.
- Examples for special purpose DSPs are MT93001, PDSP16515A and UPDSP16256.

Applications of P-DSPs are:

- communication systems
- audio signal processing
- control and data acquisition
- biometric information processing
- image/video processing, etc

ADVANTAGES

1. The DSP processors supports fast processing of arrays.
2. require single clock cycle to execute instructions.
3. support parallel execution of instructions.
4. have separate data and program memories.
5. support simultaneous fetching of multiple operands.
6. have three separate computational units. Arithmetic logic unit, multiplier and accumulator, and shifter.
7. consist of powerful interrupt structure and timers.
8. have multiprocessing ability.
9. have on chip program memory and data memory.

MULTIPLIER AND MULTIPLIER ACCUMULATOR (MAC)

- Array multiplication is one of the most common operations required in digital signal processing applications.
- An example is: convolution and correlation which require array multiplication operation.

Two approaches

1. A dedicated MAC unit may be implemented in hardware, which integrates multiplier and accumulator in a single hardware unit. Example for this approach is Motorola DSP5600X.
2. Have separate multiplier and accumulator. Example for this approach, is TIDSP320C5X. In this approach, the output of the multiplier is stored into the product register and the content of the product register is added to accumulator register in the central ALU.

In both the approaches, the MAC operation (Mandatory requirement of PDSP) can be completed in one clock cycle.

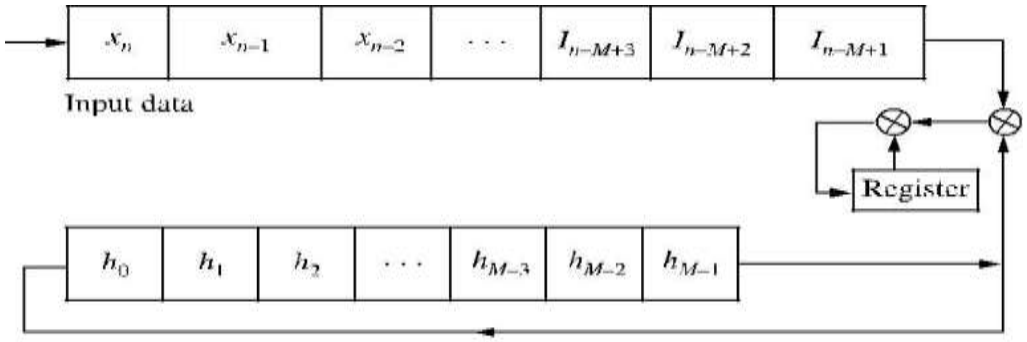
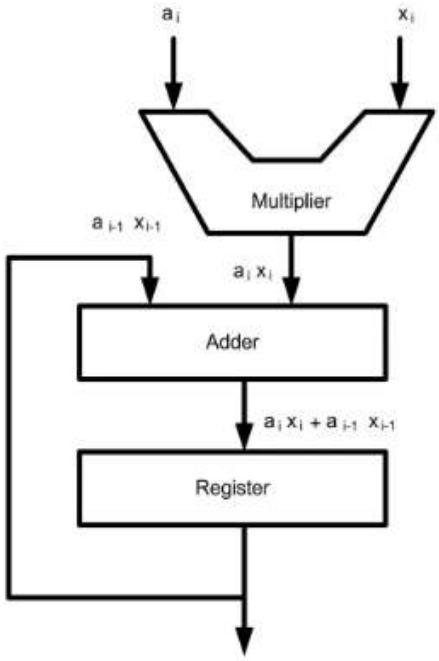


Fig 1: Implementation of convolver with single multiplier/adder

- Convolution is the fundamental and important operation in signal processing .
- Multiply-Accumulate operation is widely used in Convolution.
- Computes the product of two numbers and adds that products to an accumulator.
- Consists of a multiplier followed by an accumulator that contains the sum of the previous consecutive products .

Single-Cycle MAC unit



$$\sum_{i=0}^{n}(a_i x_i)$$

Can compute a sum of *n*-products in *n* cycles

MODIFIED BUS STRUCTURES AND MEMORY ACCESS SCHEMES IN P-DSPs

- The MACD instruction, that is, the MAC operation with data move requires four memory accesses per instruction cycle. The four memory accesses/clock period required for the MACD instructions are as follows:

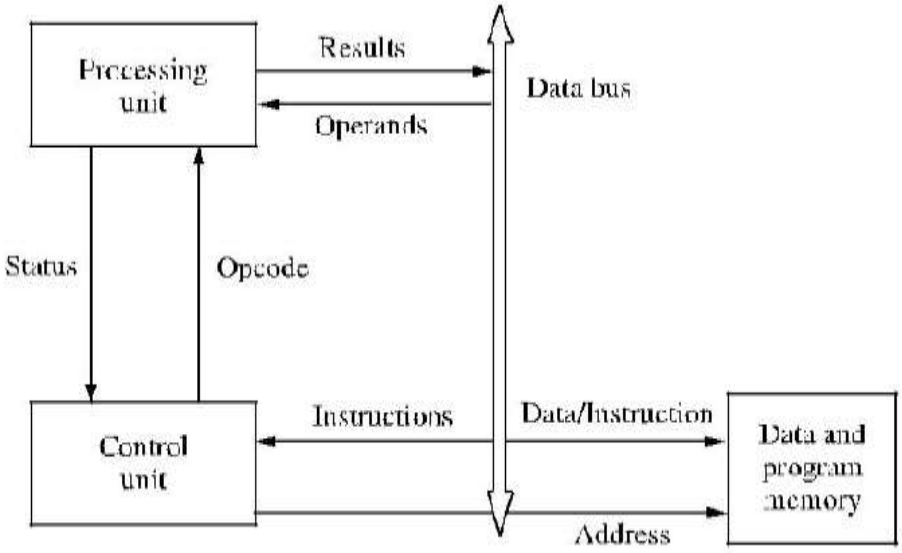
  1. Fetch the MACD instruction from the program memory.

2. Fetch one of the operands from the program memory(pma).

3. Fetch the second operand from the data memory(dma).

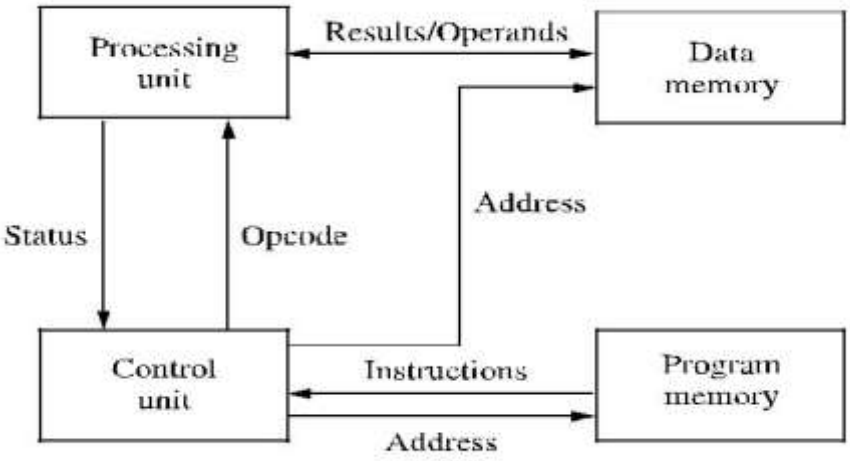
4. Write the content of the data memory with address ‘dma’ into the location with the address ‘dma + 1’.

Von Neumann architecture



- In this architecture, the CPU can be either reading an instruction or reading/writing data from/to memory. Both cannot occur at the same time since the instruction and data use the same signal path ways and memory.
- The execution of each instruction requires four clock cycles because there is a single address bus and there is a single data bus for accessing the program as well as data memory area.

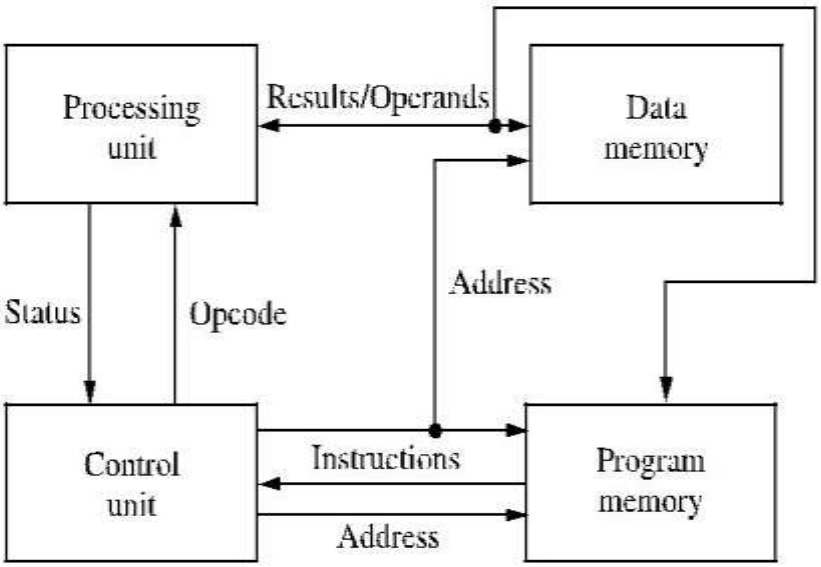
Harvard Architecture.



- In this, there are two separate buses for the program and data memory. Hence the content of program memory and data memory can be accessed in parallel.

- The instruction code is fed from the program memory to the control unit and the operand is fed to the processing unit from the data memory.
- It needs two independent memory banks.
- Required number of memory accesses/clock cycle was two.

Modified Harvard architecture



- The P-DSPs normally follow this. One set of bus is used to access a memory that has both program and data and another set of bus is used to access data alone.
- In modified Harvard architecture, data can also be transferred from one memory to another memory. This architecture is used in several P-DSPs.
- Motorola DSP5600X, DSP96002, etc. have three separate buses and so have three memory accesses/clock cycle. TMS320C54X has four address buses and so has four memory accesses per clock cycle.

Multiple access memory and Multi-ported memory

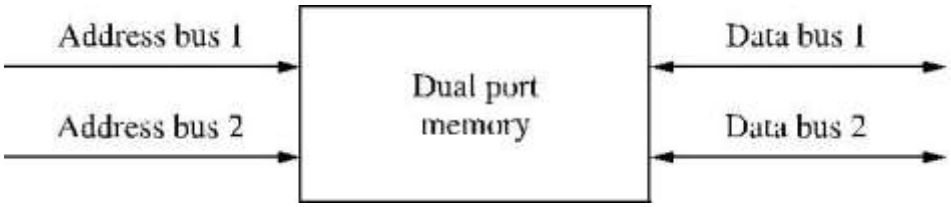
- The different techniques adopted for increasing the number of memory accesses/instruction cycle are:

  (i) Multiple access memory and (ii) Multiported memory

- Using high speed memory, that permits more than one access/clock period is called multiple access memory. (using high speed memory).

  Example: DARAM (2) & P-DSP(HA)(2) - 4

- Multiported memories dispense with the need for storing the program and data in two different memory chips in order to permit simultaneous access to both program and data memory.



- One of the major limitations of the dual ported memory is the increase in the cost compared to two single port memories of the same total capacity.
- This is due to the increased number of pins and larger chip area required for the dual port memory.
- Larger and more expensive package and a larger die size is required for larger number of I/O pins.

VLIW Architecture

- Very long instruction word (VLIW) architecture is another architecture used for P-DSPs (Example: in TMS320C6X).
- The VLIW processor consists of architecture that reads a relatively large group of instructions and executes them at the same time.
- These P-DSPs have a number of processing units (data paths), ALU's, MAC units, shifters etc.

Operation:

1.Multiple functional units share a common multiported register file for fetching the operands and storing the results.

2. Parallel random access by the functional units to the register file is facilitated by the read/write cross bar.

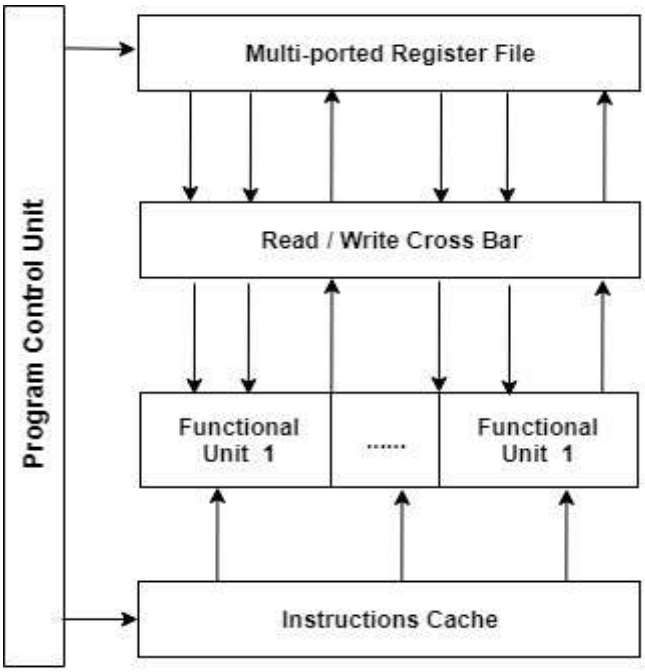
3. Execution of operations in the functional units is carried out concurrently with the load/store operation of data between a RAM and the register file.

- The performance gain depends on :
  - The degree of parallelism of algorithm (higher throughput, if algorithm executes independent operations).
  - Number of functional units (usage of 8 units reduce time required for convolution by a factor of 8).

Drawbacks:

1. Not always possible to have independent stream of data for processing.
2. Number of functional units limited by hardware cost.

VLIW architecture- Block Diagram



VLIW Architecture

Pipelining

- Instruction Pipelining is used to increase the efficiency of P-DSP's/advanced microprocessors.
- An instruction cycle requires 4 microinstructions in 4 phases as:
  - Fetch Phase: instruction fetched from program memory.
  - Decode Phase: instruction is decoded.
  - Memory Read Phase: operand required for execution of instruction is read from data memory.
  - Execution Phase: execution, storage of the results into registers/memory is carried out.
- Above instructions carried out by 4 functional units,

  Let 4 phases take equal time for completion.

Conventional microprocessor with no pipelining

- Each functional unit is busy only 25% of the time, as only one instruction is processed at the CPU at a time.
- The time required for executing N instructions is 4NT.

Value of T	Fetch	Decode	Read	Execute
1	I1			
2		I1		
3			I1	
4				I1
5	I2			
6		I2		
7			I2	
8				I2
9	I3			
10		I3		
11			I3	
12				I3

Instruction cycles of a processor with pipelining

- Functional units busy all time by processing number if instructions simultaneously in the CPU.
- The time required for N instructions execution is (N+4)Ts.

Value of T	Fetch	Decode	Read	Execute
1	I1			
2	I2	I1		
3	I3	I2	I1	
4	I4	I3	I2	I1
5	I5	I4	I3	I2
6	I6	I5	I4	I3
7	I7	I6	I5	I4
8	I8	I7	I6	I5
9	I9	I8	I7	I6
10		I9	I8	I7
11			I9	I8
12				I9

SPECIAL ADDRESSING MODES in P-DSP's

- P-DSP's have special addressing modes that permit single word/instruction format, speed up the execution by making effective use of the instruction pipelining.

1.Short immediate addressing

2.Short direct addressing

3.Memory mapped addressing

4.Indirect addressing

5.Bit reversed addressing

6.Circular addressing

Short immediate addressing

- In short immediate addressing mode, the operand is specified as a short constant that forms part of a single word instruction.
- The length of the short constant depends on the programmable DSP and the instruction type.
- In TMS320C5XDSPs, an 8 bit constant can be specified as one of the operands in the single word instruction like AND, OR, addition, subtraction, etc.

Short direct addressing

- In short direct addressing mode, the lower order address of the operand is specified in the single word instruction.
- In TITMS320DSPs, the higher order 9 bits of the memory are stored in the data page pointer and only the lower 7 bits are specified as part of the instruction.
- Using short direct addressing in the Motorola DSP5600X processor, an instruction is specified with a 6 bit address.

Memory-mapped addressing

- In this addressing mode, the CPU registers and the I/O registers are accessed as memory locations by storing them in either the starting page or the final page of the memory space.
- For example, in TMS320C5X, page 0 corresponds to the CPU registers and I/O registers.
- In the case of Motorola DSP5600X, the last page of the memory space containing 64 locations is used as the memory map for the CPU and I/O registers.

Indirect addressing

- This addressing mode has a number of options in P-DSPs. This mode permits an array of data to be efficiently processed, fetched and stored.
- The address of the operands can be stored in one of the registers called indirect address registers.

- In the case of TI processors, the indirect address registers are called auxiliary registers .
- The content of the indirect address registers may also be updated by a constant using bit reversed addressing mode.

Bit reversed addressing

- The binary pattern corresponding to a particular decimal number is obtained by writing the natural binary equivalent of the number in the reverse order.
- Therefore, the least significant bit of the bit reversed number becomes the most significant bit of the natural binary number and vice versa.
- In this addressing mode, the address is incremented or decremented by the number represented in the bit reversed form.

Circular addressing mode

- In this mode, the memory can be organized as a circular buffer with the beginning memory address and the ending memory address corresponding to this buffer designed by the programmer.
- In the circular addressing mode, when the address pointer is incremented, the address will be checked with the ending memory address of the circular buffer.
- If it exceeds that, the address will be made equal to the beginning address of the circular buffer.

ON-CHIP PERIPHERALS

- The P-DSPs have a number of on-chip peripherals that relieve the CPU from routine functions.
- Further they also help to reduce the chip count on the DSP system based around P-DSP

On-chip Timer

- Two of the common applications of timers are generation of periodic interrupts to the DSPs and generation of the sampling clocks for A/D converters. The timer can be programmed by the P-DSPs.

Serial Port

- The serial port enables the data communication between the P-DSP and an external peripheral such as A/D converter, D/A converter or an RS232C device.
- These ports normally have input and output buffers so that the P-DSP writes or reads from the serial port in parallel form and the serial port sends and receives data to the peripherals in serial form.

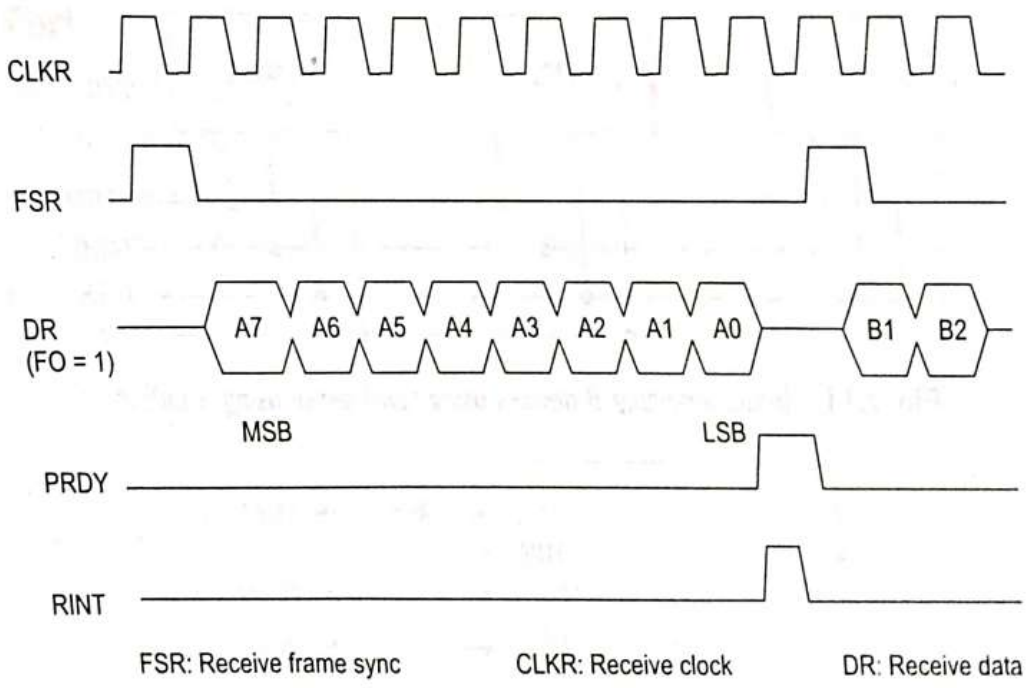


Fig : Burst mode serial port receive operation

TDM Serial Port

- The TDM serial port is a special serial port the P-DSPs have. This port permits a P-DSP to communicate with other devices or P-DSPs by using time division multiplexing (TDM).
- Devices generate frame sync pulse that indicates beginning of a TDM frame and bit clock, the duration for a bit to be transmitted.
- The TDM frame is split into a number of equal slots and each slot can be allotted for one of the devices.

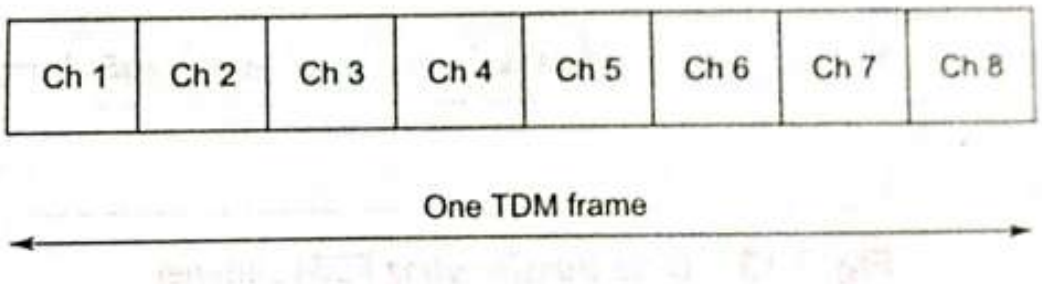


Fig: TDM Frame with 8 time slots

- The TDM serial port normally uses 4 lines for the purpose of serial communication. They are:
  - TFRM : the frame sync signal
  - TClock : the bit clock

- TADD : the address of the serial device that is outputting data in a particular TDM slot.
- TDAT : the data transmitted into the TDM channel by the authorized device.

Note:

1. TADD & TDAT- bidirectional & are tri-state controlled

   so that only one of the devices transmit the data and address in thee lines at a time.

2. Any device generate TFRM & TClock, used by other devices as a reference**.**

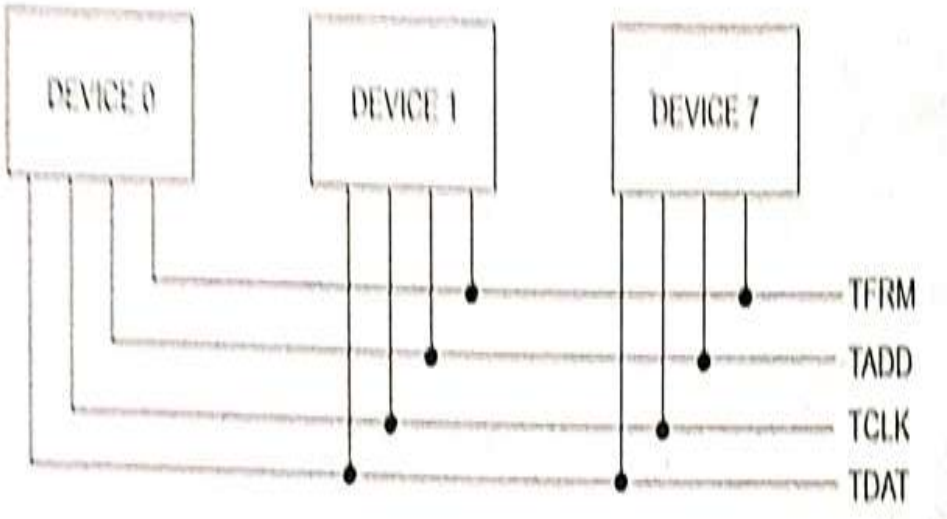


Fig (a): Interconnecting 8 devices using TDM serial using 4-bit Bus

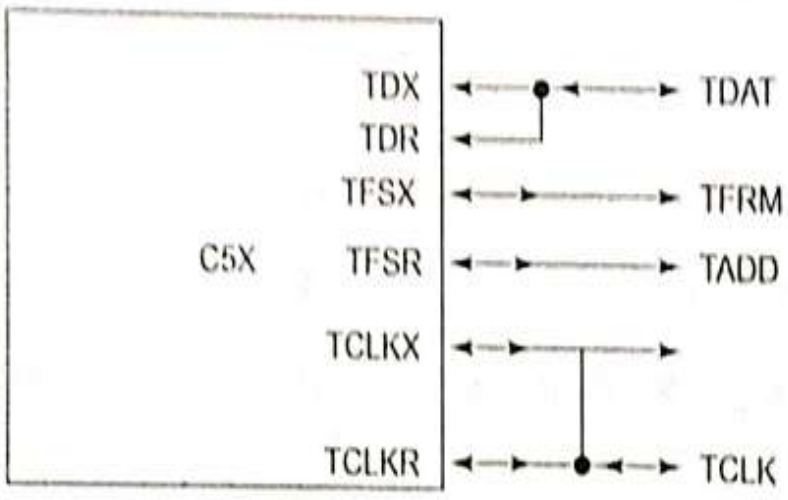


Fig (b): TMS320C5X configured to be one of TDM devices

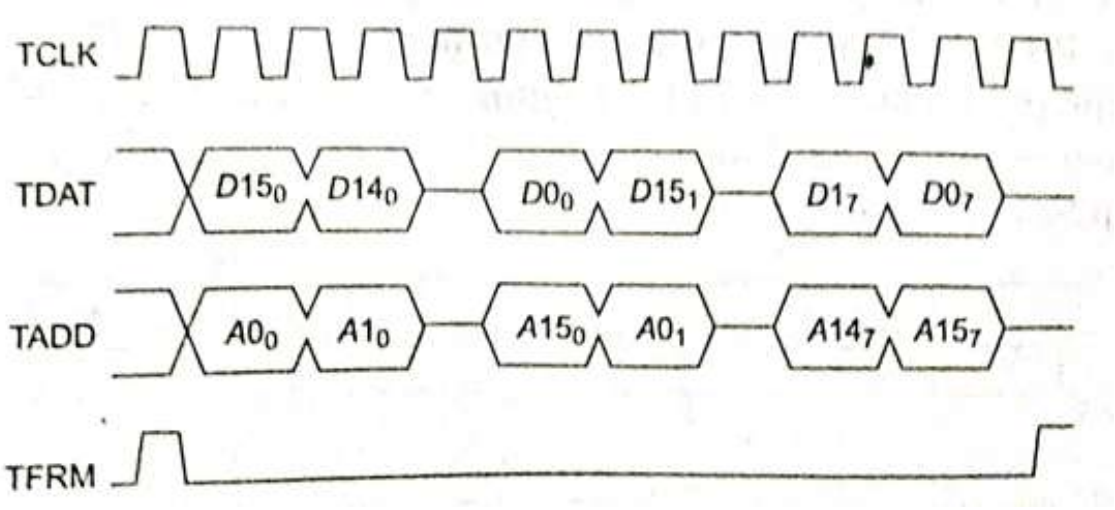


Fig (c): Data transfer using TDM channel

Parallel Ports

- Parallel ports enable communication between the P-DSP and other devices to be faster compared to the serial communication by using a number of lines in parallel.

Bit I/O Ports

- These are additional I/O ports the P-DSPs have that are single bit wide. These port bits may be individually set, reset or read.
- These bits are normally used for control purposes, but they can also be used for data transfer.

Host Ports

- Host port is a special parallel port the P-DSPs have. This enables the P-DSPs to communicate with a microprocessor or a PC, which is called a host.
- In addition to data communication, the host can generate interrupts and also cause the P-DSP to load a program from ROM to the RAM on reset.

Comm Ports

- These are parallel ports that are used for interprocess communication between a number of identical P-DSPs in a multiprocessor system.

On-chip A/D and D/A Converters

- Some of the P-DSPs targeted towards voice applications such as cellular telephones and tapeless answering machines have A/D and D/A converters inside the P-DSPs.

P-DSPs WITH RISC AND CISC

- P-DSPs may be implemented using either the RISC processor or the CISC processors

Advantages of Restricted Instruction Set Computer (RISC) Processors

1.In RISC processor, the control unit uses only around 20% of the chip area because of the reduced number of instructions. Hence the remaining area can be used for incorporating other features.

2.The delayed branch and call instructions are used to improve the speed of the RISC processors.

3.The execution time required for all the instructions of RISC processor is same because all the instructions are of uniform length.

4.The RISC processors have smaller and simpler control units, which have fewer gates.

5.The speed of the RISC processor is high because of smaller control unit and smaller propagation delays.

6.Since a simplified instruction set allows for a pipelined superscalar design, RISC processors often achieve two to four times the performance of CISC processor using comparable semiconductor technology and the same clock rates.

7.Because the instruction set of a RISC processor is simpler, it uses much less chip space than a CISC processor. Extra functional units such as memory management units or floating point arithmetic units can be placed on the same chip.

8.The throughput of the processor can be increased by applying pipelining and parallel processing.

9.Since RISC processors can be designed more quickly, they can take advantage of new technological developments sooner than corresponding CISC design.

10.High level language (HLL) support; The programs can be written in C and C^{++}. It relieves the programmer from learning the instruction set of a P-DSP which in turn increases the throughput of the programmer.

Advantages of Complex Instruction Set Computer (CISC) Processors

1.The CISC processors have a very rich instruction set that even support high level language constructs similar to “if condition true then do”, “for” and “while”.

2.The CISC processors have instructions specifically required for DSP applications such as MACD, FIRS, etc.

3.The assembly language program of a CISC processor is very short and easy to follow.

4.For RISC architecture compliers are essential. So this becomes costly. For CISC compilers are not required. Hence they are of low cost.

5.New CISC processors are designed to be upward compatible with the older processors. This makes the learning curve steeper.

6.Microprogramming is easier to implement and much less expensive than hardwiring a control unit.

7.Since micro program instruction sets can be written to match the constructs of high-level languages, the complier need not be very complicated.

8.As each instruction is more capable, fewer instructions could be used to implement a given task. This made more efficient use of the relatively slow main memory.