14CS IT303

Hall Ticket Number:

II/IV B.Tech (Supplementary) DEGREE EXAMINATION

April, 2017 — **Common for CSE & IT**

Third Semester — **Digital Logic Design**

Time: Three Hours — **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1. Answer all questions (1X12=12 Marks)

a Convert $(100101)_{gray}$ to binary.
b Which logic gate is used in parity checkers?
c How many numbers of Boolean functions that can be generated by n variables?
d Differentiate between a prime implicant and non-prime implicant.
e Write truth table for 2-bit magnitude comparator.
f Design EX-OR gate using decoder
g Write characteristic equation of JK flip flop.
h Compare combinational and sequential circuits.
i How many flip flops are required to build MOD-12 counter?
j What is meant by PAL?
k How many number of states can count by n-bit Johnson counter
l Draw the block diagram of RAM cell.

UNIT I

2.a Explain about signed magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable? 6M

2.b Design all basic gates with NOR and NAND gates. 6M

(OR)

3.a With respect to the Boolean expressions identify correct and in-correct statements
$(i)A' + AB = A + B, (ii)\ A(A+B) = A, (iii)\ (A+B')(B'+C) = AC,\ (iv)\ A + A + AA' + B + B + BB' + AB = A$
4M

3.b Simplify the following Boolean function using 4-varaiable K-map and implement the simplified function with basic gates (inverter, and, & or) only.
f(A,B,C,D) = ∑m(1,5,6,7,11,12,13,15) 8M

UNIT II

4.a Minimize the following Boolean function using tabulation method
f(w,x,y,z) = ∑m(1,4,6,7,8,9,10,11,15) 6M

4.b Design a full adder with two half adders and basic gates. 6M

(OR)

5.a Implement the following Boolean function using a single 8 X 1 multiplexer and no other gate.
F(A, B, C, D) = $BC + ABD' + A'C'D$ 6M

5.b Design seven segment display decoder. 6M

UNIT III

6.a Design a MOD – 6 asynchronous counter using T-flip flops. 6M

6.b Design a synchronous BCD counter using JK-flip flops. 6M

(OR)

7.a Derive D flip flop and JK flip flop from T flip flop. Give the procedure for flip flop inter conversion. 5M

7.b Explain about SR flip flop with its truth table. Write its characteristic table, excitation table and characteristic equation. Draw its logic diagram 7M

UNIT IV

8.a	Draw a 4-bit shift register using JK flip flop which can shift the data to register one by one on the application of a clock.	6M
8.b	Design a 4-bit binary up and down ripple counter.	6M

(OR)

9.a	Implement the following function using PLA F1 = $\sum$m(1,2,4,6) F2 = $\sum$m(0,1,6,7) F3 = $\sum$m(2,6)	7M
9.b	Elucidate the importance of ROM with neat diagrams.	5M