14CS IT403

Hall Ticket Number:

II/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

April, 2017 **Common for CSE & IT**

Fourth Semester **Computer Organization**

Time: Three Hours **Maximum:** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1. Answer all questions (12X1=12 Marks)

a) Define Throughput and Throughput rate.
b) Write basic performance equation.
c) What do you mean by out-of order execution? Is it Desirable?
d) What are virtual and logical addresses?
e) List out Various branching technique used in micro program control unit?
f) What is known as Multi-Phase clocking?
g) What is an index register?
h) What is write-through Protocol?
i) What is locality of reference?.
j) What is a Memory Controller?
k) What are the steps required for a pipelined processor to process the instruction?
l) What is DMA?

UNIT I

2. a) What is the addressing mode? Explain different addressing modes in detail. **(6M)**
b) Explain different functional units of a digital computer. Mention the functions of different processor registers i)IR ii)MAR iii)PC **(6M)**

(OR)

3. a) Write the procedure for integer division for dividing (101101)2 (45)10 by (000110)2 (6)10 **(6M)**
b) Write the use of Rotate & Shift instructions with examples. **(6M)**

UNIT II

4. a) Give the different instruction formats of a CPU in detail. **(6M)**
b) Explain horizontal and vertical organizations in micro programmed control. **(6M)**

(OR)

5. a) Give Booth's algorithm to multiply two binary numbers. Explain the working of the algorithm taking an example. **(6M)**
b) Explain in detail the principle of carry look ahead adder. Show how 16-bit CLAs can be constructed from 4-bit adders with an example. **(6M)**

UNIT III

6. (a) Explain detail the working of a micro programming control unit. **(6M)**
(b) What are handshaking signals? Explain asynchronous data transfer with hand shaking signals. **(6M)**

(OR)

7. (a) What are data hazards? Explain how data hazards effect pipelining. **(6M)**
(b) Discuss the various mapping schemes in cache design. Compare the schemes in terms of cost and performance. **(6M)**

UNIT IV

8. (a) Why is priority handling desired in priority controllers? How do the different priority schemes work? Explain **(6M)**
(b) What are Interrupt nesting? Briefly bring out the methods involved in the processor attending to simultaneous requests. **(6M)**

(OR)

9. (a) Discuss the main phases involved in the operation of SCSI bus in detail. **(6M)**
(b)Write short notes on (a) USB (b)PCI bus **(6M)**