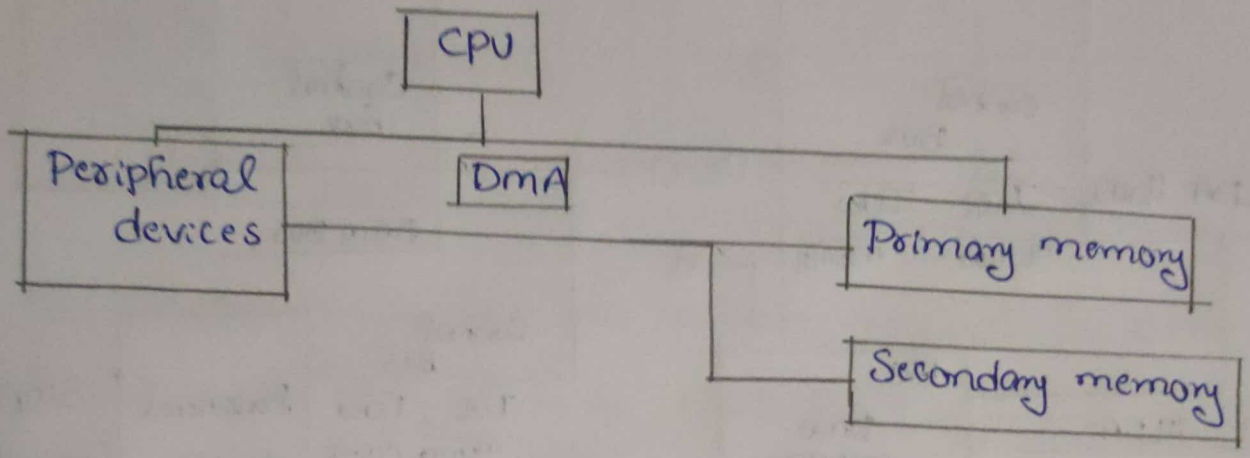
DMA Controller (Direct memory access)

It is a method that allows an Input/output (I/O) devices to send or receive data directly to or from the main memory. By passing the CPU to speed up memory operations. The process is managed by a chip known as a DMA controller



→ DMA transfers are performed by a control circuit that is the part of the I/O device interface

→ It refer to this circuit as a DMA controller

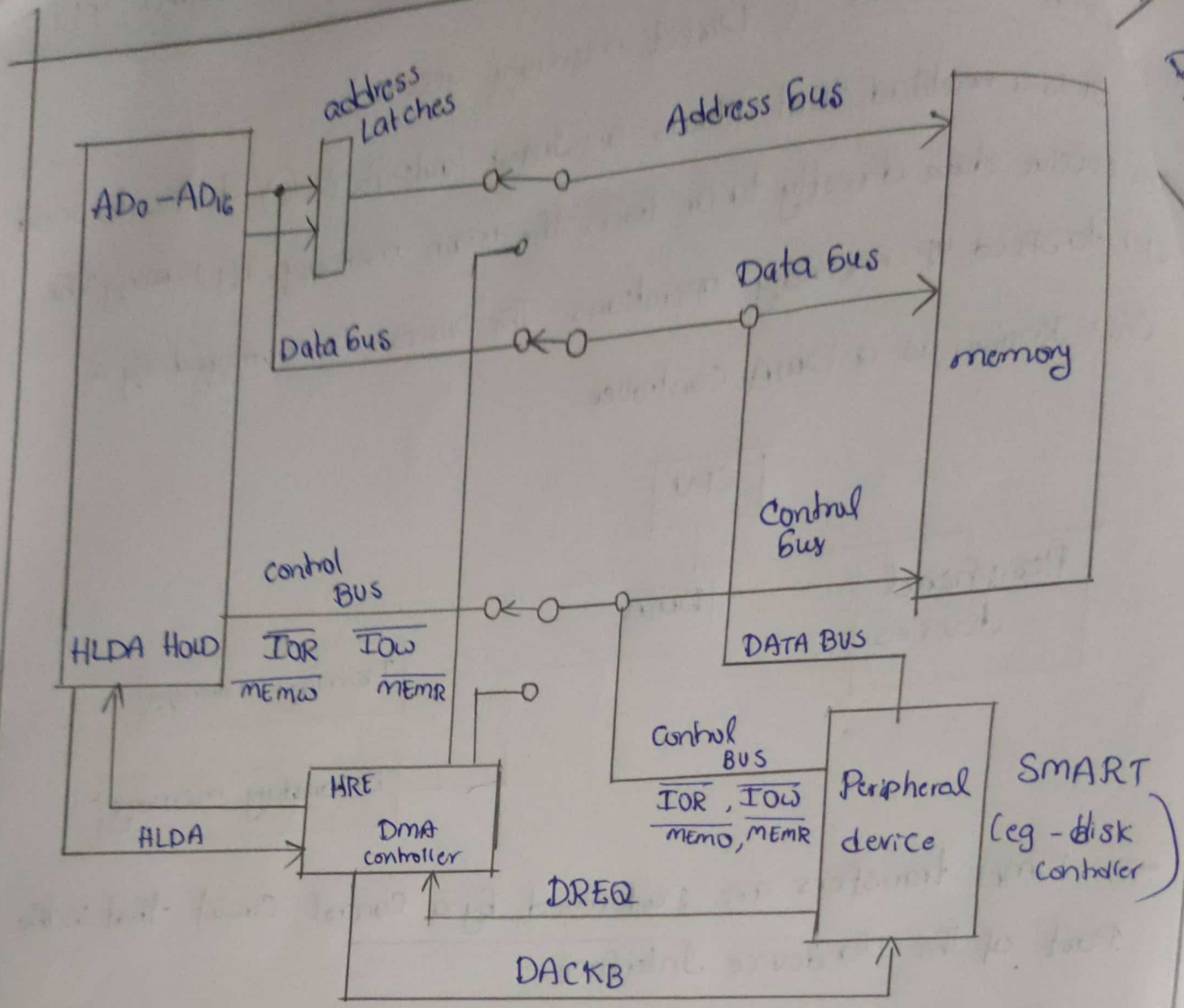
→ The DMA controller performs the function that would normally be carried out by the processor when processing the main memory

→ Device wishing to perform DMA asserts the processors bus request signal

→ Processor completes the current bus cycle and then asserts the bus grant signal to the device

Basic DMA operation

→ The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled



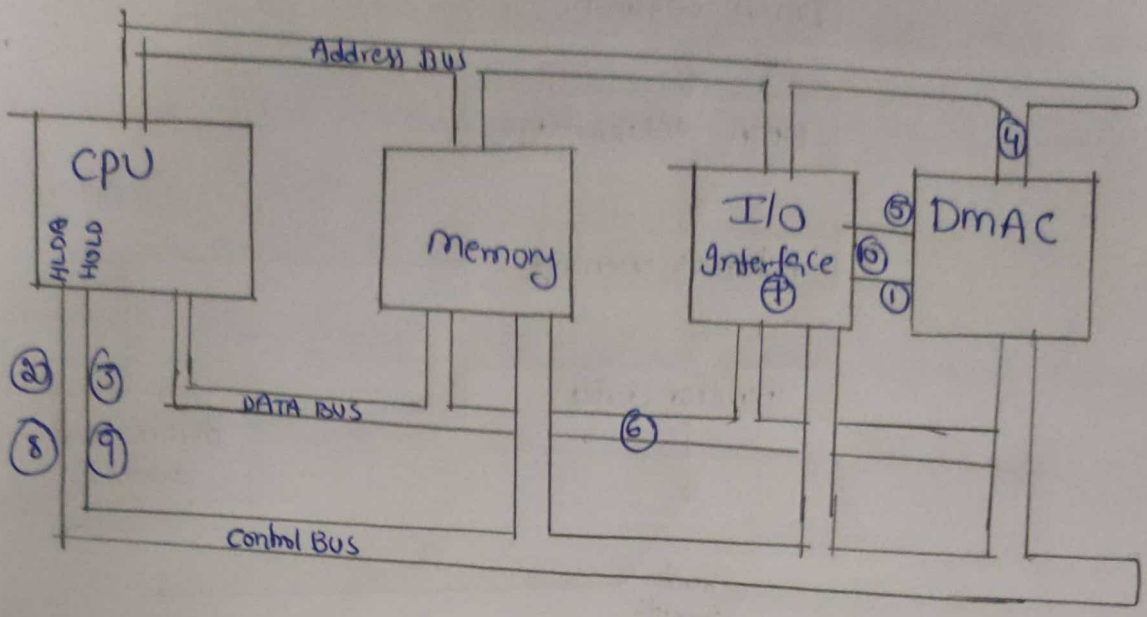
→ A DMA controller tempararily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly blw an I/o Port and a series of memory locations

→ The DMA controller is also used to do high-speed memory to memory transfer

→ Two control signal are used to request and acknowledge a DMA transfer in the microprocessor based system.

→ During a block Input byte transfer, the following sequence across as the data byte is sent from the Interface to memory

Data transfer with a DMA Controller



→ The Interface Sends the DMA controller, a request for DMA service

→ A Bus request is made to the HOLD Pin (active high) on the 8086 microprocessor and the Controller gains the Control of bus

→ A bus grant is returned to the DMA Controller from the HLDA Pin (active high) on the 8086 microprocessor

→ The DMA Controller places contents of the address register on to the address bus

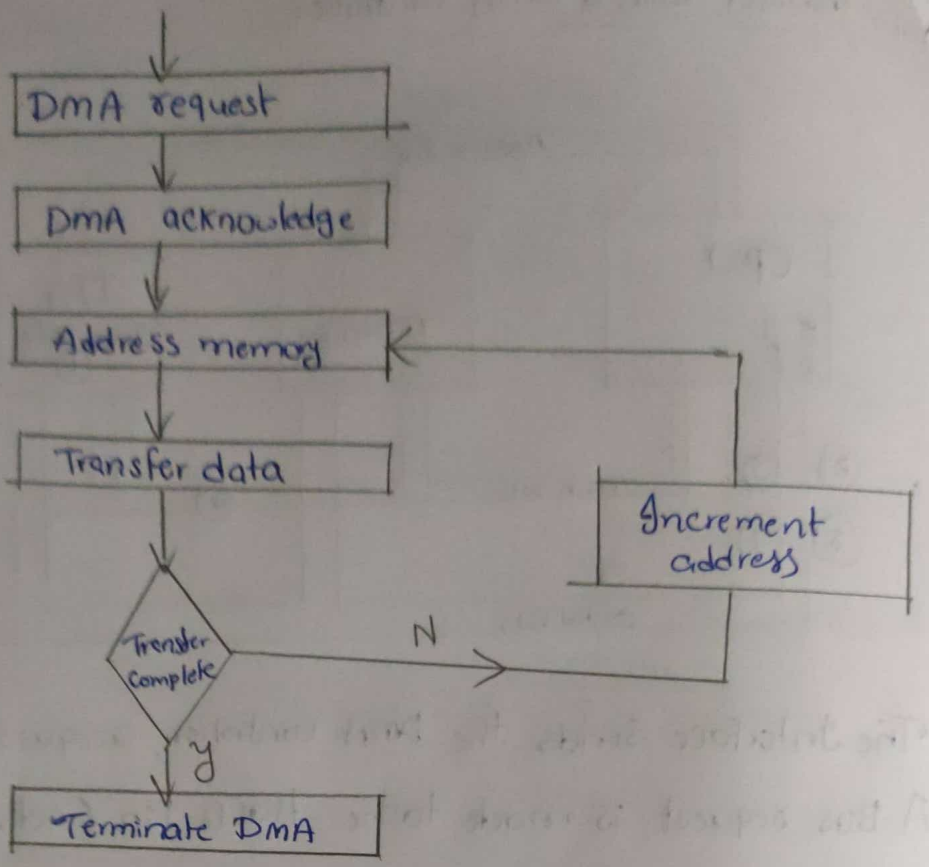
→ The controller Sends the Interface to a DMA acknowledge which tells the Interface to put data on the data bus

(For an output it signals the Interface to latch the next data placed on the bus)

→ The data byte is transferred to the memory location Indicated by the address bus

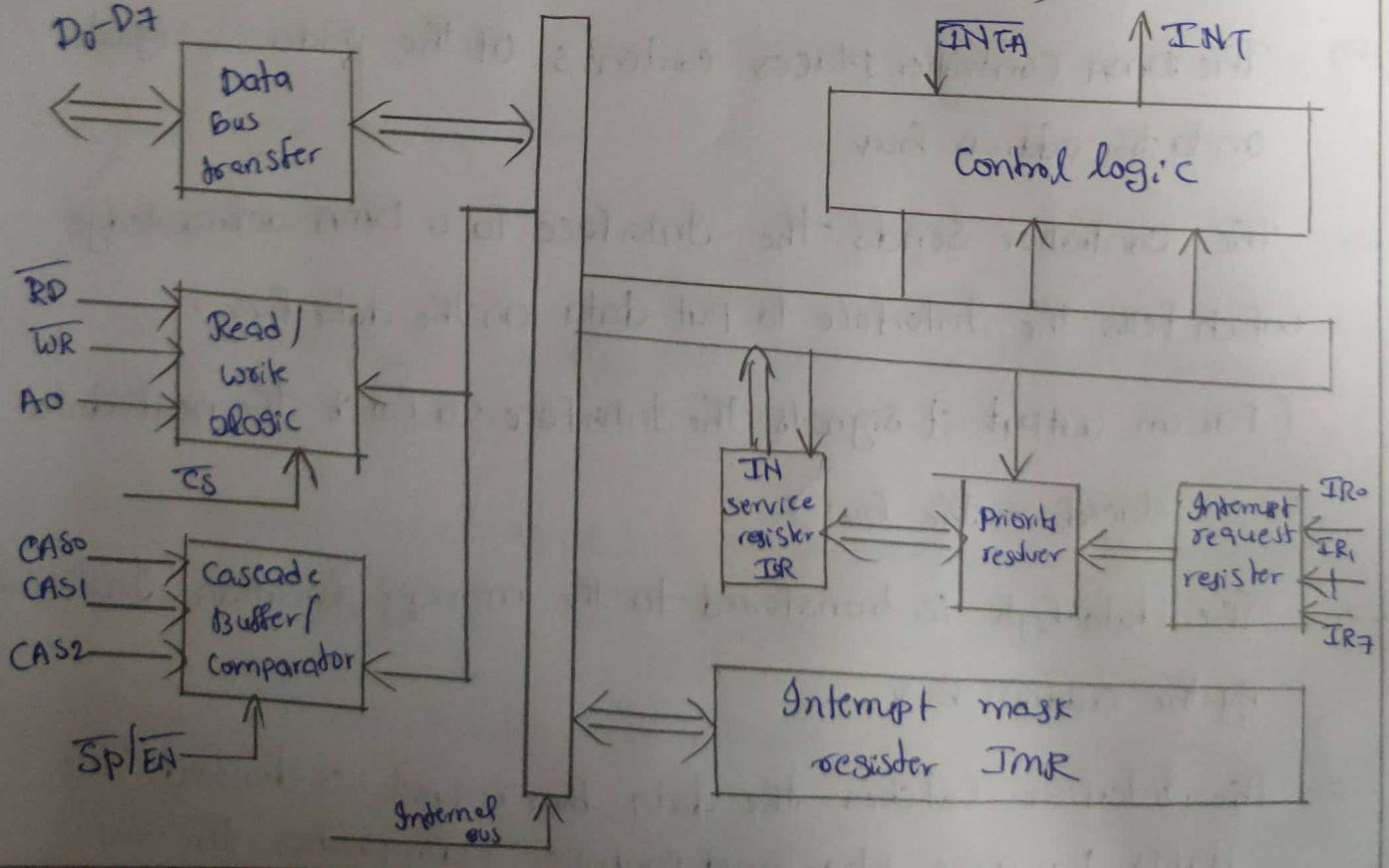
→ The Interface latches the data, bus request is dropped. The HOLD Pin goes low and controller relinquishes the bus

→ Flowchart



(2) 8259 PIC Controller

→ Only 8 Interrupts can be taken (IR_0 to IR_7)



Interrupt request register (IRR) The Interrupts at IR0 Input lines are handled by Interrupt request Internally. IRR stores all the Interrupt request in it in order to serve them one by one on the Priority basis

→ In-Service register (ISR) This stores all the Interrupts requests those are being served ie. ISR keeps track of the request being served

→ Priority resolver The unit determines the priorities of the Interrupt requests appearing simultaneously. The highest Priority is selected stored into the corresponding bit of the ISR during INTA pulse. The IR_0 has the heighest priority while the IR_7 has the lowest one. normally in fixed priority mode. The Priorities however may be altered by programming the 8259A in rotating priority mode.

→ Interrupt mask Register (IMR) This register stores bits required to mask the Interrupt Inputs. IMR operates on IRR at the direction of Priority resolver

→ Interrupt Control logic

This block manages the Interrupt and Interrupts acknowledge signals to be sent to the CPU. for Serving one of

eight Interrupt request. This also accepts the Interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on the data bus

→ Data Bus Buffer This tristate bidirectional buffer interfaces Internal 8259A bus to the microprocessor system data bus control words, status and vector information pass through data buffer during read or write operations

→ Read/write control logic This circuit accepts and decodes commands from the CPU. This block also allows the status of the 8259A to be transsferred onto data bus

→ Cascade buffer / comparator This block stores and compares the ID's all the 8259A used in system. The thread I/o pins CAS0-2 are outputs when the 8259A is used as a master. The same pins act as input when the 8259A is in slave mode. The 8259A in master mode sends the ID of Interrupting device on these lines

→ CS : This is an active-low chip select signal for enabling RD and WR operations of 8259A INTA functions is independent of CS

WR : This pin is an active low write enable input to 8259A. This enables it to accepts command words from CPU

→ RD: This is an active low read enable input to 8259A A low on this line enables 8259A to release status onto data bus of CPU

→ D_0-D_7: These pins from a bidirectional data bus that carries 8-bit data either to control word or from status word register This also carriers Interrupt vector Information.

→ CAS0 - CAS2 cascade lines A signal 8259A provides eight vectored Interupts If more Interupts are required. The 8259A is used in cascade mode. In Cascade mode, a master 8259A along with eight slaves 8259A can Provide upto 64 vectored Interupt lines. These three lines act as Select lines for addressing the slave 8259A

→ $\overline{SP}/\overline{EN}$: This pin is dual purpose pin when the top of chip is used in buffered mode. It can be used in buffered enable to control buffer transreceivers.

→ INT: This pin goes high whenever a valid Interupt resquest is asserted. This is used to Interupt the CPU and is connected to the Interupt Input of CPU

IR_0-IR7 (Interupt request) These pins acts as inputs to accept Interupt request to CPU.

→ RD : This is an active low read enable input to 8259A A low on this line enables 8259A to release status onto data bus of CPU

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(3) ⇒ Interfacing a Keyboard / LED to 8086 microprocessor

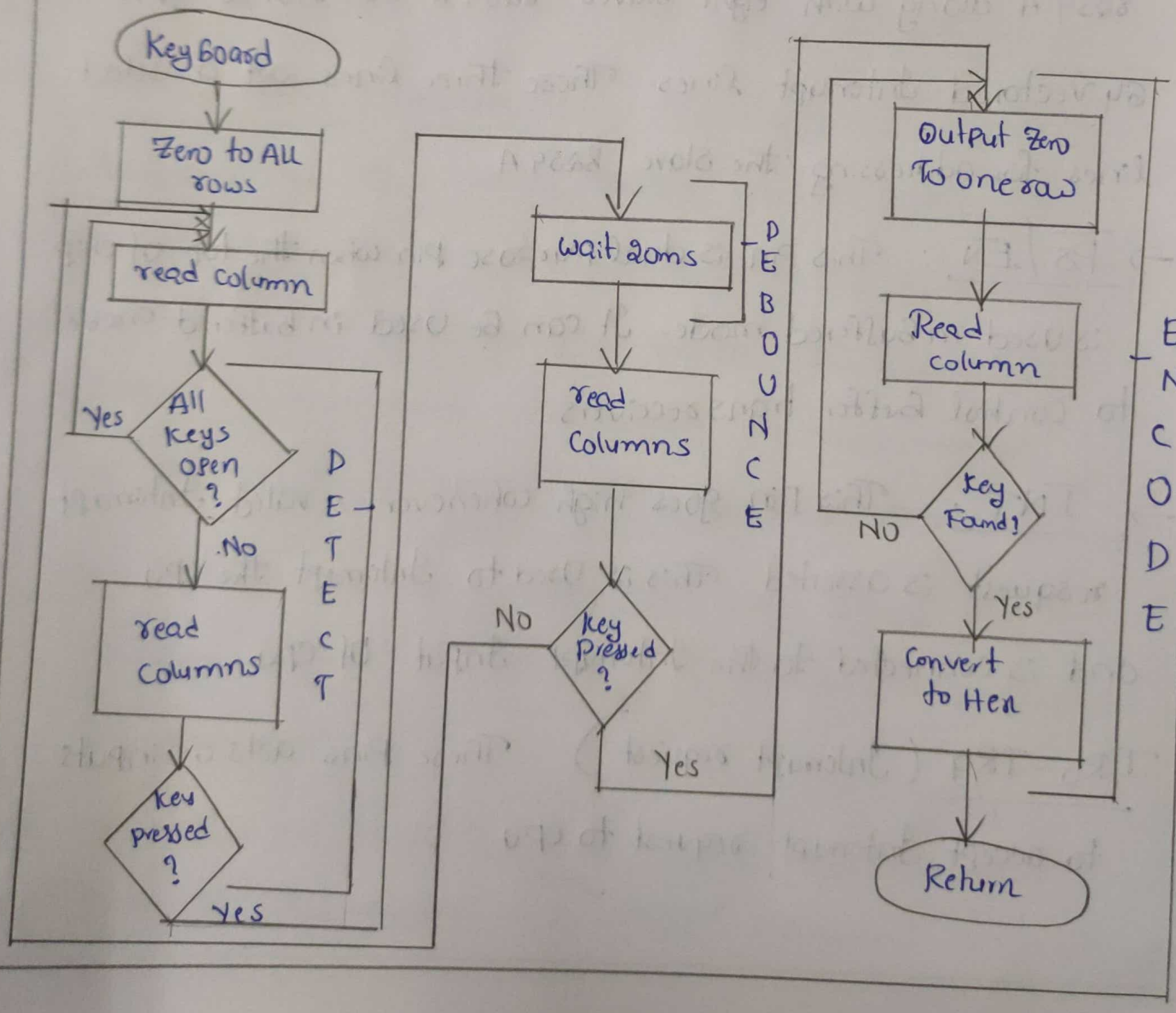
When you pass a key on your computer, your activated a switch

→ when key is pressed column and rows a link will be formed and that particular key will be displayed

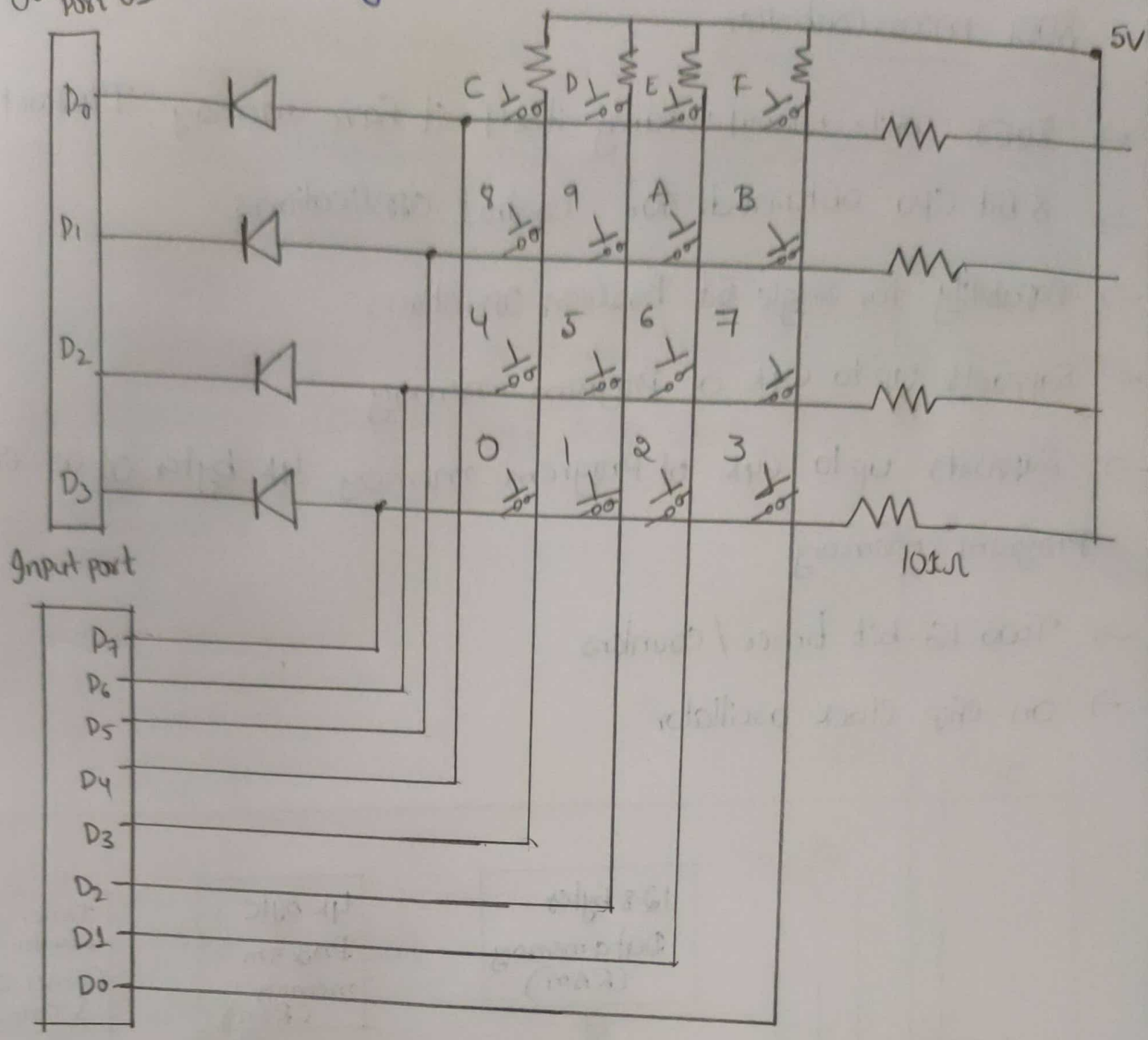
→ In three ways key is pressed is identified

1) detect key press
2) Debounce key press
3) encode key press

Flow Chart



4x4 keyboard



→ We are using debounce period to avoid some software Problems, So this debounce will wait for 20 milli seconds so before 20ms if any key is pressed so it will not consider

→ After the debounce time another check is made to see if key still Pressed. If the column are now all high then no key is pressed and initial detection was caused by noise Pulse or alight brushing past a key

(4) 8051 micro Controller

→ 8051 while manufacturing itself it have memory, I/o Port etc.
→ 8 bit CPU obtained for control applications
→ Capability for single bit Boolean Operations
→ Supports Up to 64K of Program memory
→ Supports up to 64K of Program memory, 4K byte of on-chip Program memory.
→ Two 16-bit timer / counters
→ on-chip Clock oscillator

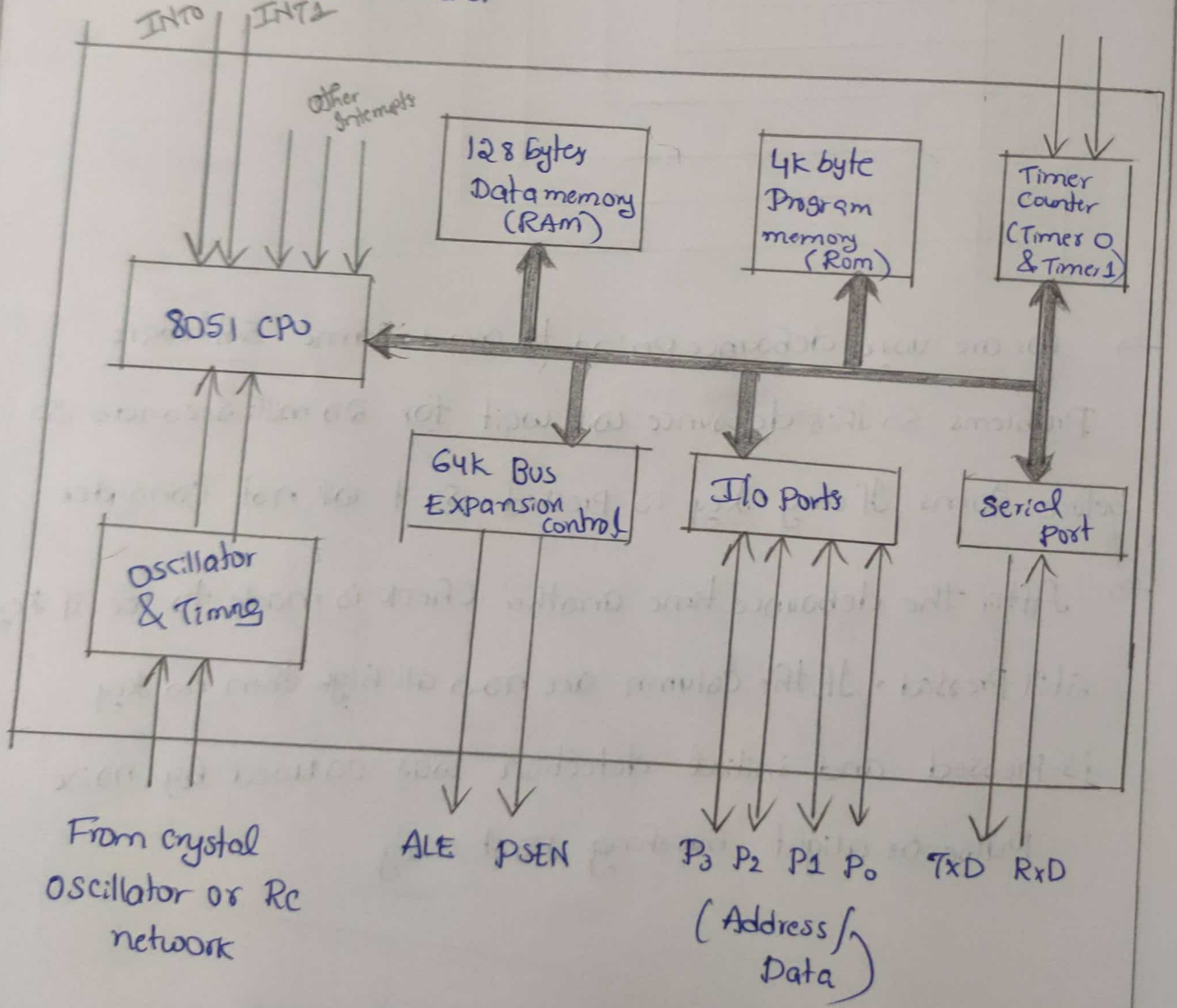


Fig: Block diagram of Generic 8051 micro Controller

→ Program and machine Control

Jump Instruction: To Jump from one Instructor to other.

CALL: To call a Subprogram (or) Procedure we use CALL Instruction

Loop: Repeated execution of Particular Instruction Untill a Condition is Satisfied for this we use loop Instruction

CALL Instruction

A CALL
L CALL
RET
RETI

Jump Instruction

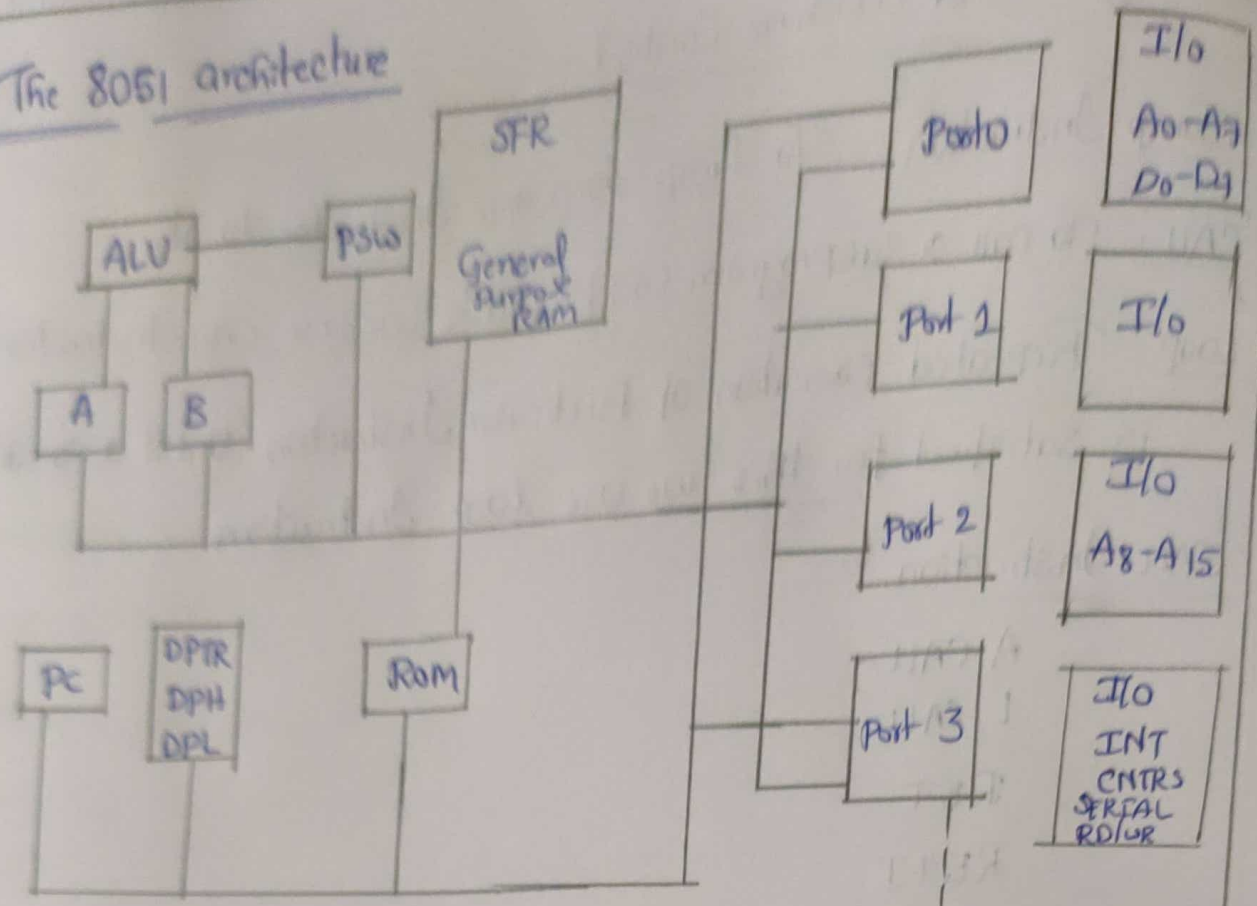
AJmp → Short
LJmp
SJmp
JZ
JNZ
Jmp, CJNE, CJNE

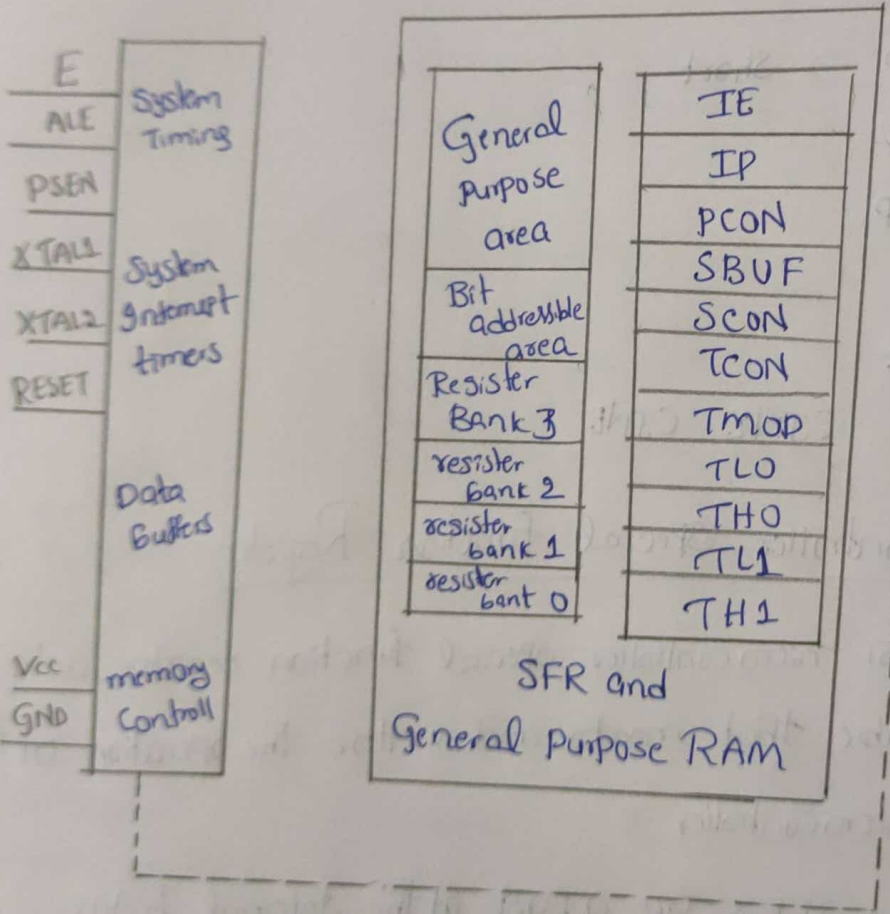
→ Microcontroller Special function Register

→ The 8051 microcontroller special function register acts a control table that monitor and control the operation of the 8051 microcontroller

→ Since the SFR's are a part of the Internal RAM Structure, you can access SFR's as if you access the Internal RAM

The 8051 architecture





They are 21 register they are

1. Acc (or) A
2. B
3. DPL
4. DPH
5. IE
6. IP
7. P0
8. P1
9. P2
10. P3
11. SCON
12. PSW
13. PCON
14. SBUF
15. SP
16. TMOD
17. TCON
18. TL0
19. TH0
20. TL1
21. TH1

→ Accumulator

To perform any operation it must use accumulator

→ Arthimatic operations like addition, subtraction, multiplicaton--

→ B (register)

→ The B register is used along with the Acc in multiplication and division operations

→ These two operations are performed on data that are stores only in register A and B

→ Program Status word (PSW)

The PSW is also called as flag register and is one of the important SFRs. The PSW register consists of flag Bits which help the programmer in checking the condition of the result and also make decision.

→ Pointer Register :- Data pointer is a 16 bit register

and is physically the combination of DPL and DPH SFRs. The data Pointer can be used as a single 16-bit register or two 8 bit registers

→ Stack Pointers

Stack Pointers Points out to the top of stack and it Indicates the next data to be accessed. Stack Pointer can be access Using PUSH, POP, CALL, RET Instructions.

→ IP (Interrupt Priority)

It is used to set the Priority of the Interrupt as high or Low If a bit is cleared. If the corresponding Interupts is assigned low Priority and if bits is SET.

→ 7, 8, 9, 10 - I/o Port register

The 8081 micro controller from Ports which can be used as, Input and /or output These are four Ports P_0, P_1, P_2 & P_3 each Port has a corresponding register with same names

→ Peripheral control register

PCON: even though at Power loss our work will be kept Save avoid deletion. So, this is called Power down mode. PCON (or) Power control as the name suggest is used control 8051 Power modes

SCON: Data will transfer in Serial (Bit by bit)

→ It is used to control Serial Port

TCON: Timer or control (or) TCON register is used to staff or stop the timer of 8051 micro controller. It is also contains bits to indicate if the Timers has overflowed.

TMOD: It is used to set the operating modes of Timers T0 & T1 the lower four bits are used to configure Timer 0 and the higher four bits are used to configure Timer 1

→ IE: The enable register is used to enable or disable individual Interupts. If a bit is SET. The corresponding Interupt is enabled and if the bit is cleared The Interupt is disabled.

→ SBUF: The register is used to hold the serial data while transmission or reception.

→ TL0 / TH0: The timer 0 consist of two SFRs TL0 and TH0

→ TL1 / TH1 (Timer 1 low/high)

The TL1 and TH1 are the lower and higher bytes of Timer 0

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