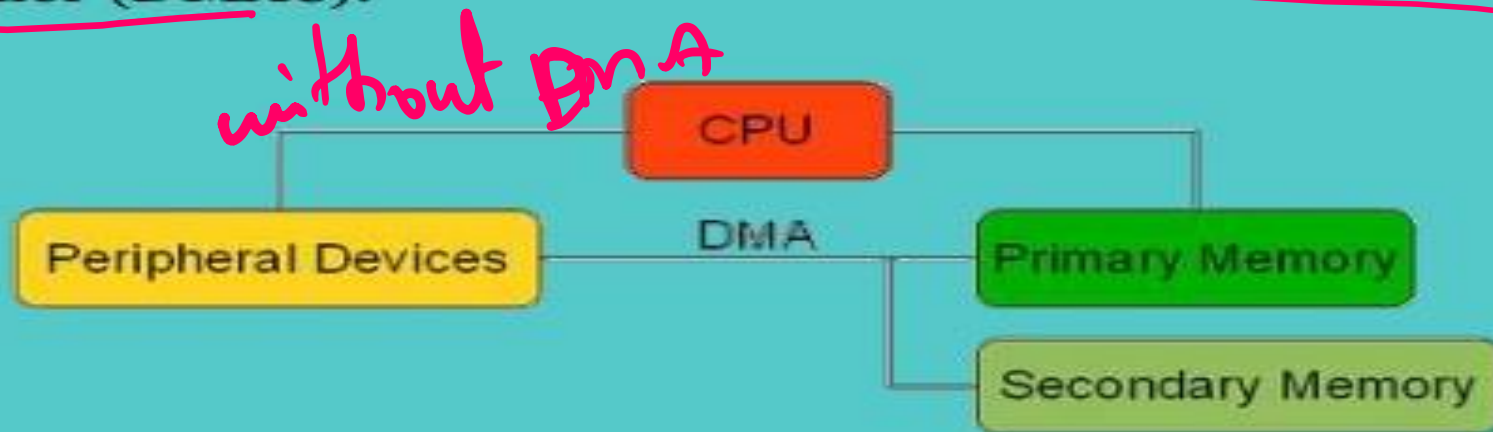# DMA

BY

SANAM SUBRAHMANYAM

EEE DEPARTMENT

BAPATLA ENGINEERING COLLEGE BAPATLA

DMA

- **Direct Memory Access (DMA)** is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory, bypassing the CPU to speed up memory operations. The process is managed by a chip known as a DMA controller (DMAC).

without DMA

DMA

• DMA transfers are performed by a control circuit that is part of the I/O device interface.

• It refer to this circuit as a DMA controller.

• The DMA controller performs the function that would normally be carried out by the processer when accessing the main memory.

• Device wishing to perform DMA asserts the processors bus request signal

• Processor completes the current bus cycle and then asserts the bus grant signal to the device.

Basic DMA operation

• The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.

• A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory locations.

• The DMA transfer is also used to do high-speed memory-to-memory transfers.

• Two control signals are used to request and acknowledge a DMA transfer in the microprocessor-based system.

Data transfer with a DMA Controller
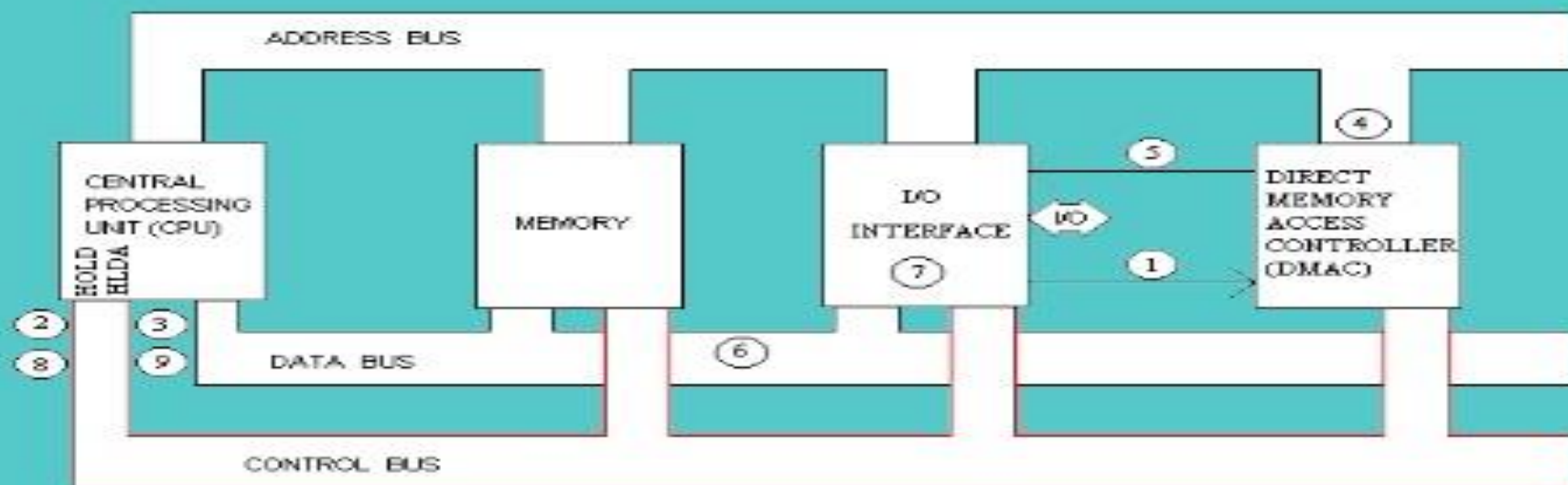
DATA TRANSFER WITH A DMA CONTROLLER

Data transfer with DMA controller

During a block input byte transfer, the following sequence occurs as the data byte is sent from the interface to the memory:

- The interface sends the DMA controller a request for DMA service.
- A Bus request is made to the HOLD pin (active High) on the 8086 microprocessor and the controller gains control of the bus.
- A Bus grant is returned to the DMA controller from the Hold acknowledge (HLDA) pin (active High) on the 8086 microprocessor.

- The DMA controller places contents of the address register onto the address bus.
- The controller sends the interface a DMA acknowledgment, which tells the interface to put data on the data bus. (For an output it signals the interface to latch the next data placed on the bus.)
- The data byte is transferred to the memory location indicated by the address bus.
- The interface latches the data.

- The Bus request is dropped, the HOLD pin goes Low, and the controller relinquishes the bus.
- The Bus grant from the 8086 microprocessor is dropped and the HLDA pin goes Low.
- The address register is incremented by 1.
- The byte count is decremented by 1.
- If the byte count is non-zero, return to step 1, otherwise stop
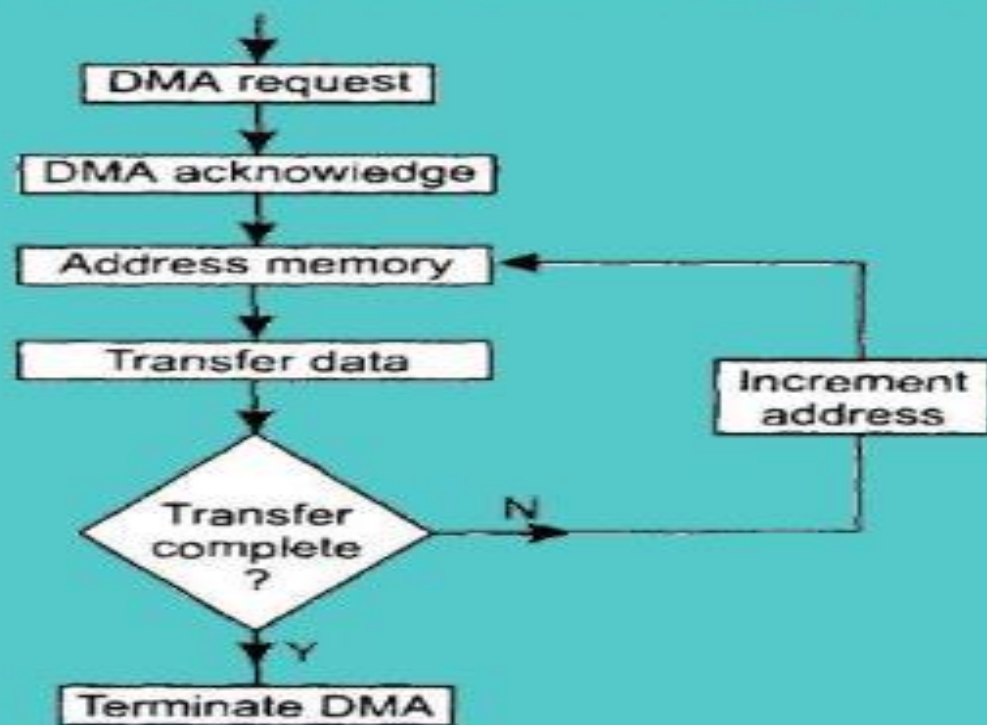
Fig : Flowchart of DMA

ADDRESS
LATCHES

ADB-AD'13

ALE

ADDRESS BUS

MEMORY

DATA BUS

DATA BUS

DATA BUS

CONTROL BUS

CONTROL BUS

IOR, IOW
MEMW, MEMR

HLDA HOLD

DATA BUS

HRQ

DMA
CONTROLLER

CONTROL BUS

IOR, IOW

MEMW, MEMR

HLDA

PERIPHERAL
DEVICE

SMART
(eg DISK
CONTROLLER)

DREQ

DACK8