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II/IV B.Tech (Supplementary) DEGREE EXAMINATION**April, 2017****Third Semester****Time:** Three Hours**Common to CSE & IT****Digital Logic Design****Maximum : 60 Marks***Answer Question No.1 compulsorily.*

(1X12 = 12 Marks)

Answer ONE question from each unit.

(4X12=48 Marks)

1. Answer all questions

(1X12=12 Marks)

- Find 1's complement of 01111110
- Convert $(0.513)_{10}$ to octal.
- State Demorgan's Laws?
- What are the basic operations in Boolean Algebra?
- What is a code convertor?
- Which gates are called the Universal Gates? Why?
- What is a literal?
- Differentiate between a latch and a Flip Flop
- What are different types of RAM?
- What is a trigger?
- What is meant by PLA?
- Distinguish between Synchronous and Asynchronous counter.

UNIT I

- Find the simplified sum of the products expression using K-map for the function
 $F = \sum m(7, 9, 10, 11, 12, 13, 14, 15)$ 6M
 - Perform the 1's and 2's complement of the following binary numbers
 i) 11101010 ii) 01111110 iii) 00000001 iv) 10000000 6M

(OR)

- Reduce the following expression to the simplest possible POS and SOP forms
 $f = \sum m(6, 9, 13, 18, 19, 25, 27, 29, 31) + d(2, 3, 11, 15, 17, 24, 28)$ 8M
 - Reduce the following expressions using a four-variable K-map $A\bar{B}C + \bar{A}BC\bar{D} + AB\bar{C}D + ABC$ 4M

UNIT II

- Obtain the set of prime implicants for the Boolean expression $f = \sum m(0, 1, 6, 7, 8, 9, 13, 14, 15)$ using the tabular method? 6M
 - Implement Full-Subtractor using two Half-Subtractors and OR Gate. 6M

(OR)

- Prove that i) $(\overline{AB} + \overline{AC})(BC + B\bar{C})(ABC) = 0$ ii) $\overline{ABC}(\overline{A+B+C}) = \bar{A}\bar{B}\bar{C}$ 6M
 - Design a code converter that converts 4-bit binary to Gray code? 6M

UNIT III

- Show the logical diagram of a clocked RS Flip Flop with four NAND gates. 6M
 - Explain the conversion of i) J-K flip flop in to S-R flip-flop ii) T-flip flop to J-K flip-flop 6M

(OR)

- With a neat diagram explain the working of SR-flip flop with characteristic table, excitation table and characteristic equation 6M
 - Explain in detail about Master-Slave Flip Flop with a logical diagram. 6M

UNIT IV

- Design an 4-bit up/down counter using D-Flip Flops. 6M
 - Explain the working of bi-directional shift register with a neat diagram 6M

(OR)

- Compare the programmable features of PAL, PLA and PROM devices. 8M
 - Realize the function $F1 = \sum m(1, 2, 4, 6)$ using PROM of size 8×3 . 4M