Hall Ticket Number:

II/IV B.Tech (Supply) DEGREE EXAMINATION
APRIL, 2018
(First Semester)
CSE/IT
(Computer Organization)

Time: Three Hours **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48)

1. Answer all questions (12X1=12 Marks)

a) Define MIPS Rate.
b) What is register indirect addressing mode? When it is used.
c) Differentiate between RISC and CISC.
d) For the given, 1) Pipelining with operand forwarding and out-of-order execution. 2) Simple Pipelining 3) Super scalar execution 4) Non-pipelining.
Arrange the above 4 concepts ascending order based on No of Cycles.
e) What is DMA? Mention it's advantages.
f) Define the terms hit, miss and ratio with respect to cache.
g) What is meant by data hazards in pipelining?
h) What is a Range of 2s Compliment numbering system?
i) What is the role of program Counter(PC) and IR(Instruction Register) ?
j) What are the various types of operations required for instructions?
k) Specify the three types of the DMA transfer techniques?
l) How the interrupt is handled during exception?

UNIT – I

2. A) What are the basic functional units of a computer? Explain the operational concepts of a computer with a neat sketch. **(6M)**

B) Write the assembly language instructions for the following code using the instruction set Move, Compare, Add, Subtract and Branch. Assume that every instruction can have utmost one memory location and the word size is 32 bits. If the memory address of the first instruction is 1000, calculate the memory address of all the instructions.

```
int a,b,c;
if(a==b)
c=a+b
else
 c=a-b;
```

(6M)

(OR)

3. a) Explain Shift and Rotate instructions. **(6M)**

b) What is an addressing mode? Explain various addressing modes with examples. **(6M)**

UNIT – II

4. a) Differentiate between Single channel and Multi channel bus. **(6M)**
b) Compare Hardwired control unit and Micro programmed control unit **(6M)**

(OR)

5. a) Explain about IEEE-754 single precision and Double precision methods. **(6M)**
b) Multiply 11010 with 10110 using booths algorithm. **(6M)**

UNIT – III

6. In a 64-Bit Computer System, The Size of Cache memory is 1 GB and Main memory size is 4GB and Each Block is having 16 Words and Each Word is having 32 Bytes. Then Calculate the No of Blocks in Cache Memory and Main Memory. And also Calculate No of bits for Tag, Block/Set, Word and Byte bits in a given Address in Direct Mapping and 8-way set associative Mapping.

Note: CM/MM divided into blocks, Blocks divided into words, Words into bytes. **(12M)**

(OR)

7. For the Given Assembly level program, List out the Data Hazards on the operands for the given instructions. And also Calculate the No of Cycles using pipelining and 4-tier Superscalar pipelining architecture.
Note: For Executing Each instruction, It has 5 stages, IF, ID, OF, EX, WB. and EX stage takes 2 cycles for Load and Store, 3-cycles for ADD and SUB, 4- Cycles for MUL, remaining stages takes one cycle.

Load A,R1
Load B, R2
Load C R3
Add R1,R2,R3
Sub R2,R1,R3
Store R3,C
Mul R1,R3,R2
Store R2,B

(12M)

UNIT – IV

8. (a) What are the different kinds of I/O Communication techniques? What are the relative advantages and disadvantages? **(6M)**

(b) Explain Different kind interruption handling mechanisms, What is DMA role in interruption handling mechanisms. **(6M)**

(OR)

9. Explain the following I/O Interface standards in detail. a) PCI b) SCSI c)USB **(3 X 4=12M)**