14CS303/14IT303

Hall Ticket Number:

II/IV B.Tech (Supplementary) DEGREE EXAMINATION

April, 2017 — **Common to CSE & IT**

Third Semester — **Digital Logic Design**

Time: Three Hours — **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1. Answer all questions (1X12=12 Marks)
   a) Find 1's complement of 01111110
   b) Convert $(0.513)_{10}$ to octal.
   c) State Demorgan's Laws?
   d) What are the basic operations in Boolean Algebra?
   e) What is a code convertor?
   f) Which gates are called the Universal Gates? Why?
   g) What is a literal?
   h) Differentiate between a latch and a Flip Flop
   i) What are different types of RAM?
   j) What is a trigger?
   k) What is meant by PLA?
   l) Distinguish between Synchronous and Asynchronous counter.

UNIT I

2. a) Find the simplified sum of the products expression using K-map for the function F = Σm(7, 9, 10, 11, 12, 13, 14, 15) 6M
   b) Perform the 1's and 2's complement of the following binary numbers i) 11101010 ii) 01111110 iii) 00000001 iv) 10000000 6M

(OR)

3. a) Reduce the following expression to the simplest possible POS and SOP forms f=Σm(6,9,13,18,19,25,27,29,31)+d(2,3,11,15,17,24,28) 8M
   b) Reduce the following expressions using a four-variable K-map $A\bar{B}C + \bar{A}BC\bar{D} + AB\bar{C}D + ABC$ 4M

UNIT II

4. a) Obtain the set of prime implicants for the Boolean expression f=Σm(0,1,6,7,8,9,13,14,15) using the tabular method? 6M
   b) Implement Full-Subtractor using two Half- Subtractors and OR Gate. 6M

(OR)

5. a) Prove that i) $(A\overline{B} + A\bar{C})(BC + B\bar{C})(ABC) = 0$ ii) $\overline{ABC}(\overline{A + B + C}) = \bar{A}\bar{B}\bar{C}$ 6M
   b) Design a code converter that converts 4- bit binary to Gray code? 6M

UNIT III

6. a) Show the logical diagram of a clocked RS Flip Flop with four NAND gates. 6M
   b) Explain the conversion of i) J-K flip flop in to S-R flip-flop ii) T-flip flop to J-K flip-flop 6M

(OR)

7. a) With a neat diagram explain the working of SR-flip flop with characteristic table, excitation table and characteristic equation 6M
   b) Explain in detail about Master-Slave Flip Flop with a logical diagram. 6M

UNIT IV

8. a) Design an 4-bit up/down counter using D-Flip Flops. 6M
   b) Explain the working of bi-directional shift register with a neat diagram 6M

(OR)

9. a) Compare the programmable features of PAL, PLA and PROM devices. 8M
   b) Realize the function F1=∑ m(1,2,4,6) using PROM of size 8×3. 4M