1811301

Hall Ticket Number:

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II/IV B.Tech (Regular / Supplementary)DEGREE EXAMINATION

February, 2021 — **Information Technology**

Third Semester — **Computer Organization & Architecture**

Time: Three Hours — **Maximum:** 50 Marks

Answer ALL Questions from PART-A. (1X10 = 10 Marks)

Answer ANY FOUR questions from PART-B. (4X10=40 Marks)

Part - A

1		Answer the following questions	(10X1 =10Marks)	
	a.	List the various computer types		COE1
	b.	What is mean by multicomputer?		COE1
	c.	What is meant by subroutine.?		COE1
	d.	Mention the commonly used condition code flags.		COE2
	e	What are the different kinds of DMA transfers		COE2
	f	Difference RAM and ROM.		COE3
	g	What is locality of reference?.		COE3
	h	Define hit ratio		COE4
	i	What is pipelining		COE4
	j	Define Hazard.		COE4

Part - B

2		Write the Assembler syntax and addressing functions of different types of addressing modes.	10M	COE1
3	a	List basic operations of control unit	5M	COE1
	b	Write the tasks performed by the system software.	5M	COE1
4	a	Write Control sequence for the instruction Add(R3),R1	5M	COE2
	b	Draw Micro program sequence instruction Flowchart of the instruction Add src, Rdst for indexed register addressing	5M	COE2
5	a	Draw the Diagram of DMA Controller and Explain?	5M	COE2
	b	Write the difference between I /O controlled transfer and DMA transfer?	5M	COE2
6		Multiply (-13) * 11 using Booth algorithm. Draw flow chart and Hardware implementation diagram	10	COE3
7	a	Explain **Associative** memory mapping technique.	5M	COE3
	b	How is Virtual memory influences to increase the effective size of the memory system	5M	COE3
8	a	Define Bus arbitration. Explain different types of Bus arbitration	5M	COE4
	b	Write the difference between Asynchronous bus and Synchronous bus	5M	COE4
9	a	How Microprocessor handling the multiple devices.	5M	COE4
	b	Write the sequence of events in handling interrupt	5M	COE4