

# DSM Quiz 2 Solutions

October 29, 2024

## Answer 1

### Subpart(a)

Full marks will be awarded if you write either of the cases.

#### Overlapping Case

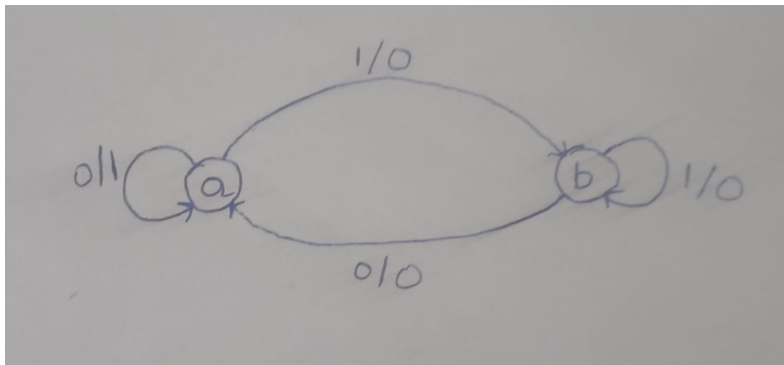


Figure 1: State transition diagram for detecting a double zero (Overlapping)

- State  $a$  denotes the state "0".
- State  $b$  denotes the state "1".

#### Non-Overlapping Case

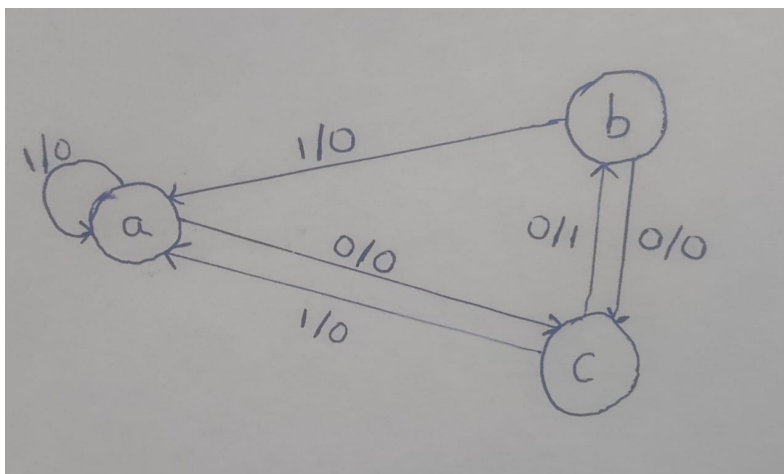


Figure 2: State transition diagram for detecting a double zero (Non-overlapping)

- State  $a$  denotes the state "00".
- State  $b$  denotes the state "10".
- State  $c$  denotes the state "01".

#### Grading scheme:

- 2 marks for correct state diagram for any of the 2 cases above. (Multiple answers might exist. All of them will be given full marks if they are correct) [Explanation doesn't carry any weightage if your diagram is correct]
- 1 mark if the state diagram is not clear/correct but a correct explanation is provided.
- 1 mark for a minor mistake in the state diagram.
- 0 marks in all other cases.

#### Subpart(b)

Full marks will be awarded if you write either of the cases.

#### Overlapping Case

In the overlapping case, we detect the sequence "00" even if it appears consecutively with overlapping bits. There are two states in total, and the state table is as follows:

Present State (Q)	Input (I)	Next State (Q')	Output
0	0	0	1
0	1	1	0
1	0	0	0
1	1	1	0

In this state table: - When the present state is 0 and the input is 0, the next state remains 0 and the output is 1, indicating that the sequence "00" has been detected.  
- For other inputs, the next state transitions accordingly and the output remains 0.

#### Non-Overlapping Case

In the non-overlapping case, we detect the "00" sequence only once for each distinct occurrence, ensuring no overlap. We use two states,  $X$  and  $Y$ , to represent the current state of the system. The state meanings are as follows:

- State 00: This state indicates that we have detected no zeros currently.
- State 01: This state indicates that we are currently on a single zero (i.e., the first zero in a possible "00" sequence has been detected).
- State 10: This state indicates that we have detected 2 zeros, and we are waiting for a new potential sequence.

The state table for this case is given below:

$X$ (Present)	$Y$ (Present)	Input (I)	$X'$ (Next)	$Y'$ (Next)	Output
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	$X$	$X$	$X$
1	1	1	$X$	$X$	$X$

Here: - When  $X = 1$  and  $Y = 0$  and the input is 0, the output is 1, indicating that a non-overlapping "00" has been detected. - The system transitions between states depending on the input to avoid detecting the sequence in an overlapping manner.

#### Grading scheme:

- 2 marks for a correct state table for either of the two cases above, provided it aligns with the drawn transition diagram.
- 1 mark if the state table is accurate but does not correspond to the transition diagram.
- 1 mark for minor errors in the state table and the state table corresponds to the transition diagram drawn.
- 0 marks in all other cases.

#### Subpart(c)

Full marks will be awarded if you write either of the cases.

#### Overlapping case

The JK flip-flop input conditions based on the state transitions are as follows:

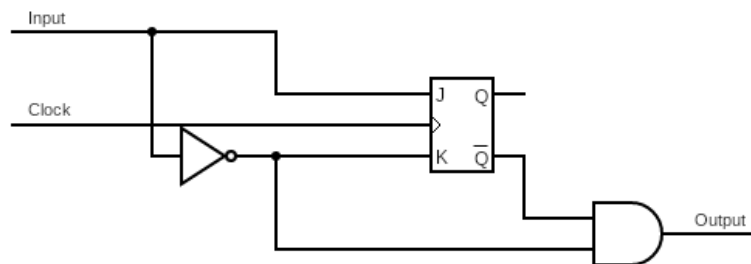
Present State (Q)	Input (I)	Next State (Q')	J	K	Output
0	0	0	0	X	1
0	1	1	1	X	0
1	0	0	X	1	0
1	1	1	X	0	0

Given the above state table, we get the expressions:

$$J = I$$

$$K = \bar{I}$$

$$\text{Output} = \bar{Q} \cdot \bar{I}$$



#### Non-Overlapping case

The JK flip-flop input conditions for  $X$  and  $Y$  are as follows (P = Present State, N = Next State):

For  $X$ :

$X(\text{Present})$	Input (I)	$X'(\text{Next})$	$J_X$	$K_X$
0	0	1	1	$X$
0	1	0	0	$X$
1	0	0	$X$	1
1	1	0	$X$	1

For Y:

$Y(\text{Present})$	Input (I)	$Y'(\text{Next})$	$J_Y$	$K_Y$
0	0	0	0	$X$
0	1	1	1	$X$
1	0	0	$X$	1
1	1	1	$X$	0

$X(P)$	$Y(P)$	Input (I)	$X'(N)$	$J_X$	$K_X$	$Y'(N)$	$J_Y$	$K_Y$	Output
0	0	0	0	0	$X$	1	1	$X$	0
0	0	1	0	0	$X$	0	0	$X$	0
0	1	0	1	1	$X$	0	$X$	1	1
0	1	1	0	0	$X$	0	$X$	1	0
1	0	0	0	$X$	1	1	1	$X$	0
1	0	1	0	$X$	1	0	0	$X$	0
1	1	0	$X$	$X$	$X$	$X$	$X$	$X$	$X$
1	1	1	$X$	$X$	$X$	$X$	$X$	$X$	$X$

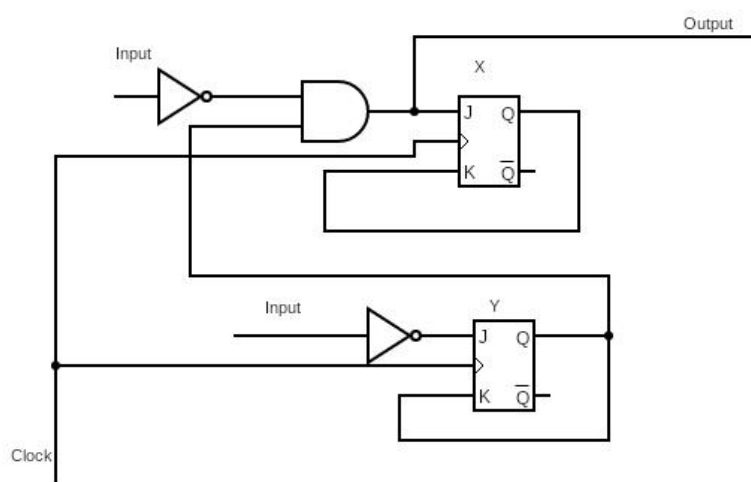
$$J_x = Y \cdot \bar{I}$$

$$K_x = X \text{ (or 1)}$$

$$J_y = \bar{I}$$

$$K_y = Y \text{ (or 1)}$$

$$\text{Output} = Y \cdot \bar{I}$$



### Grading scheme:

Full marks will be given for a correct circuit diagram with correctly labelled inputs and outputs (for both overlapping and non-overlapping case).

## Answer 2

### (a) SR Latch vs. JK Flip-Flop

#### SR Latch

- The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled S and R.
- We realize that the outputs  $Q$  and  $Q'$  are normally the complement of each other.
- The latch has two stable states.
- When the output  $Q = 1$  and  $Q' = 0$ , the latch is said to be in the set state.
- When  $Q = 0$  and  $Q' = 1$ , it is in the reset state.
- Setting and resetting can be done through the two inputs (S and R).
- After setting or resetting, applying 00 at the input retains the previous state.
- However, when both inputs are equal to 1 at the same time, a condition in which both outputs are equal to 0 (rather than be mutually complementary) occurs.
- If both inputs are then switched to 0 simultaneously, the device will enter an unpredictable or undefined state or a metastable state.

#### JK Flip-Flop

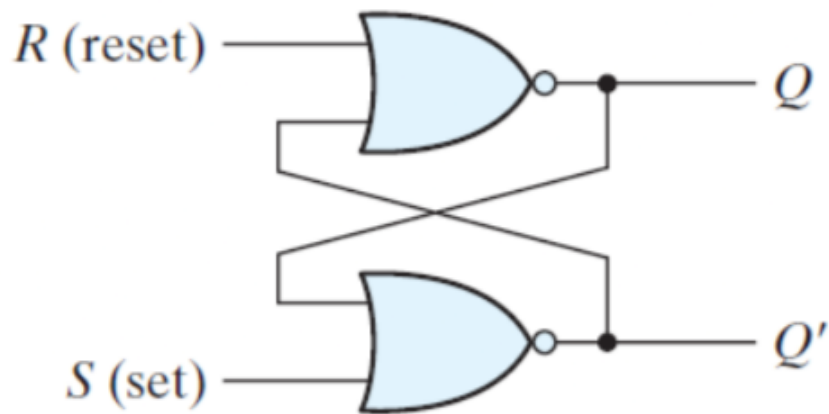
- There are four operations we are looking to perform in a flip-flop: set it to 1, reset it to 0, retain or complement its output.
- With only a single input, the D flip-flop can set or reset the output, depending on the value of the D input immediately before the clock transition.
- Synchronized by a clock signal, the JK flip-flop has two inputs and performs all four operations.
- The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented.
- This can be obtained if the D input is:

$$D = JQ' + KQ$$

- When  $J = 1$  and  $K = 0$ ,  $D = Q' + Q = 1$ , so the next clock edge sets the output to 1.
- When  $J = 0$  and  $K = 1$ ,  $D = 0$ , so the next clock edge resets the output to 0.
- When both  $J = K = 1$  and  $D = Q'$ , the next clock edge complements the output.
- When both  $J = K = 0$  and  $D = Q$ , the clock edge leaves the output unchanged.
- Because of their versatility, JK flip-flops are called universal flip-flops.

#### Grading Scheme

- 1 mark for description of JK FlipFlop and SR Latch
- 1 mark if comparisons are done.



$S$	$R$	$Q$	$Q'$	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$ )
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$ )
1	1	0	0	(forbidden)

5

### (b) Shift Register vs. Parallel Register

Shift Register	Parallel Register
Moves data bits sequentially	Transfers data bits simultaneously
Pros: Simple, good for serial data	Pros: Faster data transfer
Cons: Slower due to sequential operation	Cons: More complex wiring

#### Grading Scheme

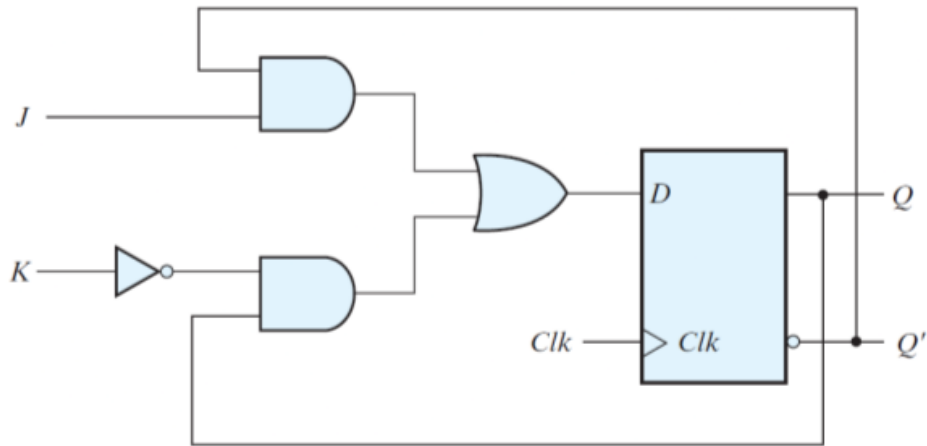
- 1 mark for description of shift and parallel registers
- 1 mark for pros and cons.

### (c) Equivalent States

*Two states are equivalent if they produce the same output for every possible input sequence. This concept helps in minimizing state machines.*

#### Grading Scheme

- 1 mark if the answer is correct
- 0 in all other cases



(a) Circuit diagram

### ***JK Flip-Flop***

<b><i>J</i></b>	<b><i>K</i></b>	<b><i>Q(t + 1)</i></b>	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

Figure 16

9

### **(d) Synchronous Reset**

*A synchronous reset occurs in sync with the clock signal. The reset action only takes place when the clock edge occurs, making the operation predictable and avoiding glitches.*

### **Grading Scheme**

- 1 mark if the answer is correct
- 0 in all other cases

## **Answer 3**

Design a 4-bit universal shift register using T flip-flops and explain its operation. [5M]

A normal universal shift register using D-flip flops:

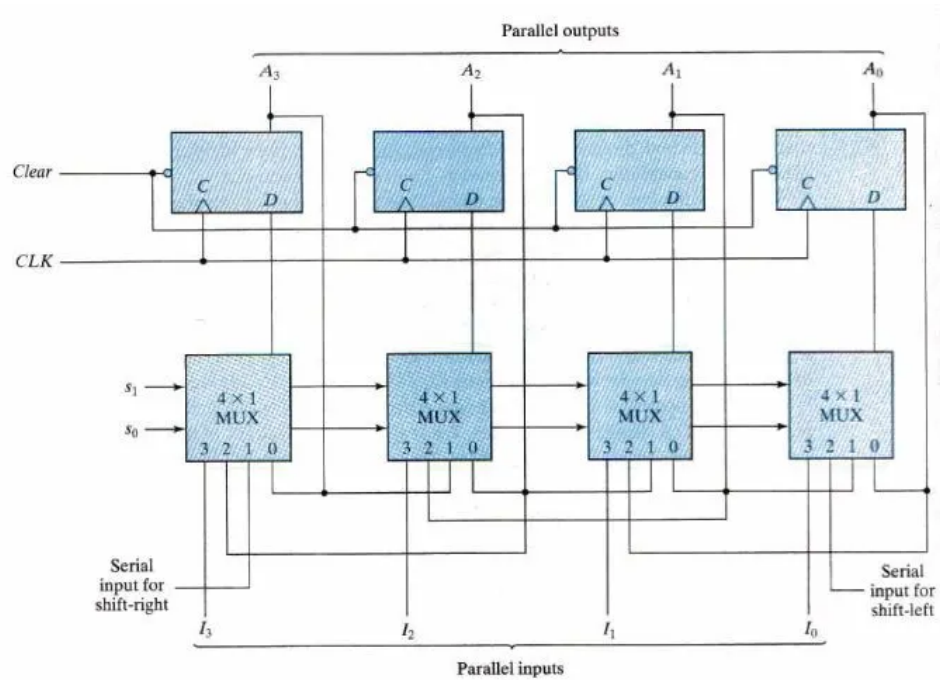


Figure 3: Using D flip-flops

Using a T-Flip flop instead of D-Flip flop:

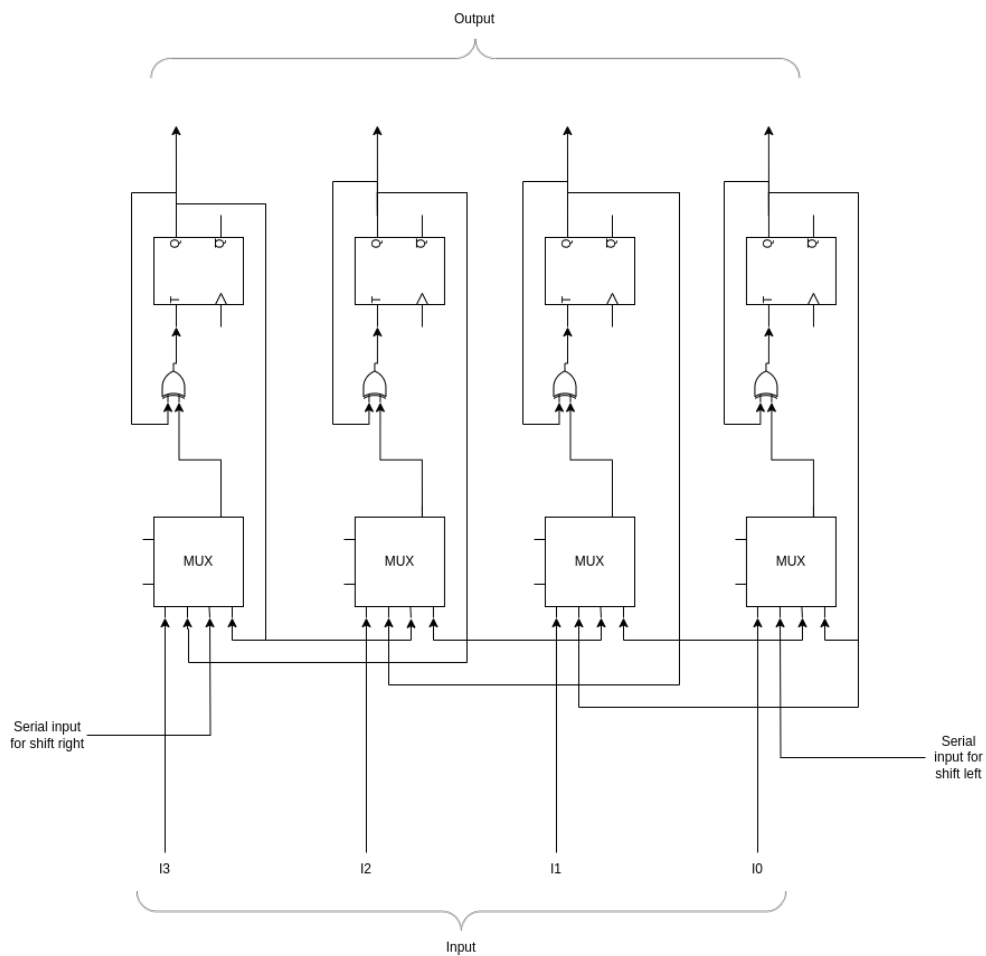


Figure 4: Using T-flip flops



**Explanation:**

Since, T flip flop works on the basis of toggling, when T is 1 then the output is toggled, and when T is 0, output remains same. The working of a D flip flop can be achieved using T flip flop simply by making  $T = Q(t) \oplus Q'(t + 1)$ , where Q' is the expected output

**Grading scheme:  $[[1.5 + 1.5] + 2]$** 

- 1.5 For writing the MUX layer correctly, i.e inputs to mux must be in correct order.
- 1.5 For writing the XOR gates and T flip-flop layer correctly.
- 2 For a valid explanation Of using the XOR gate.