Prof: Abishek Srivastava, CVEST

23 Lectures
- 39 hours

Grading:

Assignment (3/4) : 10 %

Course Project : 20 %

Quiz : 10 % + 10 %

Midsem : 20 %

Endsem : 30 %

VLSI Design

Assignment Deadline: 6pm

VLSI Design

→ **Topics:-**

1) Intro to VLSI Design

2) CMOS Inverter

3) Multi-stage Logic Design and Optimization

4) Other logic styles

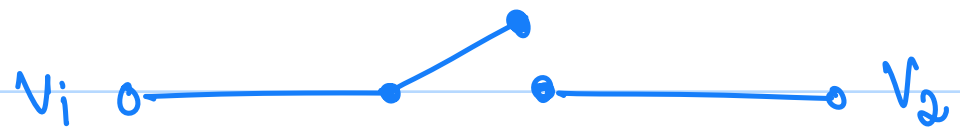
5) Intro. to HDL System Design.

- SCL - Semiconductor Complex Limited. Only Fabrication facility in India. Can do upto 180 nm CMOS. Located in Mohali.
  ↳ Considered a very old technology.

- We will be using 180 nm technology in this course, since it is now open-source.

→ **High impedance state:-**

- When a node is not connected to any well defined voltage, it is said to be existing in a high impedance state.

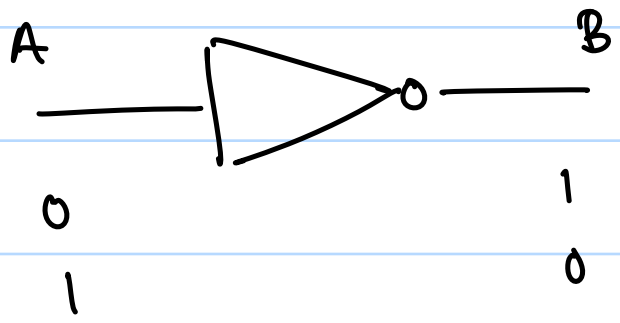


V_2 is in a high impedance state.

(Refer Wasta & Harris MOS T Physics for today's lecture)

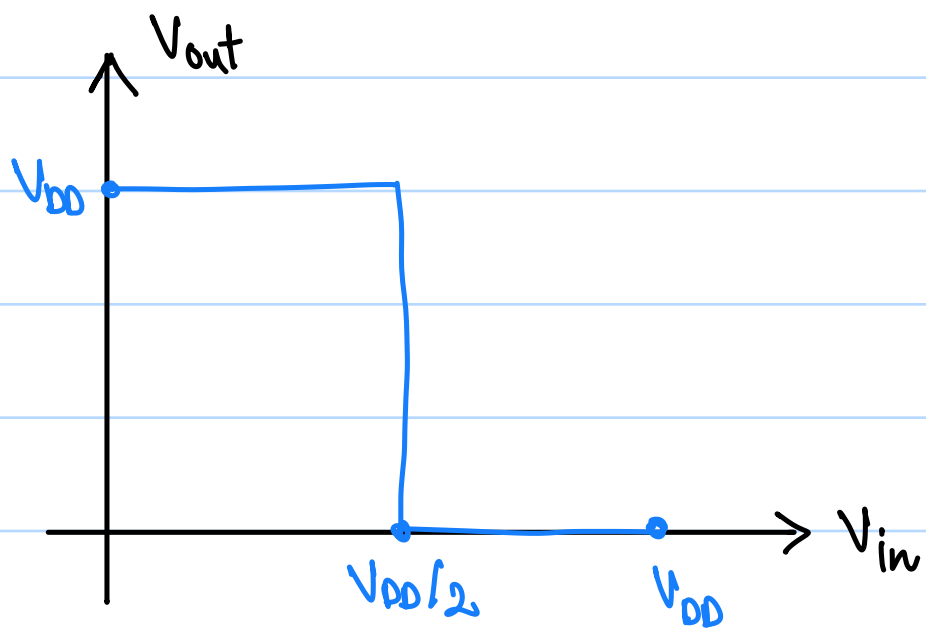
5/8/25

→ **Inverter :-**



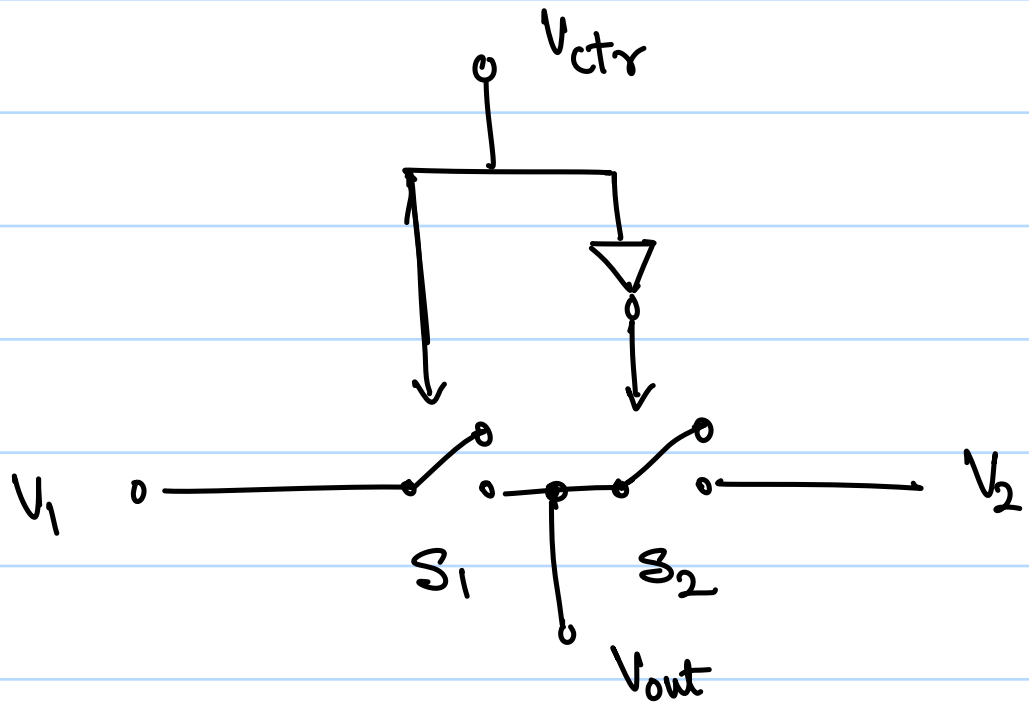
A	B
0	1
1	0

- 1 and 0 correspond to 2 different voltage levels.
- Ideally,



The above plot is termed as a VTC plot (Voltage Transfer Characteristics).

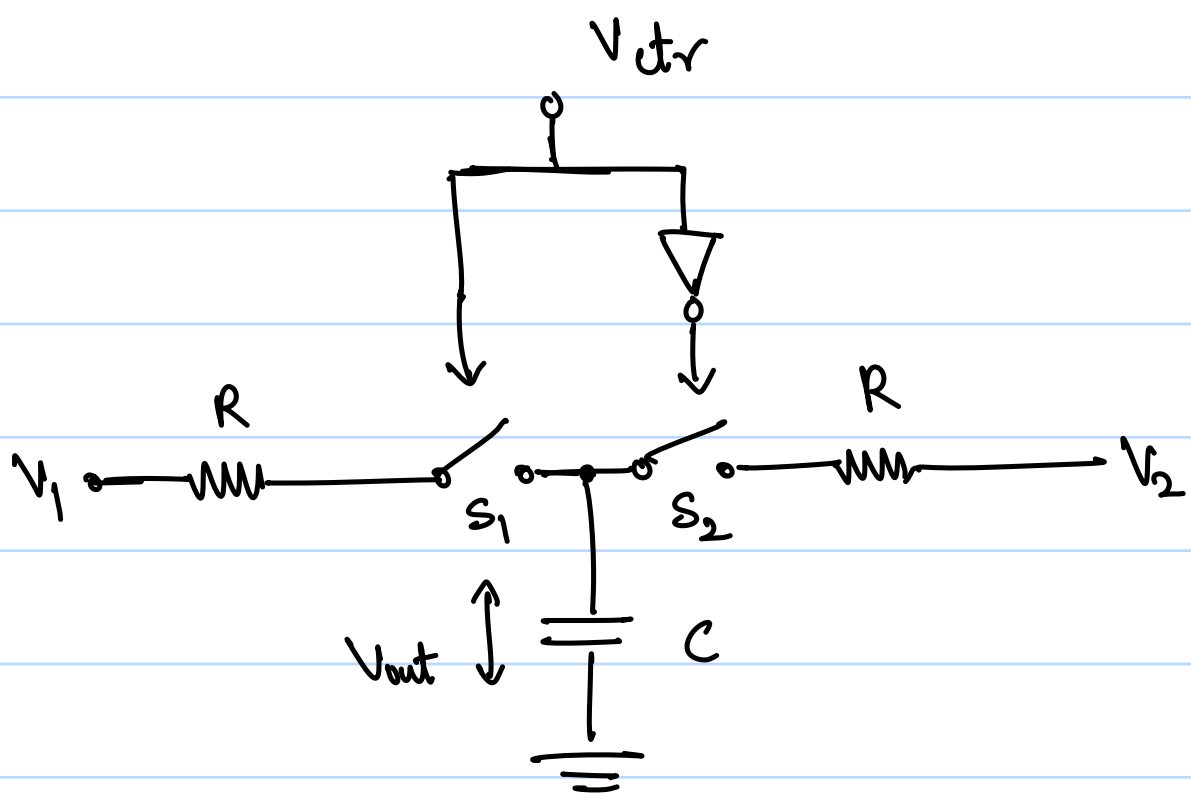
1)



Truth Table:

V_{ctl}	V_{out}
0	V_2
1	V_1

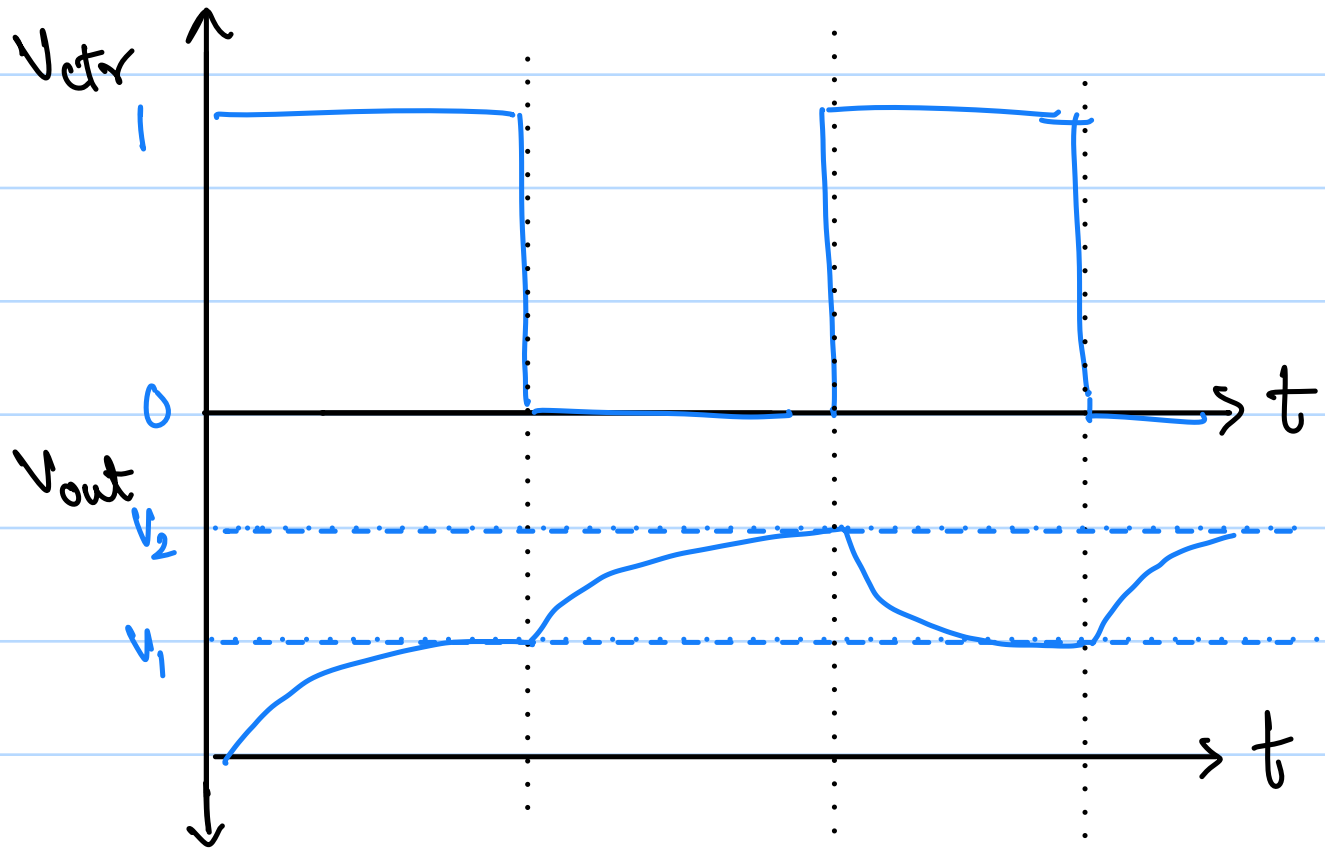
2)



Here, $V_{out} = \begin{cases} V_2(1 - e^{-t/RC}), & V_{ctr} = 0 \\ V_1(1 - e^{-t/RC}), & V_{ctr} = 1 \end{cases}$

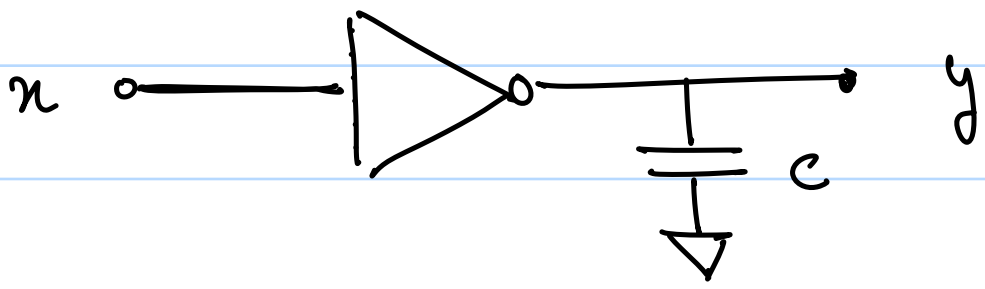
If there is no resistance involved, the current through the capacitor will be a Dirac impulse, infinite for an infinitesimal time.

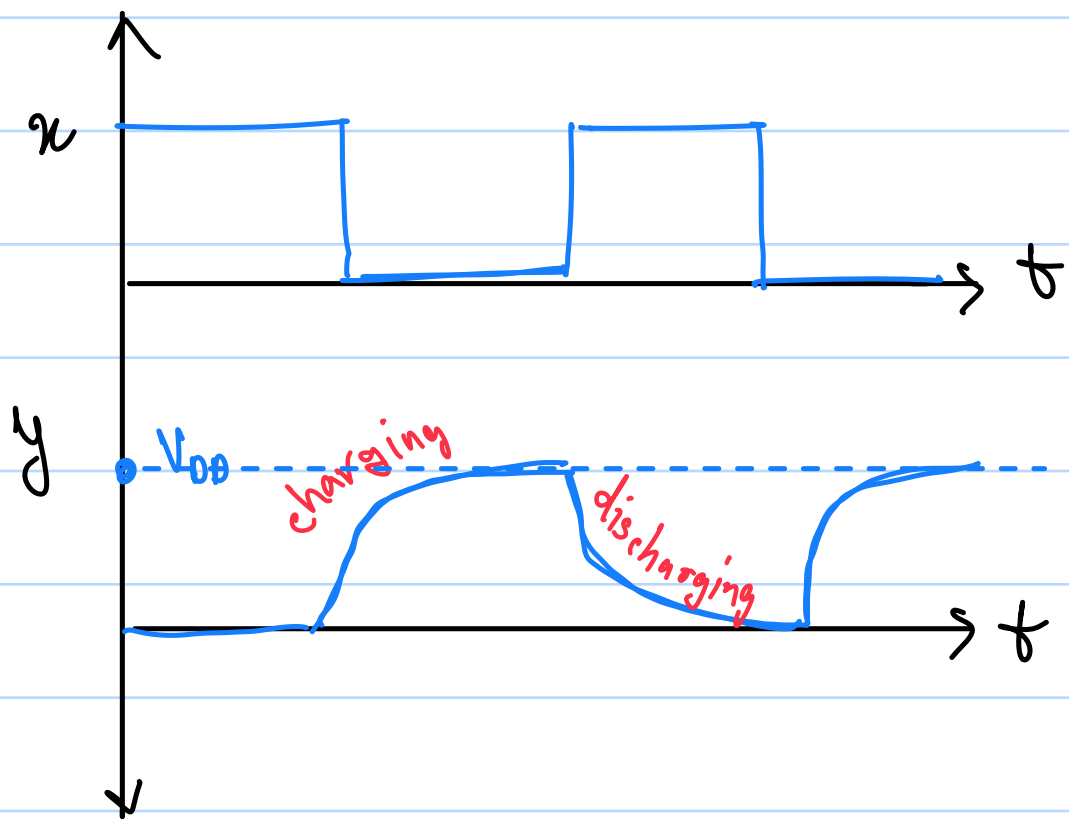
($i = C\frac{dV}{dt}$, dt is very small)



This is a timing diagram

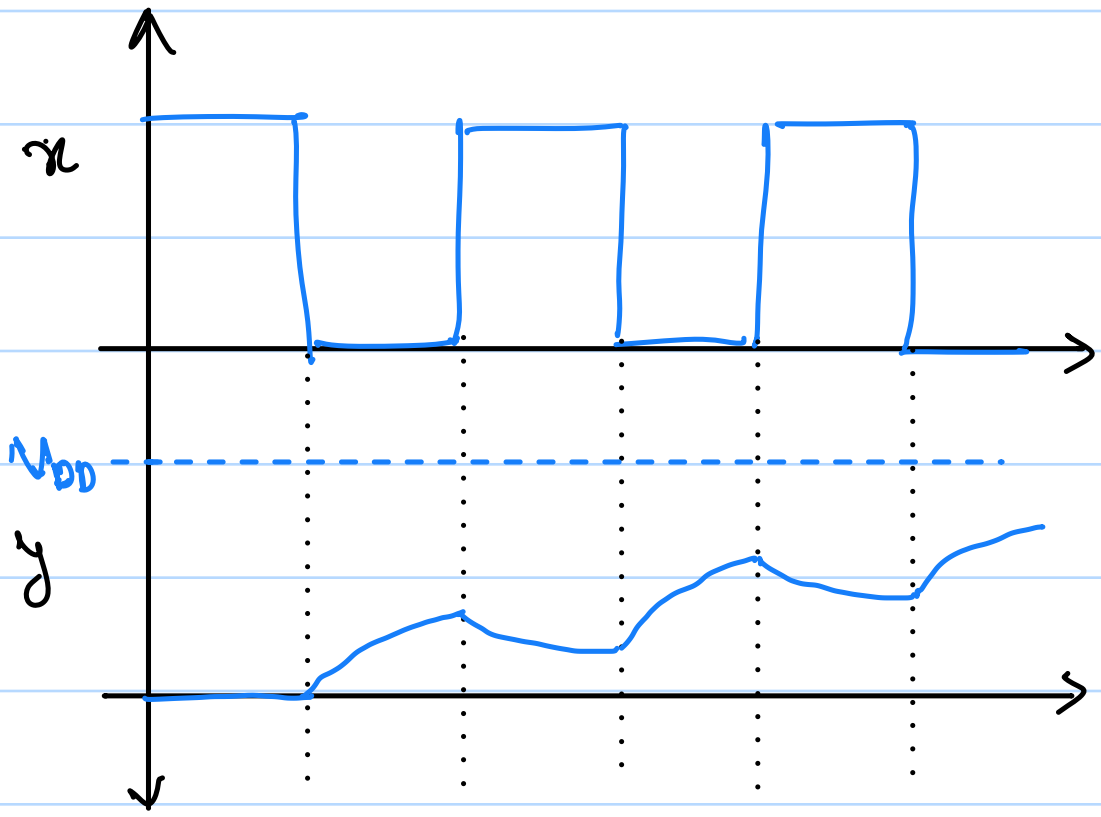
3)





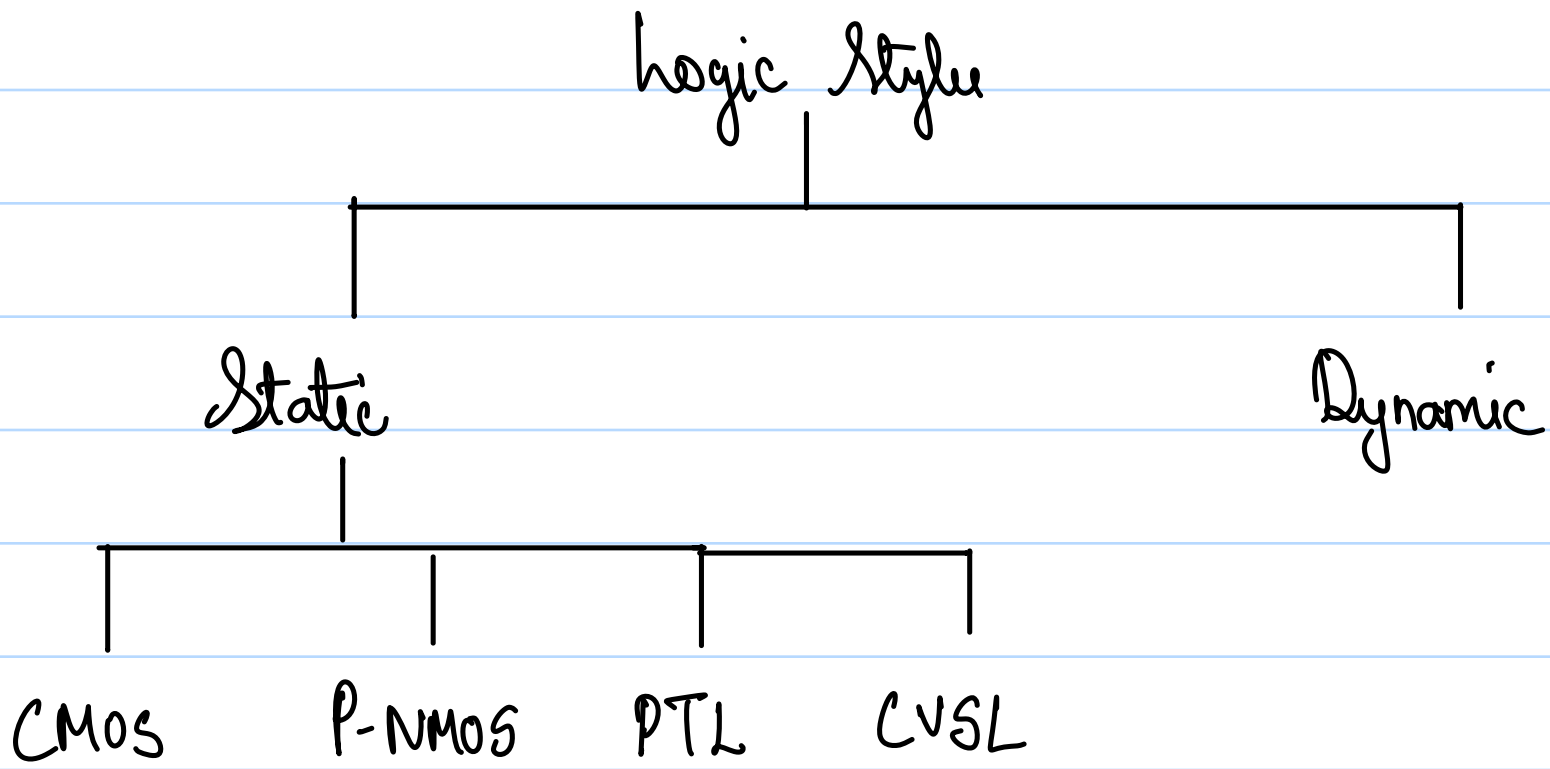
- The charging and discharging speeds of the capacitor are dependent on the RC / time constants of the circuit.

If RC is very large,



The capacitor is not fast enough to reach V_{DD} and zero, so information is lost.

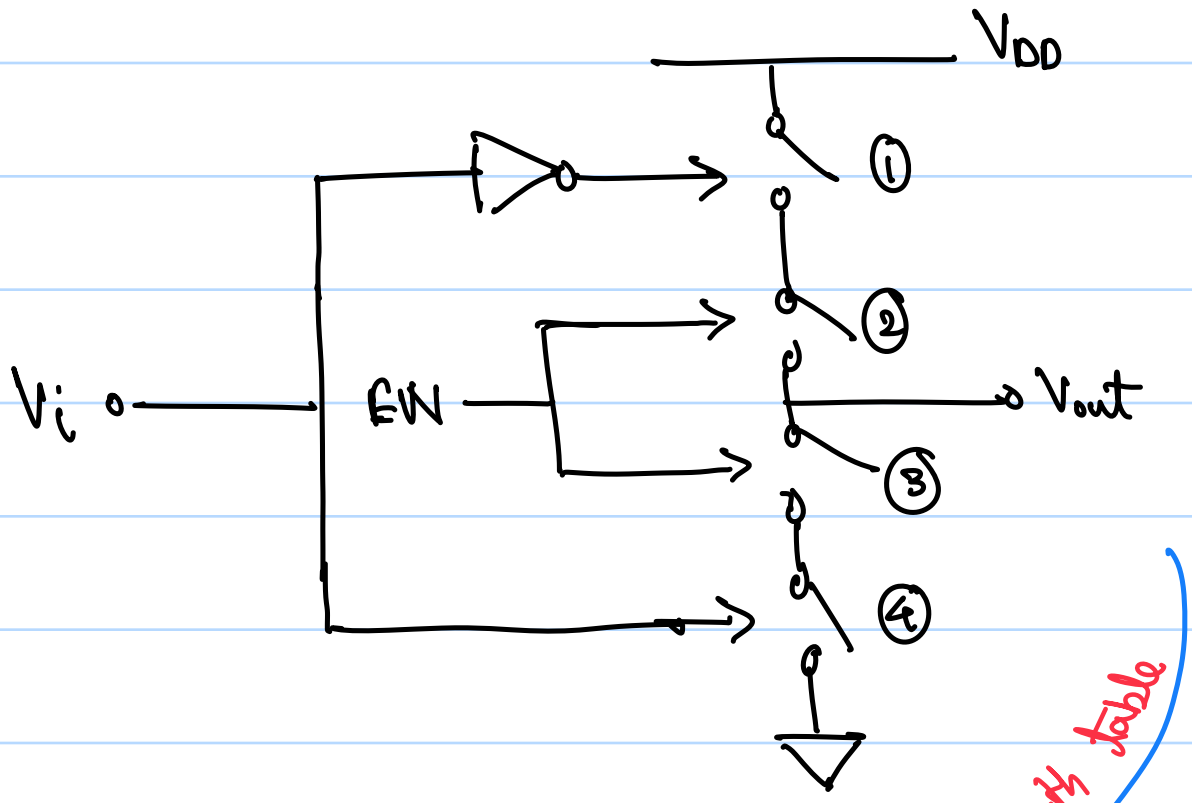
- Because of this, the RC parameters of the circuit must be fast enough to handle the input speed/frequency.



Circuit Design

- Combinational
- Sequential
- Memory

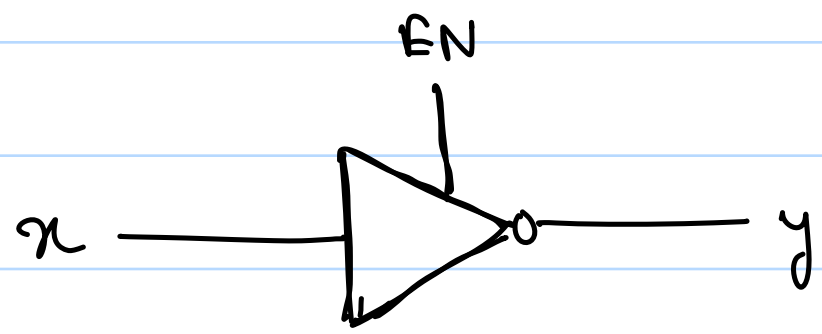
4)



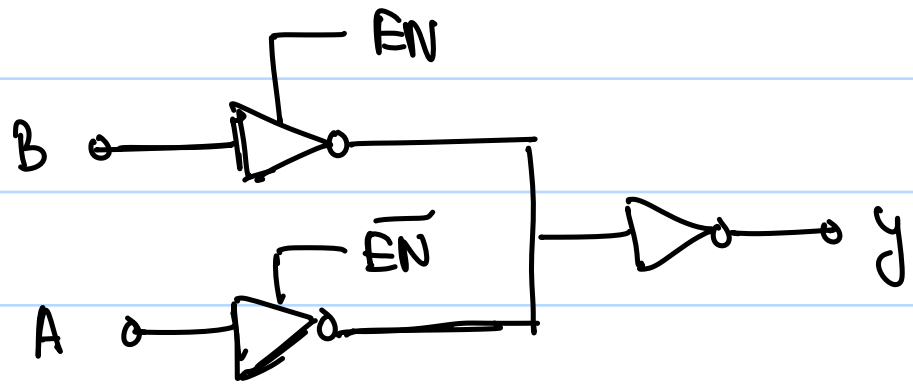
truth table

EN	V_i	V_o
0	0	Z
0	1	Z
1	0	V_{DD}
1	1	0

- The above device acts like an inverter if EN = 1. This is the design of a tri-state inverter.



5)

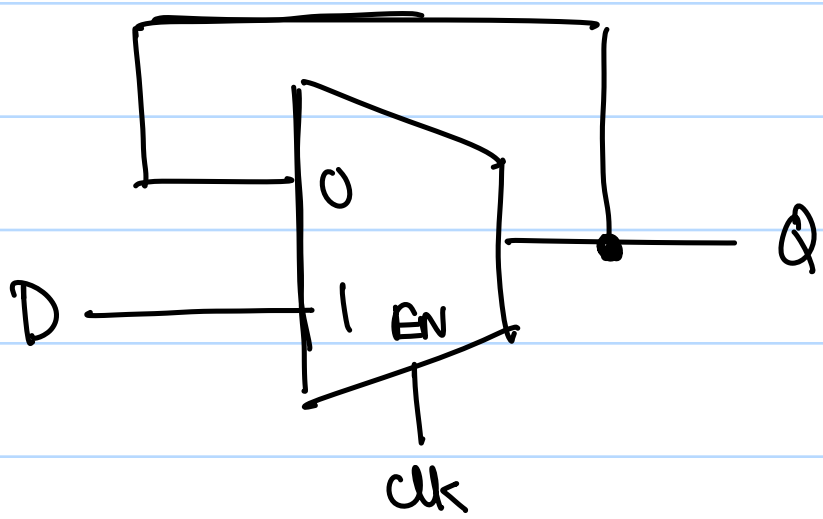


Truth table :

EN	y
0	A
1	B

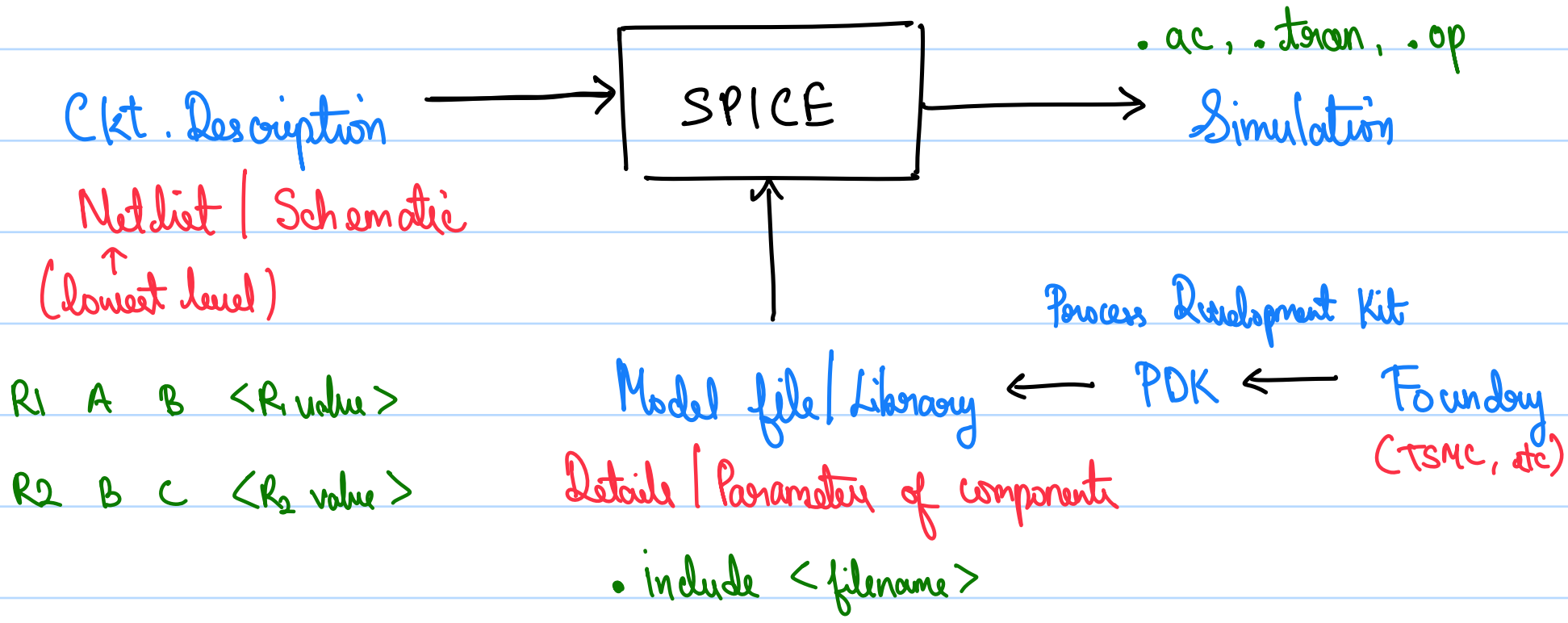
- Due to the high impedance, the output of one tri-state inverter will not be affected by the other, since one output is always Z.

- The above device will act as a 2×1 MUX, which can be used to design devices like gates and latches.



Level Triggered D-Latch

→ SPICE :-



R1 A B <R1 value>

R2 B C <R2 value>

→ Technology Node:

- To make a semiconductor chipset on a substrate, we use a "stencil" of the circuit layout.

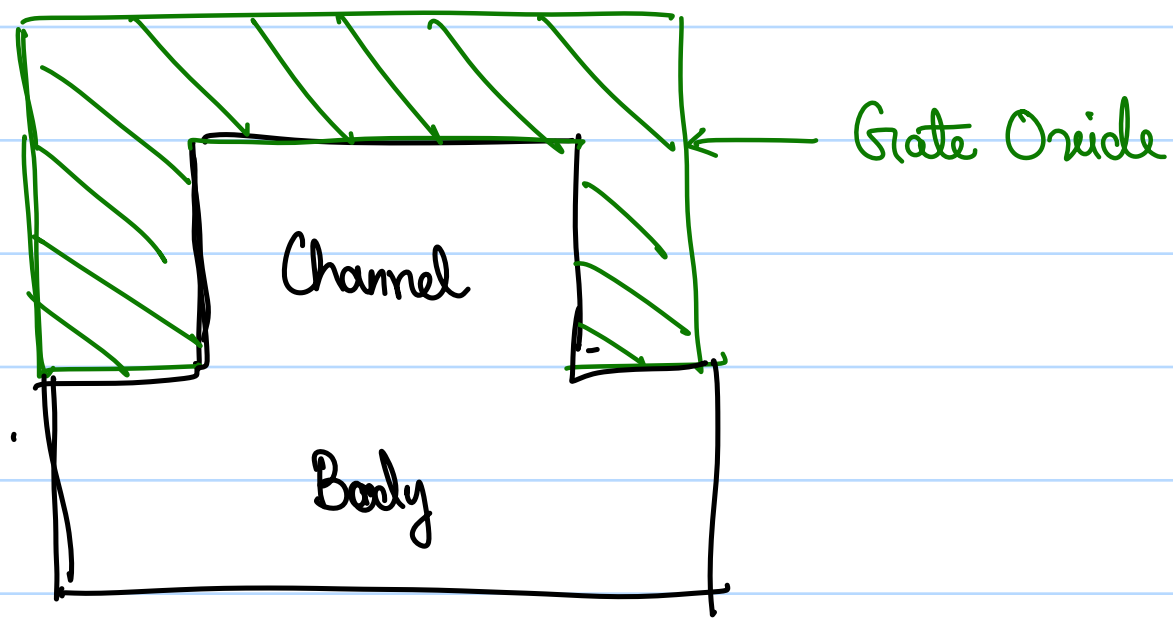
- In the chipset, there are multiple metal layers on top of the substrate, to provide the interconnections between the MOSFETs.

- Within the MOSFETs, there are multiple dimensions that vary between them, depending on the usage of that MOSFET

- The minimum of those dimensions, i.e., minimum feature length among the MOSFETs is deemed as the "technology node" of that MOSFET. Usually minimum channel length.

- 3nm (N3) node – Retail products released
  2nm (N2) node – Will release soon next year.

- < 22nm – FinFETs are used instead of MOSFETs.



View of FinFET through Source/Drain

In FinFETs, the oxide wraps around the channel, enabling better inversion at a lower gate potential, better than MOSFETs.

- A14 – 1.4nm node
  A7 – 0.7nm node } In development.

- 180 nm is still widely used, in devices that do not require extremely high computation.

- Lower transistor size => lower cost per transistor.

- <u>Clock Speed</u>:

  - Recently the clock speed of processes has saturated.

  - Since the packing density has increased by a lot, the heat and leakage of the transistors have increased by a lot.

- These factors made it difficult for clock speed to improve as fast as the technology node.

→ Shannon's Expansion :-

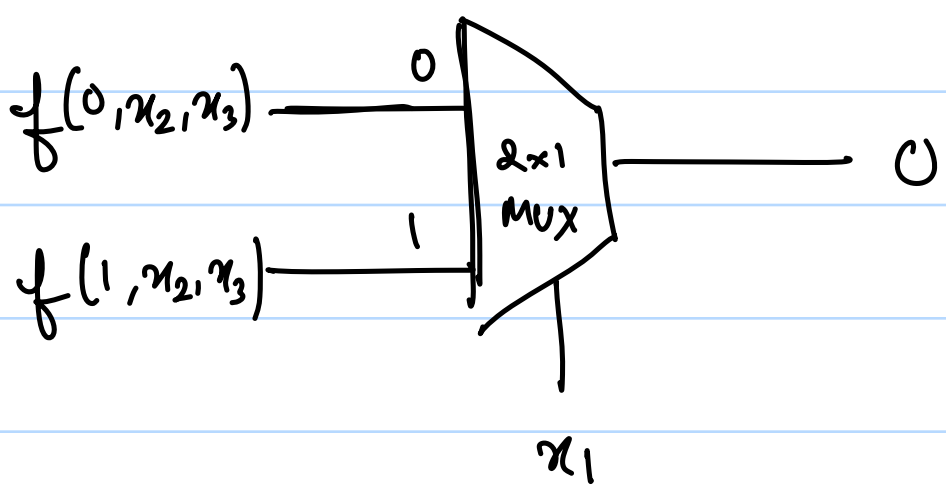
- For any function $f(x_1, x_2, x_3 \dots x_n)$,

$$f(x_1, x_2, x_3 \dots x_n) = x_1 f(1, x_2, x_3 \dots x_n) + \overline{x_1} f(0, x_2, x_3 \dots x_n)$$

Example: Expand $f(x_1, x_2, x_3) = \overline{x_1}\,\overline{x_3} + x_1 x_2 + x_1 x_3$ wrt x_1

$$\Rightarrow f(x_1, x_2, x_3) = x_1 (x_2 + x_3) + \overline{x_1} (\overline{x_3})$$

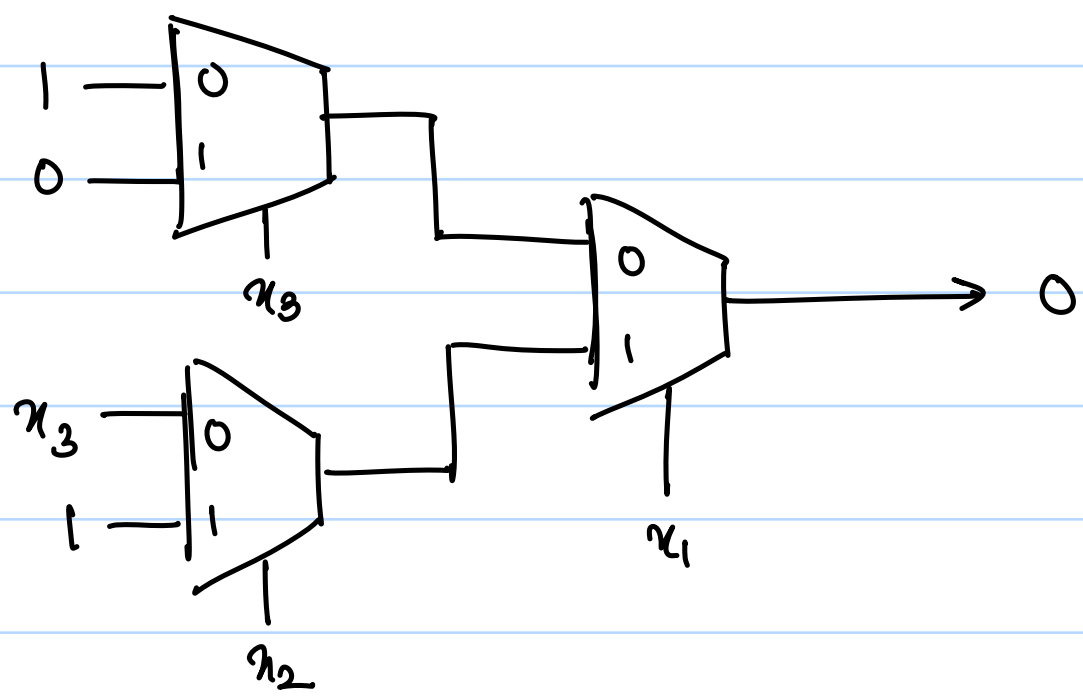
- If we expand the function in this way, we can use a 2×1 MUX to express the function, using x_1 as the selection variable.



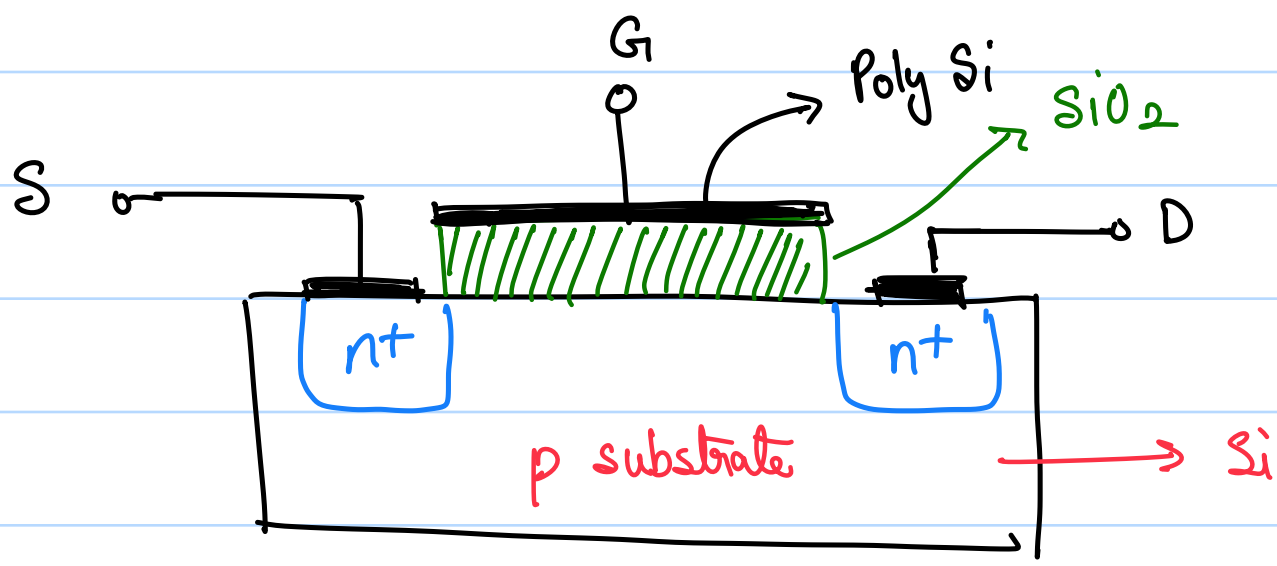
Example: Express the prev. function only using 2x1 MUXes.

$$f(x_1, x_2, x_3) = \overline{x_1}\,\overline{x_3} + x_1 x_2 + x_1 x_3$$
$$= x_1 (x_2 + x_3) + \overline{x_1} (\overline{x_3})$$

$$f(x_2, x_3) = x_2 + x_3$$
$$= x_2 (1) + \overline{x_2} (x_3)$$



→ MOSFETs :-

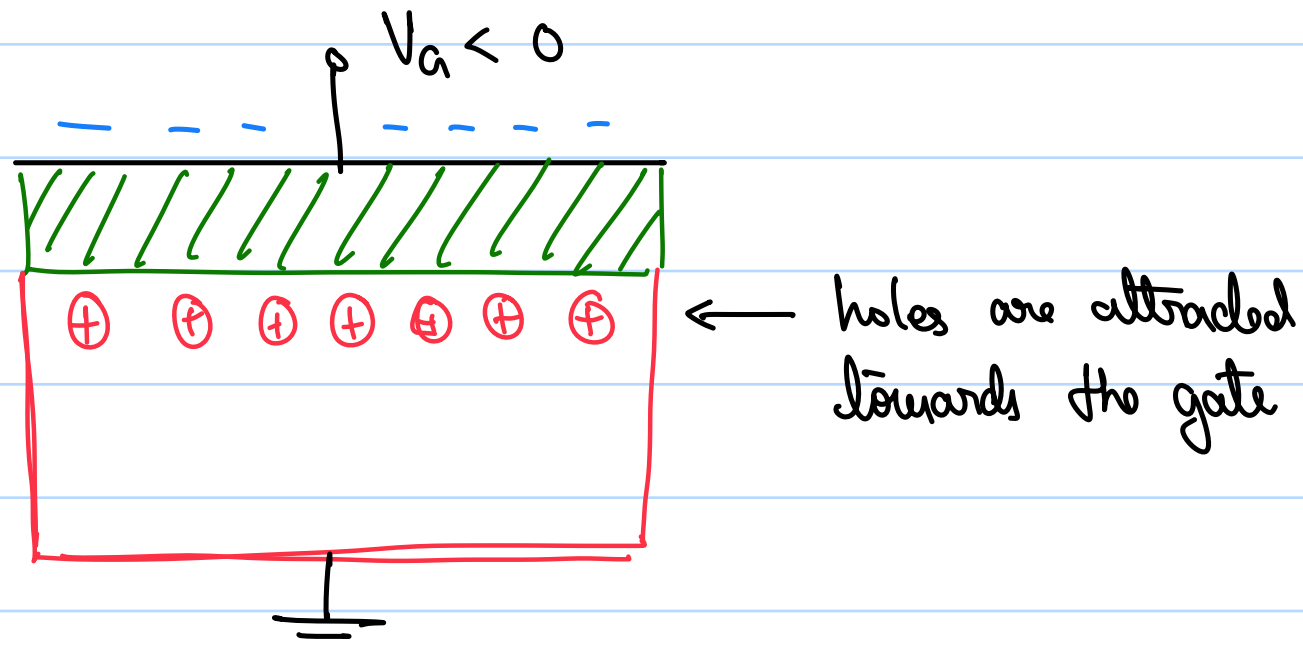


NMOS Structure

- Poly silicon is used in the gate terminal to simplify the manufacturing process, since silicon is the major element of a MOSFET.

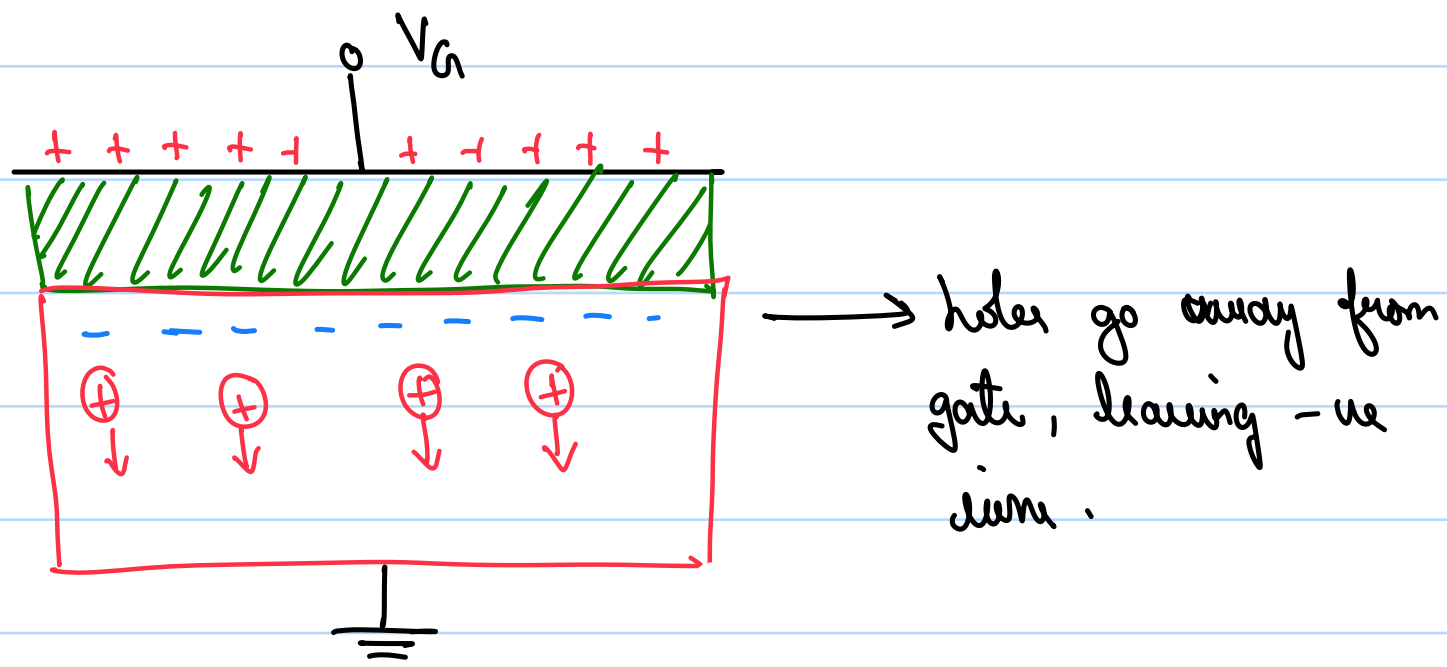
- Let S and D be grounded and,

1) $V_G < 0$



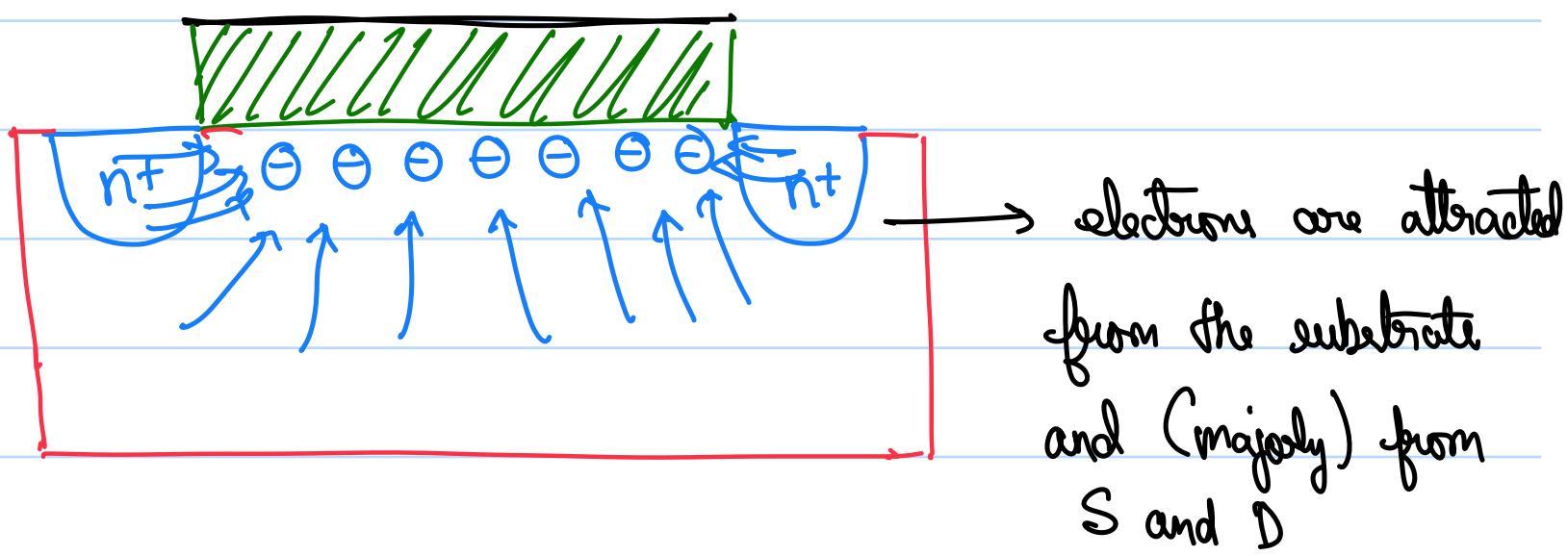
- This is accumulation mode of operation.

2) $V_G > 0$

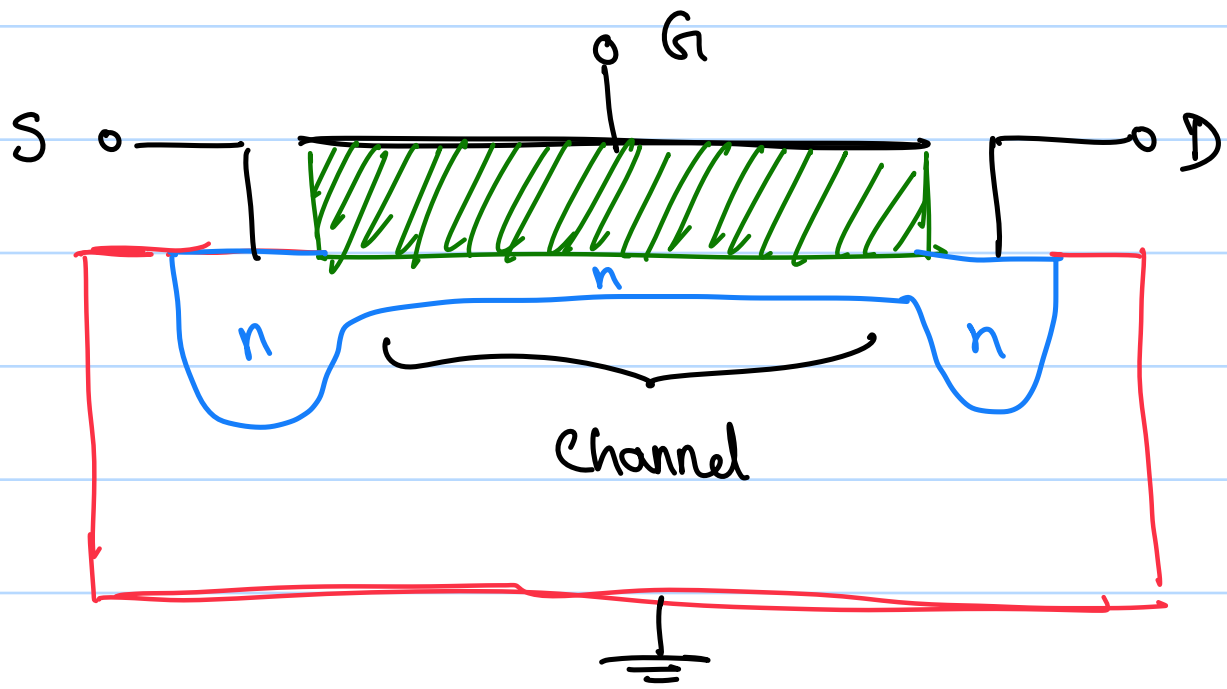


- This is depletion mode of operation.

3) $V_G >> 0$



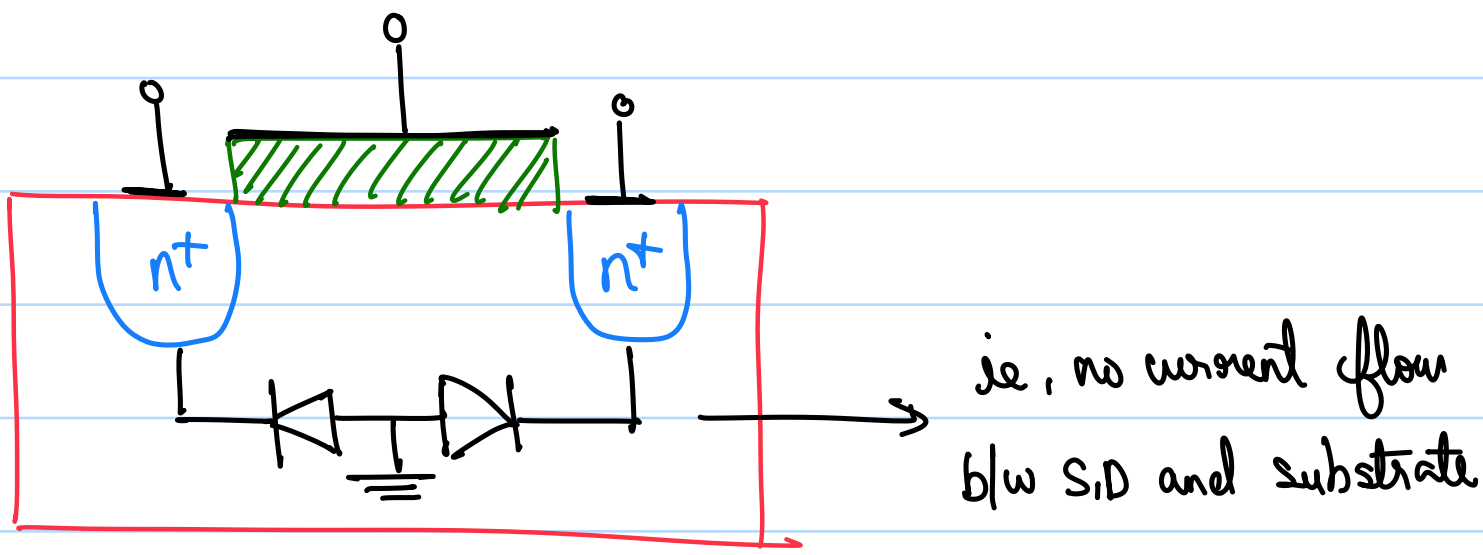
- The surface of the p-substrate becomes dominated by electrons, ie, becomes n-type.



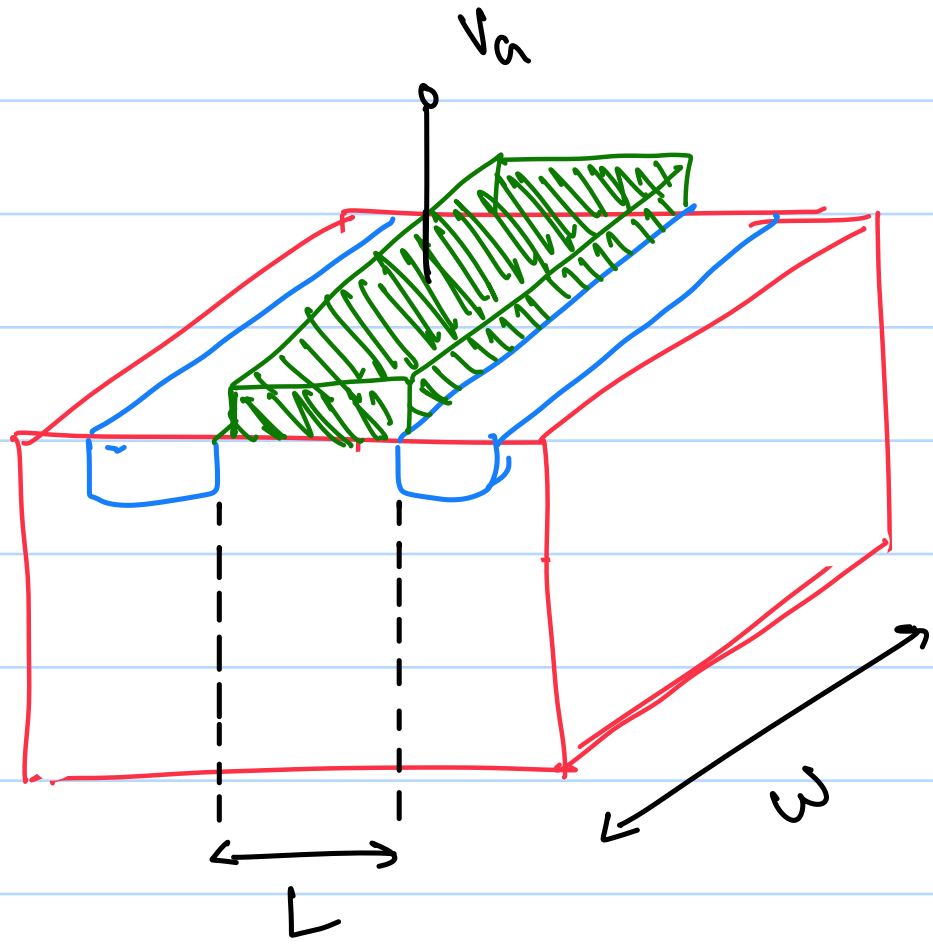
- This is inversion mode of operation.

- If n_e at surface $< N_A$ (hole conc. of substrate), it is weak inversion / subthreshold mode.

- If n_e at surface $\geq N_A$, it is strong inversion. The min. gate voltage to attain strong inversion is V_{TH} (threshold voltage)



- 3D View:-



Since the n-channel is not perfectly conductive, it has some resistance to it, depending on the dimensions L and W.

Based on V_{GS}
- Accumulation
- Depletion
- Inversion

Based on V_{DS}
- Linear
- Saturation

1) $V_{GS} \leq 0 \Rightarrow I_D = 0 \ \forall \ V_{DS}$. Accumulation mode has zero channel.

V_t - thermal voltage

2) $0 < V_{GS} < V_{TH} \Rightarrow I_D \approx I_{D0} e^{\frac{V_{GS} - V_{TH}}{nV_t}}$.
Subthreshold conduction.

3) $V_{GS} > V_{TH}$ & $V_{DS} < V_{GS} - V_{TH} = V_{OV}$. (Overdrive voltage)

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(2 V_{OV} V_{DS} - \frac{V_{DS}^2}{2}\right) \longrightarrow \text{Linear Mode of Opn.}$$

If $V_{DS} << V_{OV}$,

$$I_D = \left(\mu_n C_{ox} \frac{W}{L} V_{OV}\right) V_{DS}$$

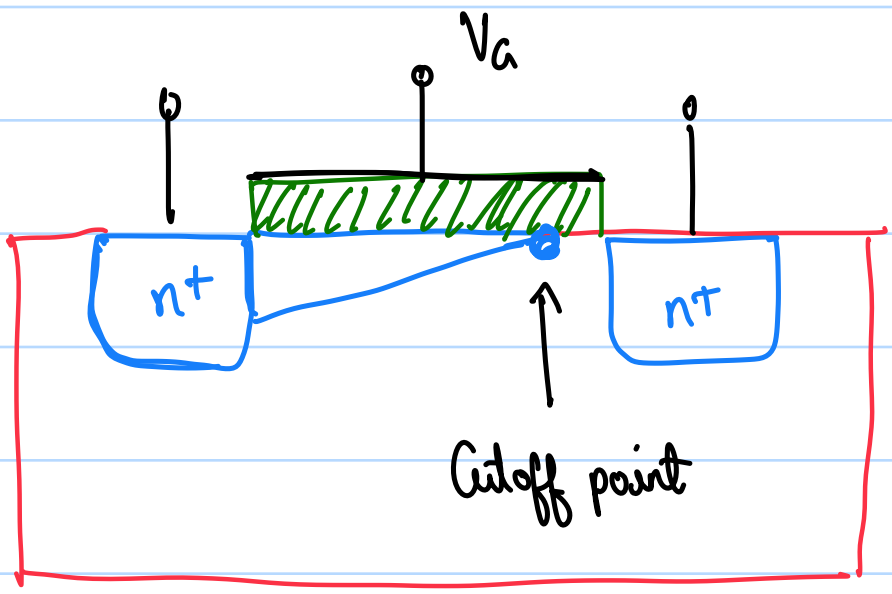
$$\Rightarrow \boxed{R = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{OV}}}$$

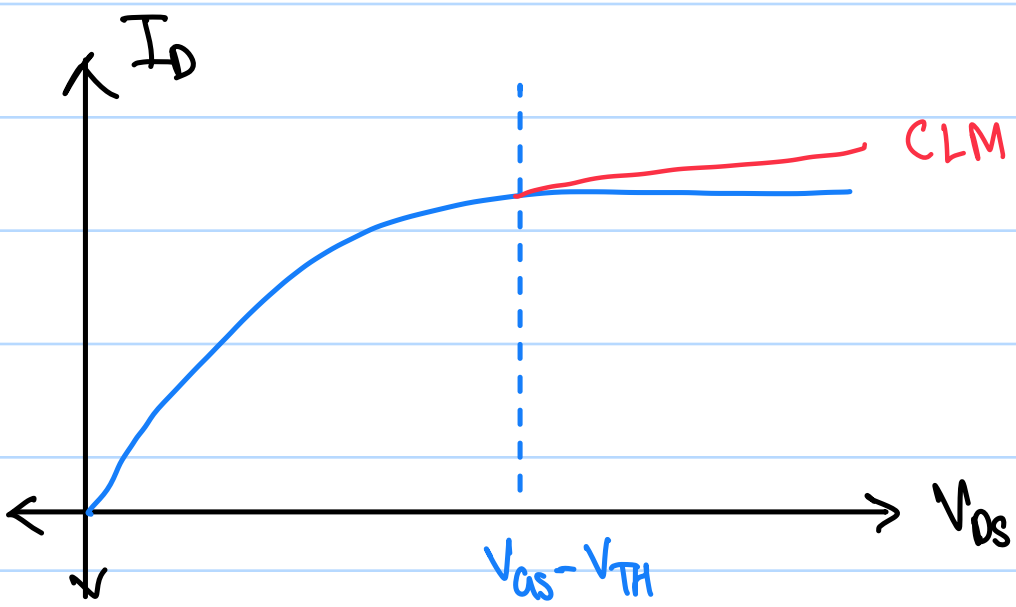
4) $V_{GS} > V_{TH}$, $V_{DS} \geq V_{GS} - V_{TH}$

$$\Rightarrow V_{GS} - V_{DS} \leq V_{TH}$$

$$\Rightarrow \underline{V_{GD} \leq V_{TH}}$$

Since $V_{GD} \leq V_{TH}$, the channel will cease to exist near the drain, since potential at the point will be lesser than threshold.





Beyond the cutoff point, the charge density is very low (depletion mode). Let linear charge density there be Q_d. $Q_d \approx 0$.

$$dQ = Q_d \cdot dx$$

$$\frac{dQ}{dt} = Q_d \frac{dx}{dt}$$

$$= \quad I = Q_d v_d$$

$$= \quad v_d = \frac{I}{Q_d} \Rightarrow \lim_{Q_d \to 0} \frac{I}{Q_d}$$

$\therefore$ $v_d \longrightarrow \infty$ for finite I.

$\therefore$ The electrons are swept almost instantaneously across the cutoff point into the drain.

- $$I_{DS} = \begin{cases} \mu_n C_{ox} \frac{W}{L} \left(2(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}\right), & V_{GS} > V_{TH},\ V_{DS} < V_{OV} \\ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2, & V_{GS} > V_{TH},\ V_{DS} > V_{OV} \\ 0, & V_{GS} \ll V_{TH} \\ I_{DS0}\, e^{V_{GS} - V_T / \eta V_t} \left[1 - e^{-V_{DS}/V_t}\right], & V_{GS} < V_{TH} \end{cases}$$

(Subthreshold leakage)

- <u>PMOS:</u>

$$I_{SD_{psat}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \left[V_{SG} - |V_T|\right]^2$$

$V_{SG} \geq |V_T|$ &

$V_{SD} \geq V_{SG} - |V_T|$

$$I_{SDplin} = \mu_p C_{ox} \frac{W}{L} \left[(V_{SG} - |V_T|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

- **Second - Order Effects :-**

1) **Channel Length Modulation :-**

Since the cutoff point moves further towards the source, as V_{DS} increases, I_D actually increases with V_{DS} even during saturation.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

CLM Parameter

$$\lambda V_{DS} = \frac{\Delta L}{L}$$

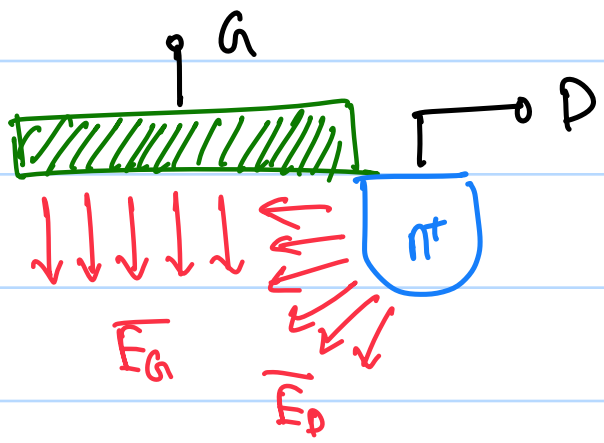
2) **Body Biasing :-**

If V_{BS} is increased, the threshold voltage of the MOSFET is decreased.

$$V_{TH} = V_{TH0} + \gamma \left[\sqrt{2\psi_s + V_{SB}} - \sqrt{2\psi_s} \right]$$

3) **Drain Induced Barrier Lowering :-**

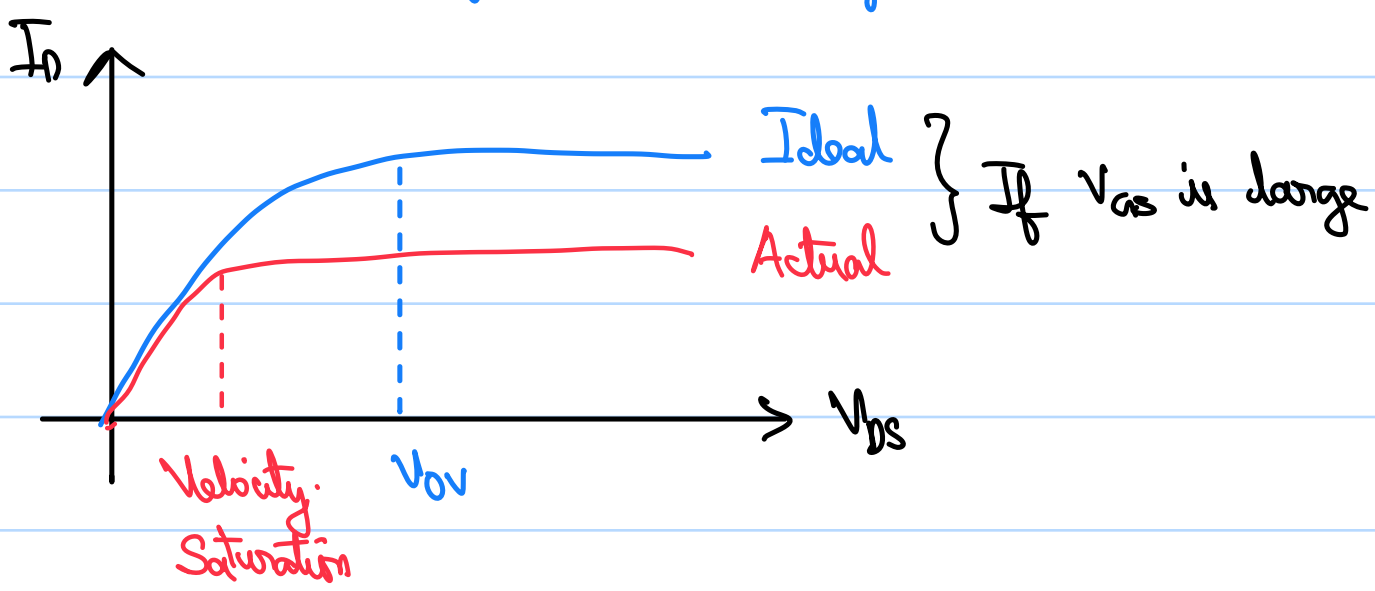
In short channel MOSFETs, the drain voltage will aid in the inversion of the channel.



Because of this aid, the threshold voltage of the MOSFET will be lower.

4) <u>Velocity Saturation</u> :-

For each channel, there is a certain v_d at which mobility degradation occurs due to scattering of the charge carriers. Prominent if V_{GS} is large.



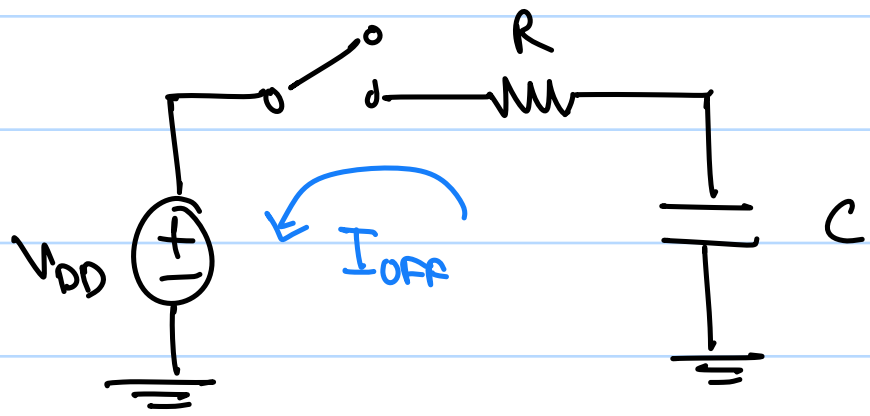
If V_{GS} is low, overdrive voltage is attained before velocity saturation, so the effect is not visible.

- <u>Switch I_{ON}, I_{OFF}</u> :-

- I_{ON} : Current through the switch when it is in the ON position.
  I_{OFF} : Current through the switch when it is in the OFF position.

- Ideally I_{OFF} should be zero, but it is non-zero due to effects like leakage.

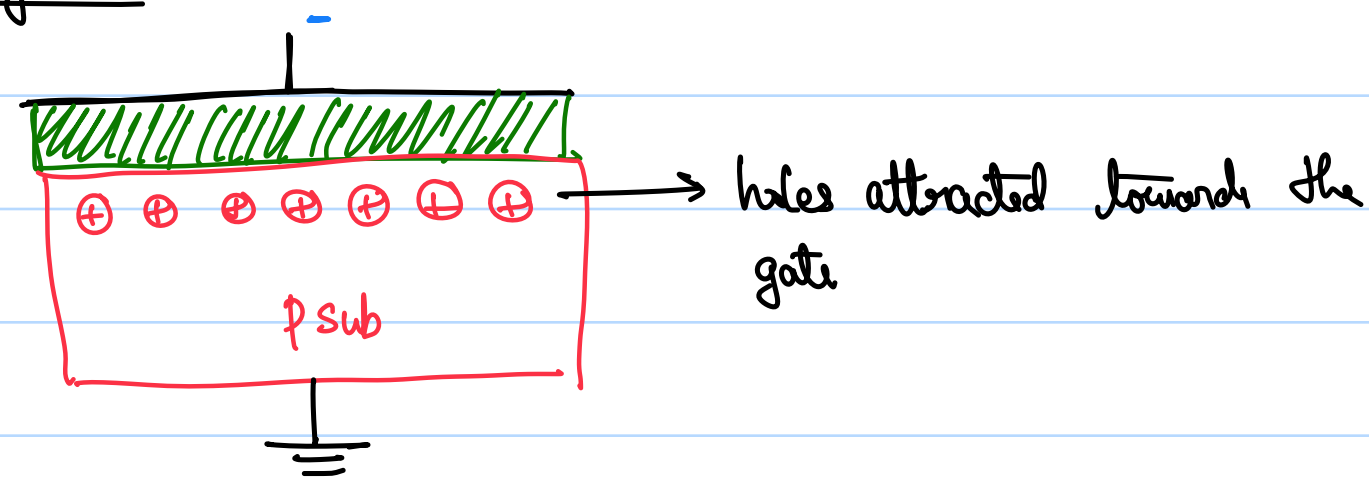
- t_{hold} : Time taken for a capacitor its discharge in an RC circuit when the switch is OFF.



For a good circuit, $t_{hold} \geq \frac{1}{2} \frac{CV_{DD}}{I_{Off}}$

- <u>MOS Capacitor</u>:

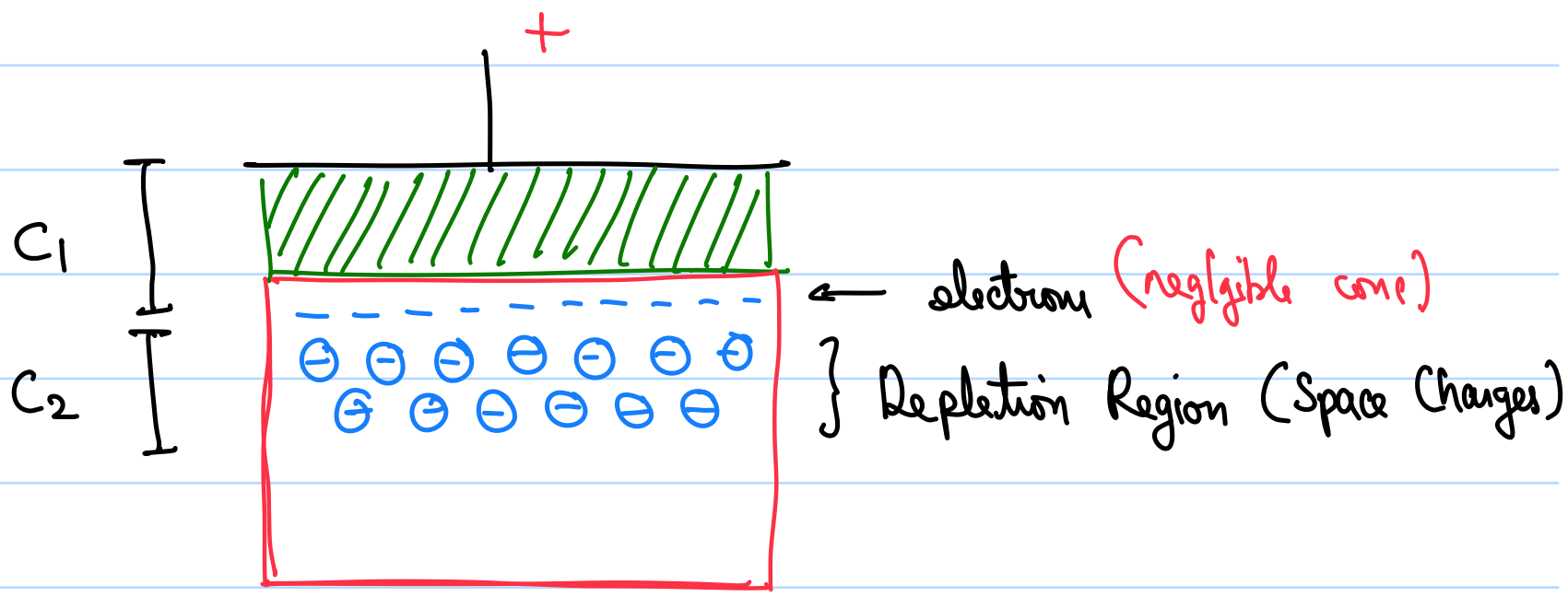
1) <u>Accumulation Region</u>:-

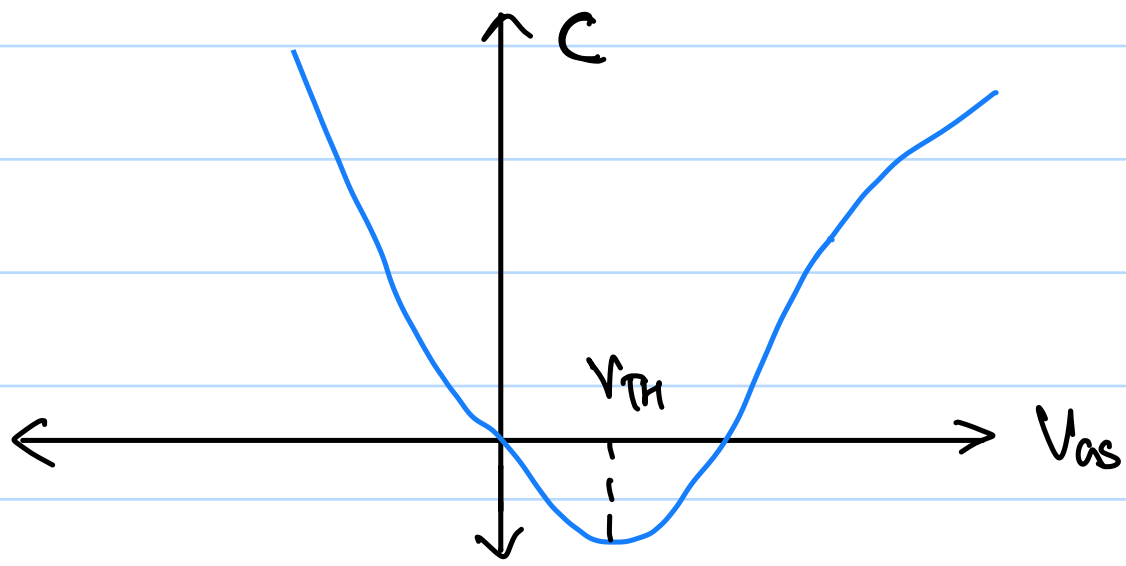


The capacitor acts like a normal parallel plate capacitor.

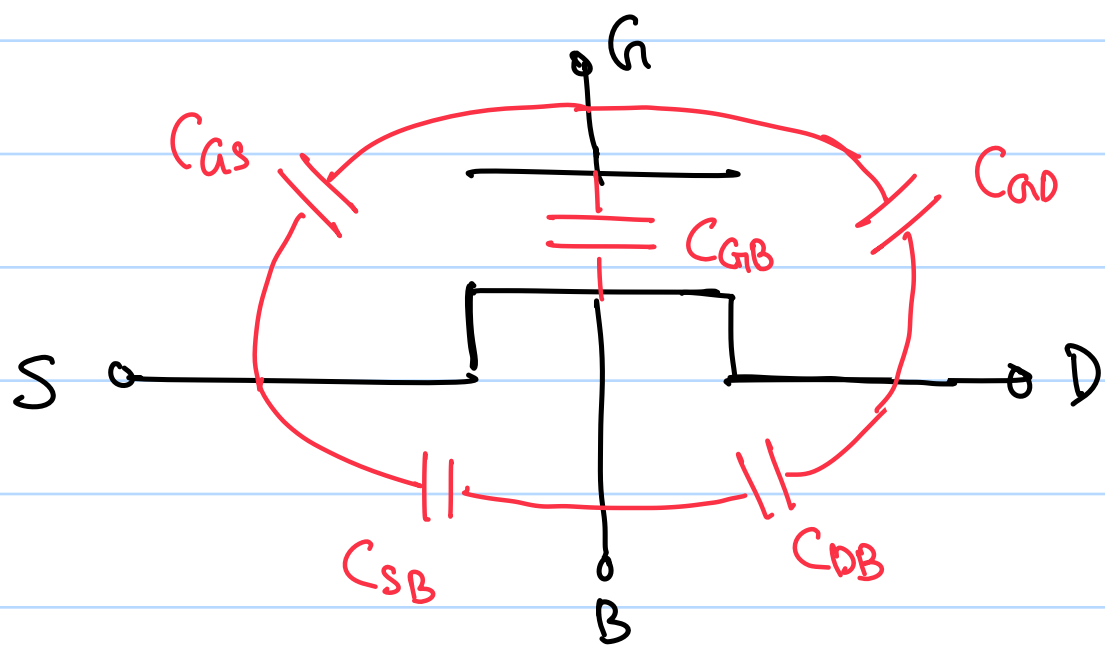
$$C = \frac{\varepsilon A}{d} = \frac{\varepsilon WL}{t_{ox}}$$

2) Depletion and Inversion :-





- Capacitance in the Modes of Operation :-



1) In Cutoff :

$C_{GS} = C_{GD} = W C_{ov}$ → Overlap Capacitance

$C_{GB} = WL C_{ox}$

2) <u>In Linear</u> :- $C_{GD} = C_{GS} = \frac{WLC_{ox}}{2}$

$$C_{GD_{ov}} = C_{GS_{ov}} = WC_{ov}$$

3) <u>In Saturation</u> :- $C_{GS} = WC_{ov} + \frac{2}{3}WLC_{ox}$

---

5) <u>Mobility Degradation</u> :-

The mobility of the channel depends on the electric field inside the channel as follows,

$$\mu \propto E^0 \quad \text{for } E < 10^3 \text{ V/cm}$$

$$\mu \propto \frac{1}{\sqrt{E}} \quad \text{for } E \approx 10^3 - 10^4 \text{ V/cm}$$

$$\mu \propto \frac{1}{E} \quad \text{for } E > 10^4 \text{ V/cm}$$

<u>Note</u>: Short Channel MOSFETs are those MOSFETs whose channel length is of the same magnitude as the dimension of the source / drain depletion regions.

6) <u>Tunneling</u> :

Tunneling is the conduction of current through the gate terminal. Significant in short channel MOSFETs.

→ Parametric Extraction :-

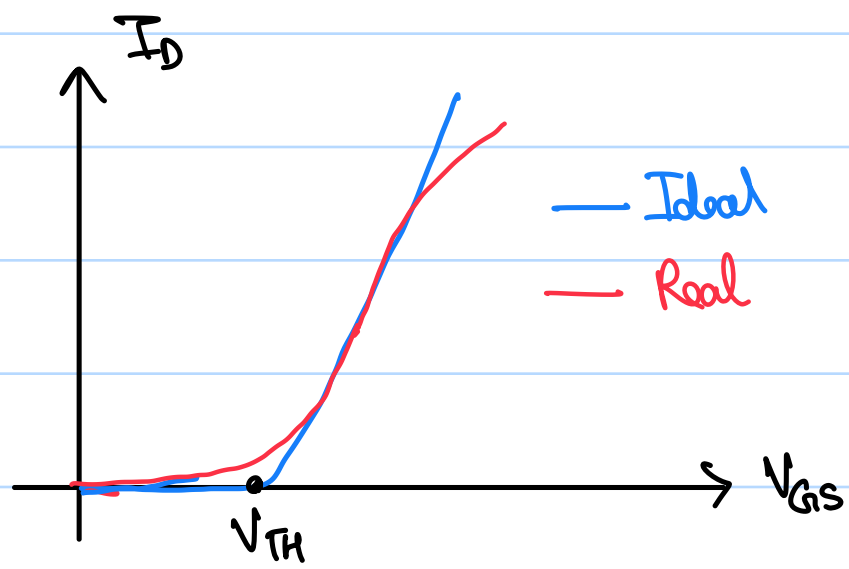
- $V_{GS} \geq V_T$ and $V_{DS} << (V_{GS} - V_T)$ [Deep Triode]

$$\Rightarrow I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

is of the form $y = m(x - x_0)$ [I_D v/ V_{GS} sweep]

x_0 is the x intercept of the line

$\therefore V_{TH}$ is the x intercept of the above line



We take the point of maximum slope to construct the line equation, to avoid mobility reducing second order effects.

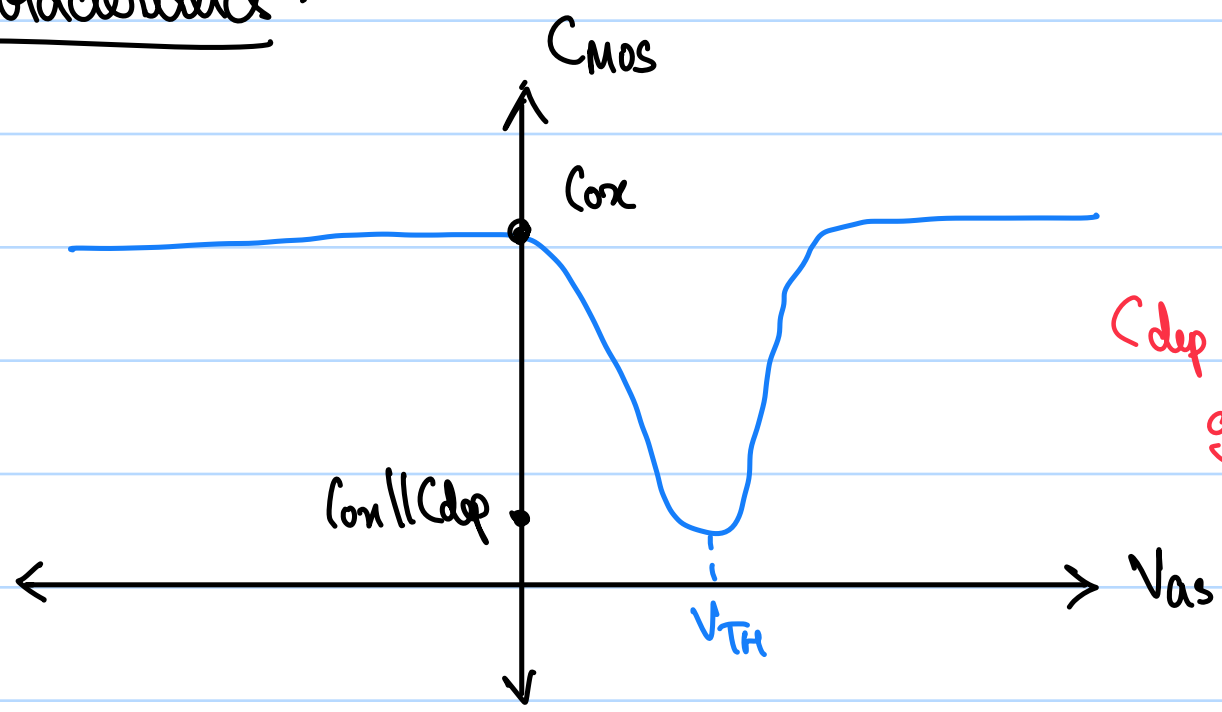
$$\mu = \frac{\mu_0}{1 + \theta (V_{GS} - V_{TH})}$$

If $V_{GS} \approx V_{TH}$

$$\mu = \frac{\mu_0}{1 + \theta (V_{GS} - V_{TH})} \approx \underline{\underline{\mu_0}}$$ [Maximum value]

The effect of all the second order effects is modelled using θ. So when $V_{GS} \approx V_{TH}$, ie at max mobility, θ's effect is low.

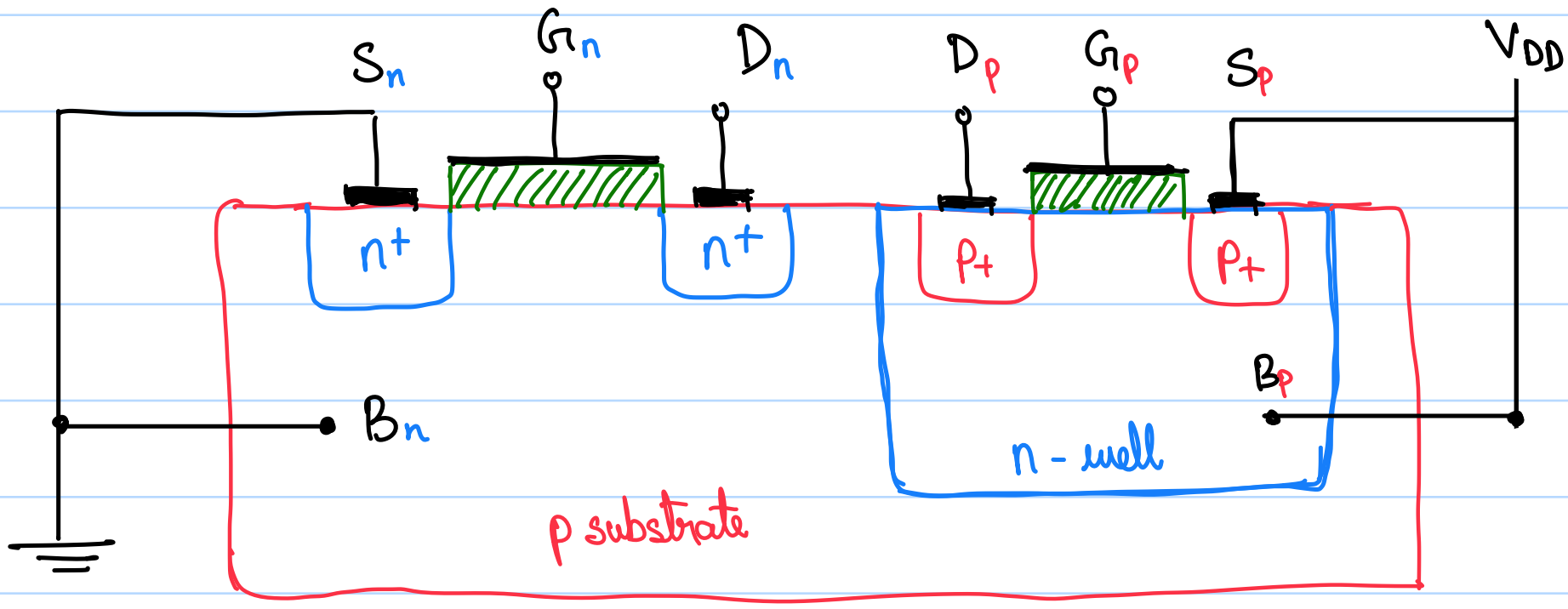
- C-V Characteristics :-



C_{dep} - Capacitance of gate-substrate depletion region.

→ CMOS Static Logic Devices :-

- CMOS - Complementary MOS (Combination of PMOS and NMOS)



CMOS Structure

(well settled)

- Static - Well defined o/p states : Either 0 (gnd) or 1 (V_{DD})

- CMOS Devices will have a Pull-Up and Pull-down networks in each logic stage.

  Pulls o/p and i/p to 0, 1 levels

- **Purpose of Logic Stage**: To evaluate i/p and pull the o/p up or down to match V_{DD} or GND.

- No static power consumption, ie, while i/ps are unchanged the power consumption is zero. Circuit still draws power when the i/ps are changed, ie, switching power is non-zero. (dynamic power)

- **CMOS Inverter** :- (Rabaey's CMOS Design textbook & Weste)

1) Transfer Characteristics (VTC) (output vs input)

2) Noise Margin

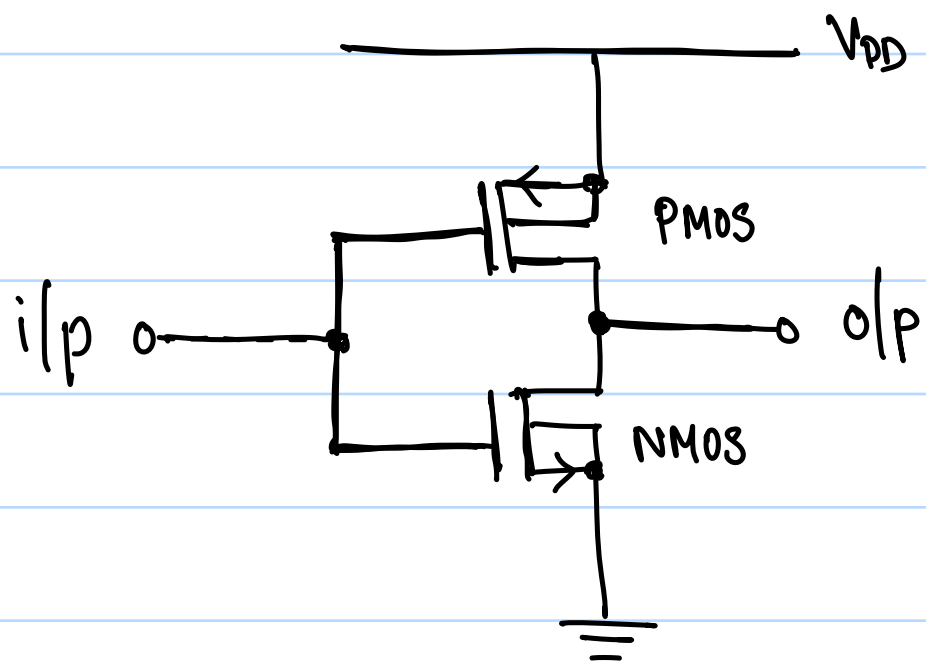
3) Dynamic Characteristics (Rise/fall, time delay)

4) Inverter Design Flow

6) Efficacy

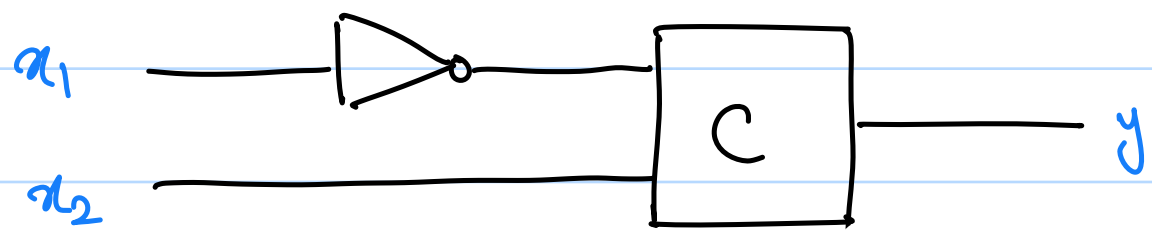
5) Inverter in Other Logics

- **Circuit**:



- The design procedure of the inverter needs to consider things like time delay, load impedance, output load type, etc.

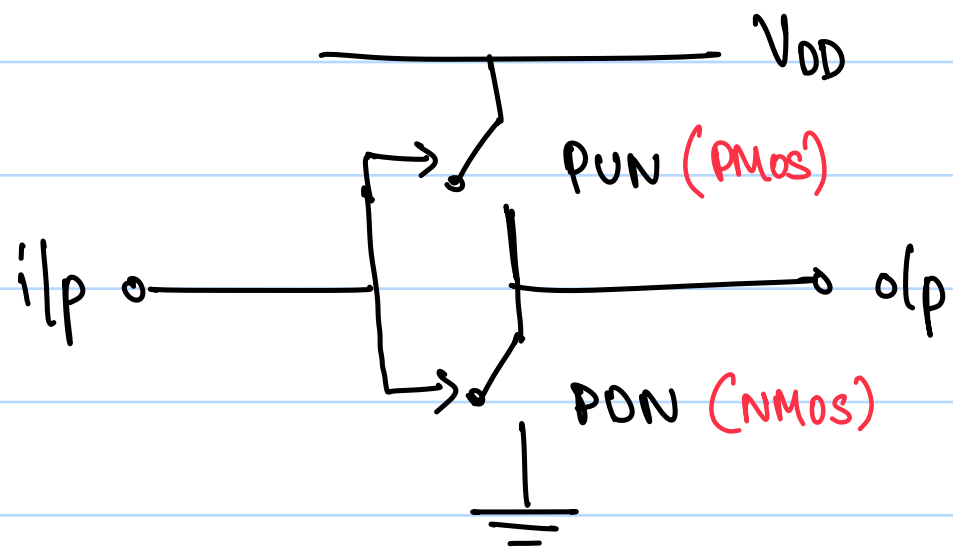
Example :



Since the inverter adds some delay, x_1 and x_2 will not reach C at the same time.

- Pull Up and Pull Down Network :-

- Pull Up : Pulls i/p to VDD
  Pull Down : Pulls i/p to GND



PUN and PDN are never on simultaneously.

- VTC of CMOS Inverter :-

- The VTC of a CMOS Inverter can be analysed by plotting the different modes of the PMOS and NMOS.

- On condition for M_n : $V_{GSn} = V_{ip} \geq V_{Tn}$

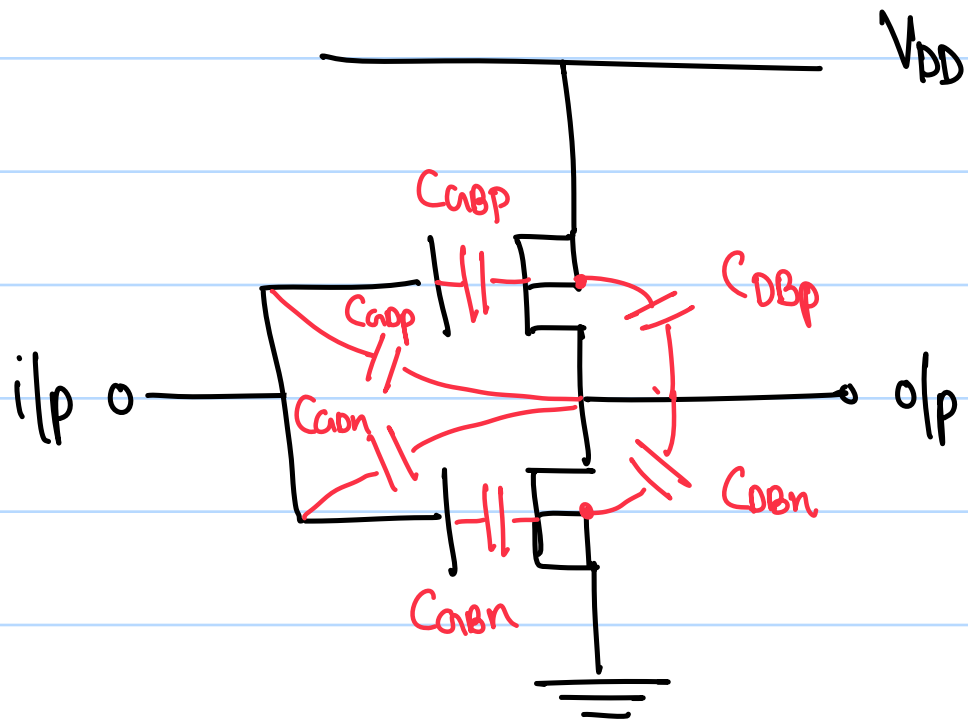
" " " M_p : $V_{SGp} = V_{DD} - V_{ip} \geq |V_{Tp}|$

$= V_{ip} \leq V_{DD} - |V_{Tp}|$

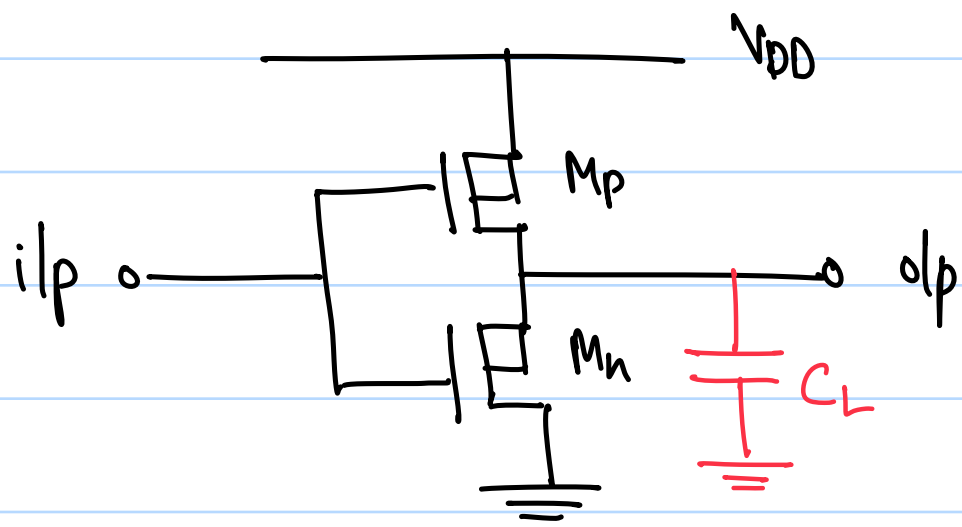
Condition	Mn	Mp	o/p
$V_{ip} = 0$	OFF	ON	V_{DD}
$V_{ip} = V_{DD}$	ON	OFF	0
	$V_{ip} \geq V_{Tn}$	$V_{ip} \leq V_{Tp} + V_{DD}$	
		$\boxed{V_{Tp} \leq 0}$	

} Inverter Behaviour

- Modelling the capacitances in the inverter



Since at the settled state, the voltages are all constant, they can be considered as AC grounds. Therefore the total capacitive impedance can be modelled as a capacitive load.



Modes of Operation of MOS

Operation Mode	Type	Condition	Equation
Cut-Off	NMOS	$V_{GS} < V_{TH}$	$I_D = 0$
	PMOS	$\lvert V_{GS}\rvert < \lvert V_{TH}\rvert$	$I_D = 0$
Linear	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \leq V_{GS} - V_{TH}$	$I_D = K_n(2(V_{GS} - V_{TH})\, V_{DS} - V_{DS}^2)$
	PMOS	$\lvert V_{GS}\rvert \geq \lvert V_{TH}\rvert$ $\lvert V_{DS}\rvert \leq \lvert V_{GS}\rvert - \lvert V_{TH}\rvert$	$I_D = K_p(2(V_{GS} - V_{TH})\, V_{DS} - V_{DS}^2)$
Saturation	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = K_n(V_{GS} - V_{TH})^2(1+\lambda V_{DS})$
	PMOS	$\lvert V_{GS}\rvert \geq \lvert V_{TH}\rvert$ $\lvert V_{DS}\rvert \geq \lvert V_{GS}\rvert - \lvert V_{TH}\rvert$	$\cancel{I_D = K_p(V_{GS} - V_{TH})^2(1-\lambda V_{DS})}$

$$I_D = K_p(V_{SG} - |V_{TH}|)^2(1+\lambda V_{DS})$$

Case 1: $0 \leq V_{i/p} < V_{Tn}$

M_n : $V_{GSn} = V_{i/p}$

$V_{i/p} \leq V_{Tn} \longrightarrow$ <u>M_n is in cutoff</u>

M_p : $|V_{GSp}| = |V_{i/p} - V_{DD}| = V_{DD} - V_{i/p}$ $\quad (V_{i/p} < V_{DD})$

$V_{DD} - V_{i/p} \geq |V_{Tp}|$ $\quad$ [Assuming $V_{Tn} \approx |V_{Tp}|$] — ①

$\Rightarrow |V_{GSp}| \geq |V_{Tp}|$

$|V_{DSp}| \approx |V_{DD} - V_{DD}| = 0$

$|V_{GSp}| - |V_{Tp}| = V_{DD} - V_{i/p} - |V_{Tp}| > 0$ $\quad$ [Assuming $V_{DD} > 2|V_{Tp}|$] ②

$\Rightarrow |V_{DSp}| \leq |V_{GSp}| - |V_{Tp}| \longrightarrow$ <u>M_p is in linear mode</u>

Case 2: $V_{Tn} \leq V_{i/p} < V_{DD}/2 \longrightarrow V_{o/p} < V_{DD}$ $\quad$ [Take $V_{o/p} \approx V_{DD}$]

M_p : $|V_{GSp}| = |V_{i/p} - V_{DD}| = V_{DD} - V_{i/p}$

$V_{DD} - V_{i/p} \geq |V_{Tp}|$ $\quad$ [By Assn. ②]

$V_{DS} = V_{o/p} - V_{DD} < 0$ $\quad$ [$V_{o/p} < V_{DD}$]

$\Rightarrow |V_{DS}| \approx 0 \Rightarrow |V_{DS}| < |V_{GSp}| - |V_{Tp}| \longrightarrow$ <u>M_p is linear</u>

M_n : $V_{GSn} = V_{i/p}$

$V_{i/p} \geq V_{Tn}$

$V_{DSn} \approx V_{DD} \Rightarrow V_{DSn} \geq V_{GSn} - V_{Tn} \longrightarrow$ Mn is in Saturation

<u>Case 3:</u> $V_{in} = V_{DD}/2 \longrightarrow V_{o/p} \approx V_{DD}/2$

M_n : $V_{GSn} = V_{DD}/2 \geq V_{Tn}$ [Assn ②]

$V_{DSn} = V_{DD}/2$

$V_{DD}/2 \geq V_{DD}/2 - V_{Tn} \longrightarrow$ Mn is in Saturation

M_p : $|V_{GSp}| = |V_{DD}/2 - V_{DD}| = V_{DD}/2 > V_{Tp}$

$|V_{DSp}| = |V_{DD}/2 - V_{DD}| = V_{DD}/2$

$V_{DD}/2 > V_{DD}/2 - |V_{Tp}| \Rightarrow |V_{DSp}| \geq |V_{GSp}| - |V_{Tp}| \longrightarrow$ Mp is in Saturation

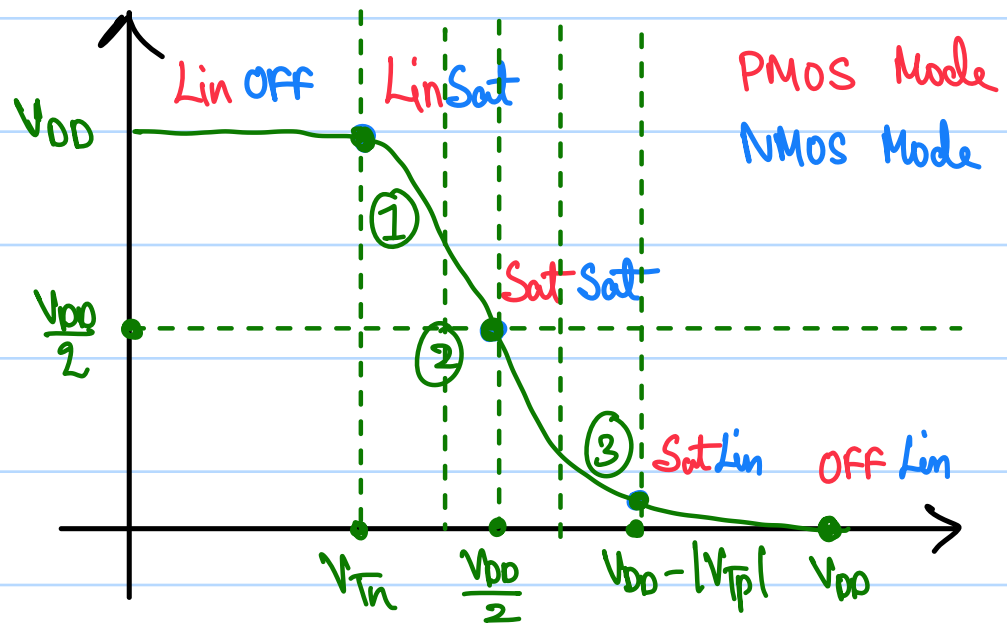
|||l proof can be stated for $V_{DD}/2 < V_{i/p} < V_{DD} - |V_{Tp}|$ and $V_{DD} - |V_{Tp}| < V_{i/p}$.

Once the voltages are settled

∴ The VTC of the CMOS Inverter can be summarized as,

Condition	Mp	Mn	o/p
$0 \leq V_{in} \leq V_{Tn}$	Lin	OFF	V_{DD}
$V_{Tn} \leq V_{in} < V_{DD}/2$	Lin	Sat	$< V_{DD}$
$V_{in} = V_{DD}/2$	Sat	Sat	$V_{DD}/2$
$V_{DD}/2 < V_{in} < V_{DD} - \lvert V_{Tp}\rvert$	Sat	Lin	$< V_{DD}/2$
$V_{DD} - \lvert V_{Tp}\rvert < V_{in}$	OFF	Lin	0

This switching point is valid if $V_{Tn} = |V_{Tp}|$



<u>Note</u>: By KCL, currents through both the MOSFETs will always be equal in the 3 intermediate points (Lin Sat Sat Sat Sat Lin)

At ① (Lin Sat)

$$I_{Dp\,lin} = I_{Dn\,sat}$$

$$= K_p\left[(V_{SGp} - |V_{Tp}|)V_{SD} - \frac{V_{SD}^2}{2}\right] = \frac{1}{2}K_n(V_{GSn} - V_{Tn})^2$$

$$= K_p\left[(V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{o/p}) - \frac{(V_{DD}-V_{o/p})^2}{2}\right] = \frac{K_n}{2}(V_{i/p} - V_{Tn})^2$$

On Solving, we will get, (Take $V_{DD} - V_{o/p} = y$, $V_{i/p} - V_{Tn} = x$ easy and $K_n = K_p$)

$$V_{o/p} = (V_{i/p} + |V_{Tp}|) \pm \sqrt{(V_{DD} - V_{Tn} - |V_{Tp}|)(V_{DD} - 2V_{i/p} + V_{Tn} - |V_{Tp}|}$$

Since $V_{o/p} \approx V_{DD}$ near ①,

$$V_{o/p} = (V_{i/p} + |V_{Tp}|) + \sqrt{(V_{DD} - V_{Tn} - |V_{Tp}|)(V_{DD} - 2V_{i/p} + V_{Tn} - |V_{Tp}|)}$$

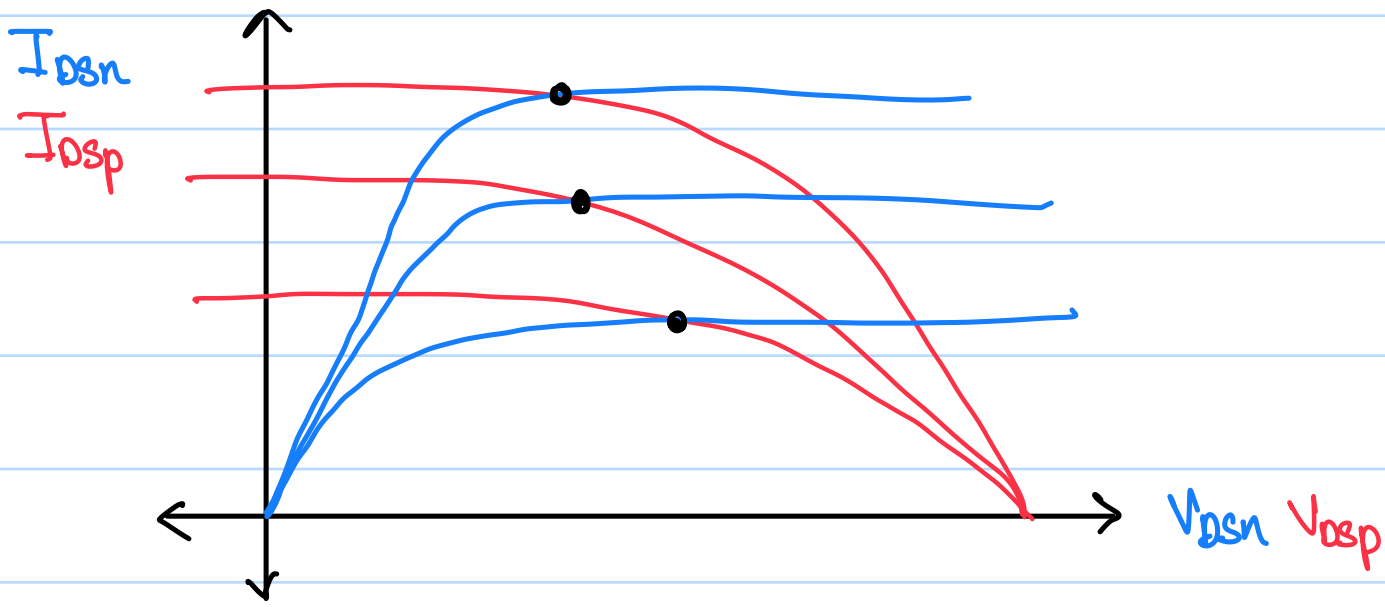
Conditions : $V_{DD} \geq V_{Tn} + |V_{Tp}|$, $V_{i/p} \leq \frac{V_{DD} + V_{Tn} - |V_{Tp}|}{2}$

Therefore, the operating requirements of a CMOS inverter are:

1) $V_{DD} \geq V_{Tn} + |V_{Tp}|$ 2) $V_{i/p} \leq \dfrac{V_{DD} + V_{Tn} - |V_{Tp}|}{2} \approx \dfrac{V_{DD}}{2}$

min. power supply max. i/p voltage

|||ly we can calculate for all the other points, by equating PMOS current and NMOS current.



$V_{DD} \approx 1.8V$ for 180nm technology node.

At ② (Sat Sat),

$$I_{DSn\,sat} = I_{DSp\,sat}$$

$$= K_n (V_{GSn} - V_{THn})^2 = K_p (V_{SGp} - |V_{THp}|^2)^2$$

$$= K_n (V_{i/p} - V_{THn})^2 = K_p (V_{DD} - V_{i/p} - |V_{THp}|^2)^2$$

$$\Rightarrow V_{i/p} = \frac{(V_{DD} + \sqrt{B}\, V_{THn} + |V_{THp}|)}{1 + \sqrt{B}} \qquad \underline{\beta = \frac{K_n}{K_p}}$$

$$V_{DSn} \geq V_{GSn} - V_{THn}$$

$$\Rightarrow V_{o/p} \geq V_{i/p} - V_{THn}$$

$$V_{SDp} \geq V_{SGn} - |V_{THp}|$$

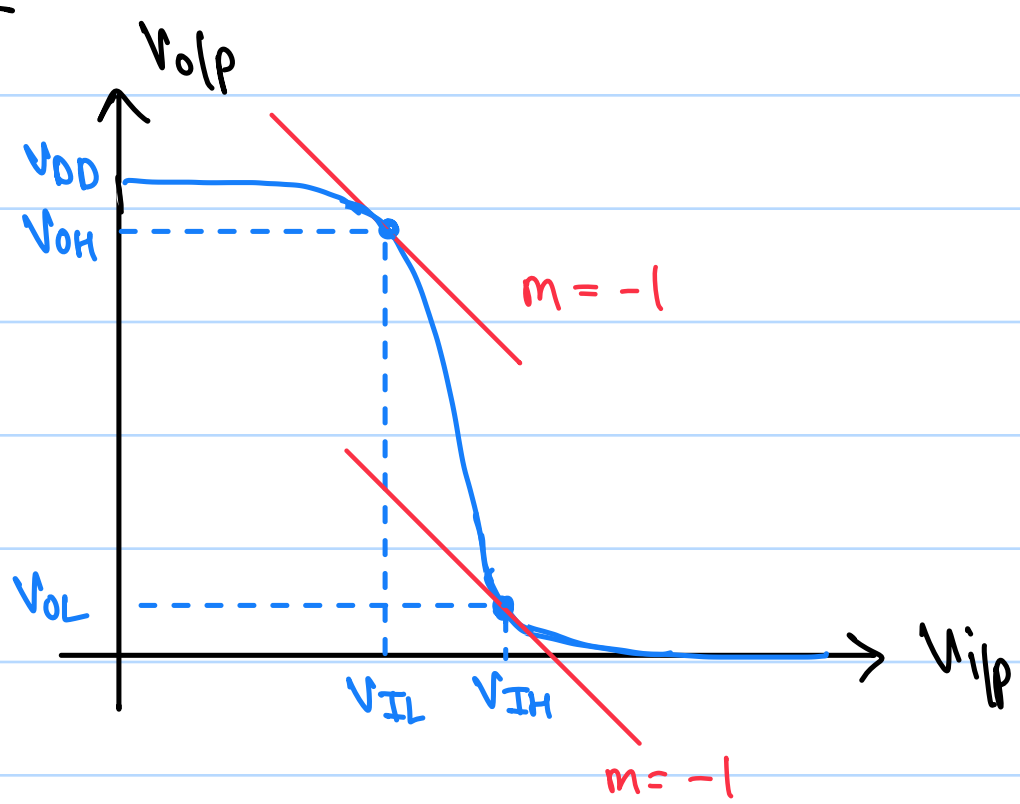
$$V_{DD} - V_{o/p} \geq V_{DD} - V_{i/p} - |V_{THp}|$$

$$\Rightarrow V_{o/p} \leq V_{i/p} + |V_{THp}|$$

$$\therefore V_{o/p} \in \left[V_{i/p} - V_{THn} \, , \, V_{i/p} + |V_{THp}| \right]$$

In this region, $V_{o/p}$ vs $V_{i/p}$ is approximately a straight line of very high slope. Therefore it shows amplifying action.

- <u>Noise Margin</u> :-



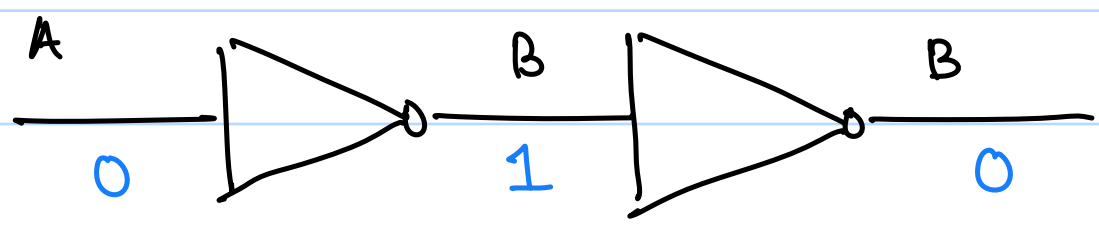
- To avoid the amplification behavior, we set

$$V_{out} \in [V_{OH}, V_{DD}] \longrightarrow \text{Logic } 1$$
$$V_{out} \in [0, V_{OL}] \longrightarrow \text{Logic } 0$$

$\Rightarrow$ V_{OH} = Minimum o/p for o/p logic 1
V_{OL} = Maximum o/p for o/p logic 0
V_{IH} = Minimum i/p for o/p logic 0
V_{IL} = Maximum o/p for o/p logic 1

- If $V_{i/p} \in (V_{IL}, V_{IH})$, the Inverter acts like an amplifier, which is unwanted since it amplifies noise as well, creating undefined behavior.

- If we have 2 inverters in series as,



$V_A \in [0, V_{IL}]$ $\quad V_B \in [V_{OH}, V_{DD}]$ $\quad V_C \in [0, V_{OL}]$

$[V_{OH}, V_{DD}] \subseteq [V_{IH}, V_{DD}]$

- From the VTC, we can say that $V_{OH} > V_{IH}$ and $V_{OL} < V_{IL}$. So, we define the noise margin of our inverter as,

$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

- But since $V_{IH} < V_{OH}$, even if $V_B < V_{OH}$, as long as $V_B > V_{IH}$ the inverter C will output 0. Hence the noise margin NM_H. Illy for V_B low, we have NM_L.

- Also if the 2 inverters are not the same, then it must be ensured that,

$$V_{OH1} > V_{IH2}$$

- The parameter extraction of $V_{OH}, V_{OL}, V_{IH}, V_{IL}$, can be done as follows,

For point (V_{IL}, V_{OH}), Inv. is in region of Lin Sat
For point (V_{IH}, V_{OL}), Inv. is in region of Sat Lin

We know the current equation at both these regions (or atleast how to derive them). The required points will have $dV_{olp}/dV_{ilp} = -1$

We will get,

$$V_{IL} = \frac{3V_{DD} + 5V_{Tn} - 8|V_{Tp}|}{8}$$

$$V_{OH} = \frac{7V_{DD} + V_{Tn} + |V_{Tp}|}{8}$$

$$V_{IH} = \frac{5V_{DD} + 3V_{Tn} - 5|V_{Tp}|}{8}$$

$$V_{OL} = \frac{V_{DD} - V_{Tn} + |V_{Tp}|}{8}$$

Assume $K_n = K_p$ (or) $\beta = 1$

$$\Rightarrow \quad NM_H = \frac{V_{DD} - V_{Tn} + 3|V_{Tp}|}{4}$$

$$NM_L = \frac{V_{DD} + 3V_{Tn} - |V_{Tp}|}{4}$$

$\frac{V_{DD} + 2V_T}{4}$ if $V_{Tn} = |V_{Tp}| = V_T$

- From the $NM_{H/L}$ equations we can see that increasing V_{DD} and V_{TH} will give us better noise margin.

Trade-offs : $V_{DD} \uparrow$ increases power consumption

$V_T \uparrow$ increases min. V_{DD}, lower current causing delays and lower speed.

Higher current charges the capacitances faster, reducing delay / increasing bandwidth