AEC Assignment 3

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1 Region Of Operation

1.1

MOSFETs have 3 regions of operation: Cutoff, Saturation and Triode.

1. **Cutoff:** Occurs when $|V_{GS}| < |V_{TH}|$, in NMOS and PMOS, Here the channel between the Source and the Drain has not been fully formed yet. So no current flows through the MOSFET, i.e,

$$I_{DS} = 0$$

2. **Triode/Linear:** Occurs in NMOS when,

$$V_{GS} \geqslant V_{TH} \text{ and } \ V_{DS} < V_{GS} - V_{TH}$$

and in PMOS when,

$$|V_{GS}| \geqslant |V_{TH}| \text{ and } \ |V_{DS}| < |V_{GS}| - |V_{TH}|$$

Here the channel between Source and Drain is fully formed and the MOSFET acts like a voltage dependent variable resistor.
The equation for I_{DS} is given by,

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right), \quad \text{for NMOS}$$
$$I_{DS} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(2(V_{SG} - V_{TH})V_{SD} - V_{SD}^2\right), \quad \text{for PMOS}$$

Where,

$$\mu_n - \text{Electron Mobility}$$
$$\mu_p - \text{Hole Mobility}$$
$$C_{ox} - \text{Gate Oxide Capacitance Per Unit Area}$$
$$W - \text{Channel Width}$$
$$L - \text{Channel Length}$$

3. **Saturation:** Occurs in NMOS when

$$V_{GS} \geqslant V_{TH} \text{ and } V_{DS} \geqslant V_{GS} - V_{TH}$$

and in PMOS when,

$$|V_{GS}| \geqslant |V_{TH}| \text{ and } |V_{DS}| \geqslant |V_{GS}| - |V_{TH}|$$

Here the channel has been pinched off at a point before the Drain terminal of the MOSFET. Current flowing in this region is mostly due to carrier injection at the pinch off point. Therefore, I_{DS} will not depend on V_{DS} as strongly as in Linear region. The equation for I_{DS} is given by,

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{for NMOS}$$
$$I_{DS} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - V_{TH})^2(1 - \lambda V_{SD}) \quad \text{for PMOS}$$

Where,

μ_n – Electron Mobility
μ_p – Hole Mobility
C_{ox} – Gate Oxide Capacitance Per Unit Area
W – Channel Width
L – Channel Length
λ – Channel Length Modulation Parameter

1.2

Common Parameters:

It given that $\mu_n C_{ox} = 300\mu A/V^2$ and $\frac{W}{L} = \frac{2\mu}{1\mu} = 2$. Therefore,

$$\mu_n C_{ox}\frac{W}{L} = 300 \times 10^{-6} \times 2 = 6 \times 10^{-4} A/V^2 \tag{1.2.1}$$

Also, we can use the results and equations mentioned in 1.1 to solve the following questions.

(a) Given: $V_G = 2V, V_S = 0.5V, V_D = 0.7V, V_{TH} = 1V$

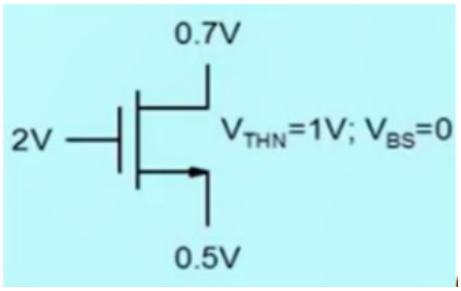

Figure 1.2.1: Circuit of 1.2(a)

$$
\begin{aligned}
V_{GS} &= V_G - V_S \\
&= 2 - 0.5 \\
&= 1.5V \\
\implies V_{GS} > V_{TH} &\implies \text{The MOSFET is not in Cutoff} \\
V_{DS} &= V_D - V_S \\
&= 0.7V - 0.5V \\
&= 0.2V \\
V_{GS} - V_{TH} &= 1.5V - 1V = 0.5V \\
\implies V_{DS} < V_{GS} - V_{TH} &\implies \text{The MOSFET is in } \textbf{Triode Region} \\
\implies I_{DS} &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right), \quad \text{from 1.1} \\
I_{DS} &= \frac{1}{2} \times 6 \times 10^{-4} \times \left(2(0.5)0.2 - 0.2^2\right) \\
I_{DS} &= 3 \times 10^{-4} \times 0.16 \\
\therefore I_{DS} &= 48\mu A
\end{aligned}
$$

(b) Given: $V_G = 2V, V_S = 0.5V, V_D = 1.5V, V_{TH} = 1V$

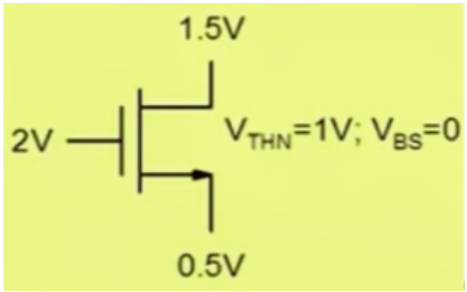

Figure 1.2.2: Circuit of 1.2(b)

$$
\begin{aligned}
V_{GS} &= V_G - V_S \\
&= 2 - 0.5 \\
&= 1.5V \\
\implies V_{GS} &> V_{TH} \implies \text{The MOSFET is not in Cutoff} \\
V_{DS} &= V_D - V_S \\
&= 1.5 - 0.5 \\
&= 1V \\
V_{GS} - V_{TH} &= 1.5V - 1V = 0.5V \\
\implies V_{DS} &> V_{GS} - V_{TH} \implies \text{The MOSFET is in } \textbf{Saturation Region} \\
\implies I_{DS} &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{from 1.1} \\
I_{DS} &= \frac{1}{2} \times 6 \times 10^{-4} \times 0.5^2, \text{ (neglecting Channel Length Modulation)} \\
I_{DS} &= 3 \times 10^{-4} \times 0.25 \\
\therefore I_{DS} &= 75\mu A
\end{aligned}
$$

(c) Given: $V_G = 2V, V_S = 0.5V$ (Since, source always has the least potential), $V_D = 1.5V, V_{TH} = 1V$

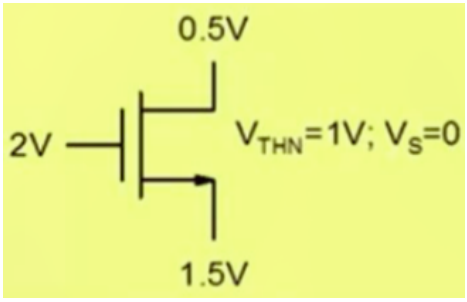

Figure 1.2.3: Circuit of 1.2(c)

Since the parameters are identical to the previous question (1.2(b)), the same results will apply, i.e,

The MOSFET is operating in Saturation region.

$I_{DS} = 75\mu A$

(d) Given: $V_G = 2V, V_S = 0V, V_D = 2V, V_{TH} = 1V$

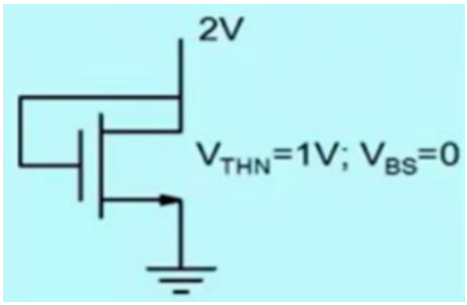

Figure 1.2.4: Circuit of 1.2(d)

$$\begin{aligned}
V_{GS} &= V_G - V_S \\
&= 2 - 0 = 2V \\
\implies V_{GS} > V_{TH} &\implies \text{MOSFET is not in Cutoff} \\
V_{DS} &= V_D - V_S \\
&= 2 - 0 \\
&= 2V \\
V_{GS} - V_{TH} &= 2 - 1 \\
&= 1V \\
\implies V_{DS} > V_{GS} - V_{TH} &\implies \text{MOSFET is in } \textbf{Saturation} \\
\implies I_{DS} &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{from 1.1} \\
I_{DS} &= \frac{1}{2} \times 6 \times 10^{-4} \times 1^2, \text{ (Neglecting Channel Length Modulation)} \\
\therefore I_{DS} &= 300\mu A
\end{aligned}$$

(e) Given: $V_G = 1V, V_S = 0.5V, V_D = 1.5V, V_{TH} = 1V$

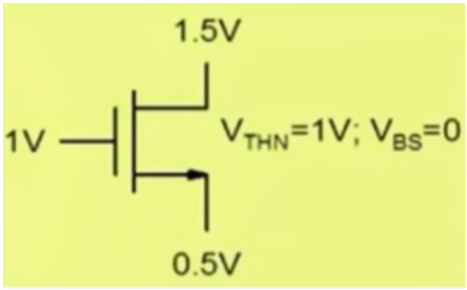

Figure 1.2.5: Circuit of 1.2(e)

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 1 - 0.5 \\ &= 0.5V \\ \implies V_{GS} < V_{TH} &\implies \text{MOSFET is in } \textbf{Cutoff} \\ \implies I_{DS} &= 0A \end{aligned}$$

1.3

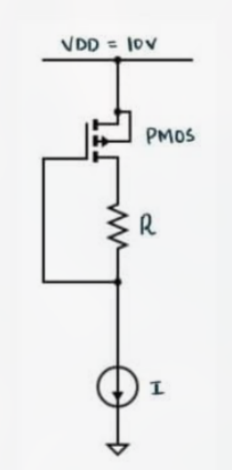

Figure 1.3.1: Circuit of 1.3

(a) To Show:
For the PMOS in the above configuration to be in Saturation, $IR \leqslant |V_{thp}|$
Since Gate Current is Negligible, we can assume,

$$I_{DS} = I \tag{1.3.1}$$

The Source of the PMOS will be at the top, since Source

$$V_{GS} = V_G - V_S$$

By KVL,

$$\begin{aligned} V_G &= 10 - V_{SD} - IR \\ V_S &= 10 \\ \implies V_{GS} &= (10 - V_{SD} - IR) - (10) \\ \implies V_{GS} &= V_{DS} - IR \\ IR &= V_{DS} - V_{GS} \end{aligned} \tag{1.3.2}$$

We know that for a PMOS to be in Saturation,

$$\begin{aligned} |V_{DS}| &\geqslant |V_{GS}| - |V_{thp}| \\ \implies |V_{GS}| - |V_{DS}| &\leqslant |V_{thp}| \\ \implies -V_{GS} - (-V_{DS}) &\leqslant |V_{thp}| \\ V_{DS} - V_{GS} &\leqslant |V_{thp}| \end{aligned}$$

Applying the result from 1.3.2, we get,

$$\implies IR \leqslant |V_{thp}|$$

Hence Proved

(b) Given: $|V_{thp}| = 1V, K_p = 0.2mA/V^2, I_d = 0.1mA$
To Find: V_{SD}, V_{SG}

(i) $R = 0\Omega$

$$\begin{aligned} IR = 0 &\implies IR < |V_{thp}| \\ \implies &\text{ MOSFET is in Saturation} \end{aligned}$$

We know that, for a MOSFET is Saturation,

$$I_{DS} = -\frac{K_p}{2}\left(V_{SG} - |V_{TH}|\right)^2 \tag{1.3.3}$$

$$\implies V_{SG} = |V_{thp}| + \sqrt{\frac{2 \cdot I_{SD}}{K_p}} \tag{1.3.4}$$

$$\begin{aligned} V_{SG} &= 1 + \sqrt{\frac{2 \times 0.1 \times 10^{-3}}{0.2 \times 10^{-3}}} \\ &= 1 + \sqrt{\frac{0.2}{0.2}} \\ &= 1 + 1 \\ \implies V_{SG} &= 2V \end{aligned}$$

Also from Equations 1.3.2, we know that,

$$\begin{aligned} V_{GS} &= V_{DS} - IR \\ \implies V_{SG} &= V_{SD} \quad (\text{IR} = 0) \\ \implies V_{SD} &= 2V \end{aligned}$$

Therefore, we have $V_{SG} = 2V$ and $V_{SD} = 2V$.

(ii) $R = 10k\Omega$

$$\begin{aligned} IR &= 0.1 \times 10^{-3} \times 10 \times 10^3 \\ &= 1V \\ \implies IR &= |V_{thp}| \implies \text{MOSFET is in Saturation, (by Q1.3(a))} \end{aligned}$$

From Equation 1.3.4,

$$\begin{aligned} V_{SG} &= |V_{thp}| + \sqrt{\frac{2 \cdot I_{SD}}{K_p}} \\ &= 1 + \sqrt{\frac{0.2}{0.2}} \\ &= 1 + 1 \\ \implies V_{SG} &= 2V \end{aligned}$$

From Equations 1.3.2,

$$\begin{aligned} V_{GS} &= V_{DS} - IR \\ -2 &= V_{DS} - 1 \\ V_{DS} &= -2 + 1 \\ \implies V_{SD} &= 1V \end{aligned}$$

Therefore, we have $V_{SG} = 2V$ and $V_{SD} = 1V$.

(iii) $R = 100k\Omega$

$$\begin{aligned} IR &= 0.1 \times 10^{-3} \times 100 \times 10^3 \\ &= 10V \\ \implies IR &> |V_{thp}| \implies \text{MOSFET is NOT in Saturation, (by Q1.3(a))} \end{aligned}$$

Since current through the MOSFET is not zero, the MOSFET cannot be in Cutoff. Therefore it must be in Linear Region. We know that for Linear Region,

$$\begin{aligned} I_{SD} &= \frac{1}{2} K_p \left(2(V_{SG} - |V_{thp}|)V_{SD} - V_{SD}^2\right) \\ \implies 0.1 \times 10^{-3} &= \frac{1}{2} \times 0.2 \times 10^{-3} \times (2(V_{SG} - 1)V_{SD} - V_{SD}^2) \\ \implies 1 &= 2(V_{SG} - 1)V_{SD} - V_{SD}^2 \end{aligned}$$

From Equations 1.3.2, we know that $V_{GS} = V_{DS} - IR$. Substituting this in the Equation, we get,

$$\begin{aligned} 1 &= 2(-(V_{DS} - 10) - 1)V_{SD} - V_{SD}^2 \\ &\implies V_{SD}^2 + 18V_{SD} - 1 = 0 \end{aligned}$$

Solving the Quadratic, we get,

$$V_{SD} = 0.05535 \ \& \ V_{SD} = -18.05535$$

Since $V_S > V_D$, as Source is the terminal with higher voltage in PMOS, $V_{SD} = 0.05535$ is the only valid solution.
Since $V_{GS} = V_{DS} - IR$, we get,

$$\begin{aligned} V_{SG} &= IR + V_{SD} \\ &= 10 + 0.05535 \\ &= 10.05535 \end{aligned}$$

Therefore, we have $V_{SG} = 10.05535V$ and $V_{SD} = 0.05535V$.

1.4

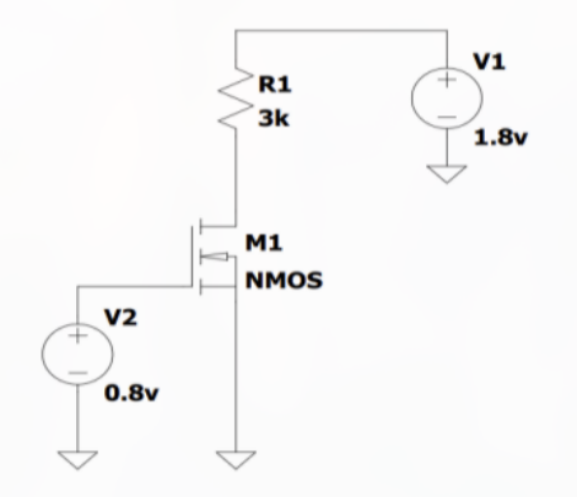

Figure 1.4.1: Circuit of 1.4

Given: $V_{thn} - 0.5V, \mu_n C_{ox} = 100\mu A/V^2, \mu_n C_{ox} = 100\mu A/V^2, \frac{W}{L} = \frac{1.8\mu}{0.18\mu}$

$$\begin{aligned} K_n &= \mu_n C_{ox} \frac{W}{L} \\ &= 100 \times 10^{-6} \times \frac{1.8\mu}{0.18\mu} \\ &= 10^{-4} \times 10 \\ \therefore K_n &= 10^{-3} A/V^2 \end{aligned}$$

(a) To determine Region Of Operation,

$$\begin{aligned} V_S &= 0V \\ V_G &= 0.8V \\ V_{GS} &= V_G - V_S = 0.8V \\ \implies V_{GS} &> V_{thn} \end{aligned}$$

$\implies$ MOSFET is not in Cutoff

$$\begin{aligned} V_{GS} - V_{TH} &= 0.8 - 0.5 \\ &= 0.3V \end{aligned}$$

Assume the MOSFET is in Saturation. So the current across the MOSFET will be given by,

$$\begin{aligned} I_{DS} &= \frac{K_n}{2} (V_{GS} - V_{TH})^2 \\ I_{DS} &= \frac{10^{-3}}{2} (0.3)^2 \\ I_{DS} &= 0.045 \times 10^{-3} \\ I_{DS} &= 45\mu A \end{aligned}$$

If we use KVL from V1 to ground,

$$\begin{aligned} 1.8V - I_{DS}R - V_{DS} &= 0 \\ V_{DS} &= 1.8 - 3000 \times 45 \times 10^{-6} \\ &= 1.8 - 0.135 \\ V_{DS} &= 1.665 > V_{GS} - V_{thp} \end{aligned}$$

Since the condition for Saturation is satisfied, we can confirm that the MOSFET is indeed in **Saturation region**.

(b) From the previous question, biasing current is found out to be $45\mu A$. The transconductance is given by,

$$\begin{aligned} g_m &= \frac{2I_{DS}}{V_{GS} - V_{thn}} \\ &= \frac{2 \times 45 \times 10^{-6}}{0.8 - 0.5} \\ &= 3 \times 10^{-4} S \end{aligned}$$

(c) For the MOSFET to be in Saturation, V_{GS} must follow 2 conditions

(i) $V_{GS} \geqslant V_{thn}$

(ii) $V_{DS} \geqslant V_{GS} - V_{thn}$

In Condition (i),

$$\begin{aligned} V_{GS} &\geqslant V_{thn} \\ \implies V_{GS} &\geqslant 0.5V \end{aligned}$$

In Condition (ii)

$$V_{DS} \geqslant V_{GS} - V_{thn}$$

Applying KVL from V1 to ground,

$$\begin{aligned} 1.8V - I_{DS}R - V_{DS} &= 0 \\ V_{DS} &= 1.8 - I_{DS}R \end{aligned}$$

We know that

$$\begin{aligned} I_{DS} &= \frac{K_n}{2} (V_{GS} - V_{TH})^2 \\ \implies V_{DS} &= 1.8 - 3000(\frac{K_n}{2})(V_{GS} - V_{thn})^2 \qquad (1.4.1) \\ \implies 1.8 - 3000(\frac{K_n}{2})(V_{GS} - V_{thn})^2 &\geqslant V_{GS} - V_{thn} \end{aligned}$$

In the above inequality, to find point of equality,

$$\begin{aligned} 1.8 - 3000(\frac{K_n}{2})(V_{GS} - V_{thn})^2 &= V_{GS} - V_{thn} \\ 1.8 - 3000(\frac{K_n}{2})(V_{GS} - V_{thn})^2 - (V_{GS} - V_{thn}) &= 0 \\ 1.8 - 3000(0.5 \times 10^{-3})(V_{GS} - V_{thn})^2 - (V_{GS} - V_{thn}) &= 0 \\ 1.8 - 1.5(V_{GS} - V_{thn})^2 - (V_{GS} - V_{thn}) &= 0 \end{aligned}$$

Considering this as a quadratic in $V_{GS} - V_{thn}$ (i.e, V_{DSAT}), upon solving, we get,

$$V_{GS} - V_{thn} = -1.478 \quad \& \quad V_{GS} - V_{thn} = 0.811$$
$$\implies V_{GS} = -0.978 \quad \& \quad V_{GS} = 1.311$$

Using these in the inequality obtained in 1.4.1, we get that for the inequality to hold,

$$V_{GS} \in [-0.978, 1.311] \tag{1.4.2}$$

Combining 1.4.2 with Condition (i), we get that for the MOSFET to be in Saturation, we need,

$$V_{GS} \in [0.5, 1.311]$$

Range $= 1.311 - 0.5 = 0.811V$, Lower Limit = 0.5V, Upper Limit, 1.311V

2 Small Signal Model And Impedances

2.1

The Small Signal Models of a NMOS and a PMOS are:

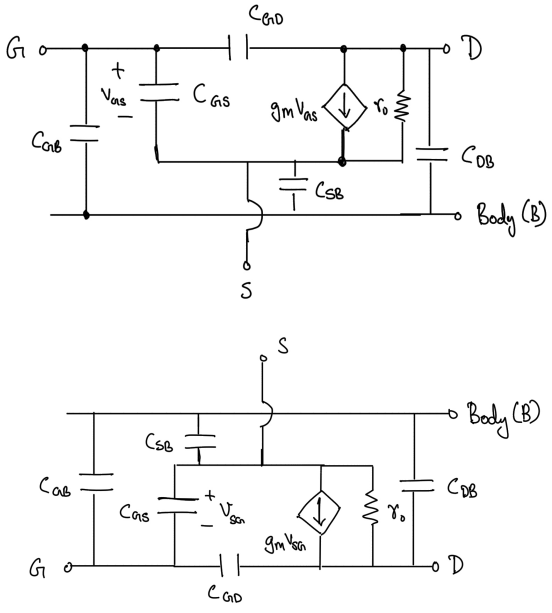

Figure 2.1.1: Small Signal Model of NMOS (top) and PMOS (bottom)

2.2

Let v_{in} be the input test voltage, and i_{in} be the current at the input terminal. Then the input impedance z_{in} is given by,

$$z_{in} = \frac{v_{in}}{i_{in}} \tag{2.2.1}$$

(i)

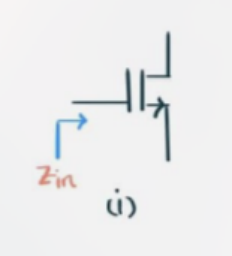

Figure 2.2.1: Circuit of 2.2(i)

Grounding the Source and Drain terminals, the equivalent small signal circuit for the same will be as Figure 2.2.2

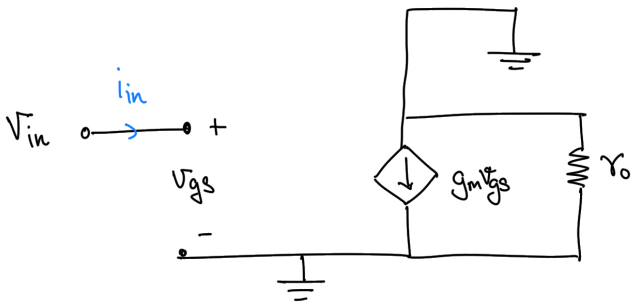

Figure 2.2.2: Equivalent Circuit of 2.2(i)

Looking at the circuit we can see that i_{in} flows into an open terminal. Therefore, by KCL, i_{in} must be zero.

$$\therefore z_{in} \to \infty$$

(ii)

Grounding the Source and Gate terminals, the equivalent small signal circuit for the same will be as Figure 2.2.4

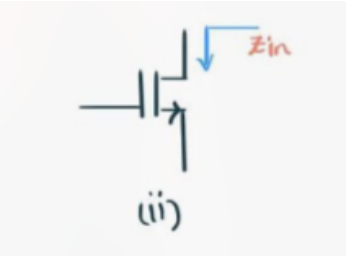

Figure 2.2.3: Circuit of 2.2(ii)

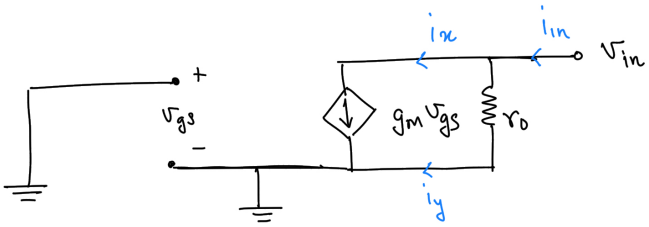

Figure 2.2.4: Equivalent Circuit of 2.2(ii)

From the equivalent circuit, we can see that,

$$\begin{aligned} i_{in} &= i_x + i_y, \text{ By KCL} \\ v_g &= 0 \\ v_s &= 0 \\ \implies v_{gs} &= 0 \\ \implies g_m v_{gs} &= 0 \\ \implies i_x &= 0 \\ \implies i_{in} &= i_y = \frac{v_{in}}{r_o} \\ \implies z_{in} &= r_o \end{aligned}$$

Therefore, $z_{in} = r_o$.

(iii)

Grounding the Drain and Gate terminals, the equivalent small signal circuit for the same will be as Figure 2.2.6

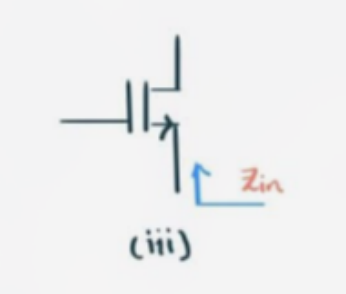

Figure 2.2.5: Circuit of 2.2(iii)

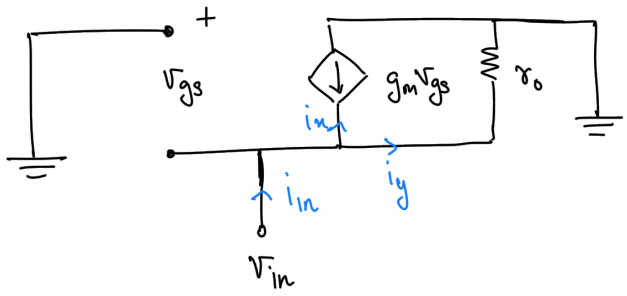

Figure 2.2.6: Equivalent Circuit of 2.2(iii)

From the equivalent circuit, we can see that,

$$\begin{aligned}
i_{in} &= i_x + i_y \\
v_g &= 0 \\
v_s &= v_{in} \\
\implies v_{gs} &= -v_{in} \\
\implies g_m v_{gs} &= -g_m v_{in} \\
i_x &= -g_m v_{gs} \\
\implies i_x &= g_m v_{in} \\
i_y &= \frac{v_{in}}{r_o} \\
\implies i_{in} &= g_m v_{in} + \frac{v_{in}}{r_o} \\
\implies z_{in} &= \frac{1}{g_m + \frac{1}{r_o}}
\end{aligned}$$

Therefore, $z_{in} = \frac{1}{g_m + \frac{1}{r_o}}$

(iv)

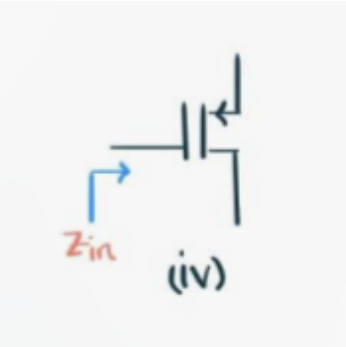

Figure 2.2.7: Circuit of 2.2(iv)

Grounding the Drain and Source terminals, the equivalent small signal circuit for the same will be as Figure 2.2.8

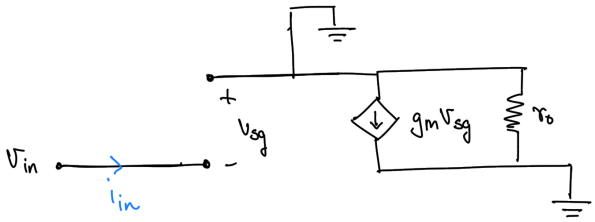

Figure 2.2.8: Equivalent Circuit of 2.2(iv)

Looking at the circuit we can see that i_{in} flows into an open terminal. Therefore, by KCL, i_{in} must be zero.

$$\therefore z_{in} \to \infty$$

(v)

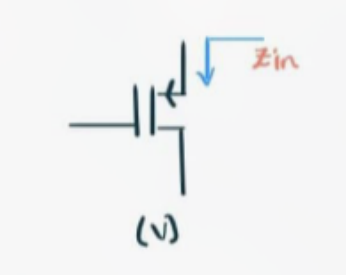

Figure 2.2.9: Circuit of 2.2(v)

Grounding the Drain and Gate terminals, the equivalent small signal circuit for

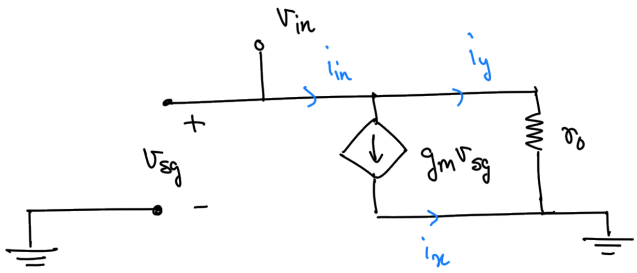

Figure 2.2.10: Equivalent Circuit of 2.2(v)

the same will be as Figure 2.2.10

From the equivalent circuit we can see that,

$$\begin{aligned} i_{in} &= i_x + i_y \\ v_s &= v_{in} \\ v_g &= 0 \\ \implies v_{sg} &= v_{in} \\ i_x &= g_m v_{sg} \\ \implies i_x &= g_m v_{in} \\ i_y &= \frac{v_{in}}{r_o} \\ \implies i_{in} &= g_m v_{in} + \frac{v_{in}}{r_o} \\ \implies z_{in} &= \frac{1}{g_m + \frac{1}{r_o}} \end{aligned}$$

(vi)

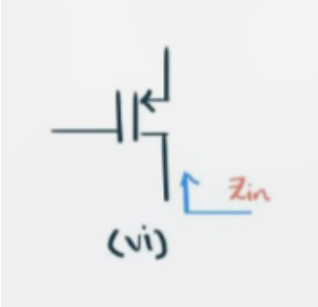

Figure 2.2.11: Circuit of 2.2(vi)

Grounding the Source and Gate terminals, the equivalent small signal circuit for the same will be as Figure 2.2.12

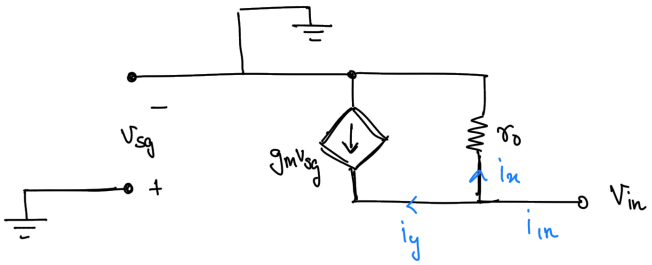

Figure 2.2.12: Equivalent Circuit of 2.2(vi)

From the equivalent circuit we can see that.

$$\begin{aligned} i_{in} &= i_x + i_y \\ v_s &= 0 \\ v_g &= 0 \\ \implies v_{sg} &= 0 \\ \implies g_m v_{sg} &= 0 \\ \implies i_y &= 0 \\ \implies i_{in} &= i_x = \frac{v_{in}}{r_o} \\ \implies z_{in} &= r_o \end{aligned}$$

(vii)

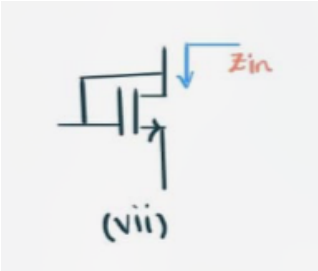

Figure 2.2.13: Circuit of 2.2(vii)

Grounding the Source terminal, the equivalent small signal circuit for the same will be as Figure 2.2.14

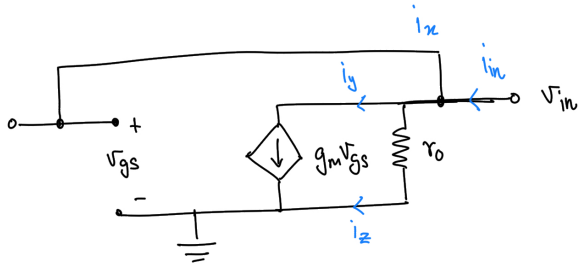

Figure 2.2.14: Equivalent Circuit of 2.2(vii)

From the equivalent circuit we can see that.

$$i_{in} = i_x + i_y + i_z$$

Since i_x flows into an open terminal, it is zero.

$$\begin{aligned} v_g &= v_{in} \\ v_s &= 0 \\ \implies v_{gs} &= v_{in} \\ i_y &= g_m v_{gs} = g_m v_{in} \\ i_z &= \frac{v_{in}}{r_o} \\ \implies i_{in} &= 0 + g_m v_{in} + \frac{v_{in}}{r_o} \\ \implies z_{in} &= \frac{1}{g_m + \frac{1}{r_o}} \end{aligned}$$

(viii)

Figure 2.2.15: Circuit of 2.2(viii)

Grounding the Drain terminal, the equivalent small signal circuit for the same

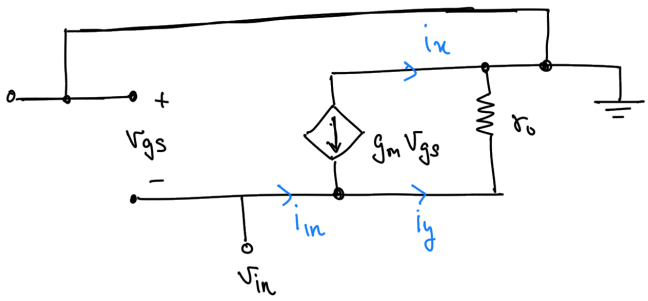

Figure 2.2.16: Equivalent Circuit of 2.2(viii)

will be as Figure 2.2.16

From the equivalent circuit we can see that.

$$\begin{aligned} i_{in} &= i_x + i_y \\ v_g &= 0 \\ v_s &= v_{in} \\ \implies v_{gs} &= -v_{in} \\ i_x &= -g_m v_{gs} = g_m v_{in} \\ i_y &= \frac{v_{in}}{r_o} \\ i_{in} &= g_m v_{in} + \frac{v_{in}}{r_o} \\ \implies z_{in} &= \frac{1}{g_m + \frac{1}{r_o}} \end{aligned}$$

(ix)

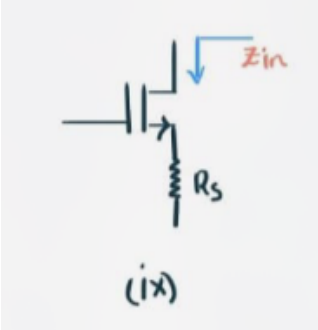

Figure 2.2.17: Circuit of 2.2(ix)

Grounding the Gate and the Resistor terminals, the equivalent small signal circuit for the same will be as Figure 2.2.18

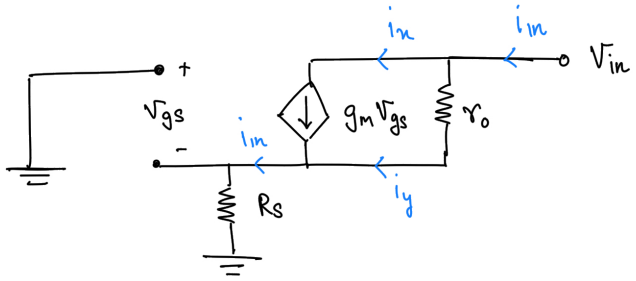

Figure 2.2.18: Equivalent Circuit of 2.2(ix)

From the equivalent circuit we can see that.

$$\begin{aligned}
i_{in} &= i_x + i_y \\
v_g &= 0 \\
v_s &= i_{in} R_s \\
\implies v_{gs} &= -i_{in} R_s \\
i_x &= g_m v_{gs} = -g_m i_{in} R_s \\
i_y &= \frac{v_{in}}{r_o} \\
\implies i_{in} &= -g_m i_{in} R_s + \frac{v_{in}}{r_o} \\
i_{in}\left(1 + g_m R_s\right) &= \frac{v_{in}}{r_o} \\
\implies z_{in} &= r_o\left(1 + g_m R_s\right)
\end{aligned}$$

(x)

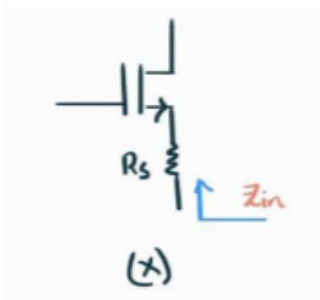

Figure 2.2.19: Circuit of 2.2(x)

Grounding the Gate and the Drain terminals, the equivalent small signal circuit for the same will be as Figure 2.2.20

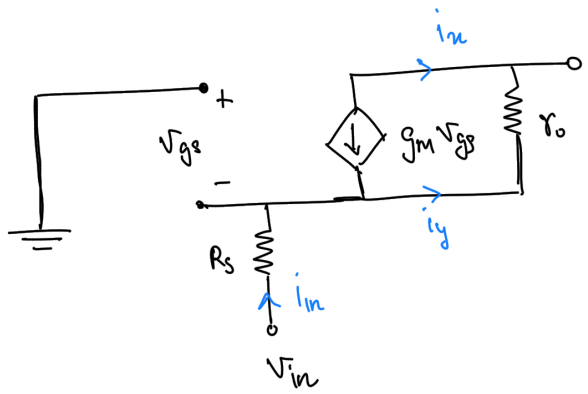

Figure 2.2.20: Equivalent Circuit of 2.2(x)

From the equivalent circuit we can see that.

$$\begin{aligned}
i_{in} &= i_x + i_y \\
v_g &= 0 \\
v_s &= v_{in} - i_{in}R_s \\
\implies v_{gs} &= i_{in}R_s - v_{in} \\
i_x &= -g_m v_{gs} = g_m(v_{in} - i_{in}R_s) \\
i_y &= \frac{v_{in} - i_{in}R_s}{r_o} \\
\implies i_{in} &= g_m(v_{in} - i_{in}R_s) + \frac{v_{in} - i_{in}R_s}{r_o} \\
i_{in}\left(1 + g_m R_s + \frac{R_s}{r_o}\right) &= v_{in}\left(g_m + \frac{1}{r_o}\right) \\
\implies z_{in} &= \frac{1 + g_m R_s + \frac{R_s}{r_o}}{g_m + \frac{1}{r_o}}
\end{aligned}$$

3 LTSpice Simulation

3.1

Plot of I_{DS} vs V_{DS} at multiple values of V_{GS} is given by Figure 3.1.2

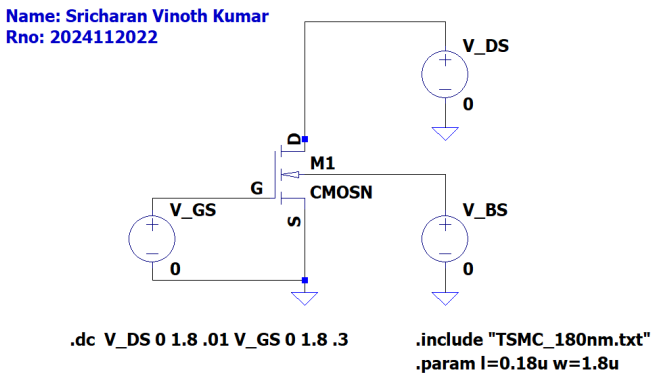

Figure 3.1.1: LTSpice Schematic

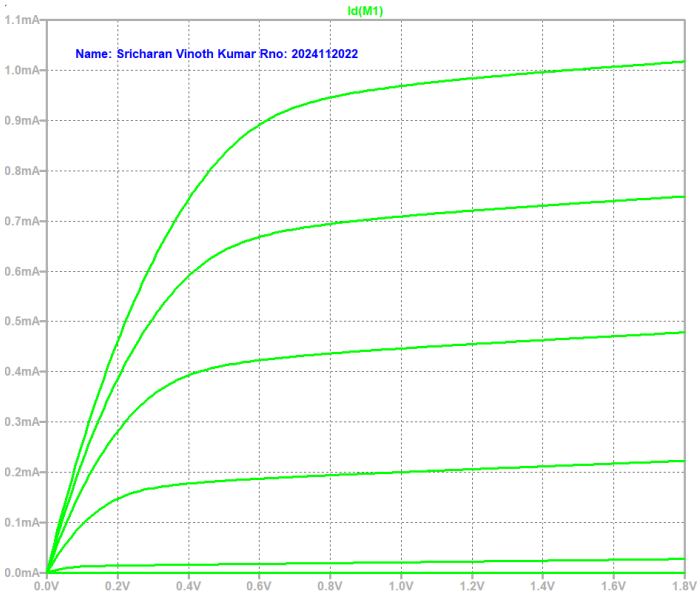

Figure 3.1.2: Plot of I_{DS} vs V_{DS}. X axis represents V_{DS} and Y axis represents I_{DS}. Each line represents a value of V_{GS}. Higher the value of V_{GS}, higher the value of I_{DS}

3.2

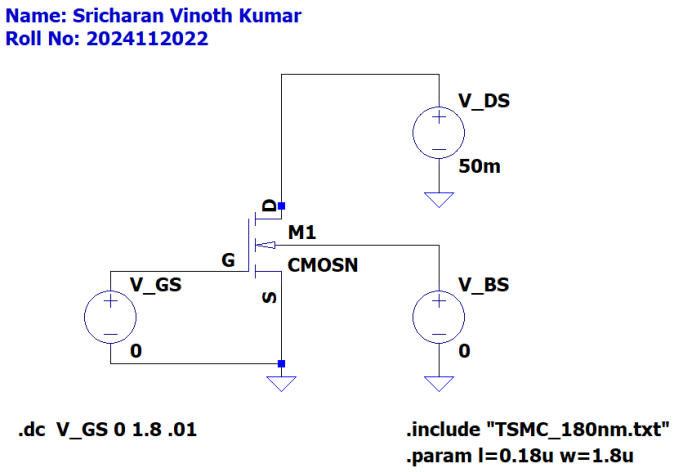

Figure 3.2.1: LTSpice Schematic

For the plot in Figure 3.2.2, the following parameters were used:

- $V_{DS} = 50mV$
- $V_{BS} = 0V$
- $\frac{W}{L} = \frac{1.8u}{0.18u}$

We know that V_{TH} is the voltage at which the channel is formed and the MOSFET starts conducting. In the context of the plot, it must be the point where the value of I_{DS} starts to become non-zero. We can approximate that point as $411.368mV$, as shown in Figure 3.2.3

To calculate $\mu_n C_{ox} \frac{W}{L}$, we take the point of highest slope, given by Figure 3.2.4, which is (707.888mV, 25.066µA)

Since V_{DS} is small, we assume the MOSFET to be in Triode region, Therefore,

$$\begin{aligned} I_{DS} &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(2(V_{GS}-V_{TH})V_{DS} - V_{DS}^2) \\ \implies \mu_n C_{ox} &= \frac{2I_{DS}}{\frac{W}{L}(2(V_{GS}-V_{TH})V_{DS} - V_{DS}^2)} \\ \implies \mu_n C_{ox} &= \frac{2 \times 25.066 \times 10^{-6}}{10 \times (2(0.7078-0.4113)0.05 - (0.05)^2)} \end{aligned}$$

On solving, we get,

$$\mu_n C_{ox} = 0.00018464825 = 184.648\mu A/V^2$$

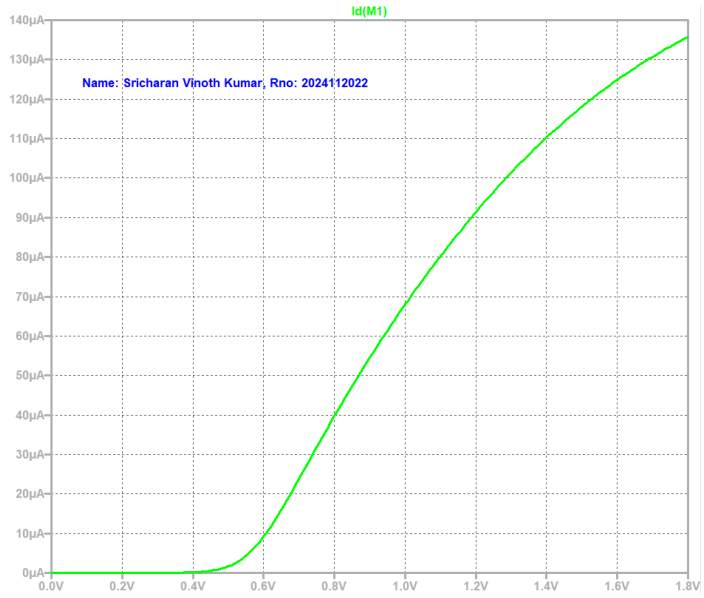

Figure 3.2.2: Plot of I_{DS} vs V_{GS}. X axis represents V_{GS} and Y axis represents I_{DS}.

The obtained value is reasonably close to the actual value (roughly $240\mu A/V^2$)

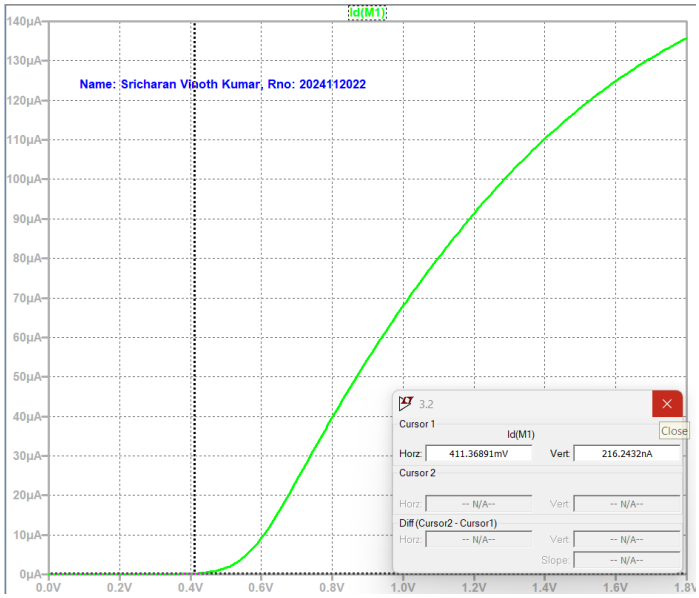

Figure 3.2.3: Plot of I_{DS} vs V_{GS} with V_{TH} approximation. X axis represents V_{GS} and Y axis represents I_{DS}.

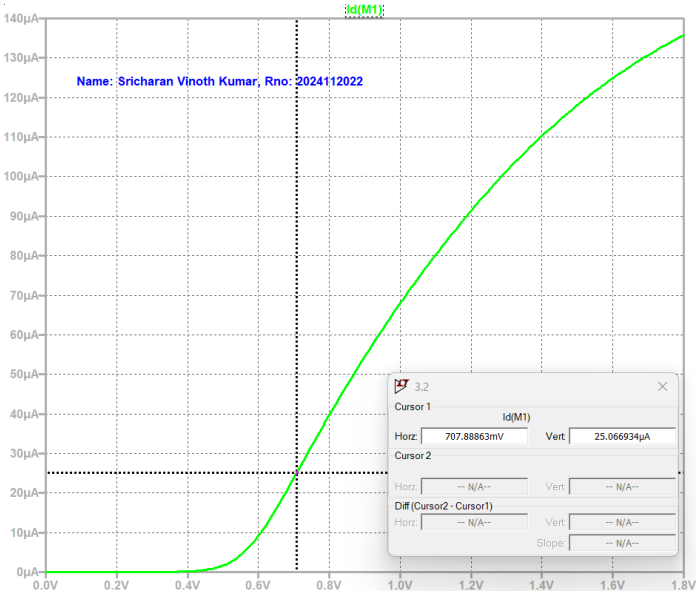

Figure 3.2.4: Plot of I_{DS} vs V_{GS} with point of maximum slope. X axis represents V_{GS} and Y axis represents I_{DS}.

For $V_{DS} = 1.8V$, we get the plot shown in Figure 3.2.5

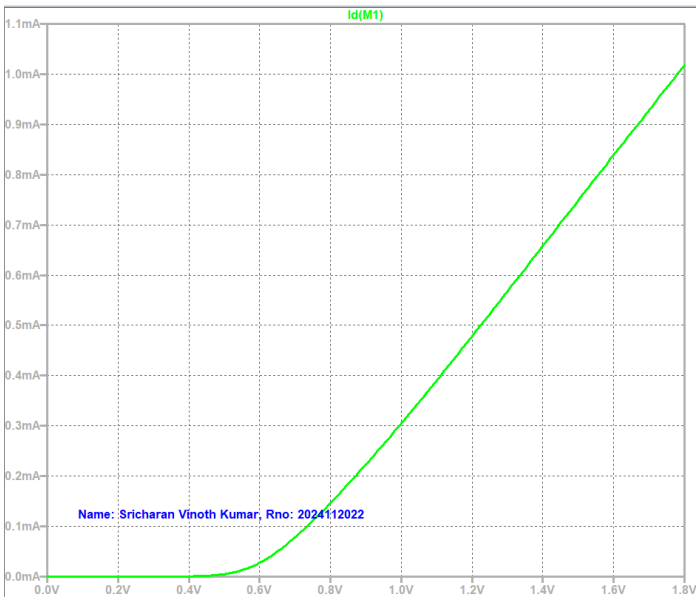

Figure 3.2.5: Plot of I_{DS} vs V_{GS} at $V_{DS} = 1.8V$. X axis represents V_{GS} and Y axis represents I_{DS}.

To find V_{TH}, using the same logic as before, i,e, find the point at which I_{DS} starts becoming non-zero, we get $V_{TH} = 369.605mV$, as per Figure 3.2.6
Note: That specific point was chosen since it had a similar current value to the point considered for V_{TH} in the $V_{DS} = 50mV$ case, (approximately 220nA), for the sake of uniformity.
We see that V_{TH} has decreased, when compared to the $V_{DS} = 50mV$ case. This can be attributed to the phenomena of Drain-Induced Barrier Lowering.

Drain-Induced Barrier Lowering:
When drain voltage increases, the threshold voltage for channel formation decreases, enabling channel formation at an earlier stage of V_{GS}. This occurs because a high drain voltage attracts charge carriers towards the Channel region, increasing charge density and making it easier to form the channel, which explains our observations.

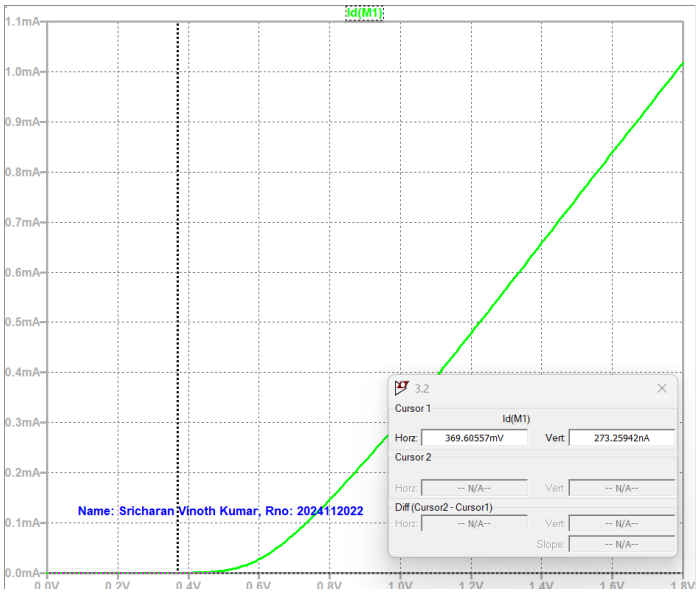

Figure 3.2.6: Plot of I_{DS} vs V_{GS} at $V_{DS} = 1.8V$,with V_{TH} approximation. X axis represents V_{GS} and Y axis represents I_{DS}.

3.3

For NMOS, taking $V_{DS} = 1V$,

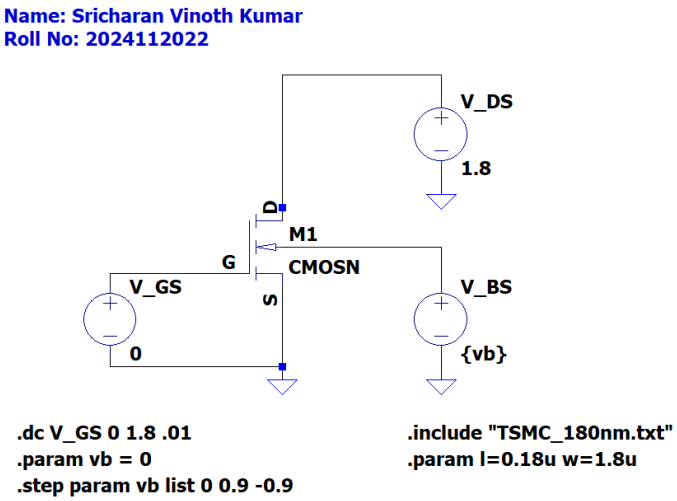

Figure 3.3.1: LTSpice Schematic

If we plot I_{DS} vs V_{GS} for different values of V_{BS}, we get the plot obtained in Figure 3.3.2

In the previous question, we took V_{TH} as the point in the plot where I_{DS} starts becoming non zero. Applying the same logic here, we get V_{TH} values as,

(a) $V_{TH} = 453.13225mV$ at $V_{BS} = 0V$

(b) $V_{TH} = 311.13689mV$ at $V_{BS} = 0.9V$

(c) $V_{TH} = 659.86079mV$ at $V_{BS} = -0.9V$

from Figure 3.3.3.

Note: These points was chosen such that they had similar corresponding current values (approximately $1.9\mu A$*), for the sake of uniformity.*

We see that V_{TH} decreases with increase in V_{BS}

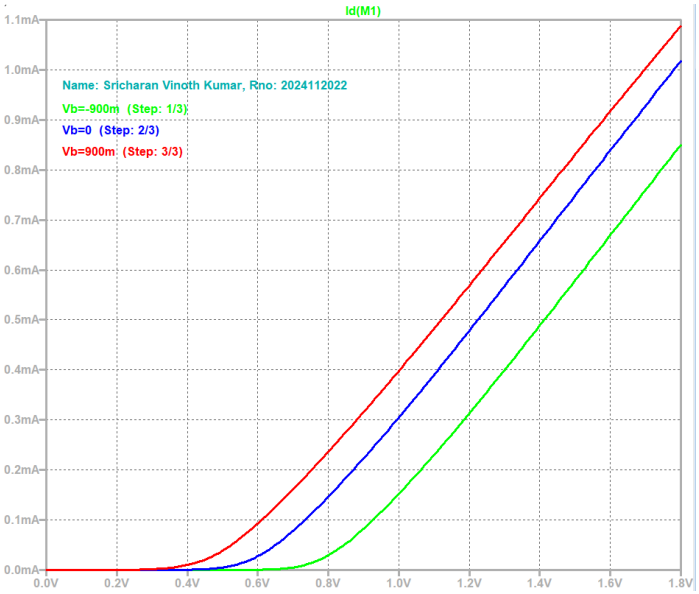

Figure 3.3.2: Plot of I_{DS} vs V_{GS} at different values of V_{BS} mentioned in the plot. X axis represents V_{GS} and Y axis represents I_{DS}.

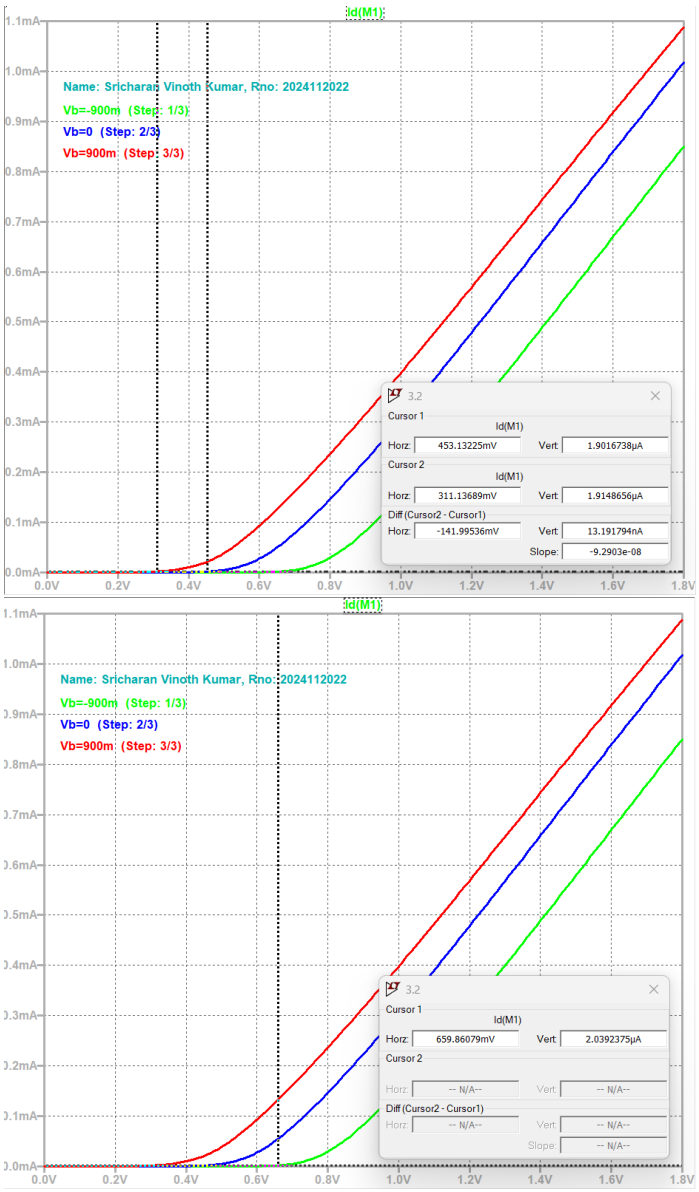

Figure 3.3.3: Plot of I_{DS} vs V_{GS} at different values of V_{BS} mentioned in the plot, with V_{TH} Measurement. X axis represents V_{GS} and Y axis represents I_{DS}. (Top Image, for $V_{BS} = 0V$ and $V_{BS} = 0.9V$, Bottom Image for $V_{BS} = -0.9V$)

For PMOS, taking $V_{SD} = 1V$,

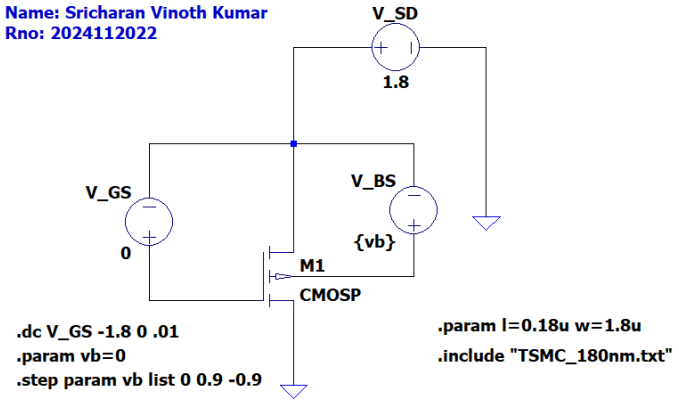

Figure 3.3.4: LTSpice Schematic

If we plot I_{DS} vs V_{GS} for different values of V_{BS}, we get the plot obtained in Figure 3.3.5

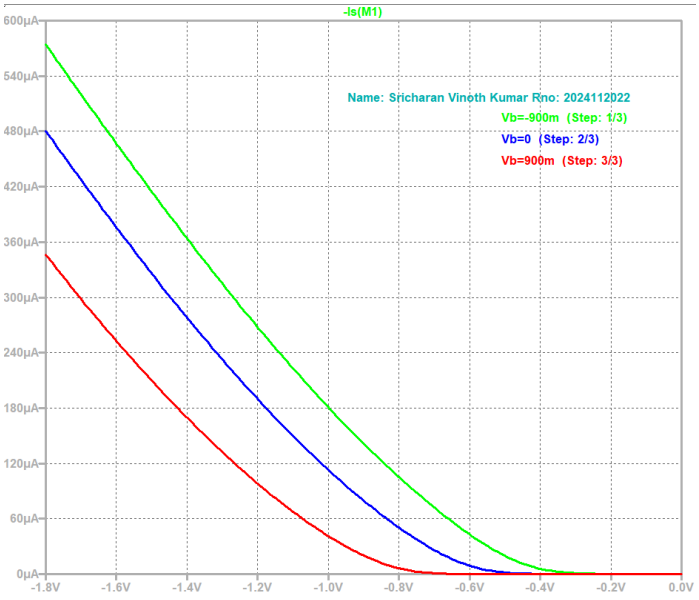

Figure 3.3.5: Plot of I_{SD} vs V_{GS} at different values of V_{BS} mentioned in the plot. X axis represents V_{GS} and Y axis represents I_{SD}.

Note: In 3.3.5, we are plotting I_{SD}, since I_{DS} is negative. So we are using the negative of I_{DS} within LTSpice to find I_{SD}, hence the negative sign in the plot label.
We are taking V_{TH} as the point in the plot where I_{DS} starts becoming zero. We get the values as,

(a) $V_{TH} = -505.00582mV$ at $V_{BS} = 0V$

(b) $V_{TH} = -733.41094mV$ at $V_{BS} = 0.9V$

(c) $V_{TH} = -331.08265mV$ at $V_{BS} = -0.9V$

from Figure 3.3.6.
Note: These points was chosen such that they had similar corresponding current values (approximately $1.9\mu A$*), for the sake of uniformity.*
We see that V_{TH} decreases with increase in V_{BS} and $|V_{TH}|$ increases with increase in V_{BS}
The 2 results obtained, from NMOS and PMOS, can be summarized as:
V_{TH} decreases with increase in V_{BS}
This result can be attributed to body effect.

Body Effect:
An increase in V_{BS} causes V_{TH} to fall. This phenomena is expressed mathematically by the equation,

$$\begin{aligned} V_{th} &= V_{th0} + \gamma\left(\sqrt{V_{SB} + \phi_f} - \sqrt{\phi_f}\right), \text{ for NMOS} \\ V_{th} &= V_{th0} + \gamma\left(\sqrt{|V_{SB} + \phi_f|} - \sqrt{\phi_f}\right), \text{ for PMOS} \end{aligned} \tag{3.3.1}$$

Where,

- V_{th} = Threshold Voltage
- V_{th0} = Threshold voltage when $V_{SB} = 0$.
- γ = Body effect coefficient.
- ϕ_f = Fermi potential.
- $V_{SB} = V_S - V_B$ (Source-to-Bulk voltage).

From the equation we see that $V_{th} \propto \sqrt{V_{SB}}$ approximately, which explains our observations.

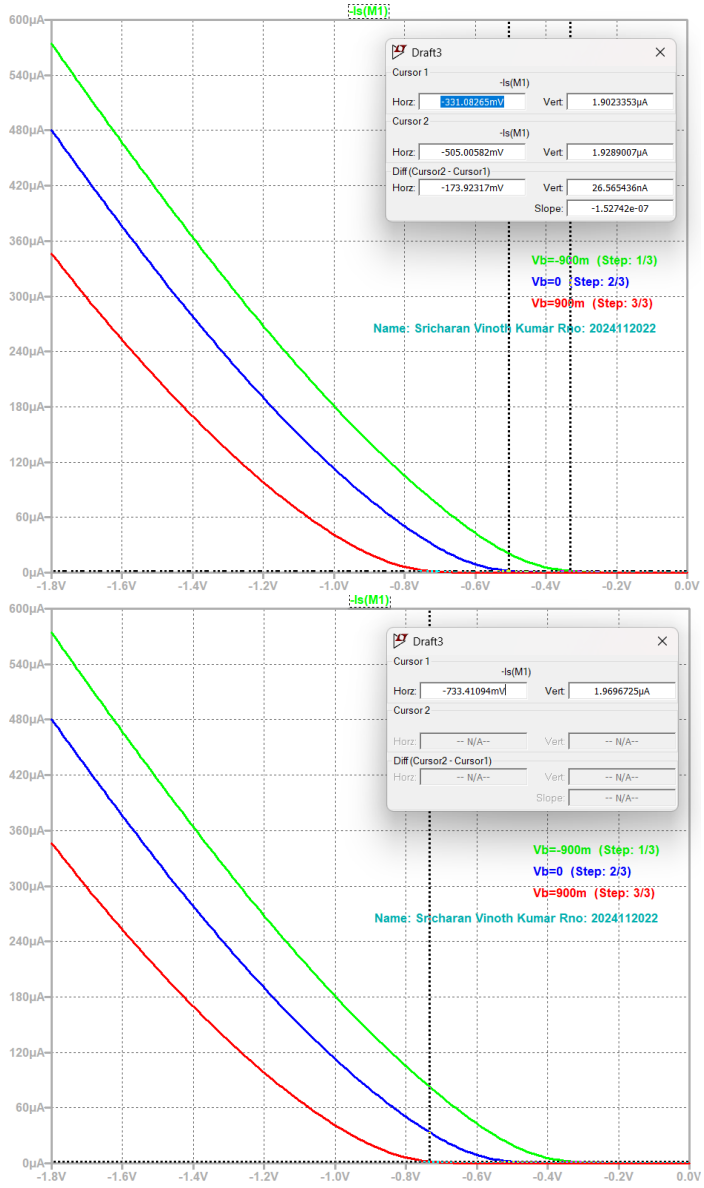

Figure 3.3.6: Plot of I_{SD} vs V_{GS} at different values of V_{BS} mentioned in the plot, with V_{TH} Measurement. X axis represents V_{GS} and Y axis represents I_{SD}. (Top Image, for $V_{BS} = 0V$ and $V_{BS} = -0.9V$, Bottom Image for $V_{BS} = 0.9V$)