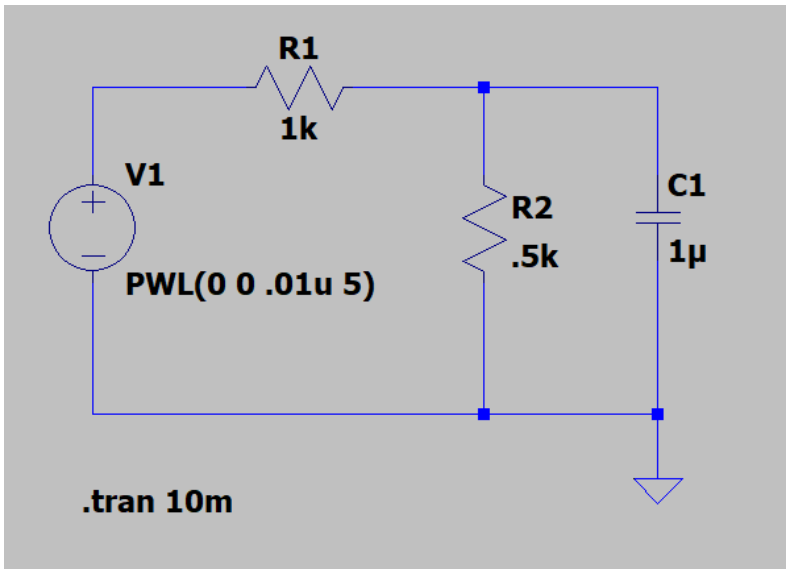
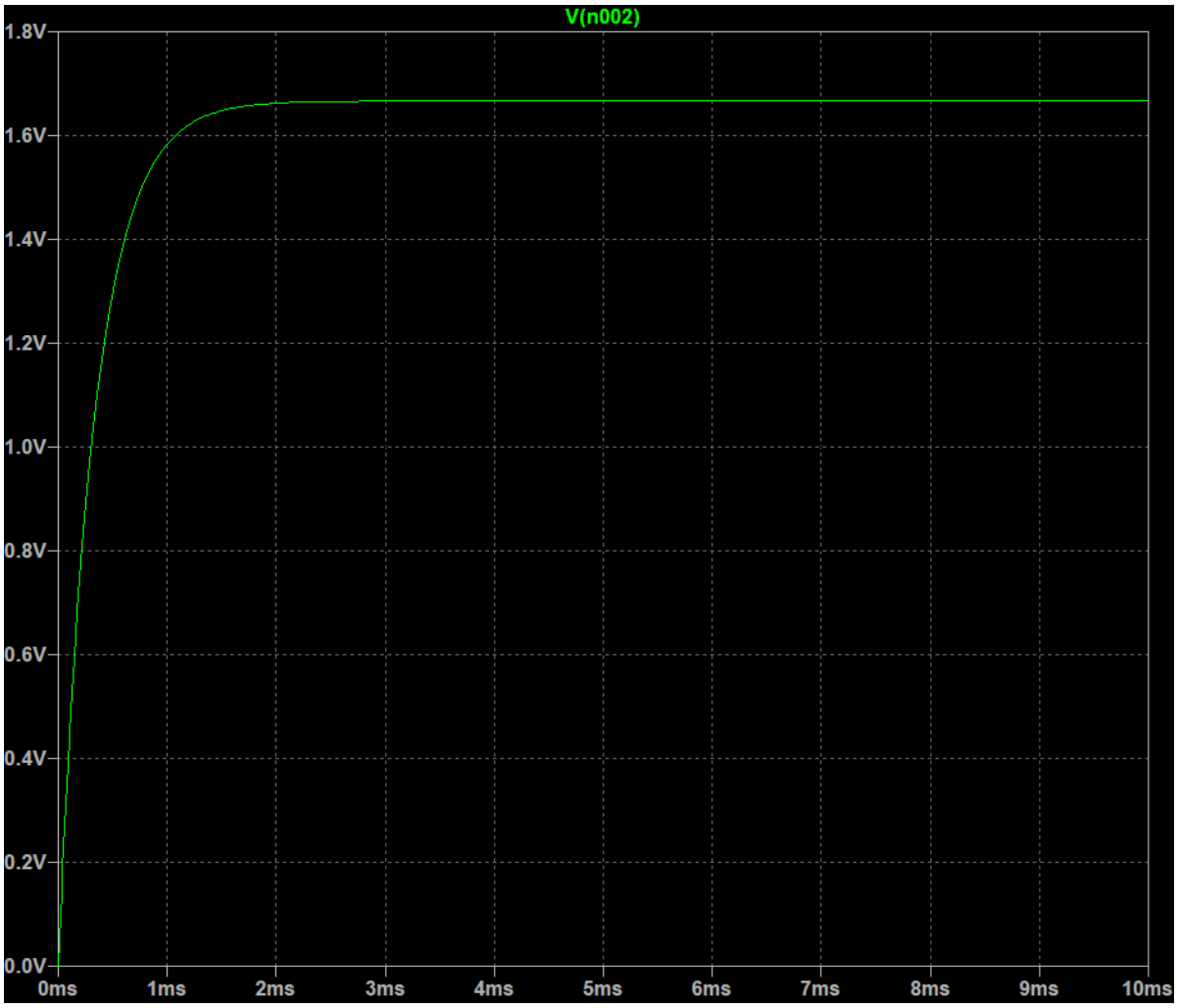
1.2

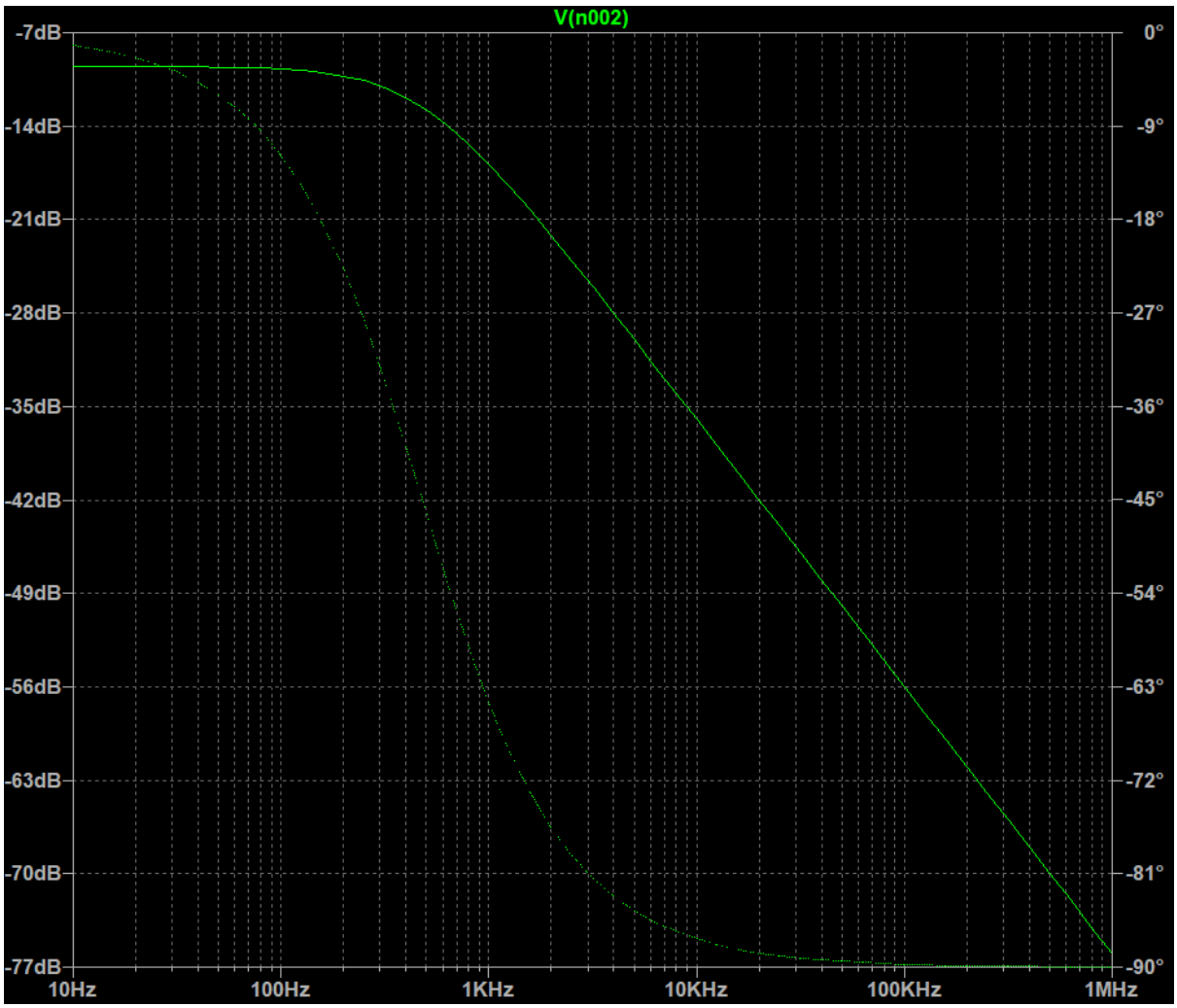
c) Circuit:



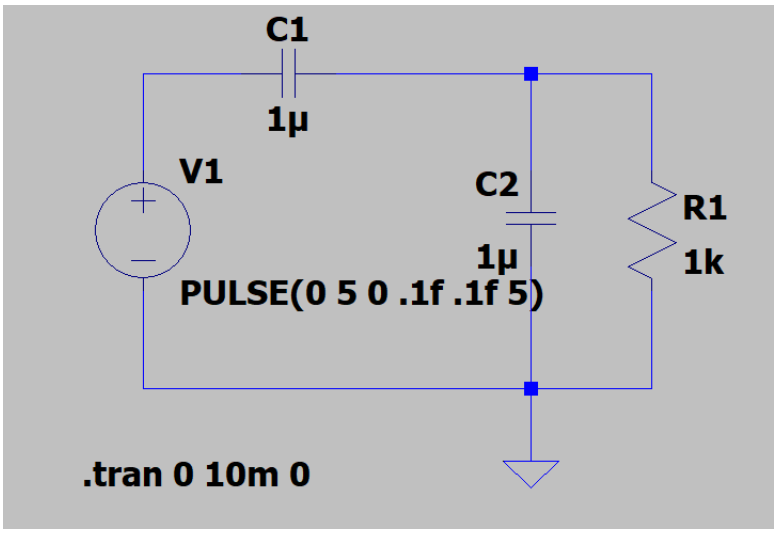
DC Response:



Bode Plot:

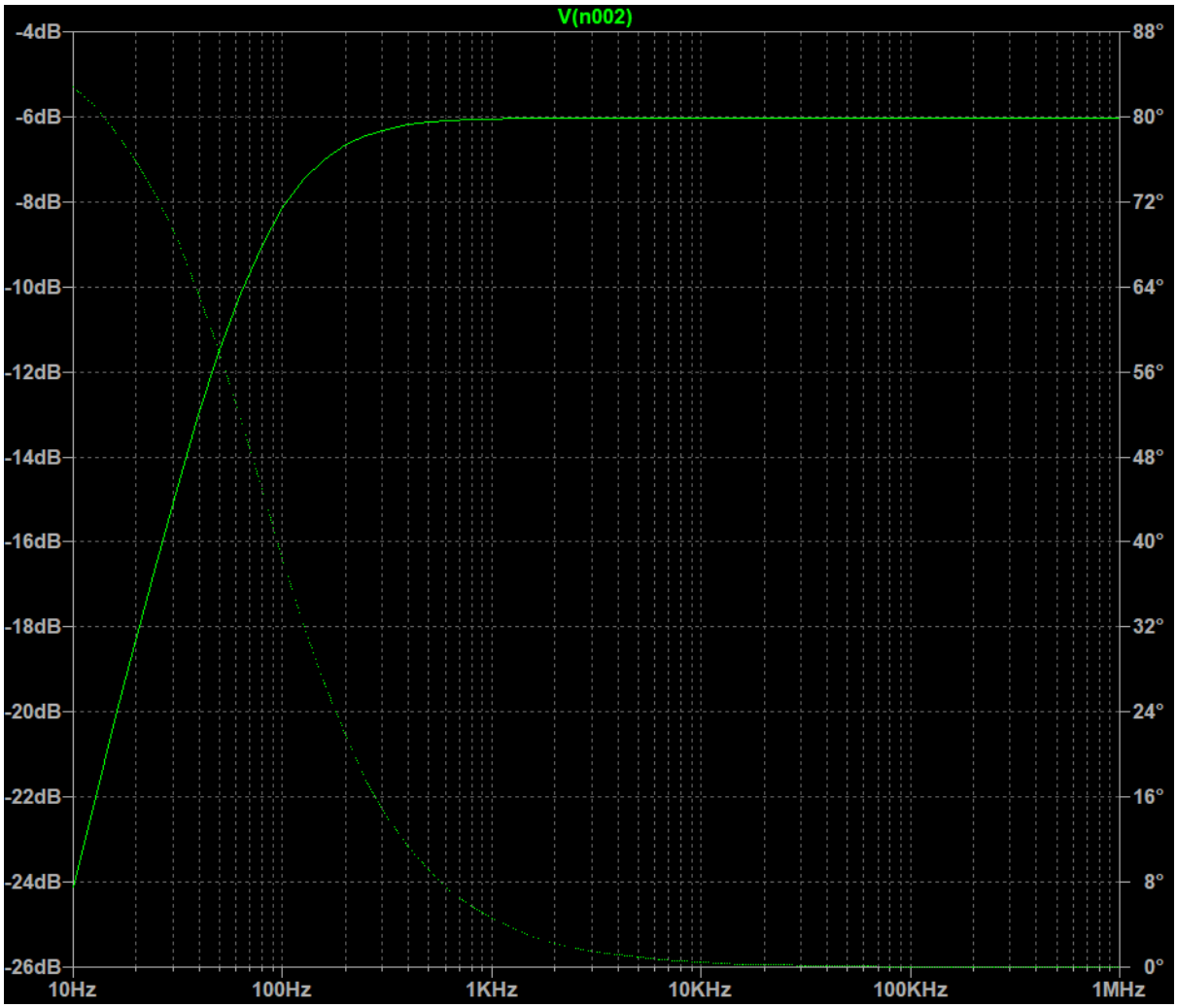

V(n002)
-7dB
-14dB
-21dB
-28dB
-35dB
-42dB
-49dB
-56dB
-63dB
-70dB
-77dB
0°
-9°
-18°
-27°
-36°
-45°
-54°
-63°
-72°
-81°
-90°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

d) Circuit:



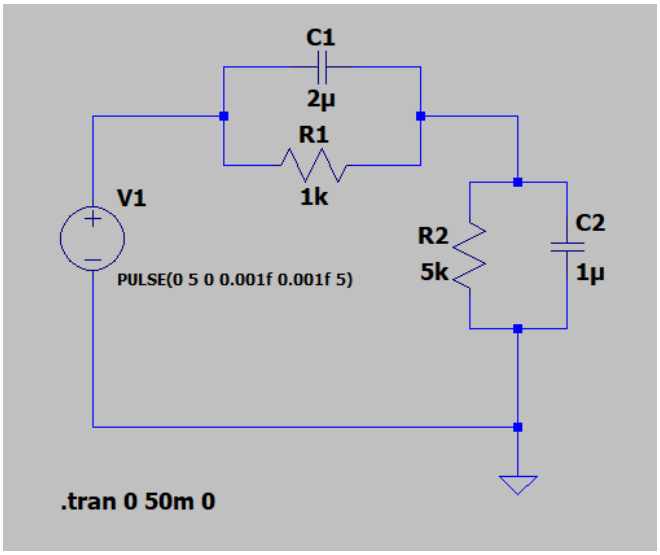
DC Response:

Bode Plot:


V(n002)
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB
-16dB
-18dB
-20dB
-22dB
-24dB
-26dB
88°
80°
72°
64°
56°
48°
40°
32°
24°
16°
8°
0°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

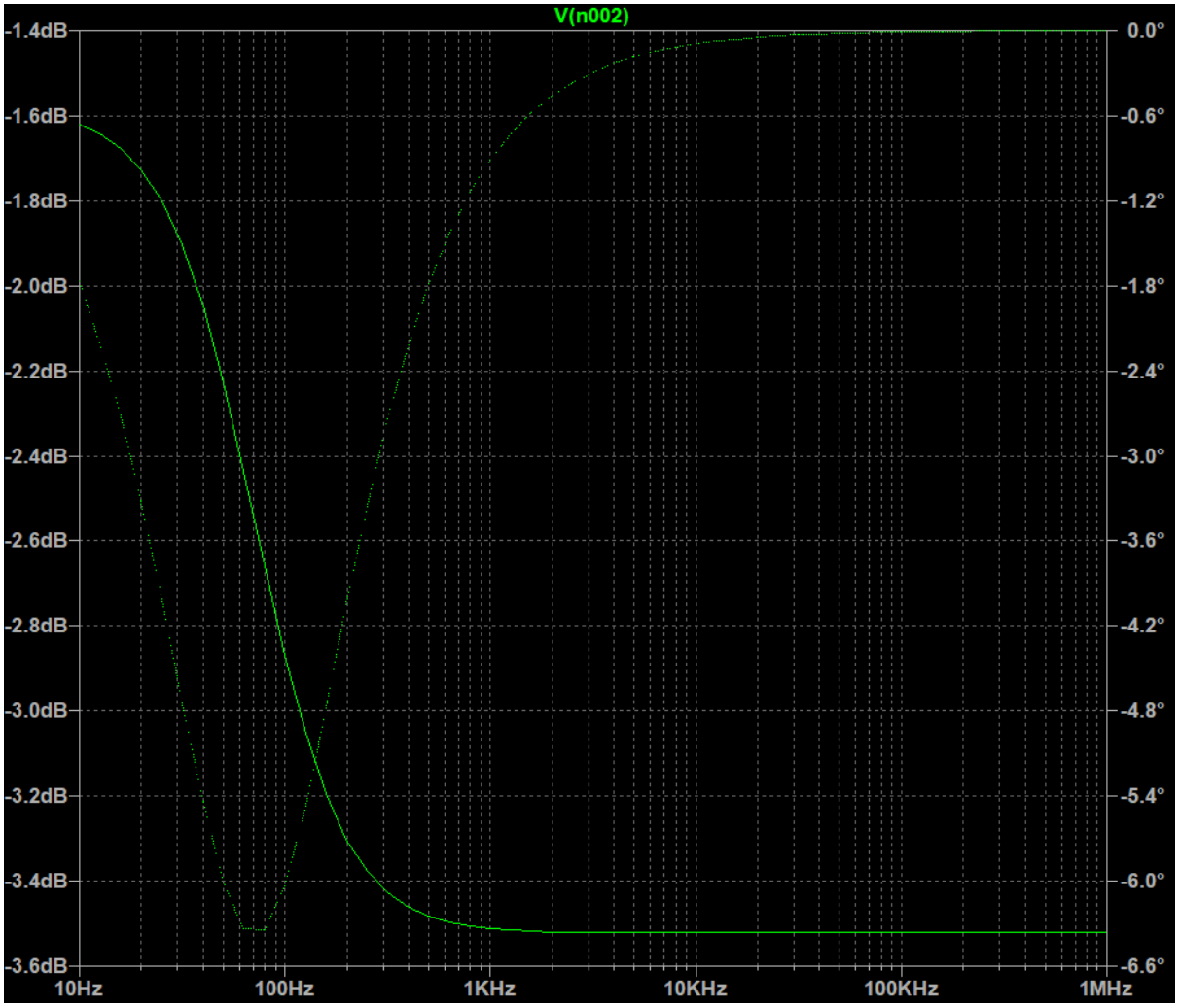
e) CASE 1:

Circuit:



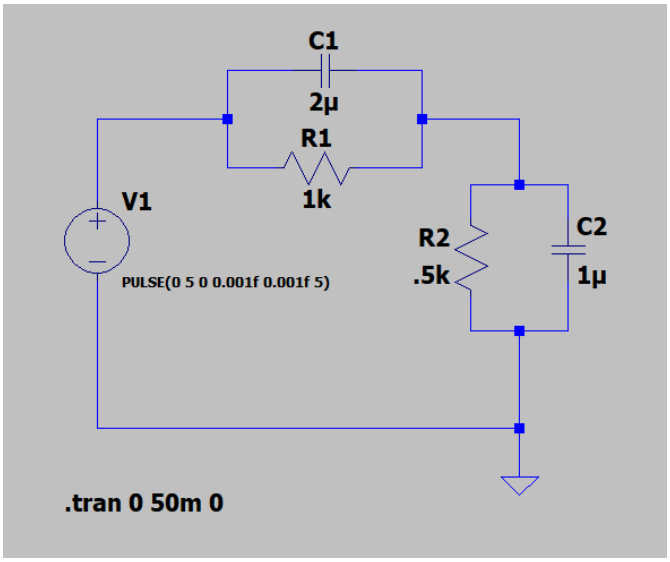
DC Response:

Bode Plot:

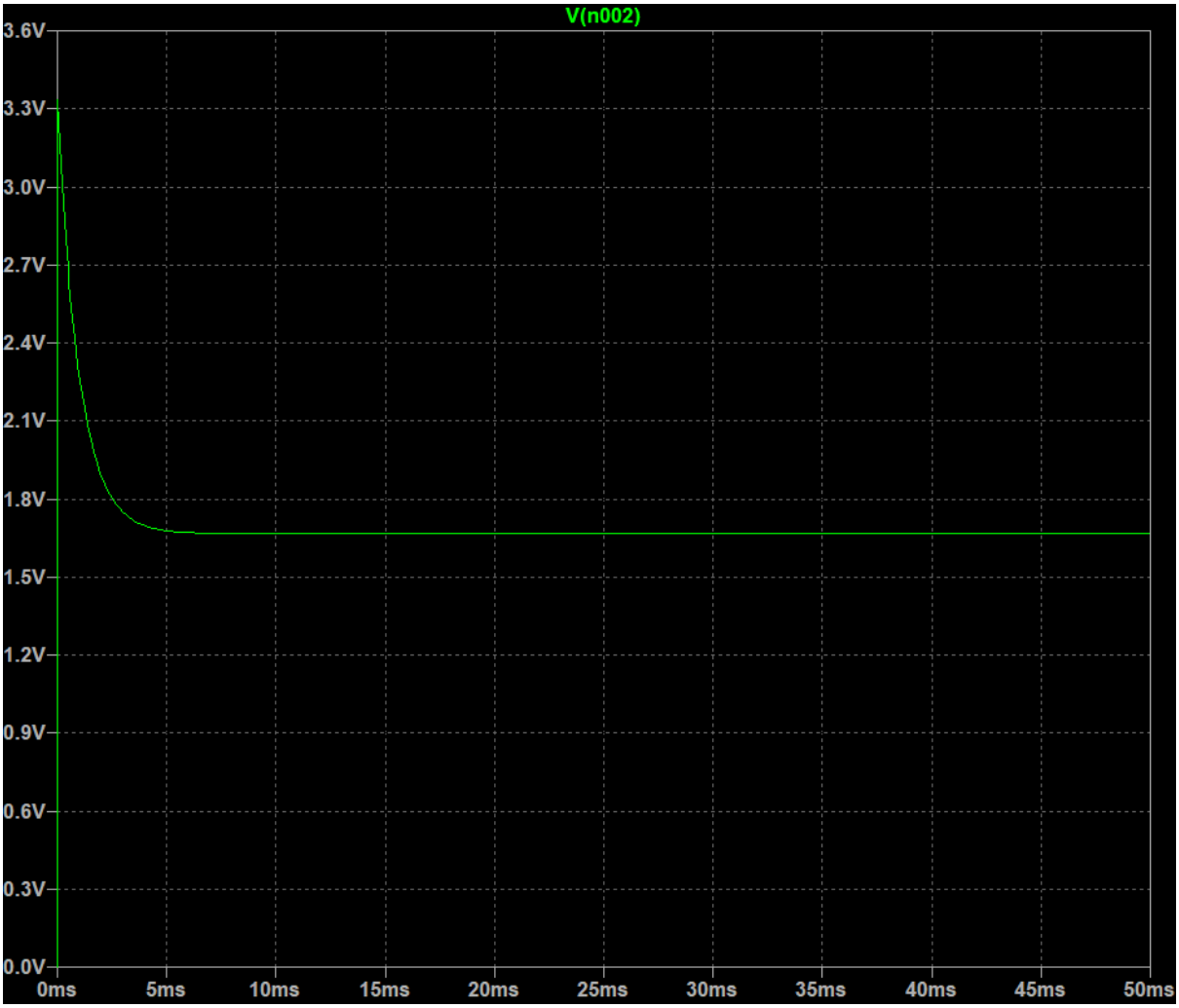

V(n002)
-1.4dB
-1.6dB
-1.8dB
-2.0dB
-2.2dB
-2.4dB
-2.6dB
-2.8dB
-3.0dB
-3.2dB
-3.4dB
-3.6dB
0.0°
-0.6°
-1.2°
-1.8°
-2.4°
-3.0°
-3.6°
-4.2°
-4.8°
-5.4°
-6.0°
-6.6°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

CASE 2:

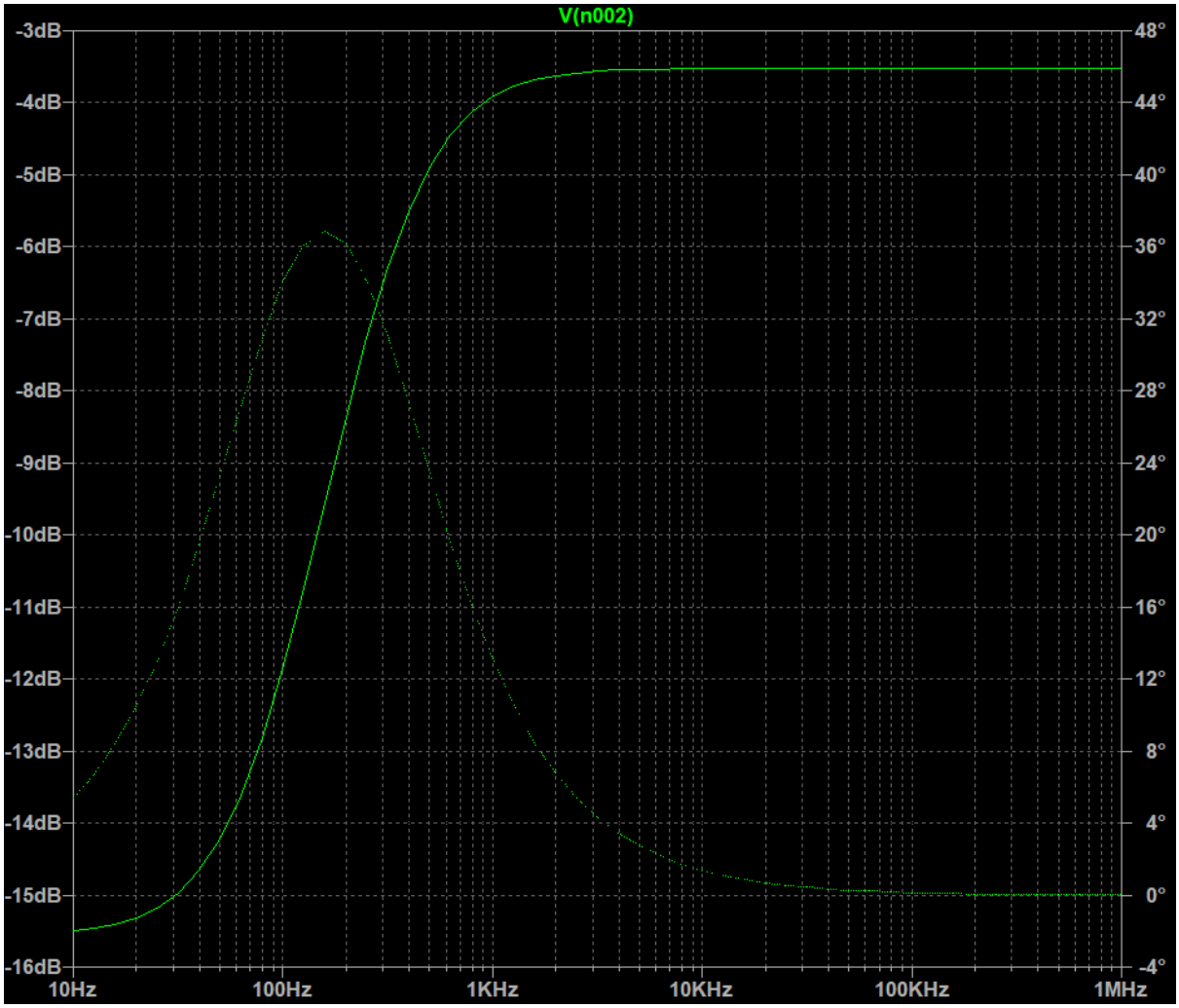
Circuit:



DC Response:

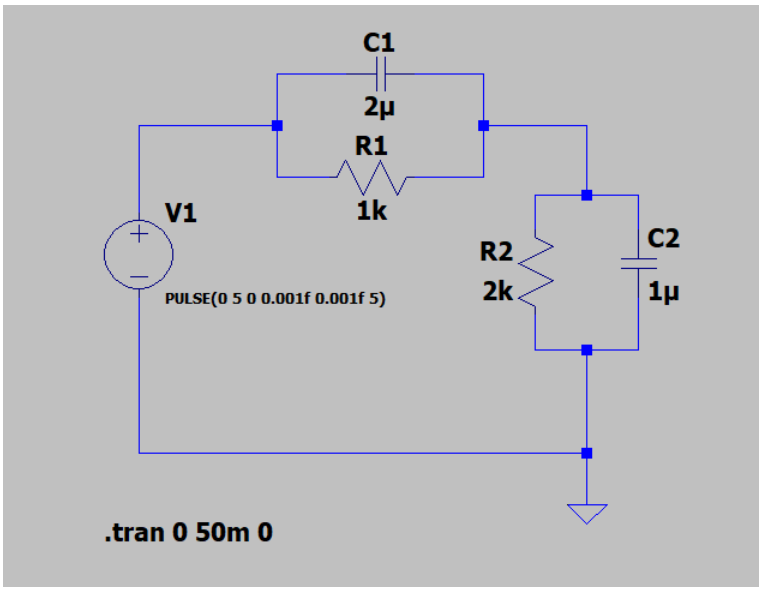


Bode Plot:

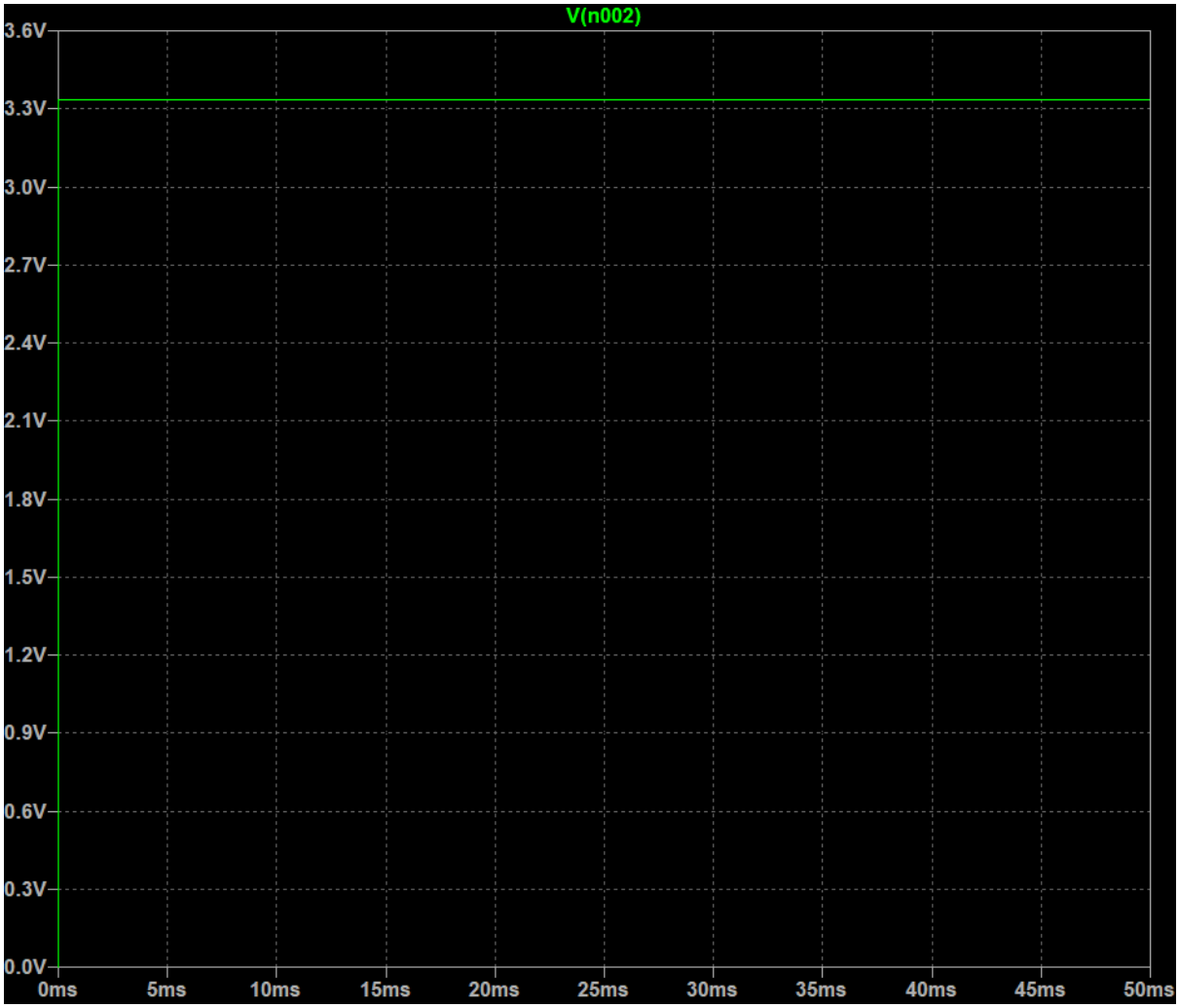


CASE 3:

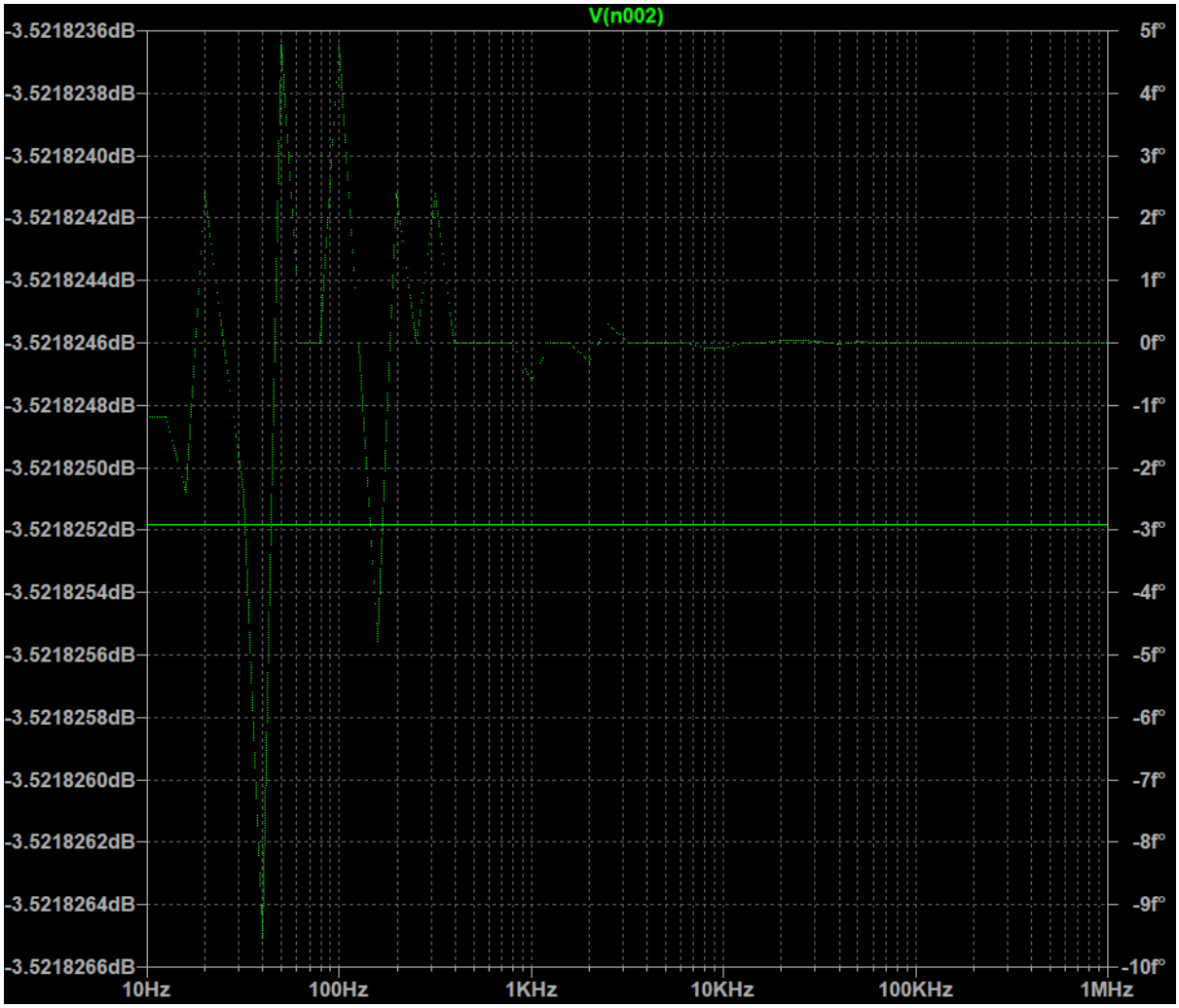
Circuit:



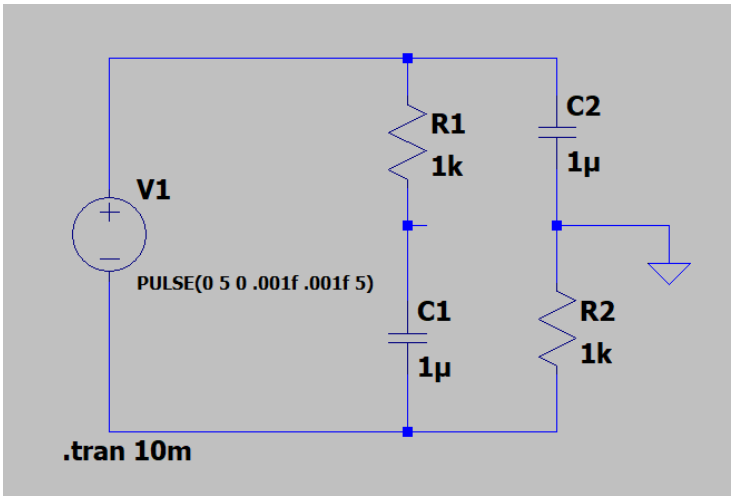
DC Response:


V(n002)
3.6V
3.3V
3.0V
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms

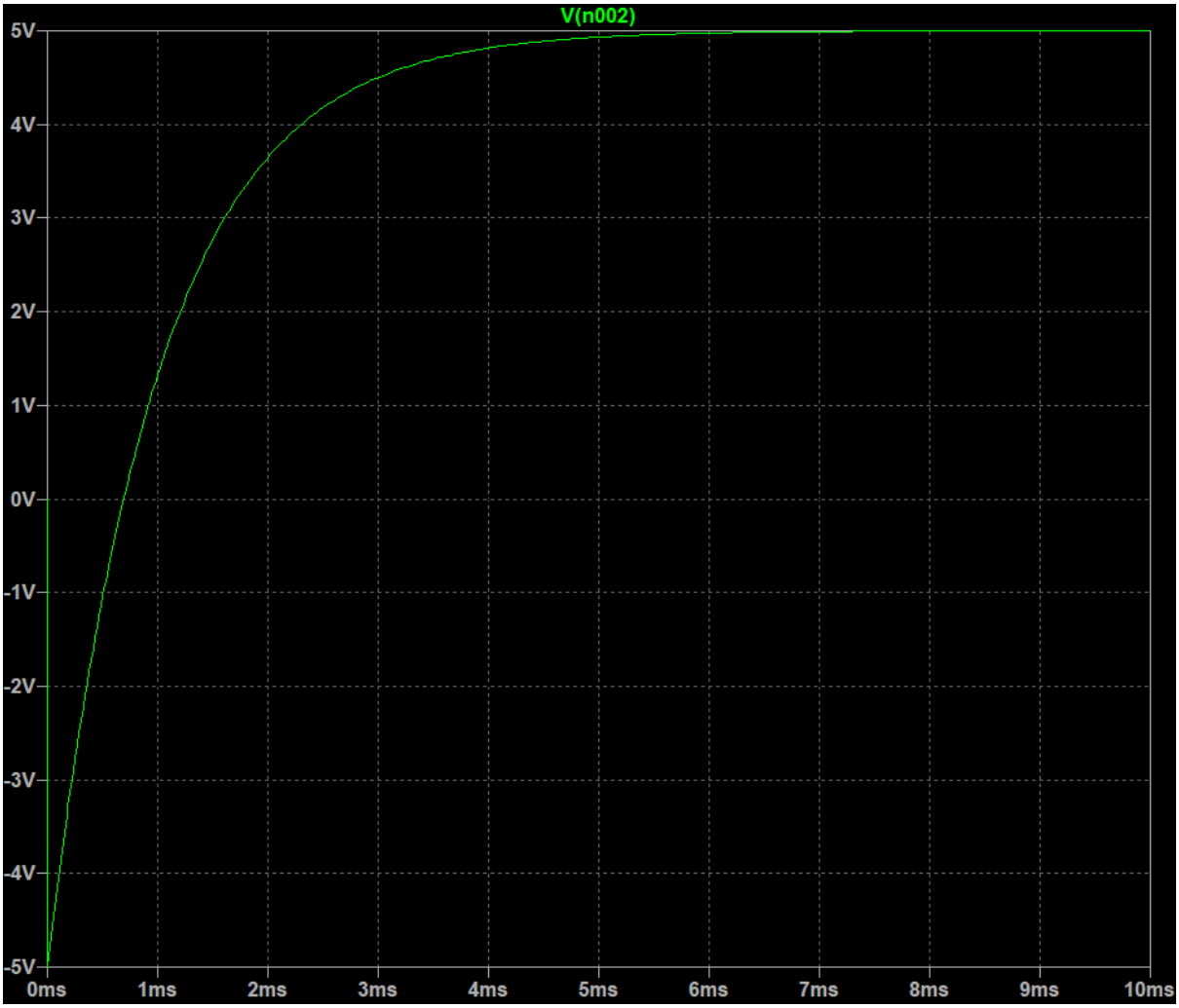
Bode Plot:


V(n002)
-3.5218236dB
-3.5218238dB
-3.5218240dB
-3.5218242dB
-3.5218244dB
-3.5218246dB
-3.5218248dB
-3.5218250dB
-3.5218252dB
-3.5218254dB
-3.5218256dB
-3.5218258dB
-3.5218260dB
-3.5218262dB
-3.5218264dB
-3.5218266dB
5f°
4f°
3f°
2f°
1f°
0f°
-1f°
-2f°
-3f°
-4f°
-5f°
-6f°
-7f°
-8f°
-9f°
-10f°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

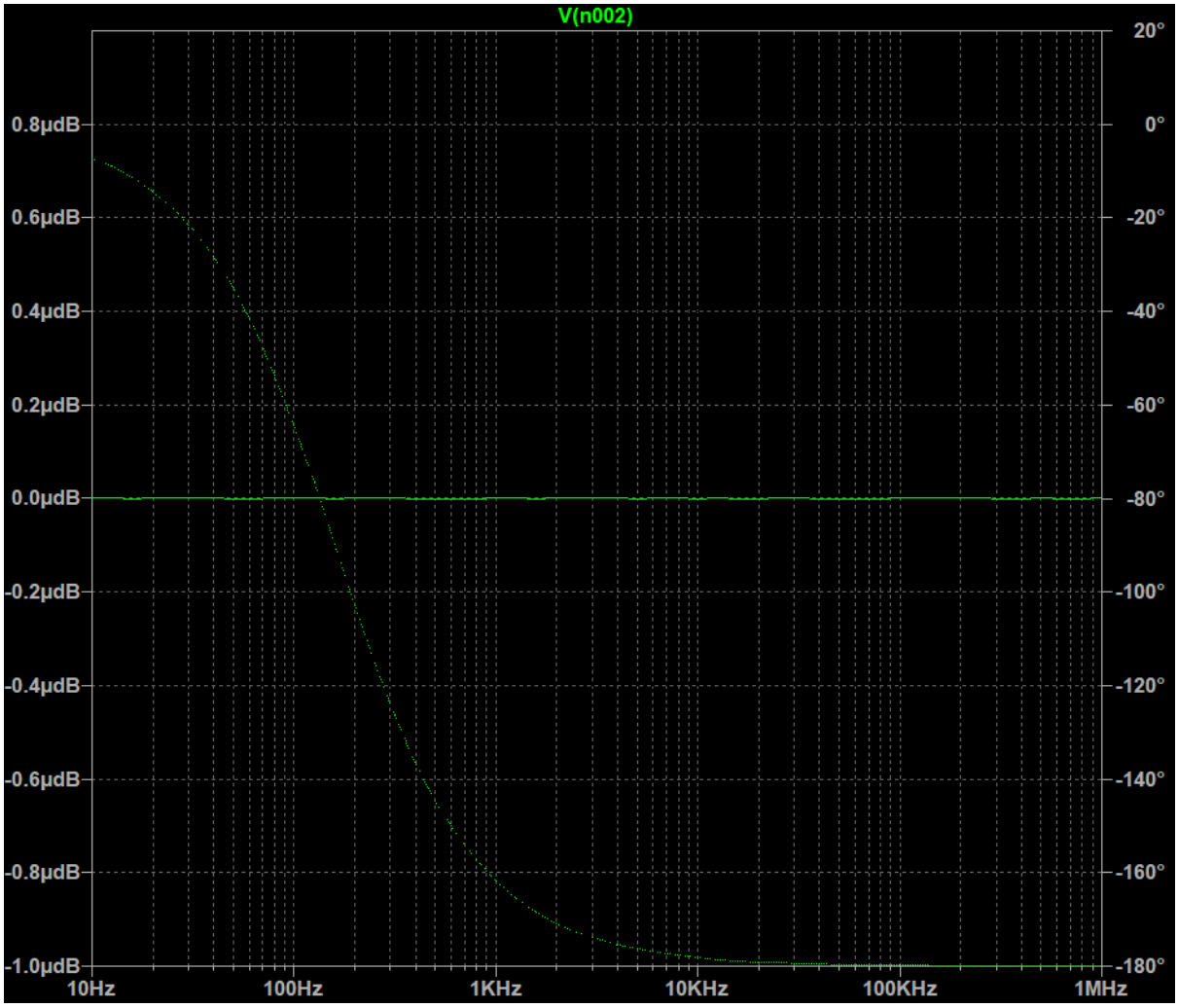
f) Circuit:



DC Response:

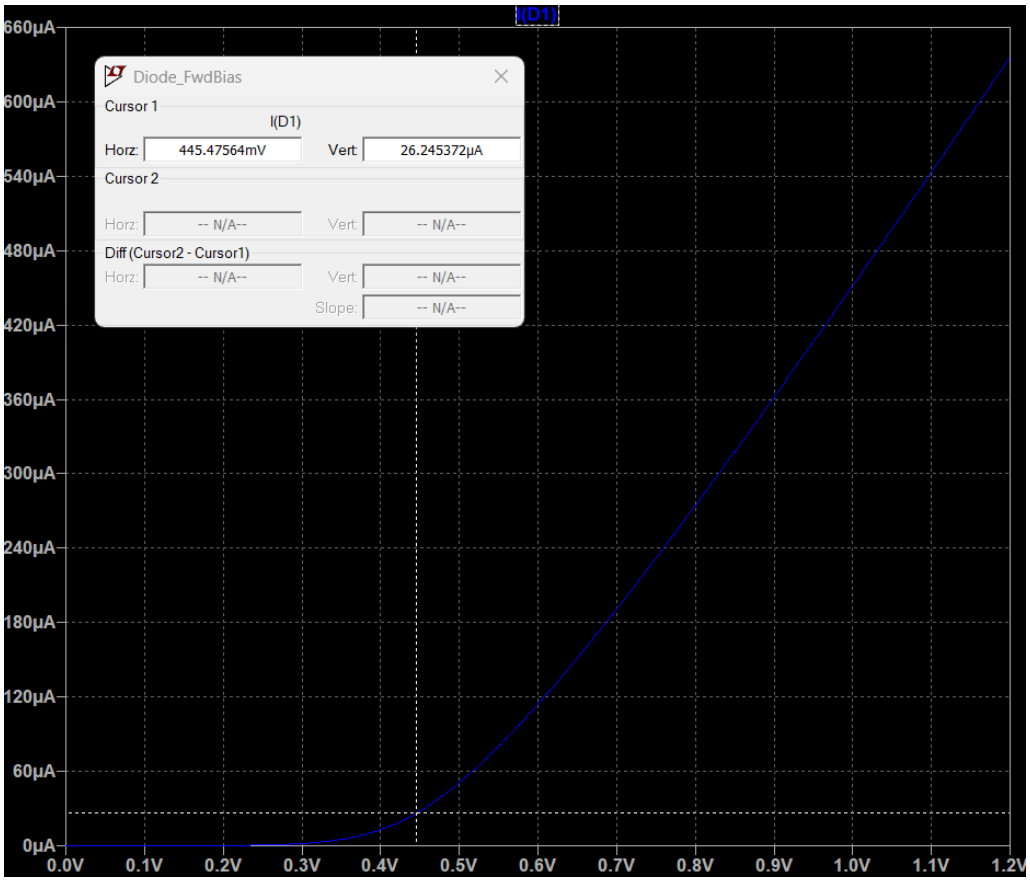


Bode Plot:


V(n002)
0.8µdB
0.6µdB
0.4µdB
0.2µdB
0.0µdB
-0.2µdB
-0.4µdB
-0.6µdB
-0.8µdB
-1.0µdB
20°
0°
-20°
-40°
-60°
-80°
-100°
-120°
-140°
-160°
-180°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

2.1

Forward Bias:



The Cut-in/Knee Voltage is measured to be approximately 445.47 mV.

To find the resistance,

The slope is measured to be 0.000835191. We know that in an I-V graph,

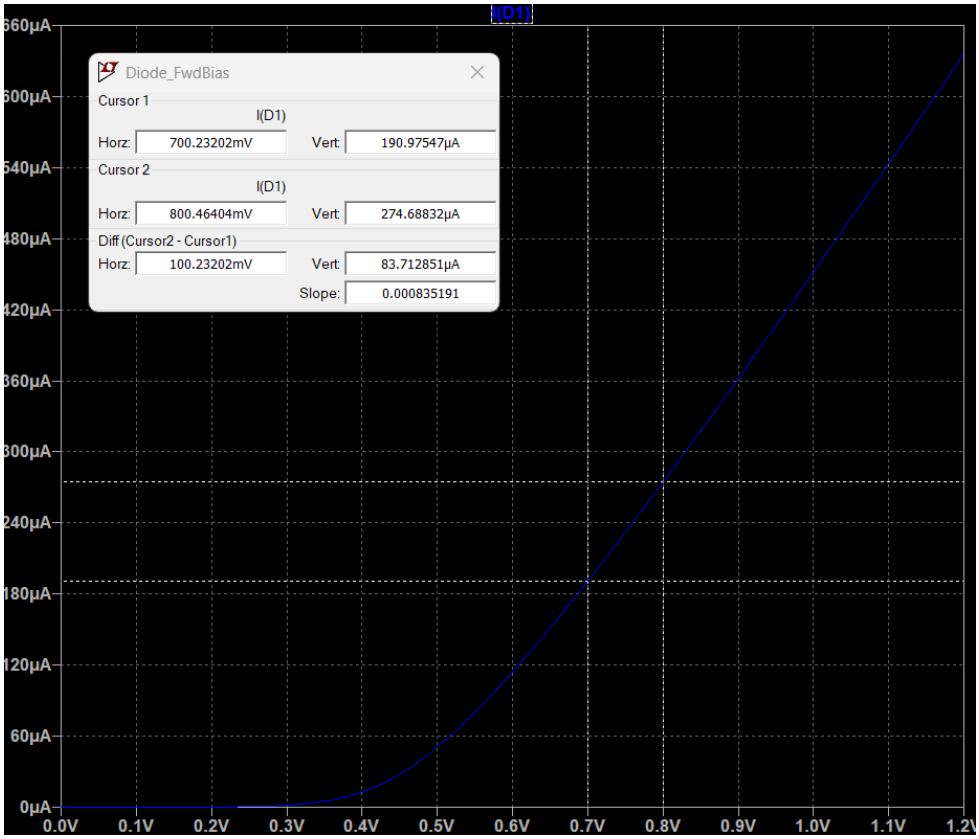
$$R = \frac{1}{Slope}$$

Therefore,

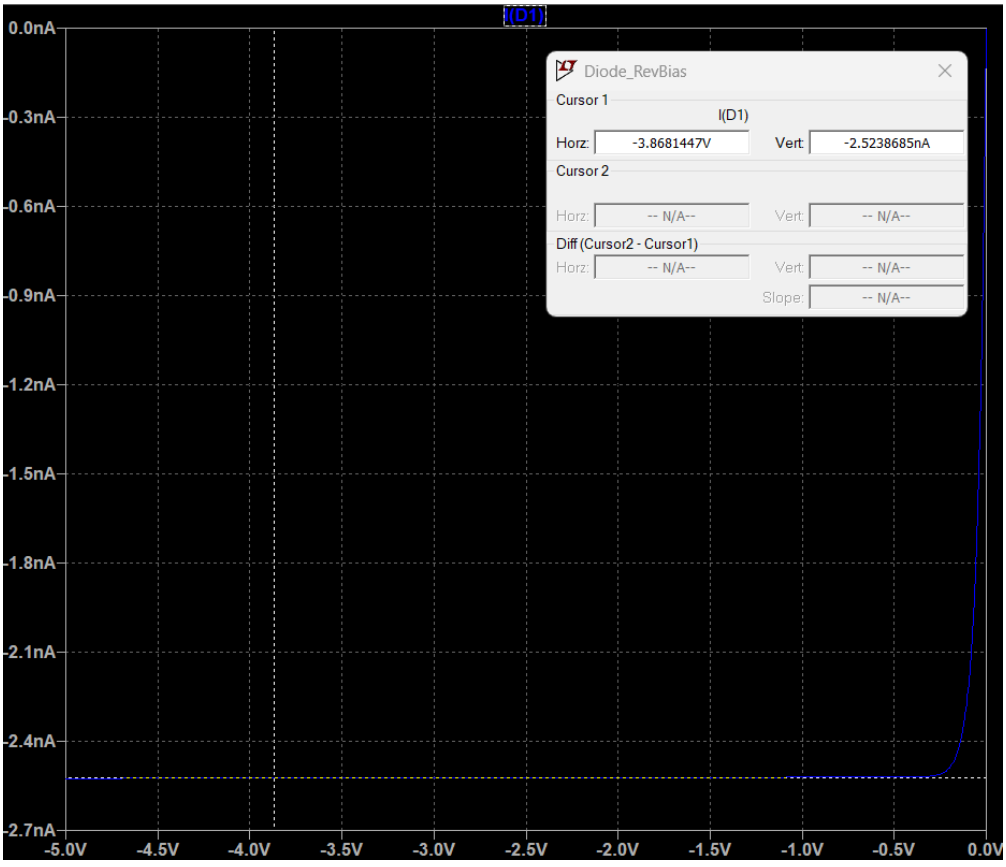
$$R = \frac{1}{0.000835191} = 1197.331\Omega$$

Since external resistance = 1000Ω,

$$R_{in} = 1197.331 - 1000 = 197.331\Omega$$



Reverse Bias:



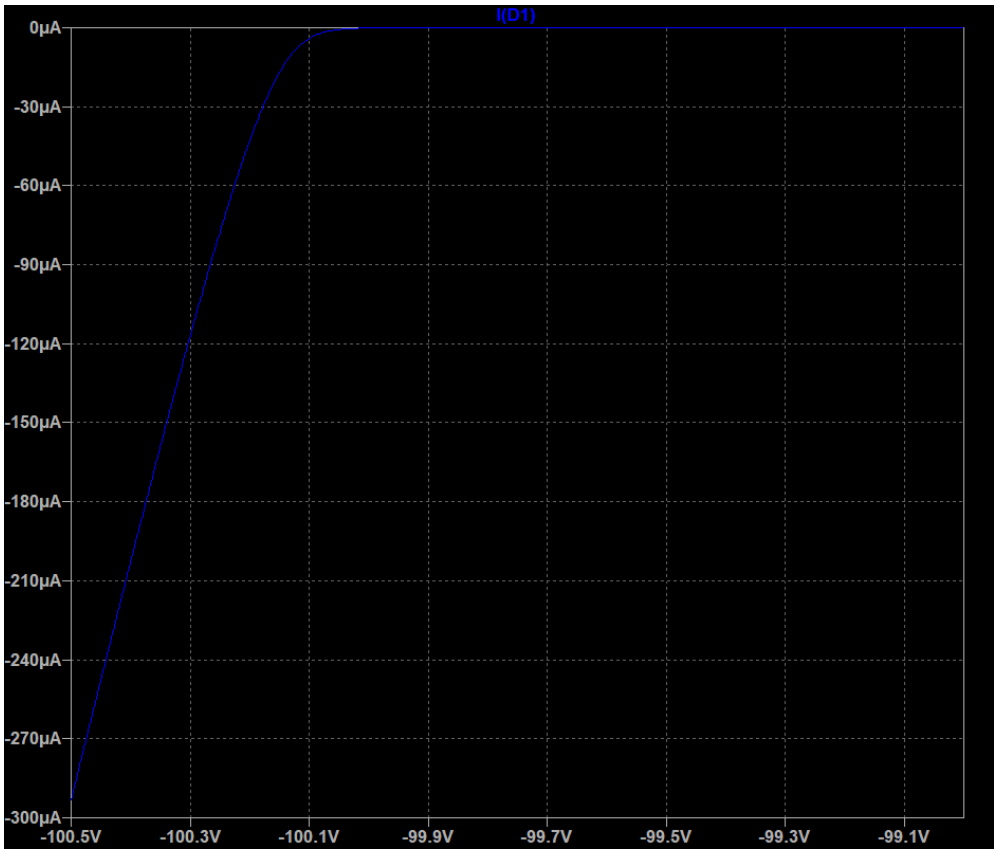
The saturation current is measured to be approximately 2.52386 nA.

Reverse Breakdown:

Since the default LTSpice 1N4148 does not allow breakdown, I have modified the parameters using the below directive,

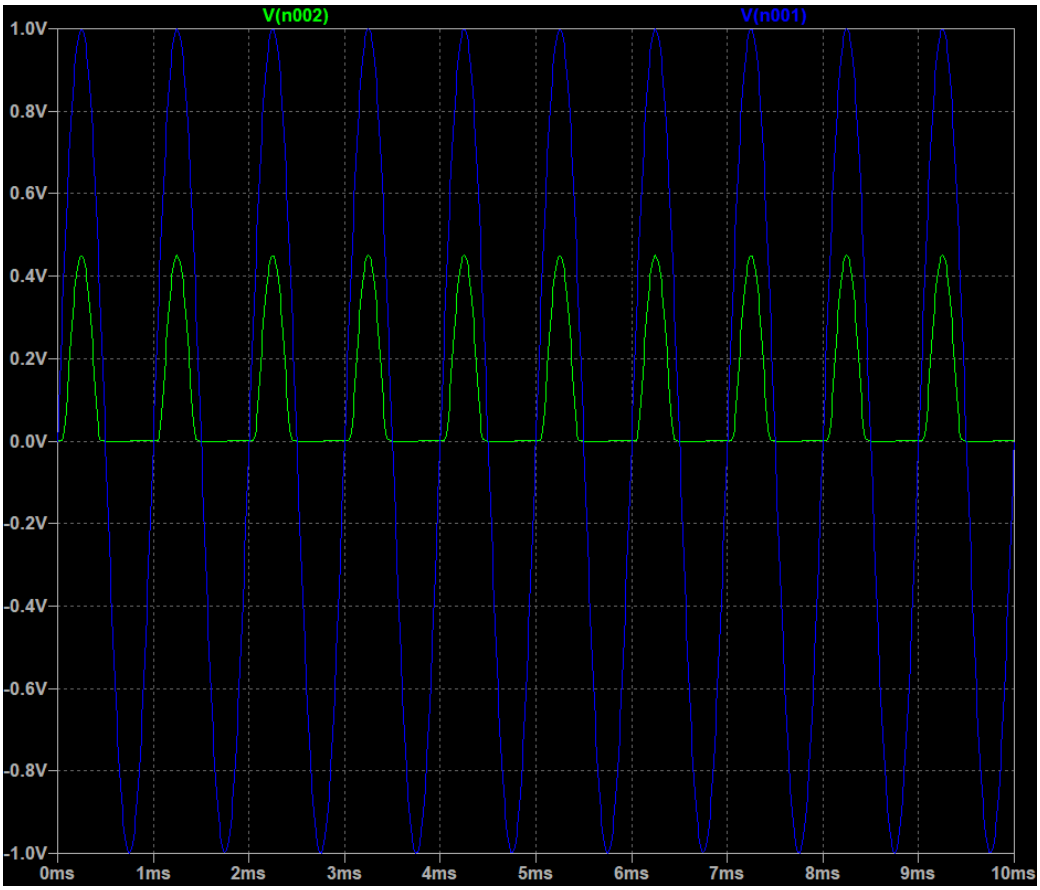
```
.model 1n4148_mod D(Is=2.52n Rs=0.568 N=1.752 Cjo=4p M=0.4 Iave=200m
Vpk=75 tt=20n BV=100 IBV=0.1u)
```

The breakdown voltage has been set to 100V as per the 1N4148 datasheet.



2.2

Voltage Plots Obtained:



V_{n001} – Input sinusoid, V_{n002} - Output sinusoid

The above plot expresses the working of a half wave rectifier.

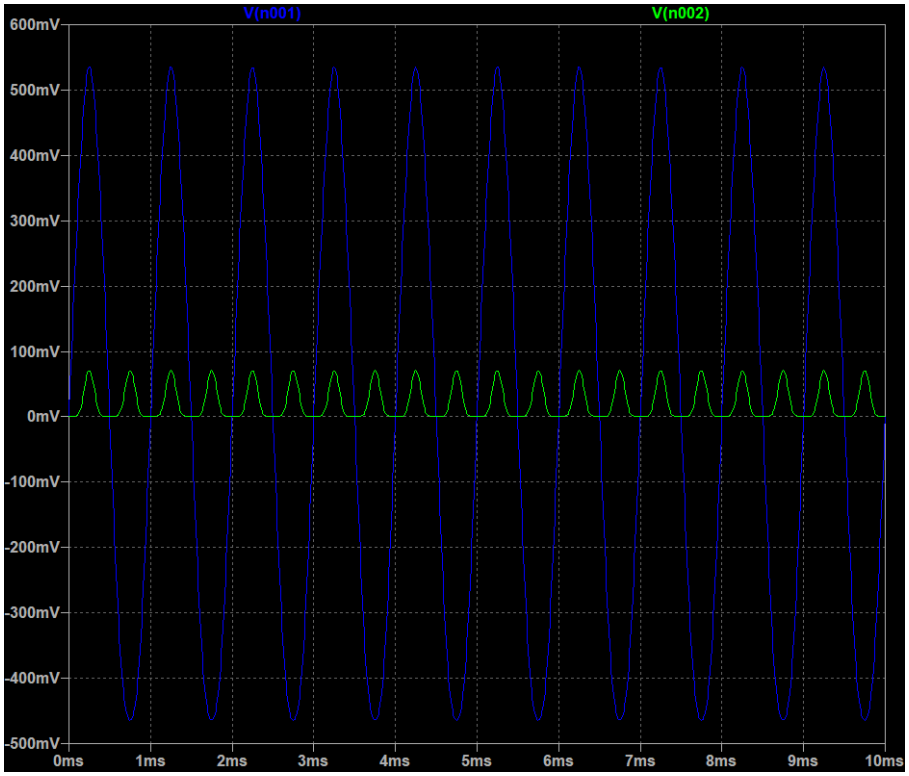
As we can clearly see, the circuit only allows the upper half of the input sinusoidal wave to pass through, due to the diode under reverse bias condition during the negative half of the sinusoid. This gives the circuit the name “half wave rectifier”.

There is also a significant reduction in the amplitude of the output sinusoid as compared to the input sinusoid. This is due to the cut-in voltage of the diode, which clips the sinusoids as below the cut-in voltage the diode does not conduct. In an ideal diode, this reduction in amplitude will be absent.

The output voltage is zero when the input sinusoid is in the negative half. This can be mitigated using filler circuits (ex: Capacitors in parallel). The filler circuits can also reduce the pulsating nature of the output.

2.3

Voltage Plots Obtained:



V_{n001} – Input sinusoid, V_{n002} - Output sinusoid

The above plot expresses the working of a full wave bridge rectifier.

The circuit rectifies both halves of the input sinusoid, creating a pulsating voltage. The pulsating nature can be reduced by using filler circuits.

There is also a significant reduction in the amplitude of the output sinusoid as compared to the input sinusoid. This is due to the cut-in voltage of the 2 diodes the current passes through during each half, which clips the sinusoids as below the cut-in voltage, the diode does not conduct. In ideal diodes, this reduction in amplitude will be absent.

3.1

Any carrier that is injected into a semiconductor can either drift, diffuse or recombine.

- If a carrier either drifts or diffuses, it must leave the point of injection. Therefore, KCL will hold for those carriers.
- If a carrier recombines with a carrier of the opposite polarity, it still represents a movement of charge, as that opposite carrier has to come in from the opposite direction, which constitutes a current in the same direction as that of the injection.

Therefore, KCL still holds during localized injection of carriers.