Analog Electronic Circuits (EC2.103) : Assignment-3

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Instructions:

1. Submit your assignment as a single pdf (Name RollNo.pdf) at moodle on or before the due date
2. Hand-written/typed (notion/latex/word) submissions are allowed
3. Report should be self explanatory and must carry complete solution - Answers with schematics, SPICE directives, annotated waveforms, inference/discussion on results as asked in the questions.
4. Use the TSMC_180nm.txt file for the MOSFET models.
5. Post your queries on moodle. Discussions are highly encouraged on moodle
6. Any form of copying/cheating will result in immediate F grade

1. Region of Operation

(1.1) List the different regions of operation for NMOS and PMOS transistors. For each region, specify the conditions on terminal voltages that define the region. Additionally, provide the corresponding drain current equations in each region.

(1.2) For the following configurations in Fig.1, find out the operating region, the current flowing through the MOSFET and justify your answer with proper equations. (You can take $\mu_n C_{OX} = 300\mu A/V^2$ and the aspect ratio of the MOSFET to be $\frac{2\mu}{1\mu}$) :

(1.3) Answer the following questions referring to Fig.2.

(a) Show that for the PMOS to operate in saturation region,

$$I \times R \leq |V_{thp}|$$

(b) If the transistor is specified to have $|V_{thp}| = 1V$ and $K_p = 0.2mA/V^2$ and for $I_d = 0.1mA$, find the voltages V_{SD} and V_{SG} for the following values of resistance : (i) 0Ω (ii) $10k\Omega$ (iii) $100k\Omega$

(1.4) For the circuit in FIg.3, find the following

(a) Region of Operation
(b) Biasing current and transconductance
(c) Range and limit of gate voltage for the MOSFET to remain in saturation

(Consider $\mu_n C_{OX} = 100\mu A/V^2$, $V_{thn} = 0.5V$ and $\frac{W}{L} = \frac{1.8\mu}{0.18\mu}$)

2. Small Signal Model and Impedances

(2.1) Draw the complete small signal model of NMOS and PMOS(include the capacitances as well).

(2.2) For the configurations of MOSFET shown in FIg.4, find the impedance as asked (assume that the MOSFETs are in saturation in all the scenarios):

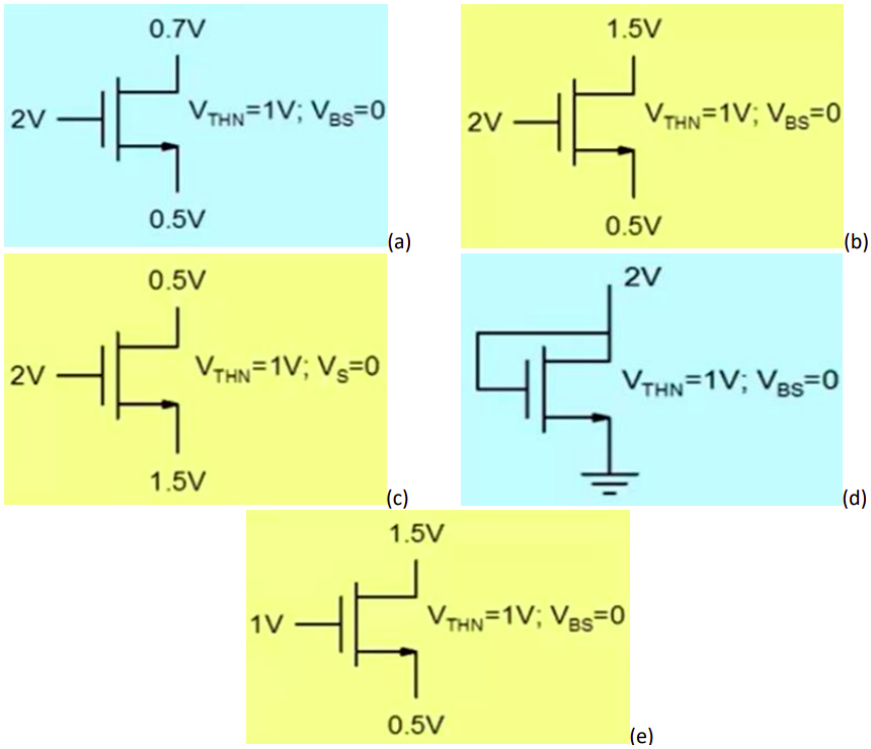

Figure 1: Figure related to 1.2

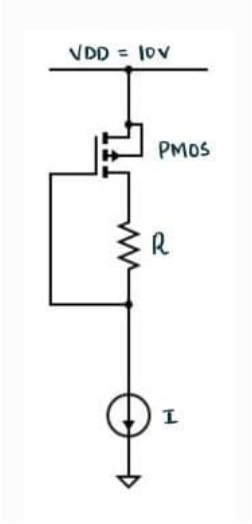

Figure 2: Figure related to 1.3

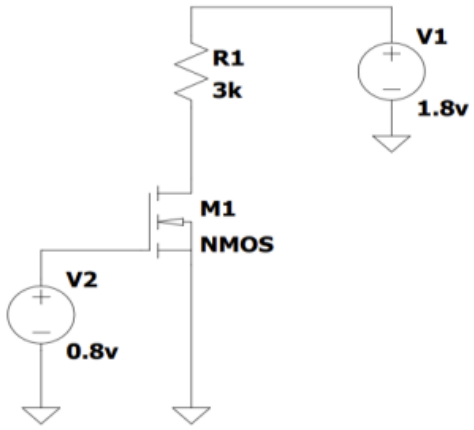

Figure 3: Figure related to 1.4

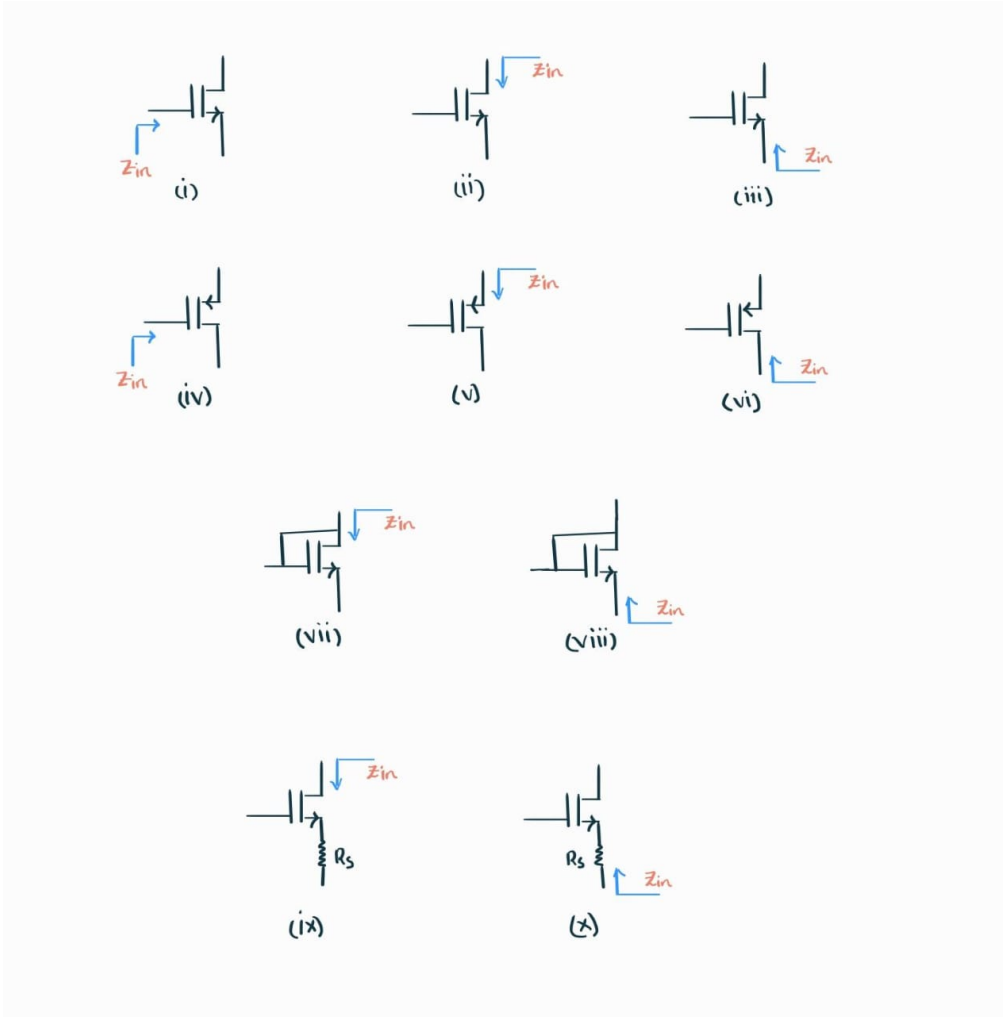

Figure 4: Figure related to 2.2

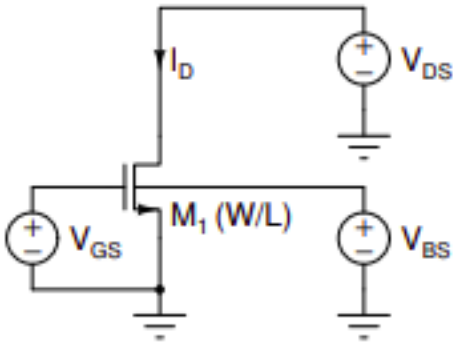

Figure 5: Figure related to 3.1

3. LTSpice Simulations : MOSFET Characterization

(3.1) As shown in Fig.5, plot I_D vs V_{GS} for an NMOS transistor having $\frac{W}{L} = \frac{1.8\mu}{0.18\mu}$ by sweeping V_{DS} from 0 to 1.8V with a step of 0.01V and sweeping V_{GS} from 0 to 1.8V with a step of 0.3V. Assume $V_{BS} = 0V$.

(**Hint**: *Use NMOS4 from library, edit and change model name to CMOSN, enter W,L,drain/source area (AD/AS), drain/source perimeter (PD/PS) as follows: AS = {5*width_N*LAMBDA}, PS = {10*LAMBDA + 2*wdith_N }, AD = {5*width_N*LAMBDA } and PD = {10*LAMBDA + 2*wdith_N } where wdith_N = W and {2*LAMBDA } = L. Use ".include TSMC_180nm.txt" in the spice directive.*)

(3.2) Plot I_D vs V_{GS} for $\frac{1.8\mu}{0.18\mu}$ NMOS transistor for $V_{DS} = 50mV$ and $V_{BS} = 0V$.

(a) Estimate the technology parameter $\mu_n C_{OX}$ and threshold voltage V_{th} from the graph for $V_{DS} = 50mV$

(b) Plot I_D vs V_{GS} for $V_{DS} = 1.8V$ and extract the threshold voltage. Compare the obtained V_{th} with $V_{DS} = 50mV$ case. Do you observe any difference in the values obtained in the two cases? If yes, explain why. (*Hint : DIBL*).

(3.3) From the simple MOS models discussed, find out V_{th} for NMOS and PMOS devices ($\frac{W}{L} = \frac{1.8\mu}{0.18\mu}$ with the help of I_D vs V_{GS} simulations for

(a) Body to source voltage, $V_{BS} = 0V$

(b) Body to source voltage, $V_{BS} = 900mV$

(c) Body to source voltage, $V_{BS} = -900mV$

Overlay the three plots . Do you observe any difference in V_{th} for the three cases? Briefly discuss.

(**Hint** : *I_D vs V_{GS} simulation with V_{BS} list , body effect. For PMOS based simulations, use PMOS4 component and use model name: CMOSP, define AS/AD/PS/PD as mentioned earlier.*)