Analog Electronic Circuits – Lab 9

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1 VTC of Op-Amp in Negative and Positive Feedback Configurations

1.1 Objective

To plot the Voltage Transfer Characteristics of the given Op-Amp in Positive and Negative feedback loop configurations

1.2 Circuit Diagram

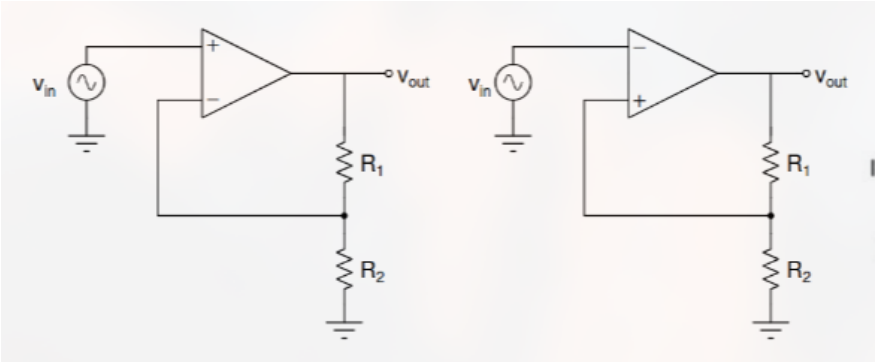

Figure 1.2.1: Op-Amp in Negative Feedback(left) and Positive Feedback(right)

1.3 Common Parameters Used

- $V_{DD} = 12V$
- $V_{SS} = -12V$
- $R_1 = R_2 = 10k\Omega$
- $v_{in} = 12V\ peak\ to\ peak,\ 100Hz\ frequency$

1.4 LTSpice Simulations

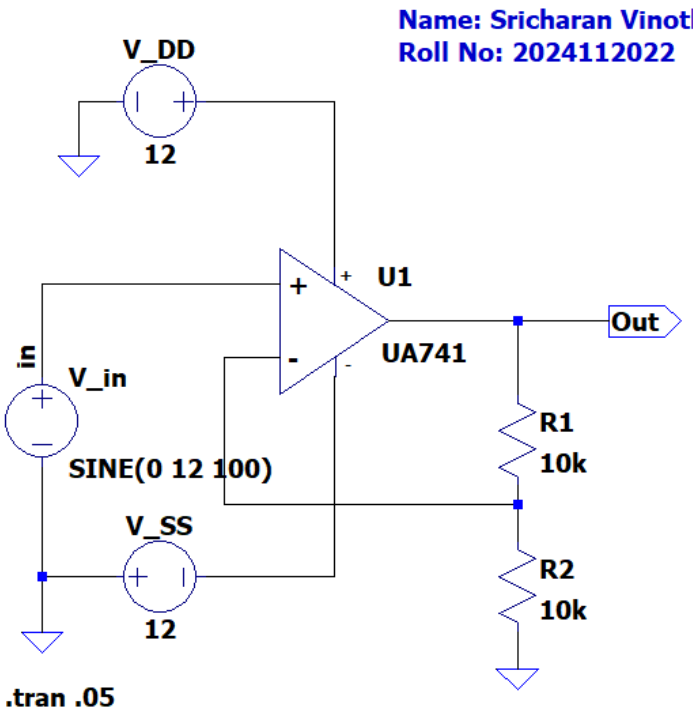

Figure 1.4.1: LTSpice Schematic of Op-Amp in Negative Feedback

VTC in Negative Feedback:

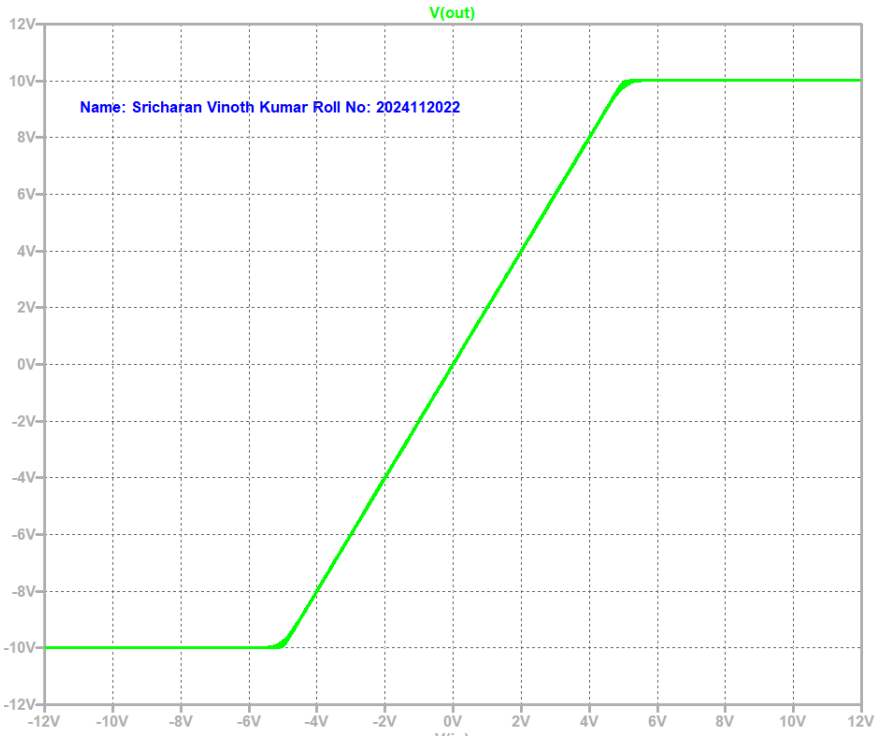

Figure 1.4.2: Negative Feedback VTC

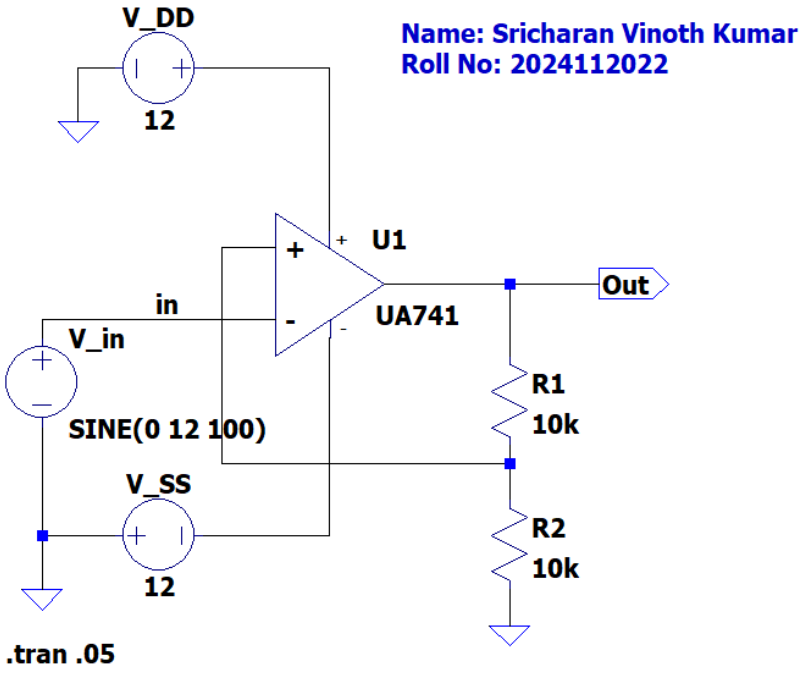

Figure 1.4.3: LTSpice Schematic of Op-Amp in Positive Feedback

VTC in Positive Feedback:

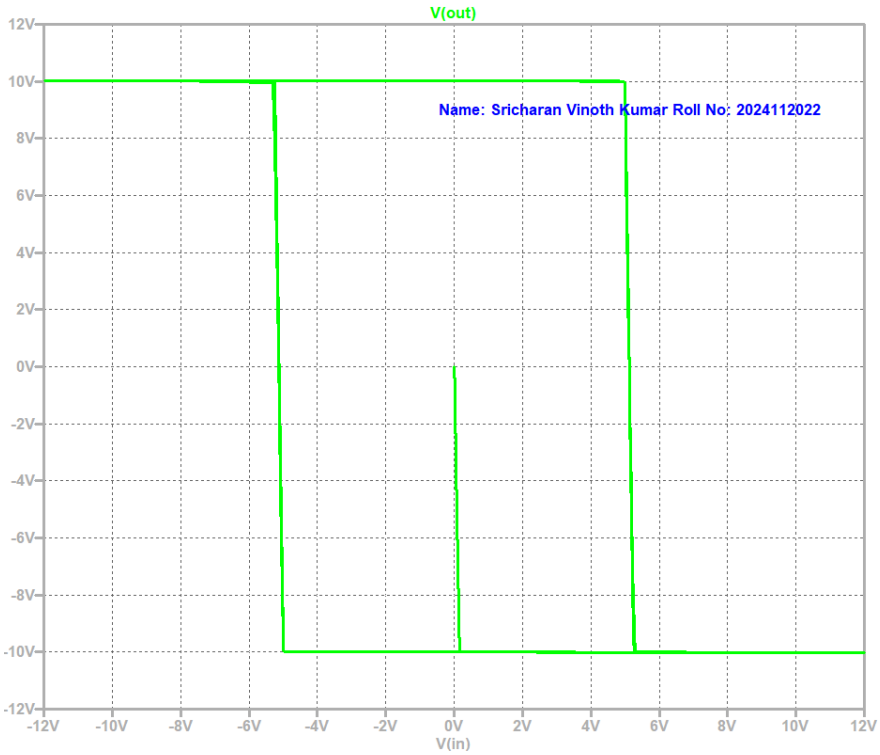

Figure 1.4.4: Positive Feedback VTC

1.5 Observations

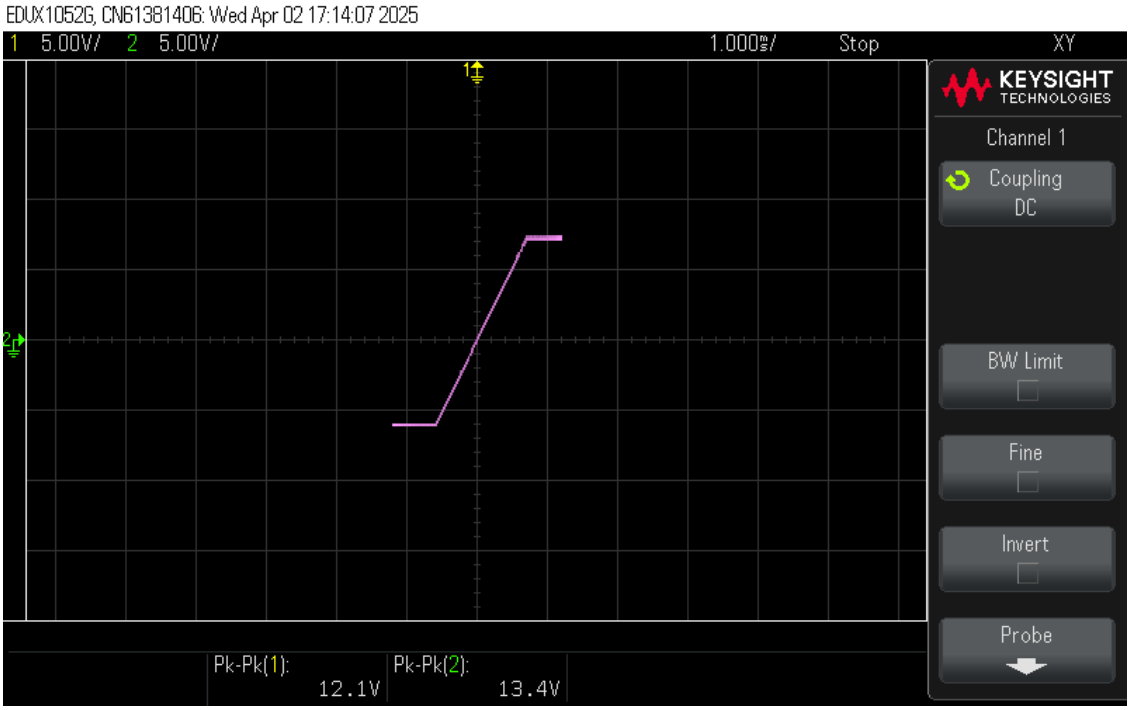

Figure 1.5.1: DSO Plot of VTC in Negative feedback configuration

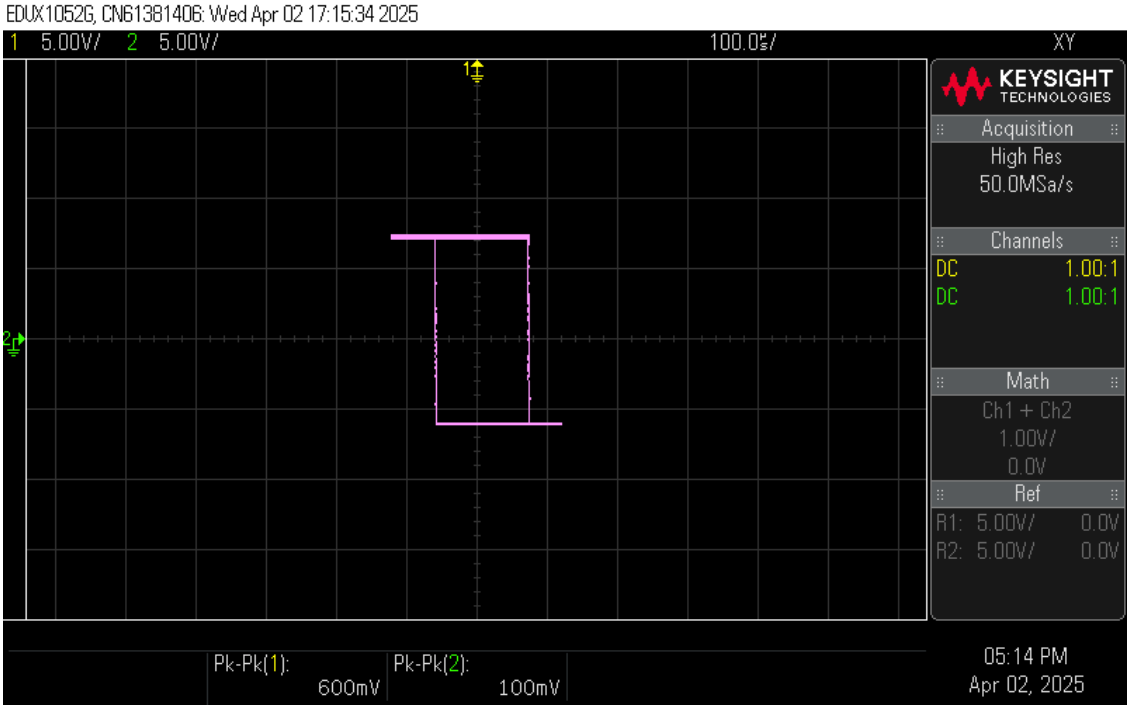

Figure 1.5.2: DSO Plot of VTC in Positive feedback configuration

1.6 Inference

We see significant hysterisis in the Positive feedback configuration.
This can be attributed to the fact that the output Voltage sticks to VDD during the rising half of the input sinusoid and V_{SS} during the falling half of the sinusoid, regardless of the magnitude of the sinusoid at that instant, creating a "memory" or a "retention" effect, causing hysterisis.

2 RC Oscillator

2.1 Objective

To construct and analyse the working of a Op-Amp based RC Oscillator.

2.2 Circuit Diagram

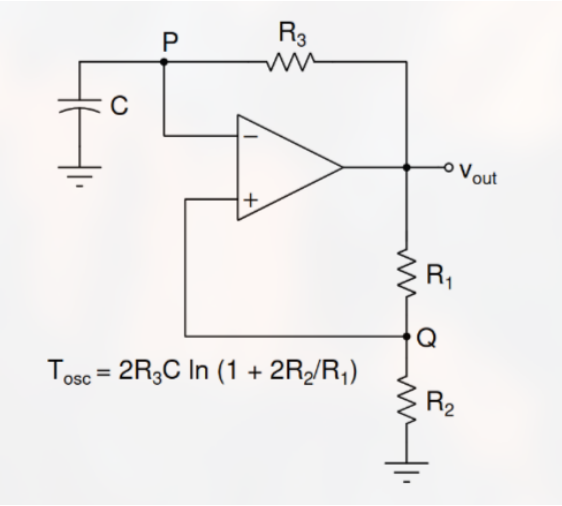

Figure 2.2.1: Circuit Diagram of Op-Amp based RC Oscillator

2.3 Derivation of Frequency of Oscillation

2.3.1 Operating Principle

This circuit operates as a relaxation oscillator where the capacitor C charges and discharges between two threshold voltages. The op-amp output switches between positive and negative saturation voltages ($+V_{sat} = V_{DD}$ and $-V_{sat} = V_{SS}$), causing the capacitor to repeatedly charge and discharge through R_3.

2.3.2 Threshold Voltages

Due to the voltage divider at the inverting input:

$$V_{TH} = +V_{sat}\frac{R_2}{R_1 + R_2}$$
$$V_{TL} = -V_{sat}\frac{R_2}{R_1 + R_2}$$

Where V_{TH} and V_{TL} are the upper and lower threshold voltages, respectively.

2.3.3 First Half-Cycle (Output at $+V_{sat}$)

When the output is at $+V_{sat}$, the capacitor charges according to:

$$V_P(t) = V_{sat} + (V_{TL} - V_{sat})e^{-t/R_3C}$$

The op-amp output switches when V_P falls to the lower threshold:

$$V_{TL} = V_{sat} + (V_{TL} - V_{sat})e^{-t_1/R_3C}$$

Substituting $V_{TL} = -V_{sat} \times \frac{R_2}{R_1+R_2}$:

$$-V_{sat} \times \frac{R_2}{R_1+R_2} = V_{sat} + \left(-V_{sat} \times \frac{R_2}{R_1+R_2} - V_{sat}\right) e^{-t_1/R_3C}$$

Rearranging:

$$V_{sat}\left(-\frac{R_2}{R_1+R_2} - 1\right) = \left(-V_{sat} \times \frac{R_2}{R_1+R_2} - V_{sat}\right) e^{-t_1/R_3C}$$
$$V_{sat}\left(-\frac{R_2}{R_1+R_2} - 1\right) = -V_{sat}\left(1 + \frac{R_2}{R_1+R_2}\right) e^{-t_1/R_3C}$$
$$\frac{R_2}{R_1+R_2} + 1 = \left(1 + \frac{R_2}{R_1+R_2}\right) e^{-t_1/R_3C}$$
$$\frac{R_1+2R_2}{R_1+R_2} = \frac{R_1+2R_2}{R_1+R_2} e^{-t_1/R_3C}$$

Therefore:

$$1 = e^{-t_1/R_3C}$$
$$-\frac{t_1}{R_3C} = \ln\left(\frac{R_1}{R_1+2R_2}\right)$$
$$t_1 = R_3C \ln\left(\frac{R_1+2R_2}{R_1}\right)$$

2.3.4 Second Half-Cycle (Output at $-V_{sat}$)

Similarly, when the output is at $-V_{sat}$, the capacitor voltage follows:

$$V_P(t) = -V_{sat} + (V_{TH} - (-V_{sat}))e^{-t/R_3C}$$

The op-amp output switches when V_P rises to the upper threshold:

$$V_{TH} = -V_{sat} + (V_{TH} - (-V_{sat}))e^{-t_2/R_3C}$$

Following similar algebraic steps as before:

$$t_2 = R_3C \ln\left(\frac{R_1+2R_2}{R_1}\right)$$

2.3.5 Total Period of Oscillation

The total period is the sum of both half-cycles:

$$T_{osc} = t_1 + t_2$$
$$= 2R_3C \ln\left(\frac{R_1+2R_2}{R_1}\right)$$

This can be rewritten as:

$$T_{osc} = 2R_3C \ln\left(1 + \frac{2R_2}{R_1}\right) \tag{2.3.1}$$

2.4 LTSpice Simulation

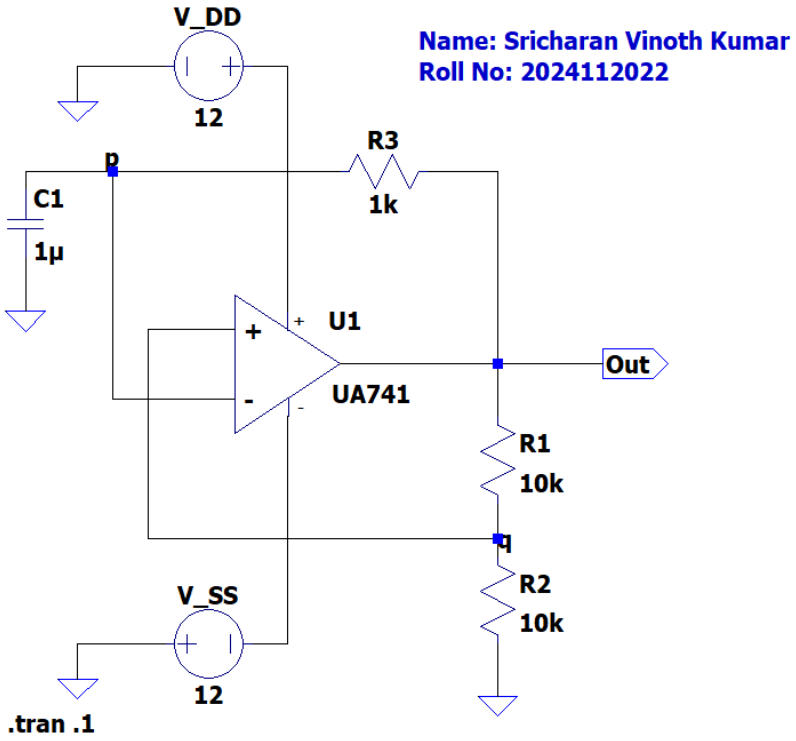

Figure 2.4.1: LTSpice Schematic of Op-Amp based RC Oscillator

To calculate the theoretical value of f_{osc}, we can use Equation 2.3.1,

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{2R_3C \cdot \ln\left(1 + \frac{2R_2}{R_1}\right)} \tag{2.4.1}$$

$$= \frac{1}{2 \times 1000 \times 10^{-6} \times \ln(1 + 2(10000/10000))}$$

$$= \frac{1}{2 \times 10^{-3} \times \ln(3)}$$

$$= 455.911693Hz$$

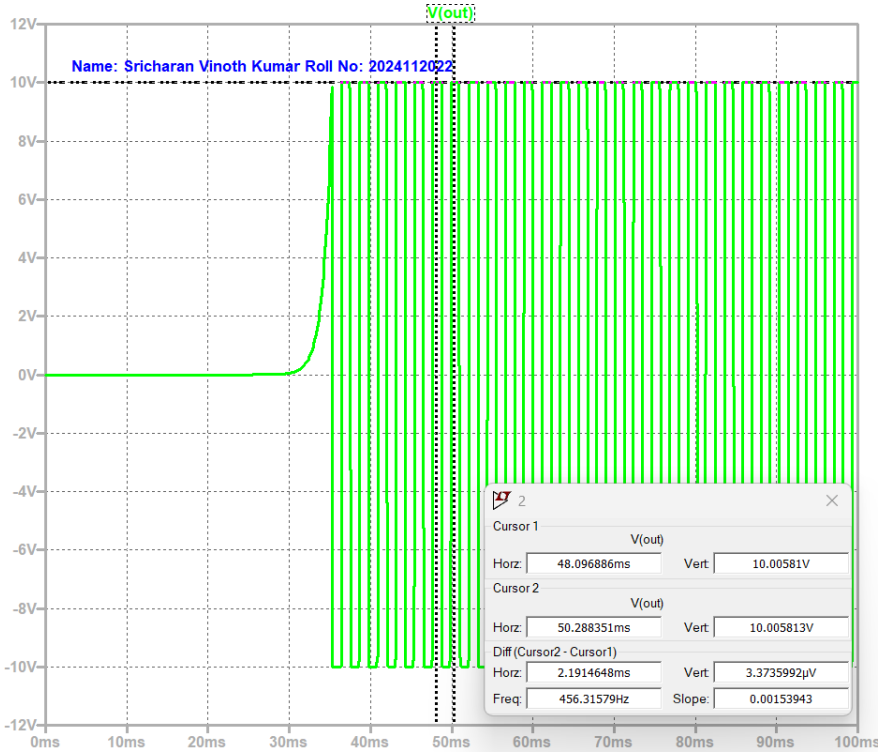

Figure 2.4.2: Plot of v_{out}

$\therefore$ Observed frequency = 456.31579Hz. This matches closely with the theoretical frequency.

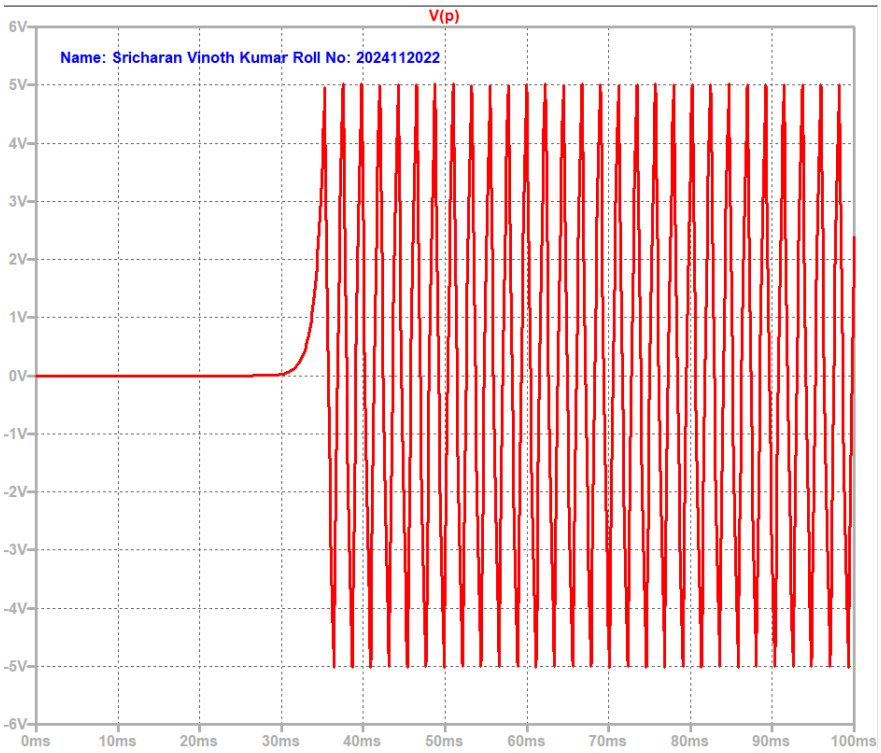

Figure 2.4.3: Plot of v_p

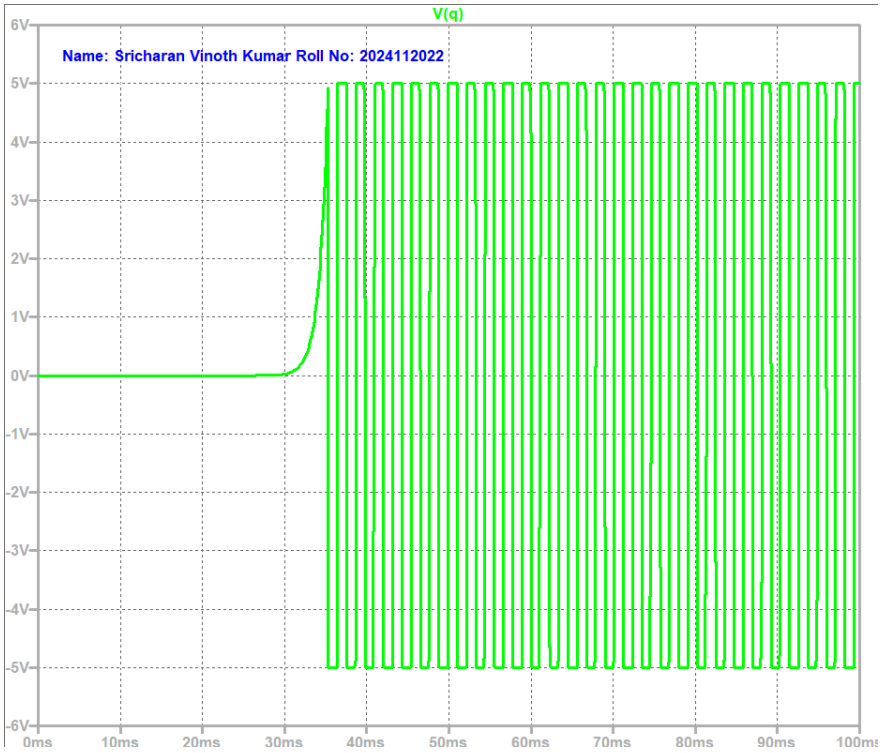

Figure 2.4.4: Plot of v_q

2.5 Observation

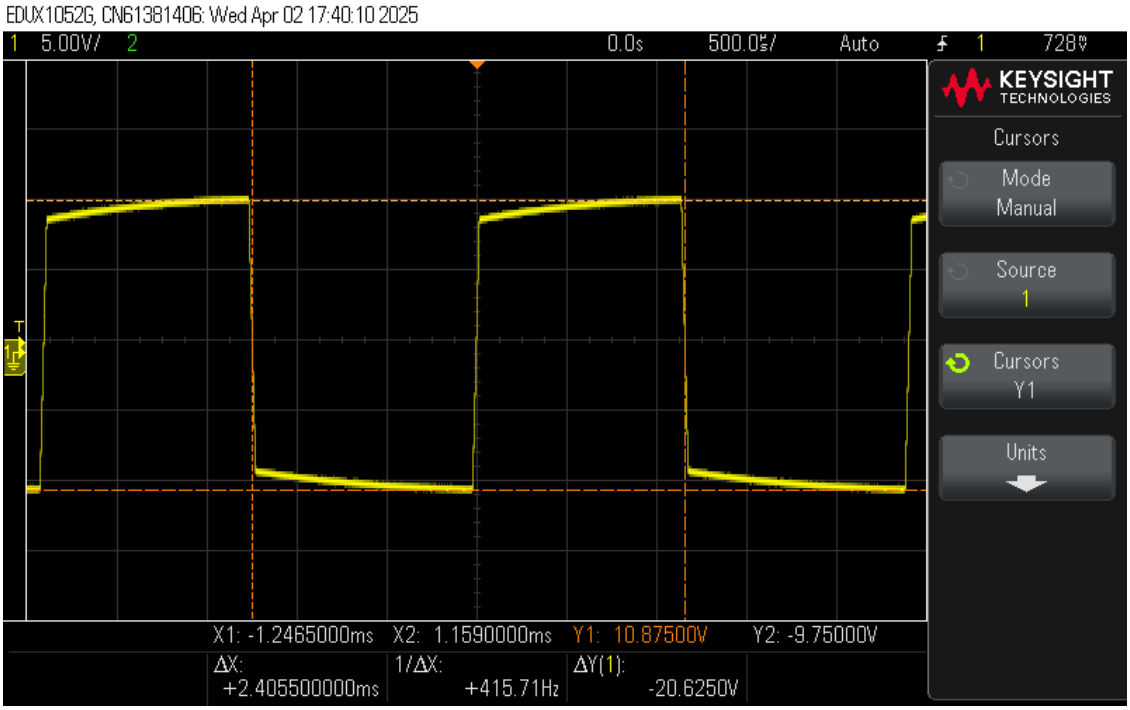

Figure 2.5.1: Plot of v_{out}

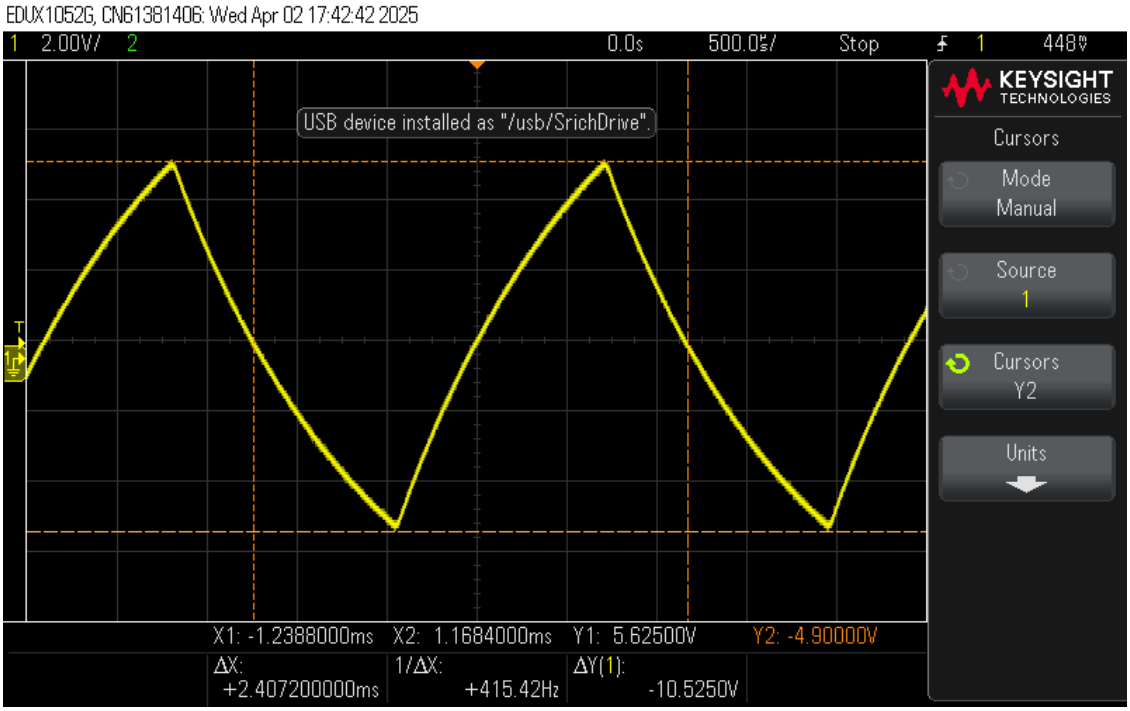

Figure 2.5.2: Plot of v_p

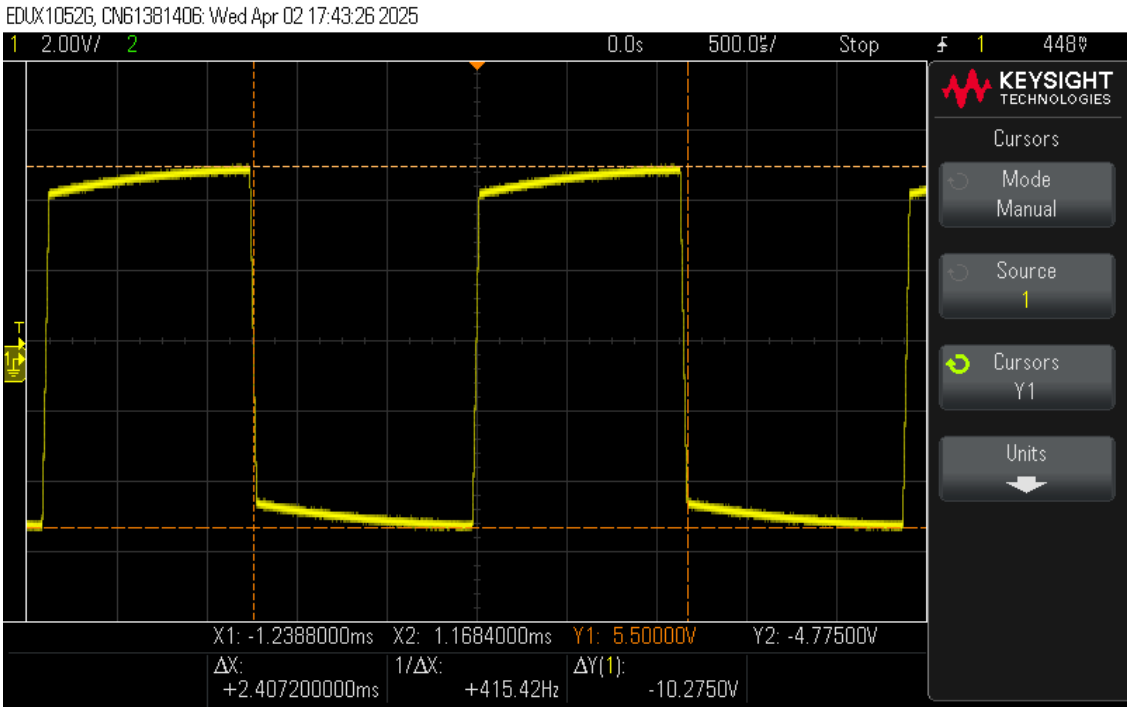

Figure 2.5.3: Plot of v_q

Observed frequency (measured using DSO) = 415.89 Hz (Matches closely with the theoretical frequency obtained in the LTSpice Simulations)
Peak to peak $v_{out} = 20.625V$
Peak to peak $v_p = 10.525V$
Peak to peak $v_q = 10.275V$

3 Integrator (-ve feedback example)

3.1 Objective

To build an Op-Amp based Integrator and observe its working.

3.2 Circuit Diagram

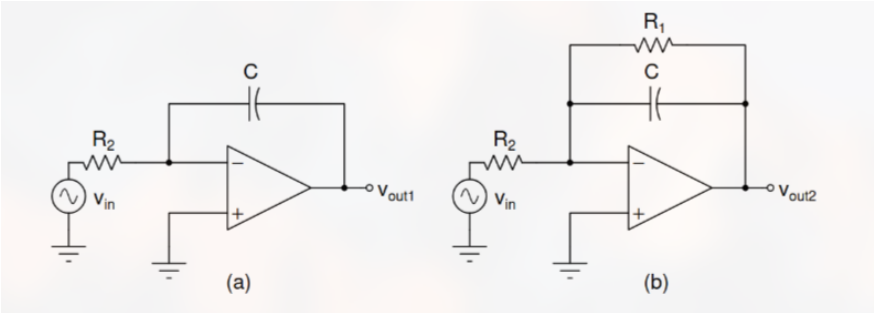

Figure 3.2.1: Op Amp based Integrator

3.3 LTSpice Simulation

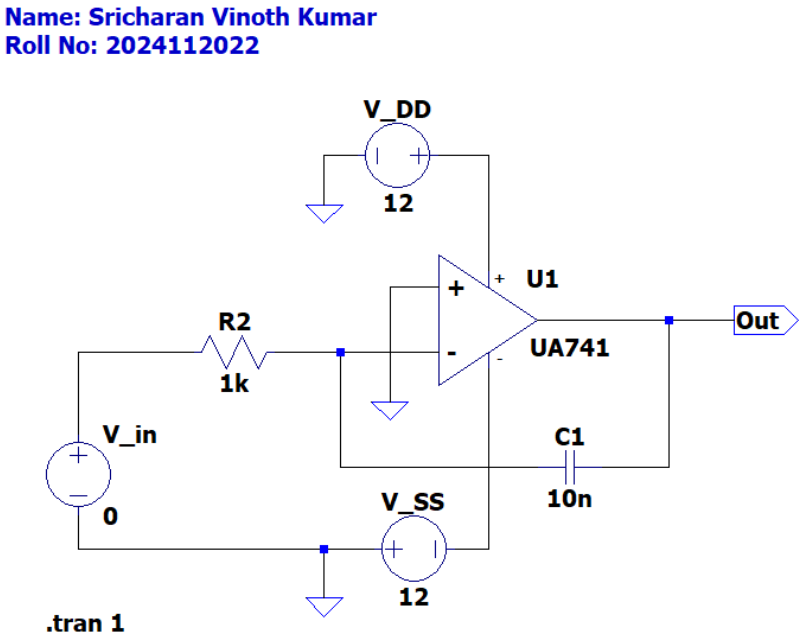

Figure 3.3.1: LTSpice Schematic of Circuit (a)

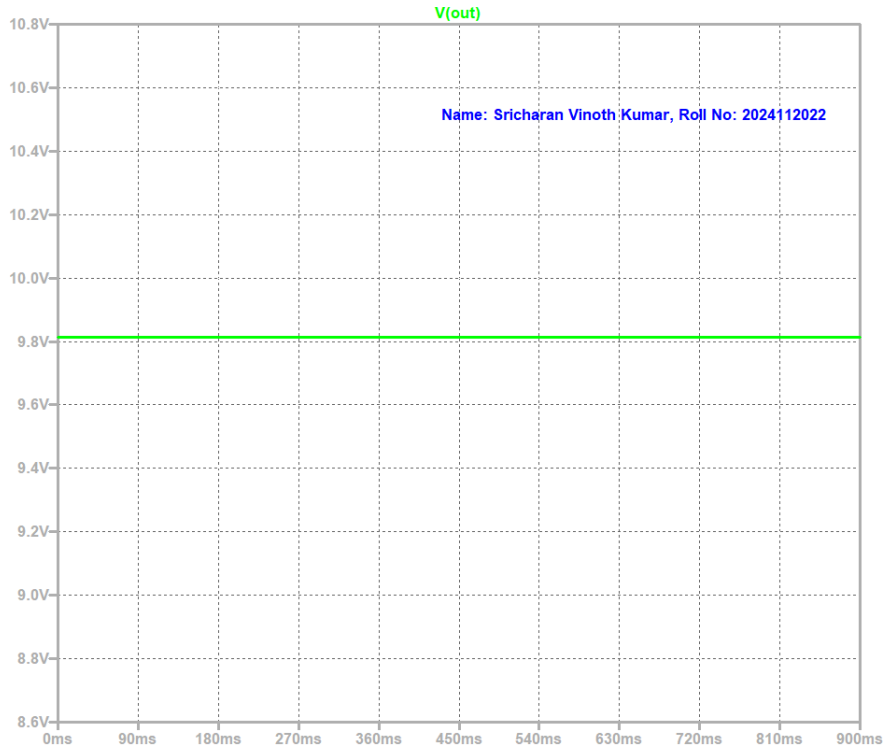

Figure 3.3.2: DC Voltage Saturation for Circuit (a) ($\approx 9.8V$)

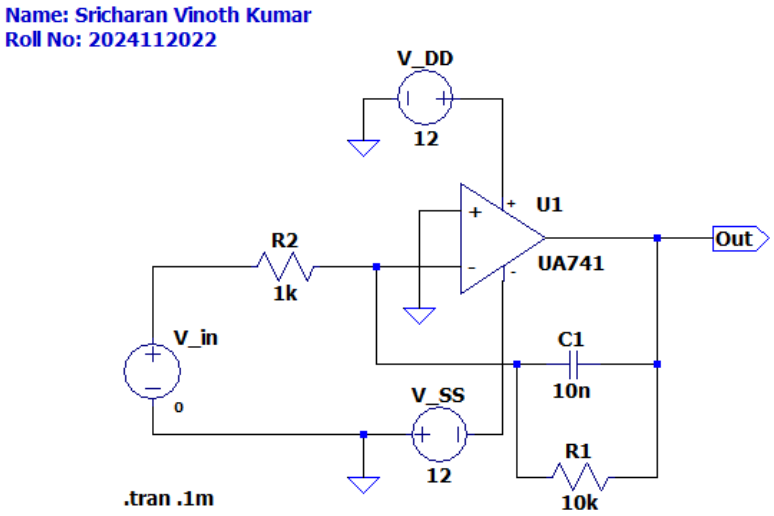

Figure 3.3.3: LTSpice Schematic of Circuit (b)

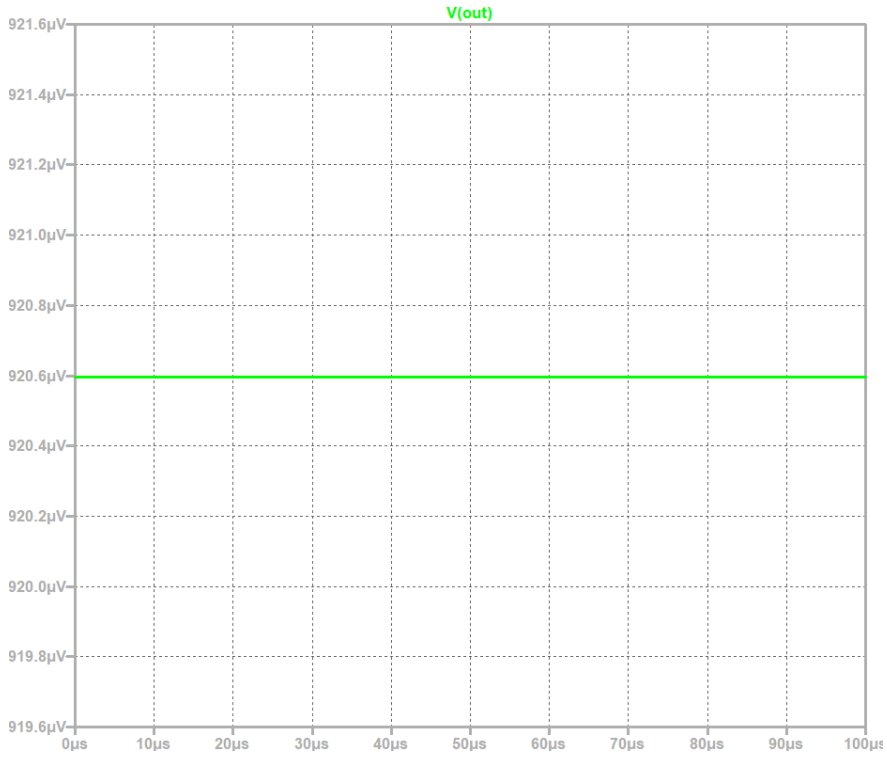

Figure 3.3.4: DC Voltage Saturation for Circuit (b) (is negligible)

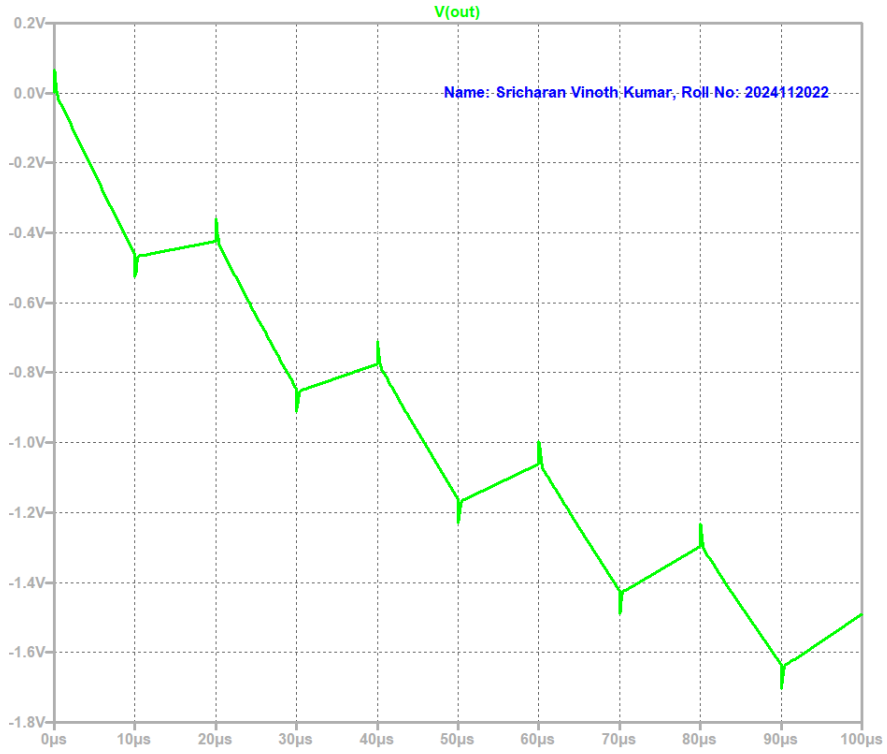

Figure 3.3.5: Integration Action with v_{in} as a pulse signal

3.4 Observation

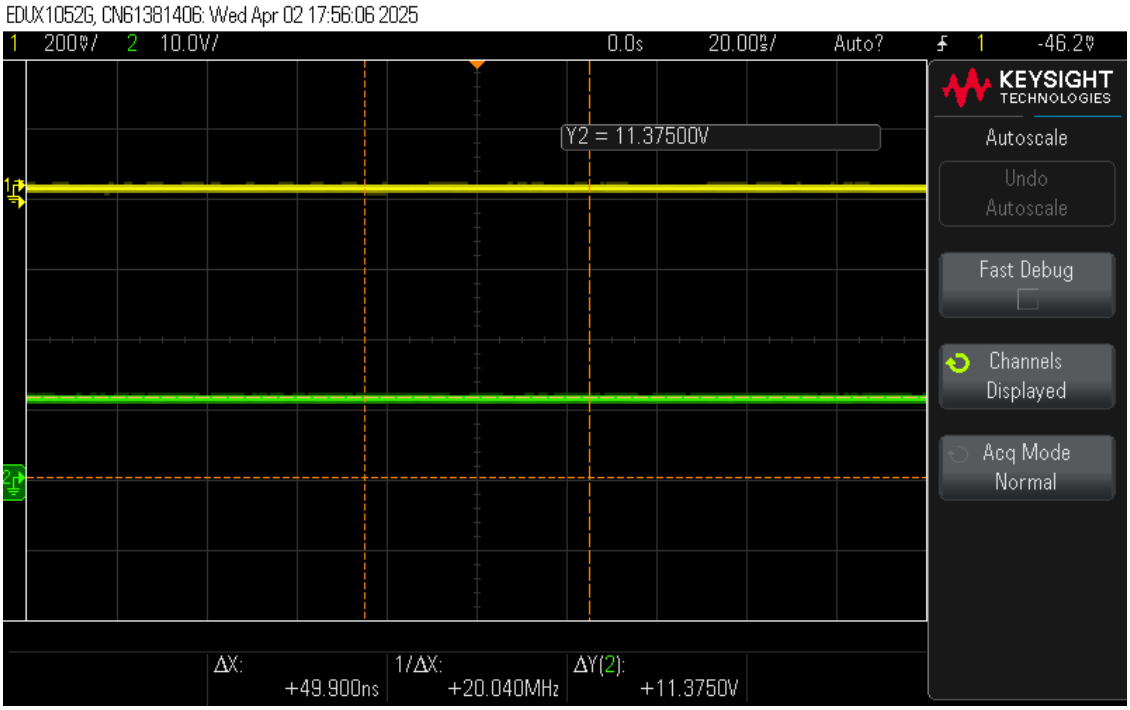

Figure 3.4.1: DC Voltage Saturation for Circuit (a) ($\approx 11.375V$)

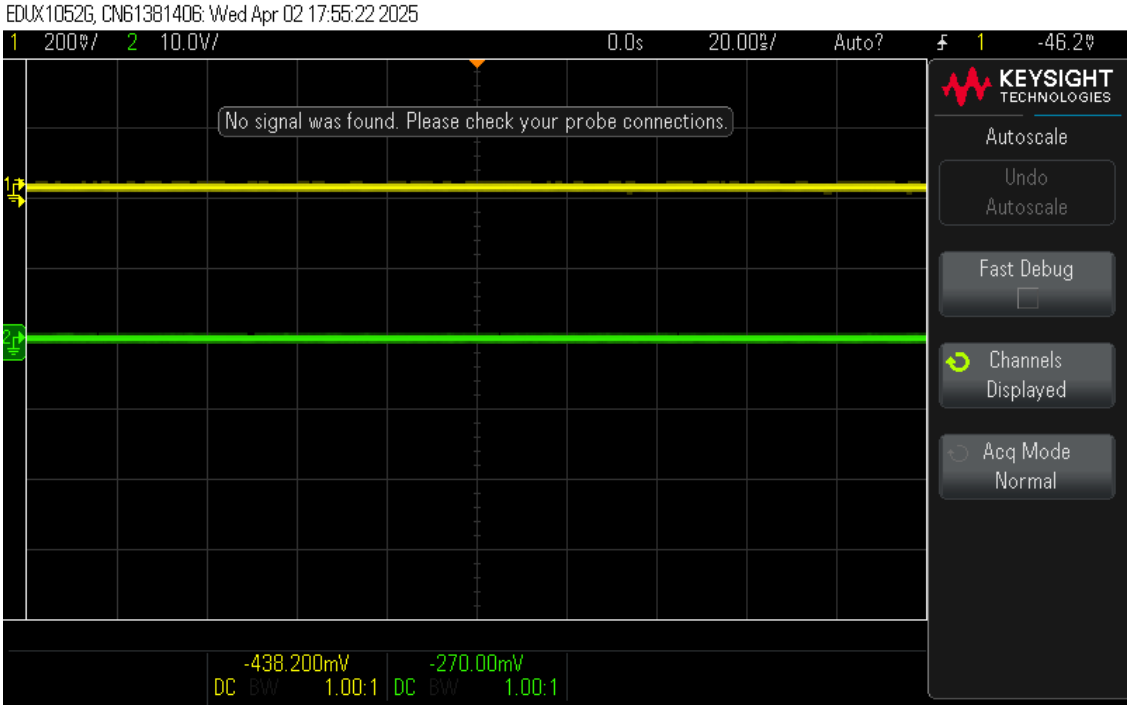

Figure 3.4.2: DC Voltage Saturation for Circuit (b) (is unobservable due to very low magnitude)

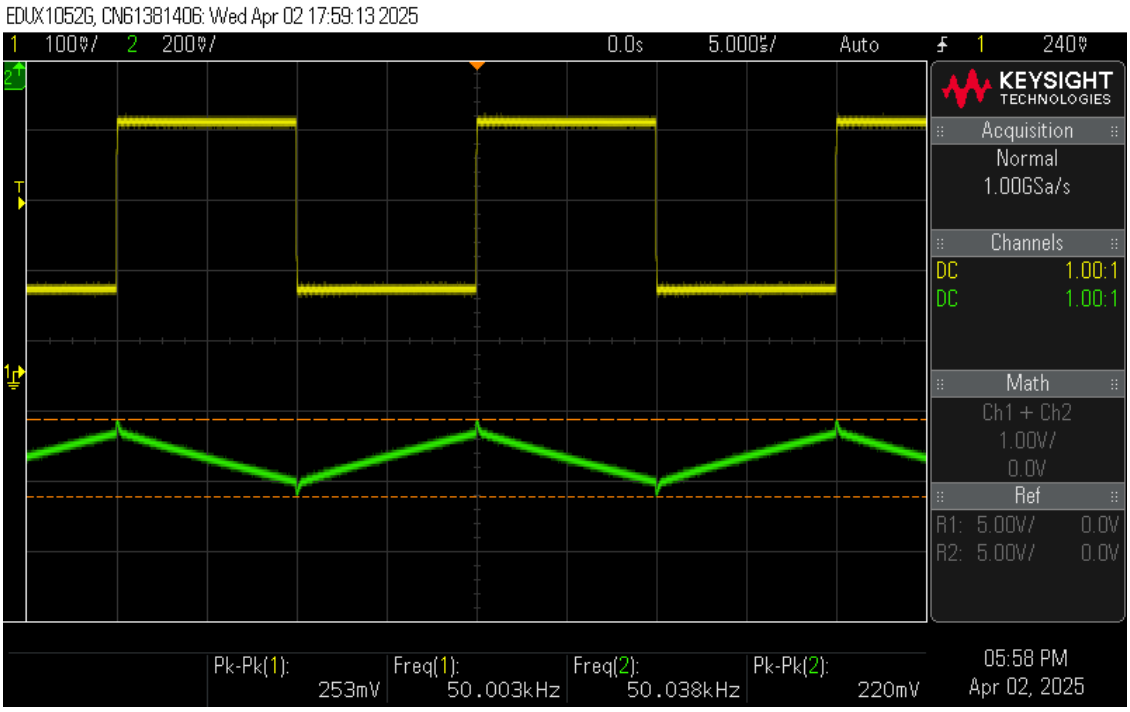

Figure 3.4.3: Integration Action with v_{in} as a pulse signal

3.5 Inference

In the DSO plot of Voltage Saturation for Circuit (b), we see no signal at the probes, due to the very low Saturation Voltage.
The presence of R_1 in Circuit (b) allows DC Current to pass across the Op-Amp. Also, since we know that,

$$gain = 1 + \frac{R_1}{R_2}$$

So, the presence of R_1 gives it finite gain, unlike in Circuit (a), where the gain is very large. Therefore the DC Offset in (a) is greatly amplified, whereas in (b) the amplified Voltage is still negligible due to finite gain.
In (b), we observe Integration action, since we see a linear growth and fall, which matches with the integration of a Square Wave.

4 Precision Half Wave Rectifier

4.1 Objective

To build a precise half wave Rectifier using an Op-Amp and a diode.

4.2 Circuit Diagram

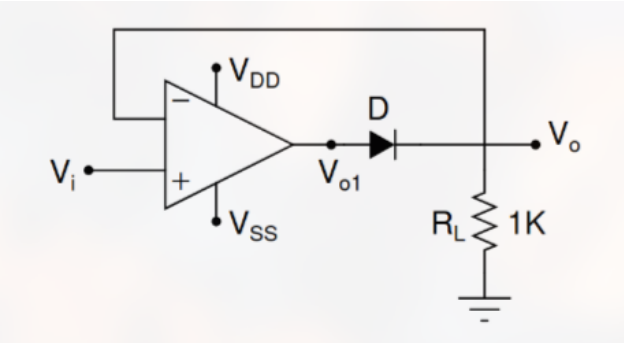

Figure 4.2.1: Circuit Diagram of Precision Half Wave Rectifier

4.3 LTSpice Simulations

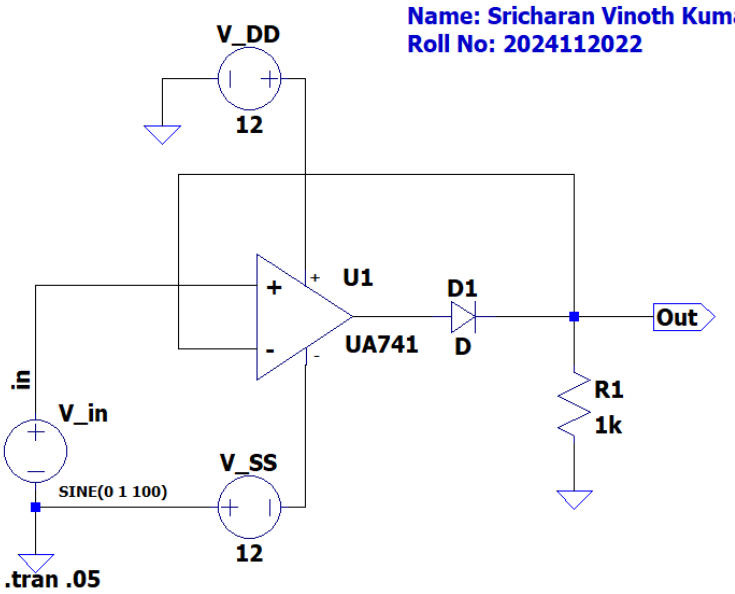

Figure 4.3.1: LTSpice of Precision Half Wave Rectifier

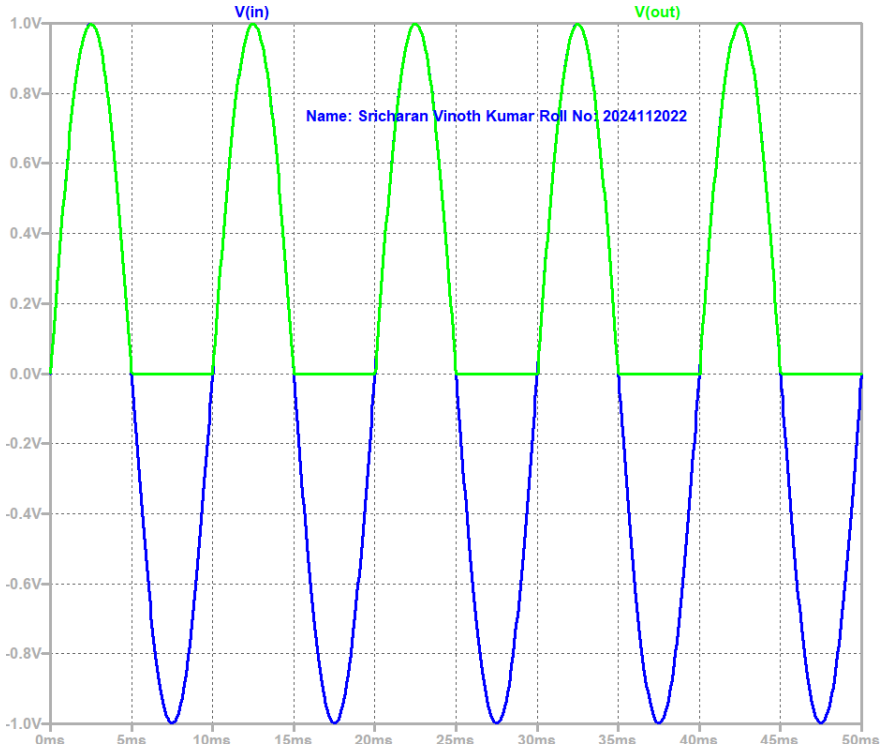

Figure 4.3.2: Plot of v_{in}(Blue) and v_{out}(Green) vs time

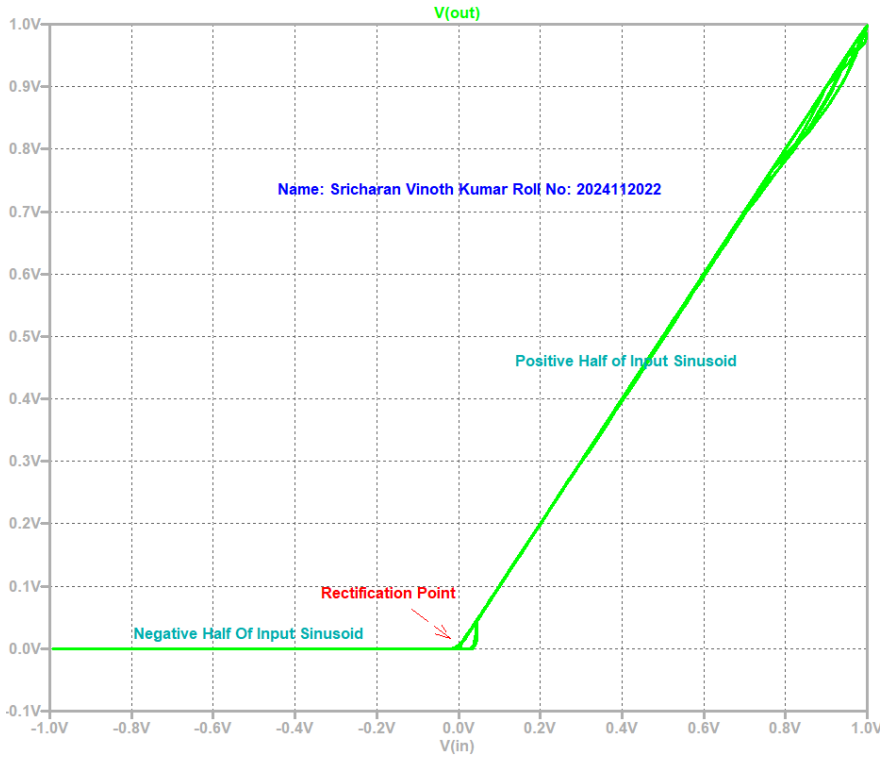

Figure 4.3.3: Plot of v_{out} vs v_{in}

From the VTC in Figure 4.3.3, we see a Voltage of 0 at Negative v_{in} and output voltage exactly matches input voltage at Positive v_{in}. This matches with what is expected in a precise Half Wave Rectifier.

4.4 Observation

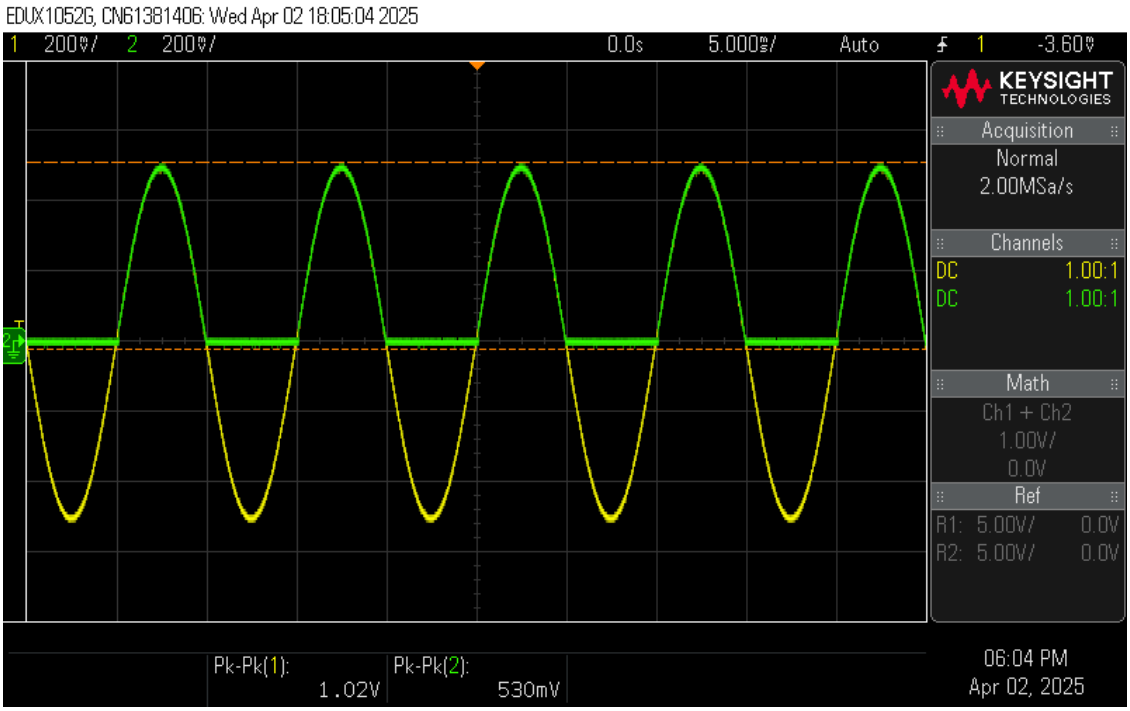

Figure 4.4.1: Plot of v_{in}(Blue) and v_{out}(Green) vs time

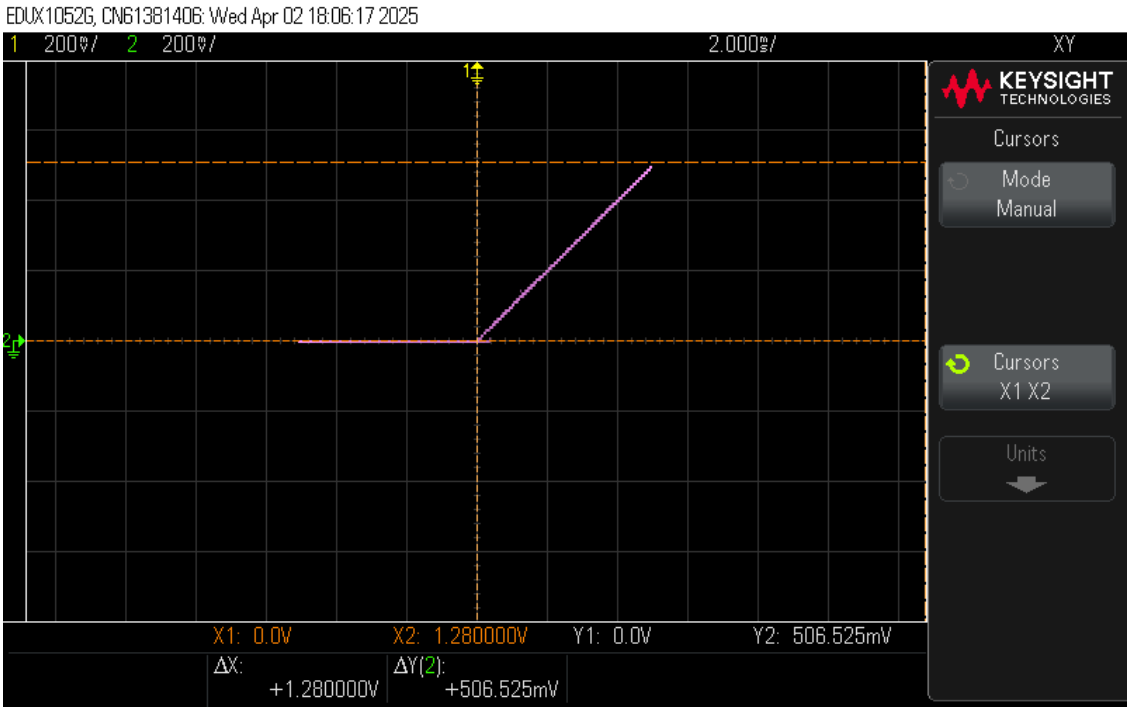

Figure 4.4.2: Plot of v_{out} vs v_{in}. (Acquire function)

From the VTC in Figure 4.4.2, we see a Voltage of 0 at Negative v_{in} and output voltage exactly matches input voltage at Positive v_{in} (The X Cursor is placed at $v_{in} = 0V$, to highlight this difference in behaviour). This matches with what is expected in a precise Half Wave Rectifier.

4.5 Inference

We see that the Precision Half Wave Rectifier is much more precise and matches more closely with what is expected from an Ideal Half Wave Rectifier than just using a single diode.
This is because, in a standard diode, we have a forward voltage drop that is needed to bias the diode in forward bias mode, which causes inaccuracies in small signals. But, since the Op-Amp is configured in Negative feedback, we need to match the output voltage with the input voltage, which causes the Op-Amp to compensate for that voltage drop, therefore, effectively eliminating the forward voltage drop.
The zeroing of the output voltage in the negative half of the input sinusoid is due to the diode being in Reverse bias, causing the final output terminal to be effectively disconnected from the output terminal of the Op-Amp, thus removing the Negative feedback configuration.