

Prof: Abhishek Srivastava , CVEST

23 lectures

- 30 hours

Grading :

Assignment (3/4) : 10 %.

Course Project : 20 %.

Quiz : 10 % + 10 %.

Midsem : 20 %.

Endsem : 30 %.

## VLSI Design

Assignment Deadline: 6pm

# VLSI Design

→ Topics:-

1) Intro to VLSI Design

2) CMOS Inverter

3) Multi-stage logic Design and Optimization

4) Other logic styles

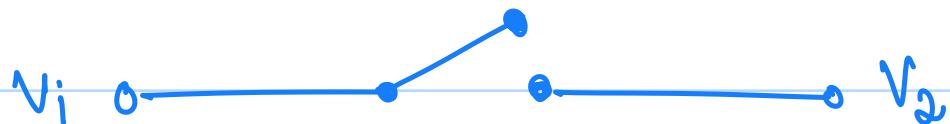
5) Intro. to HDL System Design.

• SCL - Semiconductor Complex Limited. Only fabrication facility in India. Can do upto 180 nm CMOS. Located in Mohali.  
↳ Considered a very old technology.

• We will be using 180 nm technology in this course, since it is now open-source.

→ High impedance state :-

• When a node is not connected to any well defined voltage, it is said to be existing in a high impedance state.

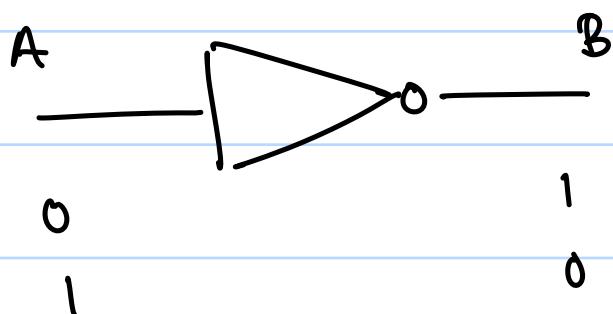


$V_2$  is in a high impedance state.

(Refer Weste & Harris MOS T Physics for  
today's lecture)

5/8/25

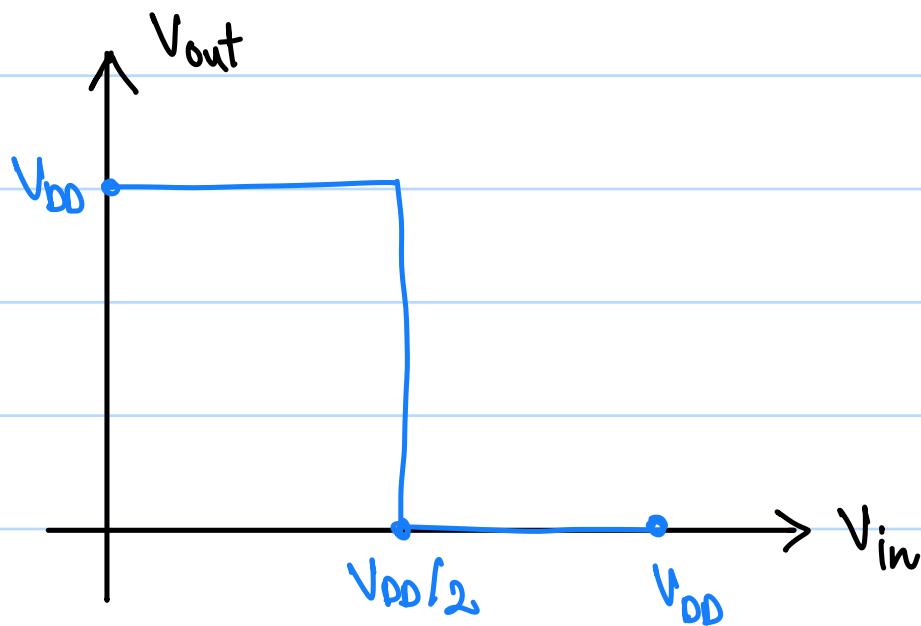
→ Inverter :-



A	B
0	1
1	0

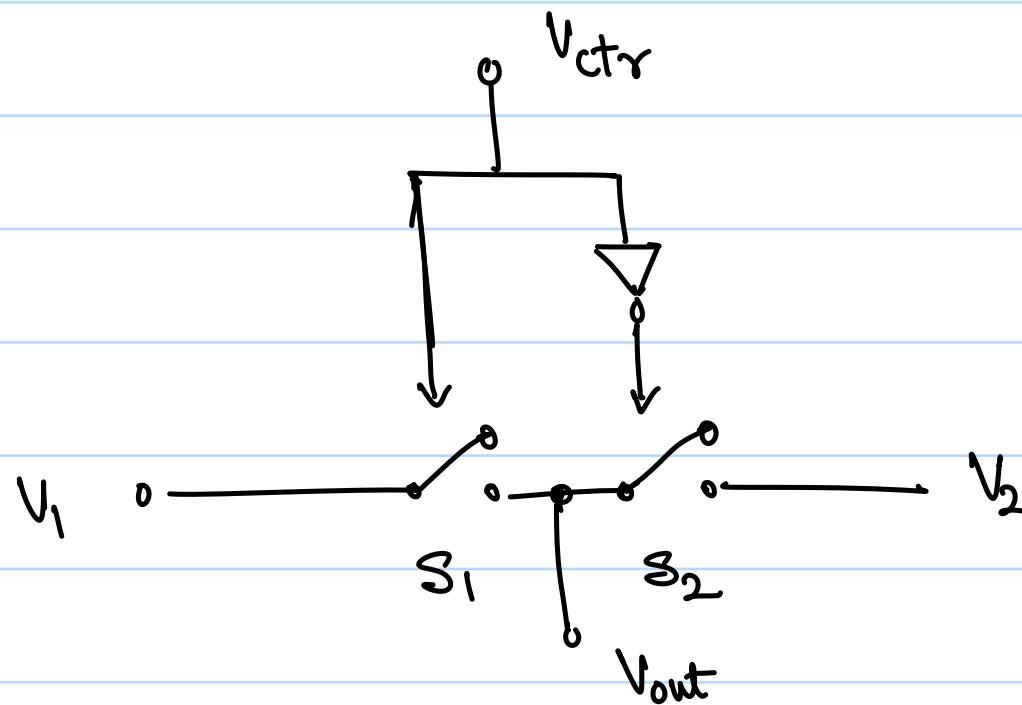
- 1 and 0 correspond to 2 different voltage levels.

• Ideally,



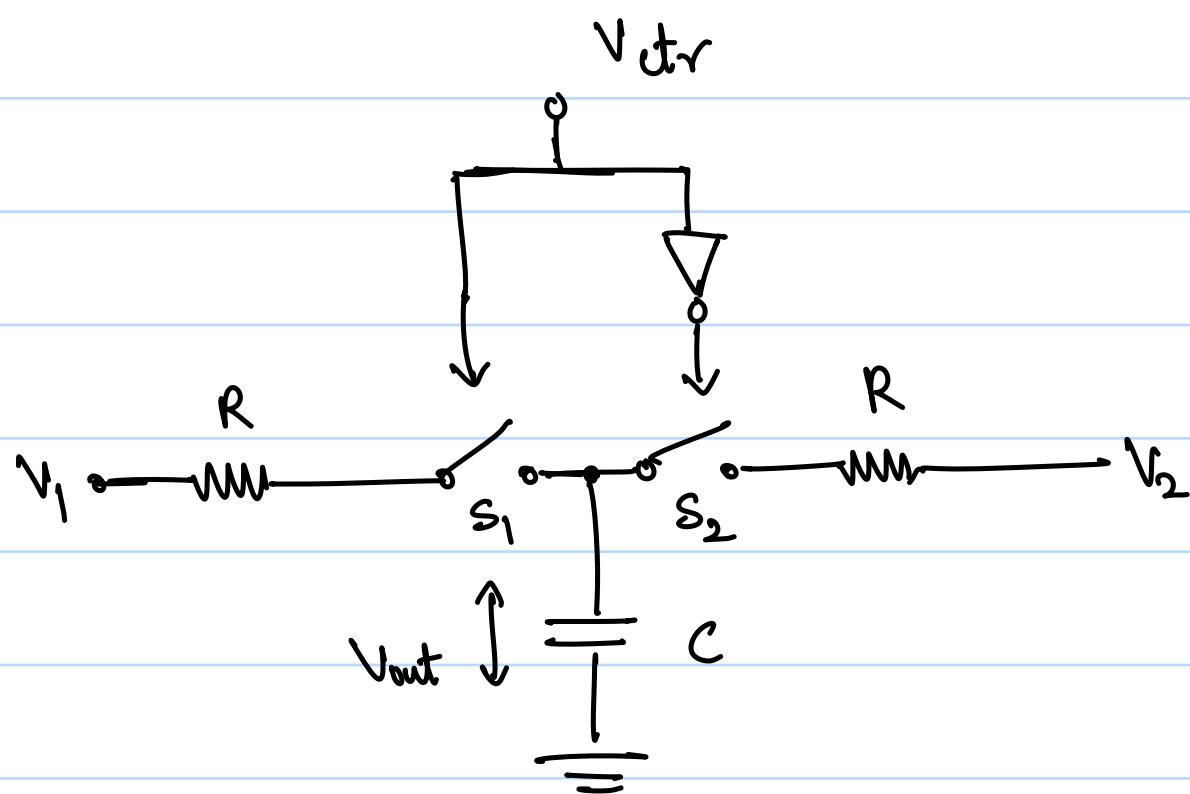
The above plot is termed as a VTC plot (Voltage Transfer Characteristics).

1)

Truth Table:

$V_{ctr}$	$V_{out}$
0	$V_2$
1	$V_1$

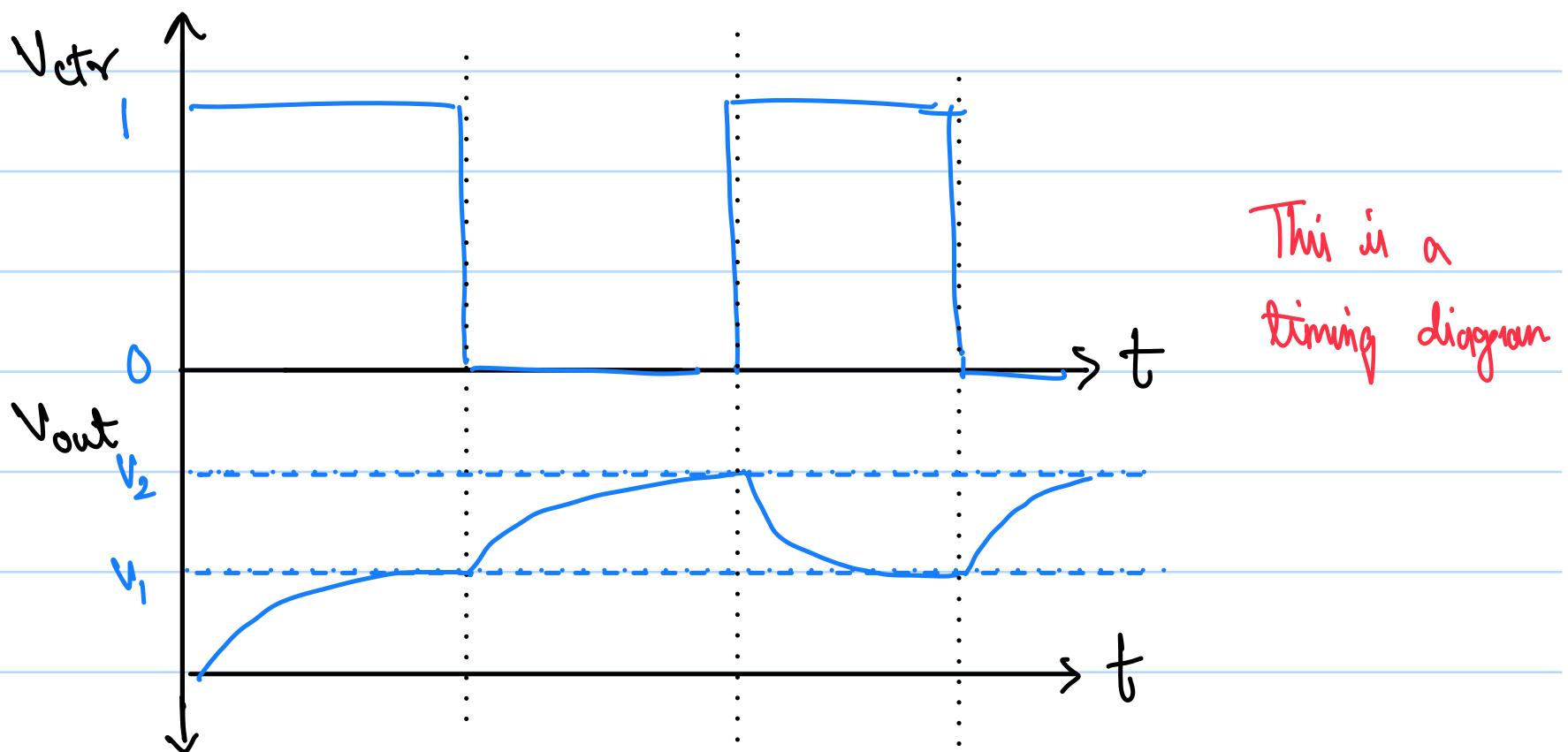
2)



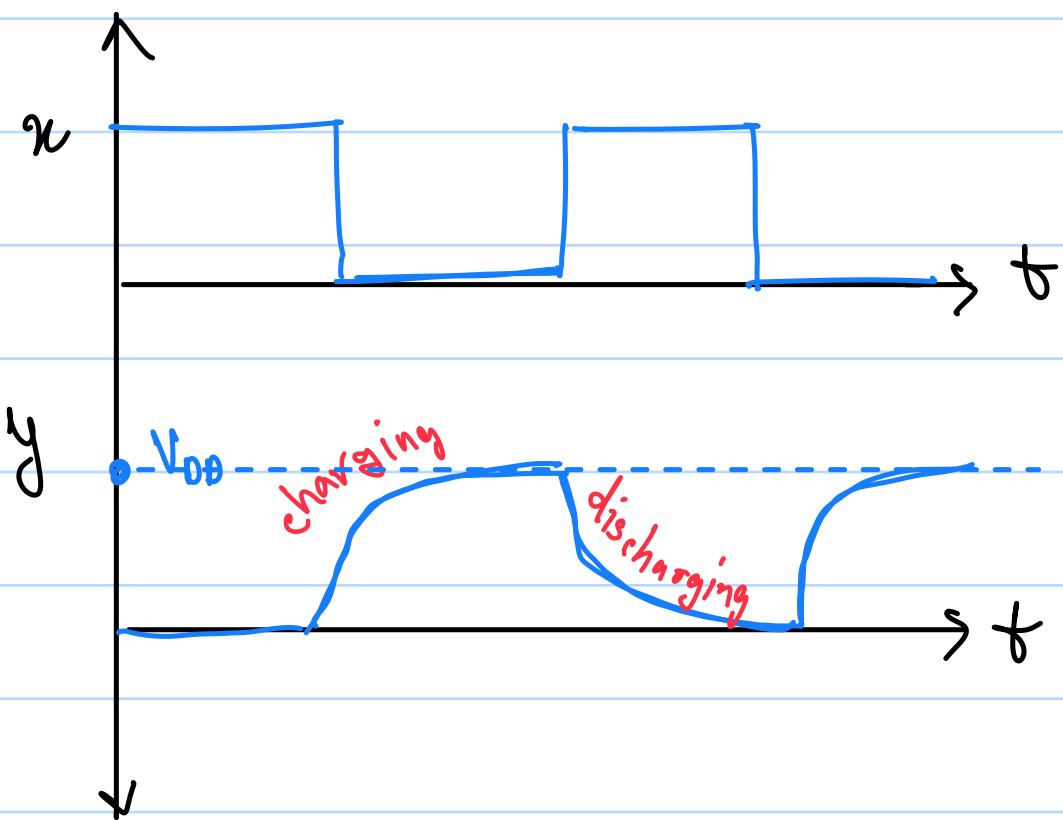
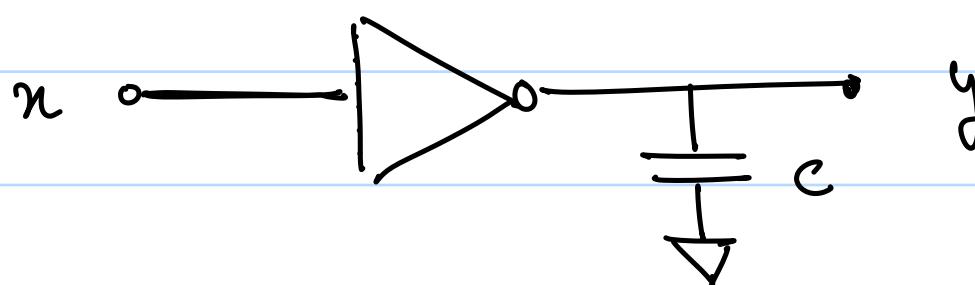
Here,  $V_{out} = \begin{cases} V_2(1 - e^{-t/RC}), & V_{ctr} = 0 \\ V_1(1 - e^{-t/RC}), & V_{ctr} = 1 \end{cases}$

If there is no resistance involved, the current through the capacitor will be a Dirac impulse, infinite for an infinitesimal time.

( $i = C \frac{dV}{dt}$ ,  $dt$  is very small)

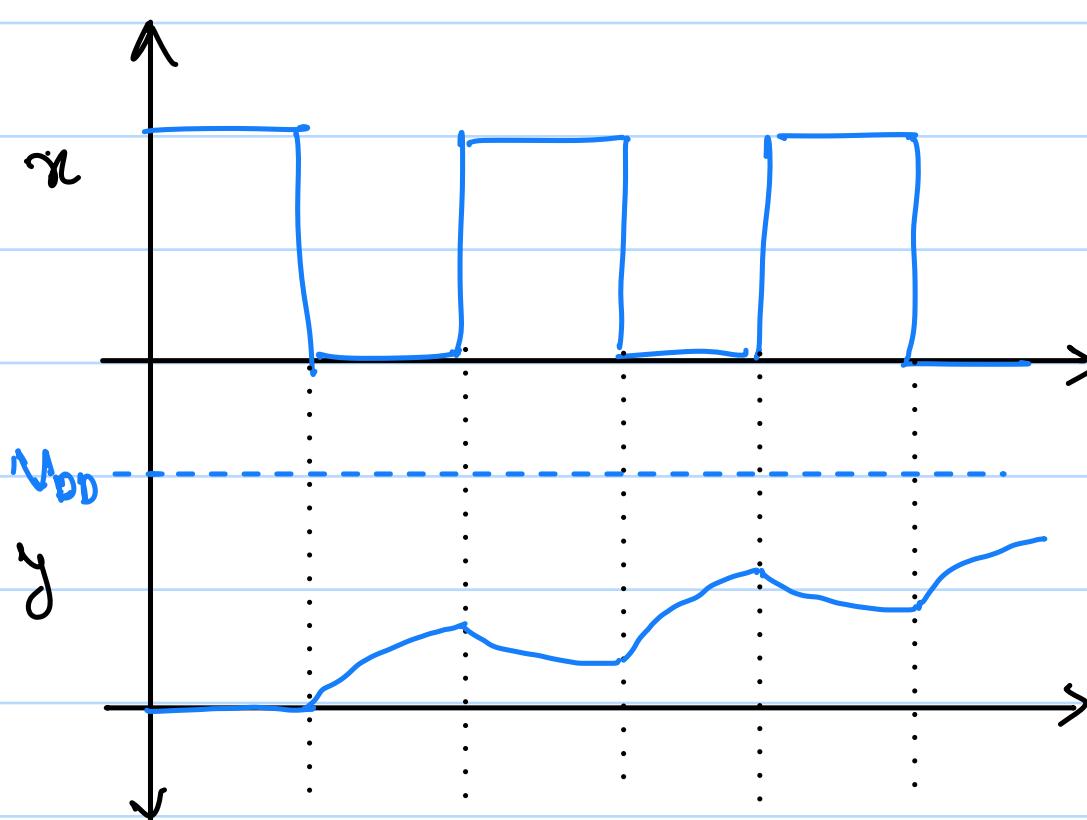


3)



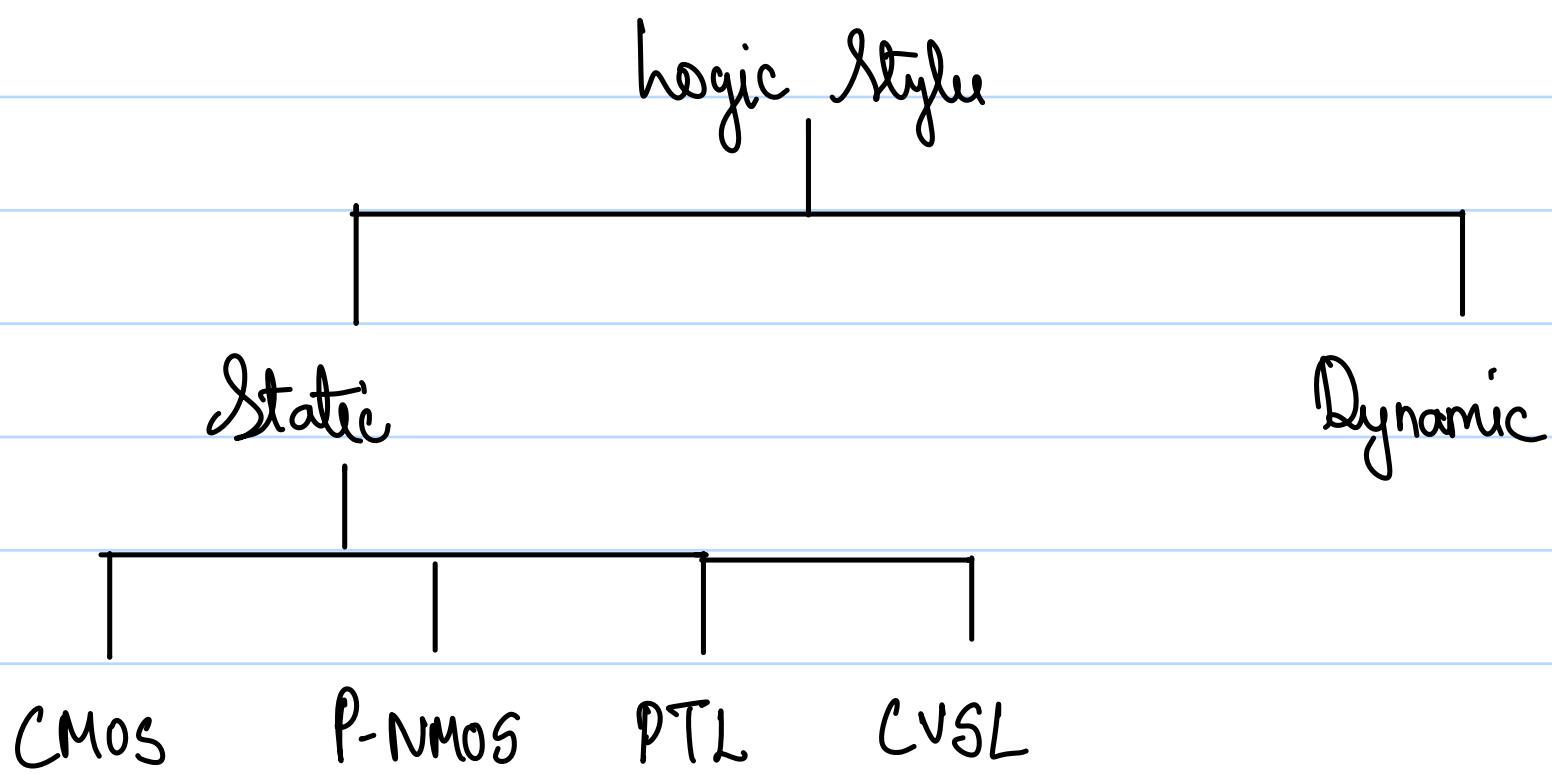
- ° The charging and discharging speeds of the capacitor are dependent on the RC / time constants of the circuit.

If  $RC$  is very large,



The capacitor is not fast enough to reach  $V_{DD}$  and zero, so information is lost.

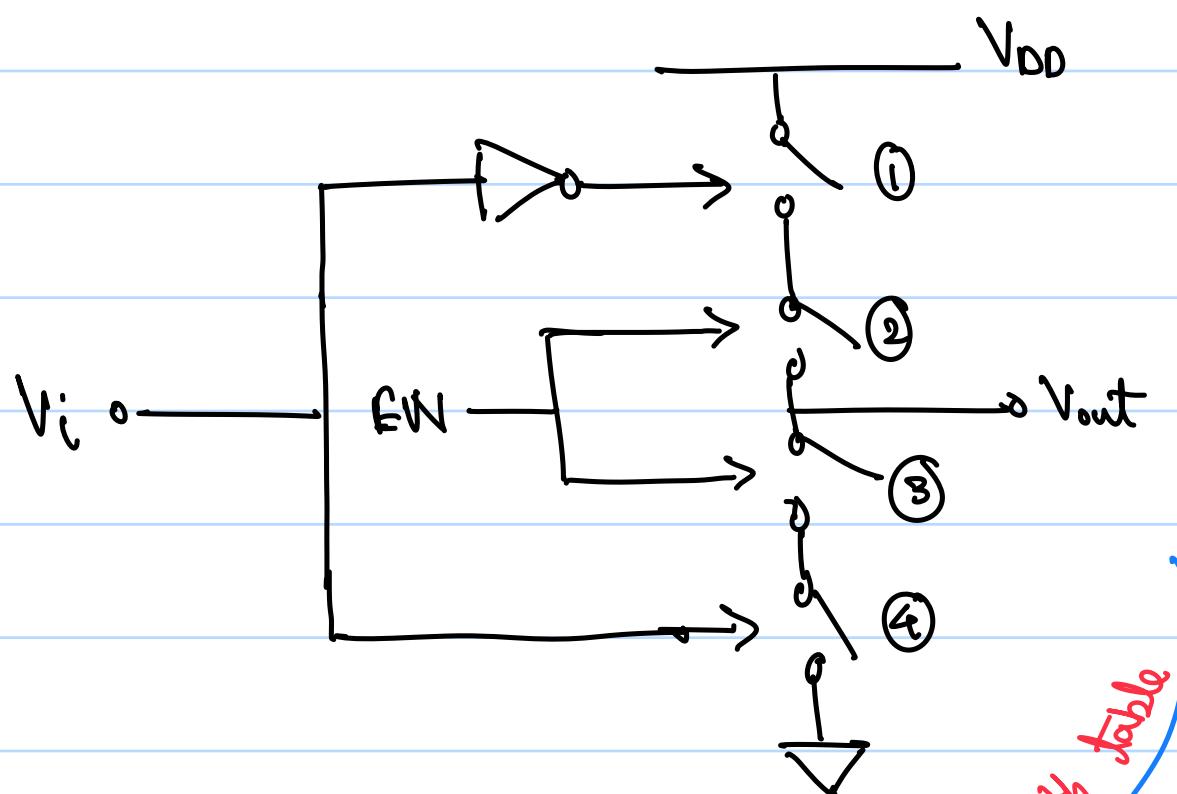
- Because of this, the RC parameters of the circuit must be fast enough to handle the input speed/frequency.



# Circuit Design

Combinational      Sequential      Memory

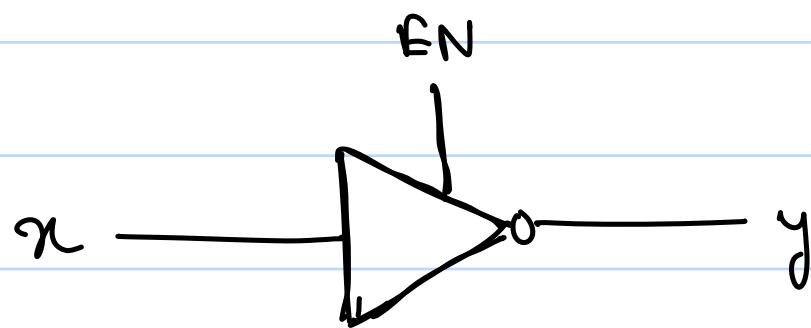
4)



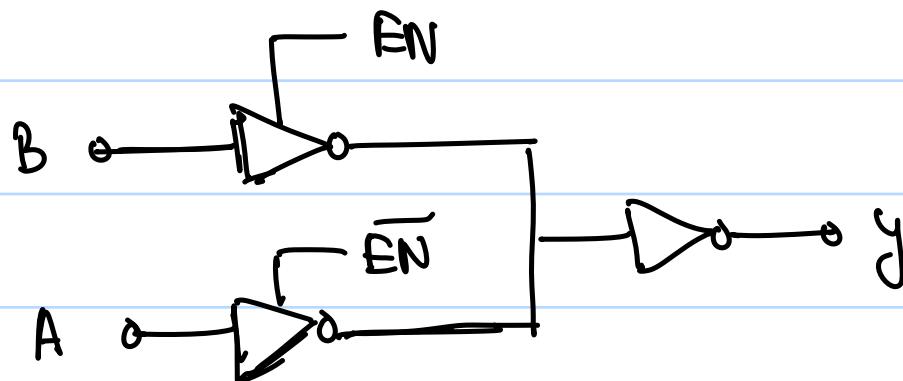
*truth table*

EN	V <sub>i</sub>	V <sub>o</sub>
0	0	Z
0	1	Z
1	0	V <sub>DD</sub>
1	1	0

The above device acts like an inverter if  $EN = 1$ . This is the design of a tri-state inverter.



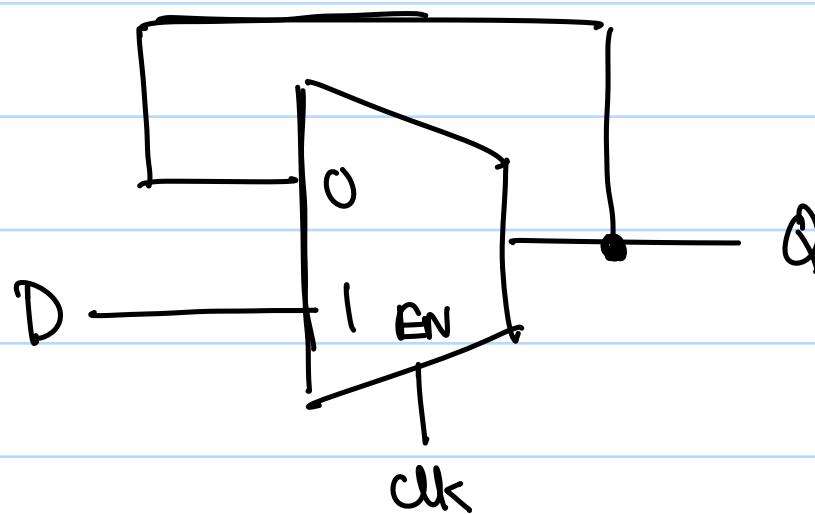
5)



Truth Table:

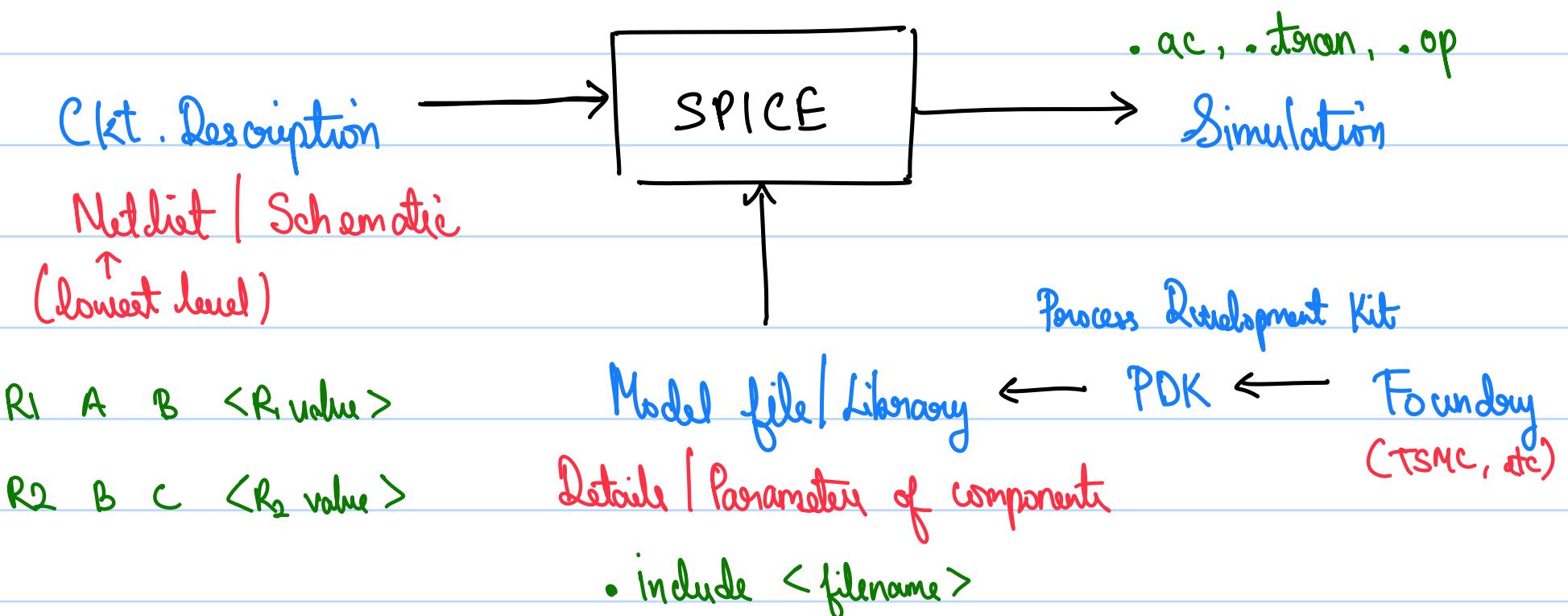
EN	Y
0	A
1	B

- Due to the high impedance, the output of one tri-state inverter will not be affected by the other, since one output is always  $z$ .
- The above device will act as a  $2 \times 1$  MUX, which can be used to design devices like gates and latches.



Level Triggered D-Latch

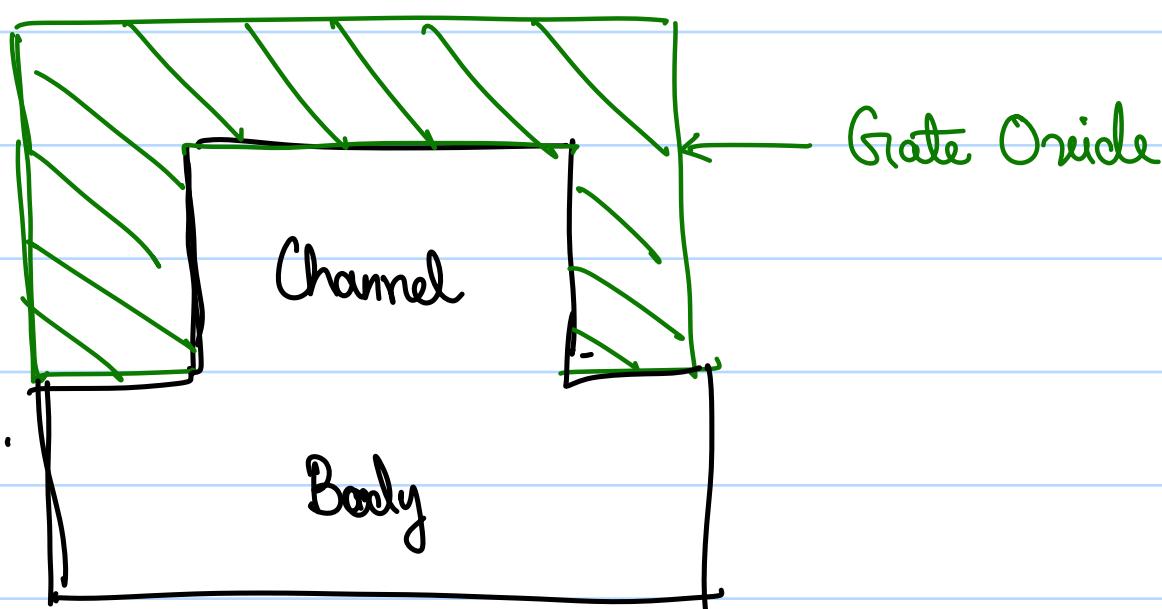
→ SPICE :-



→ Technology Node:

- To make a semiconductor chipset on a substrate, we use a "stencil" of the circuit layout.
- In the chipset, there are multiple metal layers on top of the substrate, to provide the interconnection between the MOSFETs.
- Within the MOSFETs, there are multiple dimensions that vary between them, depending on the usage of that MOSFET
- The minimum of those dimensions, ie, minimum feature length among the MOSFETs is deemed as the "Technology node" of that MOSFET. Usually minimum channel length.
- 3nm (N3) node - Retail products released  
2nm (N2) node - Will release early next year.

- < 22nm - FinFETs are used instead of MOSFETs.



View of FinFET through Source/Drain

In FinFETs, the oxide wraps around the channel, enabling better inversion at a lower gate potential, better than MOSFETs.

- A14 - 1.4nm node } In development.
- A7 - 0.7nm node }

- 180nm is still widely used, in devices that do not require extremely high competition.

- Lower transistor size  $\Rightarrow$  lower cost per transistor.

- Clock Speed:

- Recently the clock speed of processes has saturated.

- Since the packing density has increased by a lot, the heat and leakage of the transistors have increased by a lot.

- These factors made it difficult for clock speed to improve as fast as the technology node.

→ Shannon's Expansion :-

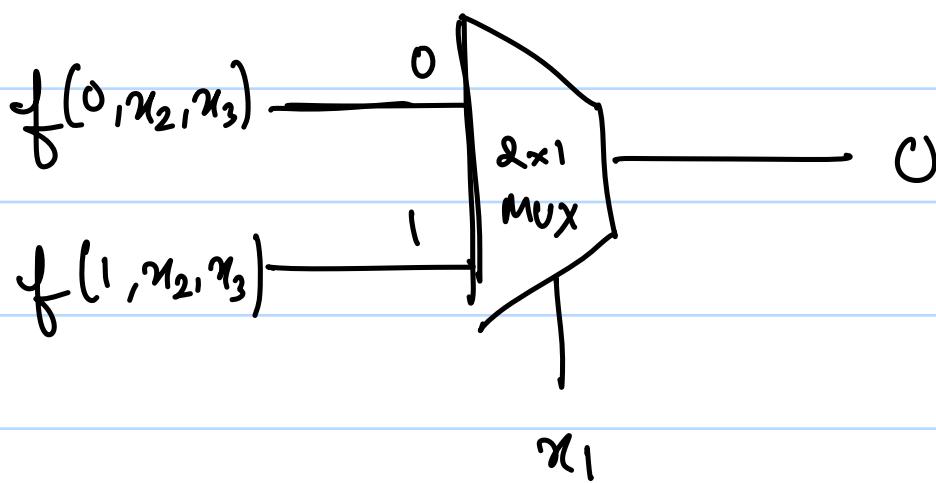
- For any function  $f(x_1, x_2, x_3 \dots x_n)$ ,

$$f(x_1, x_2, x_3 \dots x_n) = x_1 f(1, x_2, x_3 \dots x_n) + \bar{x}_1 f(0, x_2, x_3 \dots x_n)$$

Example: Expand  $f(x_1, x_2, x_3) = \bar{x}_1 \bar{x}_3 + x_1 x_2 + x_1 x_3$ . w.r.t  $x_1$

$$\Rightarrow f(x_1, x_2, x_3) = x_1 (x_2 + x_3) + \bar{x}_1 (\bar{x}_3)$$

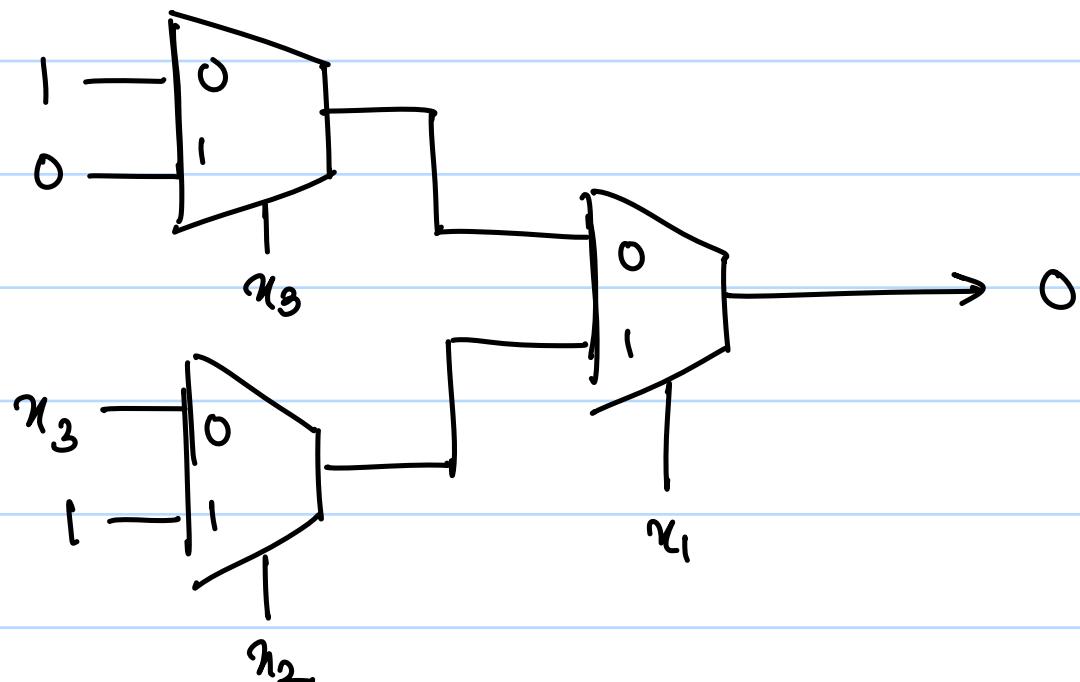
- If we expand the function in this way, we can use a  $2 \times 1$  MUX to implement the function, using  $x_1$  as the selection variable.



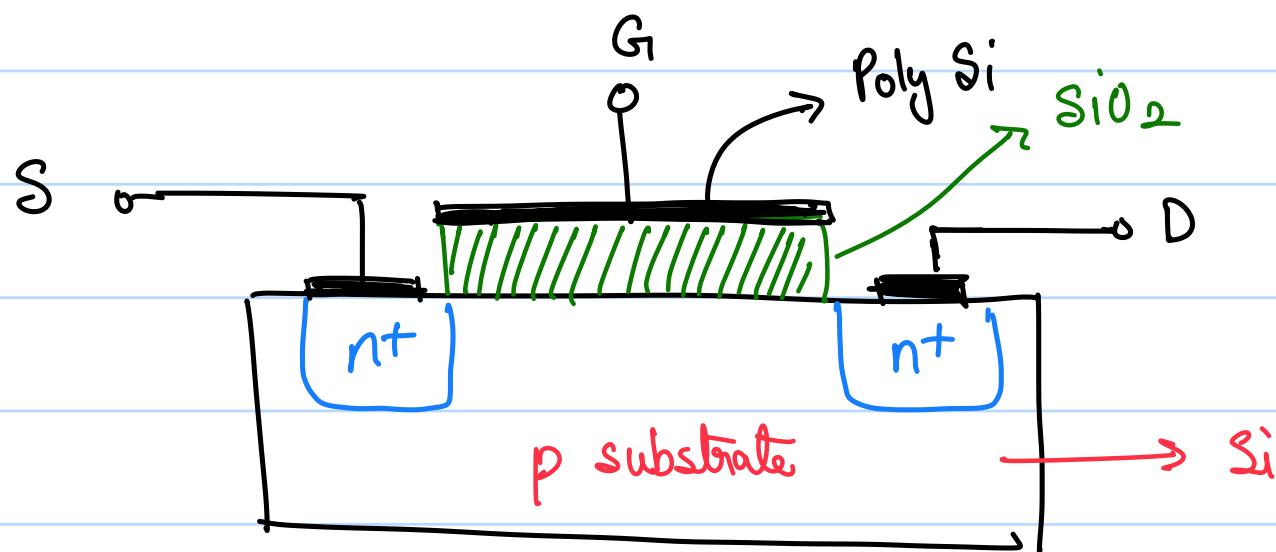
Example: Express the prev. function only using 2x1 MUXes.

$$\begin{aligned} f(x_1, x_2, x_3) &= \bar{x}_1 \bar{x}_3 + x_1 x_2 + x_1 x_3 \\ &= x_1 (x_2 + x_3) + \bar{x}_1 (\bar{x}_3) \end{aligned}$$

$$\begin{aligned} f(x_2, x_3) &= x_2 + x_3 \\ &= x_2(1) + \bar{x}_2(x_3) \end{aligned}$$



→ MOSFETs :-

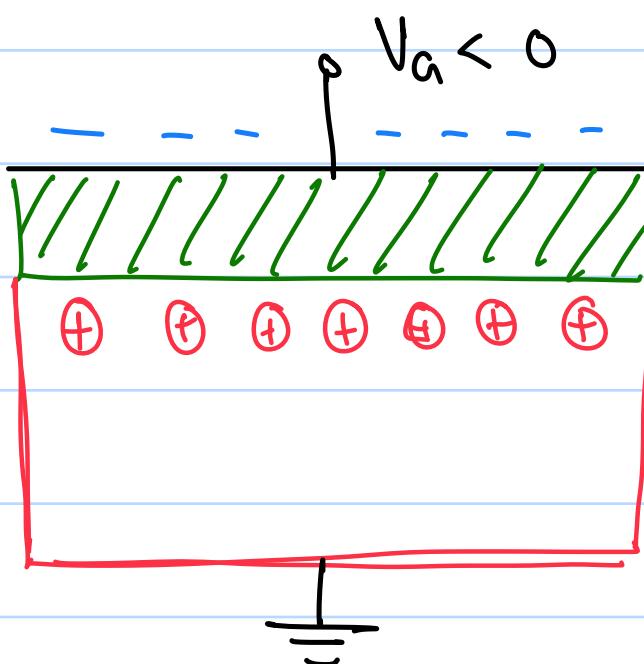


NMOS Structure

- Poly silicon is used in the gate terminal to simplify the manufacturing process, since silicon is the major element of a MOSFET.

- Let S and D be grounded and ,

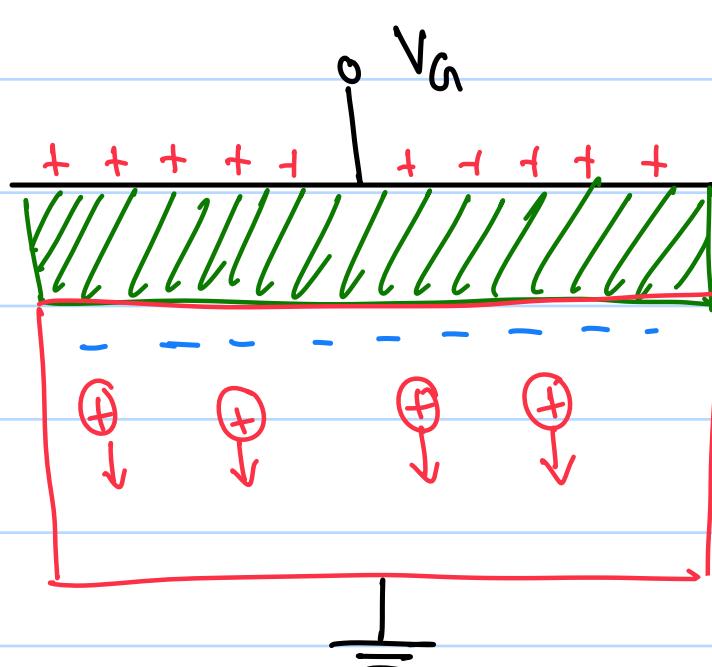
1)  $V_G < 0$



holes are attracted towards the gate

- This is accumulation mode of operation .

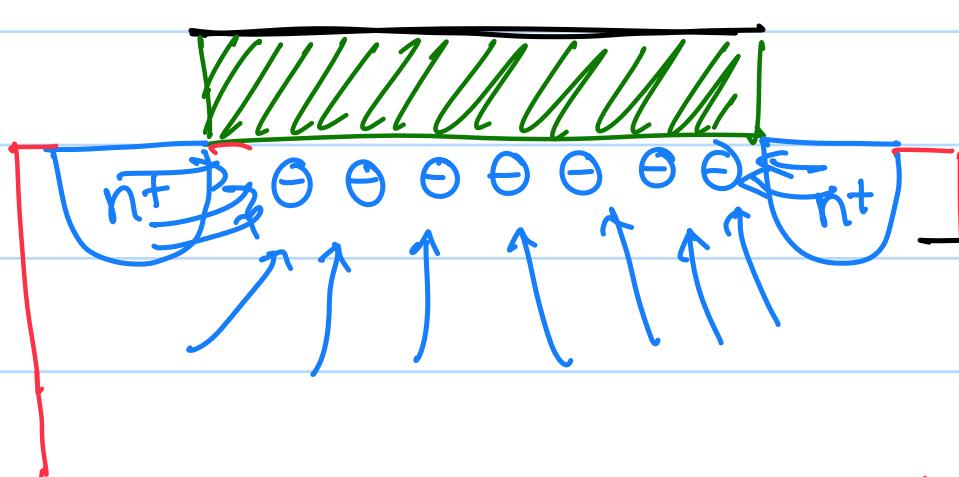
2)  $V_G > 0$



holes go away from gate, leaving -ve charge .

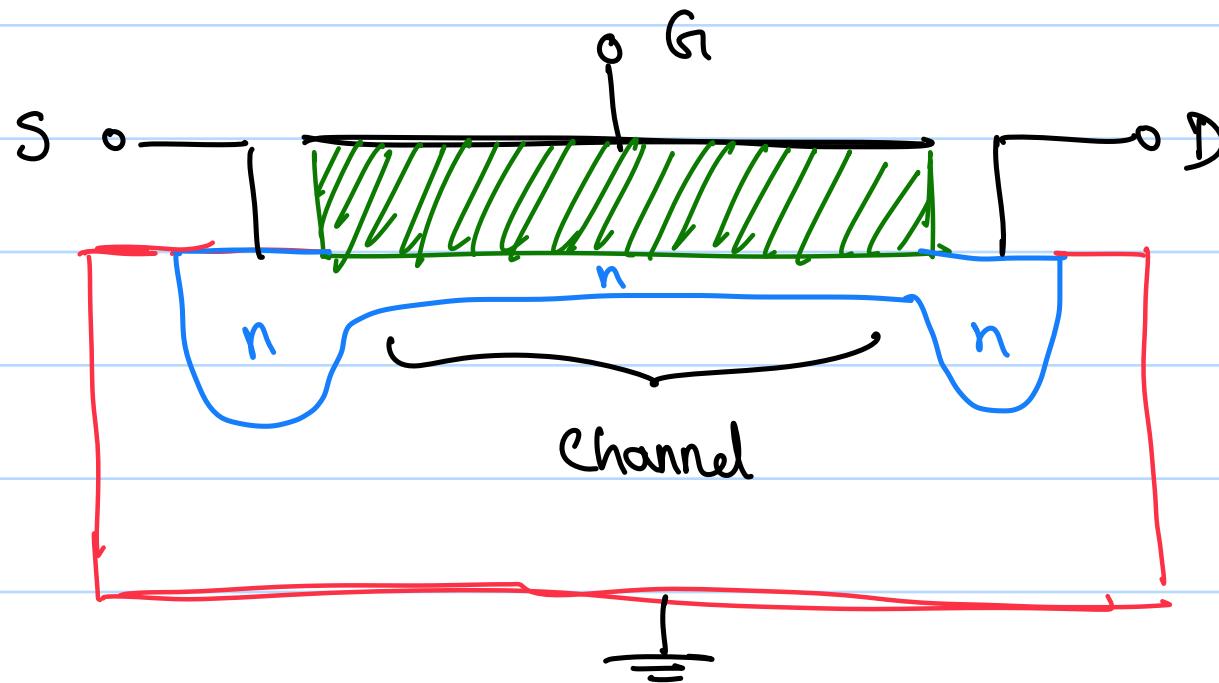
- This is depletion mode of operation .

3)  $V_G \gg 0$



electrons are attracted from the substrate and (majority) from S and D

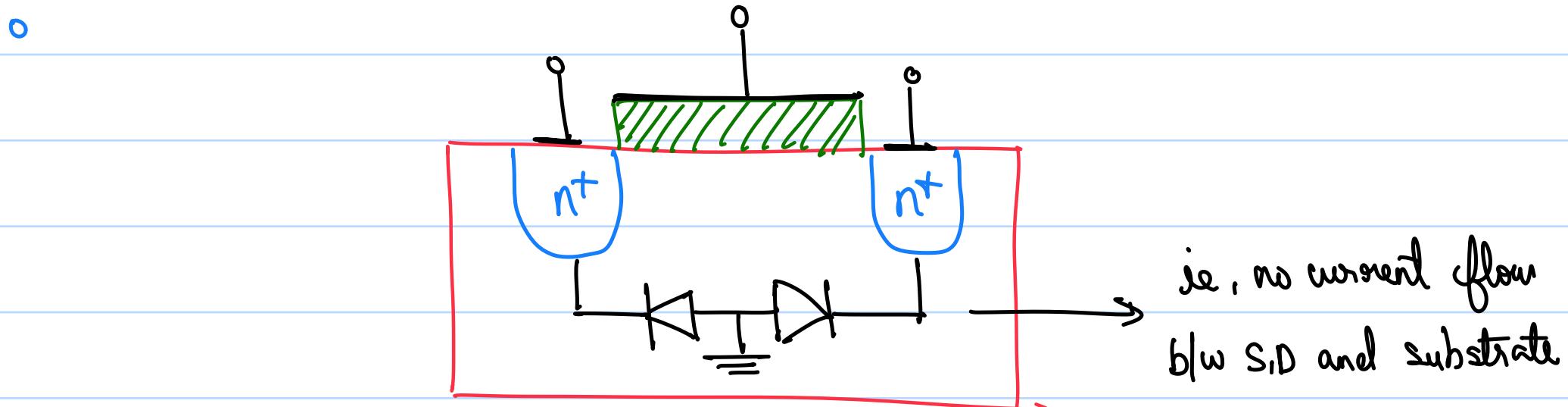
- The surface of the p-substrate becomes dominated by electrons, ie, becomes n-type.



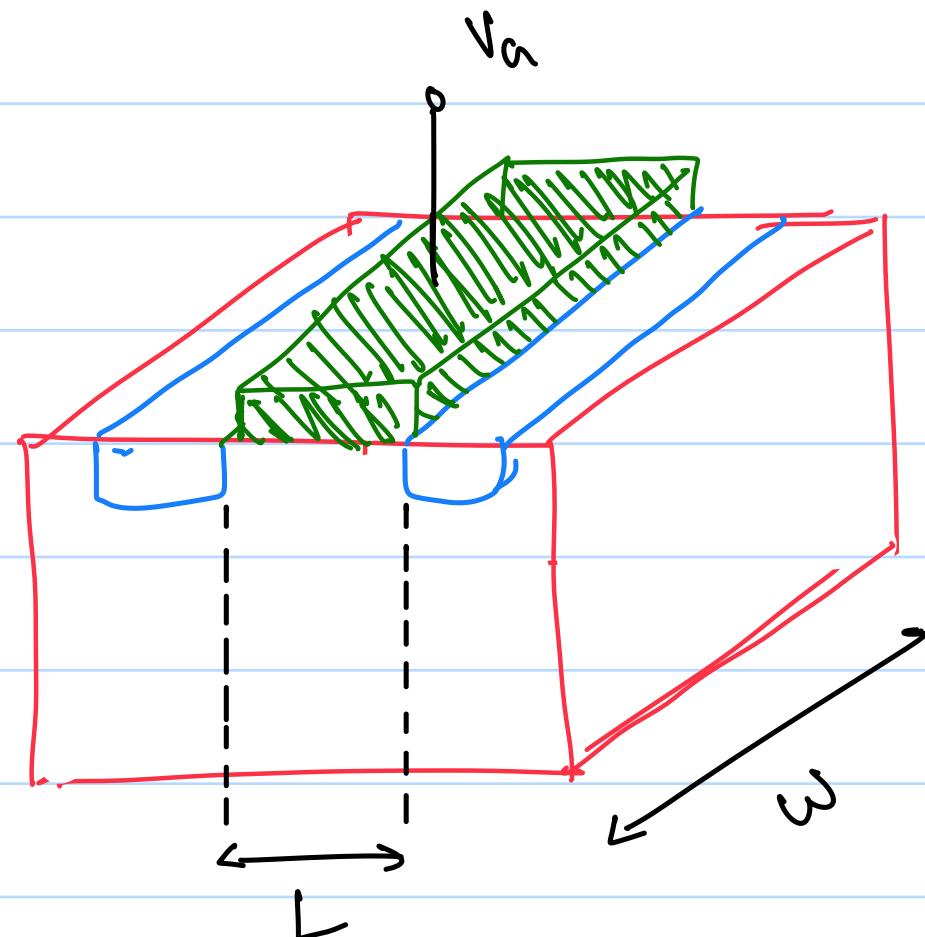
- This is inversion mode of operation.

- If  $n_e$  at surface  $< N_A$  (hole conc. of substrate), it is weak inversion / subthreshold mode.

- If  $n_e$  at surface  $\geq N_A$ , it is strong inversion. The min. gate voltage to attain strong inversion is  $V_{TH}$  (threshold voltage)

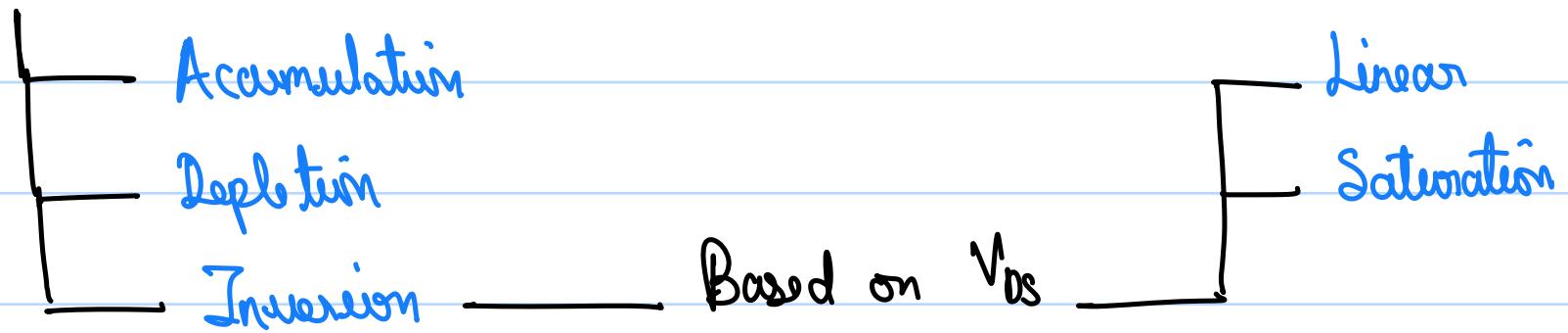


• 3D View:-



Since the n-channel is not perfectly conductive, it has some resistance to it, depending on the dimensions L and w.

Based on  $V_{AS}$



1)  $V_{AS} \leq 0 \Rightarrow I_D = 0 + V_{DS}$ . Accumulation mode has zero channel.

2)  $0 < V_{AS} < V_{TH} \Rightarrow I_D \approx I_{D0} e^{\frac{V_{AS}-V_{TH}}{nVt}}$ .  $V_t$  - thermal voltage.

Subthreshold conduction.

3)  $V_{AS} > V_{TH}$  &  $V_{DS} < V_{AS} - V_{TH} = V_{ov}$ . (Overshoot voltage)

$$I_D = \frac{1}{2} \mu_n C_o \frac{w}{L} \left( 2V_{ov}V_{DS} - \frac{V_{DS}^2}{2} \right) \rightarrow \text{Linear Mode of Opn.}$$

If  $V_{DS} \ll V_{OV}$ ,

$$I_D = \left( \mu_n C_o x \frac{W}{L} V_{OV} \right) V_{DS}$$

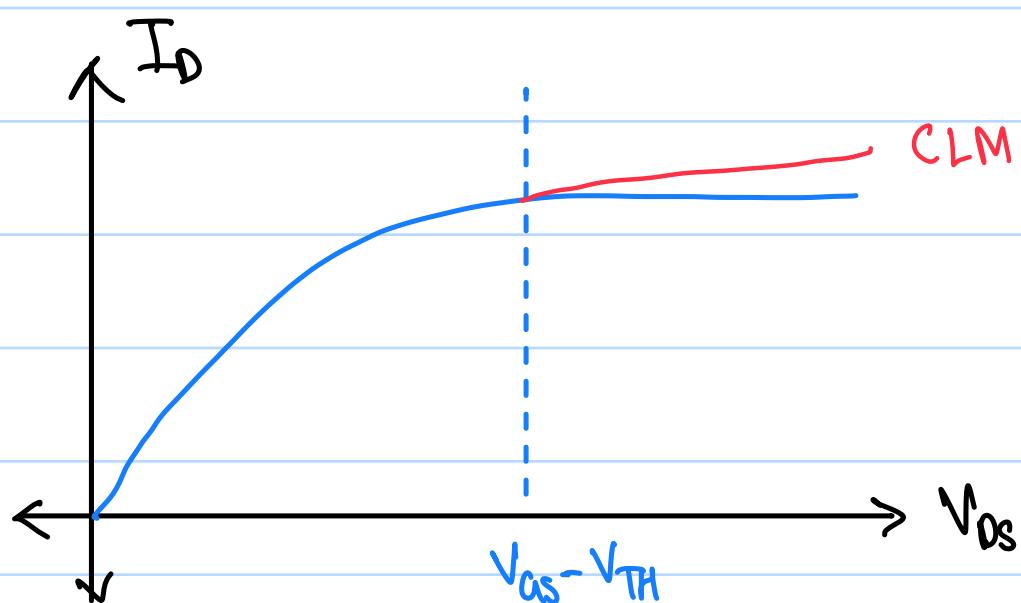
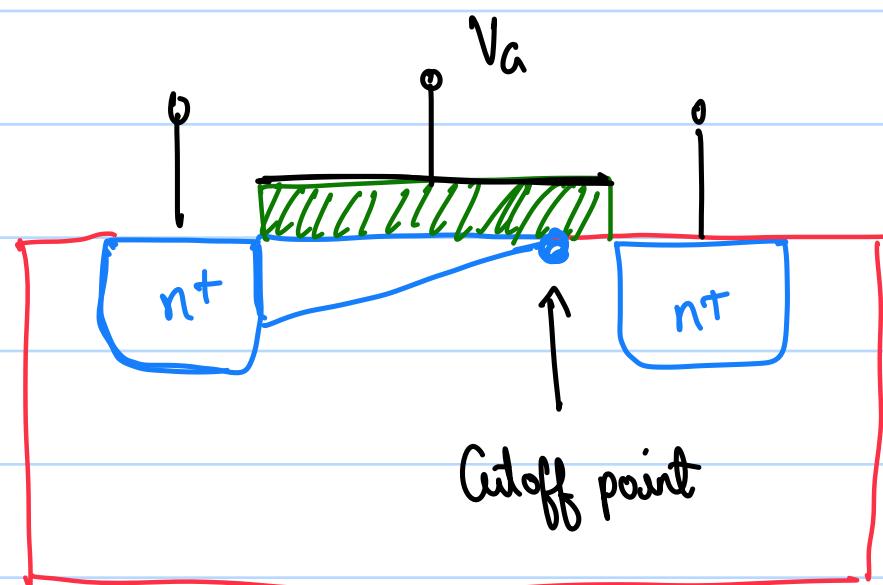
$$\Rightarrow R = \frac{1}{\mu_n C_o x \frac{W}{L} V_{OV}}$$

4)  $V_{GS} > V_{TH}$ ,  $V_{DS} \geq V_{GS} - V_{TH}$

$$\Rightarrow V_{GS} - V_{DS} \leq V_{TH}$$

$$\Rightarrow \underline{V_{DS} \leq V_{TH}}$$

Since  $V_{DS} \leq V_{TH}$ , the channel will cease to exist near the drain, since potential at the point will be lesser than threshold.



Beyond the cutoff point, the charge density is very low (depletion mode). Let linear charge density there be  $Q_d$ .  $Q_d \approx 0$ .

$$dQ = Q_d \cdot dx$$

$$\frac{dQ}{dt} = Q_d \frac{dx}{dt}$$

$$= I = Q_d V_d$$

$$= V_d = \frac{I}{Q_d} \Rightarrow \lim_{Q_d \rightarrow 0} \frac{I}{Q_d}$$

$\therefore V_d \rightarrow \infty$  for finite  $I$ .

$\therefore$  The electrons are swept almost instantaneously across the cutoff point into the drain.

$$I_{DS} = \begin{cases} \mu n C_o \frac{W}{L} (2(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}), & V_{GS} > V_{TH}, V_{DS} < V_{ov} \\ \frac{1}{2} \mu n C_o \frac{W}{L} (V_{GS} - V_{TH})^2, & V_{GS} > V_{TH}, V_{DS} > V_{ov} \\ 0, & V_{GS} \ll V_{TH} \\ I_{DSS} e^{\frac{V_{GS}-V_T}{nVt}} [1 - e^{\frac{V_{DS}}{4}}], & V_{GS} < V_{TH} \end{cases}$$

(Subthreshold leakage)

• PMOS:

$$I_{SD_{PSOL}} = \frac{1}{2} \mu p C_o \frac{W}{L} [V_{SA} - |V_T|]^2$$

$$V_{SA} \geq |V_T| \quad \&$$

$$V_{SD} \geq V_{SA} - |V_T|$$

$$I_{SD\text{plin}} = \mu_p C_{ox} \frac{W}{L} \left[ (V_{SD} - |V_T|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

• Second-Order Effects :-

1) Channel Length Modulation :-

Since the cutoff point moves further towards the source, as  $V_{DS}$  increases,  $I_D$  actually increases with  $V_{DS}$  even during saturation.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$\lambda$  CLM Parameter

$$\lambda V_{DS} = \frac{\Delta L}{L}$$

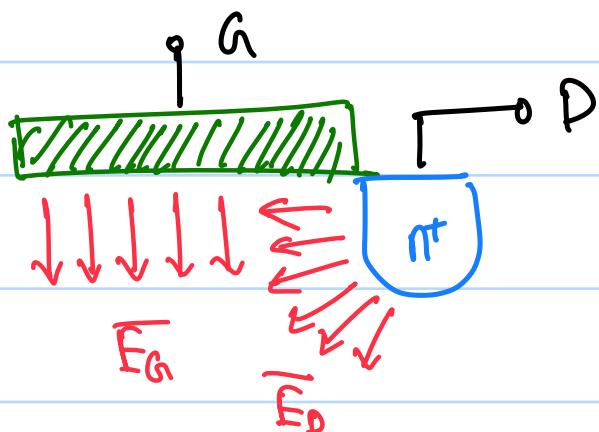
2) Body Biasing :-

If  $V_{BS}$  is increased, the threshold voltage of the MOSFET is decreased.

$$V_{TH} = V_{TH0} + \sqrt{2\psi_s + V_{SB}} - \sqrt{2\psi_s}$$

3) Drain Induced Barrier Lowering :-

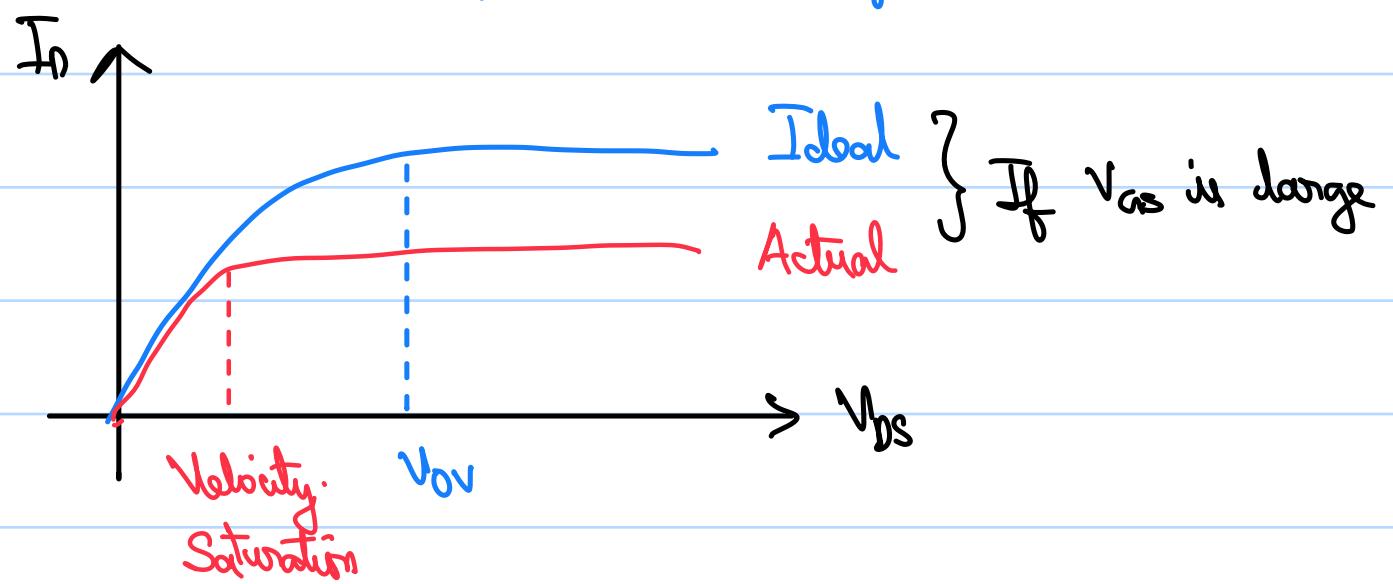
In short channel MOSFETs, the drain voltage will aid in the inversion of the channel.



Because of this aid, the threshold voltage of the MOSFET will be lower.

#### 4) Velocity Saturation :-

For each channel, there is a certain  $V_d$  at which mobility degradation occurs due to scattering of the charge carriers. Prominent if  $V_{as}$  is large.

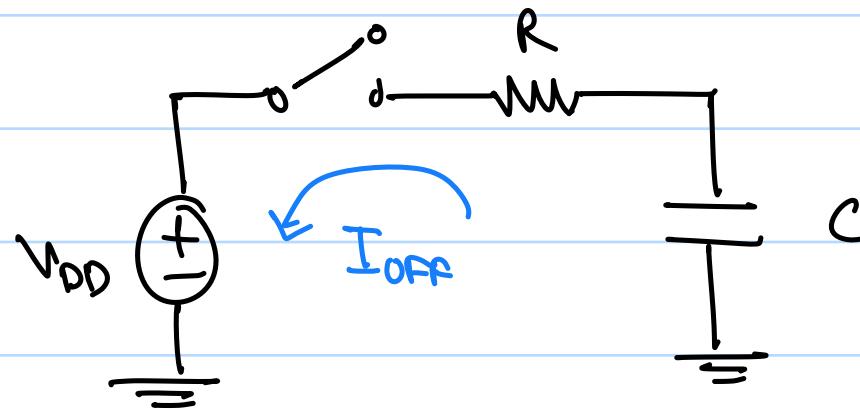


If  $V_{as}$  is low, overdrive voltage is attained before velocity saturation, so the effect is not visible.

#### • Switch $I_{ON}, I_{OFF}$ :-

- $I_{ON}$  : Current through the switch when it is in the ON position.
- $I_{OFF}$  : Current through the switch when it is in the OFF position.
- Ideally  $I_{OFF}$  should be zero, but it is non-zero due to effects like leakage.

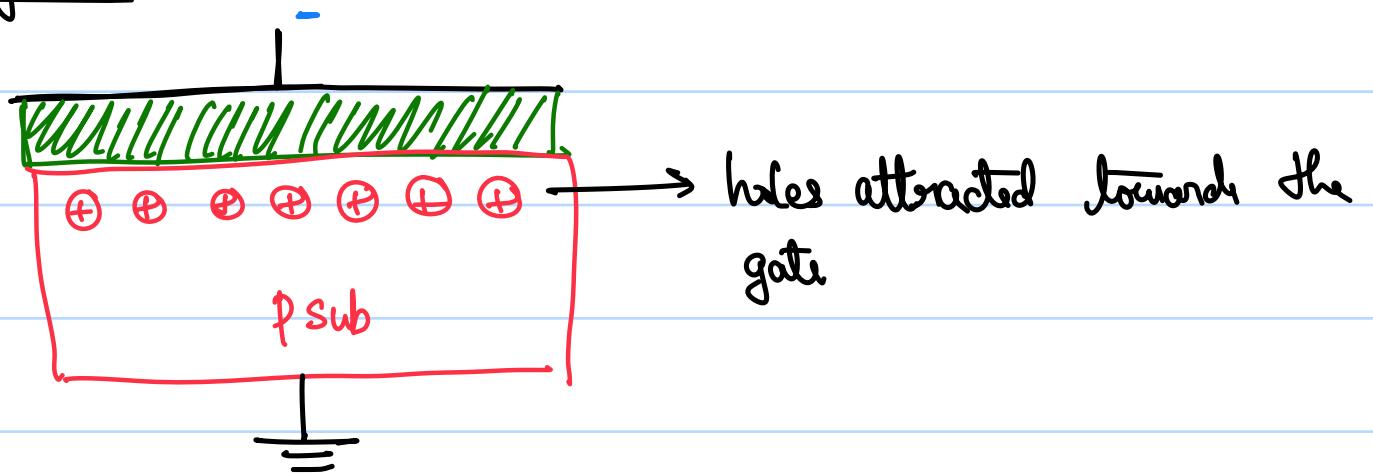
-  $t_{\text{hold}}$  : Time taken for a capacitor to discharge in an RC circuit when the switch is OFF.



$$\text{For a good circuit, } t_{\text{hold}} \geq \frac{1}{2} \frac{C V_{DD}}{I_{OFF}}$$

- MOS Capacitor:

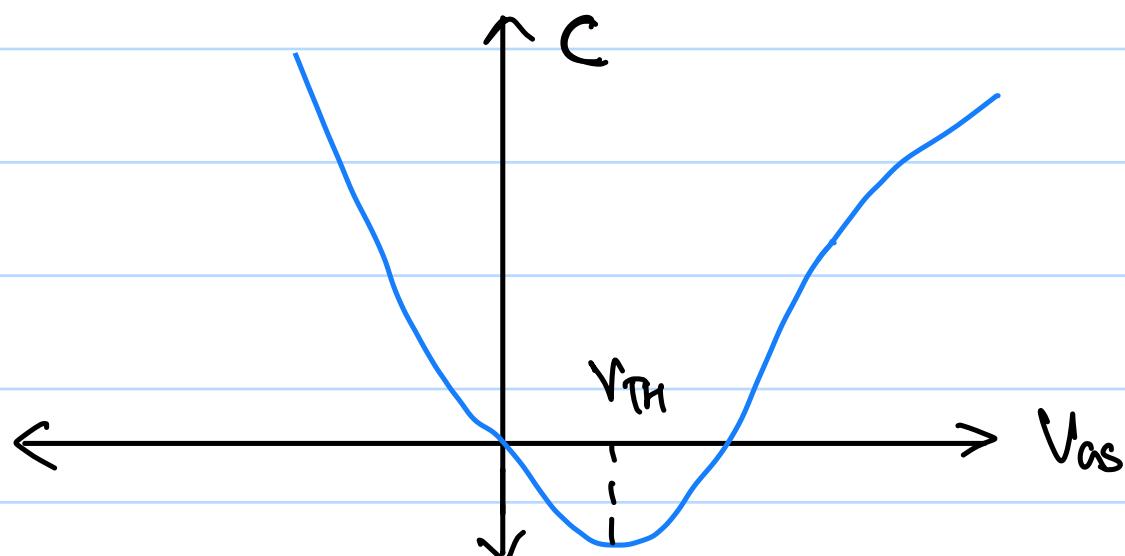
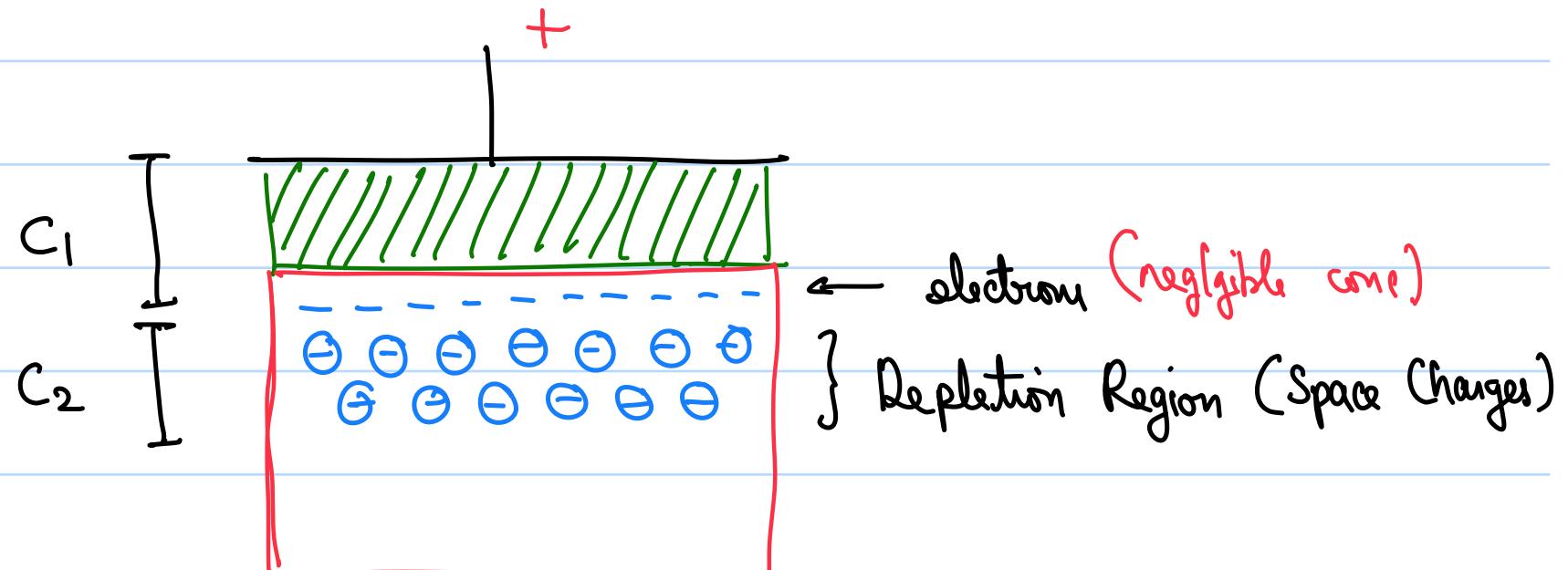
- i) Accumulation Region:-



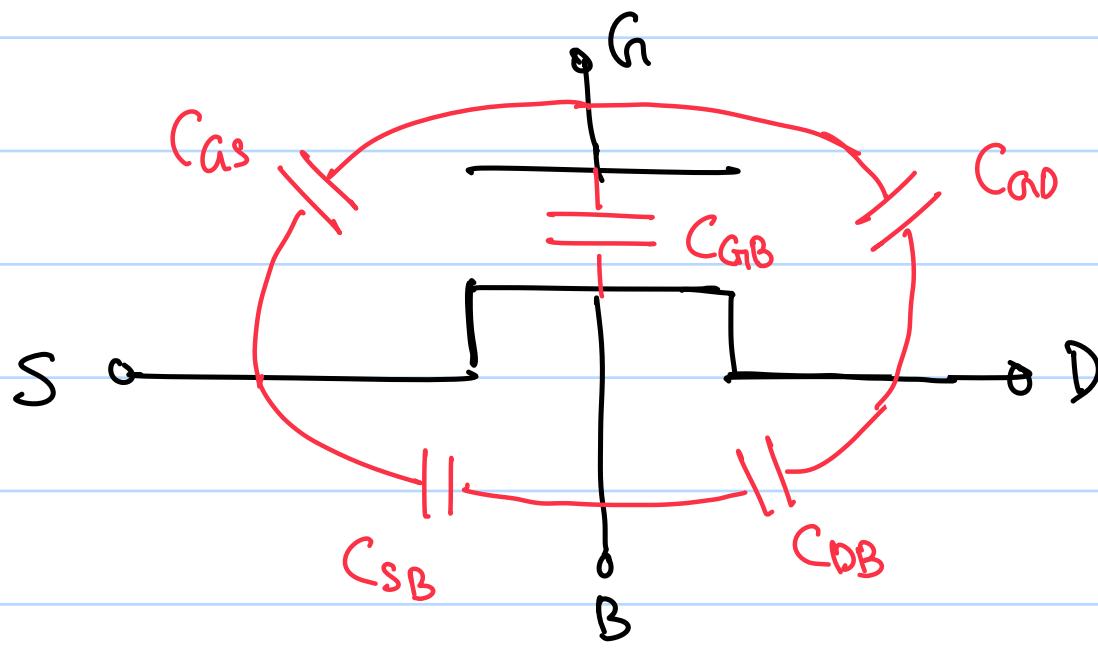
The capacitor acts like a normal parallel plate capacitor.

$$C = \frac{\epsilon A}{d} = \frac{\epsilon W L}{t_{ox}}$$

## 2) Depletion and Inversion :-



## • Capacitance in the Modes of Operation :-



1) In Cutoff:  $C_{GS} = C_{GD} = wC_{ov} \rightarrow$  Overlap Capacitance

$$C_{ov} = WL C_{ox}$$

2) In Linear :-  $C_{GD} = C_{GS} = \frac{WLCon}{2}$

$$C_{GD_{ov}} = C_{GS_{ov}} = WLCon$$

3) In Saturation :-  $C_{GS} = WLCon + \frac{2}{3}WLCon$

5) Mobility Degradation :-

The mobility of the channel depends on the electric field inside the channel as follows,

$$\mu \propto E^0 \text{ for } E < 10^3 \text{ V/cm}$$

$$\mu \propto \frac{1}{\sqrt{E}} \text{ for } E \approx 10^3 - 10^4 \text{ V/cm}$$

$$\mu \propto \frac{1}{E} \text{ for } E > 10^4 \text{ V/cm}$$

Note: Short Channel MOSFETs are those MOSFETs whose channel length is of the same magnitude as the dimensions of the source / drain depletion regions.

6) Tunneling :

Tunneling is the conduction of current through the gate terminal. Significant in short channel MOSFETs.

## → Parametric Extraction :-

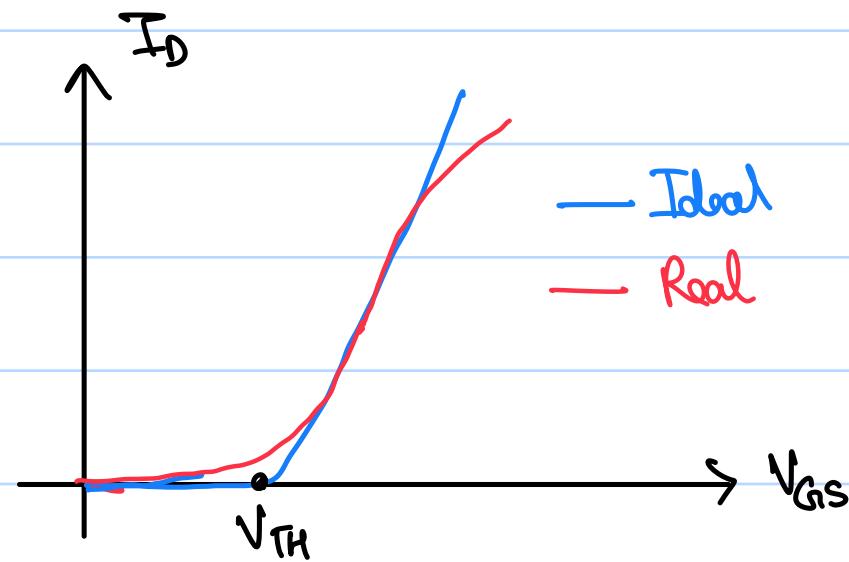
- $V_{GS} \geq V_T$  and  $V_{DS} \ll (V_{GS} - V_T)$  [Deep Trickle]

$$\Rightarrow I_D = \mu_n C_o \frac{w}{L} (V_{GS} - V_{TH}) V_{DS}$$

is of the form  $y = m(x - x_0)$  [I<sub>D</sub> v/ V<sub>GS</sub> sweep]

$x_0$  is the x intercept of the line

$\therefore V_{TH}$  is the x intercept of the above line



We take the point of maximum slope to construct the line equation, to avoid mobility reducing second order effects.

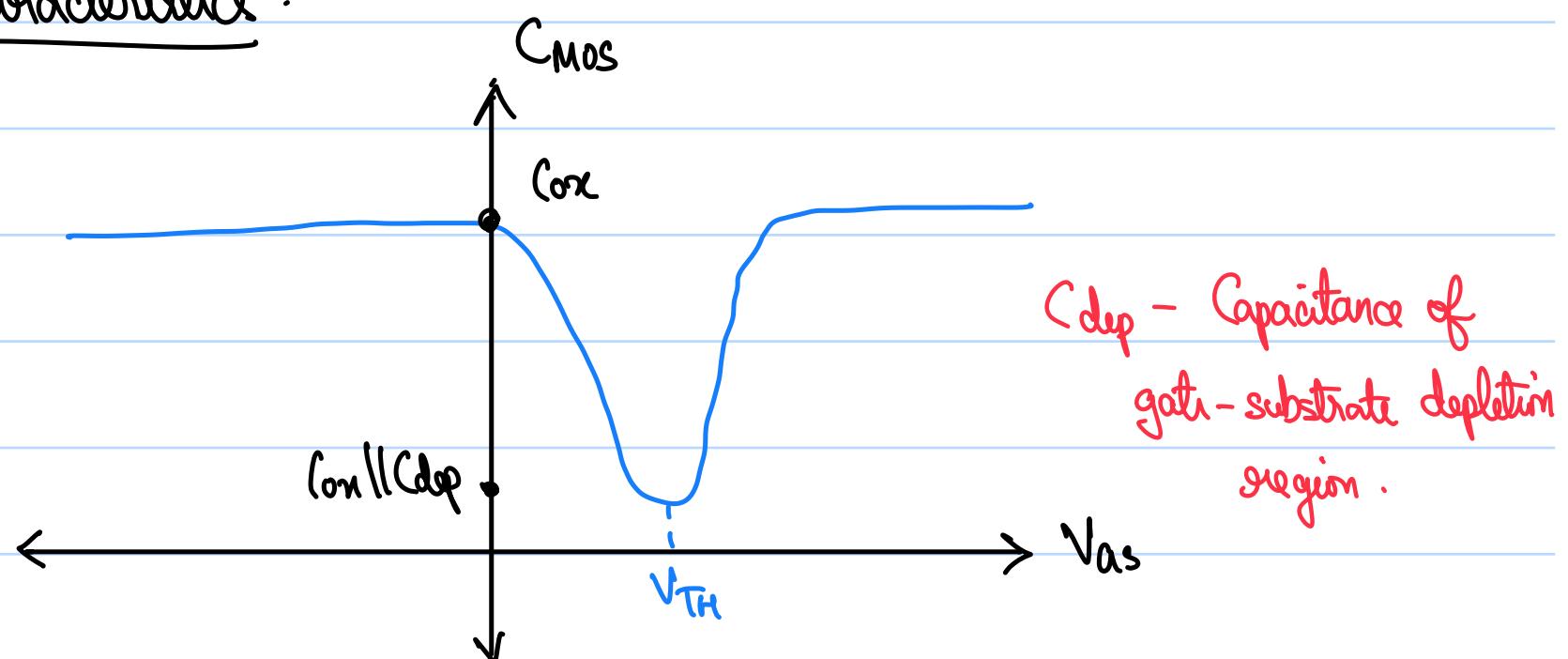
$$\mu = \frac{\mu_0}{1 + \Theta(V_{GS} - V_{TH})}$$

If  $V_{GS} \approx V_{TH}$

$$\mu = \frac{\mu_0}{1 + \Theta(V_{GS} - V_{TH})} \approx \underline{\underline{\mu_0}} \quad [\text{Maximum value}]$$

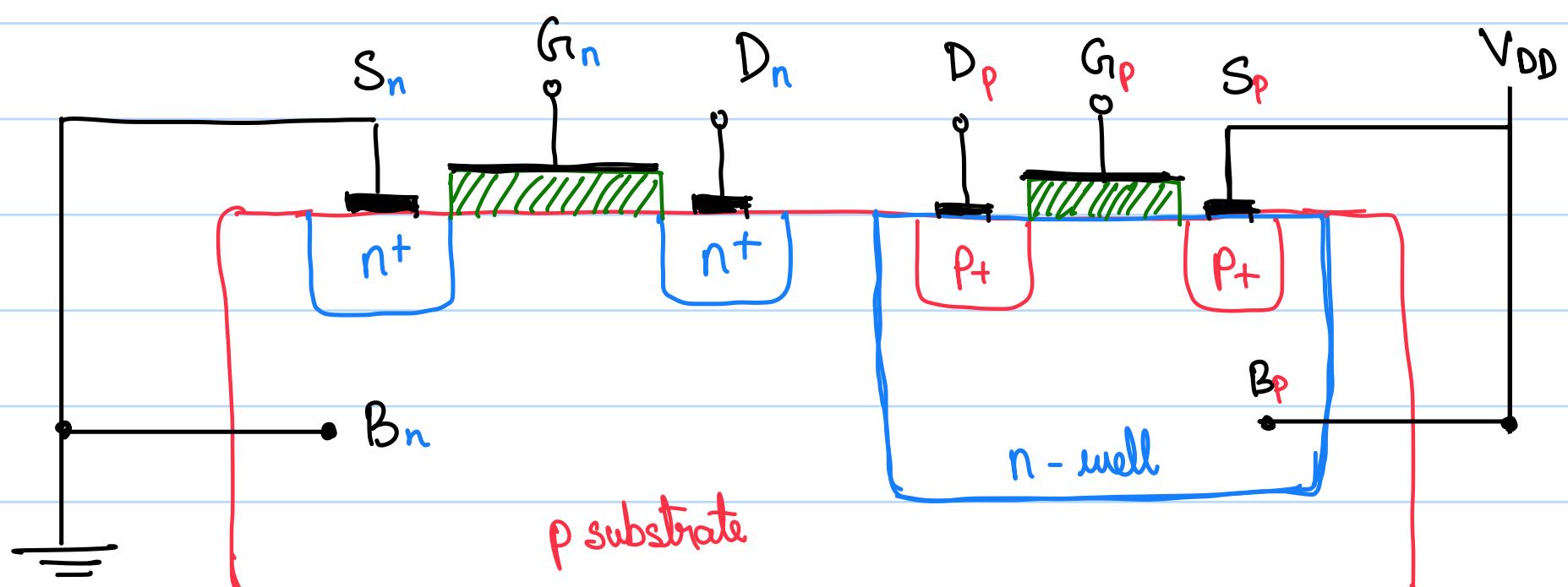
The effect of all the second order effects is modelled using  $\Theta$ . So when  $V_{GS} \approx V_{TH}$ , ie at max mobility,  $\Theta$ 's effect is low.

- C-V Characteristics :-



- CMOS Static Logic Devices :-

- CMOS - Complementary MOS (Combination of PMOS and NMOS)



CMOS Structure

(Well settled)

- Static - Well defined op states : Either 0 (gnd) or 1 ( $V_{DD}$ )

- CMOS Devices will have a Pull-up and Pull-down networks in each logic stage.

Pulls op and ip to 0,1 levels

- Purpose of Logic Stage : To evaluate i/p and pull the o/p up or down to match  $V_{DD}$  or GND.
- No static power consumption , ie, while i/p's are unchanged the power consumption is zero. Circuit still draws power when the i/p's are changed , ie, switching power is non-zero. (dynamic power)

- CMOS Inverter :- ( Rabaray's CMOS Design textbook & Weste )

1) Transfer Characteristic (VTC) (output vs input)

2) Noise Margin

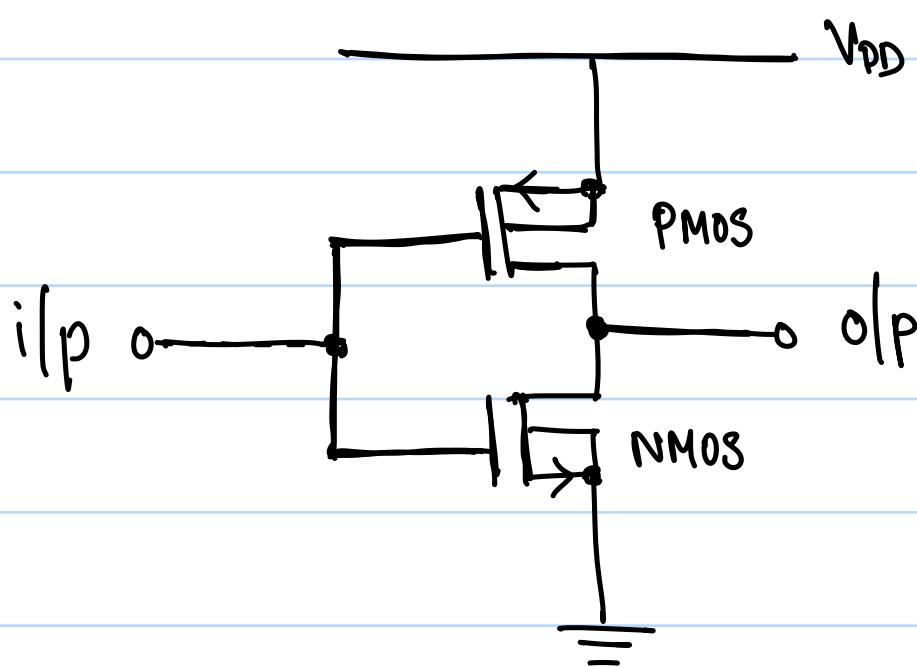
3) Dynamic Characteristics (Rise/fall, time delay)

4) Inverter Design Flow

5) Efficacy

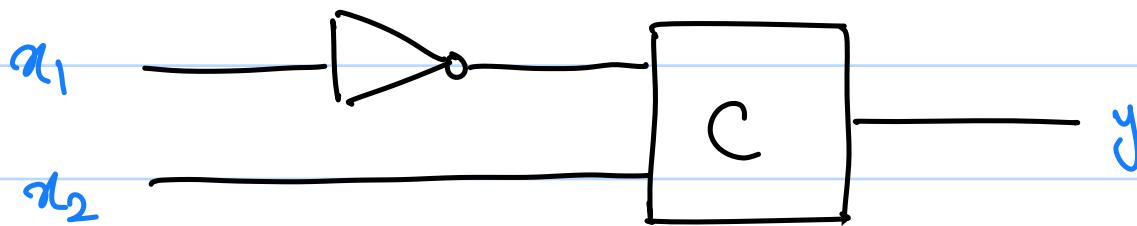
6) Inverter in Other Logics

- Circuit:



- The design procedure of the inverter needs to consider things like time delay, load impedance, output load type, etc.

Example:

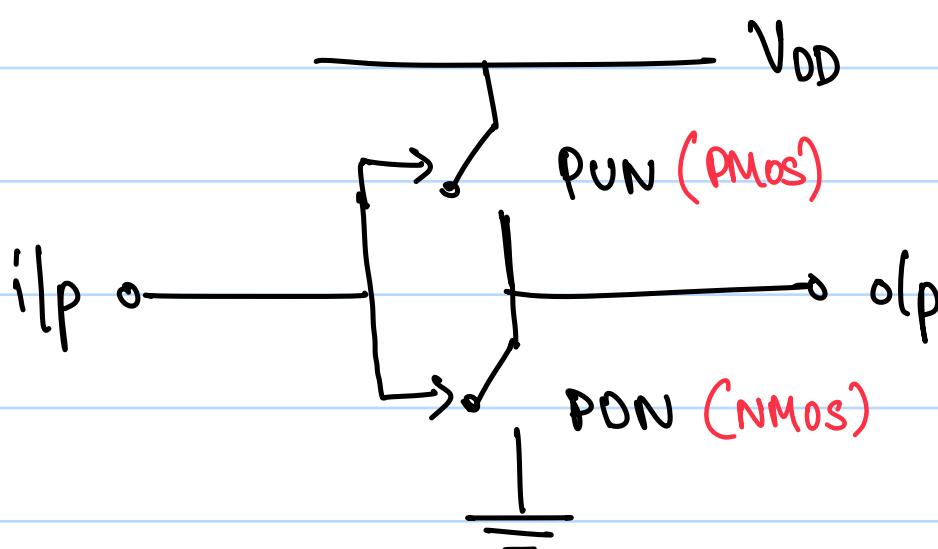


Since the inverter adds some delay,  $x_1$  and  $x_2$  will not reach C at the same time.

- Pull Up and Pull Down Network :-

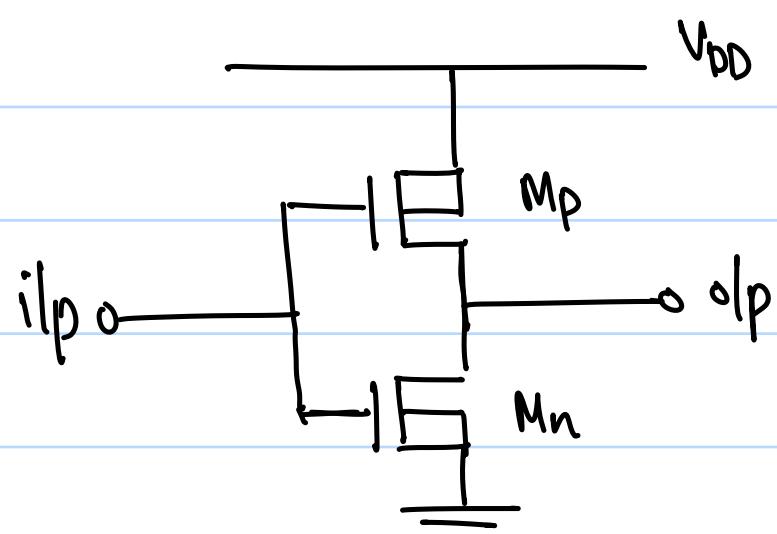
- Pull Up : Pulls ilp to VDD

Pull Down : Pulls ilp to GND



PUN and PDN are never on simultaneously.

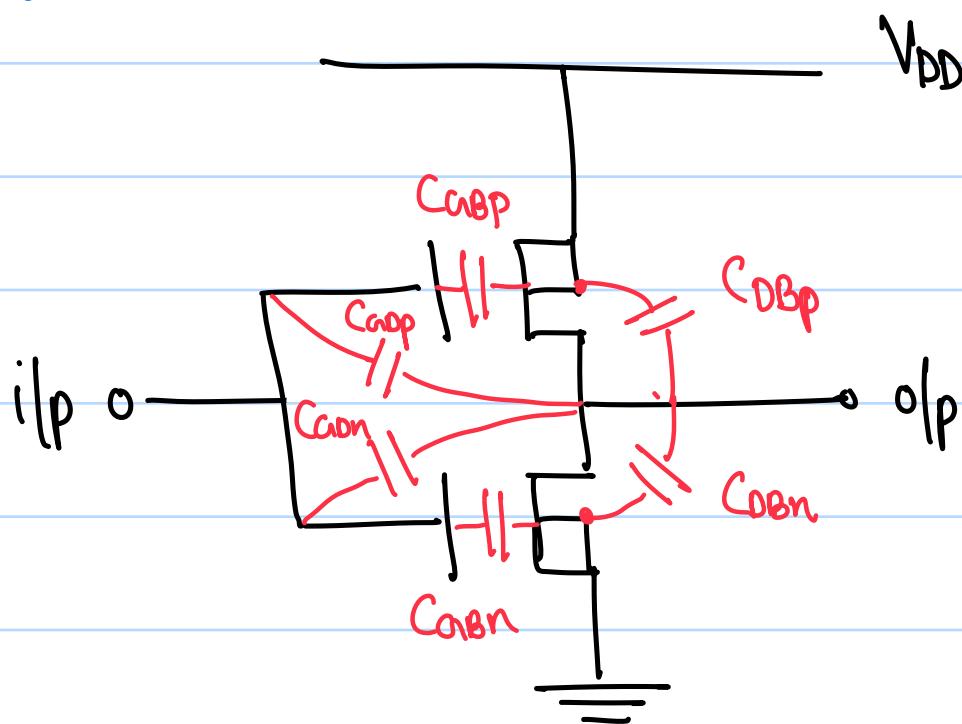
- In the CMOS Inverter,



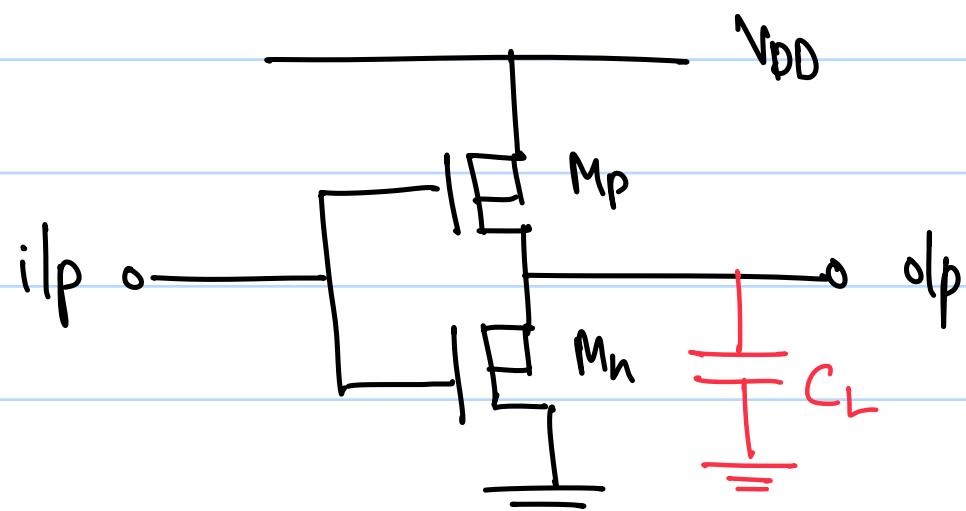
- On condition for  $M_n$  :  $V_{GSn} = V_{ip} \geq V_{Tn}$
- " " " "  $M_p$  :  $V_{Sop} = V_{DD} - V_{ip} \geq |V_{Tp}|$   
 $= V_{ip} \leq V_{DD} - |V_{Tp}|$

Condition	$M_n$	$M_p$	$o/p$
$V_{ip} = 0$	OFF	ON	$V_{DD}$
$V_{ip} = V_{DD}$	ON	OFF	0 } Inverter Behavior $V_{ip} \geq V_{Tn}$ $V_{ip} \leq V_{Tp} + V_{DD}$ $(V_{Tp} \leq 0)$

- Modelling the capacitances in the inverter



Since at the settled state, the voltages are all constant, they can be considered as AC grounds. Therefore the total capacitive impedance can be modelled as a capacitive load.



## Modes of Operation of MOS

Operation Mode	Type	Condition	Equation
Cut-Off	NMOS	$V_{GS} < V_{TH}$	$I_D = 0$
	PMOS	$ V_{GS}  <  V_{TH} $	$I_D = 0$
Linear	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \leq V_{GS} - V_{TH}$	$I_D = K_n(2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2)$
	PMOS	$ V_{GS}  \geq  V_{TH} $ $ V_{DS}  \leq  V_{GS}  -  V_{TH} $	$I_D = K_p(2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2)$
Saturation	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = K_n(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$
	PMOS	$ V_{GS}  \geq  V_{TH} $ $ V_{DS}  \geq  V_{GS}  -  V_{TH} $	$I_D = K_p(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$

Case 1:  $0 \leq V_{ilp} < V_{Th}$

$$M_n : V_{asn} = V_{ilp}$$

$$V_{ilp} \leq V_{Th} \rightarrow M_n \text{ is in cutoff}$$

$$M_p : |V_{asp}| = |V_{ilp} - V_{DD}| = V_{DD} - V_{ilp} \quad (V_{ilp} < V_{DD})$$

$$V_{DD} - V_{ilp} \geq |V_{Tp}| \quad [\text{Assuming } V_{Th} \approx |V_{Tp}|] \quad \text{--- (1)}$$

$$\Rightarrow |V_{asp}| \geq |V_{Tp}|$$

$$|V_{asp}| \approx |V_{DD} - V_{DD}| = 0$$

$$|V_{asp}| - |V_{Tp}| = V_{DD} - V_{ilp} - |V_{Tp}| > 0 \quad [\text{Assuming } V_{DD} > 2|V_{Tp}|]$$

$$\Rightarrow |V_{asp}| \leq |V_{asp}| - |V_{Tp}| \rightarrow M_p \text{ is in linear mode}$$

Case 2:  $V_{Th} \leq V_{ilp} < V_{DD}/2$   $\rightarrow V_{ilp} < V_{DD}$  [Take  $V_{ilp} \approx V_{ilp}$ ]

$$M_p : |V_{asp}| = |V_{ilp} - V_{DD}| = V_{DD} - V_{ilp}$$

$$V_{DD} - V_{ilp} \geq |V_{Tp}| \quad [\text{By Assn. (2)}]$$

$$V_{DS} = V_{ilp} - V_{DD} < 0 \quad [V_{ilp} < V_{DD}]$$

$$\Rightarrow |V_{DS}| \approx 0 \Rightarrow |V_{DS}| < |V_{asp}| - |V_{Tp}| \quad \xrightarrow{\text{Mp is linear}}$$

$$M_n : V_{asn} = V_{ip}$$

$$V_{ip} \geq V_{Tn}$$

$$V_{bsn} \approx V_{DD} \Rightarrow V_{bsn} \geq V_{asn} - V_{Tn} \rightarrow M_n \text{ is in Saturation}$$

$$\text{Case 3: } V_{in} = V_{DD}/2 \rightarrow V_{ip} \approx V_{DD}/2$$

$$M_n : V_{asn} = \frac{V_{DD}}{2} \geq V_{Tn} \quad [\text{Assn ②}]$$

$$V_{bsn} = \frac{V_{DD}}{2}$$

$$\frac{V_{DD}}{2} \geq \frac{V_{DD}}{2} - V_{Tn} \rightarrow M_n \text{ is in Saturation}$$

$$M_p : |V_{asp}| = \left| \frac{V_{DD}}{2} - V_{DD} \right| = \frac{V_{DD}}{2} > V_{Tp}$$

$$|V_{asp}| = \left| \frac{V_{DD}}{2} - V_{DD} \right| = \frac{V_{DD}}{2}$$

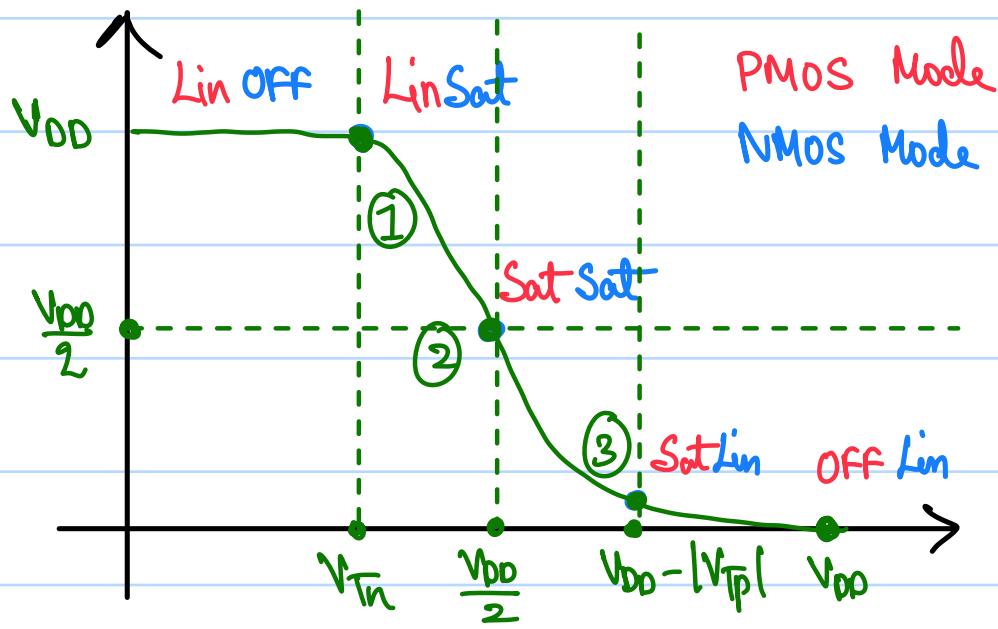
$$\frac{V_{DD}}{2} > \frac{V_{DD}}{2} - |V_{Tp}| \Rightarrow |V_{asp}| \geq |V_{asp}| - |V_{Tp}| \rightarrow M_p \text{ is in Saturation}$$

III proof can be stated for  $V_{DD}/2 < V_{ip} < V_{DD} - |V_{Tp}|$  and  $V_{DD} - |V_{Tp}| < V_{ip}$ .

∴ The VTC of the CMOS Inverter can be summarized as,

Condition	M <sub>p</sub>	M <sub>n</sub>	O/p
$0 \leq V_{in} \leq V_{Tn}$	Lin	OFF	$V_{DD}$
$V_{Tn} \leq V_{in} < \frac{V_{DD}}{2}$	Lin	Sat	$< V_{DD}$
$V_{in} = \frac{V_{DD}}{2}$	Sat	Sat	$\frac{V_{DD}}{2}$
$\frac{V_{DD}}{2} < V_{in} < V_{DD} -  V_{Tp} $	Sat	Lin	$< \frac{V_{DD}}{2}$
$V_{DD} -  V_{Tp}  < V_{in}$	OFF	Lin	0

This switching point is valid if  $V_{in} = |V_{Tp}|$



Note: By KCL, currents through both the MOSFETs will always be equal in the 3 intermediate points (LinSat SatSat SatLin)

At ① (LinSat)

$$I_{Dp\ lin} = I_{Dn\ sat}$$

$$= K_p \left[ (V_{SD} - |V_{Tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right] = \frac{1}{2} K_n (V_{SD} - V_{Tn})^2$$

$$= K_p \left[ (V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{Dp}) - \frac{(V_{DD} - V_{Dp})^2}{2} \right] = \frac{K_n}{2} (V_{Dp} - V_{Tn})^2$$

On Solving, we will get, (Take  $V_{DD} - V_{Dp} = y$ ,  $V_{Dp} - V_{Tn} = x$  easy)  
and  $K_n = K_p$

$$V_{Dp} = (V_{Dp} + |V_{Tp}|) \pm \sqrt{(V_{DD} - V_{Tn} - |V_{Tp}|)(V_{DD} - 2V_{Dp} + V_{Tn} - |V_{Tp}|)}$$

Since  $V_{Dp} \approx V_{DD}$  near ①,

$$V_{Dp} = (V_{Dp} + |V_{Tp}|) + \sqrt{(V_{DD} - V_{Tn} - |V_{Tp}|)(V_{DD} - 2V_{Dp} + V_{Tn} - |V_{Tp}|)}$$

$$\text{Conditions : } V_{DD} \geq V_{Tn} + |V_{Tp}|, V_{Dp} \leq \frac{V_{DD} + V_{Tn} - |V_{Tp}|}{2}$$

Therefore, the operating requirements of a CMOS inverter are:

$$1) V_{DD} \geq V_{Th} + |V_{Tp}| \quad 2) V_{ilp} \leq \frac{V_{DD} + V_{Th} - |V_{Tp}|}{2}$$

