VLSI Design : Assignment-3

Monsoon 2025, IIIT Hyderabad (Instructor: Abhishek Srivastava)

Release date: 9^{th} October; Due date : 18^{th} October, 2025 (18:00 hrs)

Instructions:

1. Submit your assignment as a single file in pdf format (Name_RollNo.pdf)
2. Use the given 180 nm technology file for the NGSPICE simulations
3. Consider lengths of NMOS and PMOS to be equal ($L_n = L_p$), and $V_{DD} = 1.8V$ until stated otherwise
4. Use 'set curplottitle= Your-name-roll-question-number-part' for every plot in your report so that it is printed on the top of each plot
5. Answers should be complete and must be presented in a systematic way with explanation, plots, annotations net-lists and HDL description
6. Utilize moodle platform to discuss and clear your questions. Discussion is highly encouraged.

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1. Simulate Pseudo-NMOS inverter. Plot VTC, transient response ($V_{OUT}(t)$ for square wave input $V_{IN}(t)$). Also plot current drawn from supply for one cycle. Comment on static power dissipation of Pseudo-NMOS inverter. Consider minimum size devices and load capacitance of 10 fF.

2. Simulate an NMOS pass transistor based 2 input multiplexor and observe the minimum and maximum voltage levels at the output. As discussed in the class, add a CMOS inverter (W_N, $W_P = \frac{\mu_N}{\mu_P} \times W_N$) at the output of the MUX and check if the logic levels are restored or not. Find rise and fall time at the output of the inverter. Plot the leakage current drawn by CMOS inverter when its input is close to $VDD - V_{TN}$. Put a Weak-Keeper as discussed in the class to overcome the leakage current problem and verify with the simulation results.

3. Size the pass transistor logic based multiplexor shown in Fig. 1 such that the average delay from input (A or B) to output (Y) is minimized. It is given that the electrical effort (C_{out}/C_{in}) for each path (input to output) is 2. Length of each transistor in the circuit is same (L=0.18 μm). Widths shown in the figure represents the ratio of PMOS and NMOS devices. There is a constraint for the output inverter that the total width $W_p + W_n = 6W$. Use NGSPICE simulations by including parasitic capacitances of the devices to find the sizes to minimize the delay. For your final design, show the functionality of the multiplexor with appropriate waveforms and report the delay of your circuit.

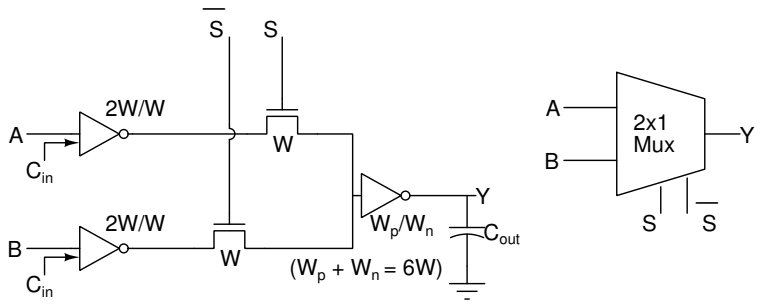

Figure 1

4. Use the 2×1 multiplexor (only) shown in Fig. 2 and implement the following logic function *(Hint: Use Shanon's expansion.)*:

$$f = x_1x_2 + x_1x_3 + x_1x_4 + x_2x_3 + x_2x_4 + x_3x_4$$

Each input (x_1 to x_4) should see a high input impedance (goes to gates of pass transistors) and the load capacitance at the output is equivalent to 4 times the minimum sized inverter. Use the same size (W) for pass transistor obtained in the previous problem.

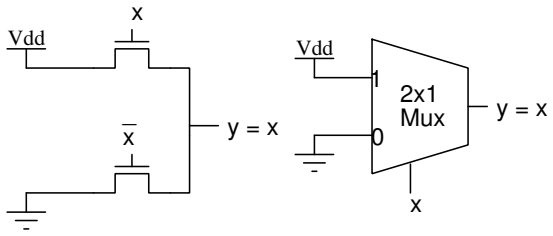

Figure 2

(a) Give the circuit diagram

(b) Write the spice netlist for the circuit and verify the functionality with simulations. Attach your plots.

(c) Find the minimum transition time taken by output (f) to change from - i) 0 to 1 (t_{PLH}) and ii) 1 to 0 (t_{PHL}). Clearly mention the input combination and paths for charging and discharging the output in your circuit.

(d) Do you observe any difference in t_{PLH} and t_{PHL}. If yes, then can you suggest some modification in your circuit to make them nearly equal. *(Hint: Charging path (V_{DD} to out) and discharging path (out to ground) should have equal number of transistors of same size. Repeaters (inverters) can be inserted at appropriate nodes to achieve the same.)*
