Prof: Abishek Srivastava, CVEST

23 Lectures
– 39 hours

Grading:

Assignment (3/4) : 10%

Course Project : 20%

Quiz : 10% + 10%

Midsem : 20%

Endsem : 30%

VLSI Design

Assignment Deadlines : 6pm

VLSI Design

→ **Topics:-**

1) Intro to VLSI Design

2) CMOS Inverter

3) Multi-stage Logic Design and Optimization

4) Other logic styles

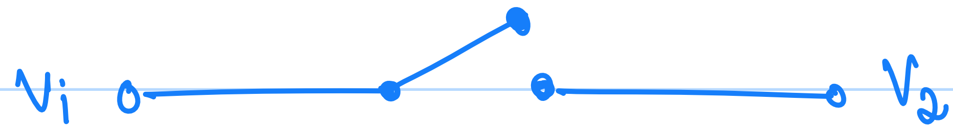
5) Intro. to HDL System Design.

- SCL - Semiconductor Complex Limited. Only Fabrication facility in India. Can do upto 180 nm CMOS. Located in Mohali.
  ↳ Considered a very old technology.

- We will be using 180 nm technology in this course, since it is now open-source.

→ **High impedance state :-**

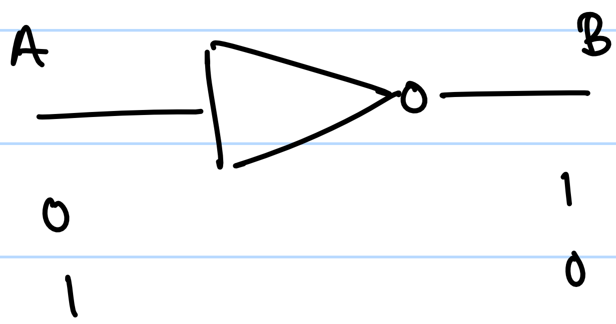
- When a node is not connected to any well defined voltage, it is said to be existing in a high impedance state.



V_2 is in a high impedance state.

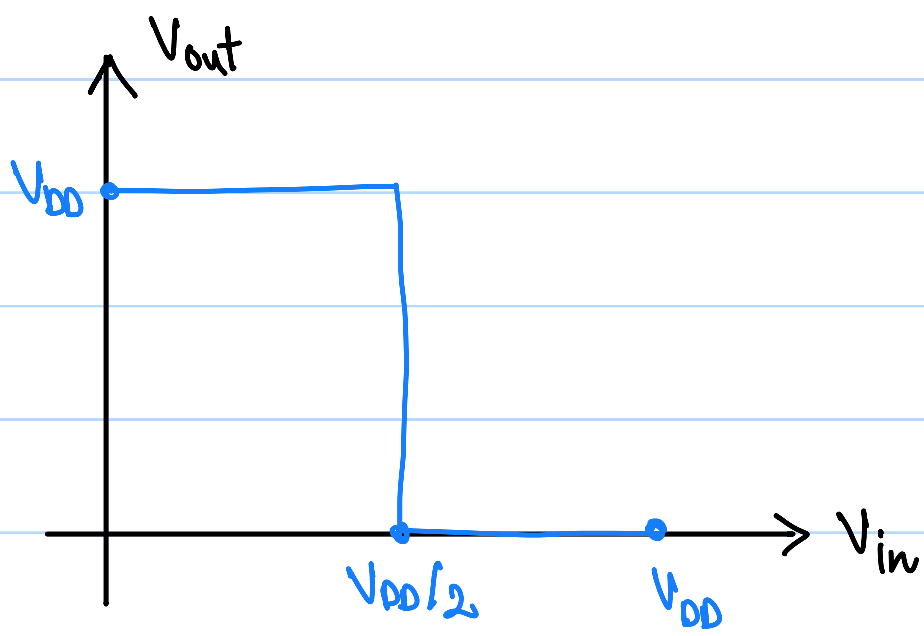
(Refer Weste & Harris MOS T Physics for today's lecture) 5/8/25

→ **Inverter :-**



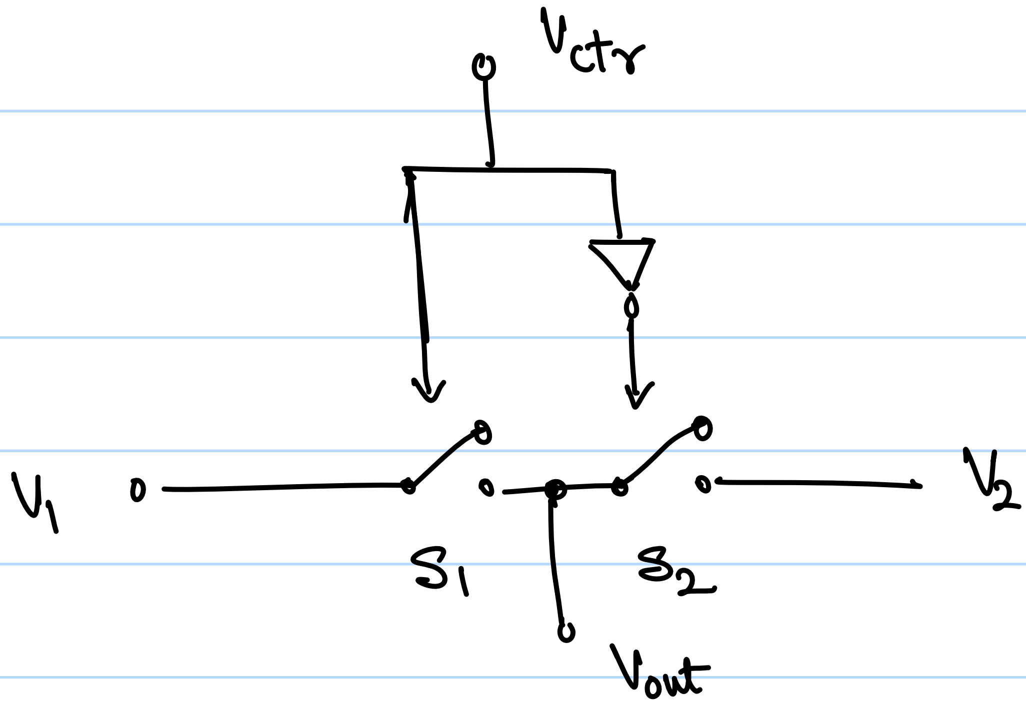
A	B
0	1
1	0

- 1 and 0 correspond to 2 different voltage levels.
- Ideally,



The above plot is termed as a VTC plot (Voltage Transfer Characteristics).

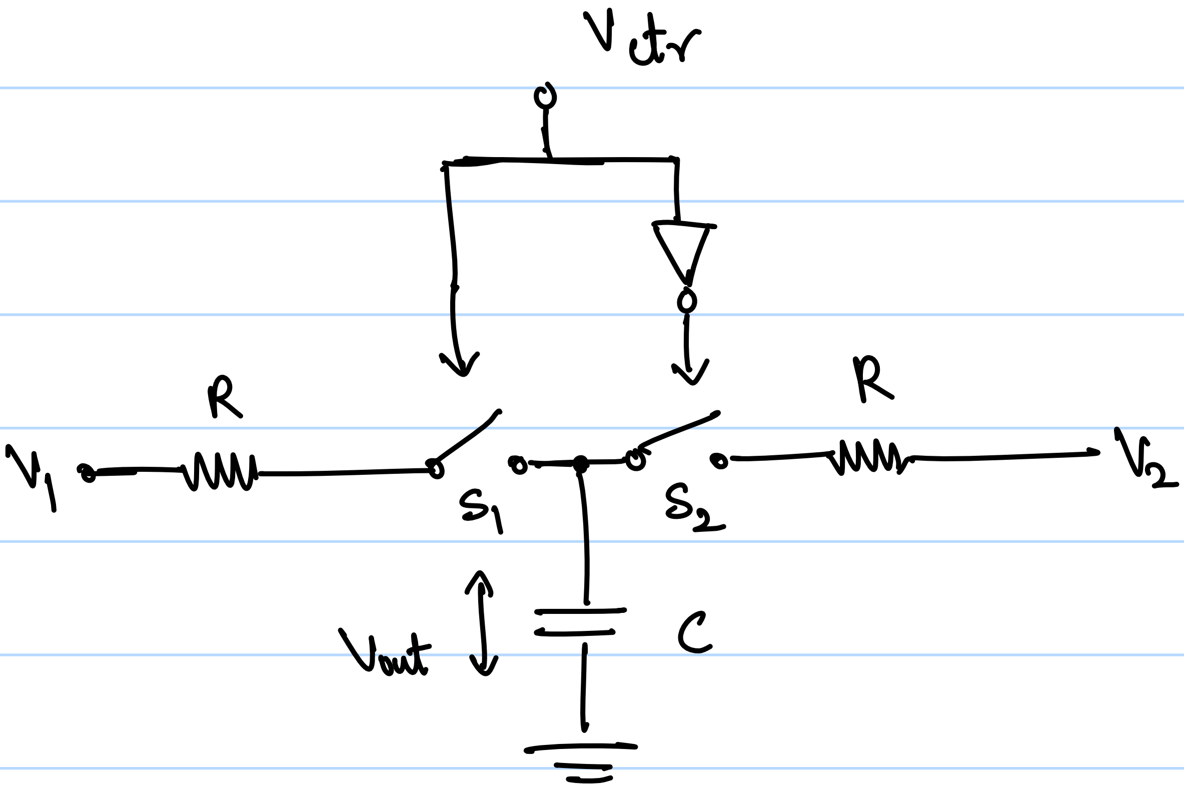
1)



Truth Table:

V_{ctr}	V_{out}
0	V_2
1	V_1

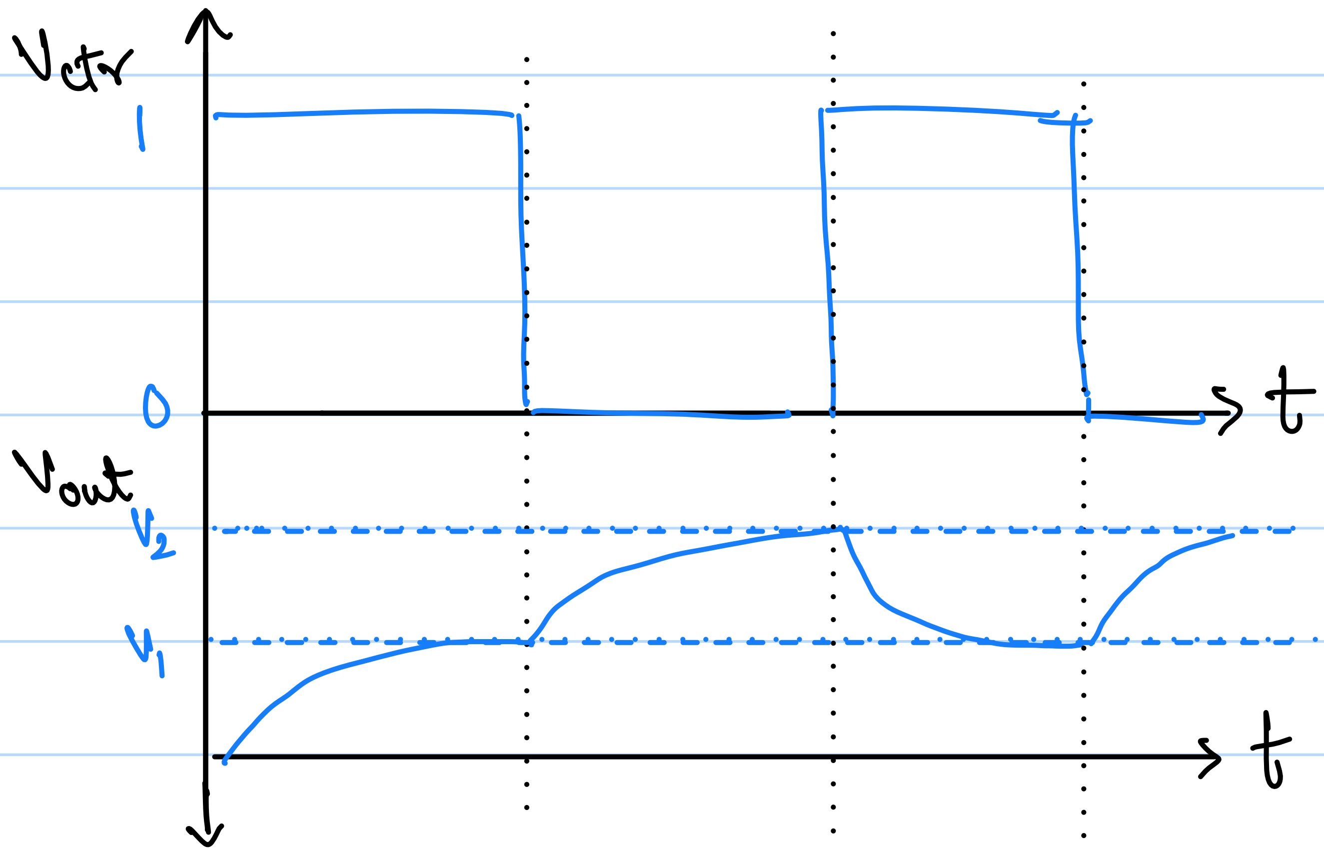
2)



Here,
$$V_{out} = \begin{cases} V_2\left(1 - e^{-t/RC}\right), & V_{ctr} = 0 \\ V_1\left(1 - e^{-t/RC}\right), & V_{ctr} = 1 \end{cases}$$

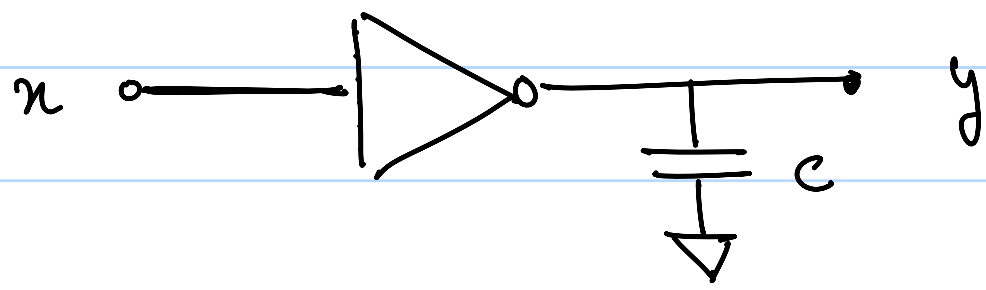
If there is no resistance involved, the current through the capacitor will be a Dirac impulse, infinite for an infinitesimal time.

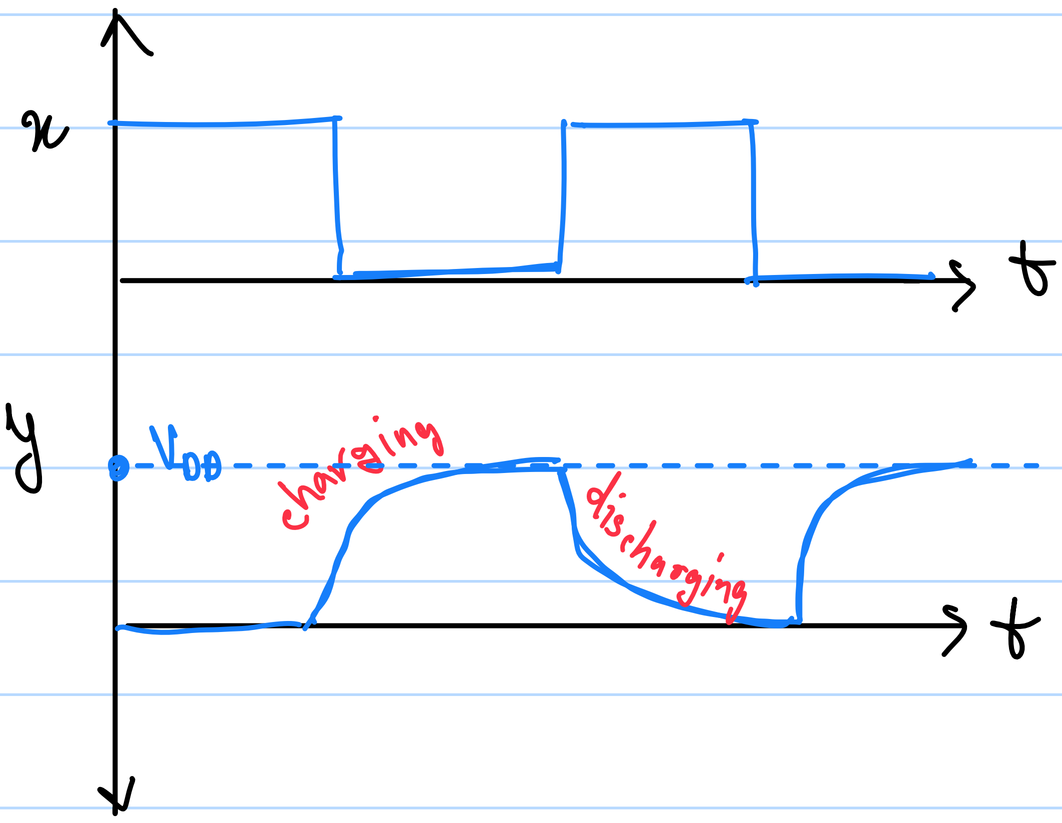
($i = C\frac{dV}{dt}$, dt is very small)



This is a timing diagram

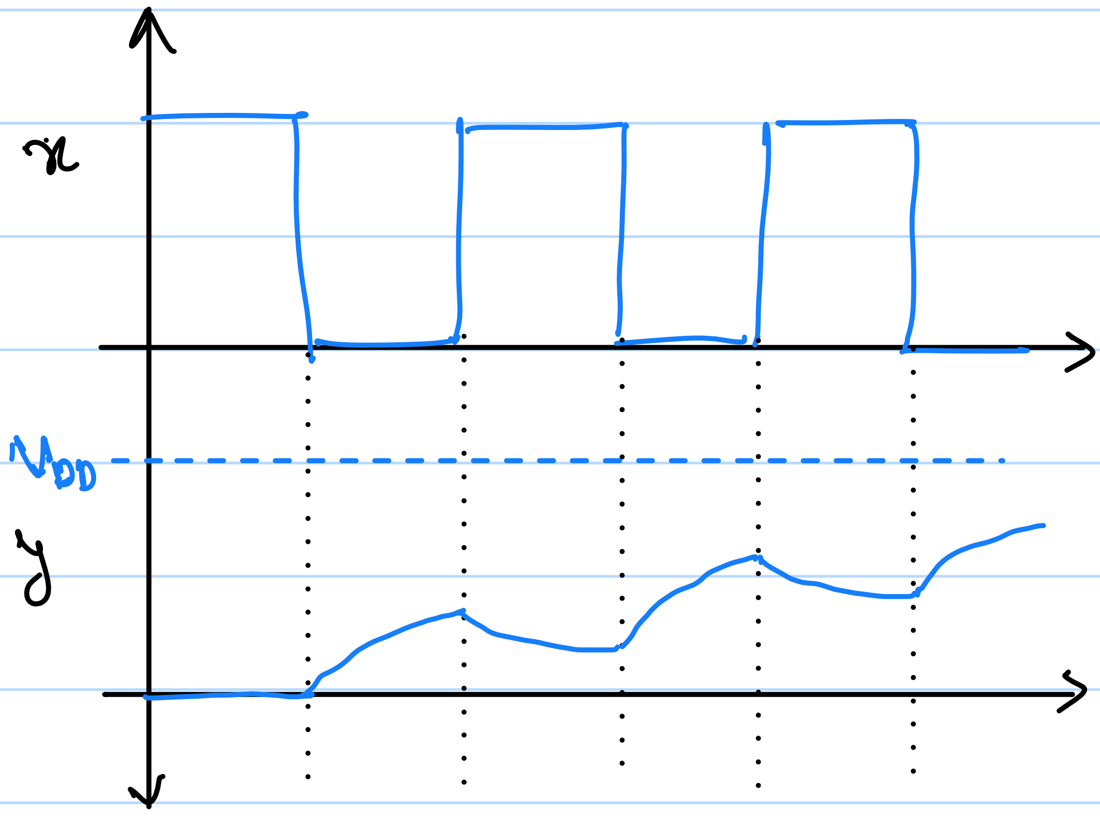
3)





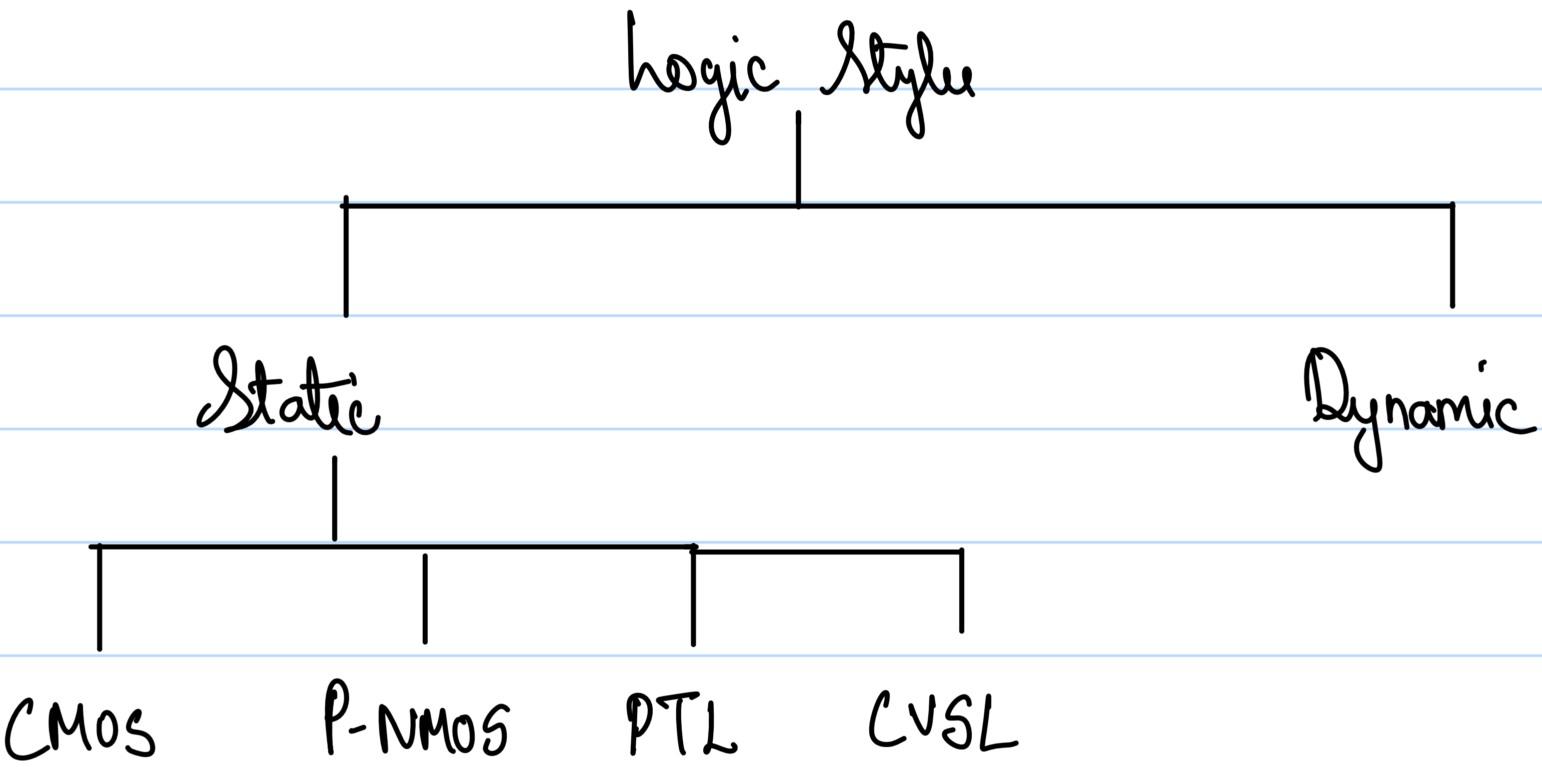
- The charging and discharging speeds of the capacitor are dependent on the RC / time constants of the circuit.

If RC is very large,



The capacitor is not fast enough to reach V_{DD} and zero, so information is lost.

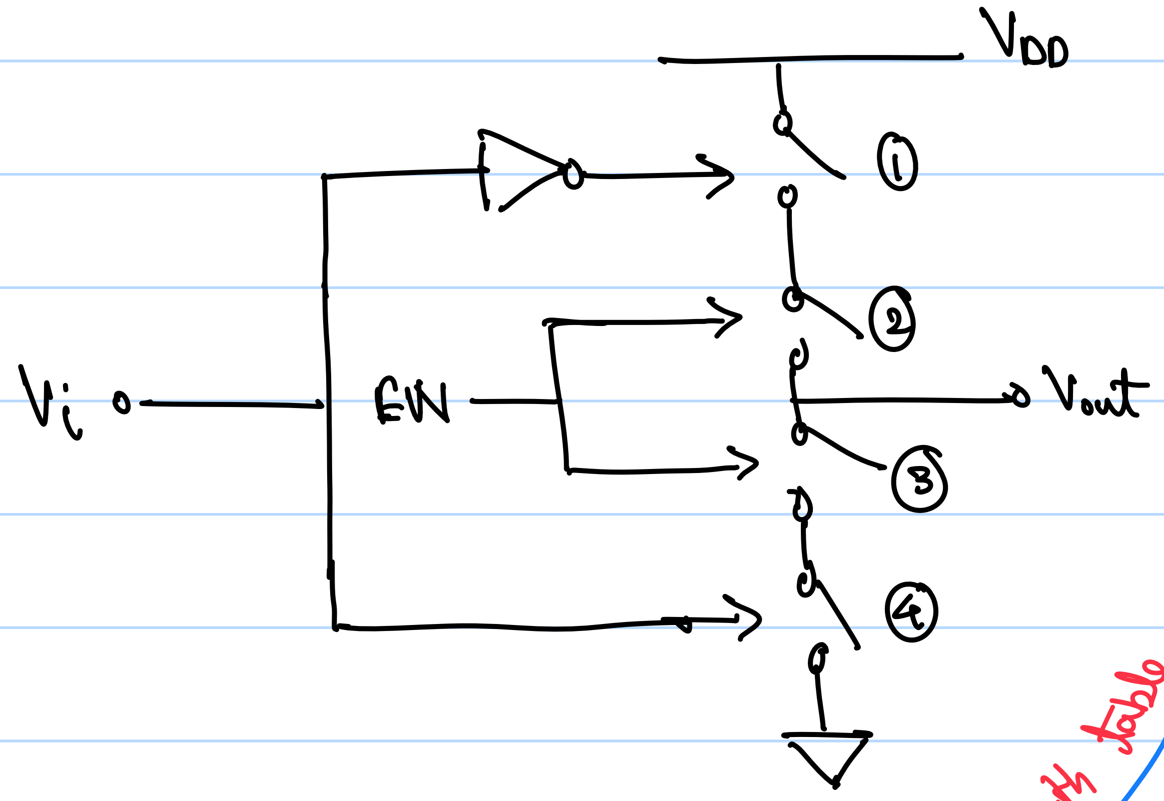
- Because of this, the RC parameter of the circuit must be fast enough to handle the input speed/ frequency.



Circuit Design

- Combinational
- Sequential
- Memory

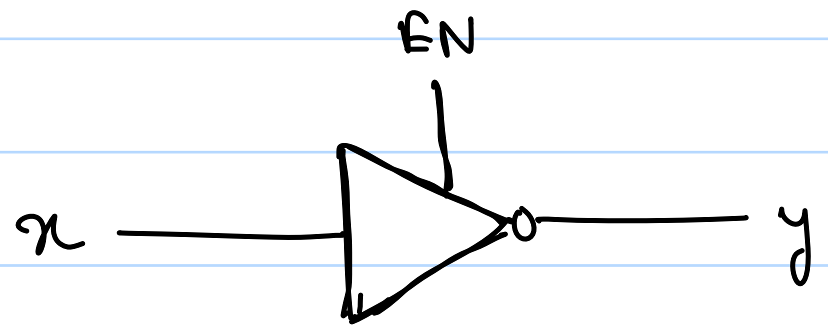
4)



truth table

EN	V_i	V_o
0	0	Z
0	1	Z
1	0	V_{DD}
1	1	0

- The above device acts like an inverter if EN = 1. This is the design of a tri-state inverter.



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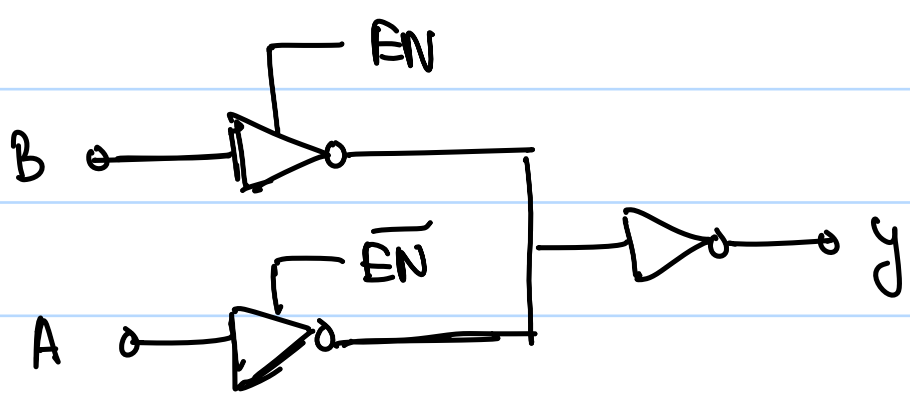
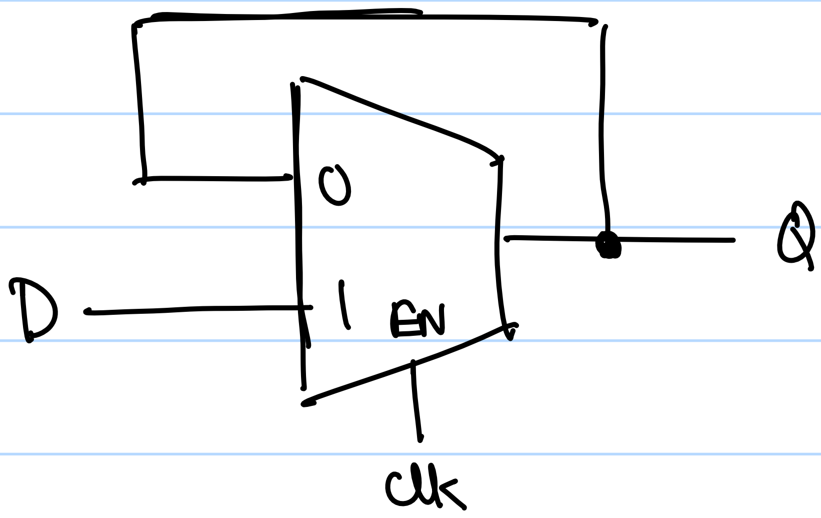


Truth table :

EN	y
0	A
1	B

- Due to the high impedance, the output of one tri-state inverter will not be affected by the other, since one output is always Z.

- The above device will act as a 2x1 MUX, which can be used to design devices like gates and latches.



Level Triggered D-Latch

→ SPICE :-

Ckt. Description → SPICE → Simulation (.ac, .tran, .op)

Netlist | Schematic
(Lowest level)

R1 A B <R1 value>

R2 B C <R2 value>

Model file | Library ← PDK ← Foundry (TSMC, etc)

Process Development Kit

Details | Parameters of components

.include <filename>

→ Technology Node:

- To make a semiconductor chipset on a substrate, we use a "stencil" of the circuit layout.

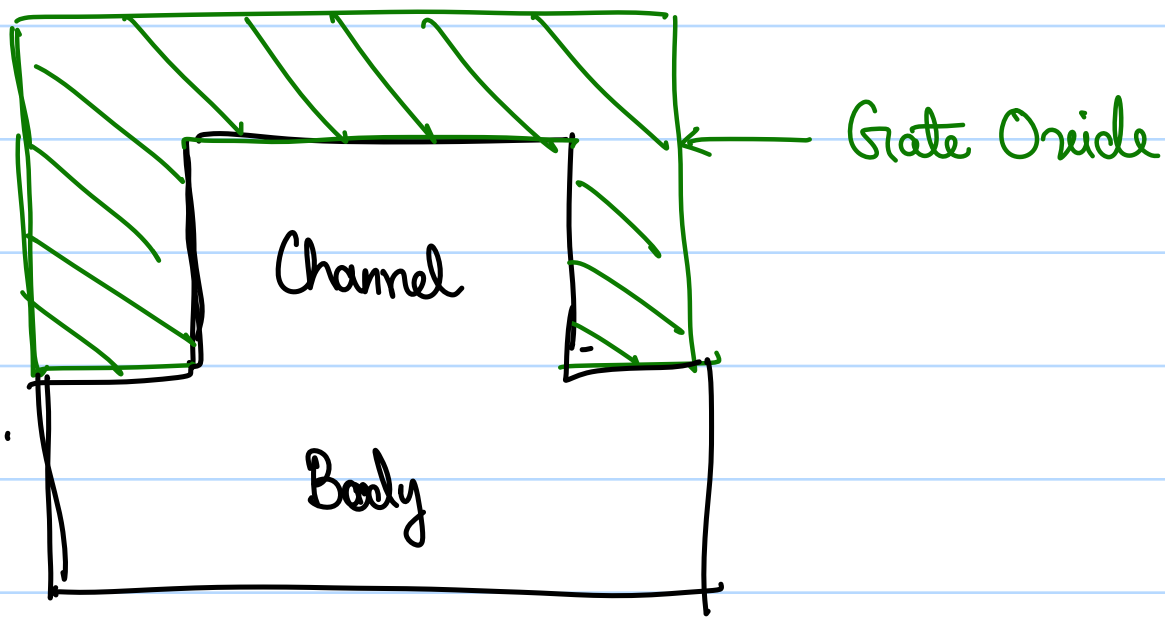
- In the chipset, there are multiple metal layers on top of the substrate, to provide the interconnections between the MOSFETs.

- Within the MOSFETs, there are multiple dimensions that vary between them, depending on the usage of that MOSFET.

- The minimum of those dimensions, i.e., minimum feature length among the MOSFETs is deemed as the "technology node" of that MOSFET. Usually minimum channel length.

- 3nm (N3) node – Retail products released
  2nm (N2) node – Will release early next year.

- < 22nm - FinFETs are used instead of MOSFETs.



View of FinFET through Source / Drain

In FinFETs, the oxide wraps around the channel, enabling better inversion at a lower gate potential, better than MOSFETs.

- A14 - 1.4nm node } In development.
  A7 - 0.7nm node

- 180 nm is still widely used, in devices that do not require extremely high computation.

- Lower transistor size => lower Cost per transistor.

- <u>Clock Speed</u>:

- Recently the clock speed of processes has saturated.

- Since the packing density has increased by a lot, the heat and leakage of the transistors have increased by a lot.

- These factors made it difficult for clock speed to improve as fast as the technology node.

→ <u>Shannon's Expansion</u> :-

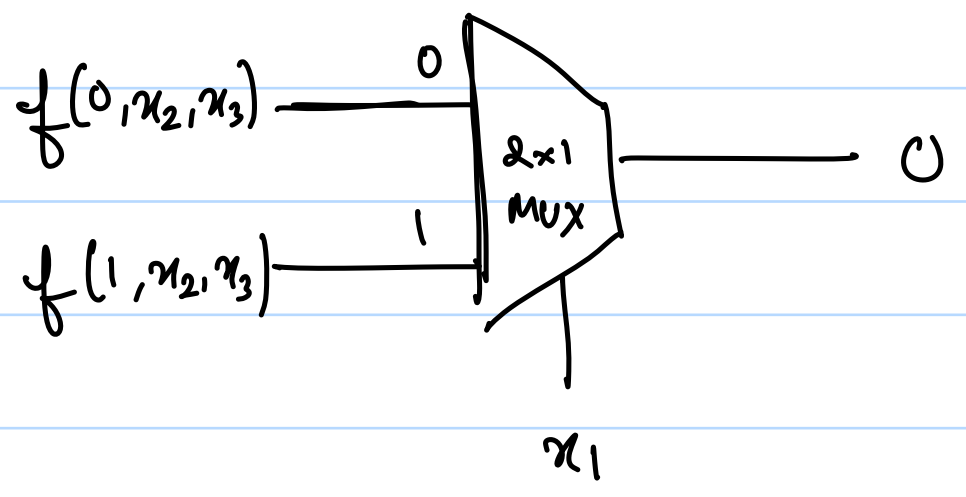
- For any function $f(x_1, x_2, x_3 \dots x_n)$,

$$f(x_1, x_2, x_3 \dots x_n) = x_1 f(1, x_2, x_3 \dots x_n) + \overline{x_1} f(0, x_2, x_3 \dots x_n)$$

<u>Example:</u> Expand $f(x_1, x_2, x_3) = \overline{x_1}\,\overline{x_3} + x_1 x_2 + x_1 x_3$ wrt x_1

$$\Rightarrow f(x_1, x_2, x_3) = x_1 (x_2 + x_3) + \overline{x_1} (\overline{x_3})$$

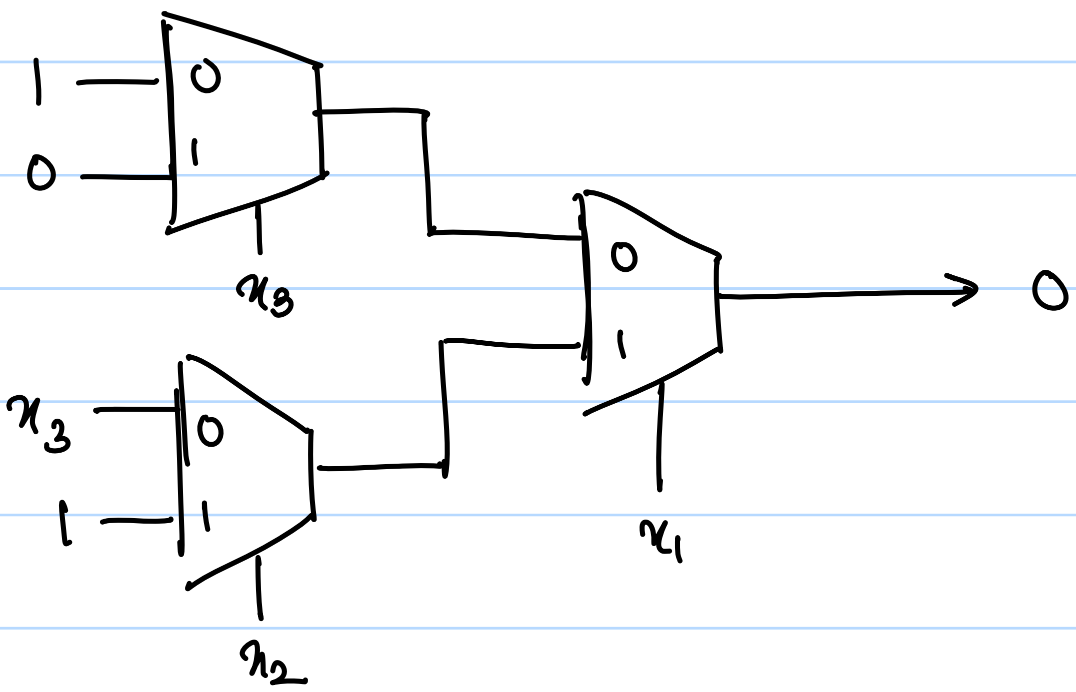
- If we expand the function in this way, we can use a 2×1 MUX to express the function, using x_1 as the selection variable.



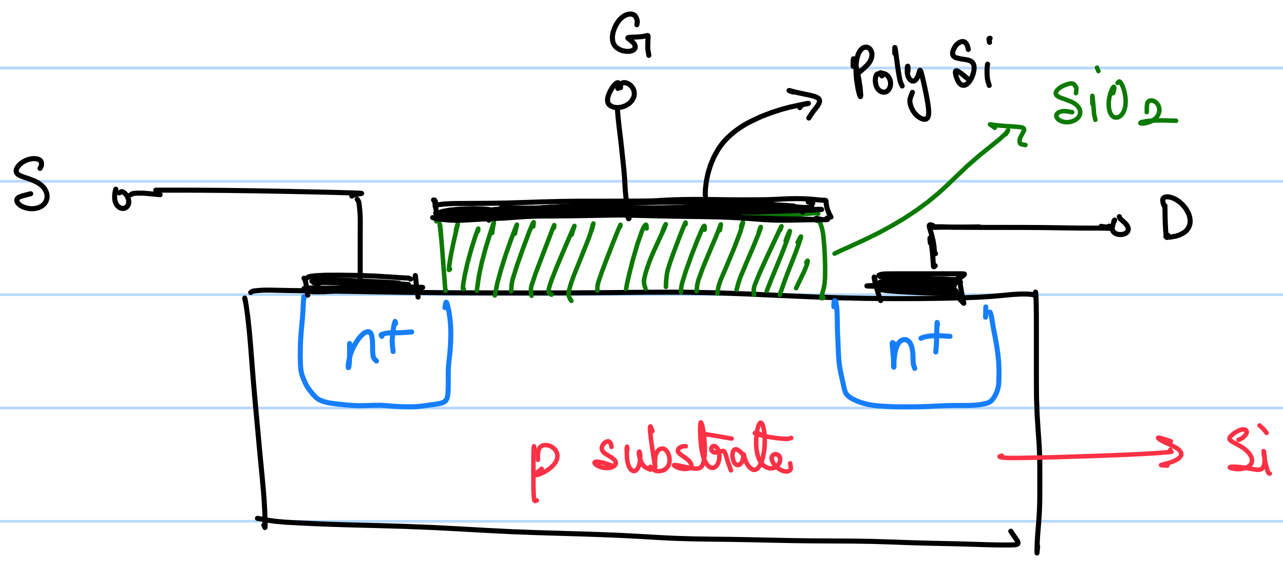
Example: Express the prev. function only using 2x1 MUXes.

$$f(x_1, x_2, x_3) = \overline{x_1}\,\overline{x_3} + x_1 x_2 + x_1 x_3$$
$$= x_1 (x_2 + x_3) + \overline{x_1} (\overline{x_3})$$

$$f(x_2, x_3) = x_2 + x_3$$
$$= x_2 (1) + \overline{x_2} (x_3)$$



→ **MOSFETs** :-

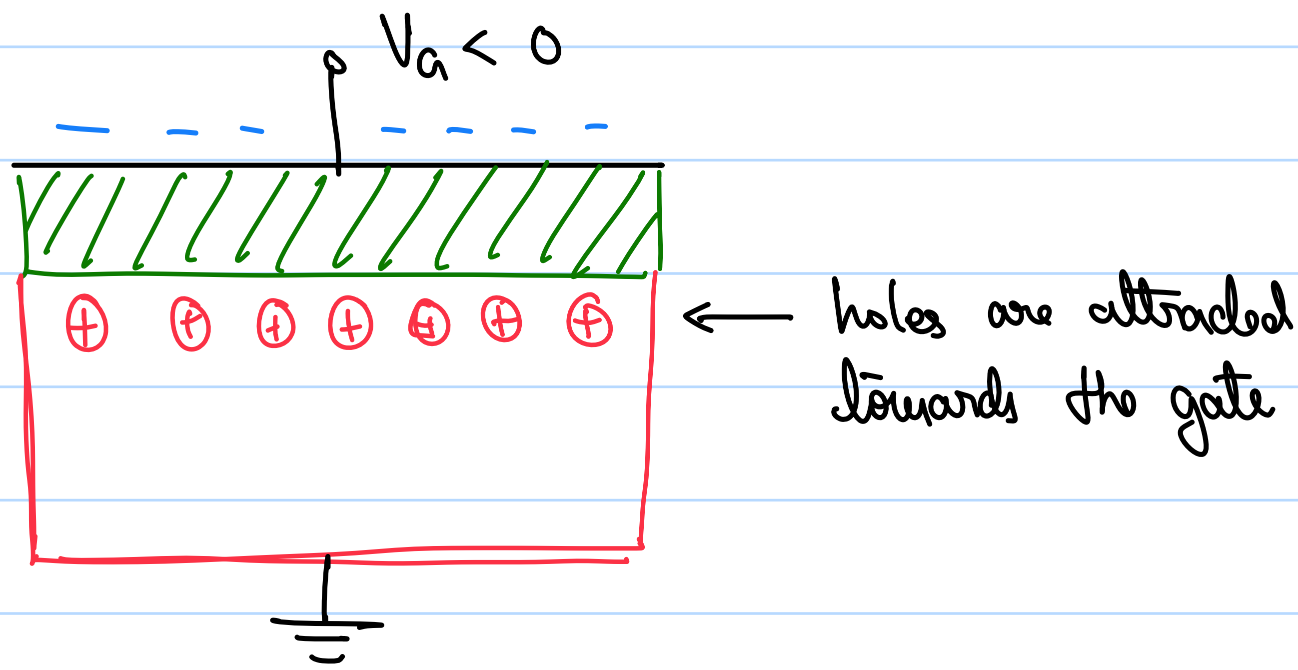


NMOS Structure

- Poly silicon is used in the gate terminal to simplify the manufacturing process, since silicon is the major element of a MOSFET.

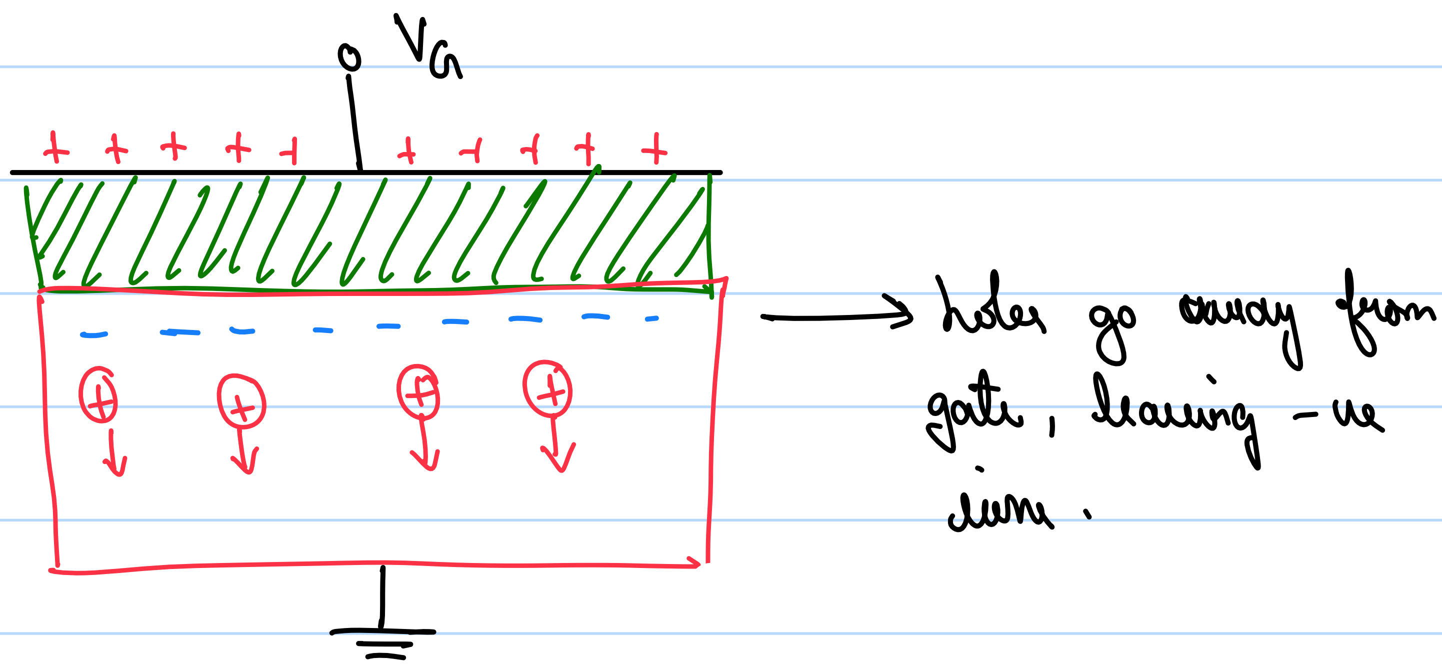
- Let S and D be grounded and,

1) $V_G < 0$



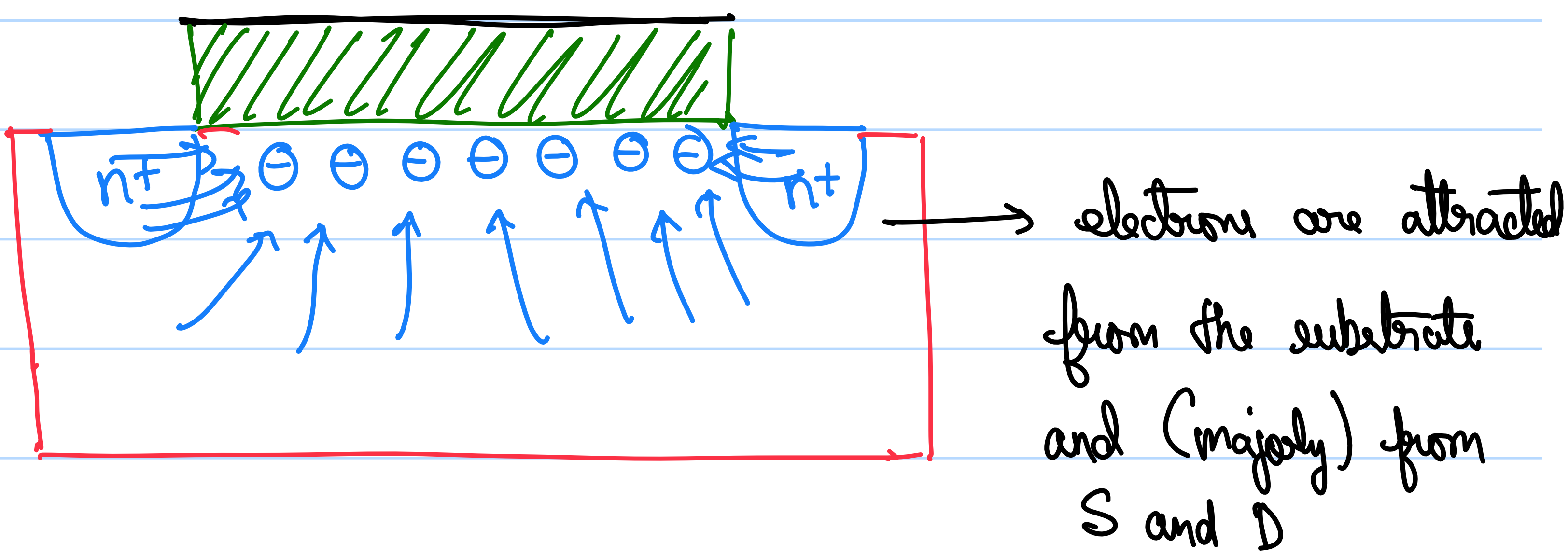
- This is accumulation mode of operation.

2) $V_G > 0$

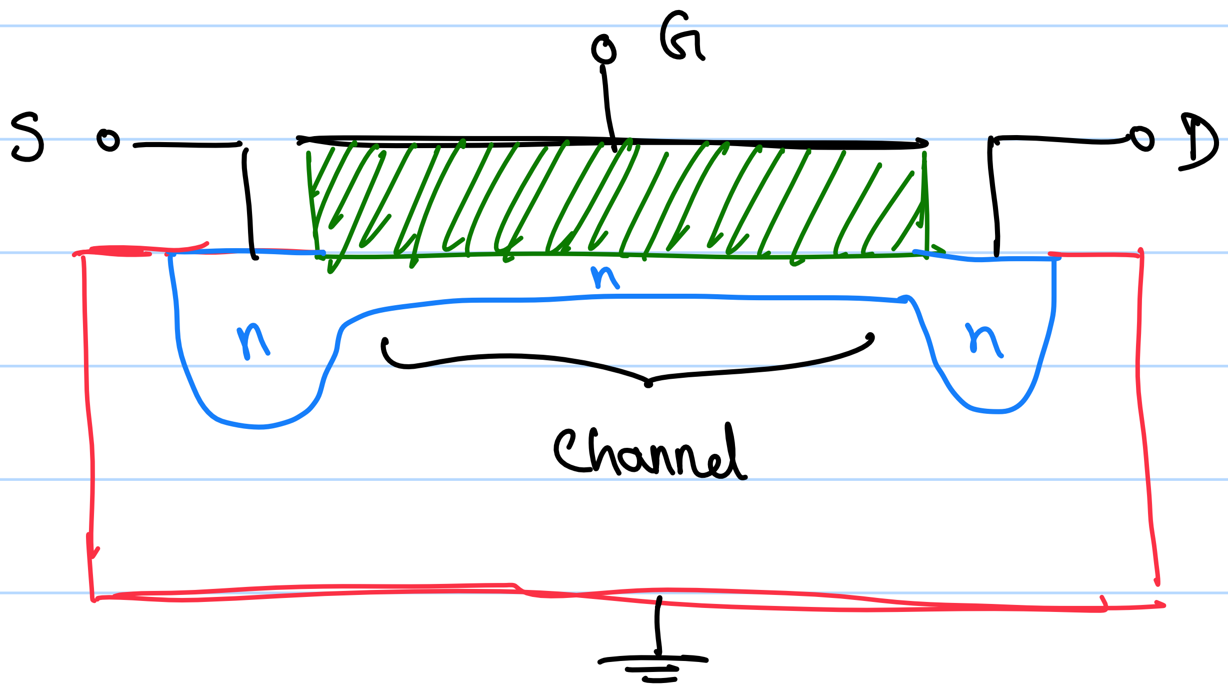


- This is depletion mode of operation.

3) $V_G \gg 0$



- The surface of the p-substrate becomes dominated by electrons, ie, becomes n-type.

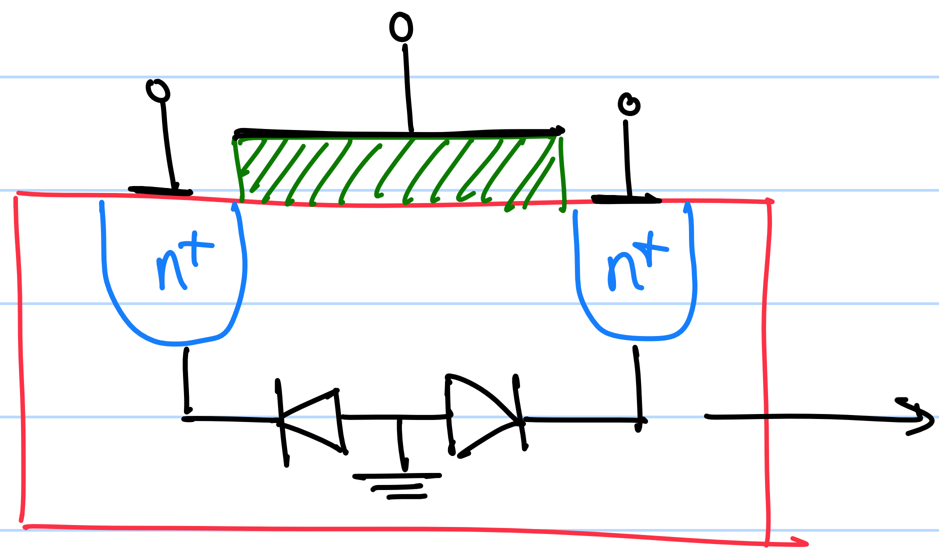


- This is inversion mode of operation.

- If n_e at surface $< N_A$ (hole conc. of substrate), it is weak inversion / subthreshold mode.

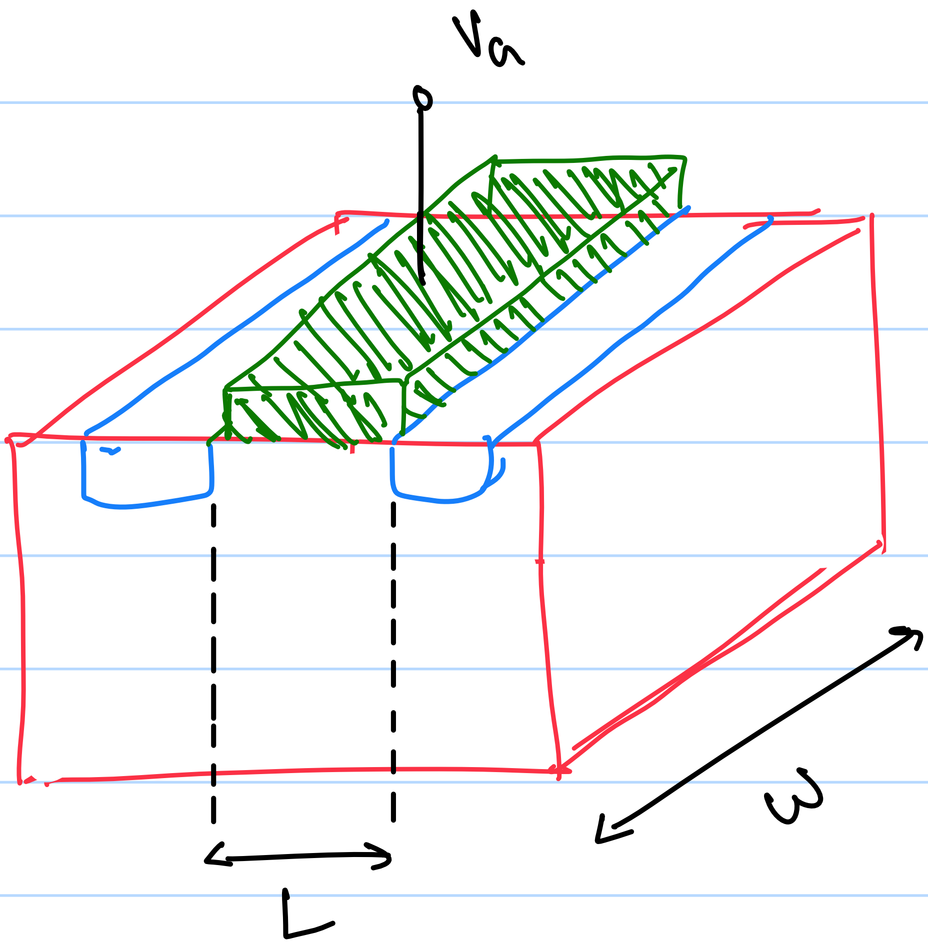
- If n_e at surface $\geq N_A$, it is strong inversion. The min. gate voltage to attain strong inversion is V_{TH} (threshold voltage)

o



ie, no current flow b/w S,D and substrate

- 3D View:-



Since the n-channel is not perfectly conductive, it has some resistance to it, depending on the dimensions L and W.

Based on V_{GS}
- Accumulation
- Depletion
- Inversion —— Based on V_{DS}
  - Linear
  - Saturation

1) $V_{GS} \leq 0 \Rightarrow I_D = 0 \; \forall \; V_{DS}$. Accumulation mode has zero channel.

2) $0 < V_{GS} < V_{TH} \Rightarrow I_D \simeq I_{D0}\, e^{\frac{V_{GS}-V_{TH}}{nV_t}}$. V_t - thermal voltage

Subthreshold conduction.

3) $V_{GS} > V_{TH}$ & $V_{DS} < V_{GS} - V_{TH} = V_{OV}$ (Overdrive voltage)

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2V_{OV}V_{DS} - \frac{V_{DS}^2}{2}\right) \longrightarrow \text{Linear Mode of Opn.}$$

If $V_{DS} << V_{OV}$,

$$I_D = \left(\mu_n C_{ox} \frac{W}{L} V_{OV}\right) V_{DS}$$

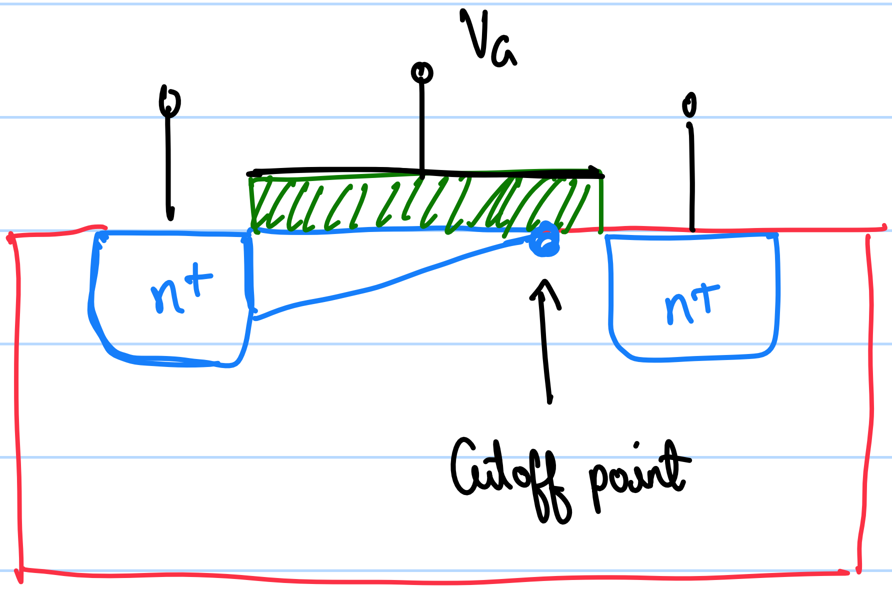
$$\Rightarrow \boxed{R = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{OV}}}$$

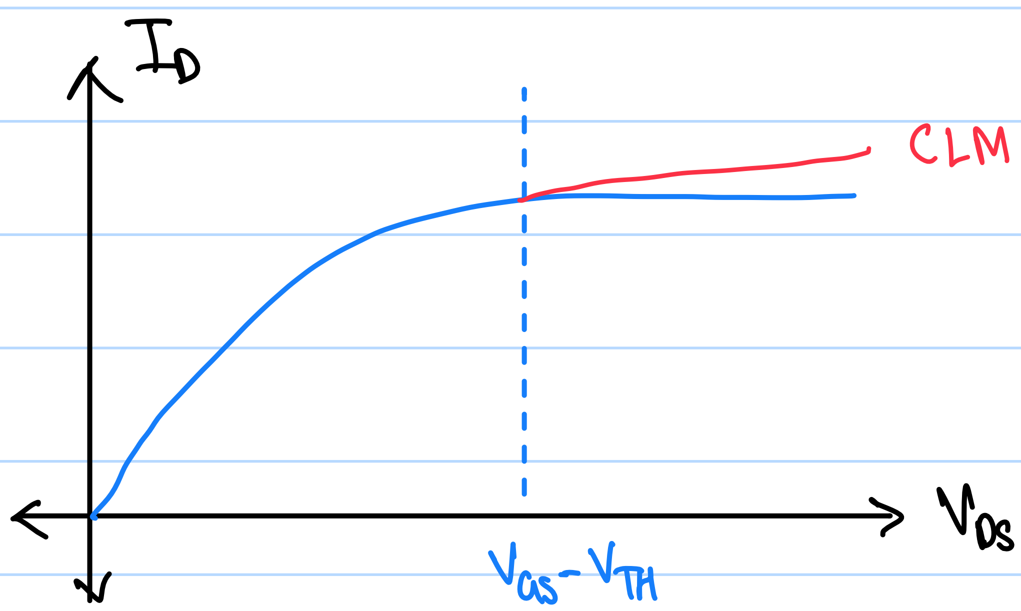
4) $V_{GS} > V_{TH}$, $V_{DS} \geq V_{GS} - V_{TH}$

$$\Rightarrow V_{GS} - V_{DS} \leq V_{TH}$$

$$\Rightarrow \underline{V_{GD} \leq V_{TH}}$$

Since $V_{GD} \leq V_{TH}$, the channel will cease to exist near the drain, since potential at the point will be lesser than threshold.





Beyond the cutoff point, the charge density is very low (depletion mode). Let linear charge density there be Q_d. $Q_d \simeq 0$.

$$dQ = Q_d \cdot dx$$

$$\frac{dQ}{dt} = Q_d \frac{dx}{dt}$$

$$= \quad I = Q_d v_d$$

$$= \quad v_d = \frac{I}{Q_d} \Rightarrow \lim_{Q_d \to 0} \frac{I}{Q_d}$$

$$\therefore v_d \longrightarrow \infty \text{ for finite } I.$$

$\therefore$ The electrons are swept almost instantaneously across the cutoff point into the drain.

∘

$$I_{DS} = \begin{cases} \mu_n C_{ox} \frac{W}{L}\left(2(V_{GS}-V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right), & V_{GS} > V_{TH},\ V_{DS} < V_{ov} \\ \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})^2, & V_{GS} > V_{TH},\ V_{DS} > V_{ov} \\ 0, & V_{GS} \ll V_{TH} \\ I_{DS0}\, e^{V_{GS}-V_T/nV_t}\left[1 - e^{-V_{DS}/V_t}\right], & V_{GS} < V_{TH} \end{cases}$$

(subthreshold leakage)

∘ PMOS:

$$I_{SD\,psat} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}\left[V_{SG} - |V_T|\right]^2$$

$$V_{SG} \geq |V_T| \ \&$$

$$V_{SD} \geq V_{SG} - |V_T|$$

$$I_{SD,lin} = \mu_p C_{ox} \frac{W}{L} \left[(V_{SG} - |V_T|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

- **Second - Order Effects :-**

1) **Channel Length Modulation :-**

Since the cutoff point moves further towards the source, as V_{DS} increases, I_D actually increases with V_{DS} even during saturation.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

λ — CLM Parameter

$$\lambda V_{DS} = \frac{\Delta L}{L}$$

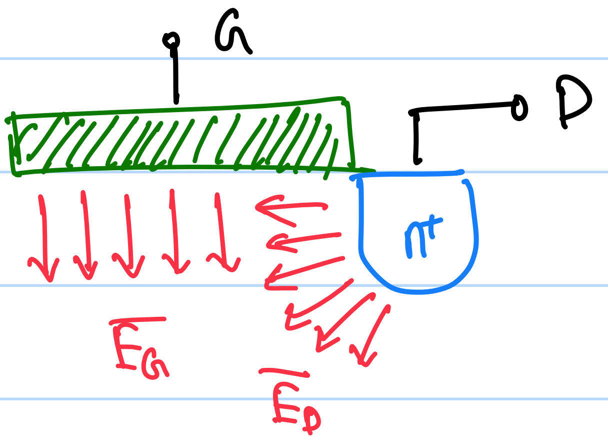
2) **Body Biasing :-**

If V_{BS} is increased, the threshold voltage of the MOSFET is decreased.

$$V_{TH} = V_{TH0} + \gamma \left[\sqrt{2\Psi_s + V_{SB}} - \sqrt{2\Psi_s} \right]$$

3) **Drain Induced Barrier Lowering :-**

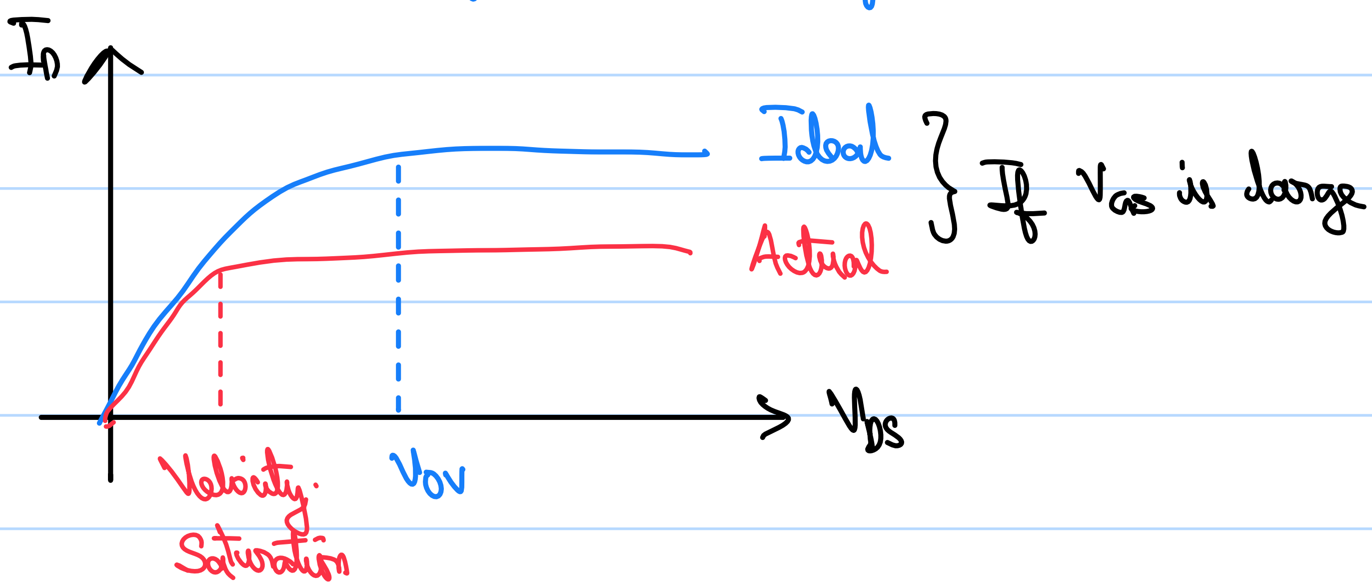
In short channel MOSFETs, the drain voltage will aid in the inversion of the channel.



Because of this aid, the threshold voltage of the MOSFET will be lower.

4) Velocity Saturation :-

For each channel, there is a certain v_d at which mobility degradation occurs due to scattering of the charge carriers. Prominent if V_{GS} is large.



If V_{GS} is low, overdrive voltage is attained before velocity saturation, so the effect is not visible.