VLSI Design - Assignment 2

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a)

Netlist Used:

```
.include "TSMC_180nm.txt"
.param W = 1.8u
.param L = 0.18u
.global gnd

*circuit
VDD Sp gnd 1.8
Vi G gnd 0

Mp1 D1 G Sp Sp CMOSP W={2.5*W} L={L}
+AS = {2.5*2.5*W*L} AD = {2.5*2.5*W*L} PS = {5*L + 2*2.5*W} PD = {5*L + 2*2.5*W}
Mn1 D1 G gnd gnd CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L + 2*W} PD = {5*L + 2*W}

Mp2 out D1 Sp Sp CMOSP W={2.5*W} L={L}
+AS = {2.5*2.5*W*L} AD = {2.5*2.5*W*L} PS = {5*L + 2*2.5*W} PD = {5*L + 2*2.5*W}
Mn2 out D1 gnd gnd CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L + 2*W} PD = {5*L + 2*W}

.dc Vi 0 1.8 0.01

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

run
let slope = deriv(V(D1))
meas DC VIL WHEN slope=-1 CROSS=1
meas DC VOH FIND V(D1) WHEN slope=-1 CROSS=1
meas DC VIH WHEN slope=-1 CROSS=2
meas DC VOL FIND V(D1) WHEN slope=-1 CROSS=2

plot V(D1)
set curplottitle=Sricharan-2024112022-q3(A)
hardcopy q3a_plot.ps V(D1)
.endc
.end
```

The VTC obtained is:

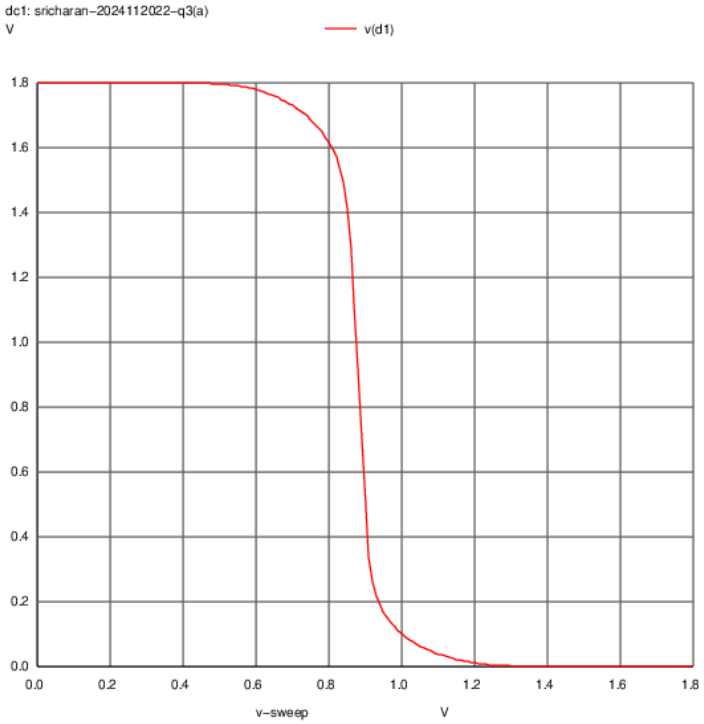

Figure 3.1: VTC of Inverter 1 (Pre-Layout)

b)

The noise margin parameters calculated from the Netlist are:

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 181
vil                 =  7.428702e-01
voh                 =  1.693732e+00
vih                 =  9.949693e-01
vol                 =  1.053852e-01
```

Figure 3.2: Noise Margin Parameters obtained from Simulation

Observed Noise Margins,

$$NM_H = V_{OH} - V_{IH} = 1.693 - 0.994 = 0.699\ V \tag{3.1}$$

$$NM_L = V_{IL} - V_{OL} = 0.742 - 0.105 = 0.637\ V \tag{3.2}$$

Theoretical Noise Margins,

$$NM_H = \frac{V_{DD} - V_{THn} + 3|V_{THp}|}{4} \tag{3.3}$$

$$NM_L = \frac{V_{DD} + 3V_{THn} - |V_{THp}|}{4} \tag{3.4}$$

The above formula is valid only for $\beta = \sqrt{\frac{K_p}{K_n}} = 1$. We know that $W_p = 2.5W_n$, C_{ox} is the same for a PMOS and a NMOS, and $\frac{\mu_p}{\mu_n} \approx \frac{1}{2}$. Therefore,

$$\beta = \sqrt{\frac{1}{2} \times 2.5} \approx 1.118 \tag{3.5}$$

So the above equations will give us a decent approximation of the theoretical noise margins. We know that $V_{THn} = 0.5183\ V$. Assume that $|V_{THp}| \approx V_{THn}$. Therefore, we get theoretical noise margins as,

$$NM_H = \frac{1.8 - 0.5183 + 3 \times 0.5183}{4} = 0.70915\ V \tag{3.6}$$

$$NM_L = \frac{1.8 + 3 \times 0.5183 - 0.5183}{4} = 0.70915\ V \tag{3.7}$$

Possible Reasons for Disparity between Observed and Theoretical values:

- Short Channel Effects, especially DIBL. (Threshold voltage of the MOSFETS will be reduced significantly due to DIBL, increasing NM_H and decreasing NM_L)
- Inaccuracies in the assumptions made ($\beta \neq 1$, $\frac{\mu_p}{\mu_n} \neq 0.5$ and $V_{THn} \neq |V_{THp}|$)

c)

Netlist Used:

```
.include TSMC_180nm.txt

* SPICE3 file created from 2inv.ext - technology: scmos

.option scale=90n

M1000 out1 inp gnd Gnd CMOSN w=20 l=2
+  ad=0.2n pd=60u as=0.2n ps=60u
M1001 out1 inp vdd vdd CMOSP w=50 l=2
+  ad=0.5n pd=0.12m as=0.5n ps=0.12m
M1002 cmos_inv_1/out out1 gnd Gnd CMOSN w=20 l=2
+  ad=0.2n pd=60u as=0.4n ps=0.12m
M1003 cmos_inv_1/out out1 vdd vdd CMOSP w=50 l=2
+  ad=0.5n pd=0.12m as=1n ps=0.24m
C0 vdd 0 5.16765f

*----------------------------------------------

.global gnd

VD vdd gnd 1.8V
```

```
Vi inp gnd 0

.dc Vi 0 1.8 0.01

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

run
let slope = deriv(V(out1))
meas DC VIL WHEN slope=-1 CROSS=1
meas DC VOH FIND V(out1) WHEN slope=-1 CROSS=1
meas DC VIH WHEN slope=-1 CROSS=2
meas DC VOL FIND V(out1) WHEN slope=-1 CROSS=2

plot V(out1)
set curplottitle = Sricharan-2024112022-q3(c)
hardcopy q3c_plot.ps V(out1)
.endc
.end
```

The VTC Obtained is:

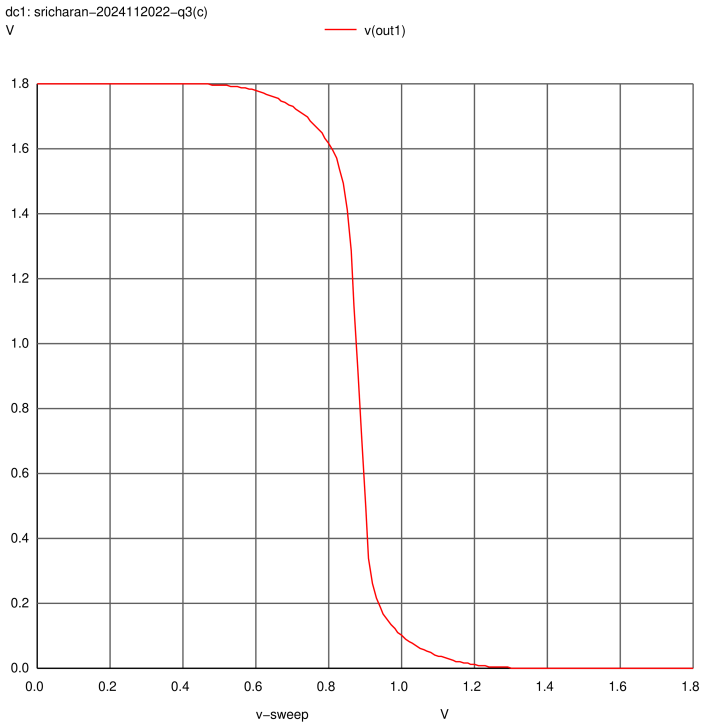

Figure 3.3: VTC of Inverter 1 (Post-Layout)

The noise margin parameters obtained are:

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Checking parameters for BSIM 3.2 model cmosp
Warning: Pd = 1.08e-11 is less than W.
Warning: Ps = 2.16e-11 is less than W.

Checking parameters for BSIM 3.2 model cmosn
Warning: Pd = 5.4e-12 is less than W.
Warning: Ps = 1.08e-11 is less than W.

No. of Data Rows : 181
vil                 =  7.428702e-01
voh                 =  1.693732e+00
vih                 =  9.949693e-01
vol                 =  1.053852e-01
```

Figure 3.4: Noise Margin Parameters obtained from Simulation

Observed Noise Margins,

$$NM_H = V_{OH} - V_{IH} = 1.693 - 0.994 = 0.699\ V \tag{3.8}$$

$$NM_L = V_{IL} - V_{OL} = 0.742 - 0.105 = 0.637\ V \tag{3.9}$$

NM	Theoretical	Pre-Layout	Post-Layout
NM_L	0.70915 V	0.637 V	0.637 V
NM_H	0.70915 V	0.699 V	0.699 V

We can see that there are no differences between the noise margin parameters pre-layout and post-layout. This is because Noise Margin is a **steady state parameter**, not a dynamic one.
Post-Layout is used to model the parasitic capacitances of the inverter. But these capacitances do not affect the steady state behavior of the circuit, only dynamic parameters (like delay). Therefore there is no difference in the Noise Margin parameters.

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a)

We know that,

$$\begin{aligned}\frac{K_p\tau_r}{C_L} &= \frac{2(V_{IL}+|V_{THp}|)}{(V_{DD}-V_{IL}-|V_{THp}|)^2}+\frac{1}{V_{DD}-V_{IL}-|V_{THp}|}\ln\left(\frac{V_{DD}+V_{OH}-2V_{IL}-2|V_{THp}|}{V_{DD}-V_{OH}}\right)\\ &= \frac{2(0.742+0.5183)}{(1.8-0.742-0.5183)^2}+\frac{1}{1.8-0.742-0.5183}\ln\left(\frac{1.8+1.693-2\times0.742-2\times0.5183}{1.8-1.693}\right)\\ &= 8.653+1.852\ln(9.087)\\ \therefore \frac{K_p\tau_r}{C_L} &= 12.74\end{aligned}$$

And,

$$\begin{aligned}\frac{K_n\tau_f}{C_L} &= \frac{2(V_{DD}-V_{IH}+V_{THn})}{(V_{IH}-V_{THn})^2}+\frac{1}{V_{IH}-V_{THn}}\ln\left(\frac{2(V_{IH}-V_{THn})-V_{OL}}{V_{OL}}\right)\\ &= \frac{2(1.8-0.994+0.5183)}{(0.994-0.5183)^2}+\frac{1}{0.994-0.5183}\ln\left(\frac{2(0.994-0.5183)-0.105}{0.105}\right)\\ &= 11.704+2.102\ln(8.06)\\ \therefore \frac{K_n\tau_f}{C_L} &= 16.09\end{aligned}$$

b)

Netlist Used for Simulation:

```
.include TSMC_180nm.txt

.param L = 0.18u
.param W = 1.8u
.global gnd

VDD vdd gnd DC 1.8
Vin A gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)

Mn1 B A gnd gnd CMOSN L={L} W={W}
+AD={2.5*L*W} AS={2.5*L*W} PD={2*W + 5*L} PS={2*W + 5*L}
Mp1 B A vdd vdd CMOSP L={L} W={2.5*W}
+AD={2.5*L*2.5*W} AS={2.5*L*2.5*W} PD={2*2.5*W + 5*L} PS={2*2.5*W + 5*L}

Mn2 C B gnd gnd CMOSN L={L} W={4*W}
+AD={2.5*L*4*W} AS={2.5*L*4*W} PD={2*4*W + 5*L} PS={2*4*W + 5*L}
Mp2 C B vdd vdd CMOSP L={L} W={10*W}
+AD={2.5*L*10*W} AS={2.5*L*10*W} PD={2*10*W + 5*L} PS={2*10*W + 5*L}

Mn3 D C gnd gnd CMOSN L={L} W={16*W}
+AD={2.5*L*16*W} AS={2.5*L*16*W} PD={2*16*W + 5*L} PS={2*16*W + 5*L}
Mp3 D C vdd vdd CMOSP L={L} W={40*W}
+AD={2.5*L*40*W} AS={2.5*L*40*W} PD={2*40*W + 5*L} PS={2*40*W + 5*L}
```

```
Mn4 E D gnd gnd CMOSN L={L} W={64*W}
+AD={2.5*L*64*W} AS={2.5*L*64*W} PD={2*64*W + 5*L} PS={2*64*W + 5*L}
Mp4 E D vdd vdd CMOSP L={L} W={160*W}
+AD={2.5*L*160*W} AS={2.5*L*160*W} PD={2*160*W + 5*L} PS={2*160*W + 5*L}

Mn5 F E gnd gnd CMOSN L={L} W={256*W}
+AD={2.5*L*256*W} AS={2.5*L*256*W} PD={2*256*W + 5*L} PS={2*256*W + 5*L}
Mp5 F E vdd vdd CMOSP L={L} W={640*W}
+AD={2.5*L*640*W} AS={2.5*L*640*W} PD={2*640*W + 5*L} PS={2*640*W + 5*L}

Cload out gnd 1pF

.tran 10p 5n

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

run

meas tran tr TRIG V(C) val=0.9 FALL=1 TARG V(D) val=0.9 RISE=1
meas tran tf TRIG V(C) val=0.9 RISE=1 TARG V(D) val=0.9 FALL=1

plot V(C) V(D)
set curplottitle=Sricharan-2024112022-q4(B)
hardcopy q4b_plot.ps V(C) V(D)
.endc
.end
```

Voltage Signals obtained:

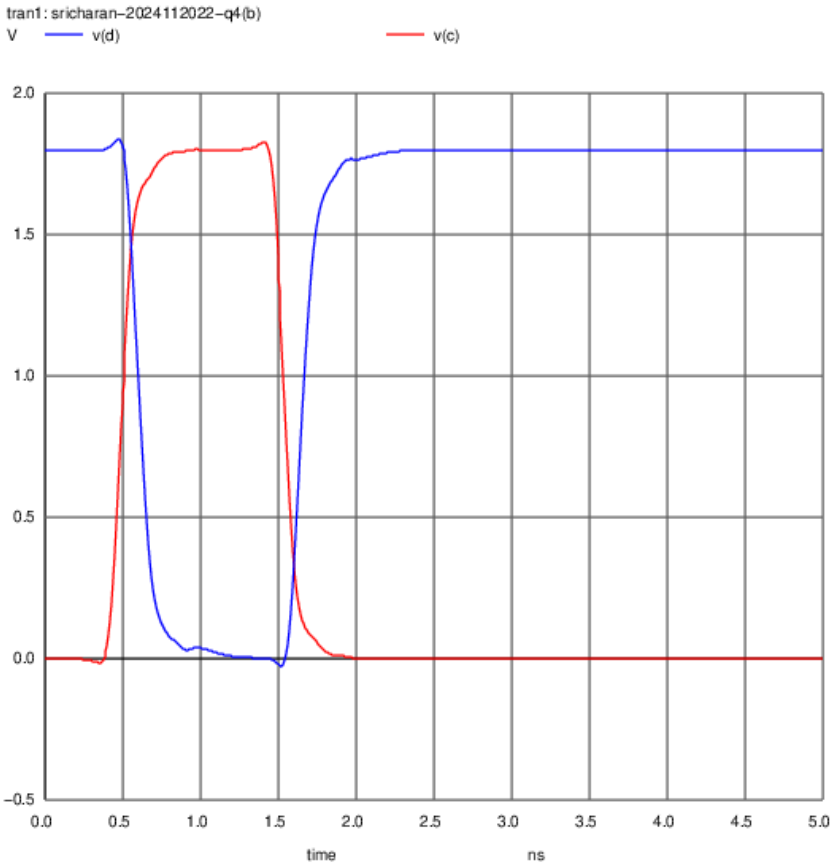

Figure 4.1: Plot of Voltage at C (red) and D (blue)

Delay parameters obtained:

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
a                                            0
b                                        1.80013
c                                     7.19725e-05
d                                        1.80006
e                                     4.66932e-05
f                                        1.79983
out                                            0
vin#branch                           -2.15234e-08
vdd#branch                           -2.82761e-05


No. of Data Rows : 517
tr                 =  1.144057e-10 targ=  1.658678e-09 trig=  1.544272e-09
tf                 =  1.121883e-10 targ=  6.123465e-10 trig=  5.001582e-10
```

Figure 4.2: Measure Rise Time Delay (tr) and Fall Time Delay (tf)

The obtained values are,

$$\tau_r = 1.144\ ps \tag{4.1}$$

$$\tau_f = 1.121\ ps \tag{4.2}$$

We can see that $\tau_r \approx \tau_f$. This can be seen by,

$$\begin{aligned} \frac{K_p\tau_r/C_L}{K_n\tau_f/C_L} &= \frac{12.74}{16.09} = 0.791 \\ \frac{\mu_p W_p}{\mu_n W_n} &= 0.791\ (\tau_r \approx \tau_f) \\ \frac{\mu_p}{\mu_n} = \frac{0.791}{2.5} &= 0.316 \end{aligned}$$

This matches with the result that μ_n is usually 2-3 times μ_p. Therefore, our rise time delay and fall time delay are similar. Also, the plot of the signals obtained is almost symmetric, causing equal delays on both sides.

c)

Netlist Used:

```
.include TSMC_180nm.txt

.param L = 0.18u
.param W = 1.8u
.global gnd

VDD vdd gnd DC 1.8
Vin A gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vprobe vdd vpr 0

Mn1 B A gnd gnd CMOSN L={L} W={W}
+AD={2.5*L*W} AS={2.5*L*W} PD={2*W + 5*L} PS={2*W + 5*L}
Mp1 B A vdd vdd CMOSP L={L} W={2.5*W}
+AD={2.5*L*2.5*W} AS={2.5*L*2.5*W} PD={2*2.5*W + 5*L} PS={2*2.5*W + 5*L}

Mn2 C B gnd gnd CMOSN L={L} W={4*W}
+AD={2.5*L*4*W} AS={2.5*L*4*W} PD={2*4*W + 5*L} PS={2*4*W + 5*L}
Mp2 C B vdd vdd CMOSP L={L} W={10*W}
+AD={2.5*L*10*W} AS={2.5*L*10*W} PD={2*10*W + 5*L} PS={2*10*W + 5*L}

Mn3 D C gnd gnd CMOSN L={L} W={16*W}
+AD={2.5*L*16*W} AS={2.5*L*16*W} PD={2*16*W + 5*L} PS={2*16*W + 5*L}
Mp3 D C vpr vpr CMOSP L={L} W={40*W}
+AD={2.5*L*40*W} AS={2.5*L*40*W} PD={2*40*W + 5*L} PS={2*40*W + 5*L}

Mn4 E D gnd gnd CMOSN L={L} W={64*W}
+AD={2.5*L*64*W} AS={2.5*L*64*W} PD={2*64*W + 5*L} PS={2*64*W + 5*L}
Mp4 E D vdd vdd CMOSP L={L} W={160*W}
+AD={2.5*L*160*W} AS={2.5*L*160*W} PD={2*160*W + 5*L} PS={2*160*W + 5*L}

Mn5 F E gnd gnd CMOSN L={L} W={256*W}
```

```
+AD={2.5*L*256*W} AS={2.5*L*256*W} PD={2*256*W + 5*L} PS={2*256*W + 5*L}
Mp5 F E vdd vdd CMOSP L={L} W={640*W}
+AD={2.5*L*640*W} AS={2.5*L*640*W} PD={2*640*W + 5*L} PS={2*640*W + 5*L}

Cload out gnd 1pF

.tran 10p 5n

.control

set color0 = white
set color1 = black
set hcopypscolor = 1

run
plot I(Vprobe)
set curplottitle = Sricharan-2024112022-Q4(d)
hardcopy q4d_plot.ps I(Vprobe)
.endc
.end
```

Plot of Supply Current through I3 Obtained:

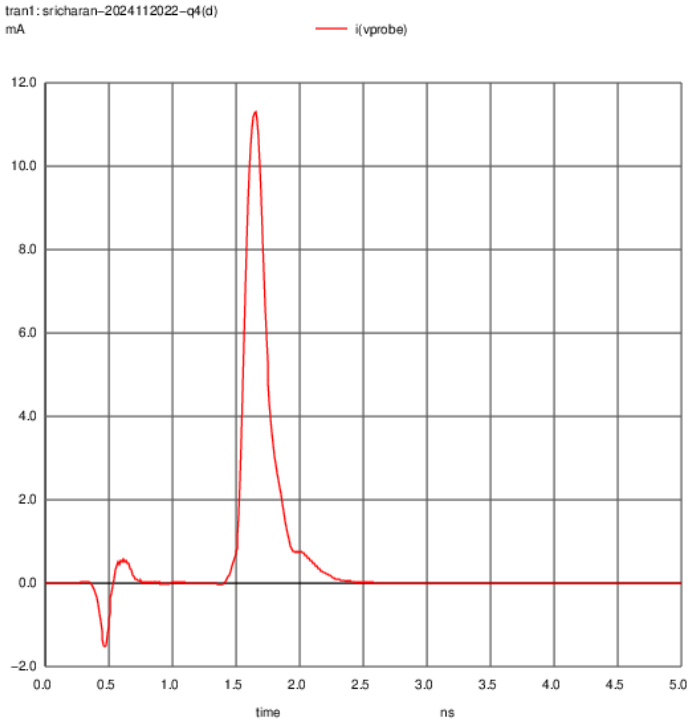

Figure 4.3: Plot of I_{DD} vs time

The supply current for I3 spikes at a certain time. Looking at Figure 4.1, we can see that the spike is roughly located at the same time as the falling edge of the input pulse. This is because,

$$\text{Input } 1 \to 0 \implies I_1\ 0 \to 1 \implies I_2\ 1 \to 0 \implies I_3\ 0 \to 1$$

So, the output of I3 is rising when the input is falling. Since when the output is rising, PMOS starts to conduct and NMOS turns off, the current through the inverter will be mostly from the drain to the output, resulting in the observed spike in I_{DD} during the falling edge of the input. The small dip observed during the rising edge of the input, is when the output of I3 is falling, which cause the current is flowing in the reverse direction of I_{DD}, to go through the NMOS to ground. The dip is small because the PMOS starts to enter cutoff mode, giving high resistance to the current.

e)

Netlist Used:

```
.include TSMC_180nm.txt

.param L = 0.18u
.param W = 1.8u
.global gnd

VDD vdd gnd DC 1.8
Vin A gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vprobe vpr gnd 0

Mn1 B A gnd gnd CMOSN L={L} W={W}
+AD={2.5*L*W} AS={2.5*L*W} PD={2*W + 5*L} PS={2*W + 5*L}
Mp1 B A vdd vdd CMOSP L={L} W={2.5*W}
+AD={2.5*L*2.5*W} AS={2.5*L*2.5*W} PD={2*2.5*W + 5*L} PS={2*2.5*W + 5*L}

Mn2 C B gnd gnd CMOSN L={L} W={4*W}
+AD={2.5*L*4*W} AS={2.5*L*4*W} PD={2*4*W + 5*L} PS={2*4*W + 5*L}
Mp2 C B vdd vdd CMOSP L={L} W={10*W}
+AD={2.5*L*10*W} AS={2.5*L*10*W} PD={2*10*W + 5*L} PS={2*10*W + 5*L}

Mn3 D C vpr vpr CMOSN L={L} W={16*W}
+AD={2.5*L*16*W} AS={2.5*L*16*W} PD={2*16*W + 5*L} PS={2*16*W + 5*L}
Mp3 D C vdd vdd CMOSP L={L} W={40*W}
+AD={2.5*L*40*W} AS={2.5*L*40*W} PD={2*40*W + 5*L} PS={2*40*W + 5*L}

Mn4 E D gnd gnd CMOSN L={L} W={64*W}
+AD={2.5*L*64*W} AS={2.5*L*64*W} PD={2*64*W + 5*L} PS={2*64*W + 5*L}
Mp4 E D vdd vdd CMOSP L={L} W={160*W}
+AD={2.5*L*160*W} AS={2.5*L*160*W} PD={2*160*W + 5*L} PS={2*160*W + 5*L}

Mn5 F E gnd gnd CMOSN L={L} W={256*W}
+AD={2.5*L*256*W} AS={2.5*L*256*W} PD={2*256*W + 5*L} PS={2*256*W + 5*L}
Mp5 F E vdd vdd CMOSP L={L} W={640*W}
+AD={2.5*L*640*W} AS={2.5*L*640*W} PD={2*640*W + 5*L} PS={2*640*W + 5*L}

Cload out gnd 1pF
```

```
.tran 10p 5n

.control

set color0 = white
set color1 = black
set hcopypscolor = 1

run
plot I(Vprobe)
set curplottitle = Sricharan-2024112022-q4(e)
hardcopy q4e_plot.ps I(Vprobe)
.endc
.end
```

Plot of Ground current through I3 obtained:

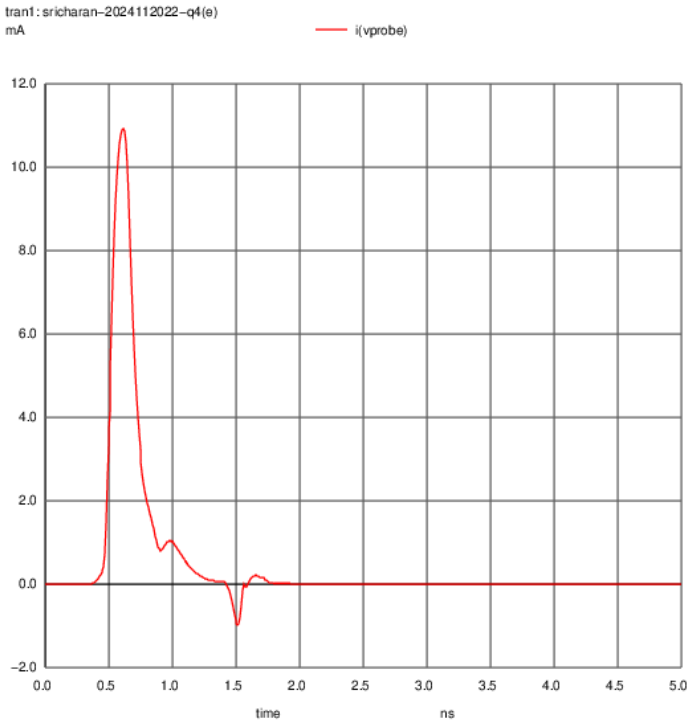

Figure 4.4: Plot of I_{SS} vs time

Similar to the situation in Q4(e), we see a spike in the graph during the rising edge of the input pulse. This is because.

$$\text{Input } 0 \to 1 \implies I_1\ 1 \to 0 \implies I_2\ 0 \to 1 \implies I_3\ 1 \to 0$$

So the output of I3 is falling when the input is rising. When the output of I3 is falling, the PMOS turns off and the NMOS starts to conduct, so the current through the inverter will be majorly from the NMOS to the ground, resulting in the observed spike in I_{SS} during the rising edge of the

input.

The small dip during the falling edge of the input pulse is when the output of I3 is rising, which cause the current to flow to the output node, in the opposite direction of I_{SS}. The dip is small because the NMOS is entering cutoff region, causing high resistance to the current.

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Netlist Used:

```
.include "TSMC_180nm.txt"
.param W = 1.8u
.param Wv = 1.8u
.param L = 0.18u
.global gnd

*circuit
VDD Sp gnd 1.8
Vi G gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns
+0V 10ns 0V)

Mp1 D1 G Sp Sp CMOSP W={2.5*W} L={L}
+AS = {2.5*2.5*W*L} AD = {2.5*2.5*W*L} PS = {5*L + 2*2.5*W} PD = {5*L + 2*2.5*W}
Mn1 D1 G gnd gnd CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L + 2*W} PD = {5*L + 2*W}

Mp2 out D1 Sp Sp CMOSP W={2.5*Wv} L={L}
+AS = {2.5*2.5*Wv*L} AD = {2.5*2.5*Wv*L} PS = {5*L + 2*2.5*Wv} PD = {5*L + 2*2.5*Wv}
Mn2 out D1 gnd gnd CMOSN W={Wv} L={L}
+AS = {2.5*Wv*L} AD = {2.5*Wv*L} PS = {5*L + 2*Wv} PD = {5*L + 2*Wv}

.tran 10ps 5ns

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

foreach f 1 2 4 6 8 10 12
    reset
    alterparam Wv = $f*{W}
    run
    meas tran TPLH trig v(G) val=0.9 fall=1 targ v(D1) val=0.9 rise=1
    meas tran TPHL trig v(G) val=0.9 rise=1 targ v(D1) val=0.9 fall=1
    let TAVG = (TPLH+TPHL)/2
    print TAVG
end
.endc
.end
```

Let $\frac{C_L}{C_{in}} \approx \frac{W_{inv2}}{W_{inv1}}$. The delay values obtained are,

$\frac{C_L}{C_{in}}$	Delay
1	0.781 ps
2	0.781 ps
4	1.019 ps
6	1.413 ps
8	1.742 ps
10	2.028 ps
12	2.291 ps

Plotting the values we get,

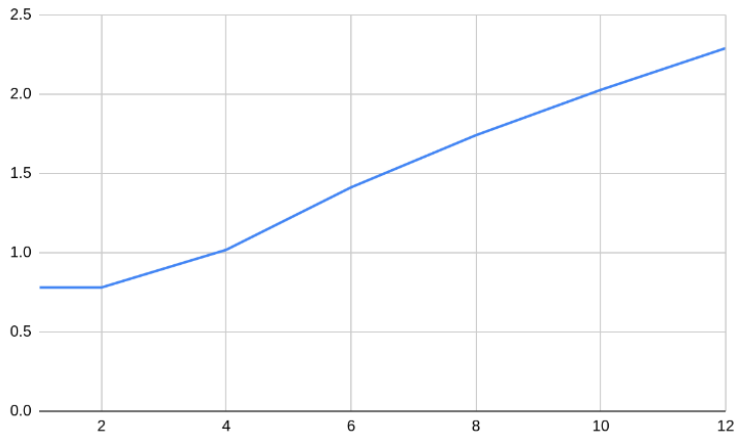

Figure 5.1: Plot of Delay vs C_L/C_{in}

We can see that the plot is roughly linear. To fine absolute parasitic delay, we know that,

$$D = \tau\left(\frac{C_{ext}}{C_{in}} + \rho\right)$$

To construct the approximate line equation, let us take the points (10, 2.028ps) and (12,2.291ps).

$$\begin{aligned} \frac{y - 2.028}{2.291 - 2.028} &= \frac{x - 10}{12 - 10} \\ \implies \frac{y - 2.028}{0.263} &= \frac{x - 10}{2} \\ \implies y &= 0.1315x - 1.315 + 2.028 \\ \therefore y &= 0.1315x + 0.713\ ps \end{aligned}$$

At x = 0, y = $\rho\tau$ = 0.713 ps. $\therefore$ the absolute parasitic delay is 0.713 ps.

To find τ,

$$\begin{aligned} D &= \tau\left(\frac{C_{ext}}{C_{in}} + \rho\right) \\ \implies \tau &= \frac{D - \rho\tau}{C_{ext}/C_{in}} \end{aligned}$$

Taking the point (10, 2.028),

$$\tau = \frac{2.028 - 0.713}{10} = 0.1315\ ps$$

In the Netlist, we are varying the C_L by using an Inverter and changing the Width of its MOSFETs uniformly. The input capacitance of the second inverter acts as the load capacitance, and since the $C_{in} \propto W$ for an inverter, increasing the width of the inverter's MOSFETs, increases the capacitance offered by the inverter.

6

a)

Netlist Used:

```
.include "TSMC_180nm.txt"
.param lb = 0.09u
.param L = {2*lb}
.param Wn = {10*lb}
.param Wp = {25*lb}
.global gnd

.subckt inverter inp out vdd gnd
Mp out inp vdd vdd CMOSP W={Wp} L={L}
+AS = {2.5*Wp*L} AD = {2.5*Wp*L} PS = {5*L + 2*Wp} PD = {5*L + 2*Wp}
Mn out inp gnd gnd CMOSN W={Wn} L={L}
+AS = {2.5*Wn*L} AD = {2.5*Wn*L} PS = {5*L + 2*Wn} PD = {5*L + 2*Wn}
.ends

VD vdd gnd 1.8
.ic V(inp) = 0

xinv1 inp A vdd gnd inverter
xinv2 A B vdd gnd inverter
xinv3 B C vdd gnd inverter
xinv4 C D vdd gnd inverter
xinv5 D E vdd gnd inverter
xinv6 E F vdd gnd inverter
xinv7 F G vdd gnd inverter
xinv8 G H vdd gnd inverter
xinv9 H I vdd gnd inverter
xinv10 I J vdd gnd inverter
xinv11 J K vdd gnd inverter
xinv12 K L vdd gnd inverter
xinv13 L M vdd gnd inverter
xinv14 M N vdd gnd inverter
xinv15 N O vdd gnd inverter
xinv16 O P vdd gnd inverter
xinv17 P Q vdd gnd inverter
xinv18 Q R vdd gnd inverter
xinv19 R S vdd gnd inverter
xinv20 S T vdd gnd inverter
```

```
xinv21 T U vdd gnd inverter
xinv22 U V vdd gnd inverter
xinv23 V W vdd gnd inverter
xinv24 W X vdd gnd inverter
xinv25 X Y vdd gnd inverter
xinv26 Y Z vdd gnd inverter
xinv27 Z AA vdd gnd inverter
xinv28 AA AB vdd gnd inverter
xinv29 AB AC vdd gnd inverter
xinv30 AC AD vdd gnd inverter
xinv31 AD inp vdd gnd inverter

.tran 10ps 10ns

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
meas tran tr TRIG V(A) VAL=0.9 FALL=1 TARG V(B) VAL=0.9 RISE=1
meas tran tf TRIG V(A) VAL=0.9 RISE=1 TARG V(B) VAL=0.9 FALL=1
let delay = (tr+tf)/2
meas tran TPERIOD TRIG V(inp) VAL=0.9 RISE=1 TARG V(inp) VAL=0.9 RISE=2
let freq = 1/TPERIOD
plot V(inp)
print delay freq
set curplottitle = Sricharan-2024112022-q6(A)
hardcopy q6a_plot.ps V(inp)
.endc
.end
```

Plot obtained:

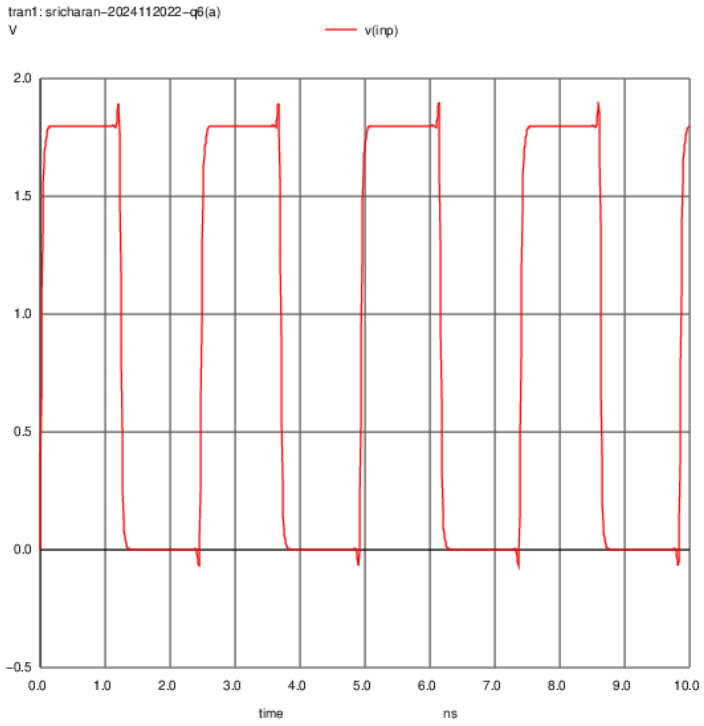

Figure 6.1: Oscillating Output of the Ring Oscillator

```
 Reference value :  9.77280e-09
No. of Data Rows : 1008
tr                =  3.905222e-11 targ=  9.864694e-11 trig=  5.959472e-11
tf                =  4.037294e-11 targ=  1.330418e-09 trig=  1.290045e-09
tperiod           =  2.462049e-09 targ=  2.481346e-09 trig=  1.929676e-11
Warning: Missing charsets in String to FontSet conversion
delay = 3.971258e-11
freq = 4.061658e+08
```

Figure 6.2: Measured Single Inverter Propagation Delay (delay) and Oscillator Frequency (freq)

The measured propagation delay by a single inverter $\tau_D = 0.397$ ps

Expected frequency $= \frac{1}{62\tau_D} = \frac{1}{62 \times 0.397 \times 10^{-10}} = 4.062 \times 10^8$ Hz

Obtained frequency $= 4.061 \times 10^8$ Hz.

Within the realm of simulation error, the obtained value of frequency is almost equal to the expected frequency from the formula $f = \frac{1}{62\tau_D}$

b)

Layout Used:

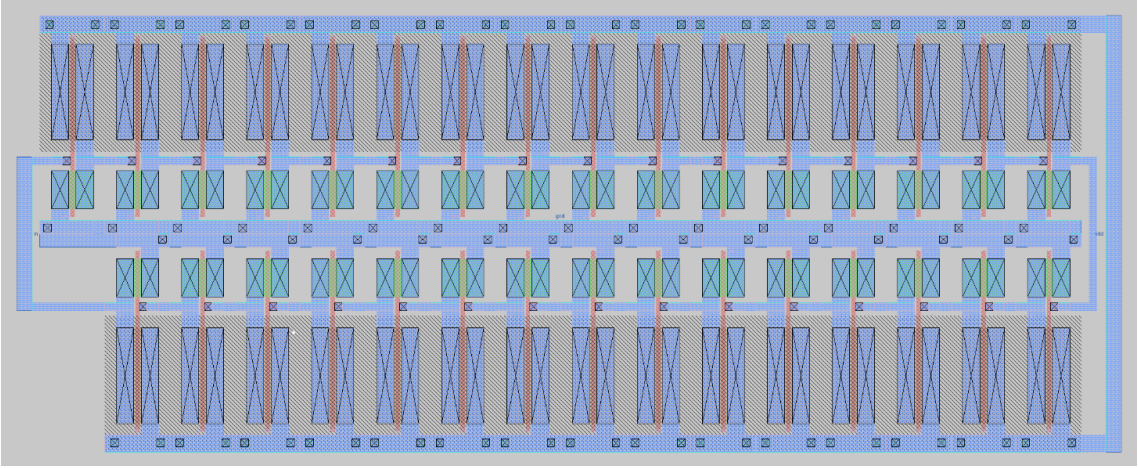

Figure 6.3: Layout of the 31-stage Ring-Oscillator in Magic

c)

Netlist Used:

```
.include "TSMC_180nm.txt"
.global gnd

* SPICE3 file created from 31ro2.ext - technology: scmos

.option scale=10n

M1000 cmos_inv_0[1]/in in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=16.2n ps=0.54m
M1001 cmos_inv_0[1]/in in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=40.5n ps=1.08m
M1002 cmos_inv_0[2]/in cmos_inv_0[1]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0.5022u ps=0.01674
M1003 cmos_inv_0[2]/in cmos_inv_0[1]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=1.2555u ps=0.03348
M1004 cmos_inv_0[3]/in cmos_inv_0[2]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1005 cmos_inv_0[3]/in cmos_inv_0[2]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1006 cmos_inv_0[4]/in cmos_inv_0[3]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1007 cmos_inv_0[4]/in cmos_inv_0[3]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1008 cmos_inv_0[5]/in cmos_inv_0[4]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1009 cmos_inv_0[5]/in cmos_inv_0[4]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1010 cmos_inv_0[6]/in cmos_inv_0[5]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1011 cmos_inv_0[6]/in cmos_inv_0[5]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1012 cmos_inv_0[7]/in cmos_inv_0[6]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
```

```
M1013 cmos_inv_0[7]/in cmos_inv_0[6]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1014 cmos_inv_0[8]/in cmos_inv_0[7]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1015 cmos_inv_0[8]/in cmos_inv_0[7]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1016 cmos_inv_0[9]/in cmos_inv_0[8]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1017 cmos_inv_0[9]/in cmos_inv_0[8]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1018 cmos_inv_0[9]/out cmos_inv_0[9]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1019 cmos_inv_0[9]/out cmos_inv_0[9]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1020 cmos_inv_0[11]/in cmos_inv_0[9]/out gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1021 cmos_inv_0[11]/in cmos_inv_0[9]/out vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1022 cmos_inv_0[12]/in cmos_inv_0[11]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1023 cmos_inv_0[12]/in cmos_inv_0[11]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1024 cmos_inv_0[13]/in cmos_inv_0[12]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1025 cmos_inv_0[13]/in cmos_inv_0[12]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1026 cmos_inv_0[14]/in cmos_inv_0[13]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1027 cmos_inv_0[14]/in cmos_inv_0[13]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1028 cmos_inv_0[15]/in cmos_inv_0[14]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1029 cmos_inv_0[15]/in cmos_inv_0[14]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1030 cmos_inv_1[0]/in cmos_inv_0[15]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1031 cmos_inv_1[0]/in cmos_inv_0[15]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1032 cmos_inv_1[1]/in cmos_inv_1[0]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1033 cmos_inv_1[1]/in cmos_inv_1[0]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1034 cmos_inv_1[2]/in cmos_inv_1[1]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1035 cmos_inv_1[2]/in cmos_inv_1[1]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1036 cmos_inv_1[3]/in cmos_inv_1[2]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1037 cmos_inv_1[3]/in cmos_inv_1[2]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1038 cmos_inv_1[4]/in cmos_inv_1[3]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1039 cmos_inv_1[4]/in cmos_inv_1[3]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1040 cmos_inv_1[5]/in cmos_inv_1[4]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
```

```
M1041 cmos_inv_1[5]/in cmos_inv_1[4]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1042 cmos_inv_1[6]/in cmos_inv_1[5]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1043 cmos_inv_1[6]/in cmos_inv_1[5]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1044 cmos_inv_1[7]/in cmos_inv_1[6]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1045 cmos_inv_1[7]/in cmos_inv_1[6]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1046 cmos_inv_1[8]/in cmos_inv_1[7]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1047 cmos_inv_1[8]/in cmos_inv_1[7]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1048 cmos_inv_1[9]/in cmos_inv_1[8]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1049 cmos_inv_1[9]/in cmos_inv_1[8]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1050 cmos_inv_1[9]/out cmos_inv_1[9]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1051 cmos_inv_1[9]/out cmos_inv_1[9]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1052 cmos_inv_1[11]/in cmos_inv_1[9]/out gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1053 cmos_inv_1[11]/in cmos_inv_1[9]/out vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1054 cmos_inv_1[12]/in cmos_inv_1[11]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1055 cmos_inv_1[12]/in cmos_inv_1[11]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1056 cmos_inv_1[13]/in cmos_inv_1[12]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1057 cmos_inv_1[13]/in cmos_inv_1[12]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1058 cmos_inv_1[14]/in cmos_inv_1[13]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1059 cmos_inv_1[14]/in cmos_inv_1[13]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
M1060 in cmos_inv_1[14]/in gnd Gnd CMOSN w=180 l=18
+  ad=16.2n pd=0.54m as=0 ps=0
M1061 in cmos_inv_1[14]/in vdd vdd CMOSP w=450 l=18
+  ad=40.5n pd=1.08m as=0 ps=0
C0 vdd 0 79.61257f

VD vdd gnd 1.8
.ic V(in) = 0

.tran 10p 10n

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
meas tran tr TRIG V(cmos_inv_0[3]/in) VAL=0.9 FALL=1 TARG V(cmos_inv_0[4]/in) VAL=0.9 RISE=1
meas tran tf TRIG V(cmos_inv_0[3]/in) VAL=0.9 RISE=1 TARG V(cmos_inv_0[4]/in) VAL=0.9 FALL=1
```

```
let delay = (tr+tf)/2
meas tran TPERIOD TRIG V(in) VAL=0.9 RISE=1 TARG V(in) VAL=0.9 RISE=2
let freq = 1/TPERIOD
plot V(in)
print delay freq
set curplottitle=Sricharan-2024112022-q6(C)
hardcopy q6c_plot.ps V(in)
.endc
.end
```

Plot obtained:

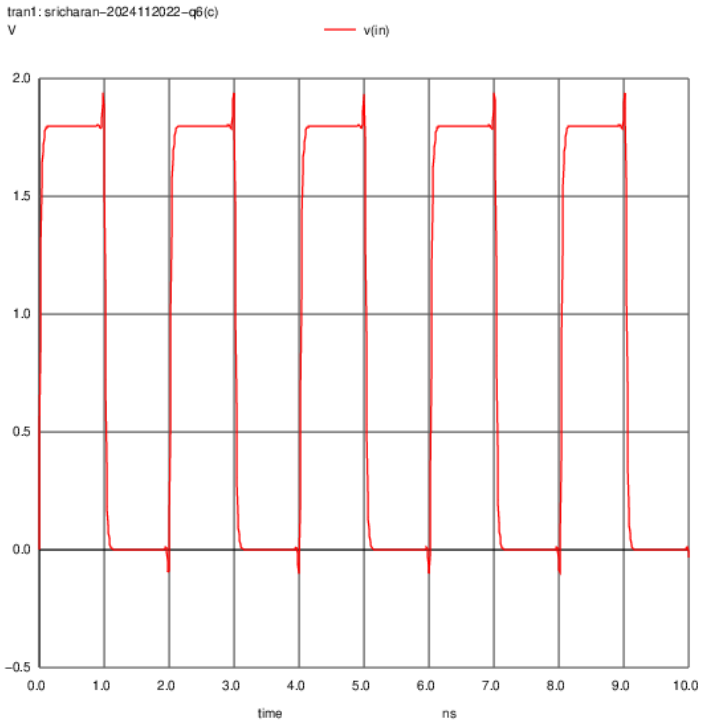

Figure 6.4: Oscillating Output of the Ring Oscillator

```
 Reference value :  7.62280e-09
No. of Data Rows : 1008
tr                 =  3.193341e-11 targ=  1.438231e-10 trig=  1.118897e-10
tf                 =  3.279853e-11 targ=  1.148102e-09 trig=  1.115303e-09
tperiod            =  2.007406e-09 targ=  2.021697e-09 trig=  1.429101e-11
delay = 3.236597e-11
freq = 4.981553e+08
```

Figure 6.5: Measured Single Inverter Propagation Delay (delay) and Oscillator Frequency (freq)

The measured propagation delay by a single inverter $\tau_D = 0.323$ ps

Expected frequency $= \frac{1}{62\tau_D} = \frac{1}{62 \times 0.323 \times 10^{-10}} = 4.993 \times 10^8$ Hz

Obtained frequency $= 4.981 \times 10^8$ Hz.

Within the realm of simulation error, the obtained value of frequency is almost equal to the

expected frequency from the formula $f = \frac{1}{62\tau_D}$

d)

We can see that the Post-Layout frequency of the Ring Oscillator is significantly higher than the Pre-Layout frequency.

This seems contradictory to what is expected from our delay equation, where,

$$\tau_D = \tau(\frac{C_{ext}}{C_{in}} + \rho)$$

The value of ρ represent the parasitics of the inverter. Since the Post-Layout simulation models the parasitics as well, ρ must be higher for the Post-Layout simulation.

However, the parasitic capacitances, especially the drain-gate and source-gate overlap capacitances, create an indirect path for transient current to flow across the inverter, before the switching fully occurs, causing the capacitances of the next inverter to be charged earlier and the switching to start earlier than expected:

From Q5, we know that if the output of an inverter is rising, current flows out of the inverter and when the output is falling, the current flows into the inverter.

- While Rising, the transient current flowing out of the next inverter charges up the parasitics through this indirect path on the next inverter, increasing the potential at the input node of the next inverter earlier than expected.
- While Falling, the parasitics on the next inverter start discharging through this indirect path, decreasing the voltage at the input node of the next inverter earlier than expected.

These reduce the propagation delay of the inverters as a whole, thereby increasing frequency of the ring oscillator significantly.