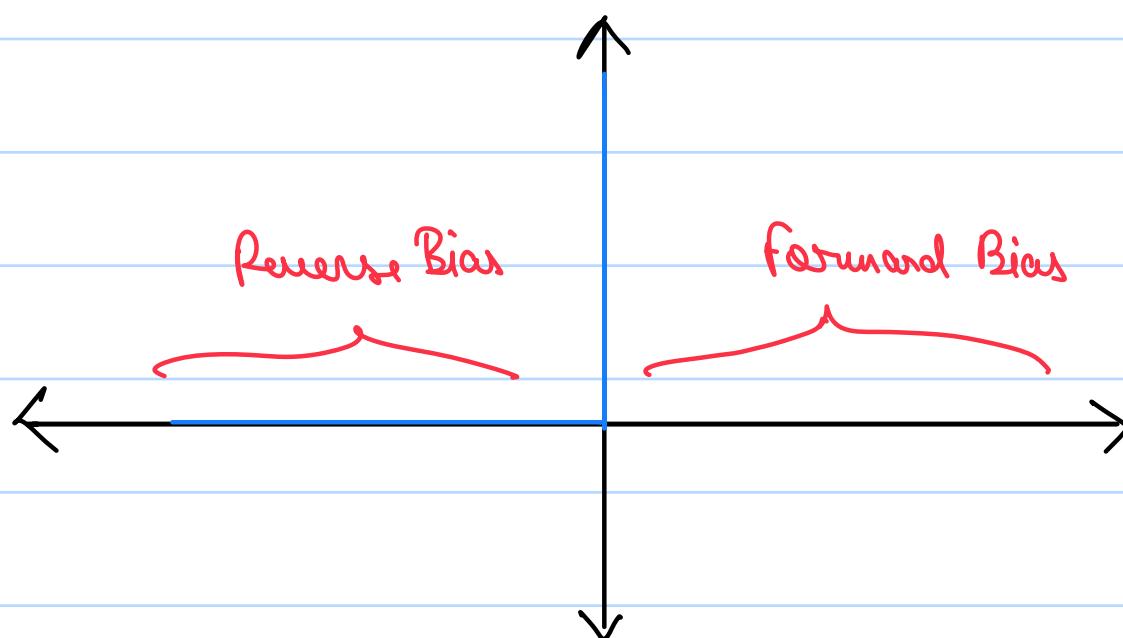

Debra
Smith

Microelectronic Circuits

- Sedra Smith

1) Diodes

- A diode is the most basic non-linear component.

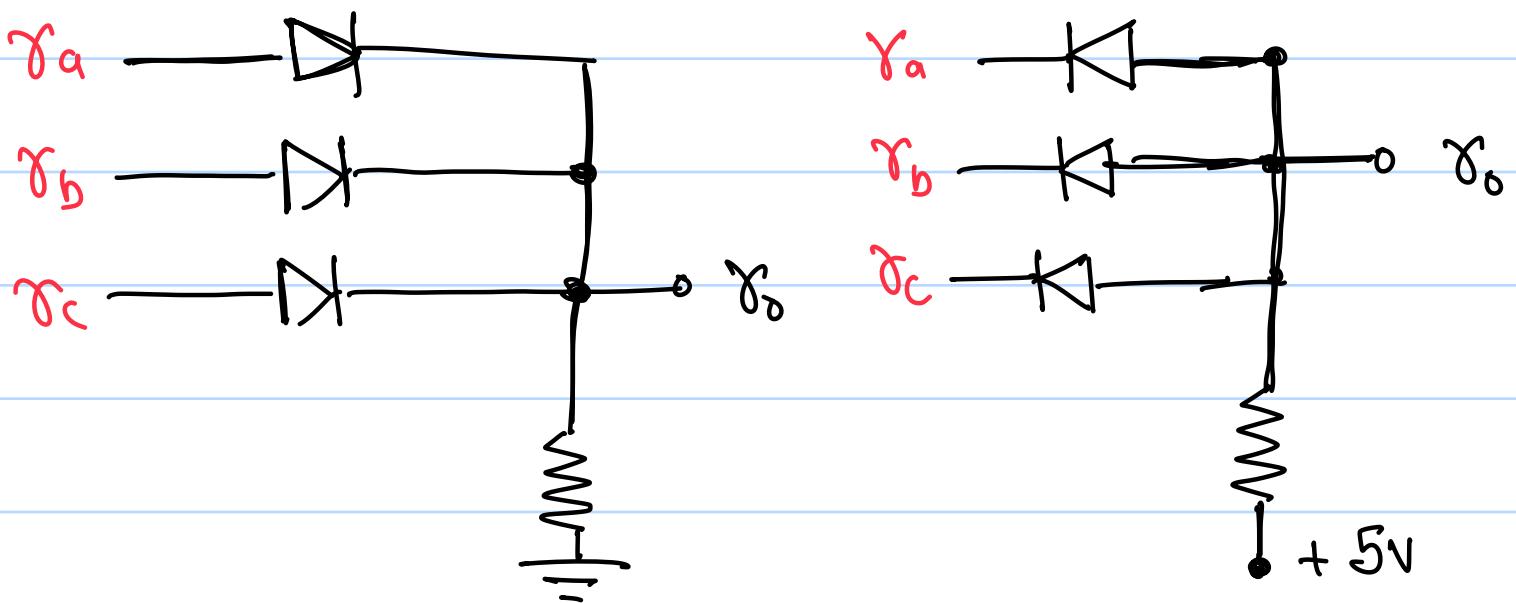


Ideal I-V Characteristics of Diode

- Clearly the IV relation in a diode is nonlinear, but it is made up of 2 line segments. Such a behavior is called piecewise linear behaviour.
- If the voltage applied is restricted within these line segments, the behavior can be assumed as linear.

◦ Application :-

1. Rectifiers.
2. Diode Logic Gates.



3 inp OR gate

3 inp AND gate

- PN Junction Diode :-

Most common implementation of a diode.

- Intrinsic Semiconductors :-

- Semiconductors are those materials with conductivity in between insulators and conductors.
- Single-element - Silicon, Germanium
Compound - Gallium-Arsenide , elements from groups III and II
or I and VI
↳ Used in LEDs
- Most common semiconductor = Silicon.
 - forms 4 covalent bonds with each other to get a regular lattice structure.
- At room temperature , there is enough energy for some of these covalent bonds to break.

- Such a break results in the formation of free electrons, which increase electrical conductivity. Therefore,

conductivity \propto Temperature

This generation of electrons is called thermal generation.

- Each free electron generated, leaves a +vely charged "hole" behind. This hole can be occupied by other free electrons. This is called recombination

- At thermal equilibrium,

rate of generation = rate of recombination

\Rightarrow Concentration of electrons is fixed.

$\Rightarrow n = p = n_i$, n_i = conc. of free electrons / cm^3 at room temp.

$$n_i = B T^{3/2} e^{-E_g/2kT}$$

$$B = 7.3 \times 10^{15} \text{ cm}^{-3} \text{ K}^{-3/2} \text{ for Si}$$

\uparrow Material dependent.

$$E_g = \text{Band Gap Energy.} = 1.12 \text{ eV for Si}$$

\uparrow Min. energy required to break the con. bond.

Applicable in
doped Si
as well

$$np = n_i^2$$

$$n_i = 1.5 \times 10^{10} / \text{cm}^3 \text{ Si}$$

n - e^- concentration
 p - h^+ concentration
 \uparrow hole.

→ Intrinsic Semiconductors :-

Intrinsic semiconductors with impurities to increase carrier concentration. The process of introducing impurities is called doping.

◦ n-type :

Dopant has 5 electrons in valence, resulting in 1 extra electron in the final lattice.

- Donor impurity. ex: Phosphorus.

- The hole associated with this extra electron is bound to the dopant.

- Electron concentration $n \approx N_D$ (Conc of donor impurity)

Hole concentration is only still affected by thermal ionization only. i.e.

$$p \cdot n = n_i^2$$
$$\Rightarrow p = \frac{n_i^2}{N_D}$$

p_n will still depend on temperature, same as n_i .

◦ p-type :

Dopant has 3 o⁻ in its valence shell; creating a negative charge at the dopant atom after lattice formation.

- Negative charge is due to surrounding Si donating e^- , thereby creating holes.

$$\rho = N_A$$

$$\Rightarrow n = \frac{N_i^2}{N_A}$$

- p-type and n-type semiconductors are electrically neutral.

Current Flow In Semiconductors :-

Drift Current :-

- In an applied electric field, the free electrons are accelerated forward, creating a current.

- Velocity of $e^- = \mu \cdot \vec{E}$ μ = mobility of material.

$$\begin{aligned} \mu_p &= \text{hole mobility}, \quad \mu_e = \text{electron mobility} \\ \text{Intrinsic Si:} \quad &= 480 \text{ cm}^2/\text{V.s} \quad = 1350 \text{ cm}^2/\text{V.s} \end{aligned}$$

e^- more faster
than h^+ in
intrinsic Si

$$I_p = nAqVd$$

$$I_{e^-} = nA(-e)Vd$$

$$= I_p = nAq\mu_p E$$

$$= nA(-e)(-\mu_e E)$$

$$I = I_p + I_e = nAq(\mu_p + \mu_e)E$$

$$J = nqE(\mu_p + \mu_e)$$

Alternate Ohm's law

$$\frac{J}{E} = nq(\mu_p + \mu_e) = \sigma$$

conductivity

- This current is very similar to that found in normal conductors.

- o Diffusion Current :- (I_D)

Current that is due to charge carrier differences within the material.

- The magnitude of current at any point is proportional to the gradient.

$$J_p = -qD_p \frac{dp(x)}{dx}$$

→ hole current

↑ conc-gradient
 ↓ diffusion const.

- D_p is the diffusion constant.

$$J_n = eD_n \frac{dn(x)}{dx}$$

→ electron current

For Si,

$$D_n = 25 \text{ cm}^2/\text{s} \quad D_p = 12 \text{ cm}^2/\text{s}$$

e^- has more diffusion ability than h^+

- o Thermal Voltage :-

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$$

V_T - Thermal Voltage

$$V_T = \frac{kT}{q}$$

- V_T is termed as the thermal voltage and this relationship b/w D, μ, V_T is termed as the Einstein relationship

At room temp $V_T = 25.9 \text{ mV}$.

- P-n Junction :-

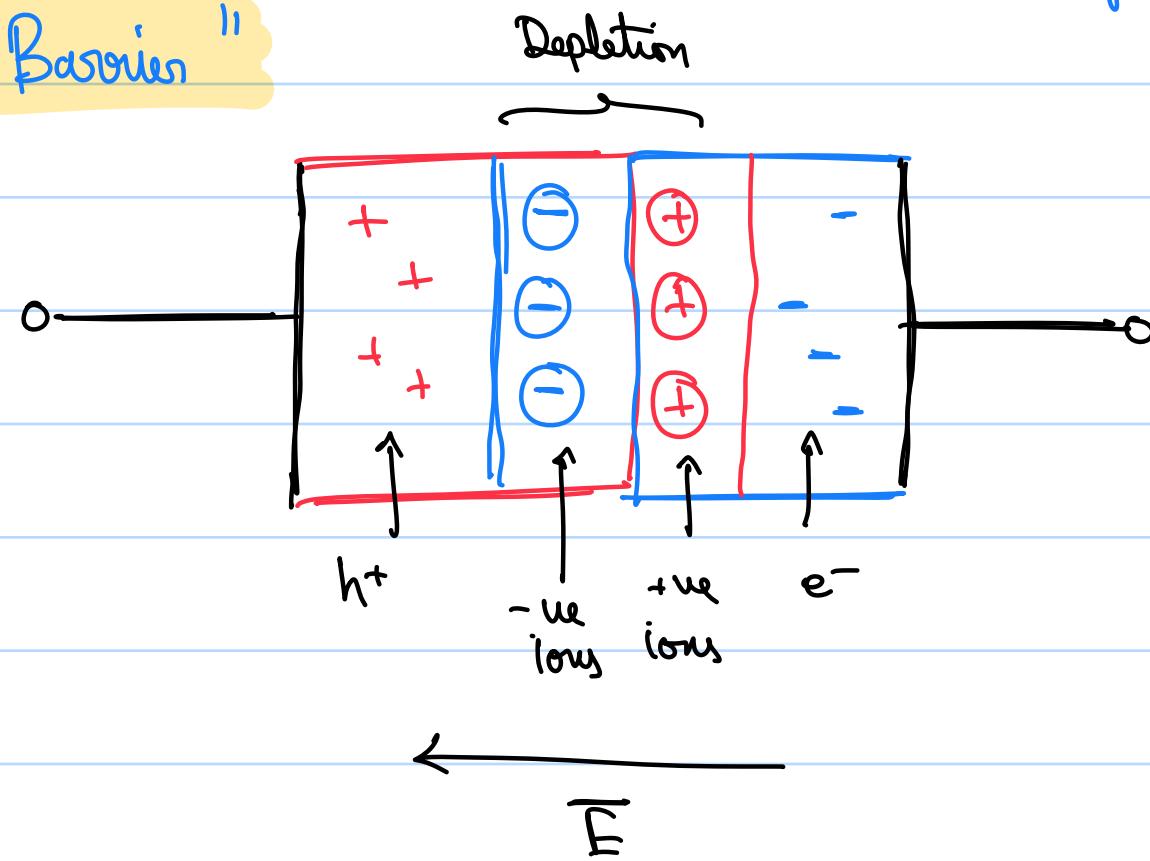
- Physical Structure :



- Made out of a single crystal of Si by injecting different dopants on each side of the crystal.
- The ends of the crystal are fixed to metal contacts.
- Operation Under Open Terminals :-
- Due to difference in concentration of holes and electrons across the junction, a diffusion current is generated, by holes $p \rightarrow n$ and electrons $n \rightarrow p$.

- In the p side, some electrons from the n side will combine with the holes close to the junction. This creates a region with no charge carriers, close to the junction.
- Similar thing happens on the n side with $n^+ \rightarrow e^-$.
- This creates a region in the junction called depletion / carrier depletion / space charge region.
- This region still has bound ions of the opposite polarity. i.e. p side has -ve ions, n side has +ve ions.

- These ions create an \vec{E} between them, that prevents further diffusion. "Barrier"



- Appearance of the barrier voltage reduces the diffusion effect across the junction.

- Drift Current : (I_s)

- Diffusion of majority carriers form the major component of the diode current.
- Drifting of minority carriers is the other component of diode current.
- The barrier electric field accelerates free electrons in the p-side into the n-side (vice versa, the holes). This creates a current from the n side to the p-side, opp to diffusion.
- Dependent on temperature since it is dependent on thermally generated electron-hole pairs.
- Independent of depletion voltage since any small value of V_0 is enough to push the minority carriers.
- At equilibrium,

$$I_D = I_S$$

If $I_D > I_S$, space charges $\uparrow \Rightarrow \vec{E} \uparrow \Rightarrow I_D \downarrow$

If $I_D < I_S$, space charge $\downarrow \Rightarrow \vec{E} \downarrow \Rightarrow I_D \uparrow$

↳ since the minority

carriers will neutralize the ions.

- Tension Built In Voltage :-

$$V_0 = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

Doping conc.

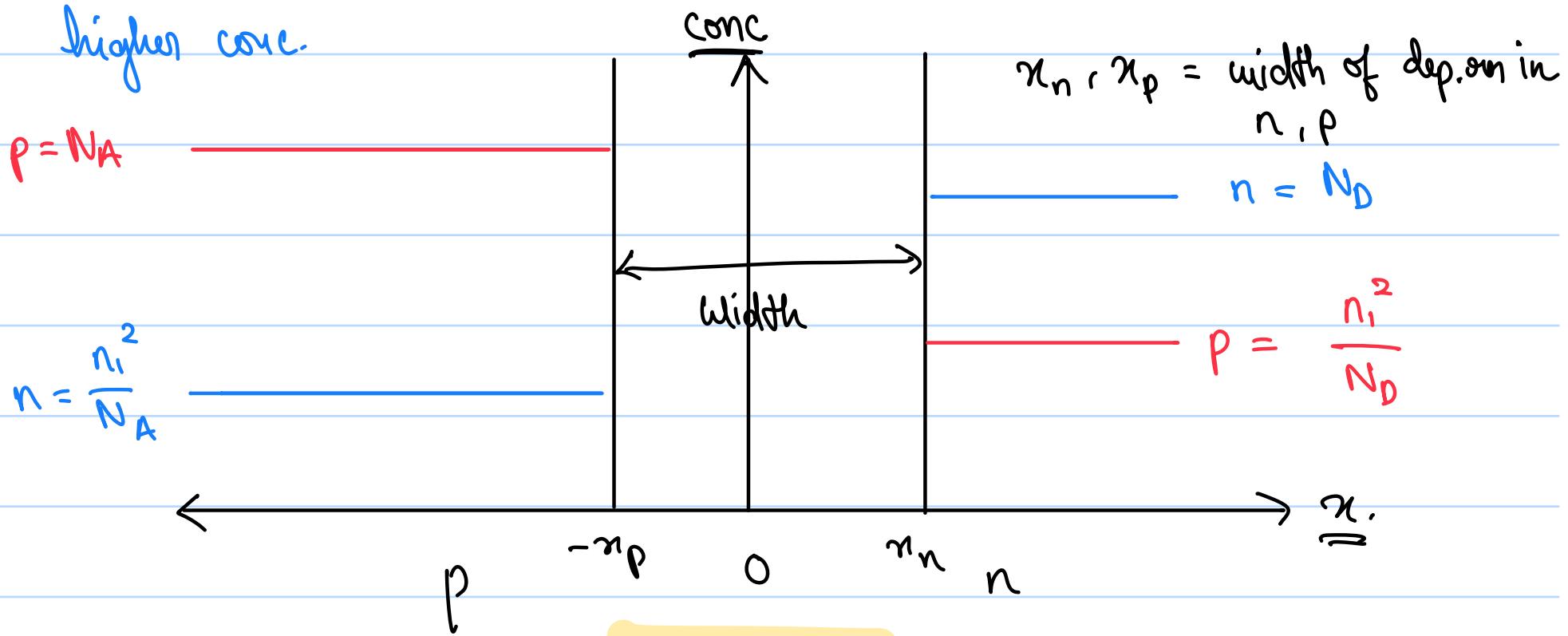
Intrinsic conc.

For Si, $V_0 = 0.6 - 0.9V$

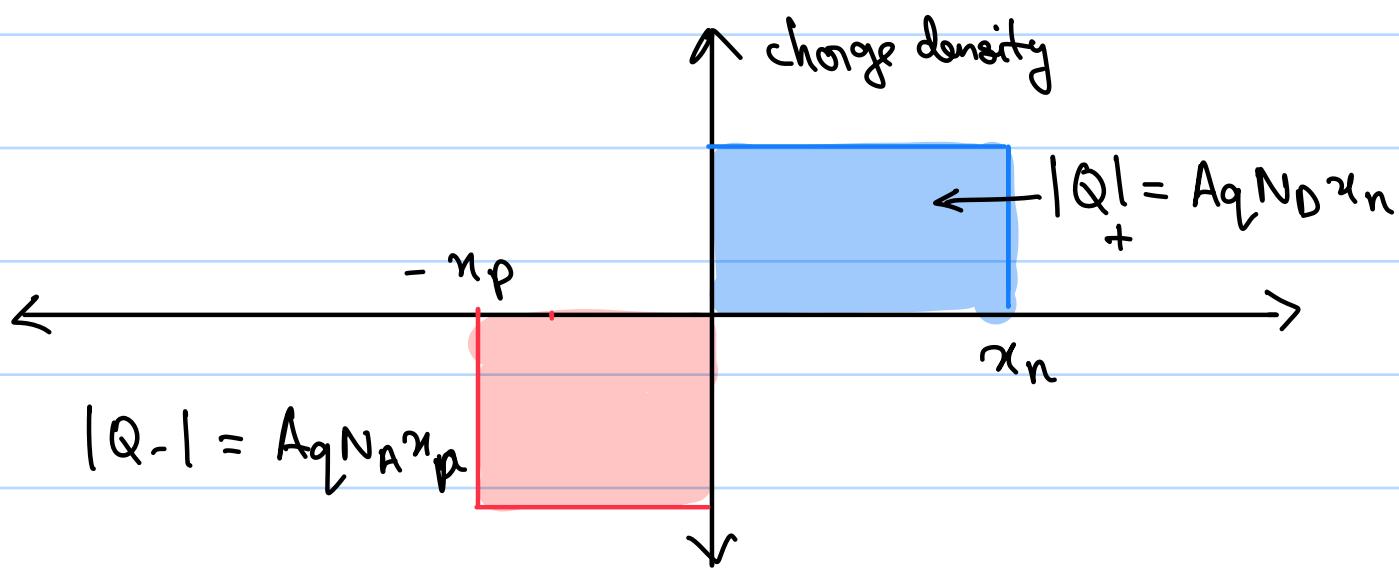
- This voltage is balanced by potentials at the metal-semiconductor contacts.

- Width of Depletion Region :-

- When $N_A > N_D$, the depletion region extends further into the n side, to counteract the excess diffusion that may occur due to higher conc.



$N_A > N_D$



- Since, to maintain neutrality,

$$|Q_+| = |Q_-|$$

$$= Aq N_D n_n = Aq N_A n_p$$

$$= \frac{n_n}{n_p} = \frac{N_A}{N_D}$$

- The width of the depletion layer is given by,

$$w = n_n + n_p = \sqrt{\frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) V_0}$$

$$\Rightarrow n_n = w \frac{N_A}{N_A + N_D}$$

$$n_p = w \frac{N_D}{N_A + N_D}$$

- The charge in each region is given by,

$$Q = Aq \left(\frac{N_A N_D}{N_A + N_D} \right) w$$

$$= Q = A \sqrt{2\epsilon q} \left(\frac{N_A N_D}{N_A + N_D} \right) V_0$$

- pn Junction Under Applied Voltage :-

- Open Circuit : $I_D = I_S$, $V = V_0$
- Fwd Bias : $I_D > I_S$, $V = V_0 - V_f$
- Rev Bias : $I_D < I_S$, $V = V_0 + V_R$

• In Reverse Bias,

- V_R is in same direction of V_0 .
- Diffusion \downarrow
- Drift current is the major component of current. So resulting current is very small. $\approx I_S$.

$$- \text{Width } w = n_n + n_p = \sqrt{\frac{2q}{\epsilon} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 + V_R)}$$

↳ **w increased**

$$\Rightarrow Q = A \sqrt{2\epsilon q \left(\frac{N_A N_D}{N_A + N_D} \right) (V_0 + V_R)}$$

↑
∴ **Q increases**

• In forward bias,

- V_f is opposite

- Diffusion \uparrow

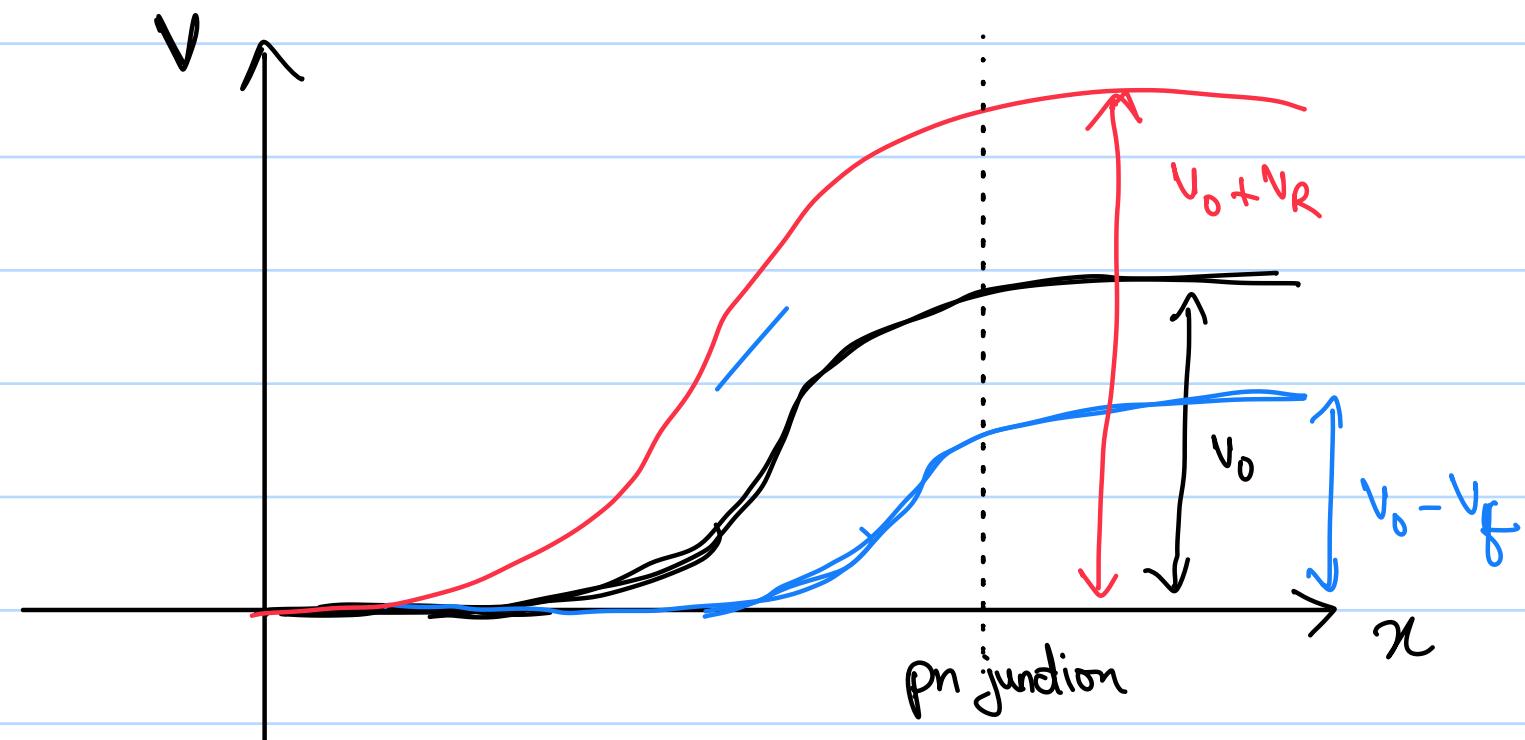
$$-\omega = \int \frac{2\epsilon}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_0 - V_f)$$

$\omega \downarrow$

$$Q = A \int 2\epsilon q \left(\frac{N_A N_D}{N_A + N_D} \right) (V_0 - V_f)$$

$Q \downarrow$

- External current $I = I_D - I_S$, which is substantial.



- IV Characteristics:-

- In forward bias, the hole conc. in the edge of the **n** side that is towards the junction, i.e given by,

$$P_n(x) = P_{no} e^{\frac{V}{V_T}}$$

P_{no} - hole conc. in n side during equilibrium.

$$\begin{aligned} \text{Excess conc} &= P_{no} e^{\frac{V}{V_T}} - P_{no} \\ &= P_{no} (e^{\frac{V}{V_T}} - 1) \end{aligned}$$

This increase in minority charge carriers, decays exponentially with length, so,

$$p_n(x) = p_{no} + (\text{Excess conc}) e^{-(x-x_n)/L_p}$$

↙ edge of dep. arm.
 ↑ diffusion length

$$= p_n(x) = p_{no} + p_{no} (e^{\nu/v_T} - 1) e^{-(x-x_n)/L_p}$$

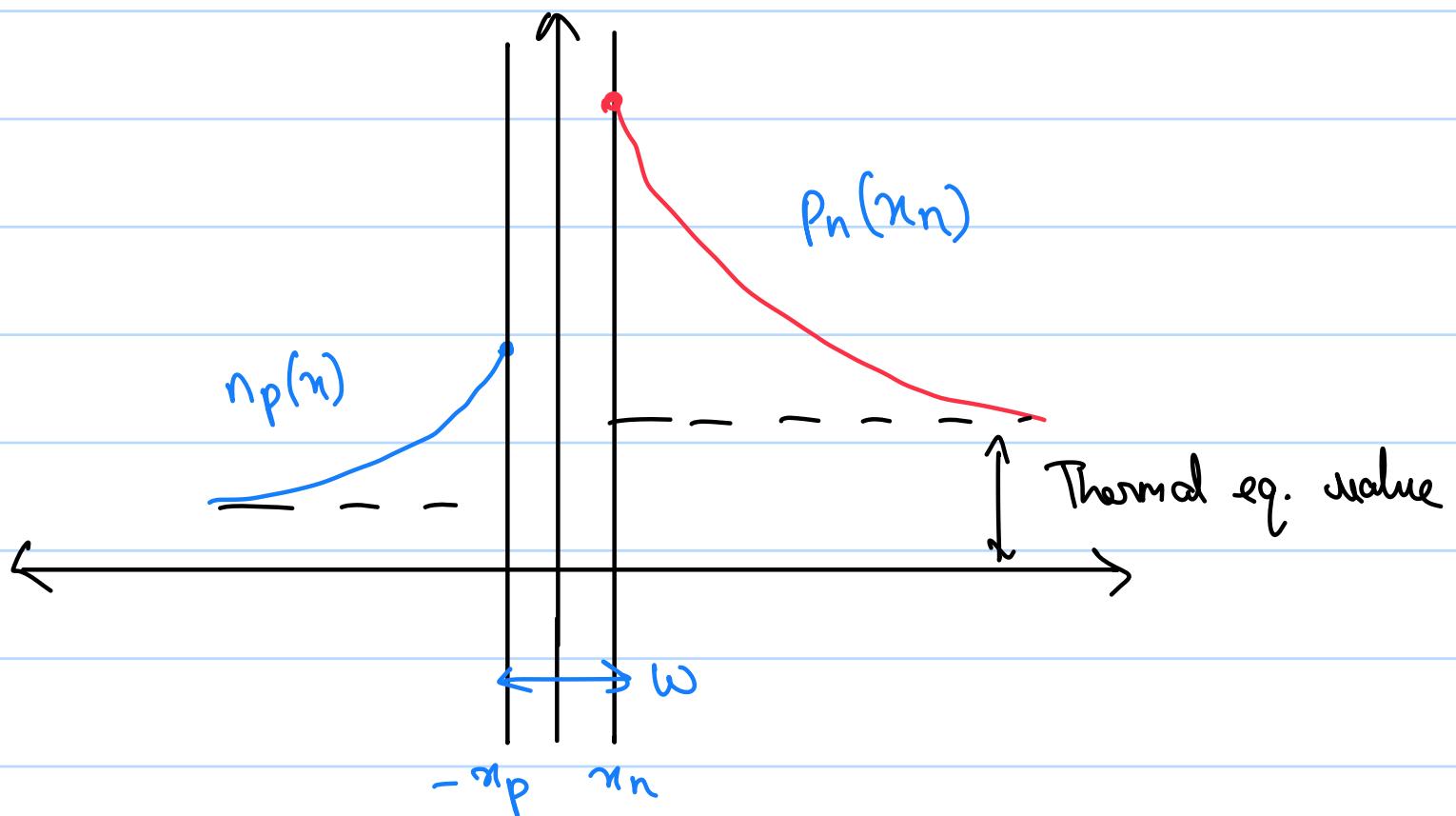
Here, we can find current density by,

$$J_p(x) = -q D_p \frac{dp_n(x)}{dx}$$

$$J_p(x) = q \left(\frac{D_p}{L_p} \right) p_{no} (e^{\nu/v_T} - 1) e^{-(x-x_n)/L_p}$$

$$\Rightarrow J_{p\max}(x) = q \left(\frac{D_p}{L_p} \right) p_{no} (e^{\nu/v_T} - 1)$$

↑ at $x = x_n$



Minority Carriers Across the Diode

Assuming $N_A > N_D$

- This decrease in $p_n(x)$ is due to recombination of the minority holes with the majority electrons.

- This recombination implies that there must be some other current replenishing the electrons. This current is from the external circuit.

- Similar behaviour is expected in the p side,

$$J_n(-x_p) = q \left(\frac{D_n}{L_n} \right) n_{p0} (e^{V/V_T} - 1)$$

- Total Current Density,

$$J = J_p + J_n = q \left(\frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0} \right) e^{V/V_T} - 1$$

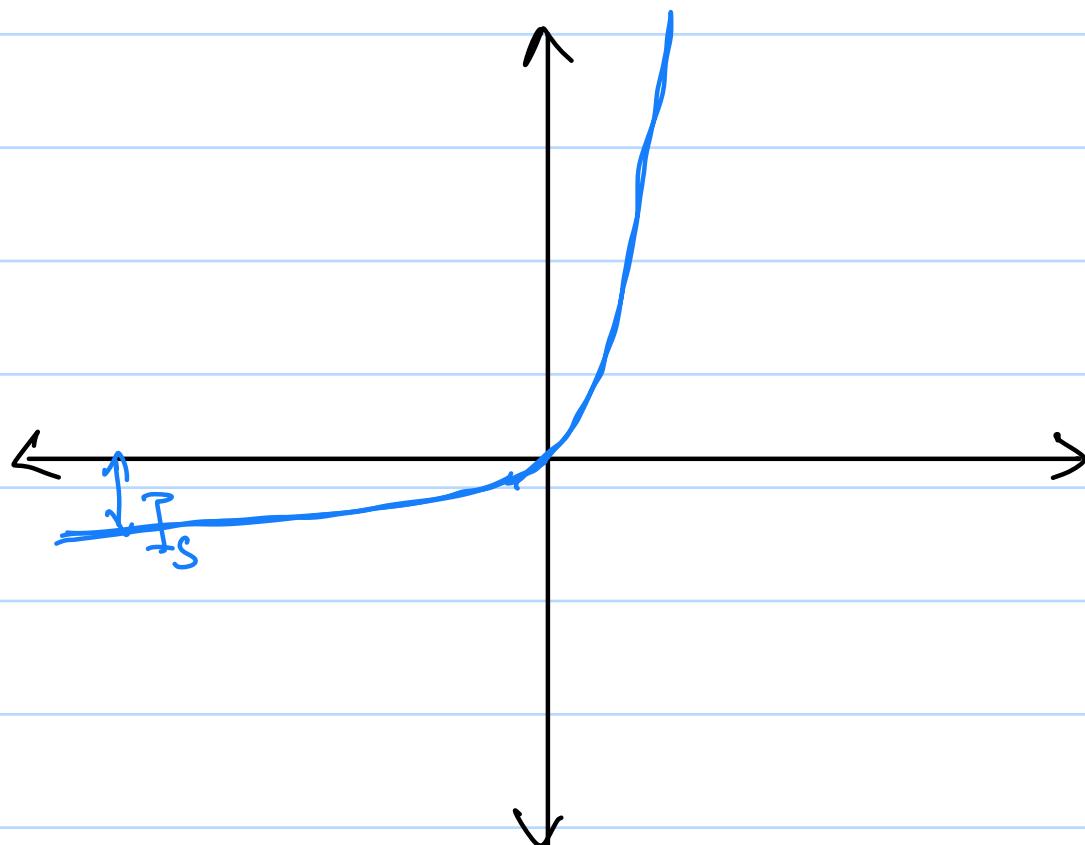
$$\Rightarrow I = A q n_i^2 \left(\frac{D_n}{L_n N_D} + \frac{D_p}{L_p N_A} \right) (e^{V/V_T} - 1)$$

Since at steady state, rev. bias current = J_S ,

$$\Rightarrow I = J_S (e^{V/V_T} - 1)$$

J_S is termed as saturation current. It does not depend on voltage. $J_S = A q n_i^2 \left(\frac{D_n}{L_n N_D} + \frac{D_p}{L_p N_A} \right)$

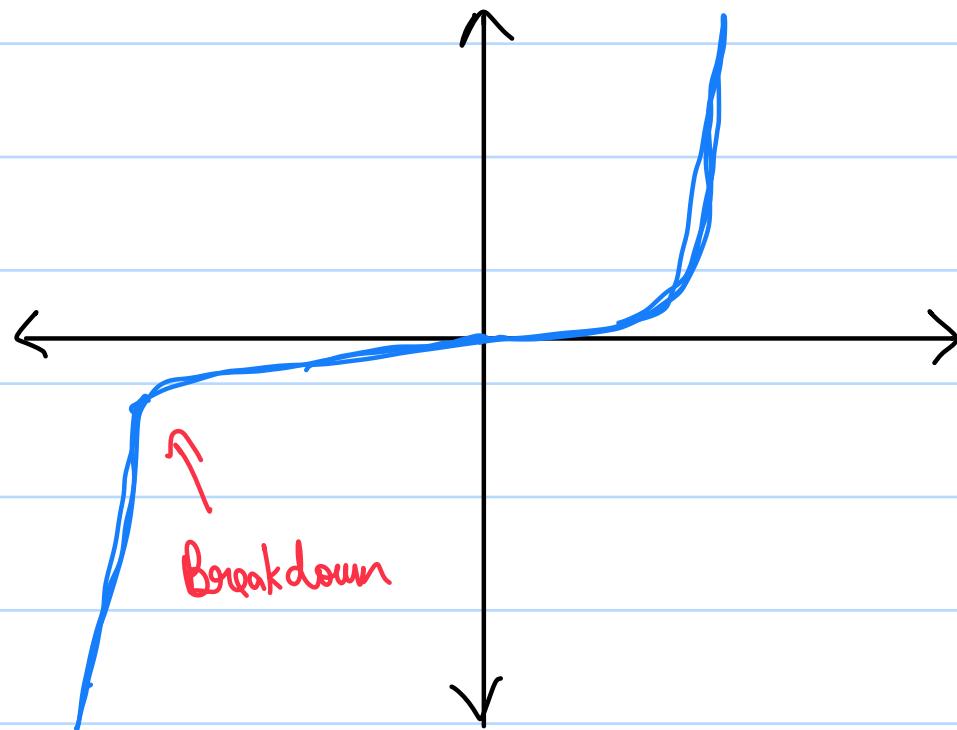
J_S increases with area and also with temperature (due to n_i^2)



I-V Characteristics

- Reverse Breakdown :-

- When the reverse bias increases continuously, the magnitude of the current increases dramatically.
- This increase in current doesn't change the voltage across the diode significantly. (Zener Diode working principle)
- This phenomenon is a Junction Breakdown. It is not a permanent effect.



- There are 2 possible causes

1) Zener effect :

- Electric field in the depletion layer breaks the covalent bonds in the crystal lattice.
- Breakage of bonds create new electron-hole pairs.

2) Avalanche :

- The minority charge carriers in the drift current have enough energy to break bonds.
 - This creates a chain reaction that greatly increases the number of charge carriers and significantly increases the current through it.
 - During a breakdown, the voltage across the diode will be nearly constant. This fact is used to build voltage regulators (Zener diode).
- Capacitance in the P-N Junction :-

The p-n junction has 2 charge storage mechanisms.

1) Depletion / Junction Capacitance :-

Associated with the charge stored in the depletion region.

During reverse bias,

$$Q_j = A \sqrt{2\epsilon \mu \frac{N_A N_D}{N_A + N_D} (V_0 + V_R)}$$

$$\Rightarrow Q_j = K \sqrt{V_0 + V_R}$$

Therefore, the charge stored in the depletion region is non-linearly related to the voltage.

We can define,

$$C_j = \frac{dQ_j}{dV} = \frac{K}{2\sqrt{V_0 + V_R}}$$

At zero bias,

$$C_{j0} = \frac{K}{2\sqrt{V_0}}$$

∴

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

This formula is applicable when we have an abrupt junction, i.e. the boundary b/w p and n is clear.

In a gradual junction,

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^m}$$

m = grading coeff.

2) Diffusion Capacitance :-

Associated with the excess minority carriers.

- In equilibrium, there is a certain amount of minority charge on each side of the junction.
- When an external voltage is applied, the concentrations must change to form a new equilibrium.

$$C = \left(\frac{T_T}{V_T}\right) I_f$$

T_T : Mean transit time

I_f : Fwd Current

→ Modelling of The Diode :-

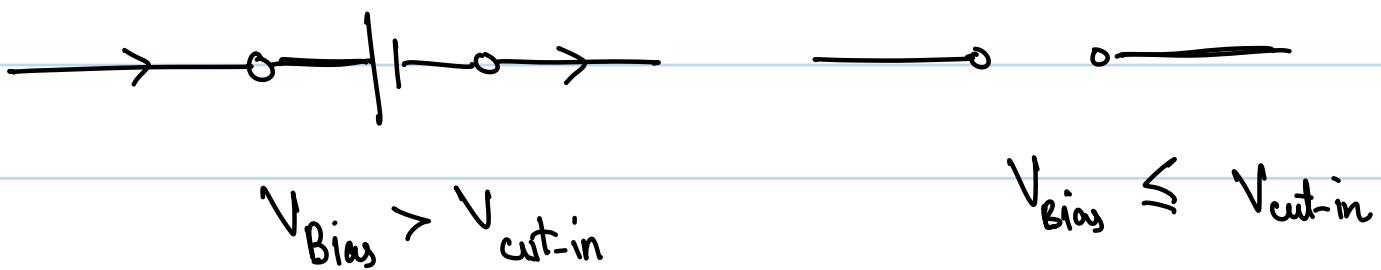
1) Open - Closed Wire Model :- (Ideal Diode Model)



- Most simplistic model of the diode

- Useful for large voltages but gives large error in small voltages due to absence of cut-in voltage.

2) Constant Voltage Model :-



- Takes into account the cut-in voltage of the diode.
- Does not take into account the exponential growth of current across the diode; and also the variation in internal resistance.

3) Exponential Model :-



$$I = I_s (e^{\frac{V}{kT}} - 1)$$

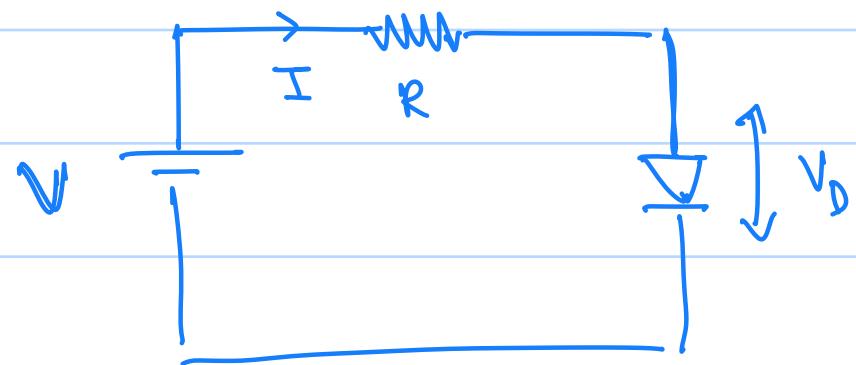
- Most accurate model of the diode.

- For large V , $I \approx I_s e^{\frac{V}{kT}}$

- Iterative Analysis :-

By KVL,

$$I = \frac{V - V_D}{R}$$



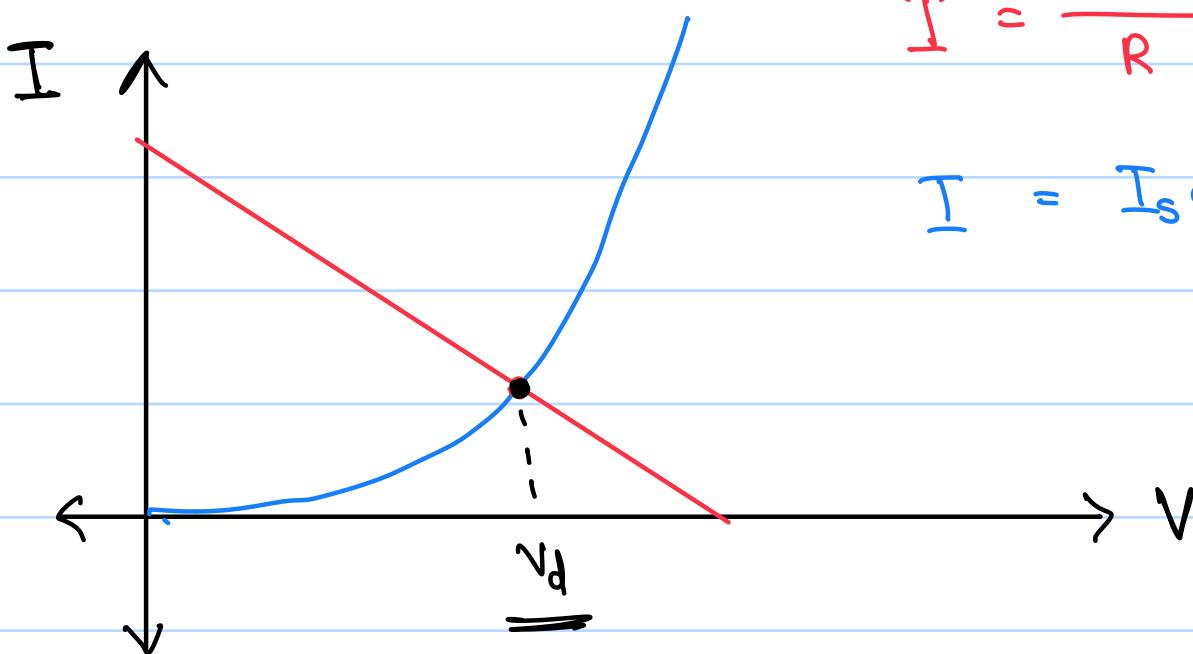
To accurately calculate V_D , first assume V_D and calculate for I in the above formula.

Then apply this I in,

$$I = I_s e^{\frac{V_D}{kT}}$$

and calculate V_D . Repeat this until change in V_D is negligible.

- Load Line :-



$$I = \frac{V - V_D}{R}$$

$$I = I_s e^{\frac{V}{V_T}}$$

The intersection of the 2 curves gives us the current through the circuit and the diode voltage.

- We can connect capacitors in parallel to the diode to take into account the diffusion capacitance and the junction capacitance.

→ Small Signal Model :-

A small signal is defined as a signal whose amplitude is negligible compared to its DC offset

$$V_S(t) = V + v_o(t) \quad \text{Amp}(v_o(t)) \ll V$$

We know that,

$$I = I_s e^{-\frac{V}{V_T}}$$

$$= I(t) = I_s e^{-\frac{(V + v_o(t))}{V_T}}$$

$$I(t) = I_s e^{-\frac{V}{V_T}} e^{-\frac{v_o(t)}{V_T}}$$

$$= I(t) = I_D e^{-V_o(t)/V_T}$$

I_D = current due to DC offset.

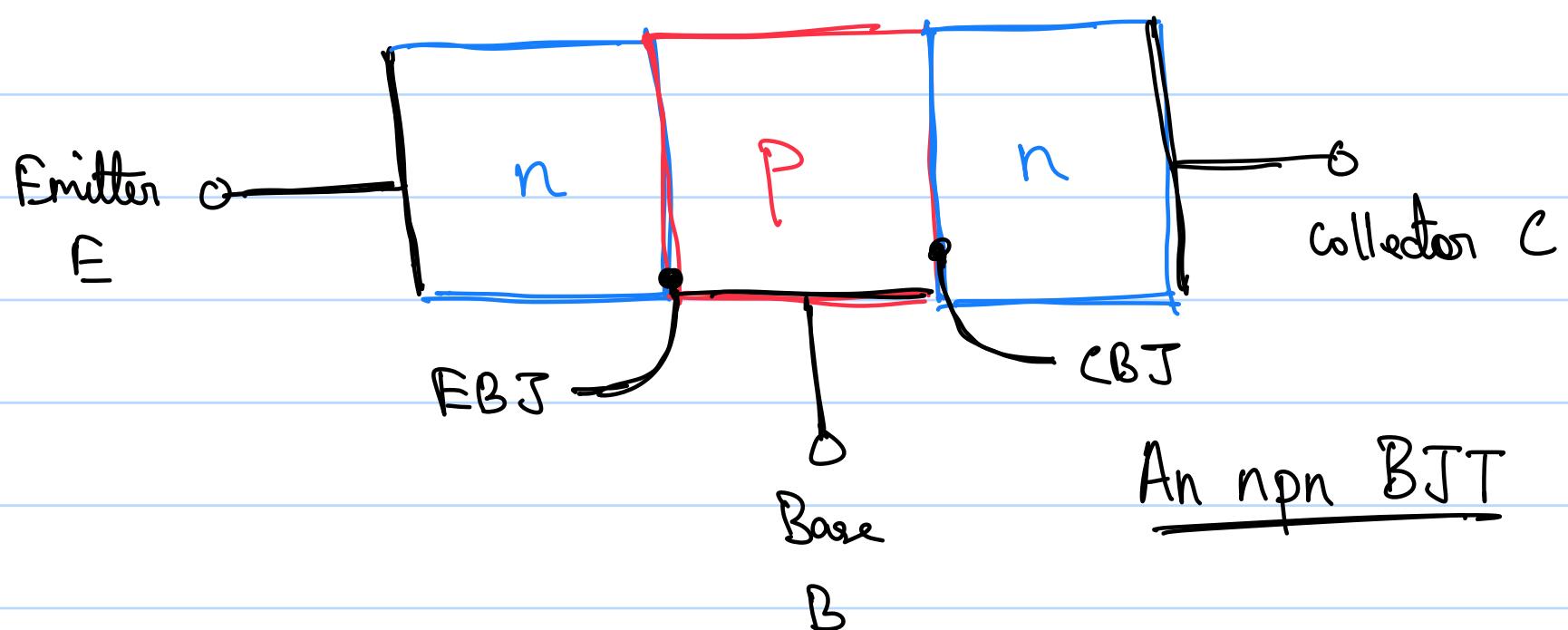
If $V_o(t) \ll V_T$

$$\Rightarrow I(t) = I_D \left(1 + \frac{V_o(t)}{V_T} \right)$$

By Taylor Series Expansion

$$\Rightarrow i(t) = \frac{I_D}{V_T} V_o(t) \rightarrow \text{current due to small signal}$$

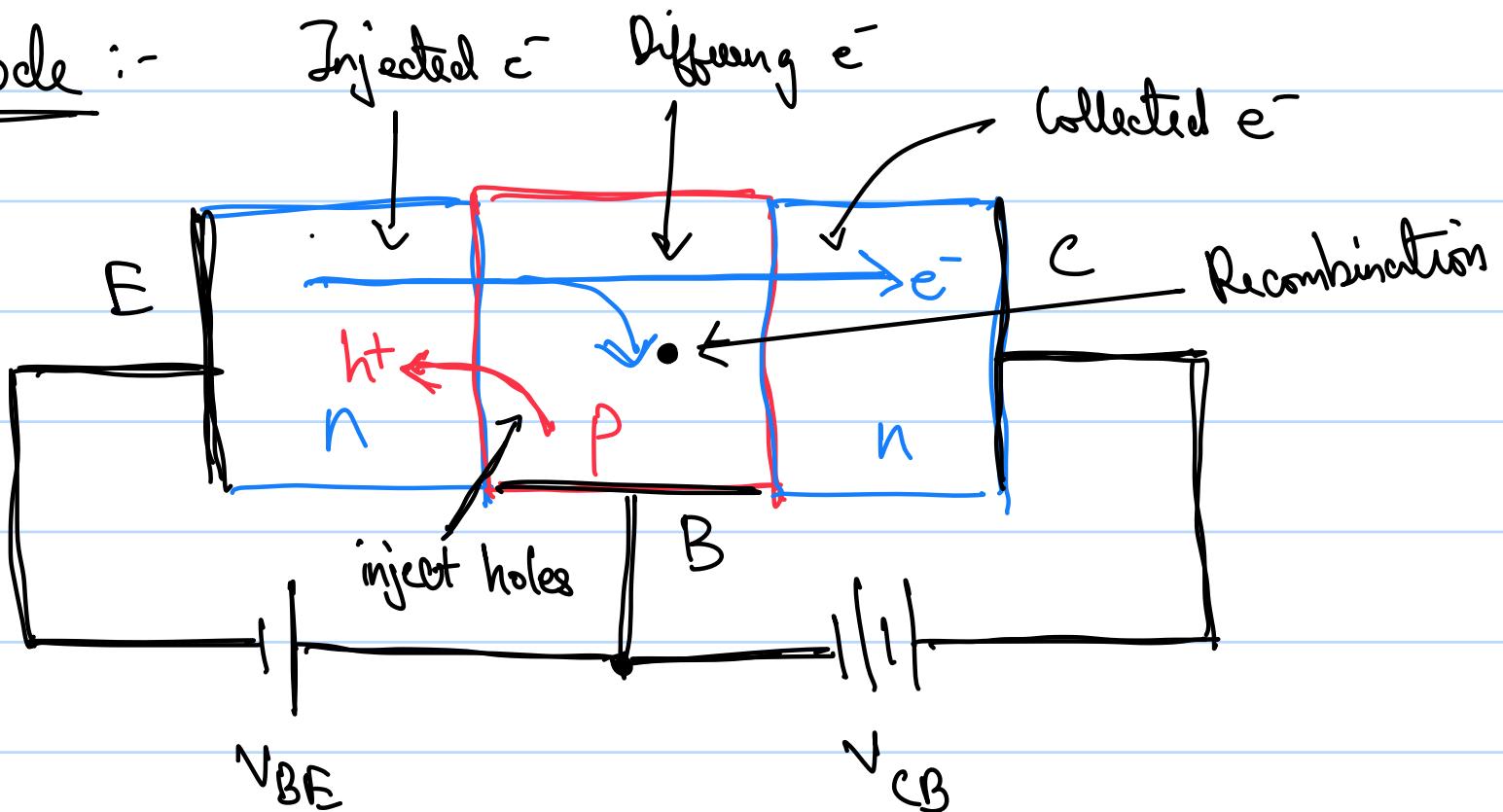
→ Bipolar Junction Transistor :-



- A BJT is a 3 terminal device that can be used to perform some logical operation
- It has 3 doped regions, collector (C) region, base (B) region, emitter (E) region, resulting in 2 junctions.
- Depending on the bias across these 2 junctions, there are 3 modes of operation for the BJT.

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

i) Active Mode :-



- $V_{coll} > V_{base} > V_{emit}$
- Current will flow across the BJT.
- The current will have 2 components,
 - 1) Current due to injection of e^- from emitter to base
 - 2) Current due to injection of h^+ from base to emitter
- It is desirable to have the first component higher than the second one. This is done by having a **heavily doped emitter**.
- The current will flow "out" of the emitter lead, dominated by electrons.
- When the injected electrons reach the base, they will be minority carriers and will start to adopt a gradient across the base region.

- Since the base is thin, the concentration gradient will be somewhat linear, starting at $n_p(0)$ on the EBJ and lowest (0) on the CBJ.

$$\bullet n_p(0) \propto e^{\frac{V_{BE}}{N_T}}, \quad n_p(0) = n_{p0} e^{\frac{V_{BE}}{N_T}}$$

↳ Thermal. equili concentration

- There is zero concentration in the CBJ due to the high potential in the collector region, causing the electrons to be swept across the CBJ.

- The sidewall diffusion current is given by,

$$I_n = A_F q D_n \frac{dn_p(n)}{dn} \quad (\text{flows from C to E})$$

$$= A_F q D_n \left(-\frac{n_p(0)}{w} \right) \rightarrow \begin{matrix} \text{Width of Base} \\ \xrightarrow{\hspace{100pt}} \text{Gross Surr Area of EBJ.} \end{matrix}$$

- Some electrons may recombine, affecting the gradient slightly, causing the slope to be higher towards the EBJ than the CBJ.

- Collector Current :-

- The current I_n brings electrons to the CBJ, from where they are swept across the CBJ depletion region.

- This sweeping across causes a current to flow in the opposite direction (i_c). $i_c = I_n$

- i_c flows from C to E.

$$\Rightarrow i_c = I_s e^{\frac{V_{BE}}{V_T}} \text{ by } i_c = I_n$$

where I_s is the saturation current given by, also called saturation current

$$I_s = \frac{A_e q D n_p}{W}$$

$$= \frac{A_e q D_n n_i^2}{N_A W} \leftarrow \text{Temp. dependence}$$

Temp doubles with $\Delta S^\circ C$

This shows that i_c does not depend on V_{CB} , ie, as long as there is a +ve voltage difference across V_{CB} , i_c will flow.

- Base Current :-

- The base current has 2 components :

- 1) Injection of holes from base into the emitter

- 2) Replenishment of holes by the external circuit.

- Both these components are proportional to $e^{\frac{V_{BE}}{V_T}}$.

\therefore Final base current is proportional to $e^{\frac{V_{BE}}{V_T}}$

- $i_B = \frac{i_c}{\beta} = \left(\frac{I_s}{\beta} \right) e^{V_{BE}/V_T}$ Transistor parameter / common-emitter current gain,
- β inversely depends on w and also directly on N_A/N_D .

- Emitter Current :-

- By KCL,

$$i_E = i_c + i_B$$

$$\Rightarrow i_E = i_c + \frac{1}{\beta} i_c$$

$$i_E = \left(\frac{\beta+1}{\beta} \right) i_c$$

$$\Rightarrow i_E = \left(\frac{\beta+1}{\beta} \right) I_s e^{V_{BE}/V_T}$$

$$\Rightarrow i_E = \frac{I_s}{\alpha} e^{V_{BE}/V_T}, \quad \alpha = \frac{\beta}{\beta+1}$$

- For any transistor, α is a constant and less than 1.
- α : Common Base Current Gain

Equivalent Circuit Models :-

- The forward bias voltage V_{BE} causes an exponential current i_c to flow in the collector terminal.

\Rightarrow Collector terminal is a current source with

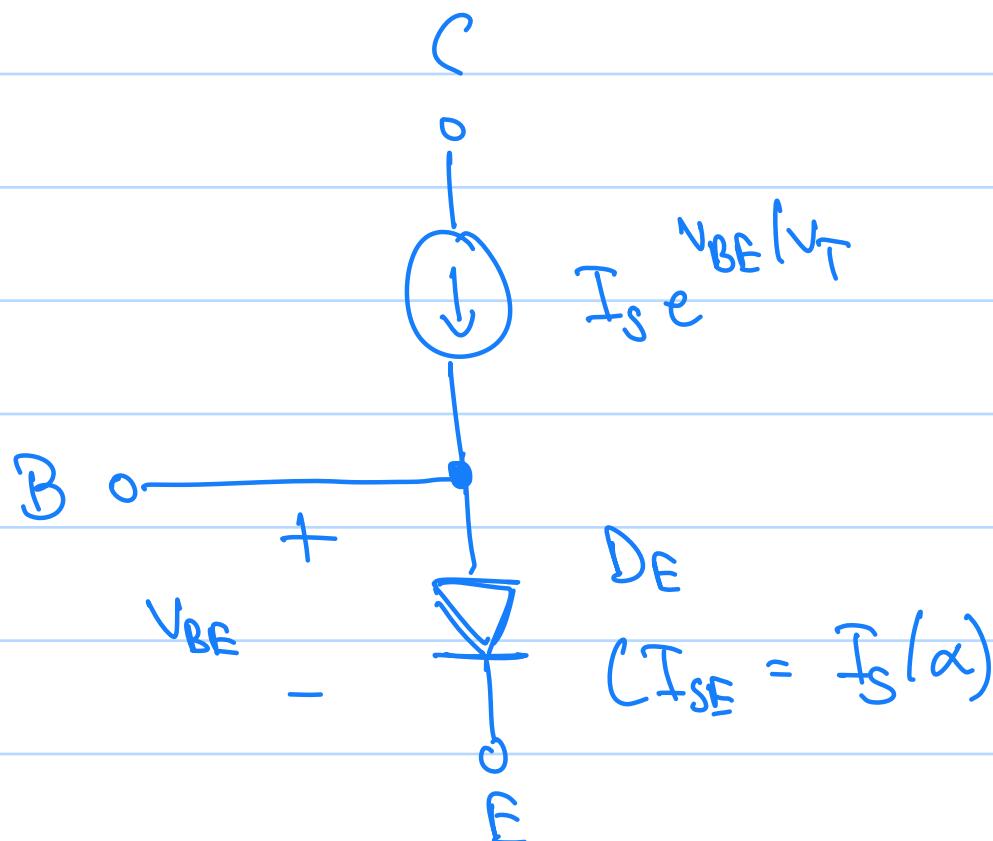
$$i = I_s e^{V_{BE}/V_T}$$

- The base current i_B is $1/\beta$ of i_c and $i_E = i_c + i_B$. Since $i_B \ll i_c$ normally ($\beta \gg 1$), $i_E \approx i_c$.

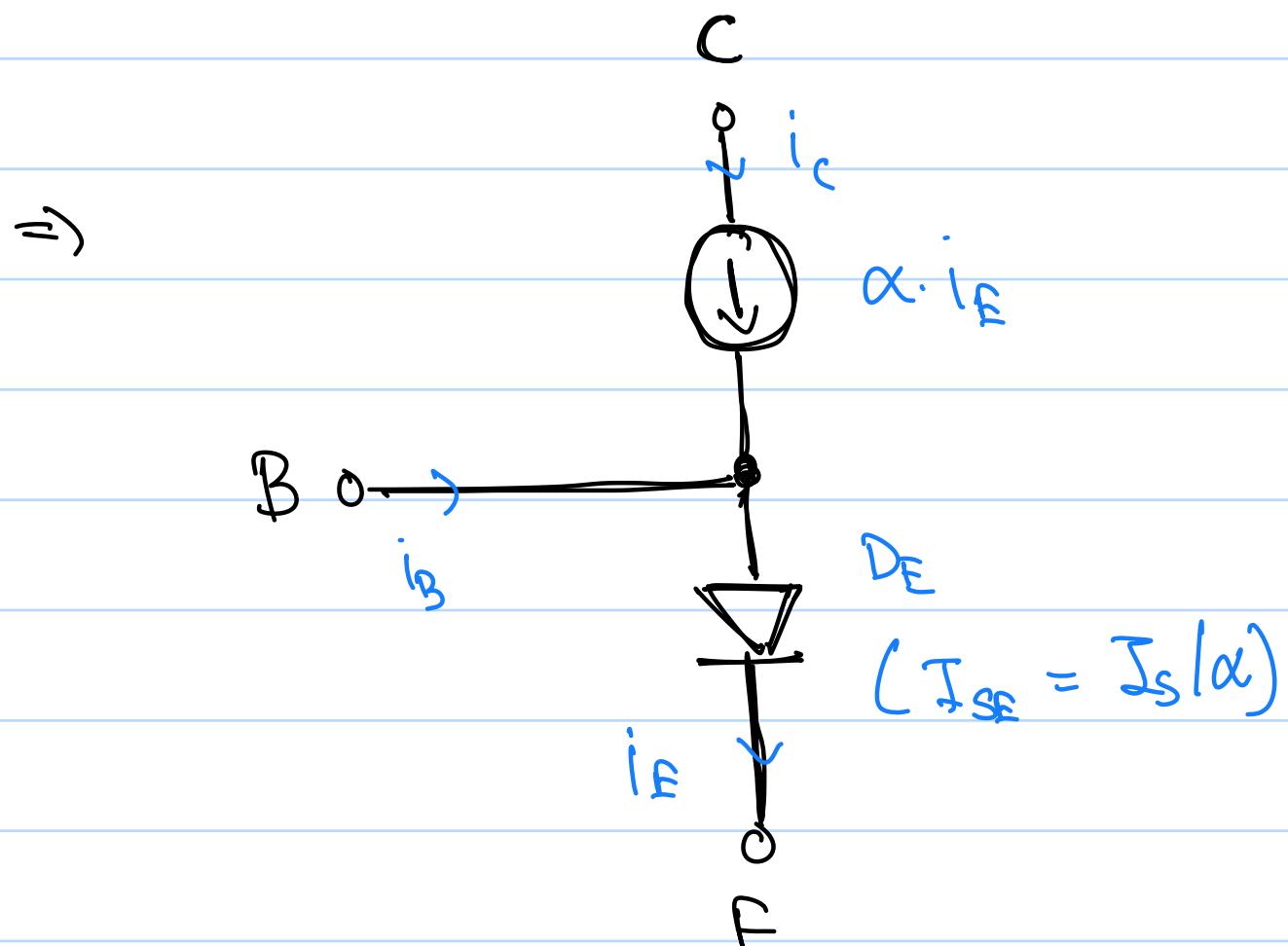
More accurately

$$i_E = \frac{i_c}{\alpha}$$

- Equivalent circuits :



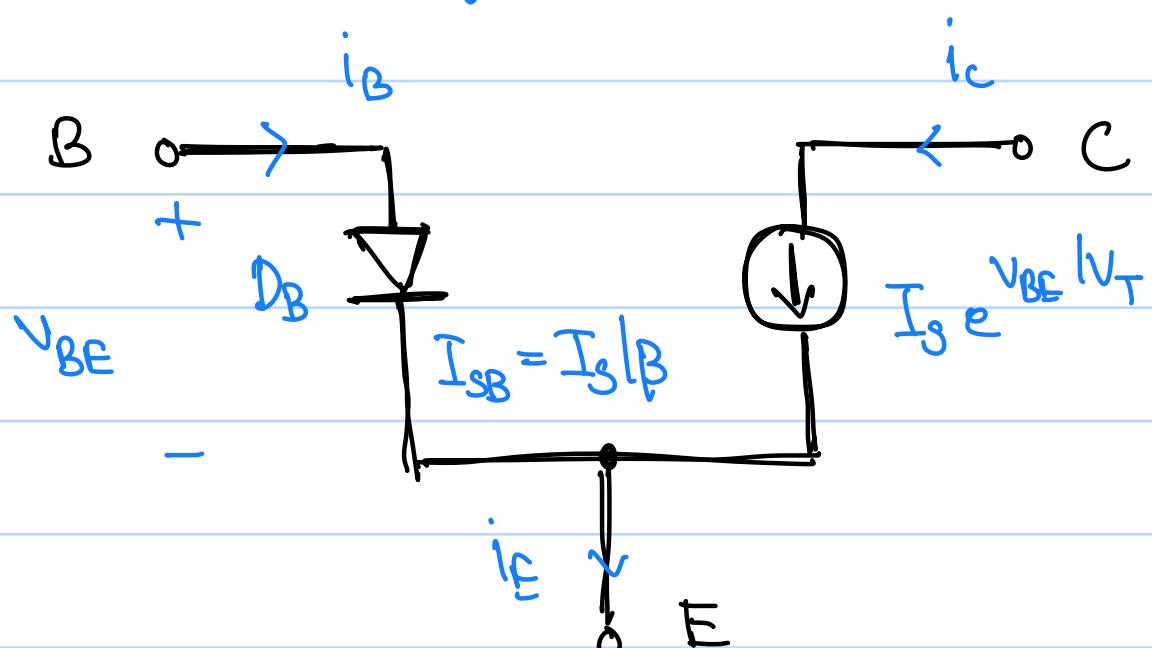
The current source is now voltage controlled. To make it current controlled, we can use the fact that $i_c = \alpha i_E$.



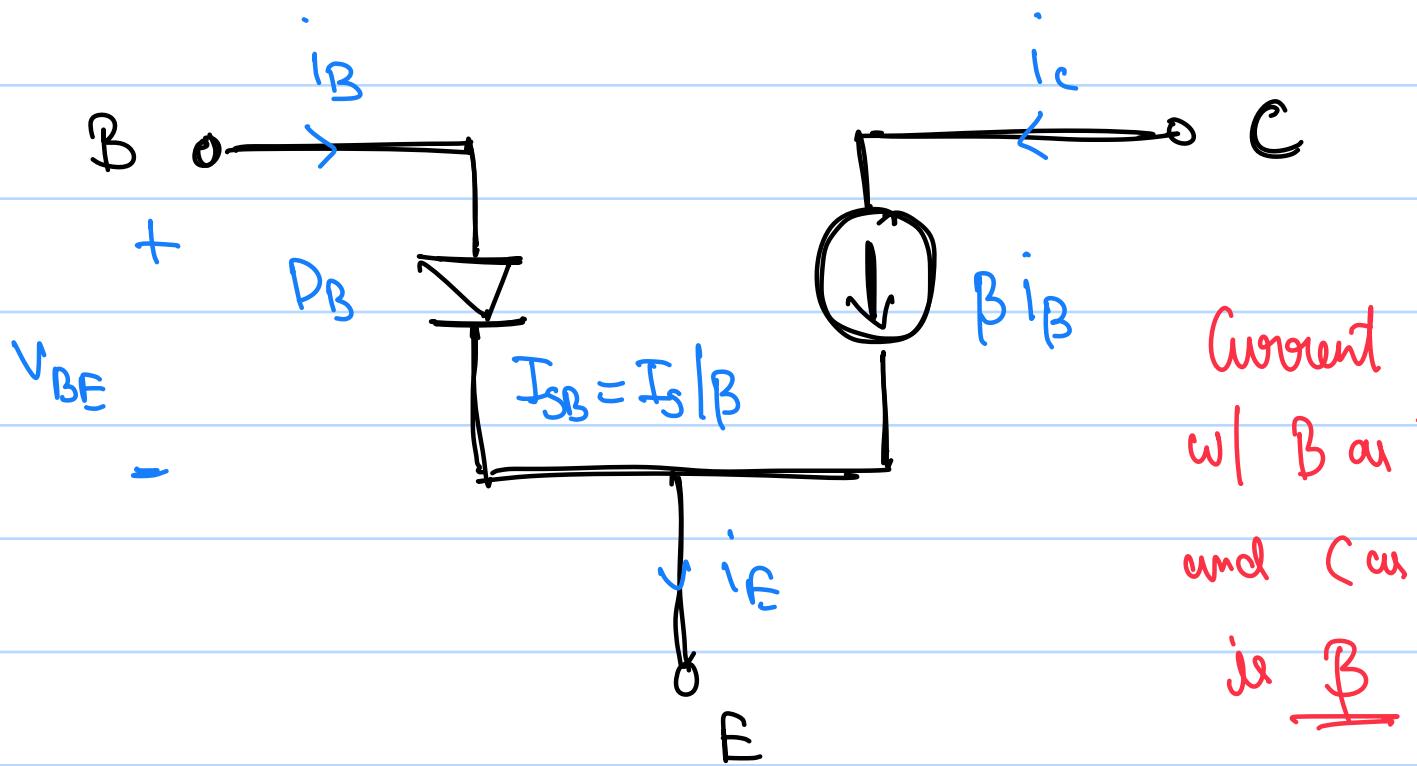
If the transistor is used as a 2 port network with input at E and output at C and B as common terminal, the current gain observed is α .

Thus α is Common Base Current Gain

This is also an equivalent circuit,

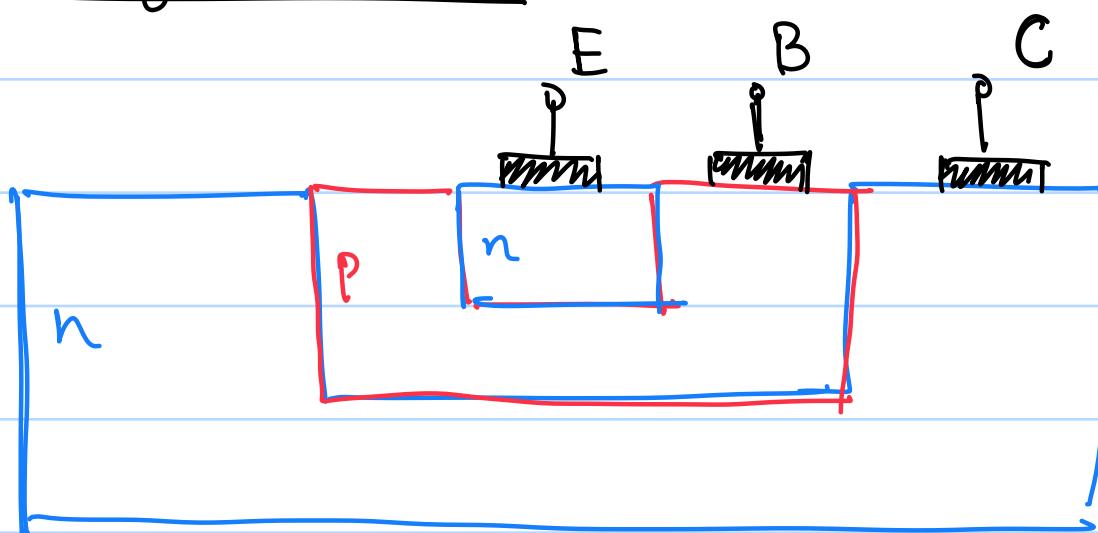


Again, by using the fact that $i_C / i_B = \beta$, we can make the voltage controlled current source into a current controlled one.



Since the above models work for any positive value of V_{BE} ,
there are **large scale models**.

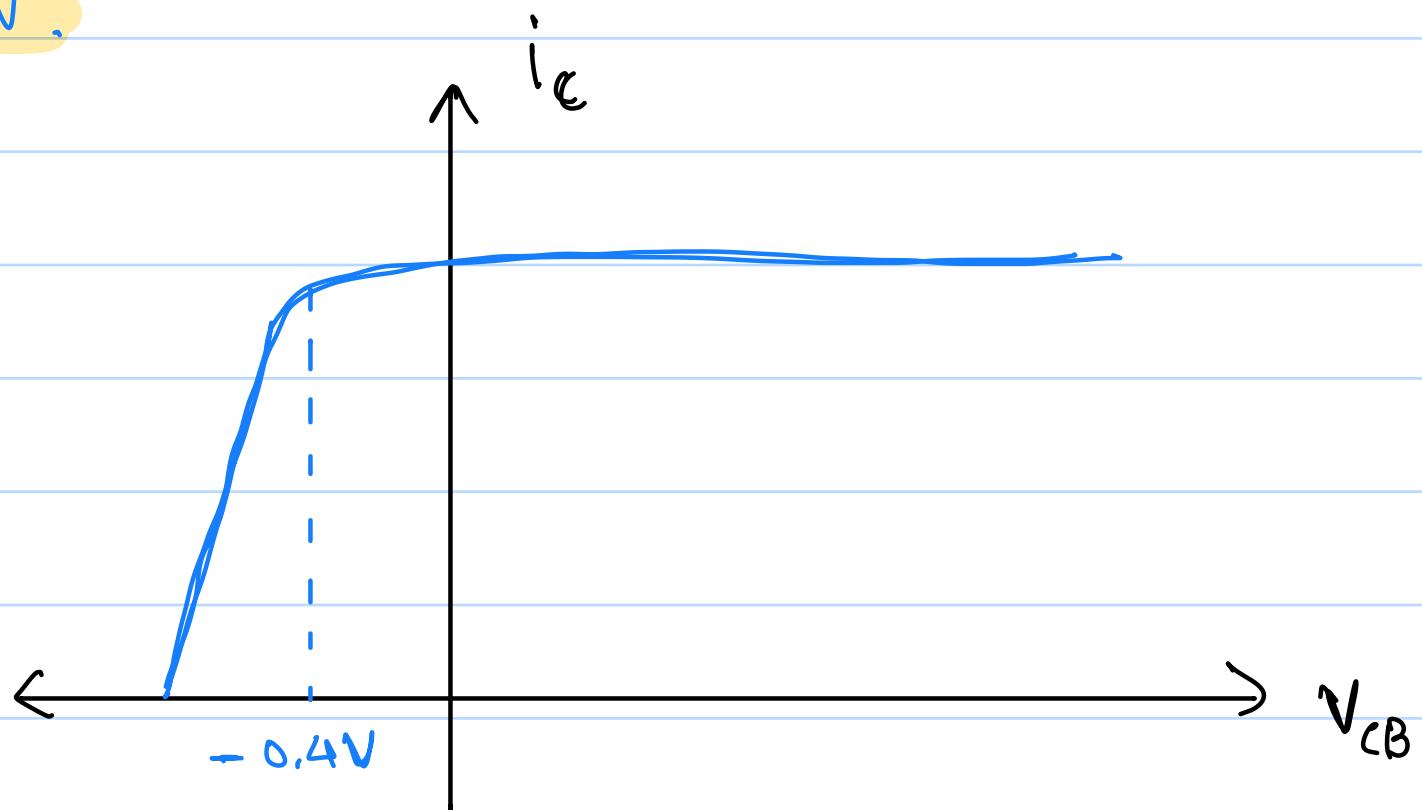
→ Structure of Transistors :-



- The collector region fully surrounds the base, to capture any electrons injected into the thin base.
- CBJ is much larger than EBJ. Thus the saturation current at CB is much higher than that of EB (typically 10x to 100x)

2) Saturation Mode:

- For active mode, we need CBJ in reverse bias.
- However CBJ is still in reverse bias until approximately $-0.4V$.



- As shown before, i_C is independent of V_{CB} , but only if $V_{CB} > -0.4V$.
- If $V_{CB} < -0.4V$, the junction goes into forward bias.
- For a forward conducting CBJ,

$$i_C = I_S e^{\frac{V_{BE}}{V_T}} - I_{SC} e^{-\frac{V_{CB}}{V_T}}$$

- The base current will become,

$$i_B = (I_S / \beta) e^{V_{BE}/V_T} + I_{SC} e^{-V_{CB}/V_T}$$

- If we take the ratio of i_C / i_B now,

$\beta_{\text{forced}} = \frac{i_C}{i_B} \leq \beta \leftarrow (\text{Transistor parameter})$

- We can use this fact to check if the transistor is operating in active / saturation mode.

- $V_{CE \text{ sat}} = V_{BE} - V_{BC}$

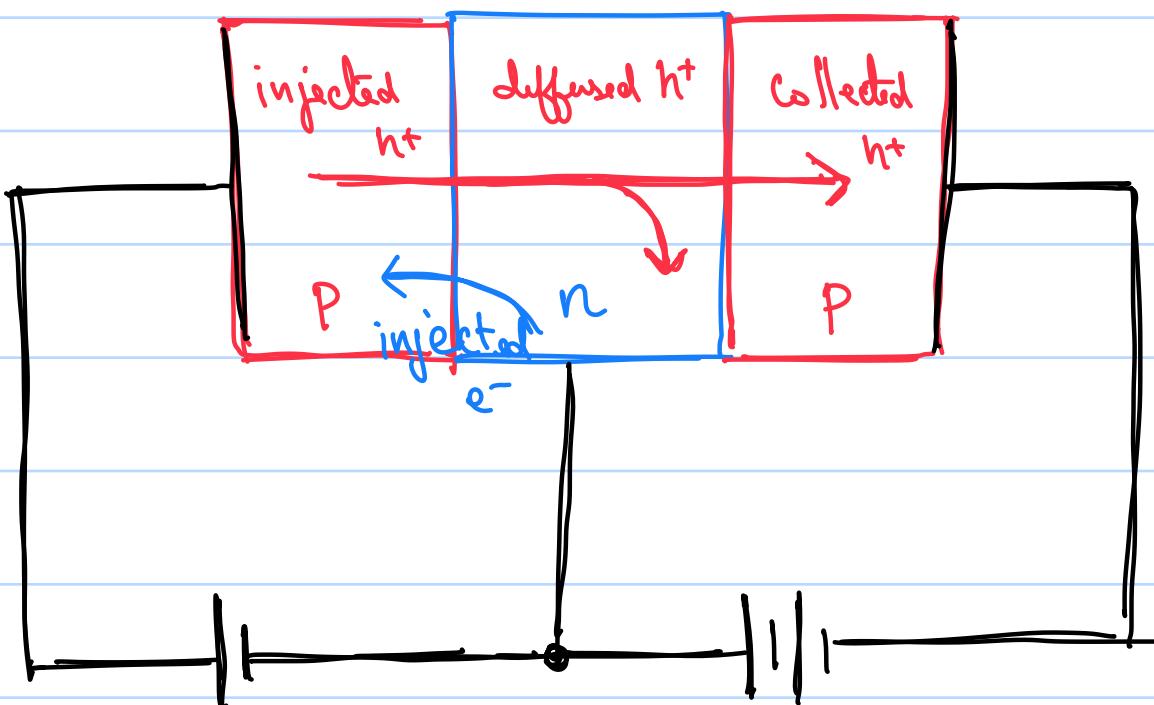
Since CBJ has a larger area than EBJ, V_{BC} will be smaller than V_{BE} , so,

$$V_{CE \text{ sat}} \approx 0.1 \text{ V to } 0.3 \text{ V}$$

Therefore, when a transistor is in saturation mode, its V_{CE} by default is taken as 0.2V (deep in saturation) / 0.3V (edge of sat.).

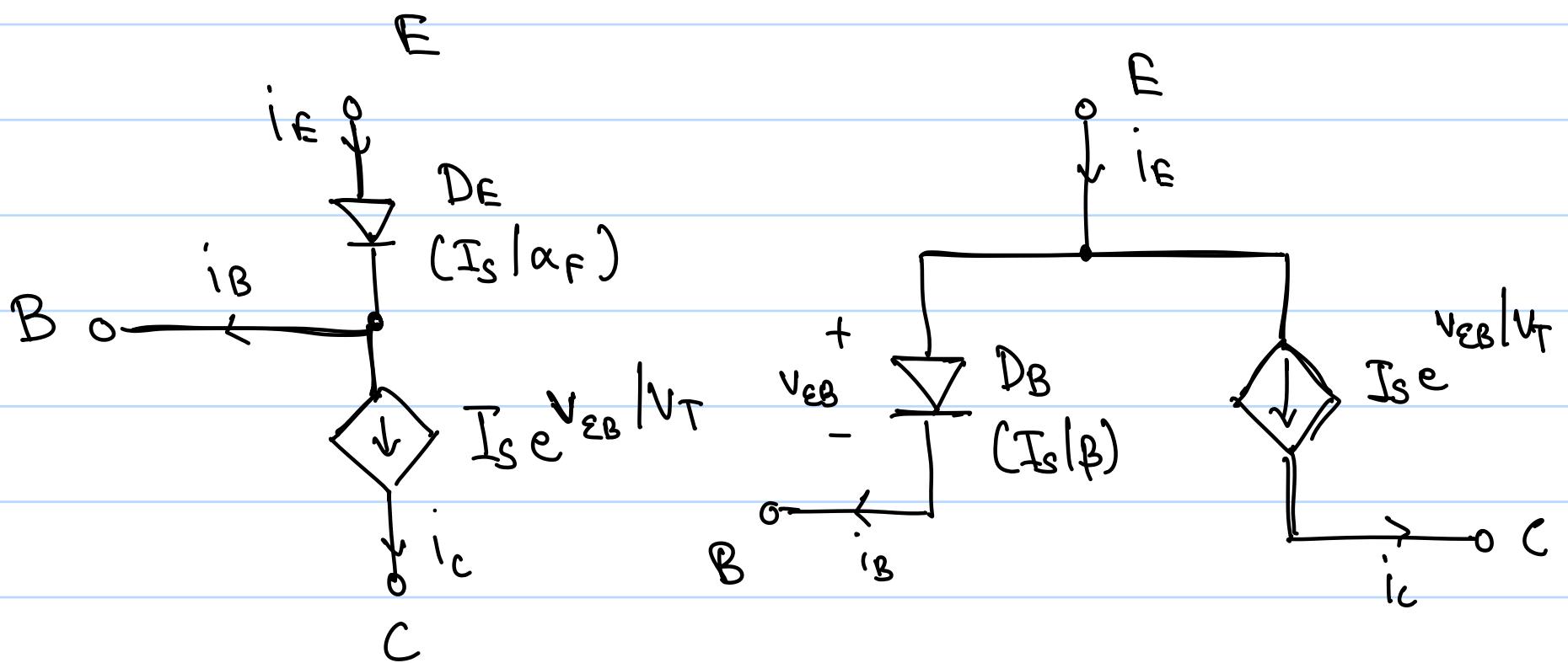
→ PNP Transistor :-

- Operates similarly to npn.
- Conduction in Pnp is mainly through holes, unlike npn.



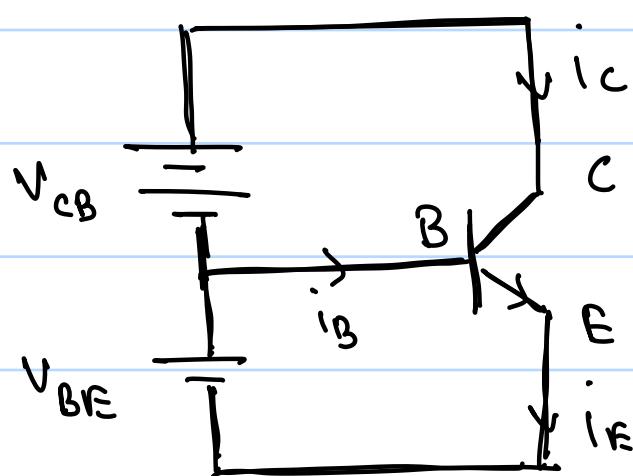
- Base Current is made of 2 components,
 - 1) Electron injection from base to emitter } i_B
 - 2) Diffusion of holes coming from emitter }
- The remaining holes will reach the CBJ and will be swept across the collector region, becoming collector current i_C
- At saturation mode, CBJ is forward biased and will start to conduct in the opp. direction of i_C , decreasing the final i_C .

• Large signal PNP models :

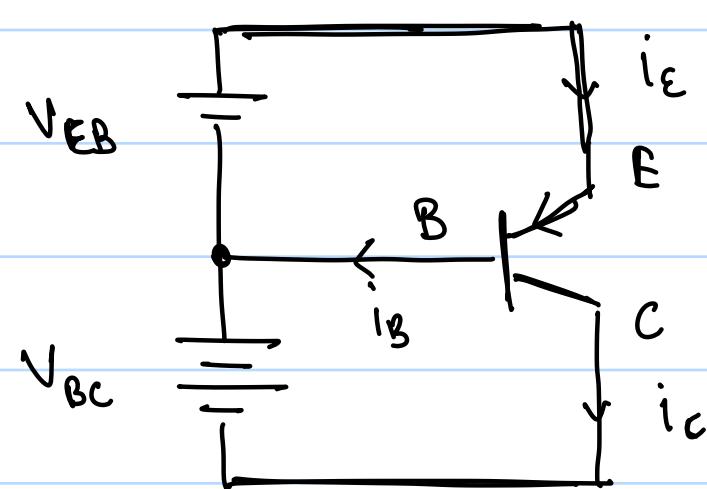


→ Current Conventions :-

npn



pnp



Active Mode:

$$V_{CB} \geq 0.4V$$

Active Mode:

$$V_{BC} \geq 0.4V$$

