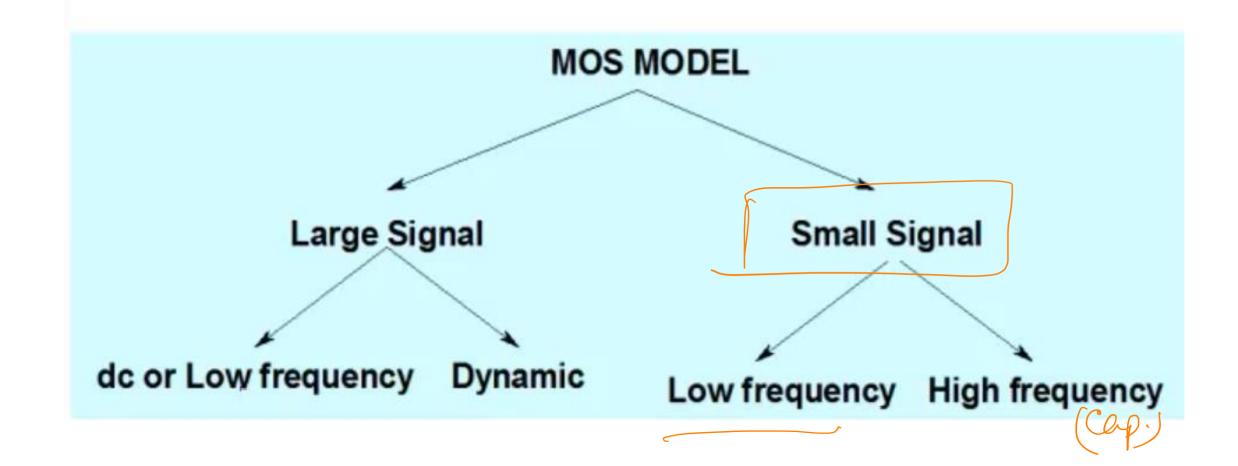
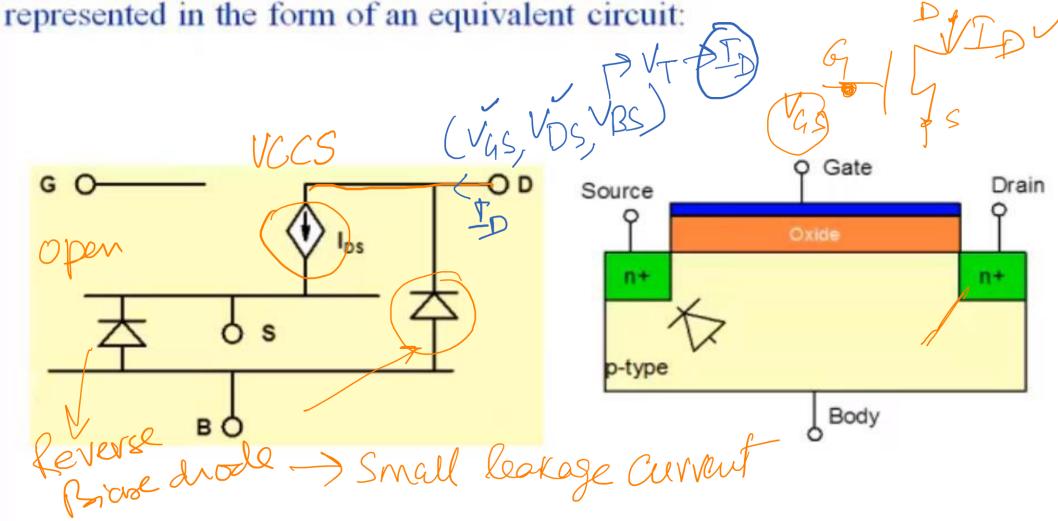
MOS models: The classification of models can be done on the basis of magnitude and frequency of applied voltages



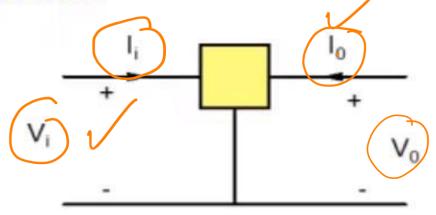
The dc model of the transistor in triode and saturation region can be

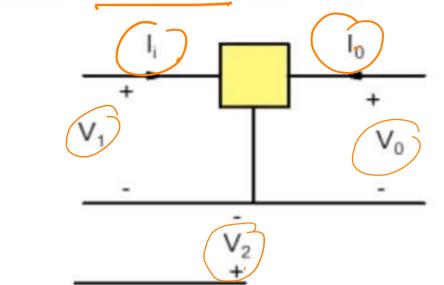


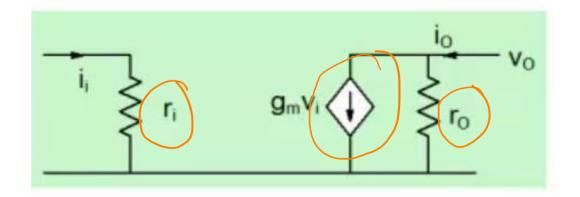
Series resistance associated with gate, source, drain and body terminals is not shown but can play an important role.

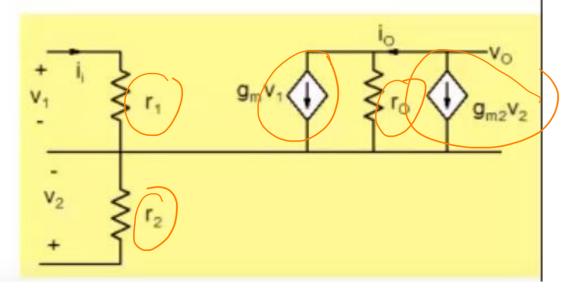
Complete small signal model (dc) for a 3-terminal unilateral

device.



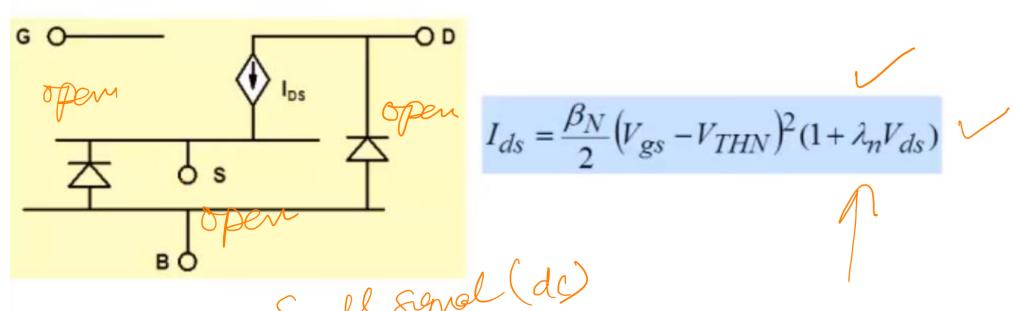






Small Signal Model (dc/low frequency)

Saturalin



$$V_{gs} = V_{GSQ} + v_{gs}$$

$$V_{ds} = V_{DSQ} + v_{ds}$$

$$V_{sb} = V_{SBQ} + v_{sb}$$

$$I_{ds} = I_{DSQ} + i_{ds}$$

$$I_{DSQ} + i_{ds} = \frac{\beta_N}{2} \Big[V_{GSQ} + v_{gs} - V_{THN} \Big(V_{BSQ} + v_{bs} \Big) \Big]^2 \Big(1 + \lambda_n V_{DSQ} + \lambda_n v_{ds} \Big)$$
not really multiplication, but function

$$i_{ds} \approx I_{DSQ} \left\{ \left(\lambda_n v_{ds} + \frac{2v_{gs}}{V_{GSQ} - V_{THN}} + \frac{\gamma \times v_{bs}}{(V_{GSQ} - V_{THN}) \times \sqrt{2\varphi_F - V_{BSQ}}} \right) \right\}$$

$$\int_{C} \int_{C} \left(V_{4S} - V_{7} \right) i_{ds} = \frac{v_{ds}}{r_{o}} + \left(g_{m} v_{gs} + g_{mb} v_{bs} \right)$$

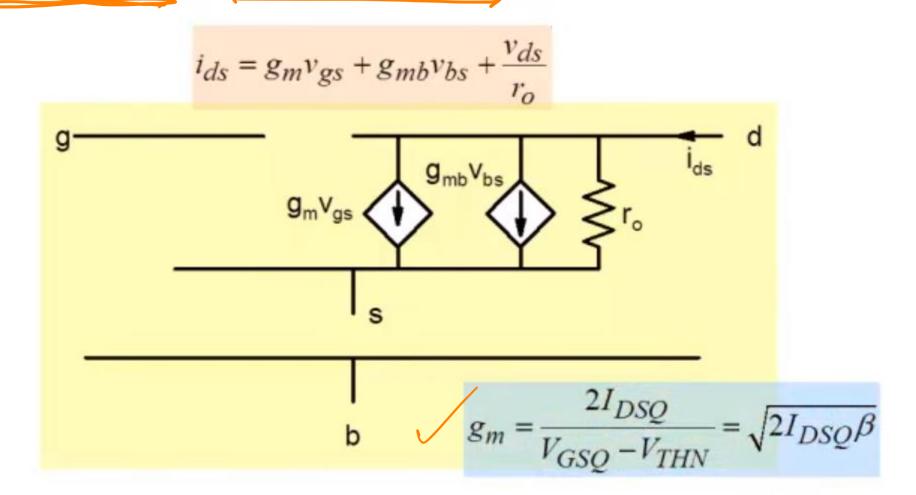
$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

$$\overbrace{g_m} = \frac{2I_{DSQ}}{V_{GSQ} - V_{THN}} =$$

$$g_{mb} = g_m.\eta$$

$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SBQ}}}$$

Low frequency Small Signal model



$$r_o = \frac{1}{\lambda_n I_{DSQ}}$$

$$g_{mb} = g_m.\eta$$

$$\sqrt{r_o} = \frac{1}{\lambda_n I_{DSQ}} \qquad \sqrt{g_{m\hat{b}}} = g_m.\eta \qquad \eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SBQ}}}$$

The small signal approximation $i_{ds} = g_m v_{gs}$ is accurate when

$$|V_{gs}| << 2(V_{GS} - V_{THN})$$

In BUT!

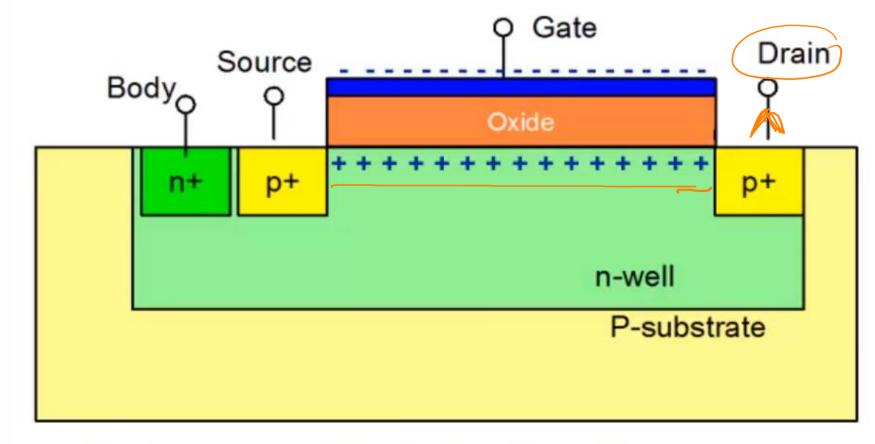
Whe < VT = KT

The < 28mV

In MOS Vge LCD VGS-VTHN

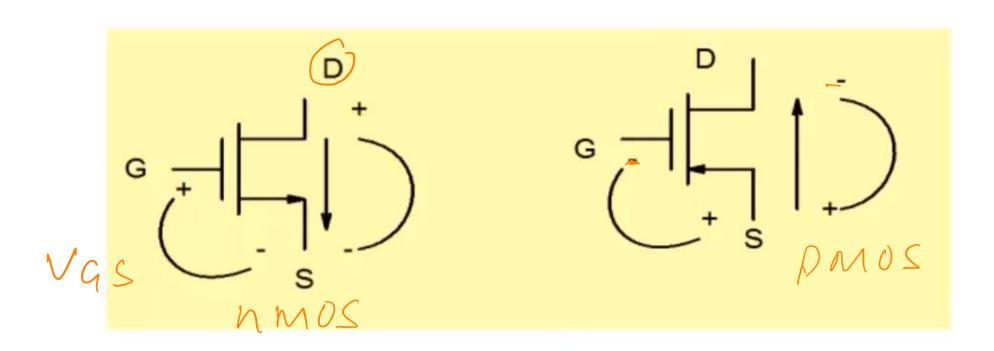
Dgs y 0.2 (Vas V) 0.2

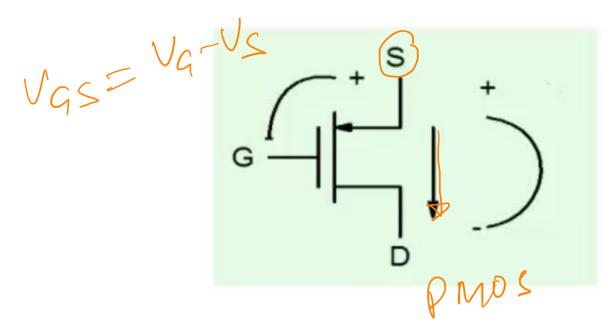
PMOS



V_{GS} is negative; Threshold voltage V_{TP} is negative

 $V_{\rm DS}$ is negative; $I_{\rm DS}$ is negative





$$V_{GSN} \to V_{SGP}$$

$$I_{DSN} \to I_{SDP}$$

$$V_{DSN} \to V_{SDP}$$

Transformations

$$V_{GSN} \rightarrow V_{SGP}$$
 $V_{DSN} \rightarrow V_{SDP}$ $V_{BSN} \rightarrow V_{SBP}$

$$V_{DSN} \rightarrow V_{SDP}$$

$$V_{BSN} \rightarrow V_{SBP}$$

$$V_{THN} \rightarrow -V_{THP}$$
 $I_{DSN} \rightarrow I_{SDP}$

$$I_{DSN} \rightarrow I_{SDP}$$

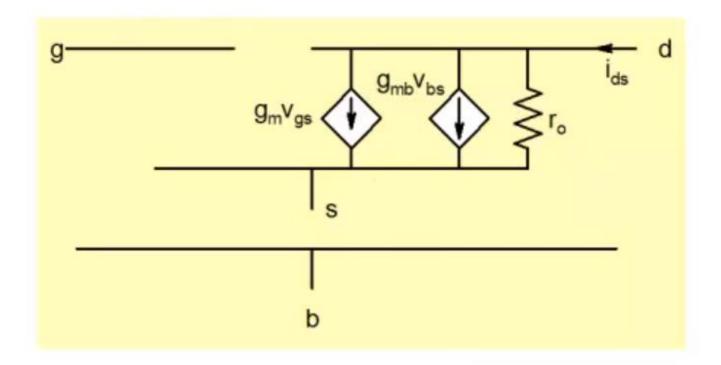
$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}] \rightarrow$$

$$I_{SD} = \frac{\beta_P}{2} (V_{SG} + V_{THP})^2 [1 + \lambda_p V_{SD}]$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + \frac{v_{sd}}{r_o}$$

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o} \text{ same as NMOS}$$

Small Signal Model



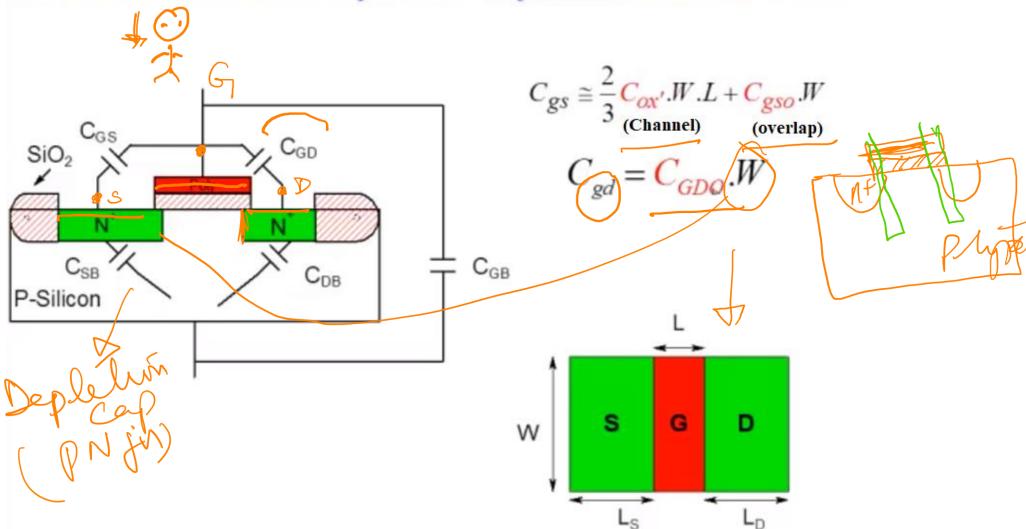
$$g_m = \frac{2I_{SDQ}}{V_{SGQ} + V_{THP}} \qquad r_o = \frac{1}{\lambda_p I_{SDQ}}$$

$$r_o = \frac{1}{\lambda_p I_{SDQ}}$$

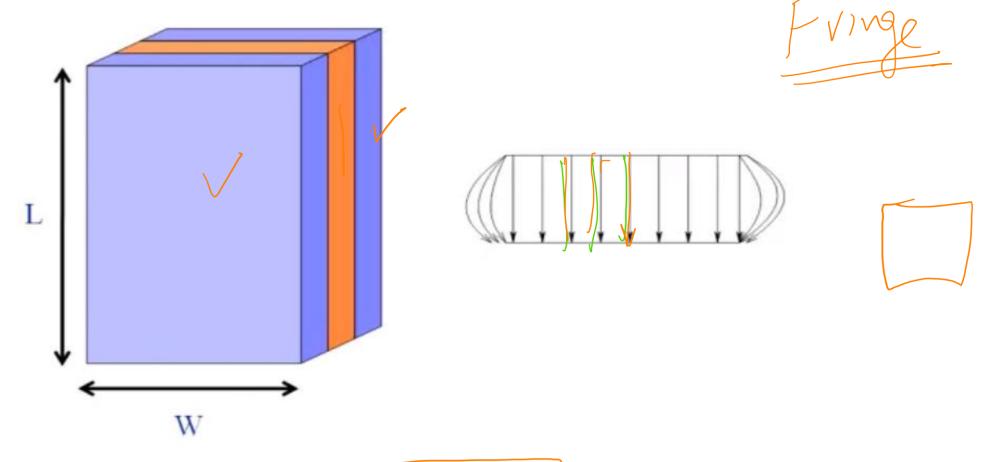
Capacitance Model



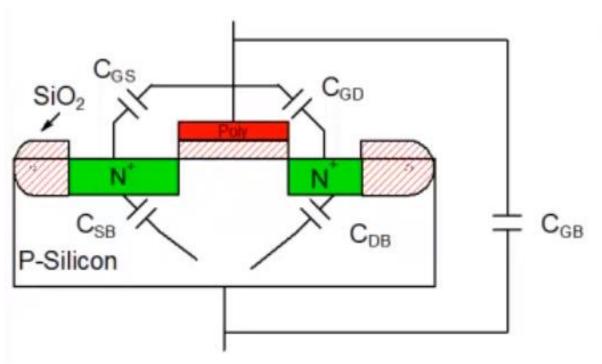
•. There are five distinct components of capacitance as illustrated below

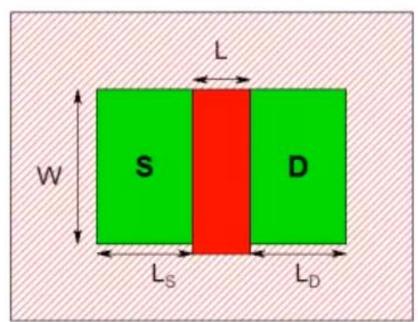


Capacitances: Area and Perimeter Components



$$C = \frac{\varepsilon}{d} \times W \times L + C_p \times (2L + 2W)$$

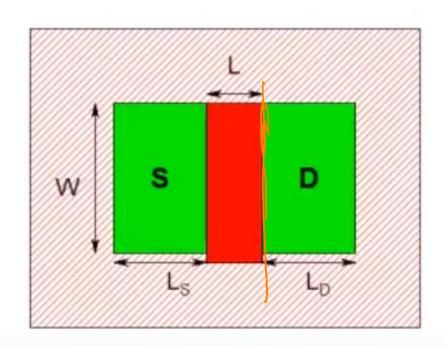




$$C_{sb} = \frac{C_{j}.A_{s}}{\left(1 + \frac{V_{SB}}{P_{B}}\right)^{M_{j}}} + \frac{C_{jsw}.P_{S}}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_{S} = 2L_{S} + W, \quad A_{s} = W.L_{S}$$

$$\frac{C_{db}}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_{j}.A_{D}}{\left(1 + \frac{V_{DB}}{P_{B}}\right)^{M_{j}}} \quad P_{D} = 2L_{D} + W$$

$$C_{gb} = C_{GBO}.L \sim \text{often negligible}$$



Triode/Linear Region



$$C_{gs} = \frac{1}{2} \frac{C_{ox}}{W}.W.L + \frac{C_{GSO}}{W}.W$$

$$C_{gd} = \frac{1}{2} \frac{C_{ox'}.W.L + C_{GDO}.W}$$

$$C_{sb} = same \, as \, before$$

$$C_{db} = same \, as \, before$$

$$C_{gb} = same as before$$

Assuming V_{DS} ~0

Cutoff Region

$$C_{gs} = C_{GSO}.W$$

$$C_{gd} = C_{GDO}.W$$

$$C_{sb} = same as before$$

$$C_{db} = same as before$$

$$C_{gb} = C_{GBO}.L + C_{ox'}.W.L$$

Assuming Tr. is in accumulation

Summary

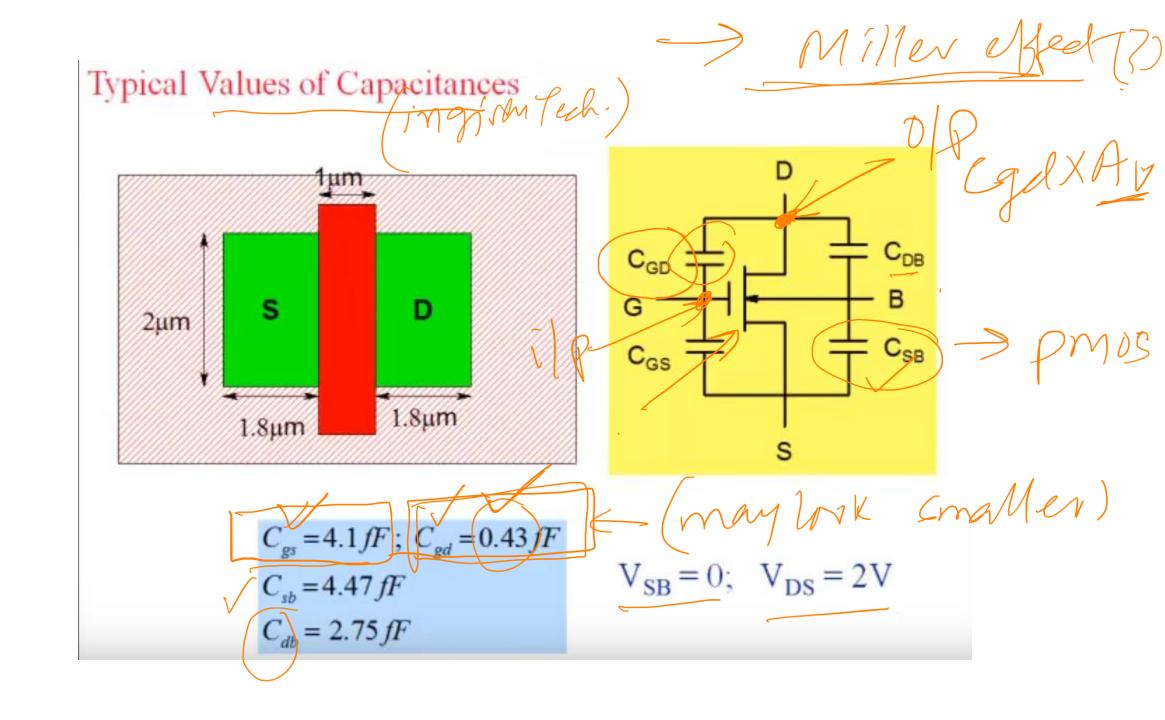
ummary
$$C_{gs} \cong \frac{2}{3}C_{ox'}W.L + C_{gso}W \qquad C_{gd} = C_{GDO}W$$

$$C_{sb} = \frac{C_{j}.A_{s}}{\left(1 + \frac{V_{SB}}{P_{B}}\right)^{M_{j}}} + \frac{C_{jsw}.P_{S}}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_{S} = 2L_{S} + W \quad , \quad A_{s} = W.L_{S}$$

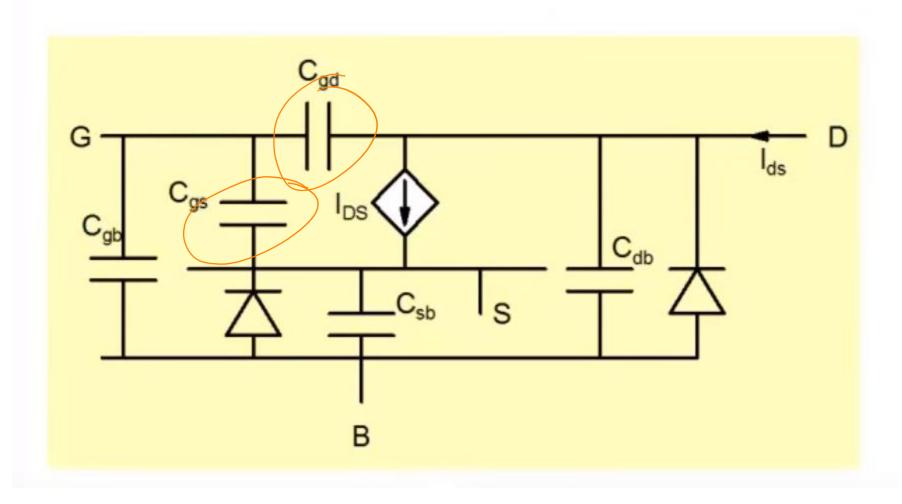
$$C_{db} = \frac{C_{jsw}.P_{D}}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_{j}.A_{D}}{\left(1 + \frac{V_{DB}}{P_{B}}\right)^{M_{j}}} \quad P_{D} = 2L_{D} + W$$

The capacitance model presented herein requires 10 parameters:

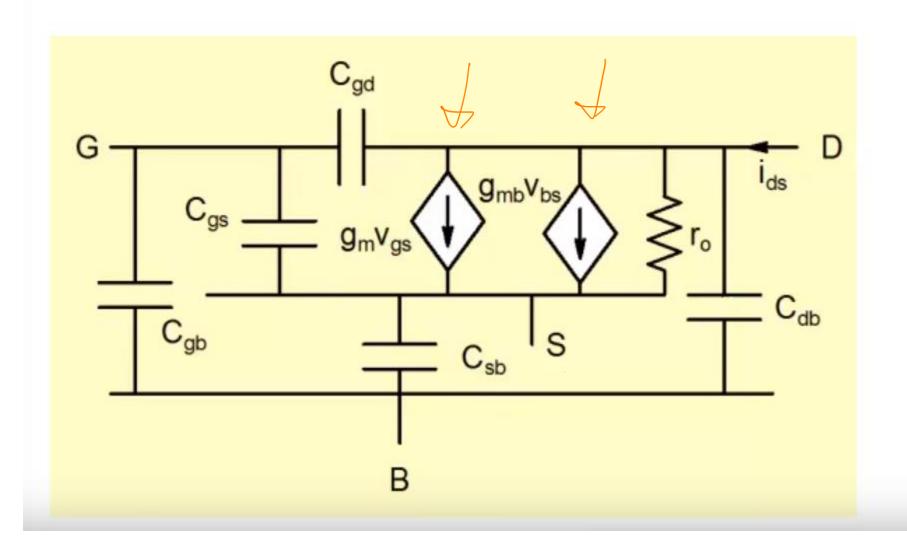
 C_{GSO} , C_{GDO} , C_{GBO} , C'_{OX} , C_{J} , PB, M_{J} , C_{JSW} , P_{BSW} , M_{JSW}



Complete Large Signal Model



High Frequency Small Signal Model



- We have so far discussed simple MOS models which are suitable for 'hand-analysis' of circuits. For more accurate prediction of circuit characteristics using circuit simulation more accurate MOS models are required.
- •SPICE and its various variants are the most popular circuit simulation tool. In SPICE, there are a number of MOS models that are available including Level-1, level-2, Level-3 BSIM1, BSIM2, BSIM3, BSIM4 etc.
- Level-1 model is the simplest and is basically similar to the large signal model that we have described earlier. A popular model for submicron devices is BSIM3 model.

^{*} SPICE- Simulation Program with Integrated Circuit Emphasis

^{*} BSIM- Berkeley Short-channel IGFET Model

BSIM3 : Berkeley Short Channel IGFET (Insulated gate Field Effect) Model

$$I_{ds} = \frac{I_{dso}(V_{dseff})}{1 + \frac{R_{ds}I_{dso}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_{A}}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}\left(1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2v_{t})}\right)V_{dseff}}{L_{eff}\left[1 + V_{dseff} / (E_{sat}L_{eff})\right]}$$

$$V_{A} = V_{Asat} + \left(1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}}\right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat} litl} (V_{ds} - V_{dseff})$$

Predictive Technology Model

Introduction

Latest Models

Nano-CMOS

Post-Silicon

Interconnect

Reliability

Contact



LATEST MODELS



ypical SPICE model files for each future generation are available here.

Attention: By using a PTM file, you agree to acknowledge both the URL of PTM: http://ptm.asu.edu/ and the related publications in all documents and publications involving its usage.

New!

June 01, 2012:

PTM releases a new set of models for multi-gate transistors (PTM-MG), for both HP and LSTP applications. It is based on <u>BSIM-CMG</u>, a dedicated model for multi-gate devices. **Acknowledgement:** PTM-MG is developed in collaboration with ARM.

Please start from models and param.inc.

- 7nm PTM-MG<u>HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS</u>
 - 10nm PTM-MG <u>HP NMOS</u>, <u>HP PMOS</u>, <u>LSTP NMOS</u>, <u>LSTP PMOS</u>
- 14nm PTM-MG <u>HP NMOS</u>, <u>HP PMOS</u>, <u>LSTP NMOS</u>, <u>LSTP PMOS</u>
- 16nm PTM-MG <u>HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS</u>
- 20nm PTM-MG <u>HP NMOS</u>, <u>HP PMOS</u>, <u>LSTP NMOS</u>, <u>LSTP PMOS</u>

The entire package is also available here: PTM-MG

November 15, 2008:

PTM releases a new set of models for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect.

- 16nm PTM LP model: V2.1
- 22nm PTM LP model: V2.1
- 32nm PTM LP model: V2.1
- 45nm PTM LP model: V2.1

September 30, 2008:

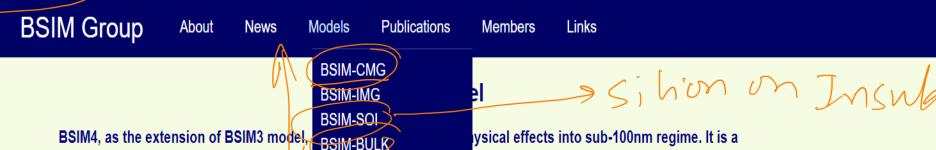
PTM releases a new set of models for high-performance applications (PTM HP), incorporating high-k/metal gate and stress effect.

- 16nm PTM HP model: <u>V2.1</u>
- 22nm PTM HP model: V2.1









physics-based, accurate, scalable, robust BSIM4 SPICE model for circuit simulation and CMOS technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. All suggestions for model improvements are charted by the Compact Model Coalition (CMC).

BSIM4 has been used for the 0.13 um, 90 nm, 65 nm, 45/40 nm, 23/28 nm, and 22/20nm technology nodes.

See BSIM3, a predecessor of BSIM4, here.

Latest Release

BSIM4 4.8.1 was released on Feb. 15, 2017.

We would like to thank CMC members for testing beta models and providing valuable feedbacks during model development.

Download BSIM4 4.8.1 model package, including

Model code in C

```
* PTM Low Power 16nm Metal Gate / High-K / Strained-Si
```

* nominal Vdd = 0.9V

.model nmos nmos level = 54

binunit = 1 +version = 4.0paramchk= 1 mobmod = 0igcmod = 1+capmod = 2igbmod = 1geomod = 1 +diomod = 1rdsmod = 0rbodymod= 1 rgatemod= 1 +permod = 1acngsmod= 0 trngsmod= 0 = 1.2e-009= 27 = 1.2e-009= 9e-010toxp +tnom toxe toxm = 0 +dtox = 3e-010epsrox = 3.9wint = 5e-009lint +11 = 0 wl = 0 11n = 1 wln = 1 +lw = 0 = 0 = 1 = 1 lwn WW wwn +lwl = 0 wwl = 0 = 0 toxref = 1.2e-009xpart +vth0 = 0.68191 k1 = 0.4k2 = 0 k3 = 0 = 0 +k3b w0 = 2.5e - 006dvt0 = 1 dvt1 = 2 +dvt2 = 0 dvt0w = 0 dvt1w = 0 dvt2w = 0 voffl +dsub = 0.1 minv = 0.05= 0 dvtp0 = 1e-011+dvtp1 = 0.1 lpe0 = 0 lpeb = 0 хj = 5e-009+ngate = 1e+023ndep = 7e + 018nsd = 2e + 020phin = 0 +cdsc = 0 cdscb = 0 cdscd = 0 cit = 0 +voff = -0.1014nfactor = 1.6eta0 = 0.0095 etab = 0 +vfb = -0.55= 0.028= 6e-010= 1.2e-018u0 ua ub = 0 vsat = 200000 = 1 = 0 +uc a0 ags +a1 = 0 a2 = 1 b0 = 0 b1 = 0 dwb +keta = 0.04 dwg = 0 = 0 pclm = 0.02 +pdiblc1 = 0.001pdiblc2 = 0.001pdiblcb = -0.005drout = 0.5 pscbe2 = 1e-007+pvag = 1e-020delta = 0.01 pscbe1 = 8.14e+008+fprout = 0.2pdits = 0.01pditsd = 0.23pditsl = 2300000 +rsh = 5 rdsw = 170 = 75 rdw = 75 rsw +rdswmin = 0rdwmin = 0rswmin = 0= 0 prwg +prwb = 0 alpha0 = 0.074alpha1 = 0.005wr = 1 +beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009cgidl = 0.0002 +egidl = 0.8 aigbacc = 0.012bigbacc = 0.0028cigbacc = 0.002