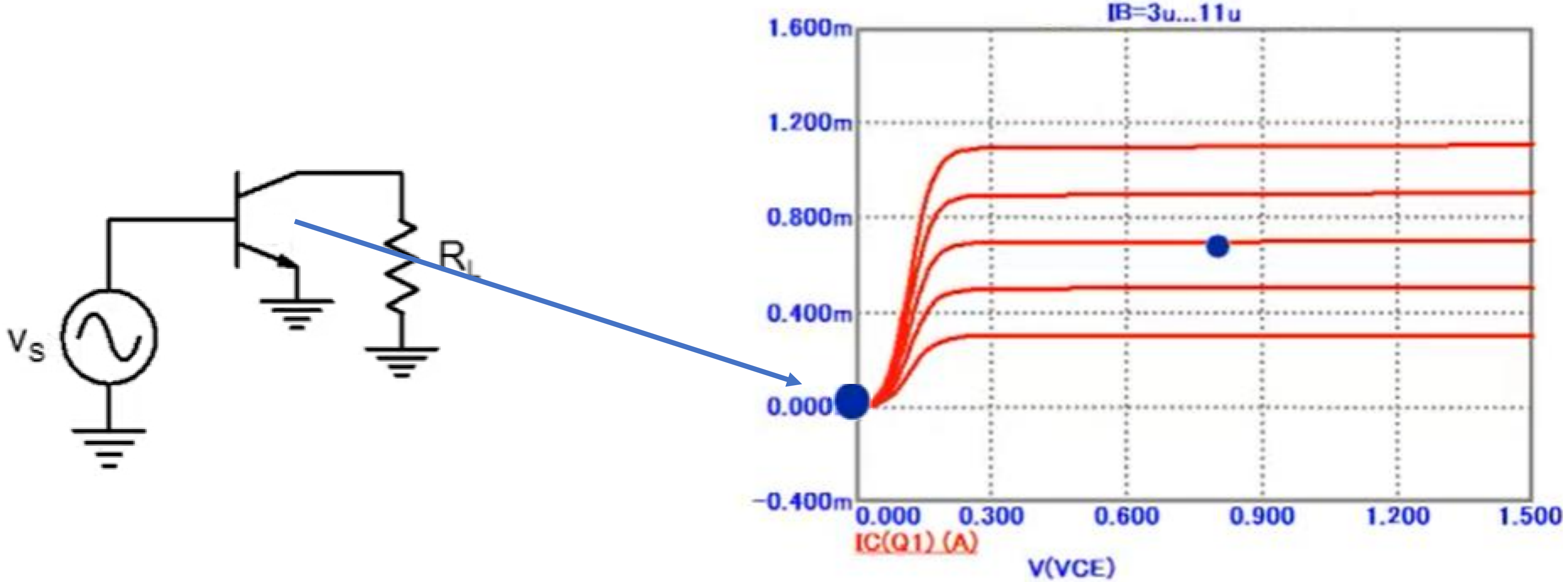
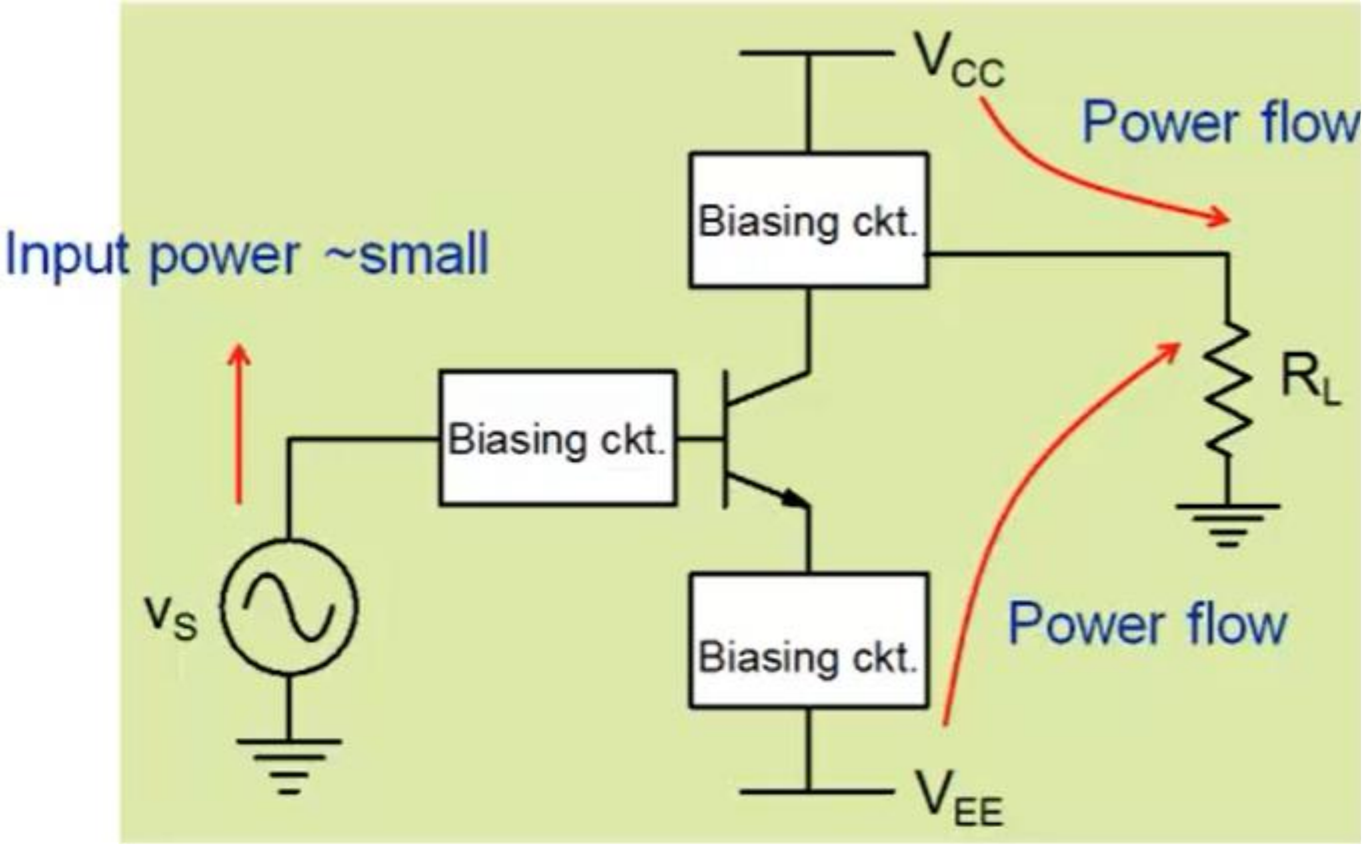
BJT Amplifier Biasing

Biasing

v_S
R_L

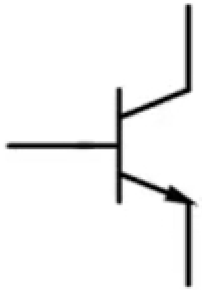


v_S
R_L
IB=3u...11u
1.600m
1.200m
0.800m
0.400m
0.000
−0.400m
0.000
0.300
0.600
0.900
1.200
1.500
IC(Q1) (A)
V(VCE)



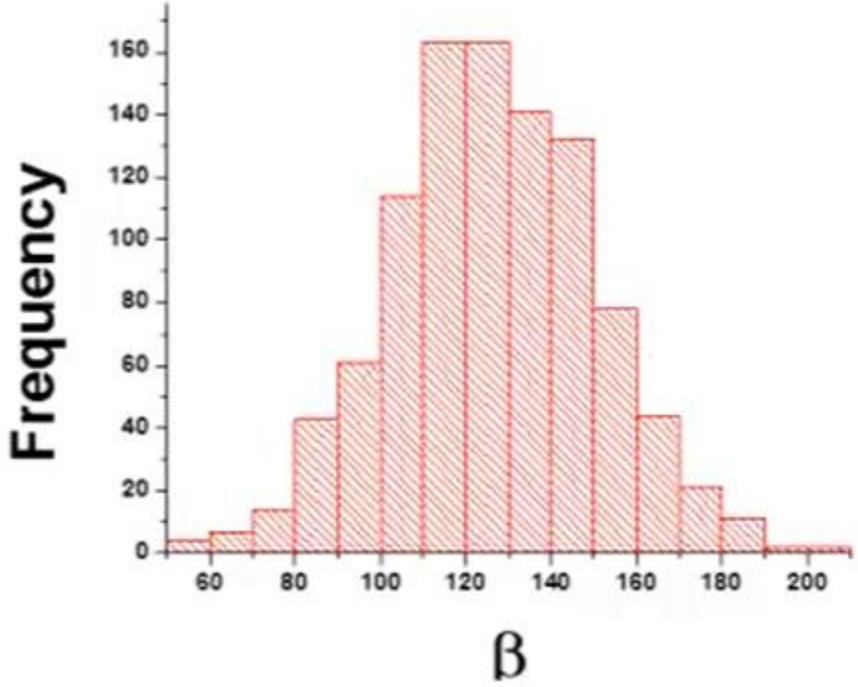
Good Biasing circuit: Bias point is stable against variations in temperature, current gain β, supply voltage etc, power efficient, low cost ....

Variations to watch out for

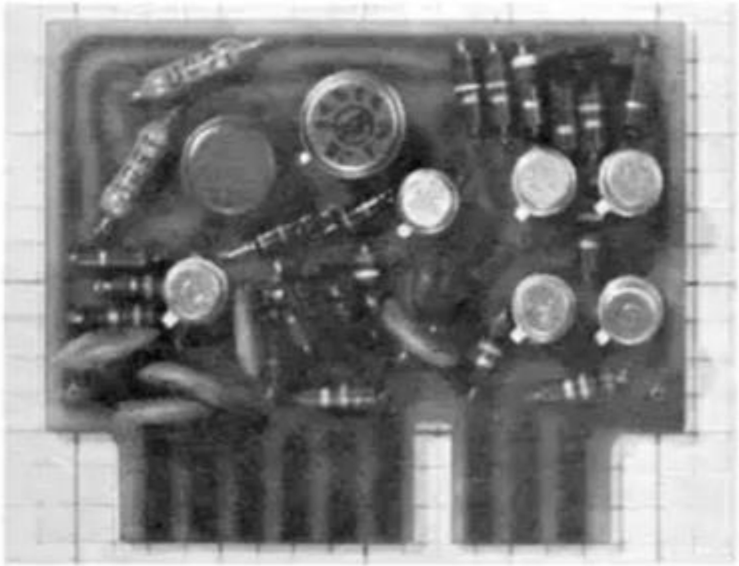


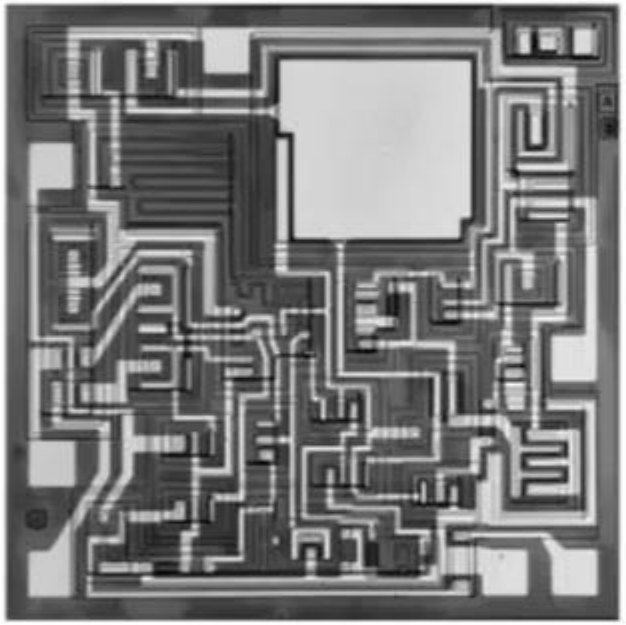
(1) $$\frac{dV_{BE}}{dT} \cong -2mV\ /^{o}\ C$$

(2)



Different biasing circuit for discrete and monolithic (IC) circuit implementation



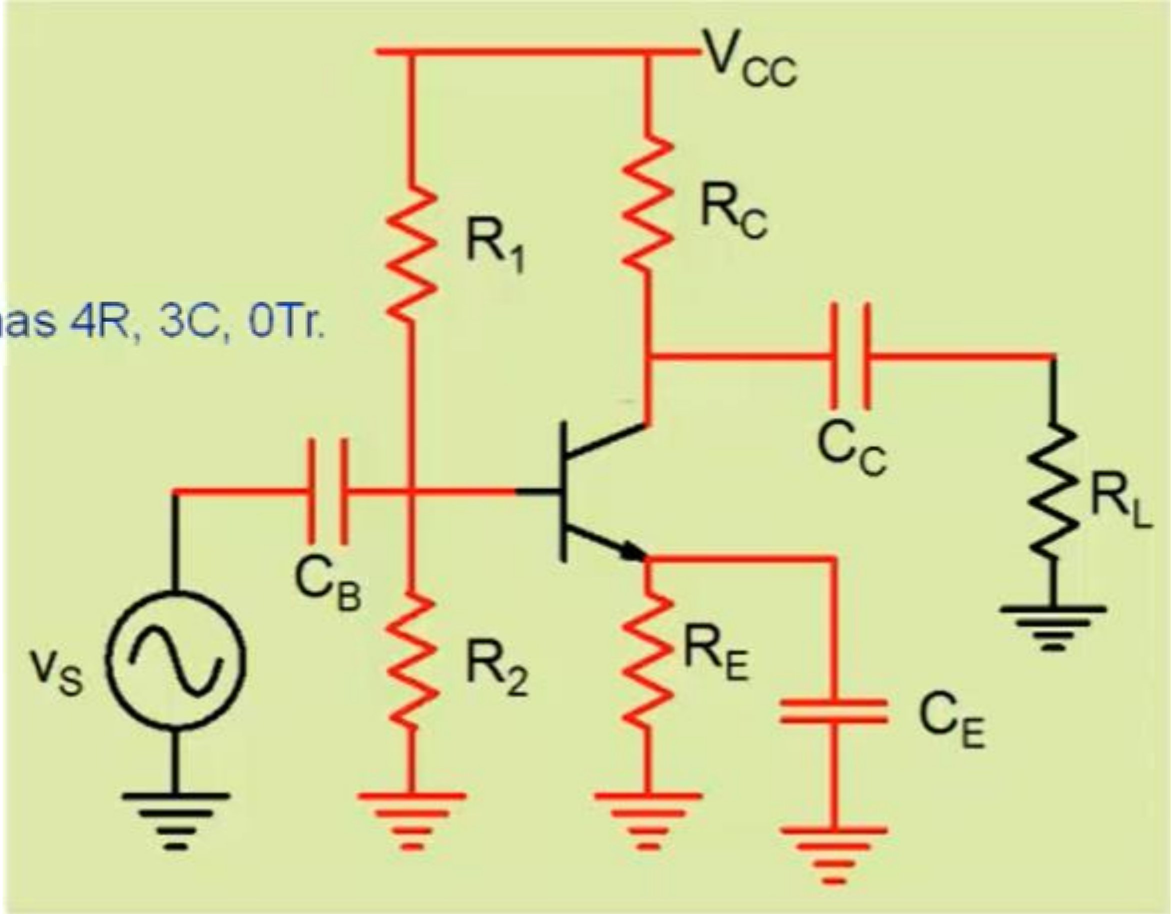


Resistors and capacitors are 'cheap' and transistors are relatively more expensive.

Higher value resistors (MΩ) are expensive and capacitors in pF range only are possible. Passive components are expensive, while transistors are cheap !

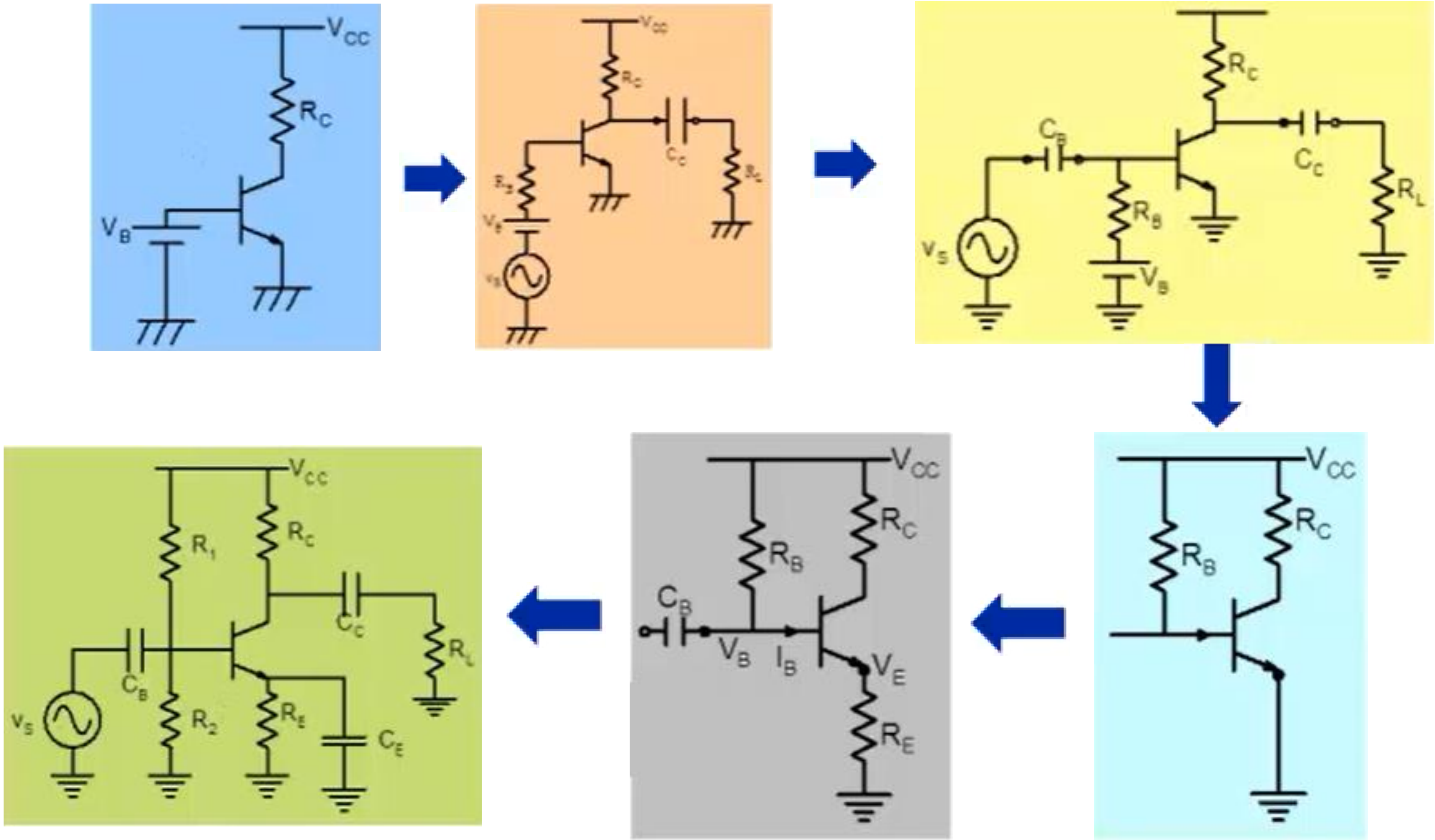
A good biasing circuit for discrete implementation

Bias circuit has 4R, 3C, 0Tr.

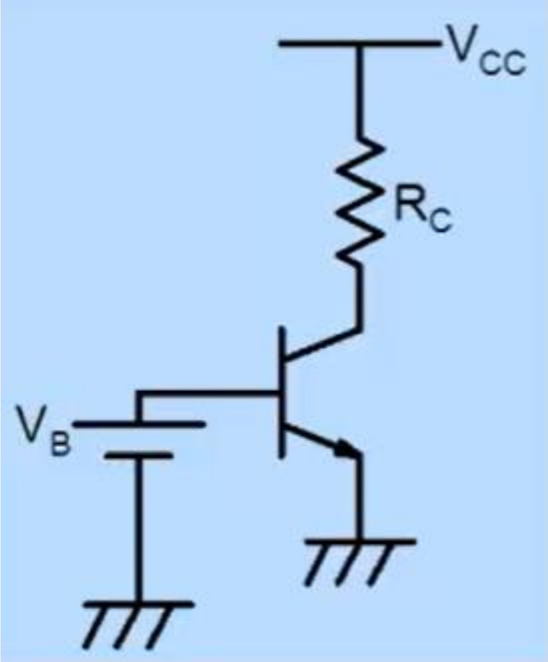


Every Circuit is a solution to one or more set of problems !

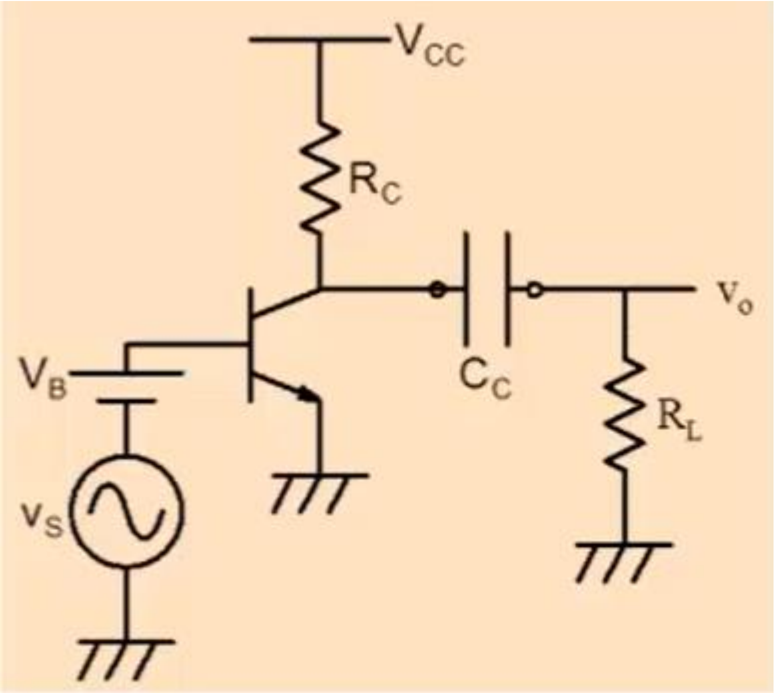
Evolution of circuit from simple to complex



BJT amp-1



Bias the Transistor in Forward Active Mode

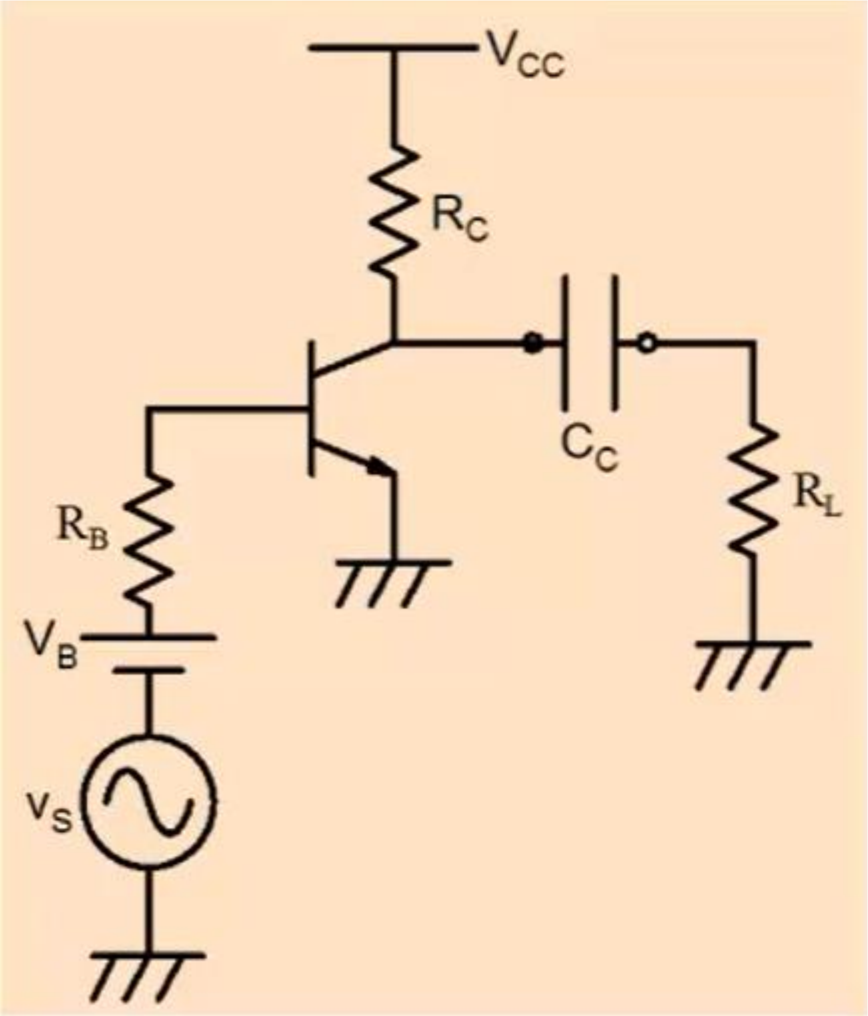


Apply the signal at the base and Connect the load

$$I_C \cong I_S \times \exp\left(\frac{V_{BE}}{V_T}\right) \qquad \Delta I_C \cong I_S \times \exp\left(\frac{V_{BE}}{V_T}\right) \times \frac{\Delta V_{BE}}{V_T} \qquad \left(\frac{\Delta I_C}{I_C}\right) = \left(\frac{\Delta V_B}{V_B}\right) \times \left(\frac{V_{BE}}{V_T}\right)$$

Biasing is very sensitive to the biasing voltage and temperature

BJT amp-2



$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$I_C = \beta \times I_B$$

$$\frac{\Delta I_C}{I_C} = \frac{-\Delta V_{BE} + \Delta V_B}{V_B - V_{BE}}$$

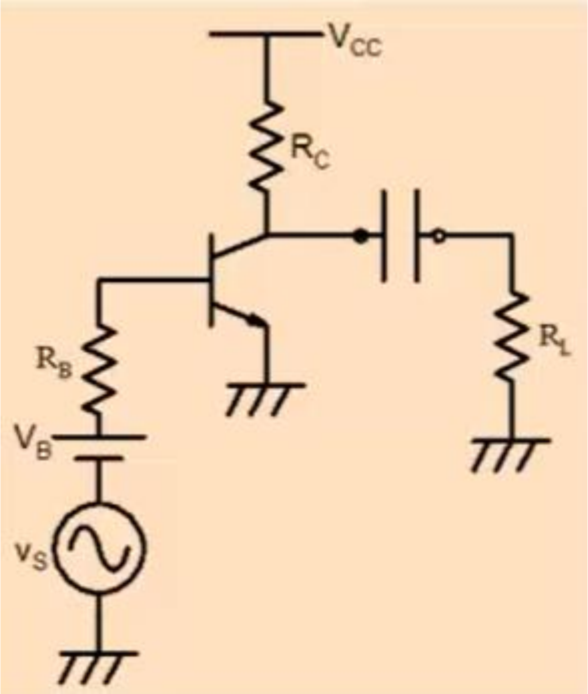
$$\frac{dV_{BE}}{dT} = -2mV/°C$$

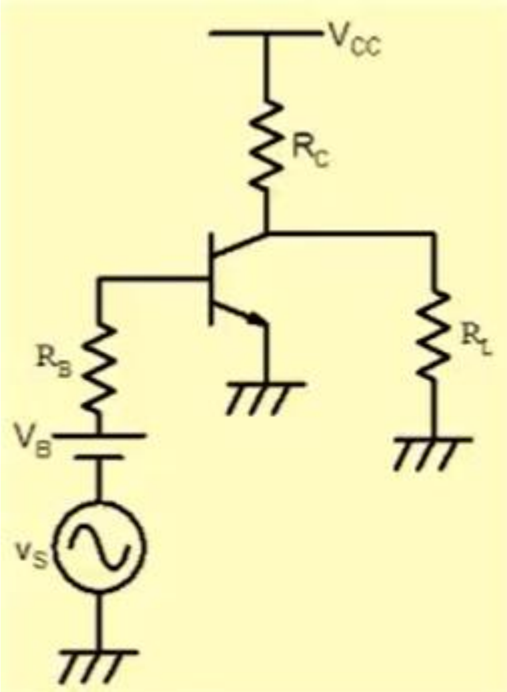
$\Delta V_{BE} = 100$ mV

$V_B - V_{BE} >> 100$ mV

$V_B - V_{BE} = I_B R_B \geq 1$ Volt

Why use a capacitor at the output?



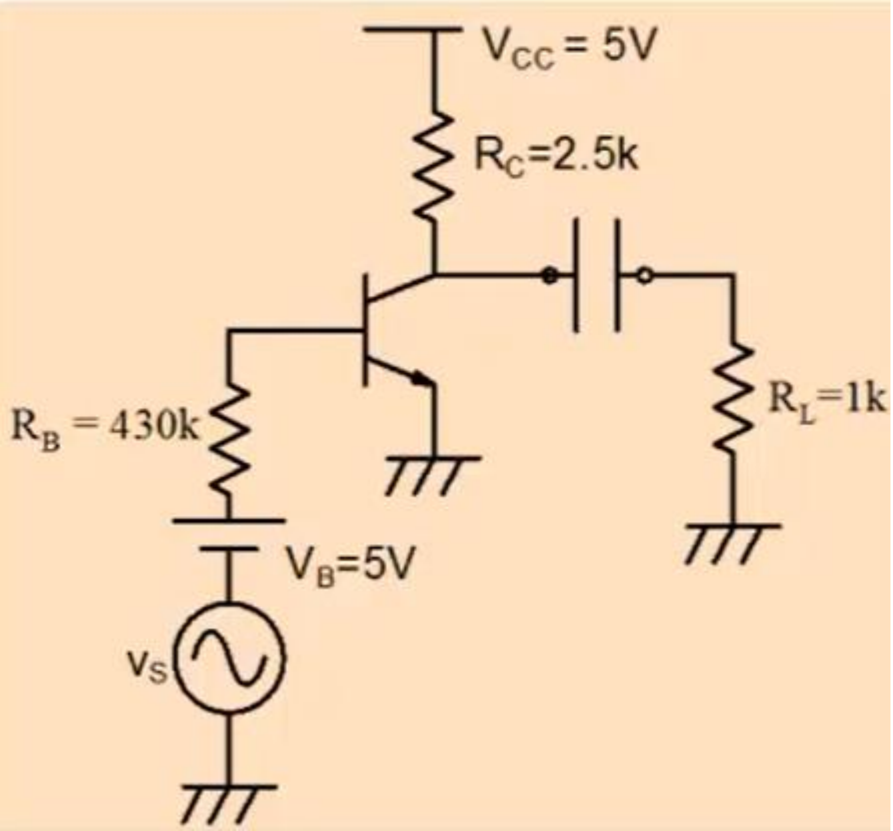


$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = \frac{V_{CC} - I_C R_C}{1 + R_C / R_L}$$

It may become difficult to obtain the desired value of V_{CE} and bias point becomes load dependent.

Example-1



Bias or quiescent (Q) Point :

$$I_{CQ} = 1mA; \quad V_{CEQ} = 2.5V$$

Design:

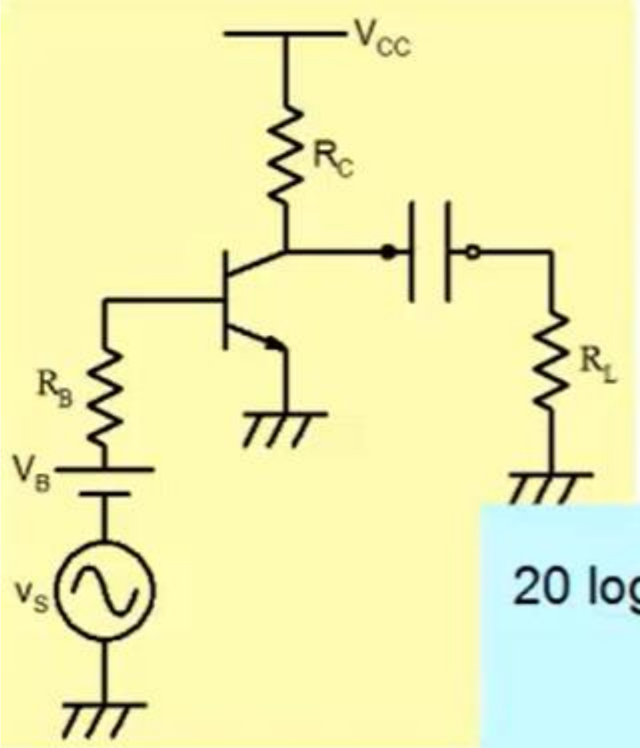
$$I_B = \frac{V_B - V_{BE}}{R_B}; I_C = \beta \times I_B$$

$$V_{CE} = V_{CC} - I_C \times R_C$$

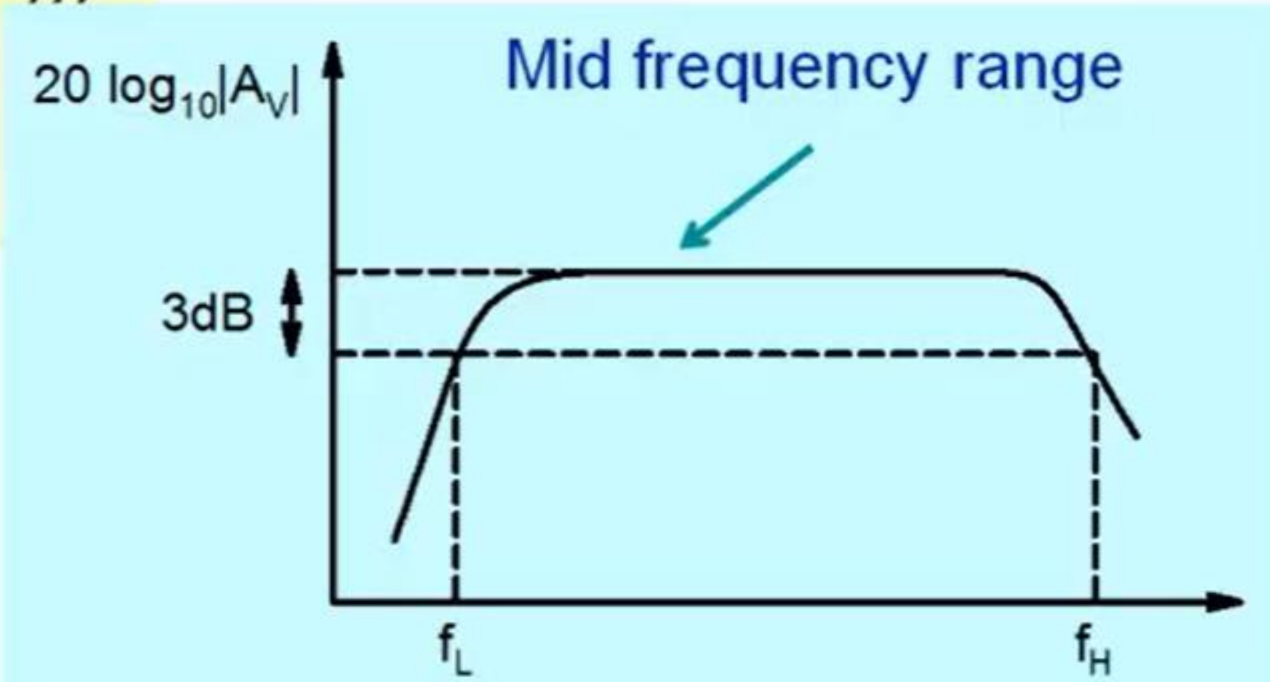
$$I_B R_B > 1V$$

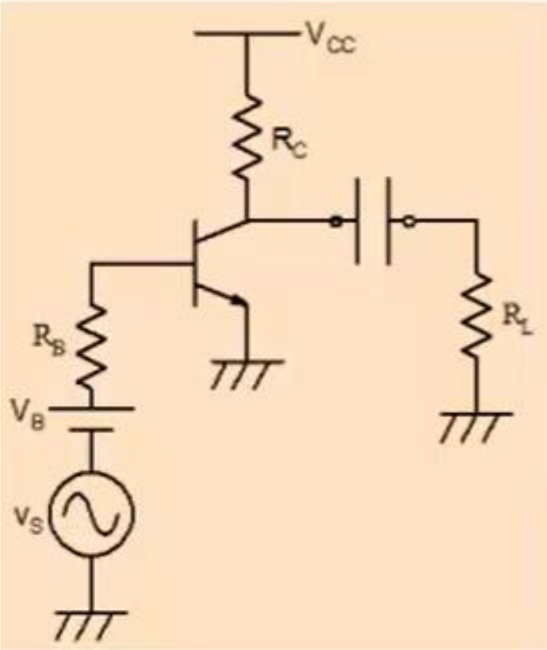
$$R_B = 430k\Omega \; ; \; R_C = 2.5k\Omega$$

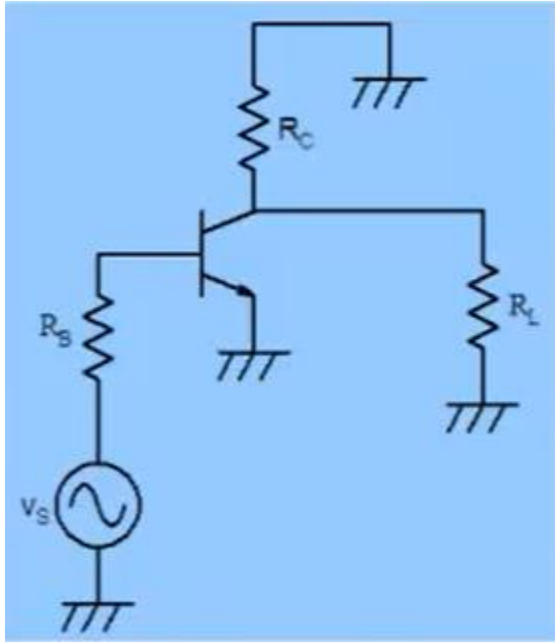
Small Signal Analysis (Mid Frequency Range)

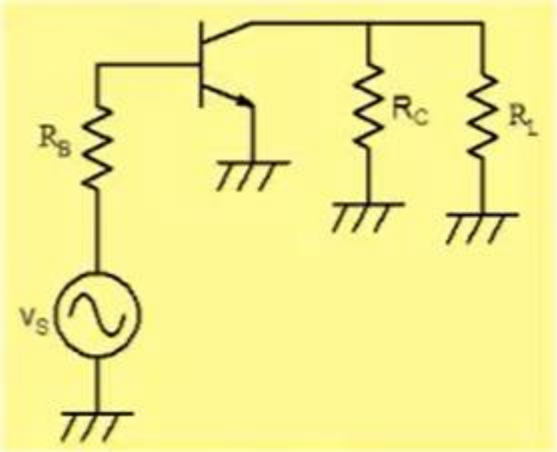


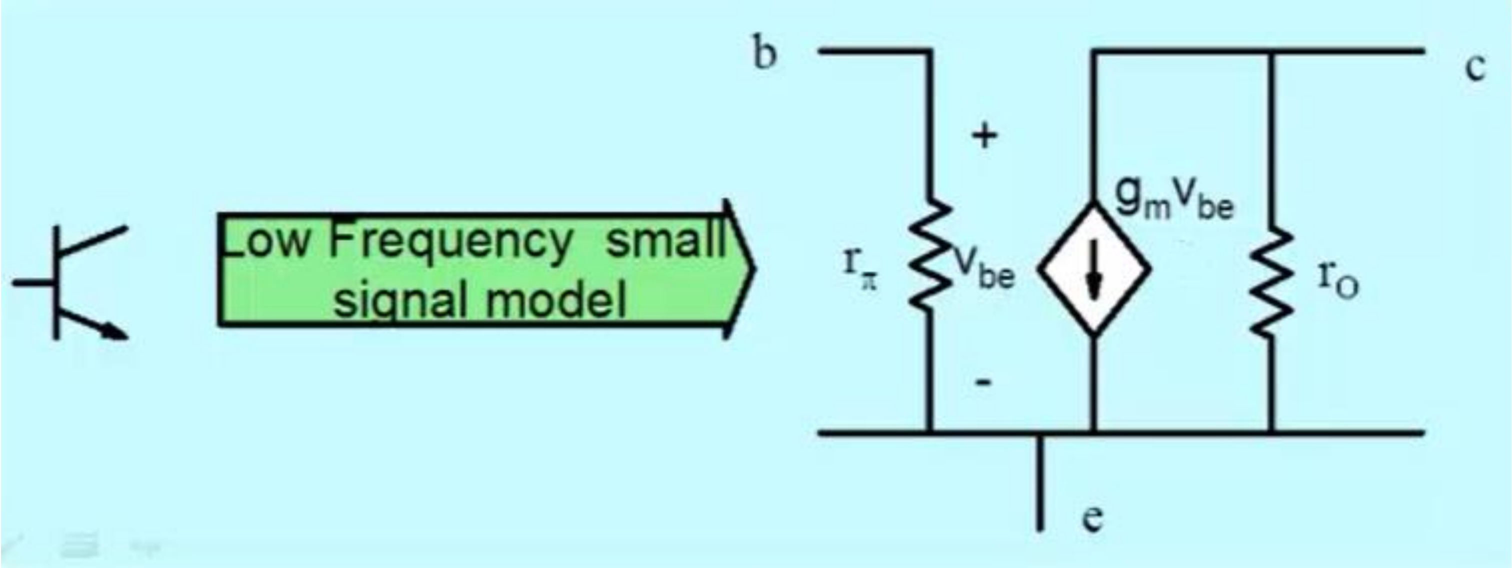
Frequency is high enough for all coupling capacitors to be assumed as short but low enough for all internal transistor capacitances to be considered as open.



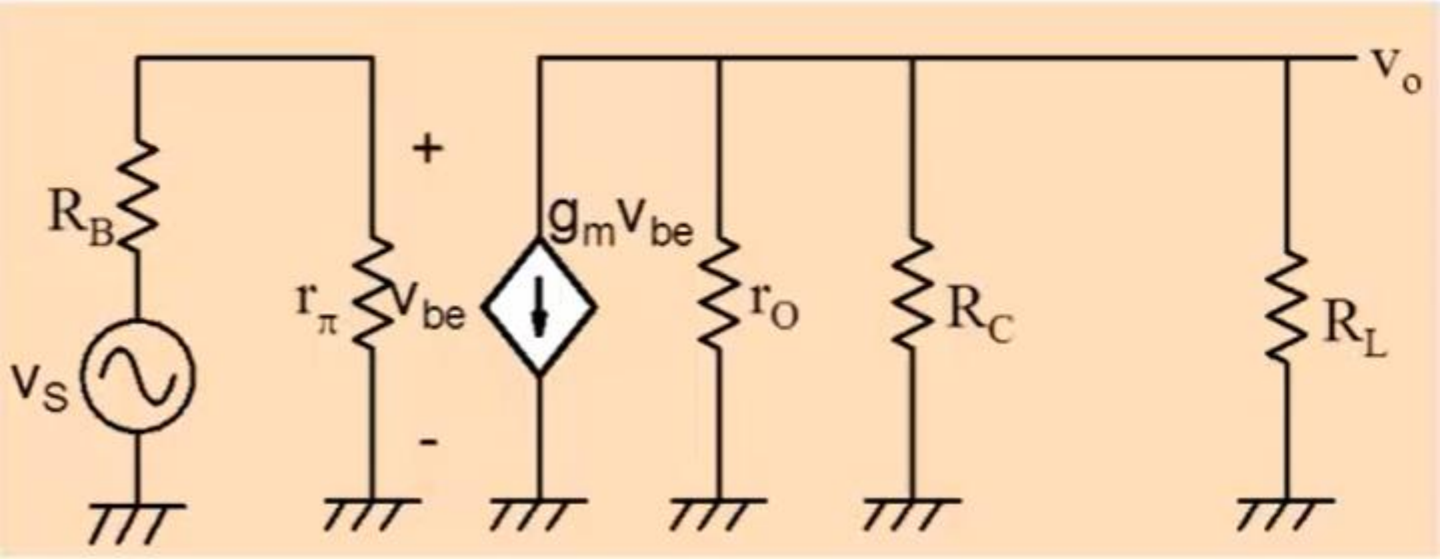

Vcc
RC
RB
VB
vS
RL


RC
RS
vS
RL


RB
RC
RL
vS


Low Frequency small signal model
b
c
e
+
-
rπ
Vbe
gmVbe
rO

Small Signal Analysis

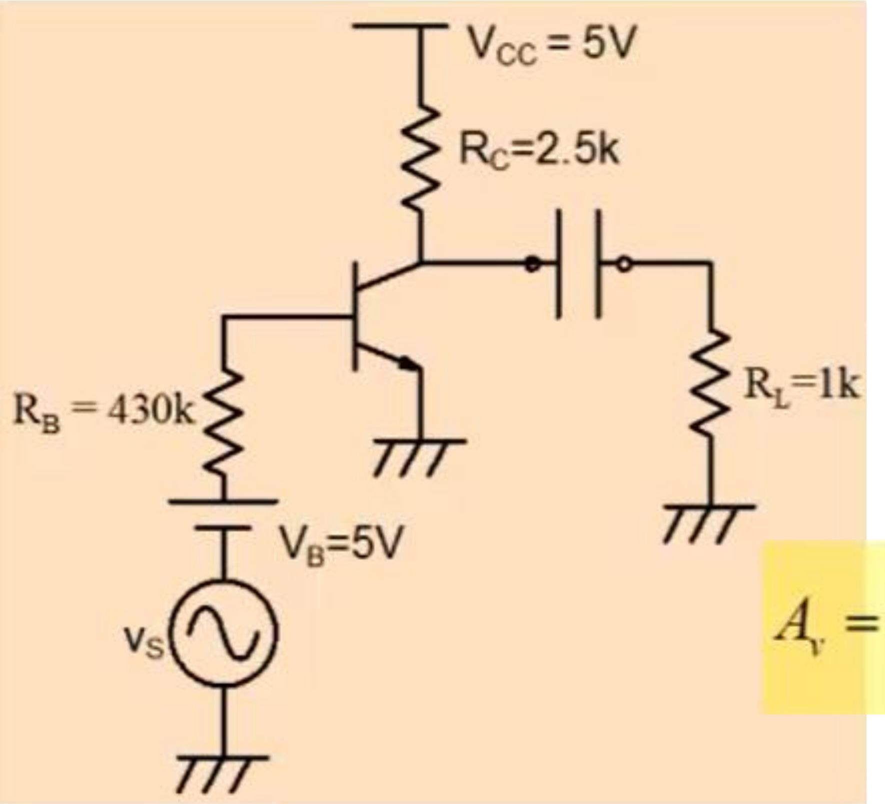


$$v_{be} = \frac{r_\pi}{r_\pi + R_B} v_S$$

$$v_o = - \quad g_m \, v_{be} \times (r_o \parallel R_C \parallel R_L)$$

$$A_v = - \left(\frac{r_\pi}{r_\pi + R_B} \right) \quad g_m \times (r_o \parallel R_C \parallel R_L)$$

Example-1



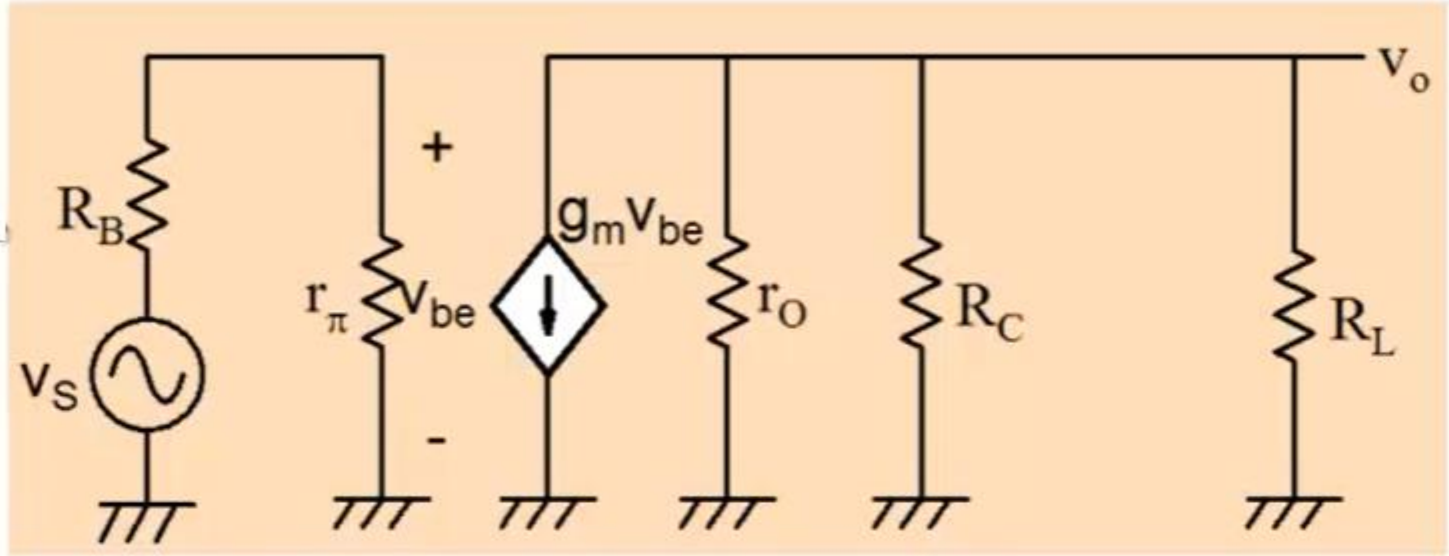
$$I_{CQ} = 1mA; \quad V_{CEQ} = 2.5V$$

$$g_m = 38m\mho; \; r_\pi = 2.6k\Omega; \; r_o = 100k\Omega$$

$$A_v = -\left(\frac{r_\pi}{r_\pi + R_B}\right)\{g_m \times (r_o \parallel R_C \parallel R_L)\}$$

$$A_v = (6\times 10^{-3})\times 27.2 = 0.164$$

Problem

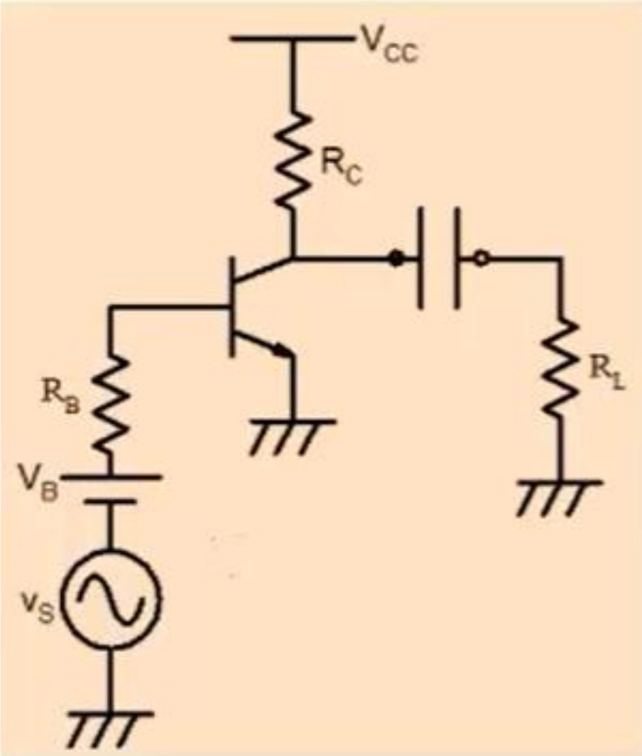


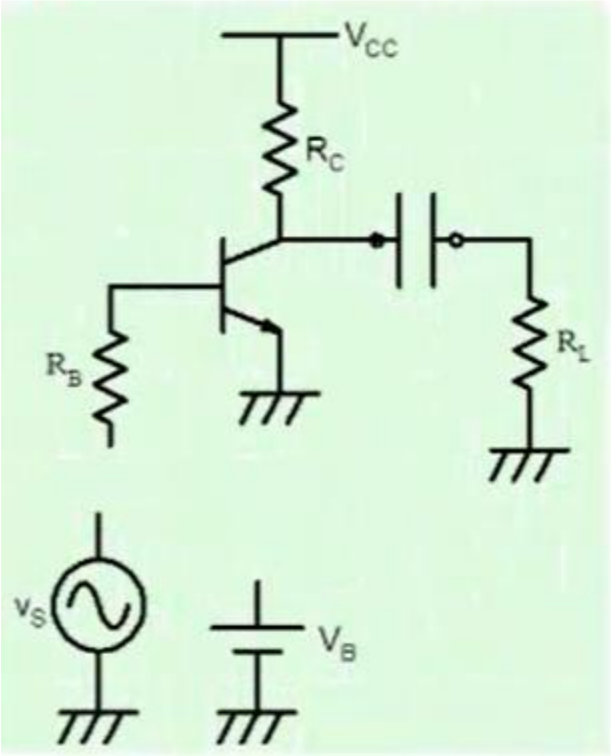
$$A_V \cong \left(\frac{r_\pi}{r_\pi + R_B}\right) g_m R_L$$

$$\left(\frac{r_\pi}{r_\pi + R_B}\right) = \frac{V_T/I_B}{(V_T/I_B) + R_B} = \frac{V_T}{V_T + I_B R_B}$$

A large fraction of input gets dropped across R_B

Another Problem

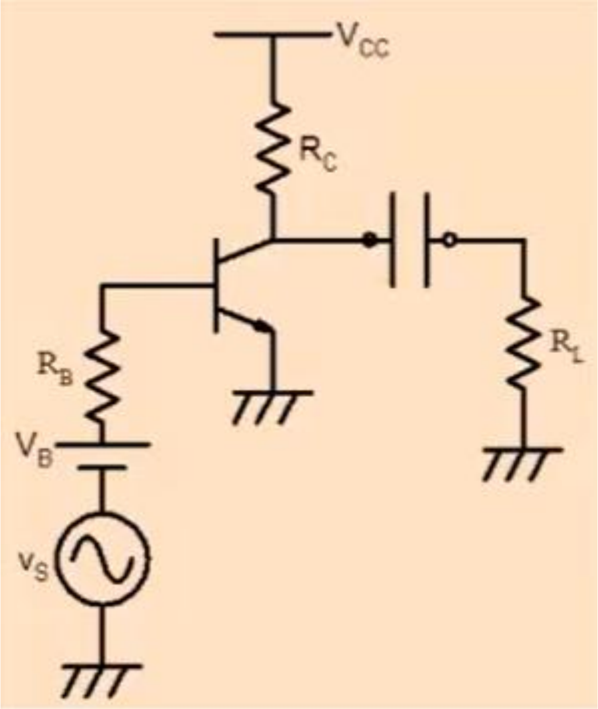


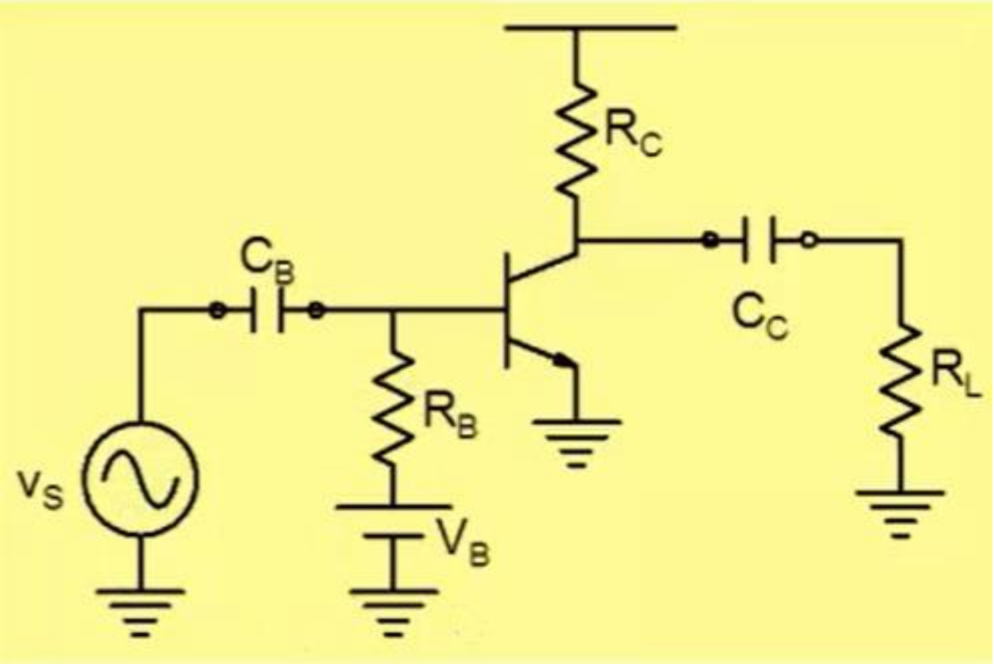


How do we connect vs and V_B in series when one terminal of both is ground?

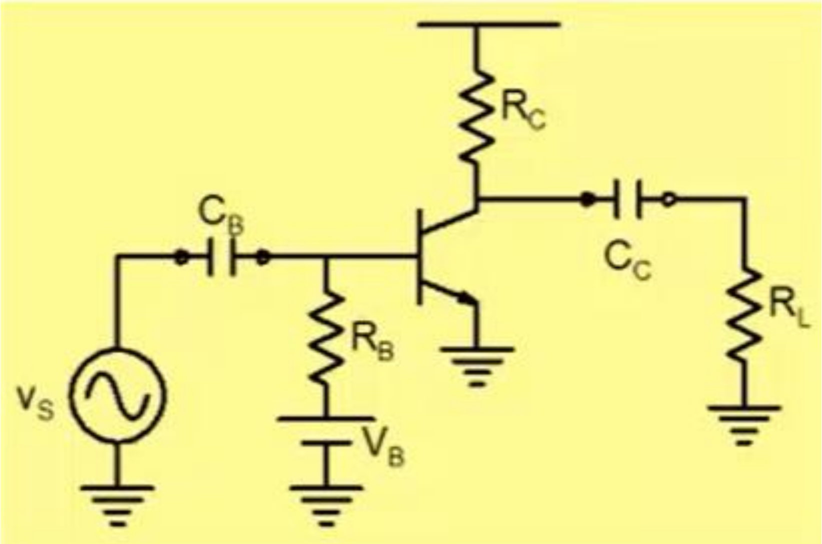
Solution

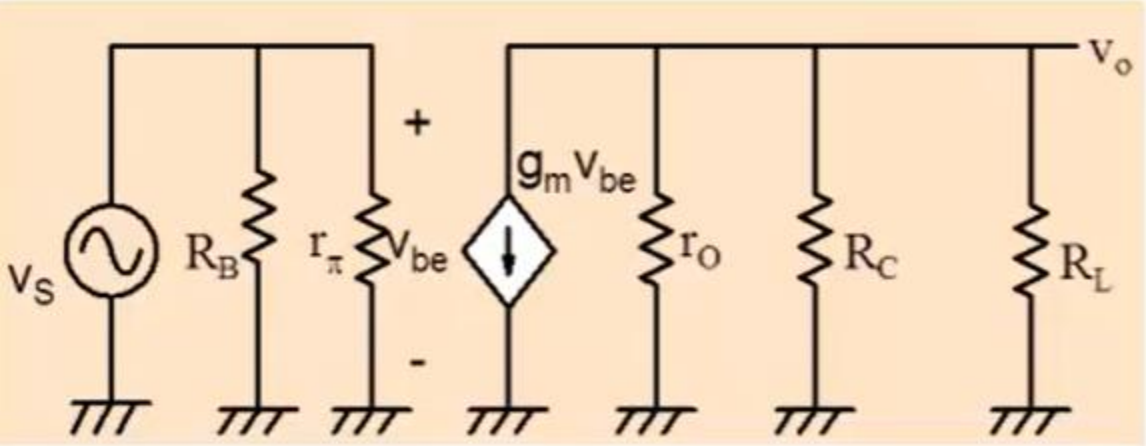
Bypass resistance R_B from the path of the input signal





Small Signal Model





$$A_v = -g_m \times r_0 \parallel R_C \parallel R_L$$

$$\cong -g_m \times R_C \parallel R_L$$

$$g_m \times R_C = \frac{I_C \times R_C}{V_T}$$