VLSI Design - Assignment 1

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2

The cross sectional diagram of a MOSFET is given below.

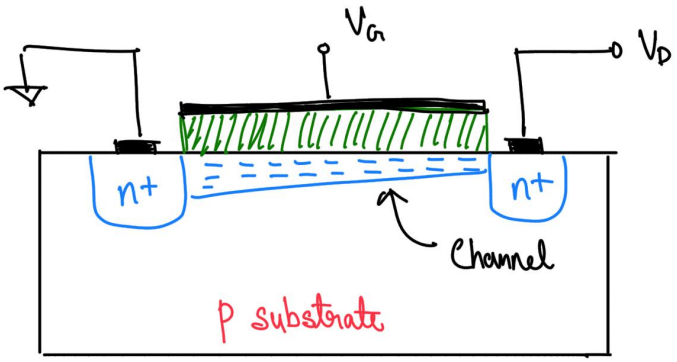

Figure 2.1: Cross Section of MOSFET

Clearly, if the gate voltage is negative, the free electron concentration in the channel region is almost zero, due to the accumulation of holes. Therefore, $I_D = 0$.
At $0 < V_{GS} < V_{TH}$, the subthreshold current is given by,

$$I_D = I_{D0} e^{\frac{V_{GS} - V_{TH}}{\eta V_t}} (1 - e^{\frac{-V_{DS}}{V_t}}) \tag{2.1}$$

Where V_t is the thermal voltage, Let the voltage due to the drain voltage V_{DS} at each point along the channel be $V(x)$, and the charge in a small region, of area Wdx along the channel be dQ. Since the gate terminal, along with the substrate behaves like a capacitor, the charge dQ will be,

$$\begin{aligned} dQ &= C \cdot V \\ \implies dQ &= C_{ox} W dx (V_{GS} - V_{TH} - V(x)) \text{ (C_{ox} - Capacitance per unit area)} \end{aligned}$$

Dividing both sides by dt,

$$\begin{aligned} \frac{dQ}{dt} &= C_{ox} W \frac{dx}{dt} (V_{GS} - V_{TH} - V(x)) \\ \implies I_D &= C_{ox} W v_d (V_{GS} - V_{TH} - V(x)) \text{ (v_d - Drift Velocity)} \end{aligned}$$

We know that $v_d = \mu_n E(x) = \mu_n \frac{dV}{dx}$

$$\begin{aligned}
\implies I_D &= C_{ox} W \mu_n \frac{dV}{dx}(V_{GS} - V_{TH} - V(x)) \\
\implies I_D\, dx &= \mu_n C_{ox} W (V_{GS} - V_{TH} - V(x))\, dV \\
\implies \int_0^L I_D\, dx &= \int_0^{V_{DS}} \mu_n C_{ox} W (V_{GS} - V_{TH} - V(x))\, dV \\
\implies I_D L &= \mu_n C_{ox} W ((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}) \\
\therefore I_D &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2) \qquad (2.2)
\end{aligned}$$

Equation 2.1 is valid for all $V_{DS} \leq V_{GS} - V_{TH}$, since the potential at each point in the channel is given by $(V_{GS} - V_{TH} - V(x)$, if at any point $V(x) \geq V_{GS} - V_{TH}$, the charge at that point will become zero (absence of any net potential), which means that the channel will cease to exist at that point. This phenomenon is termed as Channel Cut-off.

The flow of current beyond the cutoff point will be due to the injection of current carriers from the channel into the substrate, which are swept off due to the positive drain potential.

Because of the cutoff (let the point of cutoff be L'), the integration limits change to, 0 to L' for x and 0 to $V_{GS} - V_{TH}$ for V. Taking $L' \approx L$, we get,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \qquad (2.3)$$

However, the approximation of $L' \approx L$ is not perfectly valid, since L' decreases as V_{DS} increases (the cutoff point moves further away from the drain). Since I_D increases if L' decreases, we can approximate this behavior, called Channel Length Modulation, as a linear relation with V_{DS}, using the below equation.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \qquad (2.4)$$

Where, λ is the Channel Length Modulation parameter. It depends on the physical properties of the transistor.

3

MOS Capacitor ($V_{DS} = 0$)

Let C_{MOS} be the capacitance of the MOS Capacitor, between the gate and substrate. The operation of a MOS capacitor can be separated into 3 regions.

Accumulation: ($V_{GS} < 0$)

A negative gate voltage accumulates holes near the channel region. The total capacitance of the MOS is equal to the capacitance due to the gate oxide.

$$C_{MOS} = C_{OX} \qquad (3.1)$$

Where, C_{OX} is the gate oxide capacitance.

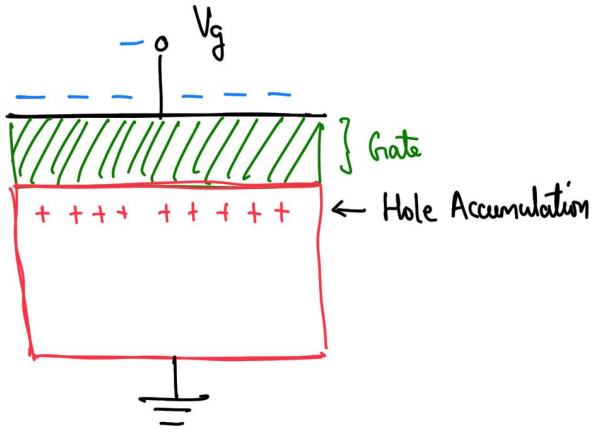

Figure 3.1: Charges during Accumulation

Depletion: $(0 < V_{GS} < V_{TH})$

The positive voltage repels holes from the channel region and creates a depletion region of negative ions. The depletion region adds some capacitance in series with the gate capacitance. Since the inversion layer isn't fully formed, the oxide capacitance and depletion capacitance are not electronically separated from each other, hence the series connection.

$$C_{MOS} = \frac{C_{OX}C_{dep}}{C_{OX} + C_{dep}} \tag{3.2}$$

Where, C_{dep} is the depletion region capacitance.

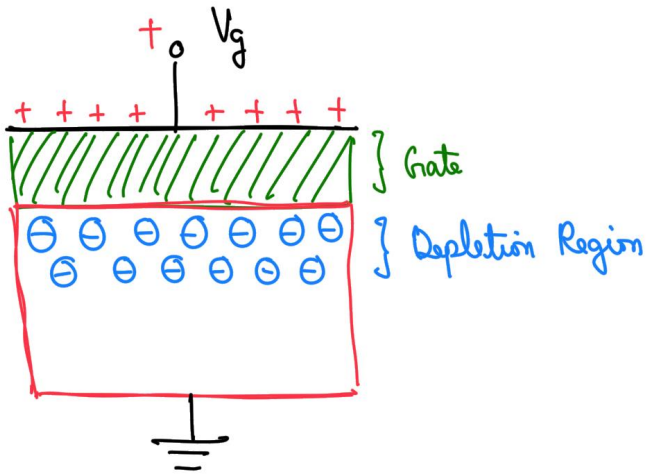

Figure 3.2: Charges during Depletion

Inversion: $(V_{GS} > V_{TH})$

Due to the inversion layer forming a conductive layer between the oxide and the depletion region, the oxide capacitance and the depletion region capacitance are electronically separated from each other in low frequencies, ie, in low frequencies the voltage signal only "sees" the oxide capacitance. Therefore,

$$C_{MOS} = \begin{cases} C_{OX} & \text{Low frequencies} \\ \frac{C_{OX}C_{dep}}{C_{OX}+C_{dep}} & \text{High frequencies} \end{cases} \tag{3.3}$$

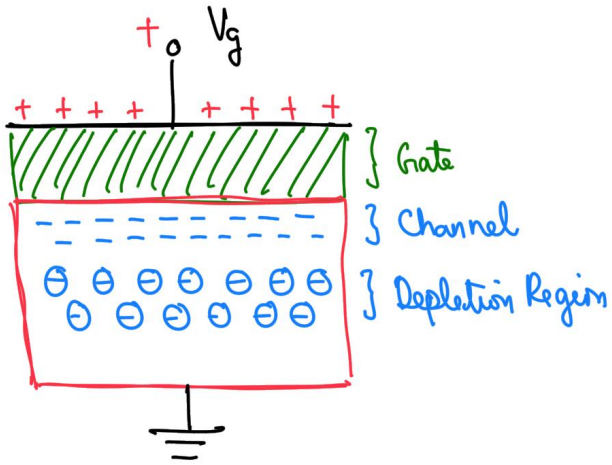

Figure 3.3: Charges during Inversion

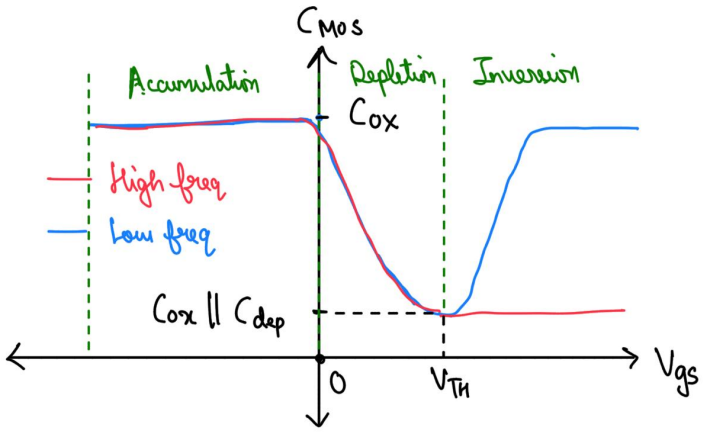

Figure 3.4: Overall C-V Characteristics of MOS Capacitor

MOS Capacitance during operation as Transistor ($V_{DS} \neq 0$)

Cutoff ($V_{GS} < V_{TH}$)

Since no current flows between drain and source, the gate capacitance follows the same behavior as the MOS Capacitance above (Accumulation behavior when $V_{GS} < 0$ and Depletion behavior when $0 < V_{GS} < V_{TH}$)

$$C_{gb} = \begin{cases} C_{OX} & V_{GS} < 0 \\ \frac{C_{OX}C_{dep}}{C_{OX}+C_{dep}} & 0 < V_{GS} < V_{TH} \end{cases} \tag{3.4}$$

Also C_{gs} and C_{gd} are due to overlap between the source/drain and the gate oxide.

$$C_{gs} \approx C_{gd} \approx C_{ov} \tag{3.5}$$

Where C_{ov} is the overall overlap capacitance ($C_{OX} = C_{ox}WL$).

Linear

Since the channel electronically separates the gate and body (since the oxide electric field ends at the channel due to its conductive nature), $C_{gb} = 0$. So only source and drain capacitances are active.

$$C_{gs} = C_{gd} = (C_{ox}WL + C_{ov})/2 \tag{3.6}$$

Where, C_{ox} is oxide capacitance per unit area.

Saturation

Since the channel is cutoff near the drain, the channel charge is concentrated towards the source, and the gate is still electronically disconnected from the body by the channel. Therefore,

$$C_{gs} = \frac{2}{3}(C_{ox}WL + C_{ov}) \tag{3.7}$$

$$C_{gd} = 0 \text{ (No charge near the drain)} \tag{3.8}$$

$$C_{gb} = 0 \tag{3.9}$$

Summary

Mode	C_{gb}	C_{gs}	C_{gd}
Cutoff(Positive V_{GS})	$C_{ox}WL$	C_{ov}	C_{ov}
Linear	0	$(C_{ox}WL)/2 + C_{ov}$	$(C_{ox}WL)/2 + C_{ov}$
Saturation	0	$\frac{2}{3}(C_{ox}WL) + C_{ov}$	C_{ov}

The overlap capacitances C_{ov} depend on the dimensions of the device, and vary from model to model, and is termed as parasitic capacitances.

MOS Diffusion Capacitance

Since the source/drain and the substrate form a p-n junction, there exists some diffusion capacitance betweent the source/drain and body (C_{sb} and C_{db}). These depend on the area and perimeter of the source/drain diffusion region (represented as AS and PS for source and AD and PD for drain, in SPICE models)

$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw} \tag{3.10}$$

$$C_{db} = AD \times C_{jbd} + PD \times C_{jbdsw} \tag{3.11}$$

Where,

- C_{jbs} - Capacitance per unit area of source-body junction
- C_{jbssw} - Capacitance per unit length of source-body junction side-walls
- C_{jbd} - Capacitance per unit area of drain-body junction
- C_{jbdsw} - Capacitance per unit length of drain-body junction side-walls

The above 4 quantites are process-dependent quantites.

4

The circuit diagram described in the Netlist is as below,

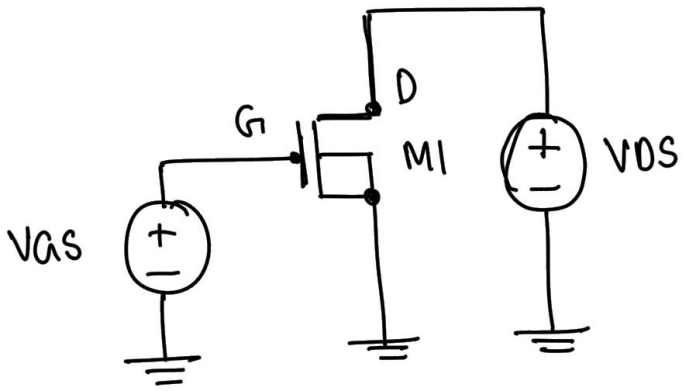

Figure 4.1: Netlist's Circuit Diagram

The Netlist also uses the following parameters:

- VGS - Sine Response with 0 DC offset, Amplitude 1.8V, Frequency 1kHz and -90 degree phase shift. (-1.8cos(1000t) voltage signal)

- VDS - Constant DC Voltage of 0.1V
- $\lambda = 0.09\mu m$
- M1 Dimensions: Width = 20λ, Length = 2λ, AS and AD = 5 x Width x λ, PS and PD = 10λ + 2 x Width

In the netlist it is mentioned that,
x = I_G (-VGS#branch is current going into the source VGS, which is gate current)
y = $\frac{dV_{GS}}{dt}$ (deriv(V(G)))
Therefore, x/y = $\frac{I}{\frac{dV_{GS}}{dt}} = C_{MOS}$
Since the netlist plots x/y vs V(G), we are plotting C_{MOS} vs V_{GS}. As V_{GS} is a sine wave of Amplitude 1.8V and Frequency 1kHz (which is relatively low), we are plotting the C-V Characteristics of the given MOSFET for voltages from -1.8V to 1.8V, at a low frequency, matching the plot mentioned in Figure 3.4.

5

The different second order effects in a MOSFET are as follows:

Channel Length Modulation

Since the cutoff point of the channel, during Saturation, moves further towards the source, with increase in V_{DS} beyond $V_{GS} - V_{TH}$, the effective channel length decreases with increase in V_{DS}. But since the voltage across the channel remains constant ($V_{GS} - V_{TH}$), the reduction in length increases the current through the channel ($I = \frac{V}{R}$ and $R = \rho\frac{L}{A} \implies I \propto \frac{1}{L}$). This effect is modeled in the current equation by the Channel Length Modulation parameter λ.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{5.1}$$

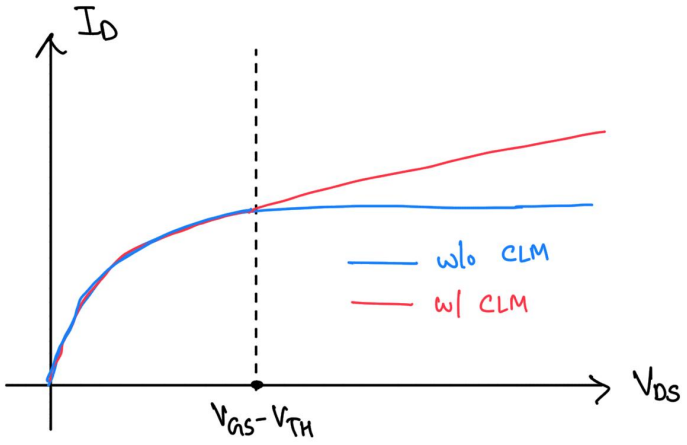

Figure 5.1: Effect of CLM in the I-V Characteristics of a MOSFET

Velocity Saturation

Since the current through the channel is because of the drift of charge carriers through the lattice, there is a certain drain voltage at which drift velocity does not increase any further due to carrier scattering by the molecules of the lattice. This results in current saturation.
The effect is more prominent for large V_{GS}, where velocity saturation may occur before channel cutoff.

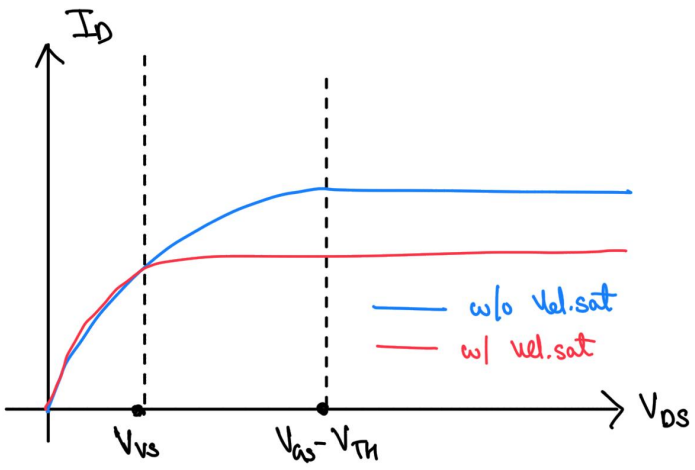

Figure 5.2: Effect of Velocity Saturation, at large V_{GS}

(V_{VS} is the drain voltage at which velocity saturation is attained.)

Mobility Saturation

At a high enough V_{GS} the vertical gate field, the carriers are more strongly attracted towards the gate terminal than the drain. This makes them scatter more, due to collisions with the gate surface, causing mobility to decrease.

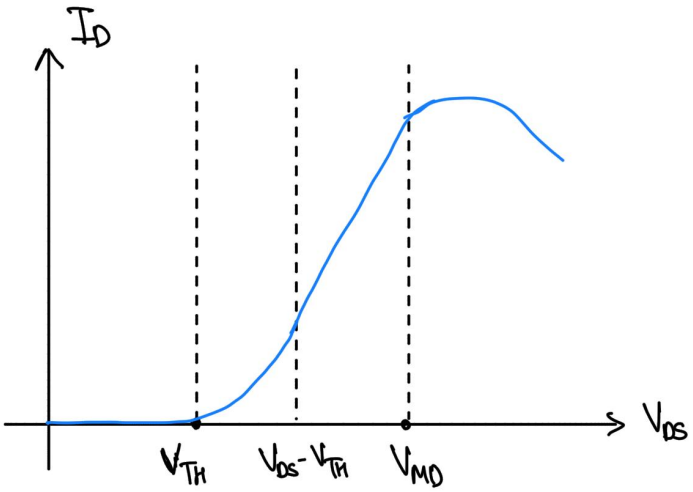

Figure 5.3: I_D vs V_{GS} with Mobility Saturation

(V_{MD} is the gate voltage at which mobility degradation becomes significant)

Drain Induced Barrier Lowering

The electric field due to the drain voltage can also contribute to the inversion of the channel, leading to a reduction in the threshold voltage V_{TH}. This effect is more prominent in short channel MOSFETs and is modelled as,

$$V_{TH} = V_{TH0} - \eta V_{DS} \tag{5.2}$$

Where,

- V_{TH0} - Threshold Voltage at $V_{DS} = 0$.
- η - DIBL Coefficient (Process dependent)

Body Effect

The substrate potential of a MOSFET also affects the threshold voltage of the device. The body terminal acts like a back-capacitor for the channel, increasing electron concentration at the surface with positive substrate potential. It also repels holes towards the depletion region, reducing the

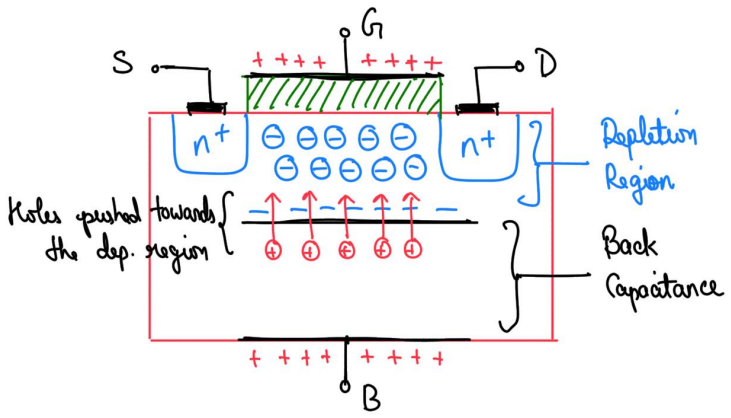

Figure 5.4: Charge Distribution of nMOSFET with Body Effect

depletion width, which reduces the repulsion of free electrons from the surface region.

The Body Effect is modeled using the below equation.

$$V_{TH} = V_{TH0} + \nu(\sqrt{|\psi_s - V_{BS}|} - \sqrt{|\psi_s|}) \tag{5.3}$$

Where,

- V_{TH0} - Threshold voltage at $V_{BS} = 0$
- ψ_s - Surface Potential
- V_{BS} - Body-Source Voltage

Subthreshold Conduction

Ideally, a MOSFET should conduct current across the drain and source only when $V_{GS} \geqslant V_{TH}$. But, as channel formation is a gradual process, not an immediate one, there exists some free electron concentration even below the threshold voltage that allows some conduction to occur. This is termed as Subthreshold leakage, and is significant for large V_{DS}, due to Drain Induced Barrier Lowering. The current due to this leakage is modelled as,

$$I_D = I_{D0} e^{\frac{V_{GS} - V_{TH}}{nV_t}} (1 - e^{\frac{-V_{DS}}{V_t}}) \tag{5.4}$$

Including DIBL and Body effect,

$$I_D = I_{D0} e^{\frac{V_{GS} - V_{TH0} + \eta V_{DS} + k_\nu V_{BS}}{nV_t}} (1 - e^{\frac{-V_{DS}}{V_t}}) \tag{5.5}$$

Where,

- I_{D0} - Current at threshold
- V_t - Thermal Voltage

6

a)

The Netlist used for the simulation is,

```
* Id vs Vgs sweep - NMOS
.include "TSMC_180nm.txt"
.param W = 1.8u
.param L = 0.18u
.global gnd

* circuit
VDS D gnd 0.05
VGS G gnd 0
M1 D G gnd gnd CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L+2*W} PD = {5*L+2*W}

* simulation
.dc VGS 0 1.8 0.1

* plot
.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
plot -VDS#branch deriv(-VDS#branch)
print -VDS#branch deriv(-VDS#branch)
hardcopy q6a_plot.ps -VDS#branch deriv(-VDS#branch)
.endc
.end
```

The simulation data obtained is as follows.

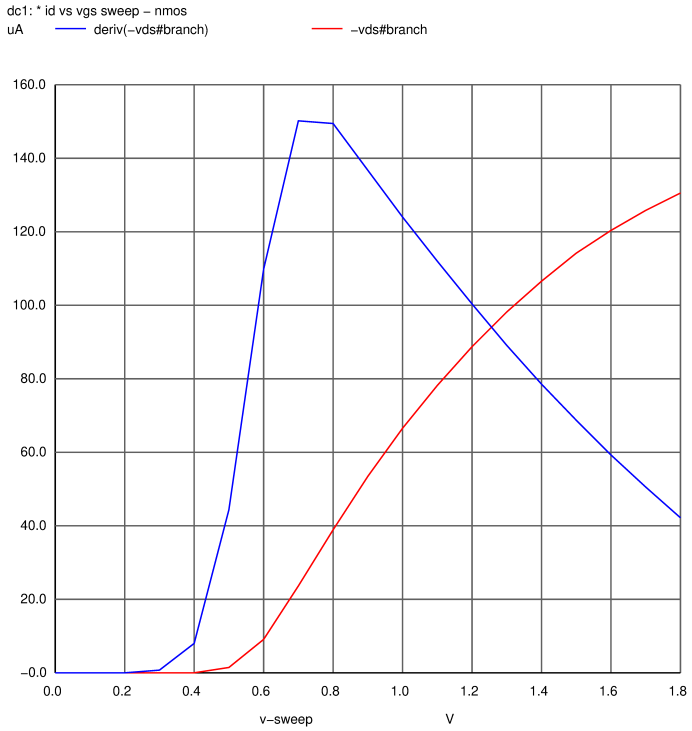

Figure 6.1: Plot of I_D and $\frac{dI_D}{dV_{GS}}$vs V_{GS}

Index	v-sweep	-vds#branch	deriv(-vds#bran
0	0.000000e+00	5.109507e-12	-3.66035e-09
1	1.000000e-01	7.169491e-11	4.992055e-09
2	2.000000e-01	1.003520e-09	6.728031e-08
3	3.000000e-01	1.352776e-08	8.121983e-07
4	4.000000e-01	1.634432e-07	7.882751e-06
5	5.000000e-01	1.590078e-06	4.449081e-05
6	6.000000e-01	9.061605e-06	1.096885e-04
7	7.000000e-01	2.352778e-05	1.501457e-04
8	8.000000e-01	3.909076e-05	1.495623e-04
9	9.000000e-01	5.344024e-05	1.367546e-04
10	1.000000e+00	6.644167e-05	1.238466e-04
11	1.100000e+00	7.820956e-05	1.118370e-04
12	1.200000e+00	8.880906e-05	1.003511e-04
13	1.300000e+00	9.827979e-05	8.926959e-05
14	1.400000e+00	1.066630e-04	7.865095e-05
15	1.500000e+00	1.140100e-04	6.859465e-05
16	1.600000e+00	1.203819e-04	5.918446e-05
17	1.700000e+00	1.258469e-04	5.047419e-05
18	1.800000e+00	1.304768e-04	4.212342e-05

Figure 6.2: Datapoints of above plot

Because of low V_{DS}, the MOSFET is mostly in Linear mode of operation where,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2\right) \tag{6.1}$$

$$\implies I_D = \mu_n C_{ox}\frac{W}{L}V_{DS}V_{GS} - \mu_n C_{ox}\frac{W}{L}V_{DS}\left(V_{TH}+\frac{V_{DS}}{2}\right) \tag{6.2}$$

$$\implies I_D = \mu_n C_{ox}\frac{W}{L}V_{DS}\left(V_{GS}-\left(V_{TH}+\frac{V_{DS}}{2}\right)\right) \tag{6.3}$$

Therefore, the x-intercept of a $I_D - V_{GS}$ plot will give us $V_{TH} - \frac{V_{DS}}{2}$, which can be used to calculate V_{TH} since V_{DS} is known. To minimize the effects of mobility reducing second order effects, we analyse the plot at the datapoint with the maximum $\frac{dI_D}{dV_{GS}}$, represented by deriv(-vds#branch). The maximum value is $1.501\times10^{-4}\ A/V$, attained at $V_{GS}=0.7V$ and $I_D = 2.352\times10^{-5}\ A$. The intercept of the tangent at this point will give us the threshold voltage of the device.
The line equation is given by,

$$y-(2.352\times10^{-5}) = (1.501\times10^{-4})(x-0.7) \tag{6.4}$$

Taking y = 0 for the intercept,

$$\begin{aligned} 0-(2.352\times10^{-5}) &= (1.501\times10^{-4})(V_{TH}+\frac{V_{DS}}{2}-0.7) \\ \implies V_{TH} &= 0.7-\frac{2.352\times10^{-5}}{1.501\times10^{-4}} = 0.7-0.05/2-\frac{0.2352}{1.501} \\ \implies V_{TH} &= 0.7-0.025-0.1566 \\ \therefore\ V_{TH} &= 0.5183\ V \end{aligned}$$

b)

The Netlist used for the simulation is,

```
* Id vs Vgs sweep - NMOS
.include "TSMC_180nm.txt"
.param W = 1.8u
.param L = 0.18u
.global gnd

* circuit
VDS D gnd 1.8
VGS G gnd 0
M1 D G gnd gnd CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L+2*W} PD = {5*L3+2*W}

* simulation
.dc VGS 0 1.8 0.1

* plot
.control
set color0 = white
set color1 = black
set hcopypscolor = 1
```

```
run
plot sqrt(-VDS#branch) deriv(-VDS#branch)
print sqrt(-VDS#branch) deriv(-VDS#branch)
hardcopy q6b_plot.ps sqrt(-VDS#branch) deriv(-VDS#branch)
.endc
.end
```

The simulation data obtained is as follows,

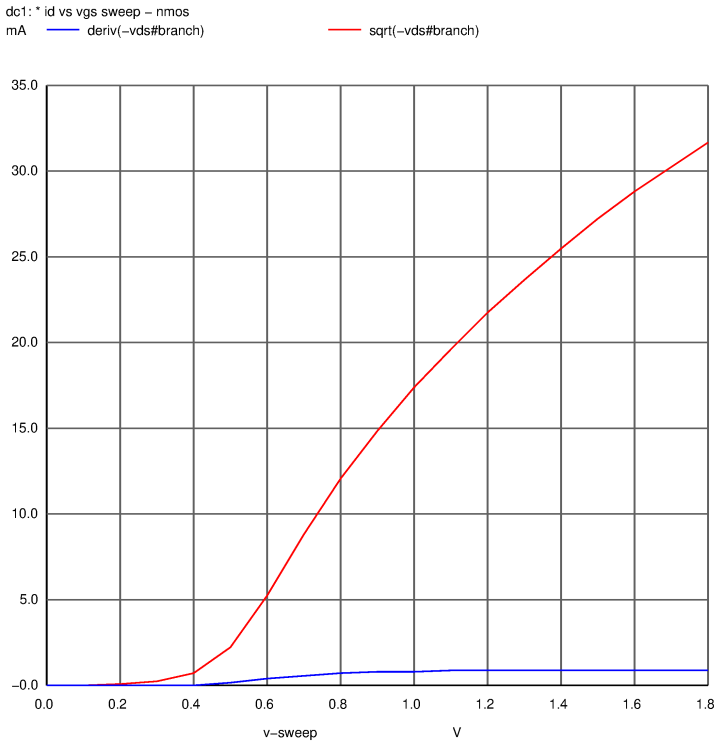

Figure 6.3: Plot of $\sqrt{I_D}$ and $\frac{dI_D}{dV_{GS}}$ vs V_{GS}

Index	v-sweep	sqrt(-vds#branc	deriv(-vds#bran
0	0.000000e+00	4.486394e-06	-1.31782e-08
1	1.000000e-01	1.615754e-05	1.799697e-08
2	2.000000e-01	6.016246e-05	2.394466e-07
3	3.000000e-01	2.194319e-04	2.788420e-06
4	4.000000e-01	7.492019e-04	2.505504e-05
5	5.000000e-01	2.249257e-03	1.341168e-04
6	6.000000e-01	5.233036e-03	3.614599e-04
7	7.000000e-01	8.794950e-03	5.859991e-04
8	8.000000e-01	1.202433e-02	7.140269e-04
9	9.000000e-01	1.483767e-02	7.814344e-04
10	1.000000e+00	1.734564e-02	8.253733e-04
11	1.100000e+00	1.962731e-02	8.560972e-04
12	1.200000e+00	2.172765e-02	8.762879e-04
13	1.300000e+00	2.367464e-02	8.877817e-04
14	1.400000e+00	2.548818e-02	8.923462e-04
15	1.500000e+00	2.718378e-02	8.915415e-04
16	1.600000e+00	2.877422e-02	8.866389e-04
17	1.700000e+00	3.027021e-02	8.786326e-04
18	1.800000e+00	3.168094e-02	8.692909e-04

Figure 6.4: Datapoints of above plot

Since V_{DS} is quite large, the MOSFET is mostly in Saturation. Hence,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.5}$$

$$\implies \sqrt{I_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}(V_{GS} - V_{TH}) \tag{6.6}$$

Therefore, the x-intercept of the above equation will give us the threshold voltage. Hence the reasoning behind plotting $\sqrt{I_D}$ vs V_{GS}. Since we need to construct a line equation for the above, let us take the 2 points near the approximate threshold, $(0.6V, 5.233 \times 10^{-3})\sqrt{A}$ and $(0.7V, 8.795 \times 10^{-3}\sqrt{A})$

The slope at those points is,

$$m = \frac{y2 - y1}{x2 - x1} = \frac{(8.795 - 5.233) \times 10^{-3}}{0.7 - 0.6} = 3.562 \times 10^{-2}\sqrt{A}/V \tag{6.7}$$

Therefore, the line equation can be constructed as,

$$y - (5.233 \times 10^{-3}) = (3.562 \times 10^{-2})(x - 0.6) \tag{6.8}$$

Taking y = 0 for the intercept,

$$0 - (5.233 \times 10^{-3}) = (3.562 \times 10^{-2})(V_{TH} - 0.6)$$

$$V_{TH} = 0.6 - \frac{5.233 \times 10^{-3}}{3.562 \times 10^{-2}}$$

$$V_{TH} = 0.6 - 0.147$$

$$\therefore V_{TH} = 0.453\ V$$

c)

We see that, $V_{TH} = 0.5183$ at $V_{DS} = 50mV$ and $V_{TH} = 0.453$ at $V_{DS} = 1.8V$. Clearly, the threshold voltage has reduced with this increase in drain voltage. This is clearly due to Drain Induced Barrier Lowering, as explained in Q5.

7

To avoid DIBL, let V_{DS} be 50mV, keeping the MOSFET in Linear Mode of Operation. Threshold can be measured using the same algorithm explained in Q6.a). Therefore the line equation to be constructed is of the form given in Equation 6.3, ie,

$$I_D = \mu_n C_{ox} \frac{W}{L} V_{DS} \left(V_{GS} - \left(V_{TH} + \frac{V_{DS}}{2} \right) \right) \tag{7.1}$$

By the above equation we can see that,

$$m = \mu_n C_{ox} \frac{W}{L} V_{DS} \quad \Longrightarrow \quad \mu_n C_{ox} = \frac{m}{\frac{W}{L} V_{DS}} = \frac{m}{10 \times 0.05} \tag{7.2}$$

$$\therefore \ \mu_n C_{ox} \quad = \quad 2m \tag{7.3}$$

$$intercept = V_{TH} + \frac{V_{DS}}{2} \quad \Longrightarrow \quad V_{TH} = intercept - 0.025 \ V \tag{7.4}$$

i) $V_{BS} = 0$

This is the same simulation as done in Q6.a). Therefore we know that,
$m = 1.501 \times 10^{-4} \ A/V$, at $V_{GS} = 0.7V$ and $I_D = 2.352 \times 10^{-5}$ Using the results defined above, we get,

$$\mu_n C_{ox} = 2m = 3.002 \times 10^{-4} \ A/V^2 \tag{7.5}$$

From Q6.a) we know that $V_{TH} = 0.5183 \ V$

ii) $V_{BS} = 0.9 \ V$

The Netlist used for this simulation is,

```
* Id vs Vgs sweep - NMOS
.include "TSMC_180nm.txt"
.param W = 1.8u
.param L = 0.18u
.global gnd

* circuit
VDS D gnd 0.05
VGS G gnd 0
VBS B gnd 0.9

M1 D G gnd B CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L+2*W} PD = {5*L+2*W}

* simulation
.dc VGS 0 1.8 0.1
```

```
* plot
.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
let ioff = i(vds)[0]
plot -(i(vds) - ioff) deriv(-i(vds))
print -(i(vds) - ioff) deriv(-i(vds))
hardcopy q7ii_plot.ps -(i(vds) - ioff) deriv(-i(vds))
.endc
.end
```

Since the substrate is p-type and drain is n-type doped, setting $V_{BS} = 0.9\ V$ when $V_{DS} = 50\ mV$ will keep the body-drain junction in forward bias, creating some diode current on top of the drain current. Since this diode current does not vary with V_{GS}, this will be a constant in our simulation, causing an offset in the plot, as shown below.

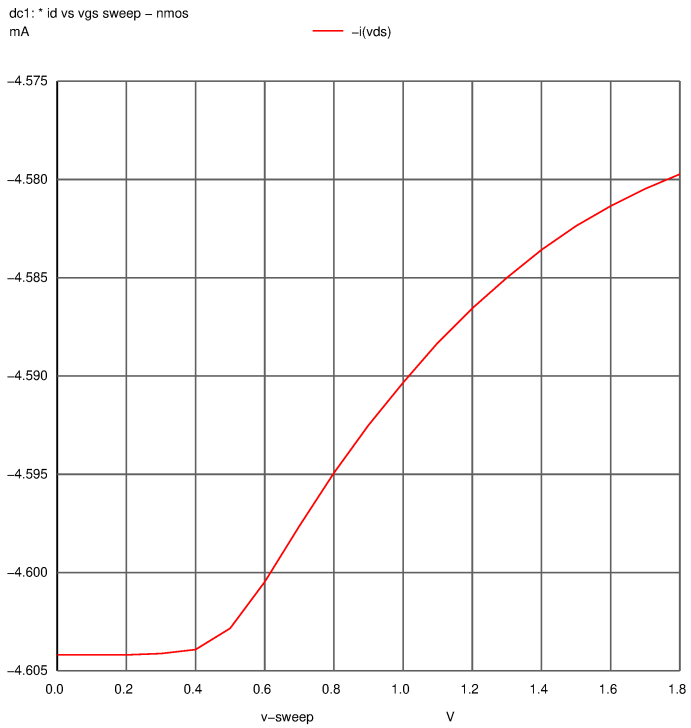

Figure 7.1: I_D vs V_{GS} with body-drain diode current. Clearly, there is an offset of around -4mA

To remove the offset, since this diode current is present at $V_{GS} = 0$ as well, ie, during cutoff, we remove the first reported value of I_D in the V_{GS} sweep, from all the reported values of I_D, giving us the below graph with the diode current offset removed from the drain current.

Note: This offset can also be removed by taking large V_{DS}, making the body-drain junction reverse biased. But this can cause inaccuracies in the reported threshold voltage due to DIBL

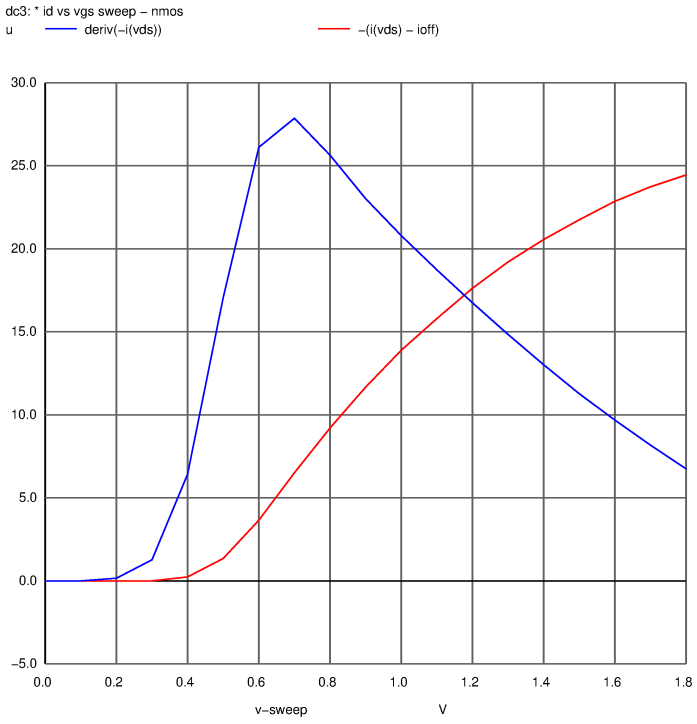

Figure 7.2: I_D vs V_{GS} plot with diode current removed

Index	v-sweep	-(i(vds) - ioff	deriv(-i(vds))
0	0.000000e+00	-0.000000e+00	-1.73122e-08
1	1.000000e-01	9.205757e-11	1.915333e-08
2	2.000000e-01	3.830665e-09	1.715670e-07
3	3.000000e-01	3.440546e-08	1.265321e-06
4	4.000000e-01	2.568950e-07	6.393853e-06
5	5.000000e-01	1.313176e-06	1.708880e-05
6	6.000000e-01	3.674656e-06	2.613558e-05
7	7.000000e-01	6.540292e-06	2.784058e-05
8	8.000000e-01	9.242772e-06	2.564179e-05
9	9.000000e-01	1.166865e-05	2.304467e-05
10	1.000000e+00	1.385171e-05	2.076260e-05
11	1.100000e+00	1.582117e-05	1.869537e-05
12	1.200000e+00	1.759078e-05	1.673386e-05
13	1.300000e+00	1.916794e-05	1.484301e-05
14	1.400000e+00	2.055938e-05	1.302642e-05
15	1.500000e+00	2.177323e-05	1.129939e-05
16	1.600000e+00	2.281926e-05	9.677100e-06
17	1.700000e+00	2.370865e-05	8.170558e-06
18	1.800000e+00	2.445337e-05	6.724030e-06

Figure 7.3: Datapoints of above plot

Using the same algorithm as Q6.a),

The maximum slope is $m = 2.784 \times 10^{-5}\ A/V$ at $V_{GS} = 0.7\ V$ and $I_D = 6.54 \times 10^{-6}\ A$

Therefore,

$$\mu_n C_{ox} = 2m = 5.568 \times 10^{-5} A/V^2$$

The line equation will be,

$$y - 6.54 \times 10^{-6} = 2.784 \times 10^{-5}(x - 0.7) \tag{7.6}$$

Setting y = 0 for the intercept,

$$\begin{aligned} 0 - 6.54 \times 10^{-6} &= 2.784 \times 10^{-5}(V_{TH} + V_{DS}/2 - 0.7) \\ \implies V_{TH} &= 0.7 - 0.05/2 - \frac{6.54 \times 10^{-6}}{2.784 \times 10^{-5}} \\ \implies V_{TH} &\approx 0.675 - 0.235 \\ \implies V_{TH} &\approx 0.44\ V \end{aligned}$$

iii) $V_{BS} = -0.9\ V$

The Netlist used for this simulation is,

```
* Id vs Vgs sweep - NMOS
.include "TSMC_180nm.txt"
.param W = 1.8u
.param L = 0.18u
.global gnd

* circuit
VDS D gnd 0.05
VGS G gnd 0
VBS B gnd -0.9

M1 D G gnd B CMOSN W={W} L={L}
+AS = {2.5*W*L} AD = {2.5*W*L} PS = {5*L+2*W} PD = {5*L+2*W}

* simulation
.dc VGS 0 1.8 0.1

* plot
.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
plot -i(vds) deriv(-i(vds))
print -i(vds) deriv(-i(vds))
hardcopy q7iii_plot.ps -i(vds) deriv(-i(vds))
.endc
.end
```

Simulation data obtained,

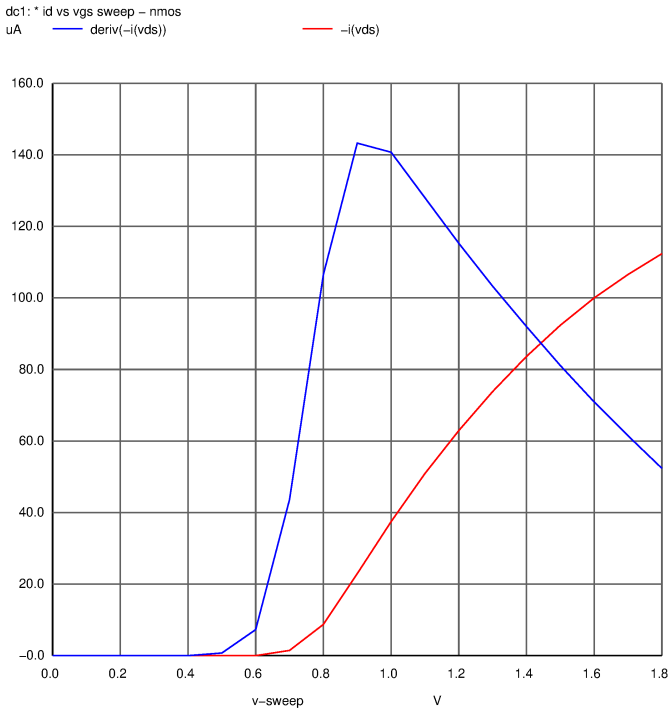

Figure 7.4: Plot of I_D vs V_{GS}

Index	v-sweep	-i(vds)	deriv(-i(vds))
0	0.000000e+00	9.541031e-13	-6.52721e-12
1	1.000000e-01	9.658073e-13	6.761293e-12
2	2.000000e-01	2.306362e-12	1.241949e-10
3	3.000000e-01	2.580479e-11	2.251513e-09
4	4.000000e-01	4.526089e-10	3.953249e-08
5	5.000000e-01	7.932302e-09	6.160627e-07
6	6.000000e-01	1.236651e-07	7.207742e-06
7	7.000000e-01	1.449481e-06	4.349691e-05
8	8.000000e-01	8.823047e-06	1.065944e-04
9	9.000000e-01	2.276836e-05	1.431153e-04
10	1.000000e+00	3.744611e-05	1.406870e-04
11	1.100000e+00	5.090577e-05	1.280195e-04
12	1.200000e+00	6.305002e-05	1.152923e-04
13	1.300000e+00	7.396422e-05	1.033021e-04
14	1.400000e+00	8.371045e-05	9.189850e-05
15	1.500000e+00	9.234392e-05	8.107716e-05
16	1.600000e+00	9.992588e-05	7.090592e-05
17	1.700000e+00	1.065251e-04	6.144791e-05
18	1.800000e+00	1.122155e-04	5.235926e-05

Figure 7.5: Datapoints of above plot

The maximum slope is $m = 1.431 \times 10^{-4}\ A/V$ obtained at $V_{GS} = 0.9\ V$ and $I_D = 2.276 \times$

10^{-5} A

Therefore,

$$\mu_n C_{ox} = 2m = 2.862 \times 10^{-4} A/V^2$$

The line equation will be,

$$y - 2.276 \times 10^{-5} = 1.431 \times 10^{-4}(x - 0.9) \tag{7.7}$$

Setting y = 0, to get the intercept,

$$\begin{aligned} 0 - 2.276 \times 10^{-5} &= 1.431 \times 10^{-4}(V_{TH} + V_{DS}/2 - 0.9) \\ \implies V_{TH} &= 0.9 - 0.025 - \frac{2.276 \times 10^{-5}}{1.431 \times 10^{-4}} \\ \implies V_{TH} &= 0.9 - 0.025 - 0.159 \\ \implies V_{TH} &= 0.716\ V \end{aligned}$$

Summary

The results obtained are as below,

V_{BS} (V)	$\mu_n C_{ox}$ (A/V)	V_{TH} (V)
0	3.002×10^{-4}	0.5183
0.9	5.568×10^{-5}	0.44
-0.9	2.862×10^{-4}	0.716

The change in V_{TH} is as expected by Body Effect, as explained in Q5, where an increase in body potential reduces the threshold voltage of the device and vice-versa.
Also, the large variation in $\mu_n C_{ox}$ for $V_{BS} = 0.9$ is due to the backward body-drain diode current, which is in the opposite direction to the normal drain current. This current, which is much larger than normal drain current (milliamps as compared to microamps) injects holes into the channel, thereby reducing electron mobility (μ_n) significantly.

8

The Netlist for the circuits are as below.

Series MOSFET Circuit

```
*Id vs Vds plot
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.18u
.global gnd
```

```
*circuit

VDS D1 gnd 0
VGS G gnd 1 ; to ensure both linear and saturation is attained
M1 D1 G D2 D2 CMOSN W={W} L={L}
+AS={2.5*L*W} AD = {2.5*L*W} PS = {5*L+2*W} PD = {5*L+2*W}
M2 D2 G gnd gnd CMOSN W={W} L={L}
+AS={2.5*L*W} AD = {2.5*L*W} PS = {5*L+2*W} PD = {5*L+2*W}

*simulation
.dc VDS 0 1.8 0.1

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

run
plot -i(VDS)
print -i(VDS)
hardcopy q8a_plot.ps -i(VDS)

.endc
.end
```

Long Channel MOSFET Circuit

```
*Id vs Vds Sweep
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.36u
.global gnd

* circuit

VDS D gnd 0
VGS G gnd 1 ; to ensure both linear and saturation is attained
M1 D G gnd gnd CMOSN W={W} L={L}
+AS={2.5*L*W} AD = {2.5*L*W} PS = {5*L+2*W} PD = {5*L+2*W}

*simulation
.dc VDS 0 1.8 0.1

.control
set color0 = white
set color1 = black
set hcopypscolor = 1

run
plot -i(VDS)
print -i(VDS)
hardcopy q8b_plot.ps -i(VDS)

.endc
.end
```

The gate voltage is kept at 1V, in order to observe both Linear and Saturation Modes of Operation.
Simulation data for circuit (a), ie, 2 MOSFETS of Length L in series,

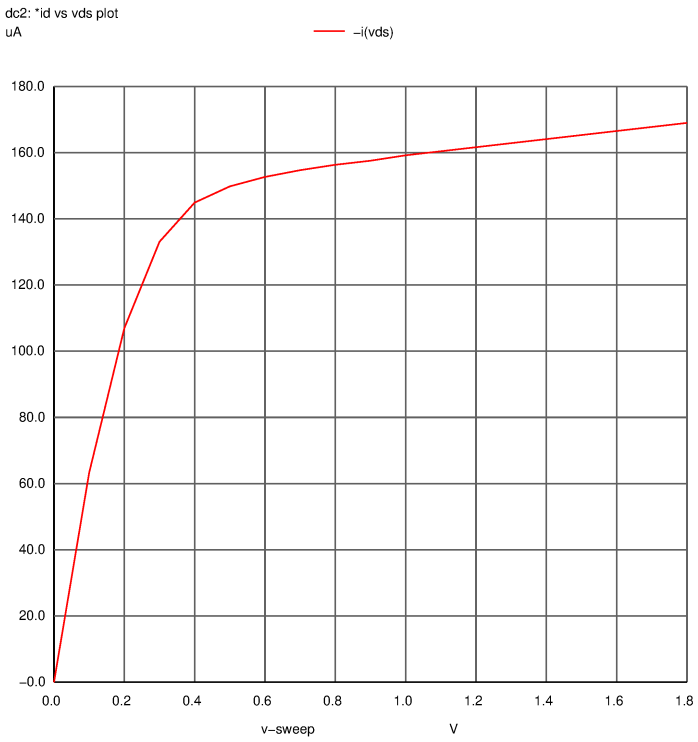

Figure 8.1: Plot of I_D vs V_{DS}

Index	v-sweep	-i(vds)
0	0.000000e+00	-2.05709e-34
1	1.000000e-01	6.328052e-05
2	2.000000e-01	1.070357e-04
3	3.000000e-01	1.331139e-04
4	4.000000e-01	1.450297e-04
5	5.000000e-01	1.498833e-04
6	6.000000e-01	1.525468e-04
7	7.000000e-01	1.545456e-04
8	8.000000e-01	1.562303e-04
9	9.000000e-01	1.577453e-04
10	1.000000e+00	1.591571e-04
11	1.100000e+00	1.605003e-04
12	1.200000e+00	1.617946e-04
13	1.300000e+00	1.630521e-04
14	1.400000e+00	1.642805e-04
15	1.500000e+00	1.654851e-04
16	1.600000e+00	1.666695e-04
17	1.700000e+00	1.678364e-04
18	1.800000e+00	1.689875e-04

Figure 8.2: Datapoints of above plot

Simulation data for circuit (b), ie, 1 longer channel MOSFET,

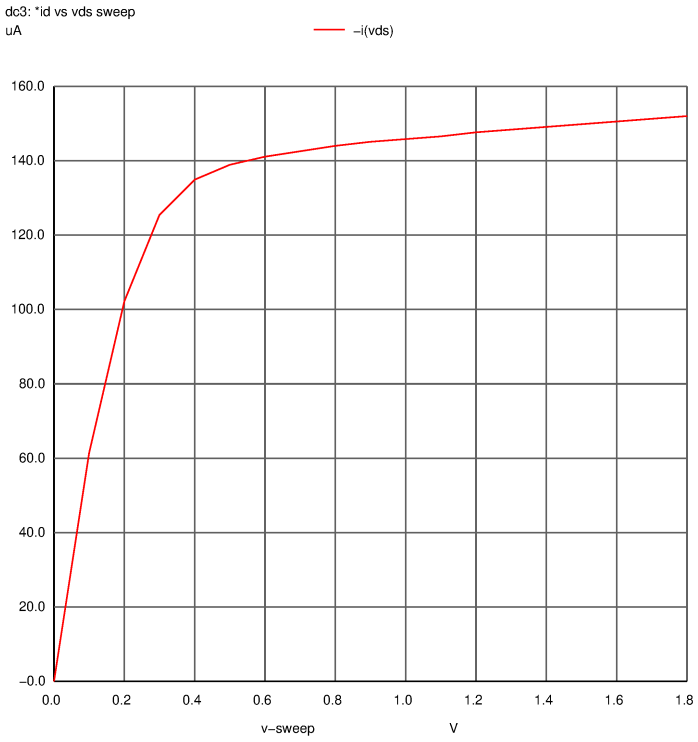

Figure 8.3: Plot of I_D vs V_{DS}

Index	v-sweep	-i(vds)
0	0.000000e+00	-1.35720e-20
1	1.000000e-01	6.151053e-05
2	2.000000e-01	1.023432e-04
3	3.000000e-01	1.252930e-04
4	4.000000e-01	1.350625e-04
5	5.000000e-01	1.390200e-04
6	6.000000e-01	1.411915e-04
7	7.000000e-01	1.427000e-04
8	8.000000e-01	1.438974e-04
9	9.000000e-01	1.449246e-04
10	1.000000e+00	1.458491e-04
11	1.100000e+00	1.467068e-04
12	1.200000e+00	1.475190e-04
13	1.300000e+00	1.482987e-04
14	1.400000e+00	1.490546e-04
15	1.500000e+00	1.497926e-04
16	1.600000e+00	1.505168e-04
17	1.700000e+00	1.512303e-04
18	1.800000e+00	1.519354e-04

Figure 8.4: Datapoints of above plot

Comparision:

We can see that the maximum drain current value reached in circuit (a) is 1.689×10^{-4} A and in circuit (b) is $1.519 \times 10^{-4} A$. Clearly the max. current in the cascoding MOSFET circuit is higher.

This can be attributed to differences in Channel Length Modulation amongst the 2 MOSFET circuits.

The longer channel MOSFET has a lower CLM parameter than the cascade MOSFET setup, since the cascade has 2 separate cutoff points, in each MOSFET, each of which moves towards their respective source, thereby exhibiting a greater CLM effect, than the long channel MOSFET, with only 1 cutoff point.

This difference in CLM can be analyzed by comparing the slope of the plot at saturation, since any increase in current during saturation is due to CLM. Approximate slope of the cascode circuit plot, (choosing points 16 and 17 from the datapoints)

$$m_1 = \frac{1.6783 \times 10^{-4} - 1.6666 \times 10^{-4}}{1.7 - 1.6} = \frac{0.0117 \times 10^{-4}}{0.1} = 1.17 \times 10^{-5}\ A/V$$

Approximate slope of the long channel circuit plot, (choosing points 16 and 17 from the datapoints)

$$m_2 = \frac{1.5123 \times 10^{-4} - 1.5051 \times 10^{-4}}{1.7 - 1.6} = \frac{0.0072 \times 10^{-4}}{0.1} = 7.2 \times 10^{-6}\ A/V$$

Clearly $m_1 > m_2$, i.e, the effect of CLM is more prominent in the cascode circuit than the long channel MOSFET circuit.

9

The Netlist for the 2 circuit simulations are as follows,

ON Circuit

```
.include TSMC_180nm.txt
.param L = 0.18u
.param W = 1.8u
.global gnd

VGS G gnd 1.8
VDS D gnd 1.8

M1 D G gnd gnd CMOSN W={W} L={L}
+ AS={2.5*W*L} PS={5*L+2*W} AD={2.5*W*L} PD={5*L+2*W}

.control
foreach val 1.8u 3.6u 18u 36u
        alterparam W=$val
        reset
        op
        print -i(VDS)
        echo --------------------------------
end
.endc
.end
```

OFF Circuit

```
.include TSMC_180nm.txt
.param L = 0.18u
.param W = 1.8u
.global gnd

VGS G gnd 0
VDS D gnd 1.8

M1 D G gnd gnd CMOSN W={W} L={L}
+ AS={2.5*W*L} PS={5*L+2*W} AD={2.5*W*L} PD={5*L+2*W}

.control
foreach val 1.8u 3.6u 18u 36u
        alterparam W=$val
        reset
        op
        print -i(VDS)
        echo --------------------------------
end
.endc
.end
```

The Simulation output is as follows,

```
No. of Data Rows : 1
-i(vds) = 1.003682e-03
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 1.941162e-03
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 8.979366e-03
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 1.674825e-02
--------------------------------
```

Figure 9.1: Simulation Data for ON Circuit

```
No. of Data Rows : 1
-i(vds) = 2.012773e-11
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 3.467543e-11
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 1.523756e-10
--------------------------------
Reset re-loads circuit *include TSMC_180nm.txt

Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 1
-i(vds) = 2.996551e-10
--------------------------------
```

Figure 9.2: Simulation Data for OFF Circuit

Tabulating the obtained datapoints we get,

Width	I_{ON} (A)	I_{OFF} (A)
$1.8\mu m$	1.005×10^{-3}	2.012×10^{-11}
$3.6\mu m$	1.941×10^{-3}	3.467×10^{-11}
$18\mu m$	8.979×10^{-3}	1.523×10^{-10}
$36\mu m$	1.674×10^{-2}	2.996×10^{-10}

For I_{ON} :

I_{ON} approximately increases with width linearly. This is explained by the formula for drain current in Saturation mode,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Which implies that $I_D \propto W$, explaining the observed behavior.

For I_{OFF} :

We know that, from Equation 5.5 in Q5, that for subthreshold leakage current,

$$I_D \propto I_{D0} \tag{9.1}$$

Where, I_{D0} is the current at $V_{GS} = V_{TH}$, ie, edge of Linear mode. We know that for Linear mode $I_{D0} \propto W$, from Equation 2.2 in Q2. Therefore,

$$I_D \propto W \tag{9.2}$$

which approximately matches the observed behavior.

10

The Netlist for the switch circuits are as follows,

i) $v_c(0^-) = 0,\ V_{in} = 1.8V$

```
.global gnd

Vin P gnd 1.8
Cp P gnd 100f

.ic V(P) = 0
.tran 0.1n 1u

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
plot V(P)
hardcopy q10sw_plot_i.ps V(P)
.endc
.end
```

ii) $v_c(0^-) = 1.8\ V,\ V_{in} = 0$

```
.global gnd

Vin P gnd 0
Cp P gnd 100f

.ic V(P) = 1.8
.tran 0.1n 1u

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run
```

```
plot V(P)
hardcopy q10sw_plot_ii.ps V(P)
.endc
.end
```

The plots obtained are as follows,

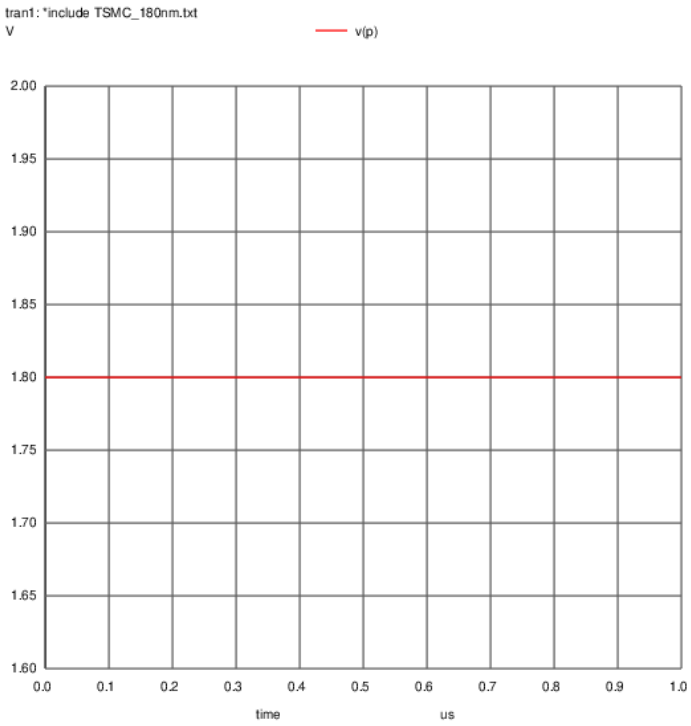

Figure 10.1: Plot of v_c over time in Circuit (i)

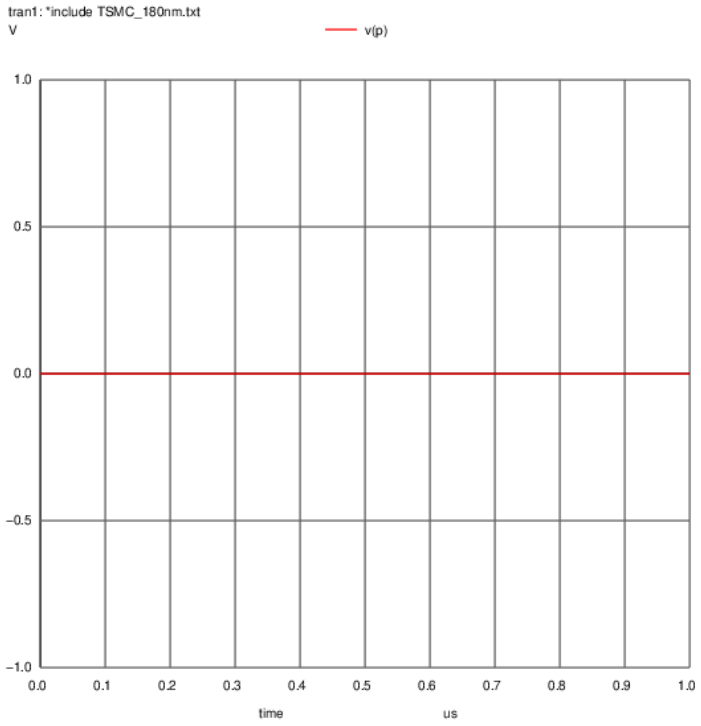

Figure 10.2: Plot of v_c over time in Circuit (ii)

Clearly, we see instantaneous charging and discharging respectively, due to an ideal switch not having any ON resistance. The same result cannot be expected in the MOSFET circuits since they will give some ON resistance to the current through them.

a) NMOS Switch

The Netlist for the charging and discharging circuits are as follows,

i)Charging:

```
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.18u
.global gnd

Vin D gnd 1.8
VGS G gnd 1.8
M1 D G P P CMOSN L={L} W={W}
+AS={2.5*W*L} AD={2.5*W*L} PS={5*L+2*W} PD={5*L+2*W}
Cp P gnd 100f

.ic V(P) = 0
.tran 0.1u 1m

.control
```

```
set color0 = white
set color1 = black
set hcopypscolor = 1
run

*Charging Time Measurement
meas tran vfin FIND v(P) AT=1m
let vt = 0.632*vfin
meas tran tau WHEN v(P)=vt RISE=1

plot V(P)
print tau
hardcopy q10nmos_plot_i.ps V(P)
.endc
.end
```

Simulation Data obtained,

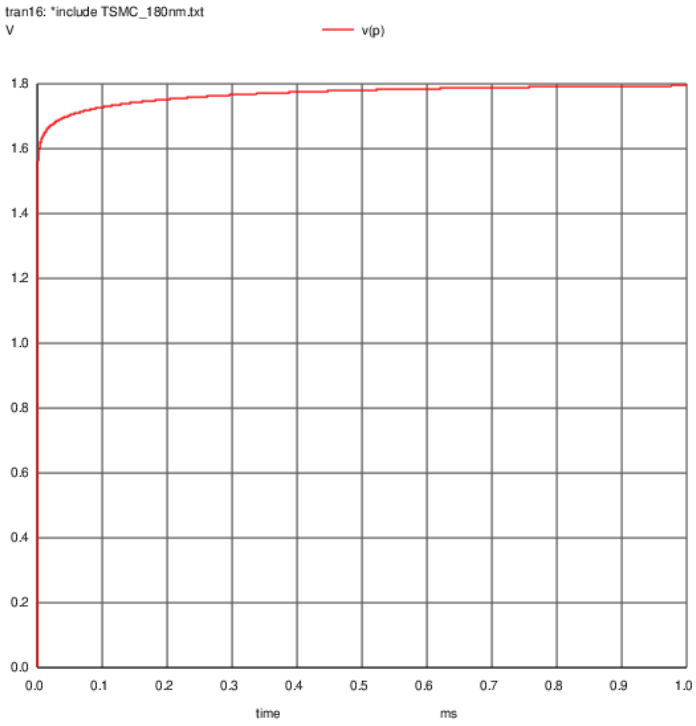

Figure 10.3: Plot of v_c over time

```
Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
d                                          1.8
g                                          1.8
p                                            0
vgs#branch                                   0
vin#branch                          -0.00100368

 Reference value :  7.35680e-04
No. of Data Rows : 10014
vfin               =  1.794197e+00
tau                =  1.184687e-09
Warning: Missing charsets in String to FontSet conversion
tau = 1.184687e-09

The file "q10nmos_plot_i.ps" may be printed on a postscript printer.
```

Figure 10.4: Output of Simulation and Time Constant Measurement

Measured Time Constant $= 1.184 \times 10^{-9}\ s$

ii) Discharging

```
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.18u
.global gnd

Vin D gnd 0
VGS G gnd 4
M1 D G D P CMOSN L={L} W={W} AS={2.5*W*L} AD={2.5*W*L} PS={5*L+2*W} PD={5*L+2*W}
Cp P gnd 100f

.ic V(P) = 1.8
.tran 0.1u 1m

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

*Charging Time Measurement
meas tran vinit FIND v(P) AT=1p
let vt = (1-0.632)*vinit
meas tran tau WHEN v(P)=vt FALL=1

plot V(P)
print tau
hardcopy q10nmos_plot_ii.ps V(P)
.endc
.end
```

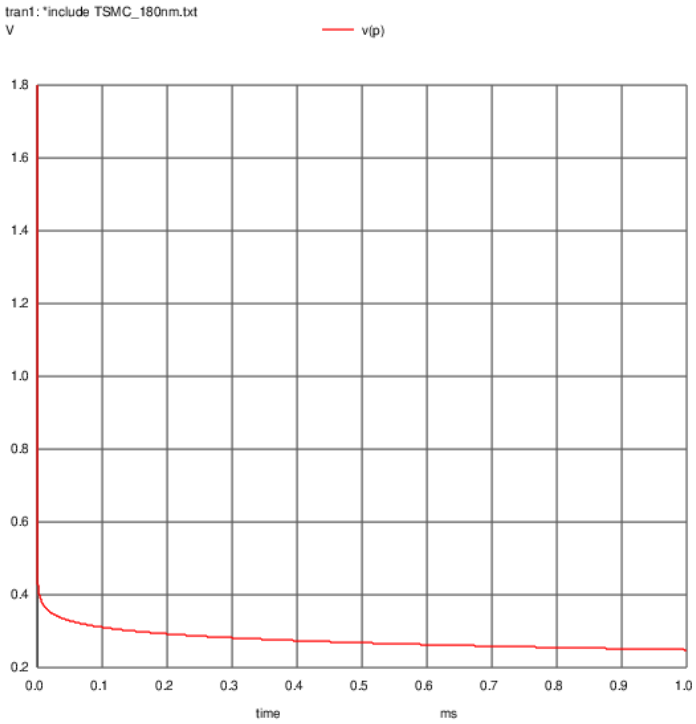

Figure 10.5: Plot of v_c over time

```
Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
d                                            0
g                                          1.8
p                                          1.8
vgs#branch                                   0
vin#branch                            0.266459

 Reference value :  7.23717e-04
No. of Data Rows : 10014
vinit               =  1.798905e+00
tau                 =  1.108463e-09
Warning: Missing charsets in String to FontSet conversion
tau = 1.108463e-09

The file "q10nmos_plot_ii.ps" may be printed on a postscript printer.
```

Figure 10.6: Output of Simulation and Time Constant Measurement

Measured Time Constant $= 1.1083 \times 10^{-9}$ s

b) PMOS Switch

The Netlist for the charging and discharging circuits are as follows,

i) Charging

```
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.18u
.global gnd

Vin D gnd 1.8
VGS G gnd 0
M1 D G D P CMOSP L={L} W={W} AS={2.5*W*L} AD={2.5*W*L} PS={5*L+2*W} PD={5*L+2*W}
Cp P gnd 100f

.ic V(P) = 0
.tran 0.1u 1m

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

*Charging Time Measurement
meas tran vfin FIND v(P) AT=1m
let vt = 0.632*vfin
meas tran tau WHEN v(P)=vt RISE=1

plot V(P)
print tau
hardcopy q10pmos_plot_i.ps V(P)
.endc
.end
```

Simulation Data obtained,

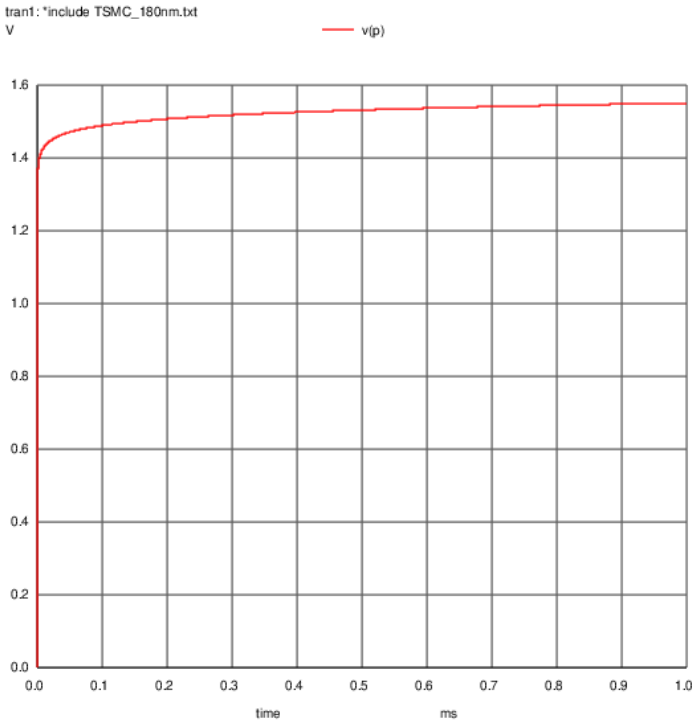

Figure 10.7: Plot of v_c over time

```
Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
d                                          1.8
g                                            0
p                                            0
vgs#branch                                   0
vin#branch                            -0.230088

 Reference value :  7.19710e-04
No. of Data Rows : 10013
vfin                =  1.550802e+00
tau                 =  7.928109e-10
Warning: Missing charsets in String to FontSet conversion
tau = 7.928109e-10

The file "q10pmos_plot_i.ps" may be printed on a postscript printer.
```

Figure 10.8: Output of Simulation and Time Constant Measurement

Measured Time Constant $= 7.928 \times 10^{-10}$ s

ii) Discharging

```
.include TSMC_180nm.txt
.param W = 1.8u
.param L = 0.18u
.global gnd

Vin D gnd 0
VGS G gnd 0
M1 D G P P CMOSP L={L} W={W} AS={2.5*W*L} AD={2.5*W*L} PS={5*L+2*W} PD={5*L+2*W}
Cp P gnd 100f

.ic V(P) = 1.8
.tran 0.1u 1m

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

*Charging Time Measurement
meas tran vinit FIND v(P) AT=1p
let vt = (1-0.632)*vinit
meas tran tau WHEN v(P)=vt FALL=1

plot V(P)
print tau
hardcopy q10pmos_plot_ii.ps V(P)
.endc
.end
```

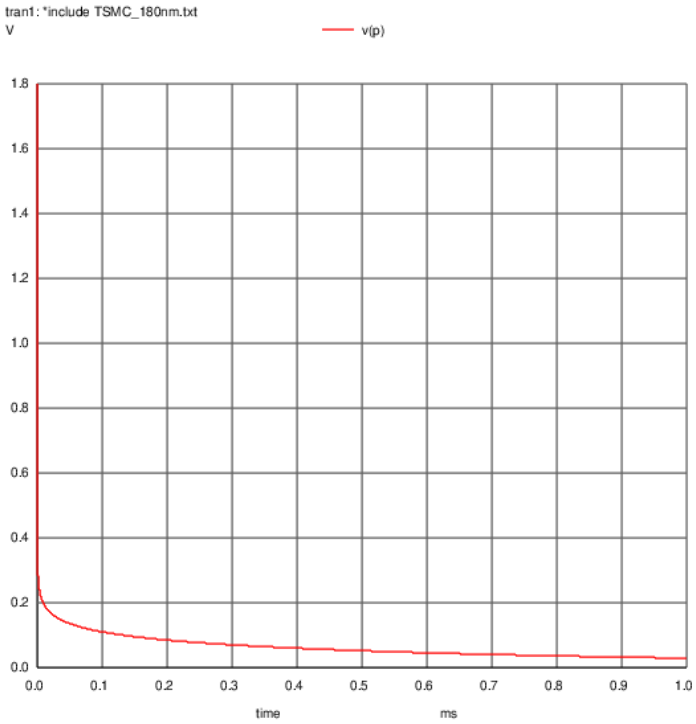

Figure 10.9: Plot of v_c over time

```
Circuit: *include TSMC_180nm.txt

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
d                                            0
g                                            0
p                                          1.8
vgs#branch                                   0
vin#branch                         0.000474907

 Reference value :  6.12384e-04
No. of Data Rows : 10016
vinit              =  1.799160e+00
tau                =  1.920445e-09
Warning: Missing charsets in String to FontSet conversion
tau = 1.920445e-09

The file "q10pmos_plot_ii.ps" may be printed on a postscript printer
```

Figure 10.10: Output of Simulation and Time Constant Measurement

Measured Time Constant $= 1.92 \times 10^{-9}$ s

Summary

In both the MOS based switches, there is some time delay to reach the steady state, due to the intrinsic and parasitic capacitances of the MOSFET.
The output voltage also does not match the input voltage, due to the threshold voltage drop across the MOSFET, and the resistance offered by the channel. Also, since the voltage across the capacitor is the source terminal in the NMOS charging/PMOS discharging and the voltage source is the source terminal in the NMOS discharging/PMOS charging circuits, V_{GS} will not always be above V_{TH}, especially when v_c or $V_{in} = V_{GS} - V_{TH}$, causing a significant voltage difference between the initial and final output voltages.
However this effect is not always present due to leakage currents, as in cutoff mode, the capacitor or source is left floating, without an undefined voltage.

11

a)

The Netlist for the circuit is given below,

```
.include TSMC_180nm.txt
.param L=0.18u
.param Wn=1.8u
.param Wp=2.5*Wn
.global gnd

Vin A gnd pulse 0 1.8 0n 100p 100p 9.9n 20n
Vdd VD gnd 1.8

Mp1 B A VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn1 B A gnd gnd CMOSN L={L} W={Wn}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}
Mp2 C B VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn2 C B gnd gnd CMOSN L={L} W={Wp}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}

CL C gnd 100f

.tran 0.1n .1u

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

meas tran rise TRIG v(A) VAL=0.9 RISE=1 TARG v(C) VAL=0.9 RISE=1
meas tran fall TRIG v(A) VAL=0.9 FALL=1 TARG v(C) VAL=0.9 FALL=1
let delay = (rise + fall)/2
```

```
plot V(A) V(C)
print delay
hardcopy q11a_plot.ps V(A) V(C)

.endc
.end
```

The Simulation Data is as follows,

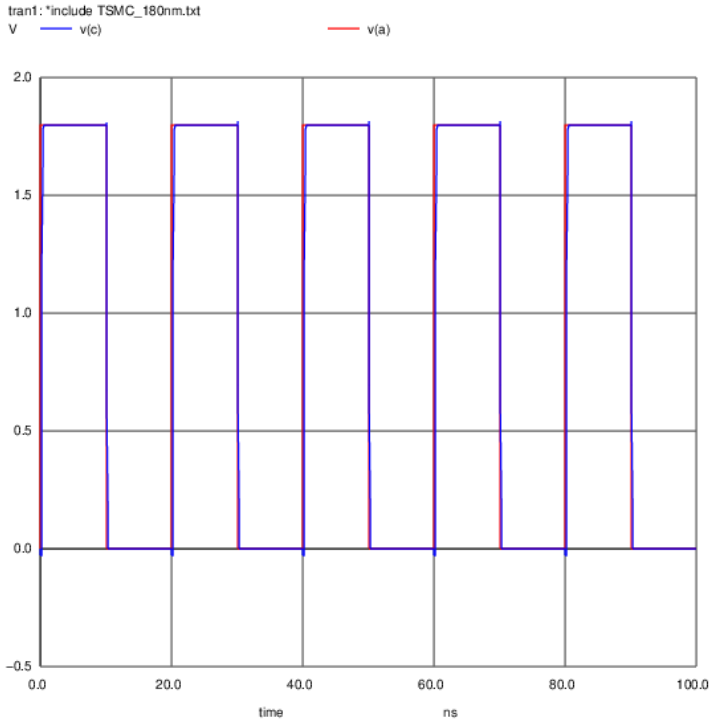

Figure 11.1: Plot of V_{in}(Red) and V_{out}(Blue) vs time

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                            0
vd                                         1.8
b                                          1.8
c                                    3.42883e-09
vdd#branch                          -4.16062e-11
vin#branch                                   0


No. of Data Rows : 1112
rise               =  1.731999e-10 targ=  2.231999e-10 trig=  5.000000e-11
fall               =  1.157769e-10 targ=  1.016578e-08 trig=  1.005000e-08
Warning: Missing charsets in String to FontSet conversion
delay = 1.444884e-10
```

Figure 11.2: Measurement Results

b)

The Netlist for the circuit is given below,

```
.include TSMC_180nm.txt
.param L=0.18u
.param Wn=1.8u
.param Wp=2.5*Wn
.global gnd

Vin A gnd pulse 0 1.8 0n 100p 100p 9.9n 20n
Vdd VD gnd 1.8

Mp1 B A VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn1 B A gnd gnd CMOSN L={L} W={Wn}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}
Mp2 C B VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn2 C B gnd gnd CMOSN L={L} W={Wp}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}

CL C gnd 500f

.tran 0.1n .1u

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

meas tran rise TRIG v(A) VAL=0.9 RISE=1 TARG v(C) VAL=0.9 RISE=1
meas tran fall TRIG v(A) VAL=0.9 FALL=1 TARG v(C) VAL=0.9 FALL=1
let delay = (rise + fall)/2

plot V(A) V(C)
print delay
hardcopy q11b_plot.ps V(A) V(C)

.endc
.end
```

The Simulation Data is as follows,

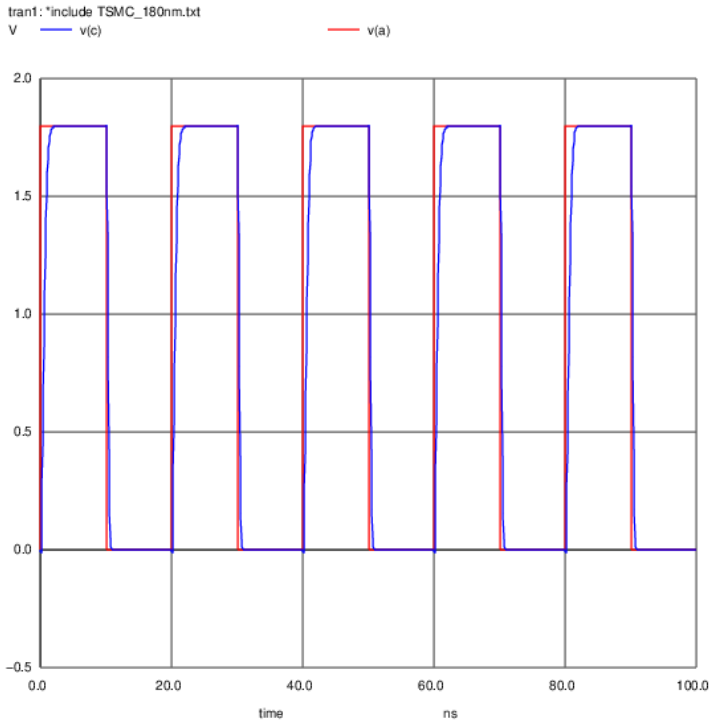

Figure 11.3: Plot of V_{in}(Red) and V_{out}(Blue) vs time

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                           0
vd                                        1.8
b                                         1.8
c                                   3.42883e-09
vdd#branch                         -4.16062e-11
vin#branch                                  0


No. of Data Rows : 1113
rise               =  4.982555e-10 targ=  5.482555e-10 trig=  5.000000e-11
fall               =  2.689461e-10 targ=  1.031895e-08 trig=  1.005000e-08
Warning: Missing charsets in String to FontSet conversion
delay = 3.836008e-10
```

Figure 11.4: Measurement Results

c)

The Netlist for the circuit is given below,

```
..include TSMC_180nm.txt
.param L=0.18u
.param Wn=9u
.param Wp=2.5*Wn
.global gnd

Vin A gnd pulse 0 1.8 0n 100p 100p 9.9n 20n
Vdd VD gnd 1.8

Mp1 B A VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn1 B A gnd gnd CMOSN L={L} W={Wn}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}
Mp2 C B VD VD CMOSP L={L} W={Wp}
+AS={2.5*L*Wp} AD={2.5*L*Wp} PS={5*L+2*Wp} PD={5*L+2*Wp}
Mn2 C B gnd gnd CMOSN L={L} W={Wp}
+AS={2.5*L*Wn} AD={2.5*L*Wn} PS={5*L+2*Wn} PD={5*L+2*Wn}

CL C gnd 500f

.tran 0.1n .1u

.control
set color0 = white
set color1 = black
set hcopypscolor = 1
run

meas tran rise TRIG v(A) VAL=0.9 RISE=1 TARG v(C) VAL=0.9 RISE=1
meas tran fall TRIG v(A) VAL=0.9 FALL=1 TARG v(C) VAL=0.9 FALL=1
let delay = (rise + fall)/2

plot V(A) V(C)
print delay
hardcopy q11c_plot.ps V(A) V(C)

.endc
.end
```

The Simulation Data is as follows,

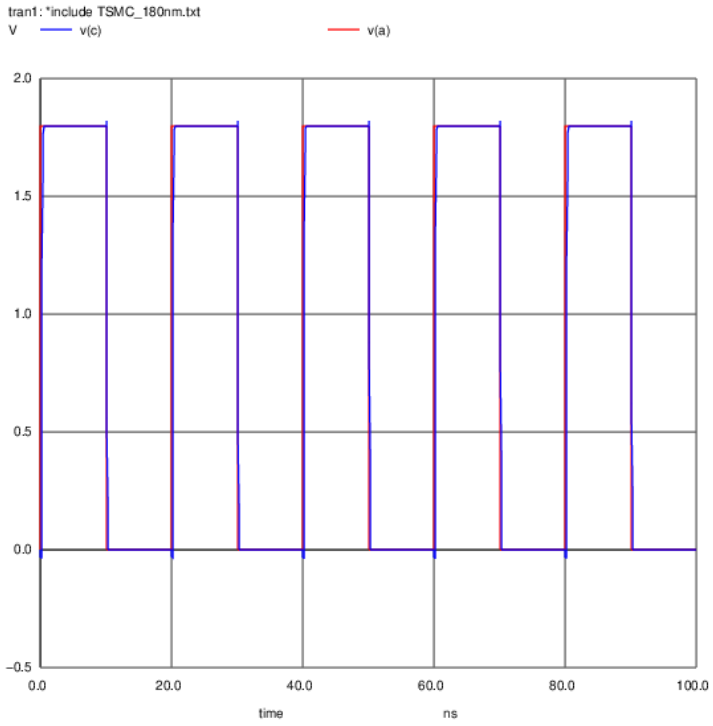

Figure 11.5: Plot of V_{in}(Red) and V_{out}(Blue) vs time

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
a                                            0
vd                                         1.8
b                                          1.8
c                                    4.08429e-09
vdd#branch                          -1.73071e-10
vin#branch                                   0


No. of Data Rows : 1187
rise               =  1.837544e-10 targ=  2.337544e-10 trig=  5.000000e-11
fall               =  1.231941e-10 targ=  1.017319e-08 trig=  1.005000e-08
Warning: Missing charsets in String to FontSet conversion
delay = 1.534742e-10
```

Figure 11.6: Measurement Results

Summary:

The data obtained is as follows

C_L(fF)	$W_n(\mu$m)	t_{pd}(s)
100	1.8	1.444×10^{-10}
500	1.8	3.836×10^{-10}
500	9	1.534×10^{-10}

From this, we can infer the following results,

- Propagation delay is directly related to the Capacitive Load. A possible reasoning for this is the increased overall Time Constant of the circuit, with higher capacitive loads, leading to higher charging and discharging times.
- Propagation delay is inversely related to the Width of the MOSFETs. A possible reasoning for this could be a higher current due to lesser resistance across the MOSFETs, leading to faster charging and discharging speeds. However this increases the input capacitance of the device, so increasing width to reduce delay may not always be ideal.