VLSI Design : Assignment-2

Monsoon 2025, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Release Date: 25 Aug 2025, Due date : 10 Sep, 2025 (18:00 HRS)

Instructions:

1. Submit your assignment as a single file in pdf format (Name_RollNo.pdf)
2. Use the given 180 nm technology file for the NGSPICE simulations and $SCN6M\_DEEP.09.tech27$ for MAGIC layout
3. Consider lengths of NMOS and PMOS to be equal ($L_n = L_p$), and $V_{DD} = 1.8V$ until stated otherwise
4. Use 'set curplottitle= Your-name-roll-question-number-part' for every plot in your report so that it is printed on the top of each plot
5. Answers should be complete and must be presented in a systematic way with explanation, plots, annotations and netlist
6. Maximum marks for each question is 10. Bonus marks (10) will be given for a good report
7. Utilize moodle platform to discuss and clear your questions. Discussion is highly encouraged.

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1. Install MAGIC and do the inverter layout example shown in the tutorial.
   (No need to submit this part).

2. Using NGSPICE, design a minimum sized CMOS inverter ($L = 0.18\mu m$, $W_n = 0.27\mu m$) such that the rise time and fall time (time taken to traverse from 10% to 90% of the transient) are equal for a load capacitance of 100 fF.
   (Hint: Adjust the width of the PMOS to get equal rise and fall times. Use .measure command fast and accurate measure. Use input pulse with 10 ps rise/fall and run transient with a resolution of few ps)
   (Practise problem; Not mandatory to submit)

3. Consider a CMOS inverter with size $'W'$, which has the following parameters : $L = 0.18\mu m$, $W_n = W = 1.8\mu m$ and $W_p = 2.5 \times W$.

   (a) Using NGSPICE, plot VTC of inverter-1 (I_1) for the case when the inverter is driving a same sized inverter (I_2) as shown in Fig. 1.

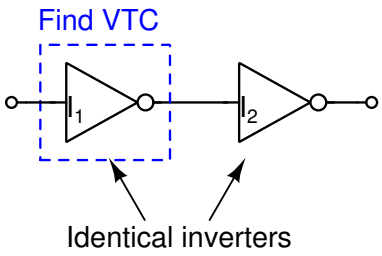

Figure 1

   (b) From the VTC plot in (a) find the noise margin parameters ($V_{IH}, V_{IL}, V_{OH}, V_{OL}$) and calculate NM_H and NM_L. Compare the noise-margins obtained from simulation with the theoretical formula derived in class for which you can use V_T values that you extracted in assignment-1.

   (c) Draw layout for case (a), extract the netlist and run post layout simulation to plot VTC of I_1 and find its NM_H and NM_L by clearly showing all noise-margin parameters on the plot. Tabulate theoretical, pre-layout and post-layout noise-margins for I_1. Do you observe any difference (pre-layout vs post-layout)? Comment.

4. A typical CMOS inverter is considered to drive 4 similar inverters or having a fan-out of 4 (FO4 inverter). We want to characterize the delay of FO4 inverter, for which input and output waveforms should also be typical in nature. Consider the figure 2, where an inverter with size $'W'$ has following parameters : $L = 0.18\mu m$, $W_n = W = 1.8\mu m$ and $W_p = 2.5 \times W_n$. Write a net-list for the given configuration and apply a piece wise linear input at node 'A' as follows : *V_{in} vin A 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V).*

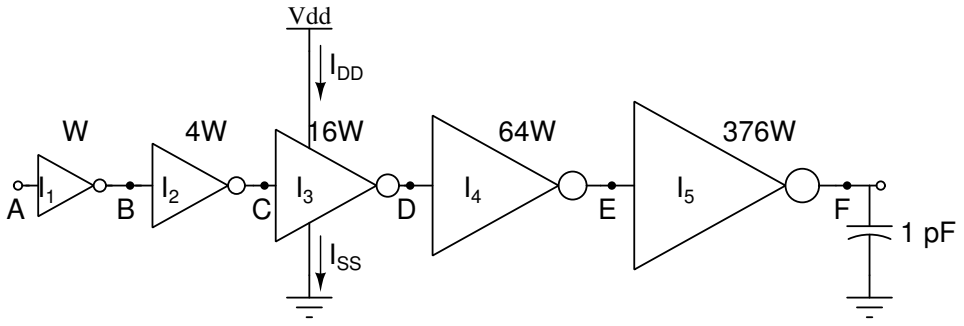

Figure 2

(a) Calculate $K_p\tau_{rise}/C_L$ and $K_n\tau_{fall}/C_L$ using τ_{rise}, τ_{fall} expressions and the required values from the results obtained in problem 3(d), where $K = \mu C_{ox}\frac{W}{L}$.

(b) Run transient simulation for 5 ns in step size of 10 ps for the given circuit and plot the signals at node 'C' and 'D' in the same graph. From the graphs, find the values of τ_{rise} and τ_{fall} at both the nodes C and D (You may consider 10% to 90% of the transient for finding rise/fall times. Use .measure for accuracy). Are they same? Comment.

(c) Use .MEASURE command in NGSPICE and tabulate the propagation delays (input to output) of inverters I_3 and I_4. Are they same? Discuss.

(d) Plot the supply current I_{DD} as shown in the figure and explain the plot obtained.

(e) Plot the ground current I_{SS} as shown in the figure and explain the plot obtained.

5. For the delay characterization of the inverter used in Problem 3(a), plot inverter delay with respect to $\frac{C_{load}}{C_{in}}$, where C_{load} is the load capacitance it drives and C_{in} is the input capacitance it presents to the gate that is driving it. Verify that the delay is of the form $gh + \rho$. From the graph, find absolute parasitic delay ($\rho\tau$) and delay unit τ for the inverter. Clearly explain the test circuit for this characterization. For varying the C_{load}, use another inverter and vary its size. Use .MEASURE command to get the delay.

6. Design a 31 stage ring oscillator (RO) using $L = 2\lambda$, $W_n = 10\lambda$ and $W_p = 25\lambda$, where $\lambda = 0.09\mu m$.

   (a) Write NGSPICE netlist for the RO and find frequency (f_{RO}) of oscillation and delay (τ_D) of a single inverter from simulation results. Do the values obtained from simulation results satisfy $f_{RO} = \frac{1}{62\tau_D}$, comment.

   (b) Draw an optimized layout for the 31 stage RO using MAGIC layout editor.
   (Hint: Some useful magic commands- :getcell inverter-layout-name, :array <columns> <rows>, :upsidedown)

   (c) Extract the netlist of the RO from the layout with parasitics and use NGSPICE to find f_{RO} and τ_D

   (d) Compare the pre-layout and post-layout simulation results and comment on the difference (if any).
