

# Intro to VLSI and Embedded Systems

5/1/26 : Aftab Hussain

→ Grading Structure :-

Class Participation - 10 %

Assignment - 20 %

Quiz 1 - 25 %

Final Sem - 45 %

→ Transistor :-

- Invented in 1947, at AT&T's Bell Labs, as a replacement for vacuum tubes. ( John Bardeen and Walter Brattain with William Shockley )
- Fairchild Semiconductors then made the IC, with Shockley. One of the inventors was Gordon Moore, who created Moore's Law.

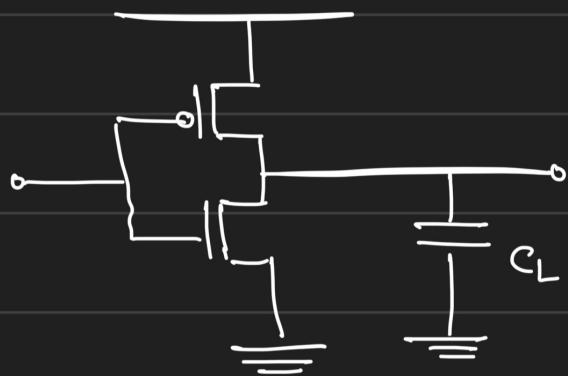
→ Silicon :-

- Second Most Common Element by weight. 28.2% of Earth's crust

- Can form both n-type and p-type semiconductors.
- Has near-perfect crystal lattice structure.
- Manufactured from sand ( $\text{SiO}_2$ ). 98% pure silicon is metallurgical grade, which is not pure enough. Semiconductor grade silicon is 9N or 10N pure (99.99999999%), which is the purest element created by humans.
- To make the silicon monocrystalline we use the Czochralski process, where the material is melted and allowed to recrystallize slowly.

→ Dimensional Scaling :-

- Propagation Delay, the time taken to receive the output signal.



Hence,

$$\tau_d \propto C_L$$

$$\Rightarrow \tau_d \propto WL C_{ox}$$

- Also, the total energy consumed in one switching is  $C V_{dd}^2$

$$\Rightarrow P = \frac{C V_{dd}^2}{\tau_d}$$

- Dimensional Scaling is the shrinking of all the components of the MOSFET by the same factor. On scaling by 3,

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \longrightarrow \frac{\epsilon_{ox}}{t_{ox}/3} = C_{ox} \cdot 3$$

$$I_{on} = g_m C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \longrightarrow I_{on} \cdot 3$$

$$C = WL C_{ox} \longrightarrow C/3$$

$$\tau_d = \frac{C V_{dd}}{2 I_{on}} \longrightarrow \tau_d/3^2$$

$$P = \frac{C V_{dd}^2}{\tau_d} \longrightarrow P/3$$

$$P/A \text{ (density)} \longrightarrow \frac{P \cdot s}{A/3^2} \longrightarrow P/A \cdot s^3$$

We can see that such a dimensional scaling increases the power density by a cubic factor.

- To combat this, we reduce the operating voltage also by a factor of 8.

Device or Circuit Parameter	Scaling Factor
Device dimension $t_{ox}, L, W$	$1/\kappa$
Doping concentration $N_a$	$\kappa$
Voltage $V$	$1/\kappa$
Current $I$	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit $VC/I$	$1/\kappa$
Power dissipation/circuit $VI$	$1/\kappa^2$
Power density $VI/A$	1

This is termed as Renard scaling, and is a more strict version of Moore's law.

- Renard scaling has also died out, due to the prevalence of short channel effects at lower length scales.

- Due to the death of Moore's Law and Demand Scaling , optimization of electronics are moving towards the application side.

9/1/26 : Zia Abbas

- The Electronic revolution started with the triode (1906), with the usage of transconductance. ( voltage / current controlled resistance )  
It enabled storage, processing and communication of information
  - Initial founders were Vacuum Tubes . ENIAC was the first computer , made using vacuum tubes. However it was expensive , energy intensive and the vacuum tubes were unreliable .
  - The transistor was invented in 1948. It was smaller and could perform the same functionality as the vacuum tube .
  - The integrated circuit was first created by Jack Kilby and Moyer in 1958 , earning them a Nobel prize .
- Monolithic Integration - All the transistors are fabricated on the same semiconductor substrate piece .

- Through monolithic packaging, the size of integrated circuits can be reduced by a lot, to cover the micron scale from each block.

## IC Economics :-

$$\text{IC Cost} = C = \frac{C_{\text{dev}}}{N} + C_{\text{prod}} \rightarrow \begin{array}{l} \xrightarrow{\text{Development Cost}} \text{Designs, RnD} \\ (\text{one-time}) \end{array}$$

$$C_{\text{prod}} \rightarrow \text{Manufacturing Cost} \\ (\text{Recurring})$$

$$C_{\text{prod}} = C_{\text{die}} + C_{\text{pack}} + C_{\text{test}}$$

↗ chip    ↗ packaging    ↗ testing

$$C_{\text{die}} \approx \frac{C_{\text{wafer}} / Y_{\text{wafer}}}{(0.85 A_w / A_{\text{IC}}) Y_{\text{die}}} \rightarrow \begin{array}{l} \xrightarrow{\text{wafer cost}} \text{wafer cost} \\ \xrightarrow{\text{wafer yield}} \text{wafer yield} \\ \downarrow \qquad \qquad \qquad \rightarrow \begin{array}{l} \text{die yield} \\ \text{wafer area} \qquad \qquad \qquad \text{IC area} \end{array} \end{array}$$

$$C_{\text{die}} \propto A_{\text{IC}}^4 \quad (\text{yield is also affected by area})$$

13/1/26 : Abhishek Srivastava

## \* Analog, RF and Mixed Signal Verticals :-

Semiconductor Tech  $\rightarrow$  (VLSI + Embedded)  $\rightarrow$  Products

→ Verticals :-

- Device / Technology Vertical :-

Foundry, Tech. Node, PDK, Device Models,

Yield & Reliability.

- Scaling down of devices - Better processors. (5nm, 3nm, N9, AI, etc)
- PDK : Generate device models to be used for simulations. Gives data about data physics.

- Logic / Digital Vertical :-

Processor design, video/image codex, Memory

controllers, RTL, function verification, SoC integration, Clocking.

- RTL : Verilog for circuit abstraction.

- Analog and Mixed Signal (AMS), RF Vertical :-

Clock Generation, Antenna,

Receiver, high-Speed interfaces, ADC/PAC, Power Design, 5G/Wi-Fi,

- Physical Design :-

Layouts → (Floor Plan, Stick Diagram, etc), Post-Layout Testing / Verification, Placement and Routing, Timing analysis, Power.

- Memory / Storage Vertical :-

SRAM, DRAM Cells, NAND Flash, Controller, HDD, SSDs.

- Packaging Vertical :-

Chip stacking, flip chip packaging, thermal dissipation, 2.5D / 3D stacking.

- EDA Verticals :-

Tools used in simulation for any design stage (Cadence, Synopsys, Ansys, Siemens)

- Works with application engineers, who represent the manufacturer and give device related insight to the developers.

- Validation / Test Vertical :-

Post-Silicon Testing, power / thermal debug, protocols, yield analysis. (Need: Scripting tools)

- AI / Neuro-morphic VLSI Vertical :-

AI acceleration, In Memory Compute

Neuro-morphic design. (Applied side of VLSI)

- Embedded Software (Firmware / RTOS) :-

Control of the different components

- side of an embedded device.

- Embedded Hardware :

Microcontroller design, SoC design, PCB design,

Power electronics integration.

- IoT / Edge :

Sensor Integration, Edge Computing (AI)

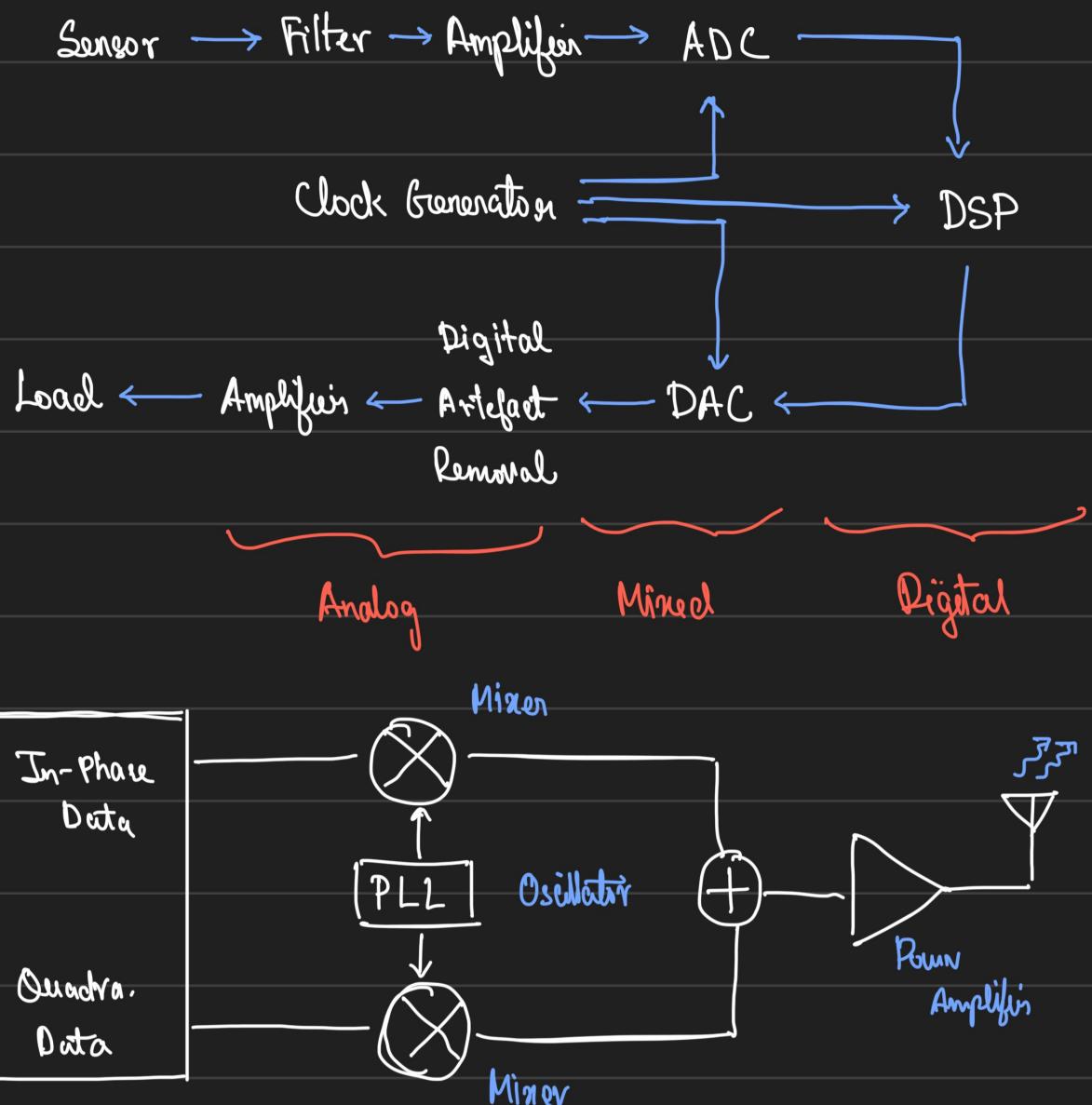
- Hardware / Software Co-Design :

Hardware - Aware performance tuning,

FPGA, etc.

→ Analog, Mixed Signal and RF :-

- Most Natural Signals are Analog. The front end of any device is an Analog circuit.



An RF Circuit

- But analog signals cannot be easily processed upm. They cannot be stored effectively.

- DSPs are repeatable and have high SNRs.
- Digital Enhances, Analog Refines.
- AMS / RF ICs :-  
Sensors, Battery Management, Clocking, RF antennae / transmitter, Power circuits, ADC / DAC, Amplifiers, Filters, Comparators, Energy-Harvesting circuits, Motor Control Devices, High-Speed interfaces, Precision-Timing circuits.

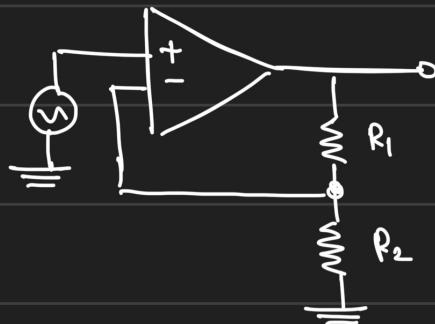
- Low Power Amplifiers - Operate in Subthreshold regime, High Gain (exponential) but low absolute voltage values.

- Analog IC Design :-

- Hard to automate - Device physics strongly affect the results
- Hard to replace.
- Hard to outsource.
- High in Demand

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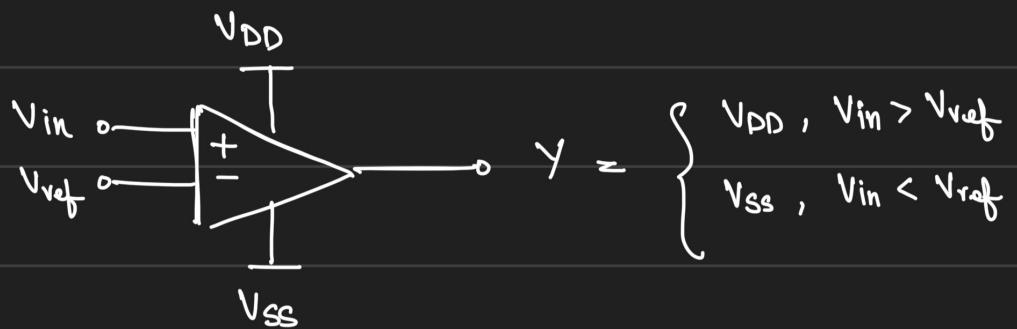
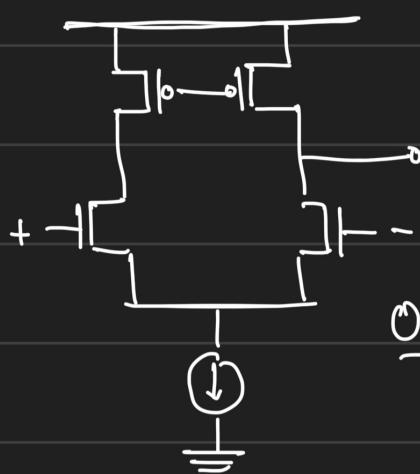
Abhishek Srivastava



Inverter (Digital)

Non Inverting Amplifier (Analog)

OpAmp:

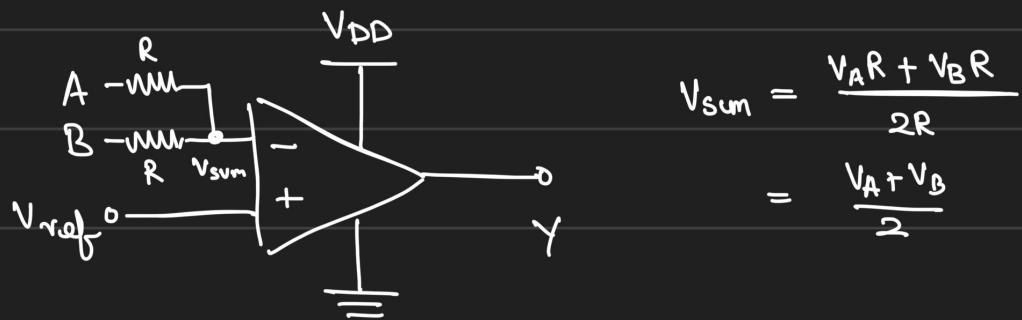


Op-Amp as a Comparator (Mixed Signal)

Can also be used as an inverter by

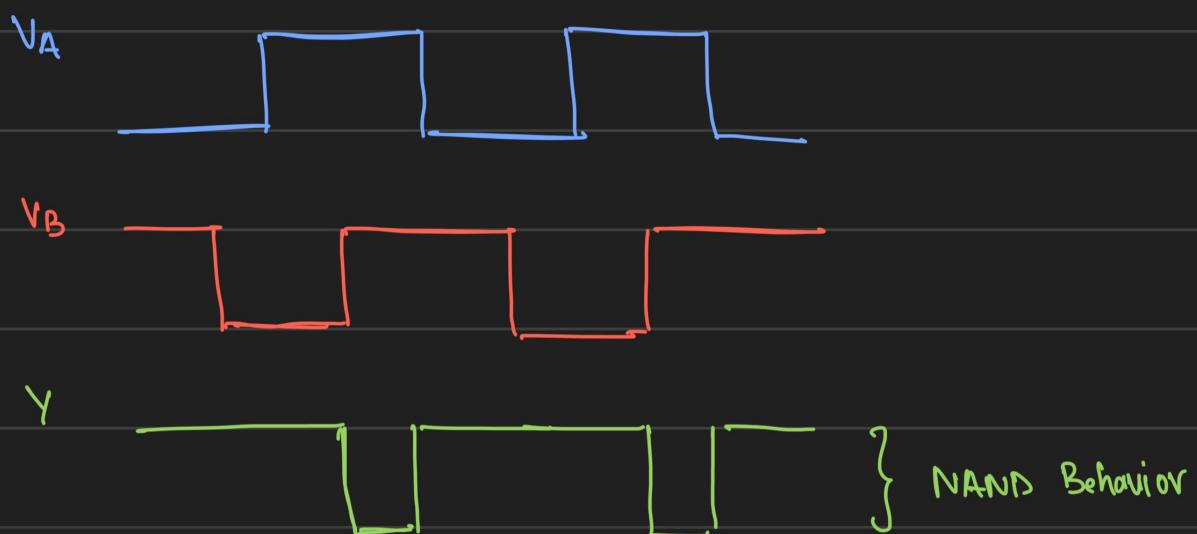
setting  $V_- = V_{in}$  and  $V_+ = \frac{V_{DD}}{2}$ ,  $V_{ss} = 0$ .

- If we use the Op-Amp as an inverter, it will occupy a higher area and draw more power (static power) than the MOS inverter.

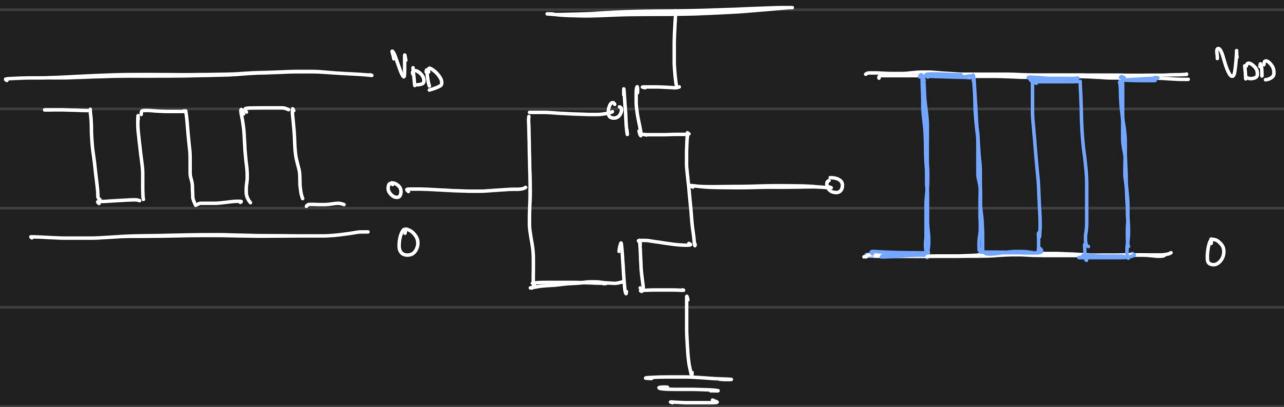


$$Y = \begin{cases} V_{DD}, & V_{\text{sum}} < V_{\text{ref}} \\ 0, & V_{\text{sum}} > V_{\text{ref}} \end{cases}$$

Say  $V_{\text{ref}} = 3.5 \text{ V}$ ,  $V_{DD} = 5 \text{ V}$

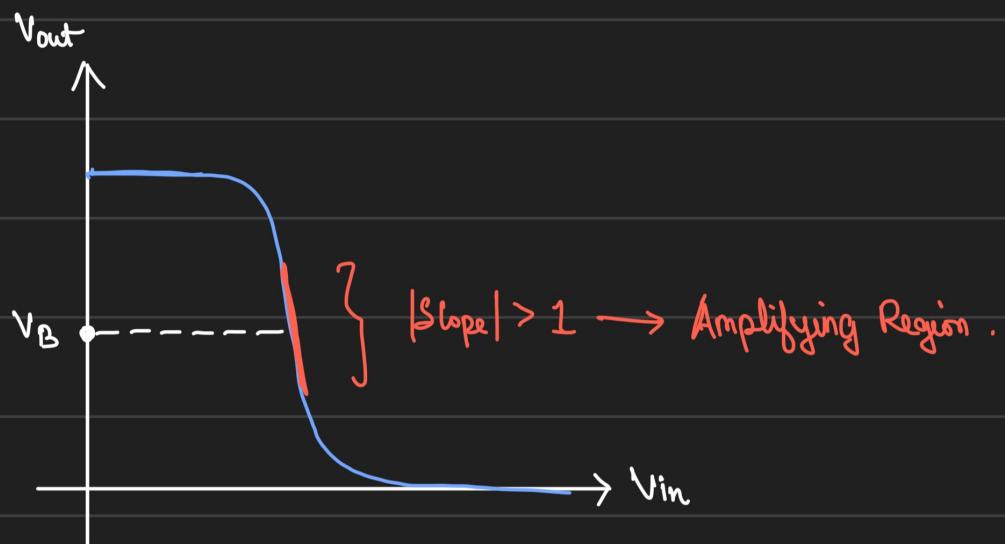


- In this configuration, the Op-Amp can be used as a digital device, namely a NAND gate.

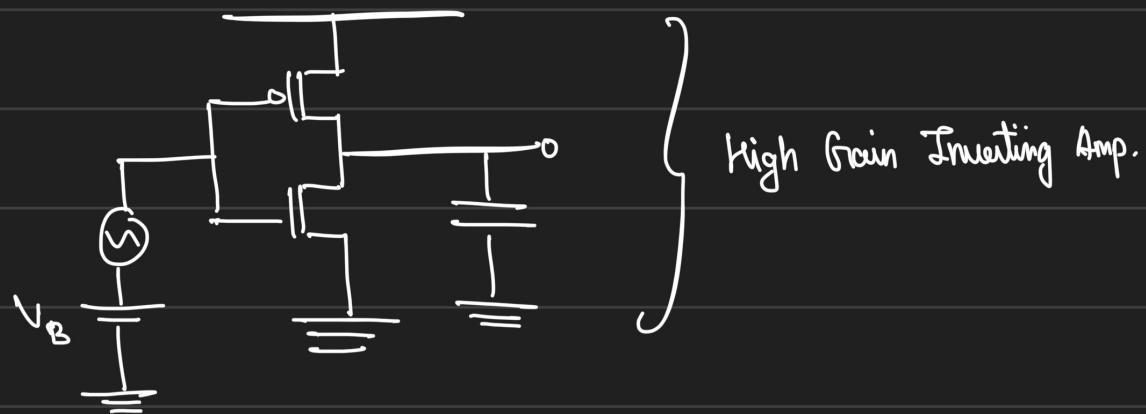


- If the inverter input is not rail to rail, there is some gain within the device that pulls the output to the rail.

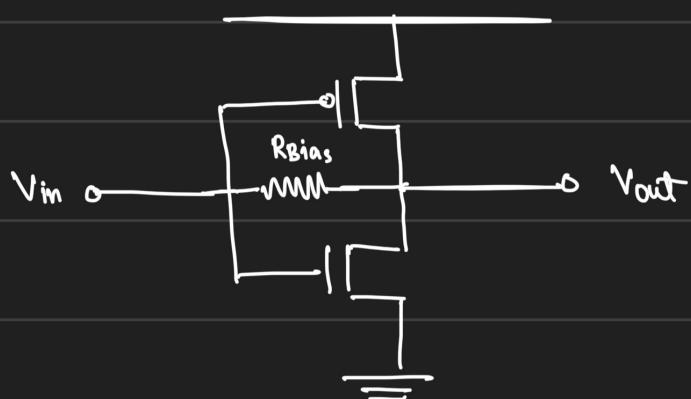
$$A_v = \frac{V_{OH} - V_{OL}}{V_{IL} - V_{IH}}$$



- At the amplifying region, the inverter will act like an analog amplifier.



° To get a proper biasing,



If  $R_{Bias}$  is very high, then the bias point of the circuit will be at  $V_m$  (switching point)

° Op-Amp Low Frequency Gain :-

- Since Op-Amp based amplifiers are high gain amps, these amplifiers can also amplify the low frequency noise present in the environment, namely the 50Hz noise.

- Op-Amp devices will also have some DC offset when the inputs are equal, due to non-idealities within the device.
- These are well known problems and affect low frequency applications, like biomedical signals.
- Low frequency gain is also termed as DC gain, due to its difference from small signal assumptions (ex: Capacitive cutoff frequencies)
- Since low pass filters cannot be used in low frequency applications (cutoff is too close to desired freq), we upconvert the signal to a higher frequency, apply the LPF and then downconvert it back to the target frequency.

This method is termed as the Chopper method, and is very common in low frequency applications.

20/1/26 - Priyesh Shukla

## \* VLSI Systems :-

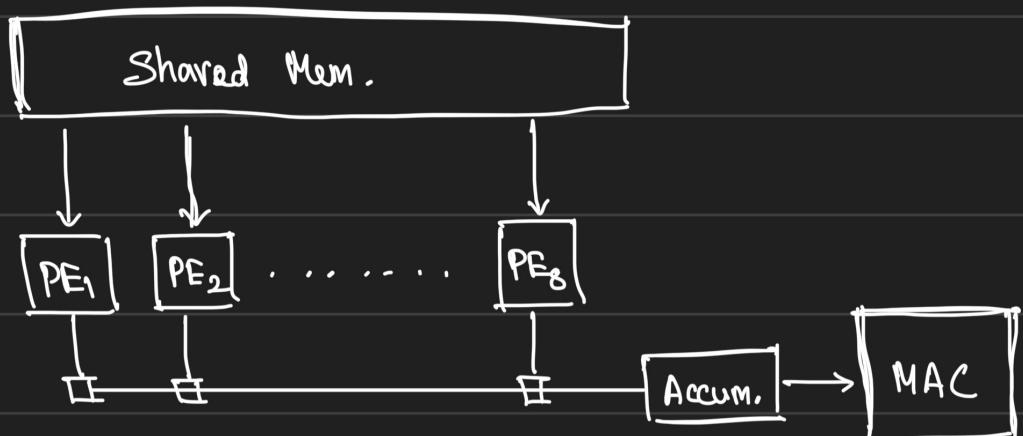
- ° Biomedical signals are of a large variety and in a hospital environment we may need to monitor multiple such signals simultaneously. ex: ECG, SpO<sub>2</sub>, Sbp, Pulse.
- ° These signals are continuous in nature and are sampled and stored as time-series data. We may also store information as text, image or audio.
- ° So, the whole device used to record the signals must be multi-modal, i.e., can process multiple modes of information (text, time-series, image, audio).
- ° The system must also be robust since it's dealing with a lot of vital signal.

23/1/26 Priyesh Shukla

- ° Say we want to evaluate the Gaussian function for a series of n values.

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)$$

- We can evaluate this using approximation algorithms like Taylor series for example.
- This task is of the complexity  $O(n)$ , when done in a conventional manner.
- But, say I have 8 different processing units (PE)



This arrangement reduces the complexity to  $O(\frac{n}{8} + 1)$ . (+1 due to accumulator.

This is a type of hardware acceleration, using of physical unit and circuit structure to reduce the time taken for an operation.

- ° Another type of hardware acceleration is In-Memory Computing, which moves the bulk (or all) of the computation to the memory devices.  
It is a domain-specific type of acceleration.
- ° Hardware acceleration comes under the domain of system design, involving compilers, operating systems, microarchitecture.