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For a full adder with inputs 'a' and 'b' and carry-in as 'cin', The output sum $= a \oplus b \oplus cin$

output carry $(C_{out}) = a \cdot b + (b + a) cin$

- carry is generated (g) when $a = b = 1$
- carry is propagated (p) when $a + b = 1$

$$\Rightarrow C_{out} = g + p\, cin \; ; \quad g = a \cdot b \quad -(1)$$
$$p = a \oplus b \quad -(2)$$

For n-bit adder with LSB indexed as 0 and MSB as n-1

i^{th} bit accepts C_i as i/p carry and produces C_{i+1} as o/p carry

We can express the o/p of i^{th} stage as.

$$C_{i+1} = G_i^1 + P_i^1 \cdot C_i$$

$$C_{i+1} = G_i^1 + P_i^1 \cdot (G_{i-1}^1 + P_{i-1}^1 \cdot C_{i-1})$$

$$= G_i^1 + P_i^1 \cdot G_{i-1}^1 + P_i^1 \cdot P_{i-1}^1 \cdot C_{i-1}$$

let $G_{i,i-1}^2 = G_i^1 + P_i^1 G_{i-1}^1$, $P_{i,i-1}^2 = P_i^1 P_{i-1}^1$

$$\Rightarrow C_{i+1} = G_{i,i-1}^2 + P_{i,i-1}^2 \cdot C_{i-1}$$

Similarly assuming $G_{i,i-3}^3 = G_{i,i-1}^2 + P_{i,i-1}^2 \cdot G_{i-2,i-3}^2$

$$P_{i,i-3}^3 = P_{i,i-1}^2 \cdot P_{i-2,i-3}^2$$

$\Rightarrow c_{i+1} = G^3_{i,i-3} + P^3_{i,i-3} c_{i-3}$.

→ assuming unit delay for each computation

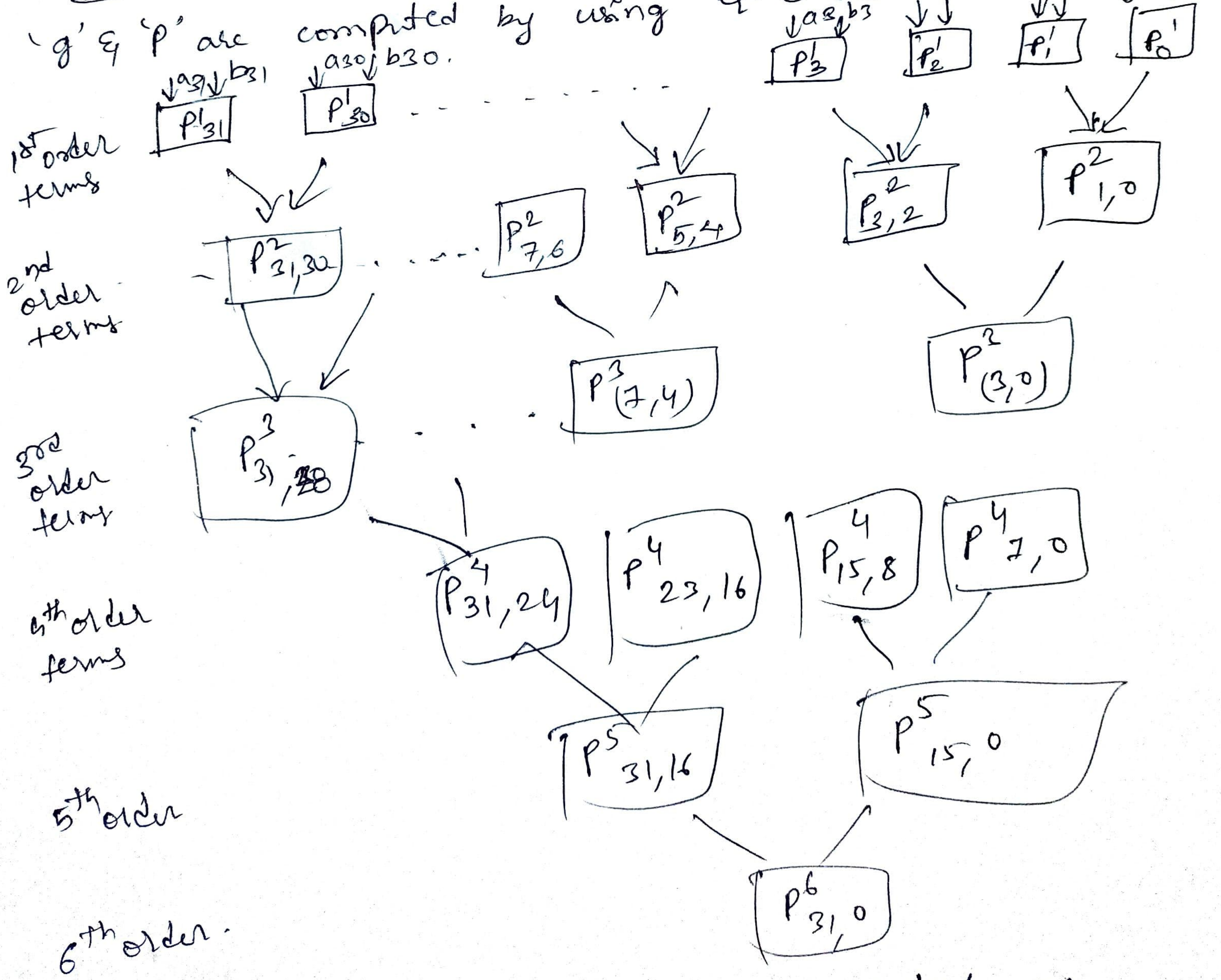
computation of G^1_i, ~~takes~~, $G^2_{i,i+1}$, $G^3_{i,i-3}$ takes 1, 2 & 3 unit delays.

Thus computing of final carry ~~out~~ of 'n' bit adder takes 'log n' as delay.

We can calculate sum of each stage as $S_i = a_i \oplus b_i \oplus c_i$
$= P_i \oplus c_i$

Example of a 32-bit Brent Kung adder

'g' & 'p' are computed by using eq-(1) & (2)



The carry of each stage is computed as

$C_1 = G_0^1 + P_0^1 C_0$, $C_2 = G_{1,0}^2 + P_{1,0}^2 C_0$

$C_4 = G_{3,0}^3 + P_{3,0}^3 C_0$, $C_8 = G_{7,0}^4 + P_{7,0}^4 C_0$ etc.

References:- Prof. Dinesh Sharama Lectures – IIT Bombay