Sridhar Gopinath

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Research interests

My interests are in programming languages and systems research to improve performance and reliability of products with real-world impact.

Education

University of Texas at Austin *Aug. 2019 - present*
Ph.D. in Computer Science *Austin, TX, USA*
Advisor: Prof. Isil Dillig

Indian Institute of Science (IISc) *Aug. 2015 - May 2017*
Master by Research in Computer Science ***GPA:*** **7.0 / 8.0** *Bangalore, India*
***Thesis**: Efficient Whole program path tracing* [1] ***Advisor**: Dr. Murali Krishna Ramanathan*
Courses: Advanced Software Engineering | Program Analysis and Verification | Operating Systems | Design and Analysis of Algorithms

Sri Jayachamarajendra College of Engineering (SJCE) *Sep. 2011 - May 2015*
Bachelor in Computer Science ***GPA:*** **9.0 / 10.0** *Mysore, India*
***Thesis**: Loop Fusion in LLVM compiler* [2] ***Advisor**: Prashantha Naduthota*

Publications & Manuscripts

Compiling KB-Sized Machine Learning Models to Constrained Hardware [3] *Jun. 2019*
***Sridhar Gopinath**, Nikhil Ghanathe, Vivek Seshadri, Rahul Sharma*
PLDI 2019 | ACM SIGPLAN Conference on Programming Language Design and Implementation

Technical report: Efficient Whole Program Path Tracing [4] *Apr. 2017*
***Sridhar Gopinath**, Murali Krishna Ramanathan, Suresh Jagannathan*
Based on Master's thesis at Indian Institute of Science

Research experience

Graduate Research student at UT Austin *Aug. 2019 - present*
***Project:** Verifying quantization of Machine Learning models (on-going)* *Austin, TX*
***Advisors:** Prof. Isil Dillig & Dr. Rahul Sharma*

- Developing a verification framework to evaluate the effectiveness of a quantization technique.
- The framework will be the first to enable direct comparisons between different quantization techniques.
- For a given user requirement, the framework can choose (with guarantees) a quantization technique that best matches the requirements.

Research Fellow at Microsoft Research *Oct. 2017 - Jul. 2019*
***Project:** Compiling KB-Sized Machine Learning Models to Constrained Hardware* *Bangalore, India*
***Advisor:** Dr. Rahul Sharma*

- Developed a programming language (SeeDot) to compile ML models to C code to run on KB-sized devices without floating-point support.
- Implemented novel compilation strategies to replace floating-point operations with integers and to optimize expensive functions (like e^x).
- SeeDot outperforms hand-optimized code by up to 12× and MATLAB-generated code by up to 82×, on microcontrollers.
- SeeDot improves FPGA programmability by generating Verilog code that outperforms Xilinx High-Level Synthesis tool by 10×.

Research Intern at Microsoft Research *Jun. 2017 - Sep. 2017*
***Project:** Detecting IRQL violations in Windows Device Drivers* *Bangalore, India*
***Advisor:** Dr. Akash Lal*

- Implemented a property checker to detect Interrupt Request Level (IRQL) violations, which is a major cause for crashes in Windows.
- The property checker generates preconditions that are used by the Z3 theorem prover to identify the defects.
- Found **26 unknown defects** in Windows 10 which have been verified by developers.
- Tool currently deployed in Windows Driver Kit (WDK) and used internally in Microsoft for testing.

Graduate Research Student at Indian Institute of Science

Aug. 2015 - May 2017

Project: *Efficient Whole Program Path Tracing* — *Bangalore, India*

Advisors: *Dr. Murali Krishna Ramanathan & Prof. Suresh Jagannathan (Purdue University, USA)*

- Designed a program analysis to minimize the overhead to derive the control-flow trace (whole program path) of an execution.
- Using control-flow graph properties, proved that this problem is a variant of the hitting-set problem, which is NP-hard.
- Designed and implemented efficient data structures and approximation algorithms to scale the analysis for large Java programs.
- Evaluated on the DaCapo benchmark suite and observed performance improvements of up to 5.4× compared to the state-of-the-art.

Research Intern at Compiler Tree Technologies

Jan. 2015 - May 2015

Project: *Loop Fusion in LLVM Compiler* — *Mysore, India*

Advisor: *Prashantha Naduthota*

- Designed a function pass which fuses loops to leverage the data stored in cache.
- Performed feasibility and data dependency analysis to identify loops for fusion.
- Verified the correctness of fusion and observed around 20% performance improvement at run-time.

Teaching

Graduate Teaching Assistant

Aug. 2019 - present

CS 380C: Advanced Topics in Compilers | ***Instructor:*** *Prof. Keshav Pingali* — *UT Austin*

Graduate Teaching Assistant

Aug. 2016 - Dec. 2016

E0210: Principles of Programming | ***Instructor:*** *Dr. Murali Krishna Ramanathan* — *IISc, Bangalore*

Organizer & tutor

Aug. 2014 - Dec. 2014

Advanced C workshop | *Linux Campus Club, SJCE* — *Mysore, India*

Presentation

Compiling KB-Sized Machine Learning Models to Constrained Hardware

Mar. 2019

Poster Presentation | *Presenting at Microsoft Research TechFest 2019* — *Redmond, USA*

Efficient Whole Program Path Tracing

Apr. 2017

Poster Presentation | *Division of Electrical, Electronics, and Computer Science (EECS) Symposium 2017* — *Indian Institute of Science, India*

Achievements

- ***All India Rank* 32** | Asia Amritapuri Site Regional Contest | **ACM ICPC - 2016**
- ***All India Rank* 527** | 99.544 percentile | **GATE - 2015**
- **1st place:**
  - *Bugsy contest, Technologix '14* | Computer Society of India | SJCE, Mysuru
  - *C-Fi contest, 8th Mile '14* | Vritanth | RVCE, Bengaluru
  - *C Night-out contest, Cyberia '14* | IEEE Student Branch | SJCE, Mysuru
  - *C Coding Contest, FOSS Camp '13* | Linux Campus Club | SJCE, Mysuru
- *Top* 50, Machine Learning contest | *National Technical Challenge '13* | IBM

Other relevant projects

Null pointer dereference analysis

Nov. 2015

Language/Tools: Java, WALA — *Indian Institute of Science, India*

- Implemented the iterative approach of inter-procedural data-flow analysis by Sharir-Pnueli (1981).
- Analyzes a given Java program and reports the objects or field references which *maybe* null.

PintOS Projects

Nov. 2015

Language/Tools: C, Qemu, GDB — *Indian Institute of Science, India*

- Designed and implemented the following key functionalities on top of base OS.
- Threads: Priority scheduling, priority donation, mlfqs scheduling.
- User programs: Execution of multi-threaded user programs, system calls for accessing file system.
- Virtual memory: Demand paging, stack growth, swapping, memory-mapped files.
- File systems: Indexed and extensible files, sub-directories, caching file blocks.

SJCEResults.com

Jan. 2015

Platform/Tools: AWS, EC2, Route 53, Amazon SES, LAMP

- Website provides deep analysis about the examination data of 6000 students over 3 academic years.
- Implemented name-wise search and multi-level rankings for each student.
- Provides performance analysis of students in each course and the performance of each department.
- Website currently has more than **2 Million** page views.

Extracurricular

Workshops & Events

- Collaborator, *Workshop on Machine Learning on Constrained Hardware* by Microsoft Research, India.
- Participant, *The First Indian SAT+SMT School* by TIFR, Mumbai.
- Volunteer, *Undergraduate Summer School on Computer Science - 2016* by CSA, IISc, Bangalore.
- Technical Organizer, *FOSS Camp '15*, for 500 students by LCC, SJCE, Mysore.

Committees

- Member | *Web System Admin team* | Department of Computer Science, IISc, Bangalore.
- Executive member, *2014 - 2015* | Linux Campus Club (LCC) | SJCE, Mysore

References

[1] Bachelor's thesis http://bit.ly/2DY8NOq

[2] Master's thesis http://bit.ly/2Si0NM8

[3] Tech report: Compiling KB-Sized Machine Learning Models to Constrained Hardware http://bit.ly/2AFyiAR

[4] Tech report: Efficient Whole Program Path Tracing http://bit.ly/2KPeBLW