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Parallel and Concurrent Programming
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PROGRAMMING ASSIGNMENT - III

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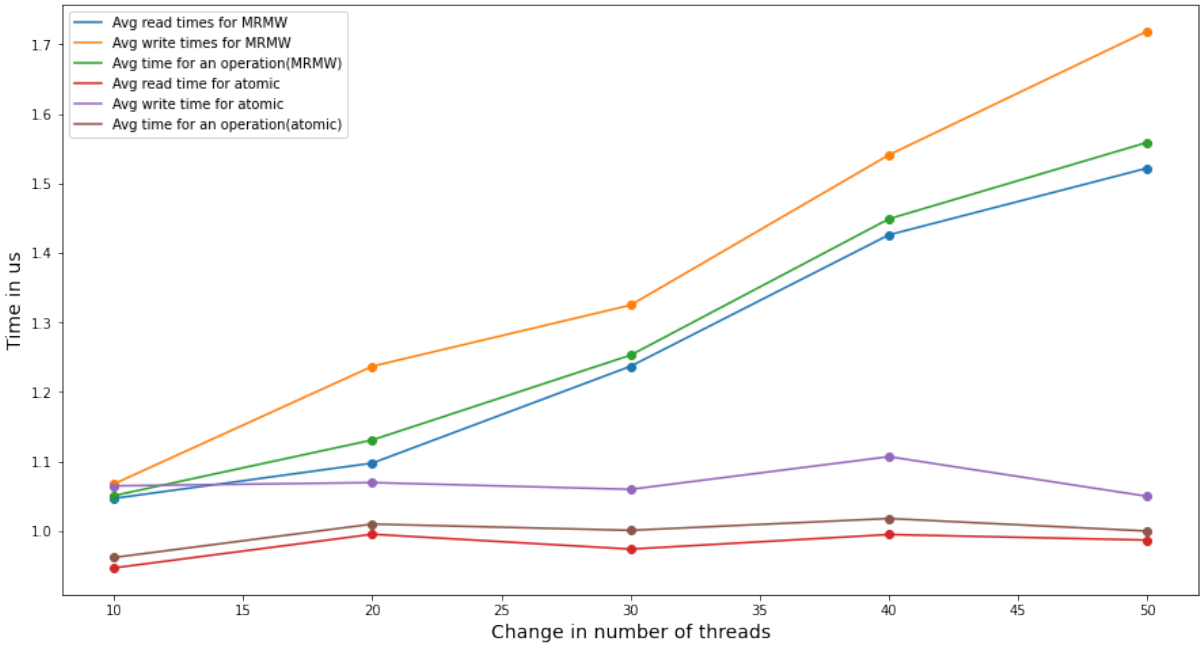
Base:

The application was designed exactly as described in the programming assignment problem statement and used text book for the reference. I implemented a m valued MRMW atomic registers from a regular m valued SRSW register using `C++`.

Graph & Observations:

Graph: Variation in average time vs Variation in number of threads(for both registers)



Every observation is the average of 5 recorded observations to remove any discrepancies in the measuring of time. The number of threads are varied from 10 to 50 while keeping repetition count as constant and set to 100 while the read probability is set to 0.8 and the lambda is set to 5.

Observations:

- The graphs were plotted by recording times for average read, write and for an average operation for both developed MRMW register and inbuilt atomic register.
- One can see that the inbuilt atomic registers are performing equally well in overall cases while the threads are varying from 10 to 50.
- This is as expected because the load equally balances and the inbuilt atomic register is well developed.
- But the curves are increasing at a very slow rate while threads are even increased for threads of size 70 and more(but not as much as that of developed m valued MRMW register)
- On the other hand, the developed MRMW register is taking more time than that of the inbuilt atomic register.
- But the time gap is not very large and could be used for small scale applications where the inbuilt atomic registers are not available.
- The time taken for writing is always greater than that of the reading from the shared variable in both developed register and inbuilt register which suggests that the developed register comes in par with the atomic operations.
- The time taken for write operation is some what higher than that of reading because of the complexity in the function.
- One can observe that the graphs are suggesting that the loads are almost equal when threads are less.
- With the trend observed, our MRMW register can outperform for fewer number of threads.

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THE END