

# IC fabrication & VLSI -

IC - Integrated Circuit

- Mr. Neeraj Tripathi

whole system is developed on same base.

→ Material used [ i.e. Material pt. of view ]

Mobility is a property of semiconductor

$v \propto E$

(Velocity  $\propto$  Electric field)

$$v = uE$$

Applied

$$u_n = 0.39 \text{ m}^2/\text{Vs}$$

$$u_h = 0.2 \text{ m}^2/\text{Vs}$$

Mobility of holes  $<$  Mobility of electrons  
(Laptops)

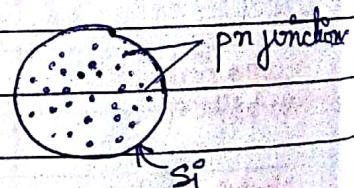
Q. We use compound semiconductors instead of elemental semiconductors

in IC-fabrication? Because electrons in compound semiconductors move faster than e<sup>-</sup> in Si, thus enabling high speed processing.

Two types of fabrication -

- 1) Mass
- 2) Batch

Properties of



## Silicon

## Germanium

Atomic weight

28.08

72.64

Intrinsic carrier conc.

$1 \times 10^{10} \text{ cm}^{-3}$

$2.4 \times 10^{15} \text{ cm}^{-3}$

e<sup>-</sup> Mobility

$\leq 1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

$\leq 3900 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

Hole Mobility

$\leq 450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

$\leq 1900 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

e<sup>-</sup> Diffusion coefficient

$\leq 3.6 \text{ cm}^2 \text{ s}^{-1}$

$\leq 100 \text{ cm}^2 \text{ s}^{-1}$

Hole Diffusion coefficient

$\leq 1.2 \text{ cm}^2 \text{ s}^{-1}$

$\leq 50 \text{ cm}^2 \text{ s}^{-1}$

Electrical Resistivity

$3-4 \mu \Omega \text{ cm} @ 0^\circ\text{C}$

$46.2 \text{ cm}$

Melting Pt.

$1414^\circ\text{C}$

$938.25^\circ\text{C}$

Density

$2.329 \text{ g cm}^{-3}$

$5.323 \text{ g cm}^{-3}$

Thermal conductivity

$1.3 \text{ W cm}^{-1} \text{ K}^{-1}$

$0.58 \text{ W cm}^{-1} \text{ K}^{-1}$

Level of Integration

Year

Density (No. of logic blocks)

Single Transistor	1958	<1
Unit logic	1960	1
→ small scale integration (SSI)	1964	2 - 20
Medium Scale Integration (MSI)	1967	20 - 200
Large scale integration (LSI)	1972	200 - 2000
Discrete Design → different components joined to func <sup>n</sup> accordingly IC " → all things on one substrate		
Rectification of Discrete Design - is possible But of IC Design is not.		
adv. & disadvantages of discrete & integrated -		
VSC	1978	2000 - 20,000
ULSI ultra large scale integration	1989	20,000 to -

Logic Block - contains 10-100 transistors, performs logical opera<sup>n</sup>,

VLSI - (2 million ) transistors

Singular Transistor	1938	< 1
One gate	1960	1
Multipunction	1962	2-4
MSI	1967	20-200
LSI	1972	200-2000
VLSI	1978	2K-20K
ULSI	1989	20K+

\* Moore's Law - Density will be doubled in 1 year or per year after some time complexity will be so large, so that it becomes major Drawback of VLSI Lab

Modified Moore's - Density would be doubled in 1.5 years i.e Large complexity doubles in 1.5 years Device reaches in a region

feature size → min. distance betn 2 points created on wafer

Min feature size  $\propto$  device to be accommodated Hence Density increased  
size manometer range

\* light doping, heavy doping, bulky

$10^{15}$  atoms/cm<sup>3</sup>  $10^{18}-10^{19}$  atom/cm<sup>3</sup>

$10^{12}$  atoms/cm<sup>3</sup>  
Initial doping

n-type is added to one side;

p-type already exists.

Hence a p-n junction is realized

(Basically process known as Diffusion).

Advantages of VLSI fabrication :-

① less Area per Volume : In a given volume, they will occupy less area;

② less power consumption : Since size is smaller, power consumption is less

(VLSI will consume less power)

③ less testing requirement : Since, its testing is done from the very At system level Beginning level, hence when the component

ready, less testing is required at the end

High Reliability :-

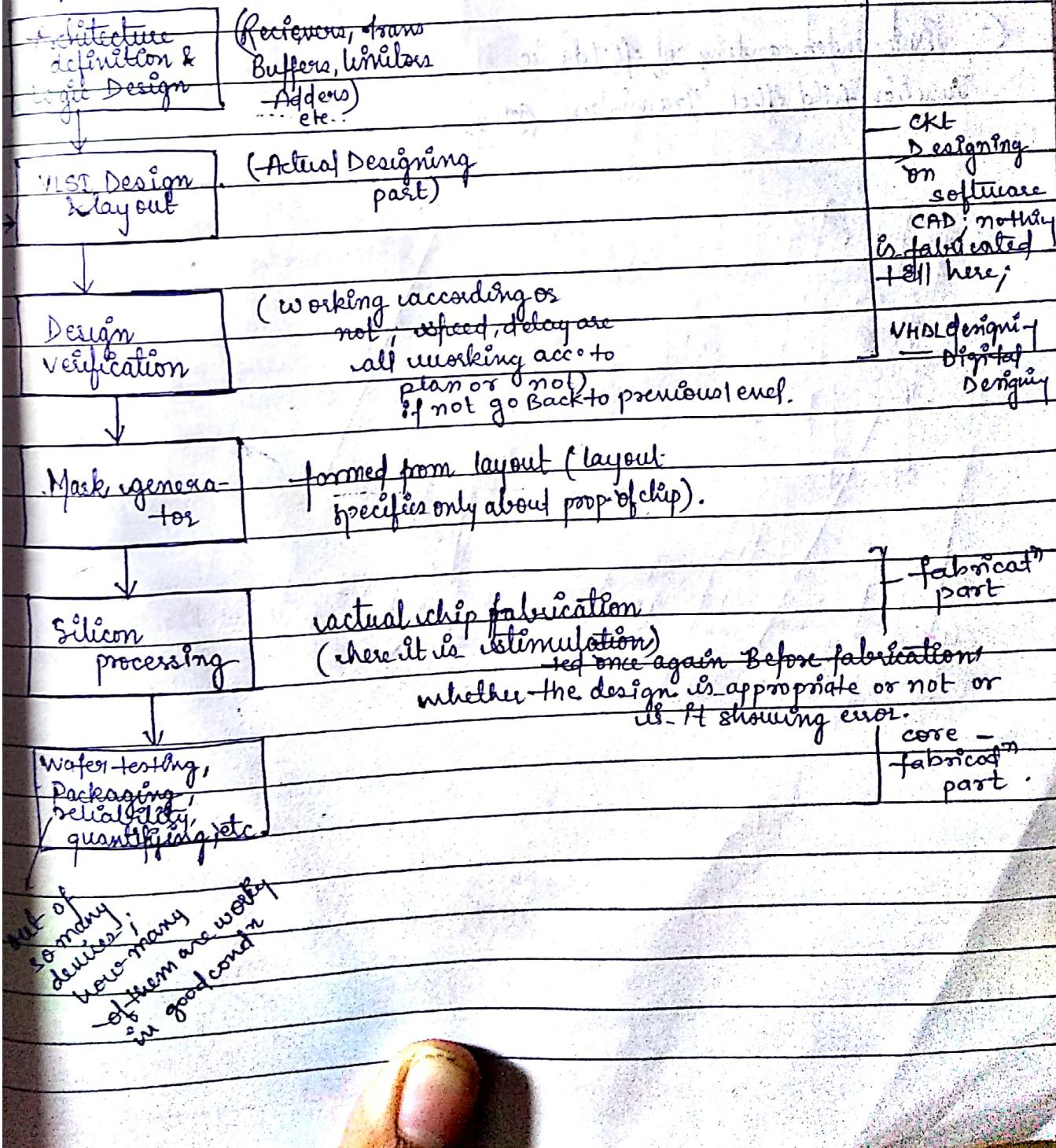
Higher speed :- These devices are very fast due to significantly reduced interconnect lines length. Less Delay Hence fast.

Significant Cost :- Since man fabrication comes into role; hence saving "fabricat" of per device is not needed which also accounts for higher cost.

## The flow of Circuit Design Procedures

our circuit designing is done) →

↓ System Requirements



Clean Room -

Official env. with low particle counts

Started in medical application for post surgery infection prevention.

Dust particles kills yield.

Adopted in semiconductor industry in 1950.

Smaller device needs higher grade clean rooms.

Lesser particles, more expensive to kill.

Clean Room Classes :-

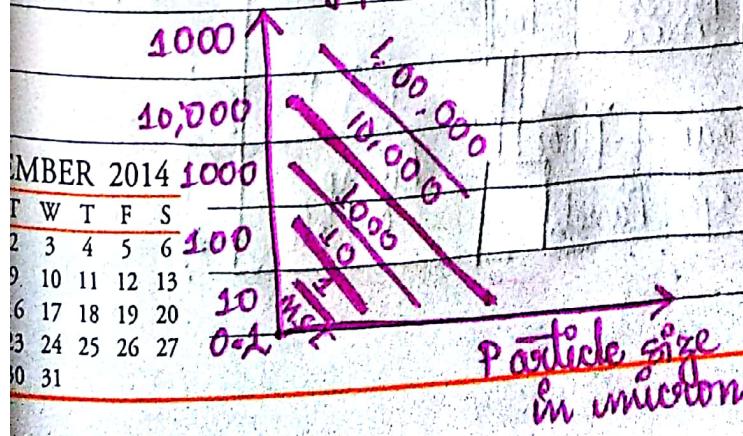
Class 10 is defined as less than 10 particles with diameter larger than  $0.5 \mu\text{m}$  / cubic foot.

Class 1 is defined as less than 1 such particles per cubic foot.

$0.18 \mu\text{m}$  device require higher than class 1 grade clean room.

	Particles / $\text{ft}^3$				
Class	$0.1 \mu\text{m}$	$0.2 \mu\text{m}$	$0.3 \mu\text{m}$	$0.5 \mu\text{m}$	$5 \mu\text{m}$
10,000	9.8	2.12	0.865	0.28	
1000	35	7.5	3	1	
100	350	75	30	10	
10	3500	750	300	100	
1	35000	7500	3000	1000	
				10,000	70

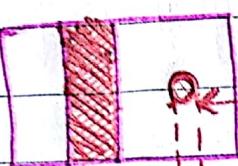
No of particles



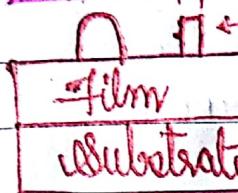
NUMBER 2014  
T W T F S  
2 3 4 5 6 100  
9 10 11 12 13 10  
6 17 18 19 20 10  
3 24 25 26 27 0.1  
10 31

No-foreign particle B/w

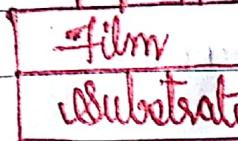
8 Mask & PR



9 Particles on mask



10 Stamp on + PR



11 film  
substrate

(Photo Resist)

12 auto Resist (PR) → Chemical layer.

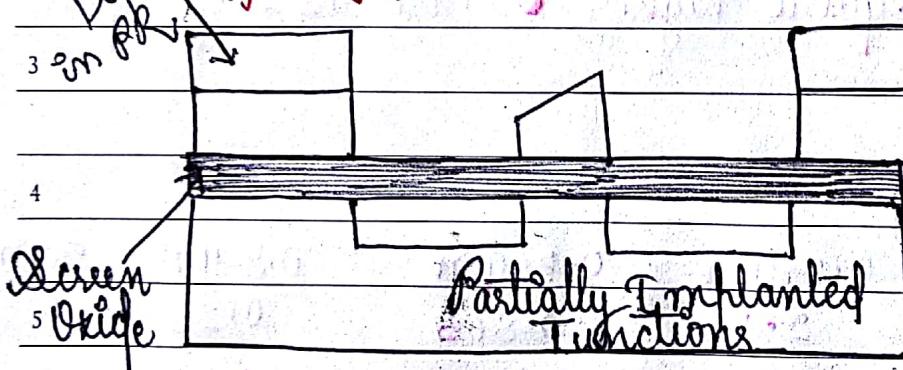
n+ Mask

Mask Pt

1 Mask ⇒ Allow fall off X-Ray.

1

2 Effect of particle combination :-



3 Purpose of  
TAN -

4 TAN filter unit  
(FFU)  
provides  
filtered  
recirculated

air to the  
clean  
room.

5 Clean Room Structure

6 Make up Air

7 Fans

8 Make up Air

NOTES  
Control  
Area

9 Class 1000

10 HEPA FILTER class 1

11 Process Area

12 Process Area

13 Equipment Area

14 Between Air

15 Raised floor with GPO Panels

16 Pump Rf etc

NOVEMBER 2014

S	M	T	W	T
30	1	2	3	4
2	3	4	5	
9	10	11	12	
16	17	18	19	
23	24	25		

NOVEMBER

Hepa filters → HEPA (High Efficiency particulate Air / Absorb is a type of air filter).

To qualify as HEPA :-

- An air filter must remove (99.97%) of particles that have a size greater than or equal to  $0.3 \mu\text{m}$ .

Areas -

Process Area

Equipment Area.

Mini Environment -

Class 1000 clean room, lower cost

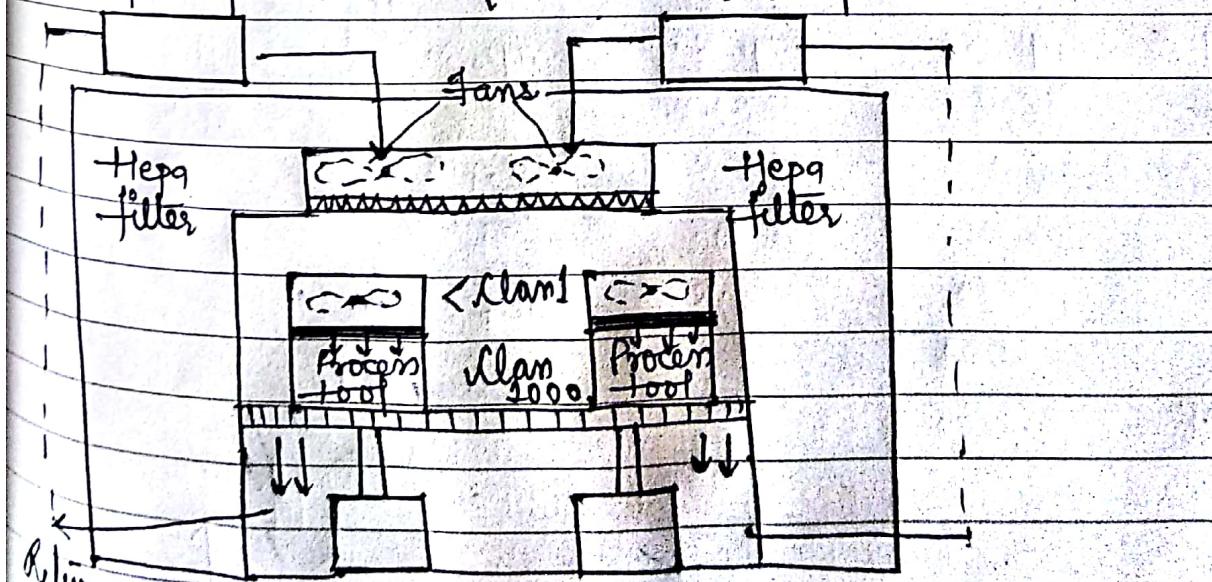
Better than class 1 environment around wafers &amp; process tools.

Broad room arrangement, no walls b/w process & equipment  
Automatic wafer bans for b/w process tools.

Mini Environment Cleanroom -

Make up Air

Make up Air



NOVEMBER 2014

W	T	F	S
3	4	5	6
10	11	12	13
17	18	19	20
24	25	26	27

Adv. &amp; Disadvantages

# Semiconductor Manufacturing processes -

Design

Wafer preparation

front-end processes

Photolithography

Etch

Cleaning

Thin films

Ion Implantation

Planarization

Test & Assembly

Ion-implantation :-

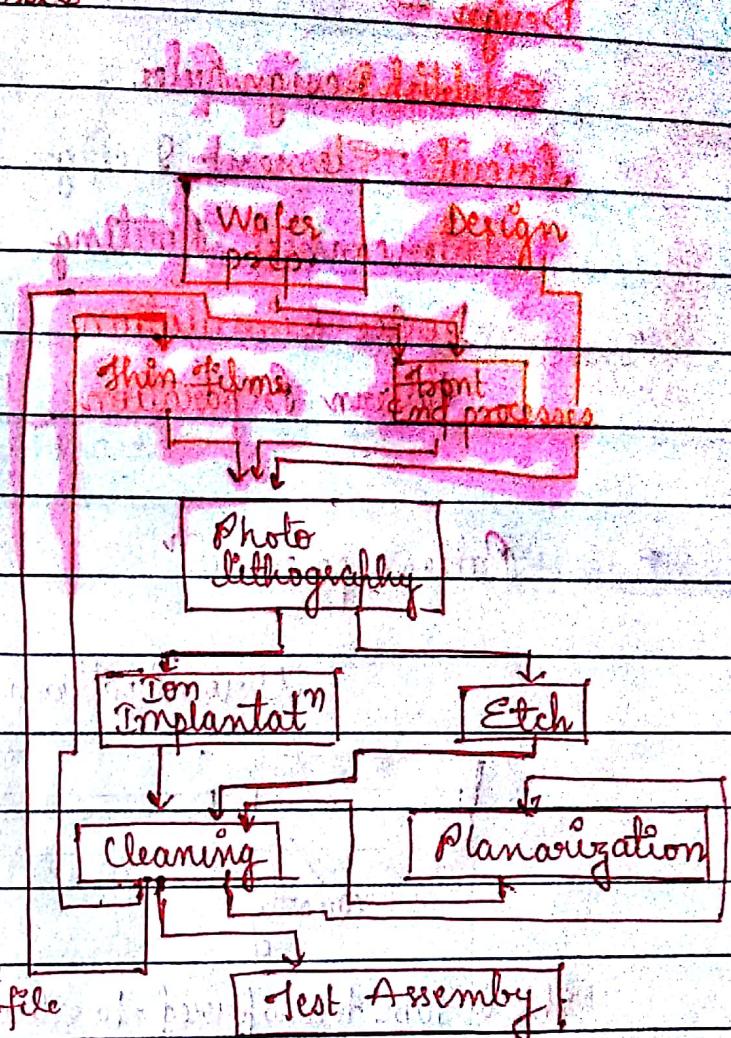
Advantages - overcomes the disadvantage of diffusion in doping profile

- Ions moving; due to their  $k_0 E^0$  they may destroy the substrate dislocation due to displacement of semiconductors

It could replace silicon from its lattice;

Planarization process of these empty spaces act as trap; trap the electrons; and prevent hamper gain as well as performance.

PR will act as a selective material i.e. will decide that whether the light will fall on which part.



## Design

### Establish Design Rules

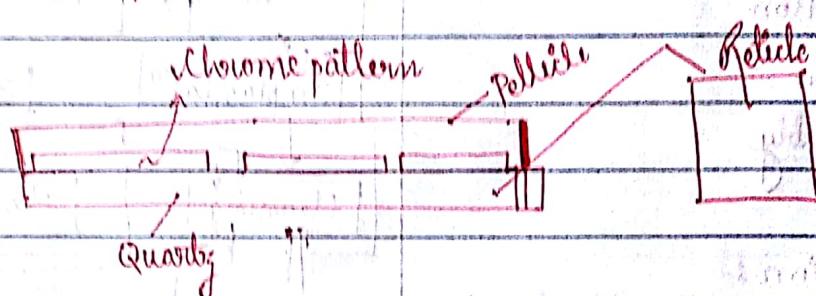
Circuit Element Design (concerned with VLSI), Ex - Single stage, multi stage

### Interconnect Routing

### Device Simulation

### Pattern Preparation

### Pattern Preparation



This is to be transferred to silicon wafer

the pattern to be transferred is developed on Quartz

Negative of this pattern is called Mask

### Initial Silicon Preparation and Purification

#### 1. Polysilicon Refining (Silicon refining)

#### 2. Crystal Pulling (Monocrystalline silicon pulled; contaminants remain inside container)

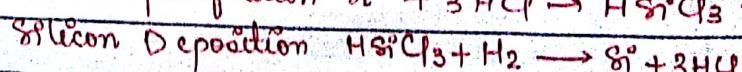
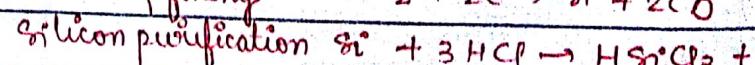
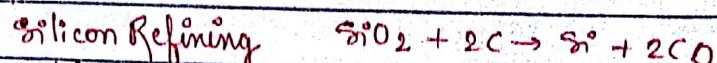
#### 3. Wafer Slicing & Polishing

#### 4. Epitaxial Layer (silicon layer deposited on these layers)

another layer on substrate layer

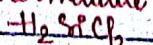
This is ultrapure layer

### Chemical Reactions -



Reactants -  $\text{H}_2$

Silicon Intermediate



Crystal pulling -  
process conditions

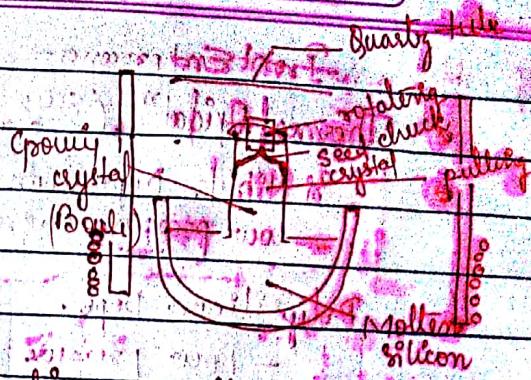
flow Rate : 20 to 50 litres/min

Time : 18 to 24 hrs

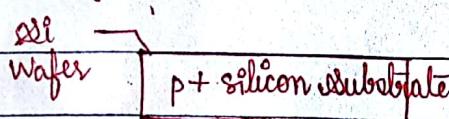
Temp :  $> 1300^{\circ}\text{C}$

Pressure : 20 torr

At this level we are able to achieve pure silicon



Wafer Slicing & Polishing -



The silicon ingot is grown and individual wafers are sliced.

The silicon ingot is sliced into individual wafers polished, and

Epitaxial Silicon Deposition -  
To provide a very pure area, for development of device  
made up of ultra clean silicon.  
To provide a very pure area, for development of device  
(very thin) wafers which produce  
develop kijayegi wahan per epitaxial layer form.

Chemical Reactn -

Silicon Deposition :  $\text{HSiCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}$

Process conditions

flow Rate = 5 to 50 litres/min

temp =  $900$  to  $1100$  degrees C.

Pressure = 100 torr to Atmosphere

(low temperature required for epitaxial layers)

Si Source	Dopants	Electant
$\text{SiH}_4$	$\text{AsH}_3$	$\text{HCl}$
$\text{H}_2\text{SiCl}_3$	$\text{B}_2\text{H}_6$	Carriers
$\text{HSiCl}_3$	$\text{PH}_3$	$\text{As}$
$\text{SiCl}_4$		$\text{H}_2$
		$\text{N}_2$

### Front End processes -

• Thermal Oxidation ( $\text{Si}^0 + \text{O}_2 \rightarrow \text{SiO}_2$  silicon reacting with oxygen)  $\rightarrow$  electrically insulating

• Nitride Deposition

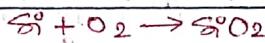
— low pressure chemical vapor Deposition (LPCVD)

• Polysilicon Depo.

— Low pressure Chemical Vapor Deposition (LPCVD)

• Annealing

\*  $\text{SiO}_2$  is property of  $\text{Si}^0$  due to which we prefer  $\text{Si}^0$  over Germanium



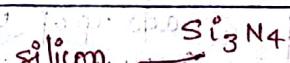
layer will not react  $\checkmark$

### Silicon Nitride Deposition -

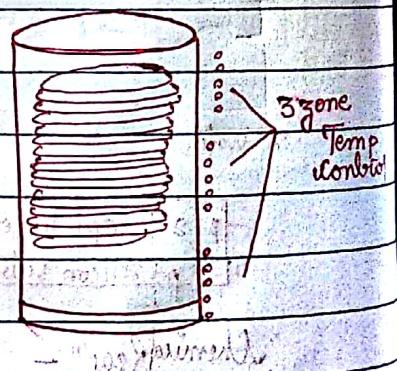
### Annealing

Thermal Oxidation :-  $\text{Si}^0 + \text{O}_2 \rightarrow \text{SiO}_2$

Nitride Deposition :-  $3\text{SiH}_4 + 4\text{NH}_3 \rightarrow$



PolySilicon Deposition :-  $\text{SiH}_4 \rightarrow \text{Si}^0 + 2\text{H}_2$



### Process Conditions (Silicon Nitride (PCVD))

flow rates : 10 - 300 sccm

Temperature : 600 degrees C

Pressure : 100 m torr

### Oxidation

Polysilicon

Nitride

Annealing

Ar

$\text{N}_2$

$\text{H}_2$

$\text{Cl}_2$

$\text{H}_2$

$\text{H}_4$

$\text{O}_2$

Dichloro ethane

### Oxidation

Ar

$\text{N}_2$

$\text{H}_2$

$\text{Cl}_2$

$\text{H}_2$

$\text{H}_4$

$\text{O}_2$

$\text{P}_4\text{H}_3$

Dichloro ethane

### Nitride

Ar

$\text{N}_2$

$\text{H}_2$

$\text{Cl}_2$

$\text{H}_2$

$\text{H}_4$

$\text{O}_2$

$\text{P}_4\text{H}_3$

Dichloro ethane

### Annealing

Ar

$\text{He}$

$\text{H}_2$

$\text{N}_2$

$\text{H}_4$

$\text{O}_2$

$\text{P}_4\text{H}_3$

Dichloro ethane

to cool the temp.

temp. is higher,

because it

is a high temp.

process.

from high temp.

low temp.

process - 1300°C

polysilicon → ? This is ultraclean.

Date : / /

Silicon unsaturated bonds at the surface are being combined with oxygen.

But when we use Boron; top layer is not formed.

\*  $\text{SiO}_2$  importance

$\text{SiO}_2$  layer acts as a perfect insulator

act as opaque; if areas are developed, further no reaction can take place over that silicon.

protect our silicon base from other processes.

or To protect layer at certain places we can go for dry as well as wet oxidation.

\* Silicon is deposited over wafer substrate.

$\text{SiO}_2$  not soluble in water. But Germanium oxide is soluble in water.

\* Why are we decreasing temp in each step?

why do we avoid high temp?

Photolithography — transferring of pattern

Photoresist Coating process

Exposure Process

transferring the pattern of mask

surface of PR is modified acc. to pattern

organic  
chemical  
material

when light falls on them,

they change their  
property either  
gets solidified or

light falling  
Mask

PR material (drop-drip given)

Silicon spreads evenly on  
the surface

spindle moving

Then PR reacts with light & gets solidified;

when we take off Mask we see

Mask's pattern has been transferred

on PR; furthermore go for etch. OR ice removal of parts on PR.

\* Also we can get complement of pattern.

Page :

Date : / /

if edge & wavelength are same, diffraction occurs  
Bending occurs.

### • Photoresist Coating processes. -

Photoreists

Negative PR: pattern, photoresist exposed to light or  
+ve PR: resist don't expose to light

Other Auxiliary Materials (Liquids)

Edge Bead Removers

-Anti-Reflective Coatings-

Adhesion promoters / Primers (HMDS)

Rinses / Thinners / Corrosion Inhibitors

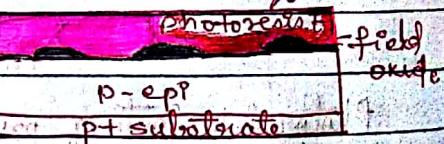
Contrast Enhancement Materials

Developers

reaction in developer - hydrophilicity

} TMAH

{ Speciality Developers



pattern developed.

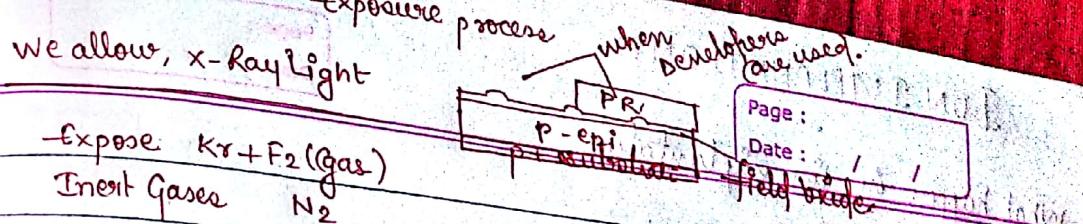
X selectively  
remove other  
of these

Inert Gases

Ar] - to remove for scratching anti-antireflective  
N<sub>2</sub>] - to create inert atmosphere inside furnace

\* Simbility < Ge. mobility

\*  $\sigma$  conductivity < Ge conductivity

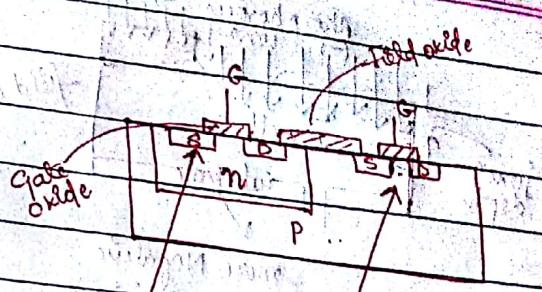


**Ion implantation :-**

Well Implants

Channel Implants

Source/Drain Implants



Substrate -

$V_g > V_{Th}$ , there will be channel inversion

MOSFET operation in saturation mode controlled by  $V_{Th}$  (Voltage)

$V_g < V_{Th}$ , there will be weak inversion

On a MOSFET

O/P voltage -  $V_{DS}$ ; I/P voltage -  $V_g$

Transfer curve -  $I_p$  vs O/P

v-I characteristic -  $V_{DS}$  versus  $I_D$   
amplification → ?

$V_g < V_{Th}$  → Mosfet will act like a capacitor. That too variable capacitor charge coupled app - in Digital cameras.

$V_{Th}$  depends upon thickness of the oxide at the back of gate.  $V_g$  will not cross  $V_{Th}$  if more thicker.

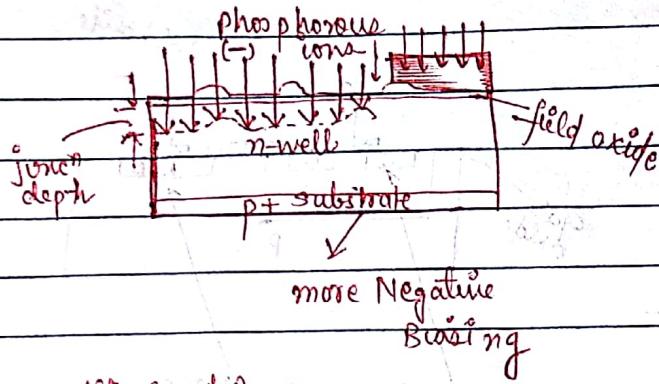
To develop slightly thick  $\text{SiO}_2$  layer, it could provide isolation (Natural)

Even if we apply, gate voltage it not effect, since the field oxide grown between these two is quite thicker.

substrate forms junction, forward biased; current flow from substrate to ground, efficiency O/P would hamper. Hence it should always be reverse biased.

substrate is grounded always; Hence substrate & device P-type substrate is grounded we ensure our if n-type ground, helping for Biased.

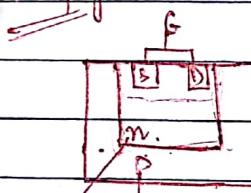
# What happens in ion implantation?



diffusion of Boron,  
due to temperature; Boron will diffuse inside the ~~so~~ layer

In diffusion process, phosphorous would not diffuse so deeply,  
since temperature gradient is not so even; (kuch neeche jake)  
accumulate  
thermal mech. is not supporting;

see fig -



this ~~will~~ development of  
n should be much thicker;

~~done through ion implantation~~  
phosphorous when diffused inside ~~substrate~~ accumulates to a certain level &  
does not go deep inside n-layer.

This is not a thermal process.  
phosphorous ions accelerated; bombarded with surface; penetrate with  
the substrate.

flow rate = 5 sccm (R 190 cm<sup>2</sup>/min)

Pressure =  $10^{-5}$  torr (for good penetration)

Accelerating voltage = 5 to 200 keV

Gases -

Ar

AsH<sub>3</sub>

B<sub>2</sub>F<sub>5</sub>

He

N<sub>2</sub>

PH<sub>3</sub>

SiH<sub>4</sub>

SiF<sub>4</sub>

GeH<sub>4</sub>

Solids -

O<sub>2</sub>

Ti

Si

Al

Si<sub>3</sub>N<sub>4</sub>

SiO<sub>2</sub>

SiC

Si<sub>2</sub>N<sub>3</sub>

Si<sub>3</sub>N<sub>4</sub>

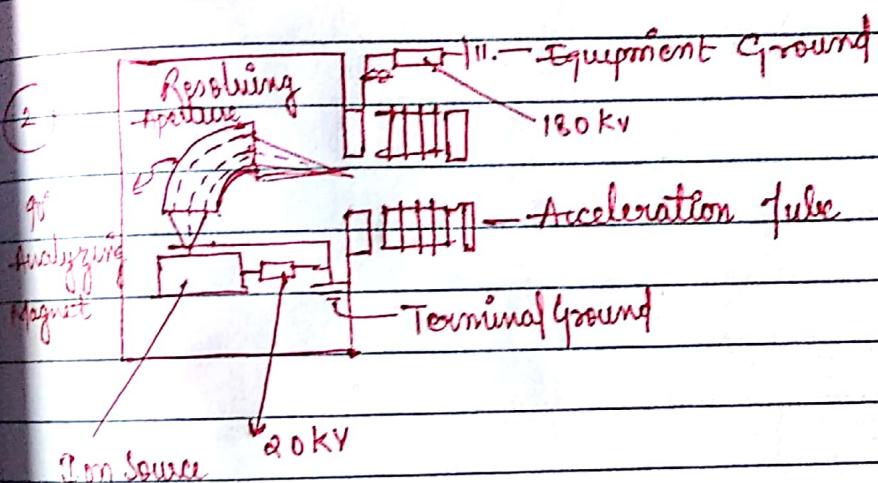
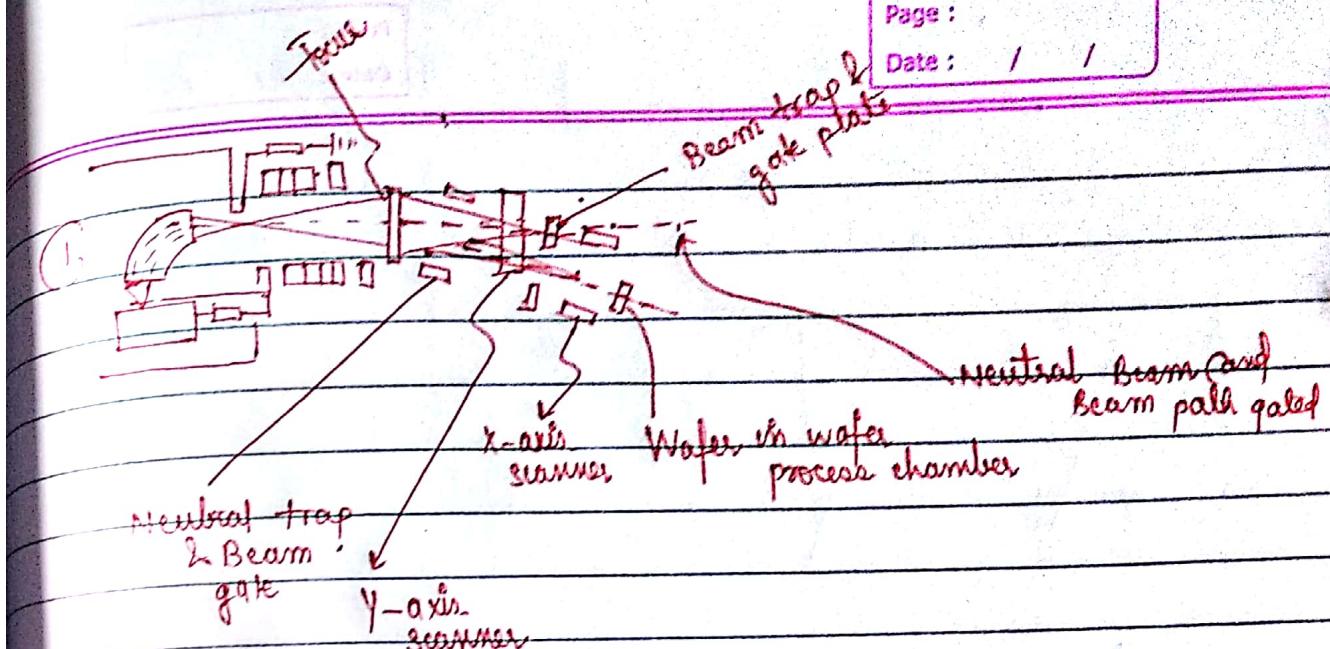
SiO<sub>2</sub>

SiC

Si<sub>3</sub>N<sub>3</sub>

SiO<sub>2</sub>

SiC



Q Why do we need Biasing?  
Q Source of es?

Speed  
concentrat<sup>n</sup>  
conc<sup>n</sup>  
olp of 1 phosphorous;

What is implantat<sup>n</sup>; how is it Being sealed;  
Disad.; Advantages?

def

→ Etch → remove material while fabricating  
(we in some cases we develop  $\text{SiO}_2$  layer).

### → Conductor Etch

- Poly Etch and Silicon

etch & etch

— Metal Etch

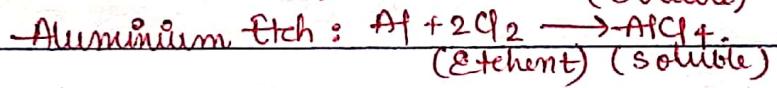
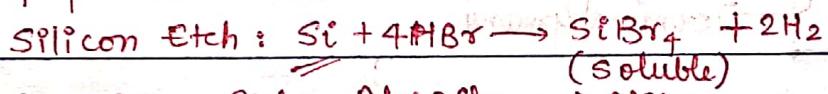
→ Dielectric Etch.

require different types of etchant.  
Mech of removal : chemical reaction

Metal interconnects - providing connection along various parts of chip

### Conductor Etch :-

Chemical Reactions :-



Process Conditions :-

flow rates : 100 to 300 ml/min

Pressure : 10 to 500 m torr

RF Power : 50 to 100 Watts

Polyconic Etches -

HBr

$\text{CF}_3$

SF<sub>6</sub>

NF<sub>3</sub>

O<sub>2</sub>

Aluminium Etches

BCl<sub>3</sub>

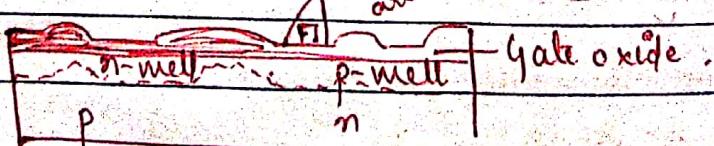
Cl<sub>2</sub>

Diluents -

Ar

He

source  
drain  
area N<sub>2</sub>

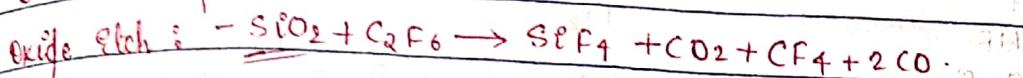


## Dielectric Etch

Page :

Date : / /

Chemical Reac<sup>n</sup> -



Process -

flow rates - 10 to 300 sccm

5 to 10 mTorr

100 to 200 Watts

Plasma Dielectric Etch

Diluents

CHF<sub>3</sub>

CO<sub>2</sub>

Ar

CF<sub>4</sub>

O<sub>2</sub>

He

C<sub>2</sub>F<sub>6</sub>

SF<sub>6</sub>

N<sub>2</sub>

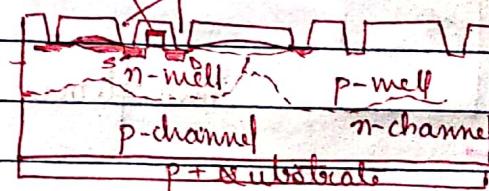
C<sub>3</sub>F<sub>8</sub>

SiF<sub>4</sub>

Metal gate

CO

Contact locations



Cleaning - (should be able to remove unwanted material)

- Critical Cleaning

- Photoresist strips (used in lithography to remove photoresist)

- Pre-Deposition Cleans.

\* Dep → The surface of the wafer should be ultraclean.

Vertical Cleaning -

Process conditions :-

Temp - Piranha Strip @ 180°C.

RCA Clean

Liquid Clean { SC1 Clean ( $\text{H}_2\text{O} + \text{NH}_4\text{OH} + \text{H}_2\text{O}_2$ )  
SC2 Clean ( $\text{H}_2\text{O} + \text{HCl} + \text{H}_2\text{O}_2$ )}

Piranha Strip -

Before contact we clean the surface since voids are created; especially in weak contact

$\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$   
to prevent device from failing in the purpose of ultra cleaning

~~Dry clean -~~

HF  
C<sub>2</sub> plasma  
Alcohol + O<sub>3</sub>

Dry strip

N<sub>2</sub>O  
O<sub>2</sub>  
CF<sub>4</sub> + O<sub>2</sub>  
O<sub>3</sub>

Solvent cleanse

NMP

Proprietary

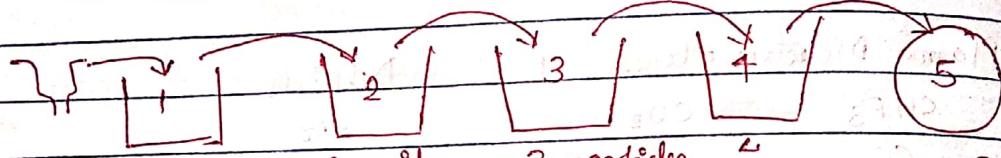
Amines (C<sub>2</sub>-C<sub>4</sub>)

Nitride strip

H<sub>3</sub>PO<sub>4</sub>

Oxide strip

HF + H<sub>2</sub>O



1 organics      2 oxides      3 particles

H<sub>2</sub>SO<sub>4</sub> +

H<sub>2</sub>O<sub>2</sub>

H<sub>2</sub>O Rinse

HF +

H<sub>2</sub>O

H<sub>2</sub>O Rinse

NH<sub>4</sub>OH +

H<sub>2</sub>O<sub>2</sub> + H<sub>2</sub>O

H<sub>2</sub>O Rinse

HCl +

H<sub>2</sub>O<sub>2</sub>

H<sub>2</sub>O Rinse

5 Dry

H<sub>2</sub>O<sub>2</sub>

IPA +

N<sub>2</sub>

## Thin films

### • Chemical Vapor

Deposition (CVD) dielectric  
(Vapour Dep. through Chemical Reac<sup>n</sup>)

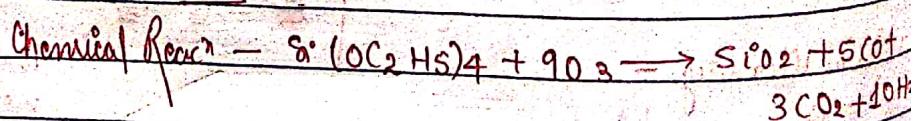
(process through which,  
we can develop a thin  
layer over &<sup>1</sup>)

### • CVD of tungsten for metallization

### • Phy. Vapour Deposition (PVD)

(Vapour Dep. through physical  
method, put it directly over the  
substrate).

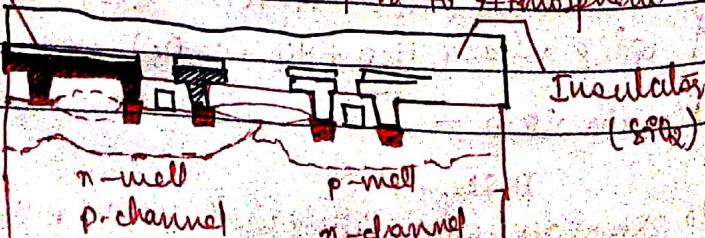
CVD

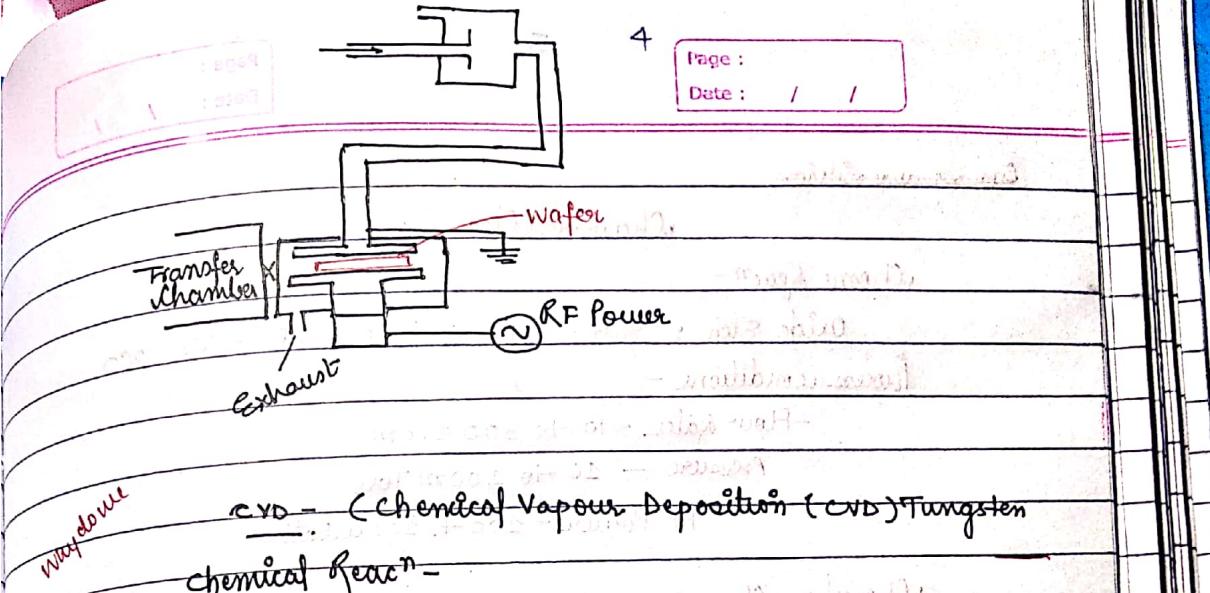


Process for condition (CLD)

Flow rate :- 100 to 300 sccm

Pressure :- 50 torr to Atmospheric





Process conditions -

- Flow Rate - 100 to 300

- Pressure - 100 m

- Temperature - 400°C

CVD Dielectric

WF<sub>6</sub>

Ar

H<sub>2</sub>

N<sub>2</sub>

- n-well & p-well created
- on epitaxial layer
- (PVD not preferred for epilayer)

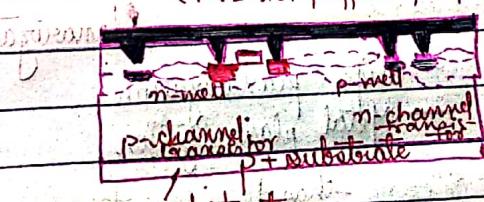
PVD -

Process conditions -

Pressure < 5 mTorr

Temp : 200 degrees C

RF Power :



Barrier Metal -

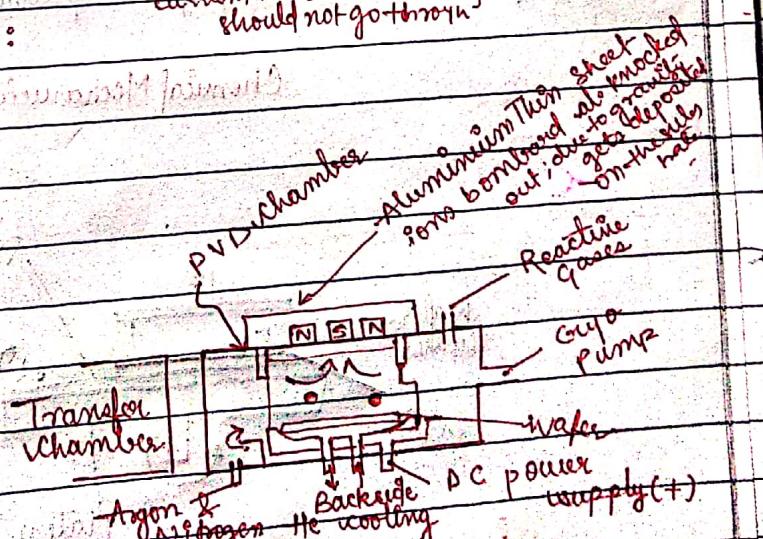
SiH<sub>4</sub>

Ar

N<sub>2</sub>

N<sub>2</sub>

T<sub>p</sub> PVD Targets



Target material will deposit over the substrate directly.  
if we change Temp? - How does the diffusion in doping profile change?

All electrical phenomena at the surface.

Gate - for control

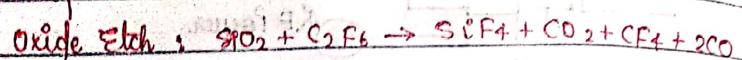
Source - charged egg

Drain - " 1019

Common Williams,

## Chamber Cleaning -

### Chemo. Reactn -



### Process conditions -

- flow Rate - 10 to 300 sccm

Pressure - 10 to 100 m Torr

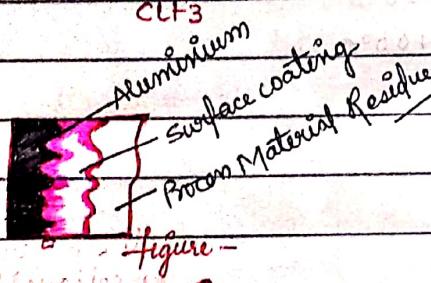
RF Power - 100 to 200 Watts

## Chamber Cleaning -

$\text{CaF}_6$

$\text{NF}_3$

$\text{ClF}_3$



wafers - layer deposited taken out from assembly

- their structure look like shown in fig -

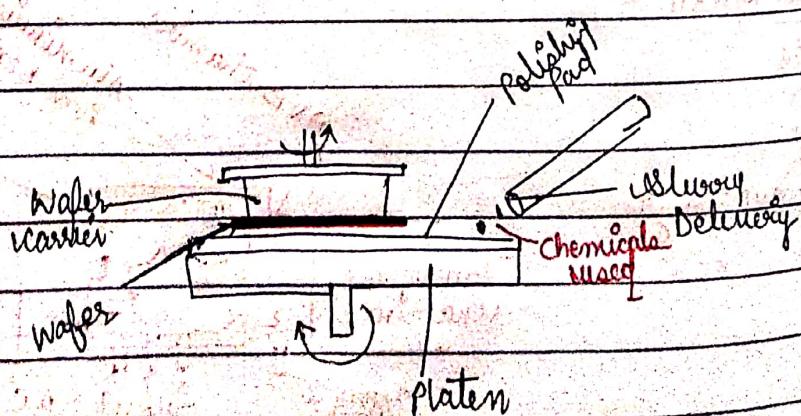
## Planarization -

- Oxide planarization

- Metal planarization

Sizing - has to be done for proper encapsulation.

## Chemical Mechanical Planarization (CMP)



### Process conditions (oxide)

flow : 250 to 2000 ml/min

Particle size : 100 to 250 nm

pH : 10 to 15 or 10.5 to 11.3 pH

Semiconductor  
Device physics

6

Page :

Date : / /

### Process Conditions (Metal)

flow : 50 to 100 ml/min

Particle size - 180 to 280 nm

Conc<sup>n</sup> - 3 to 7%, 4-14.4 pH

CMP (metal)

Alumina

Fe NO<sub>3</sub>

CMP (Okta)

Silica Slurry

KOH

NH<sub>4</sub>OH

H<sub>2</sub>O.

### Test & Assembly -

provide electrical connection to the chip.

Backing (carrier film)

Polyurethane

Pad

Polyurethane

Pad conditioner

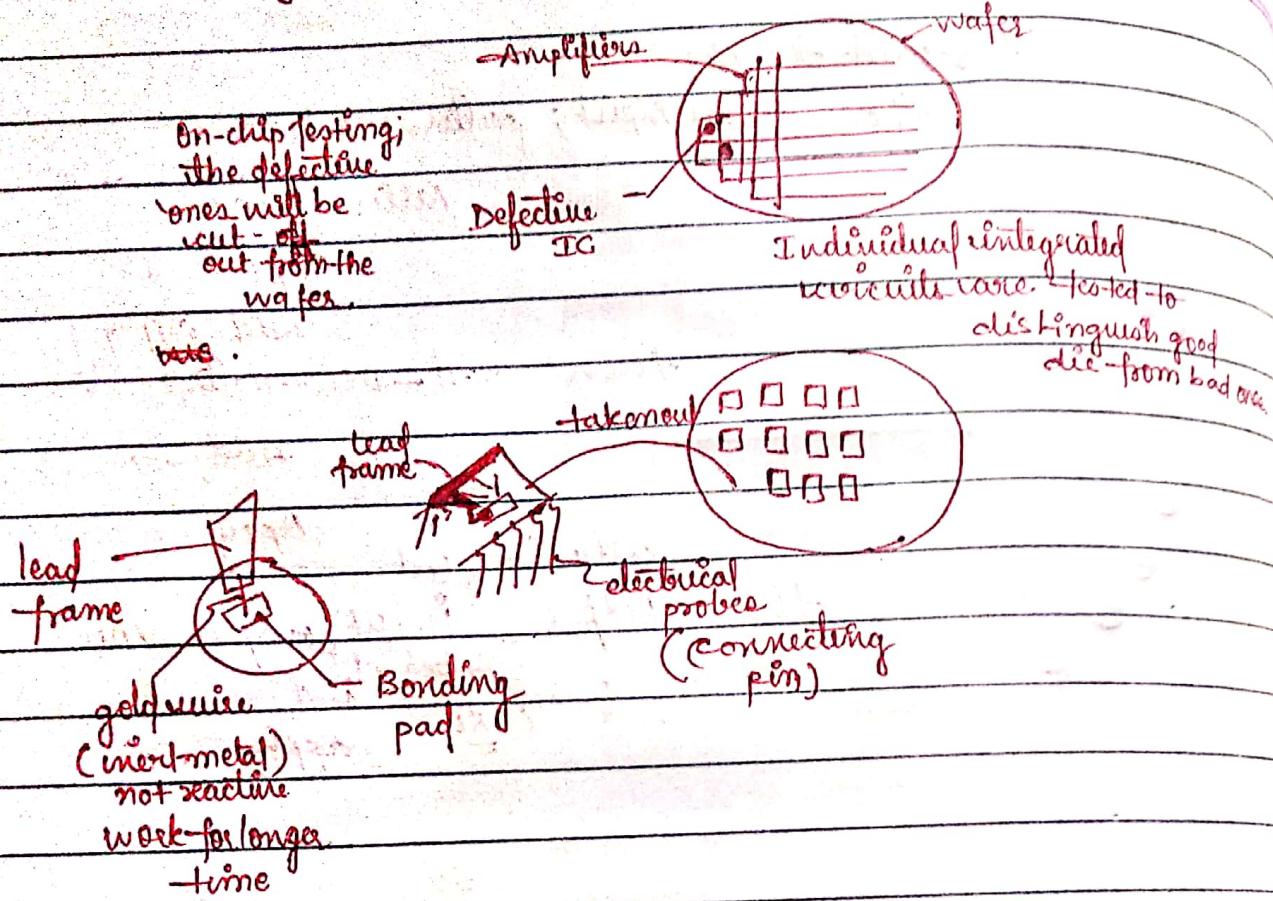
Abrasives

— last process in fabrication —

- ① Electrical Test probe (Amplification being performed or not)
- ② Die cut and Assembly (Devices are cut on wafer)
- ③ Die Attach & Wire Bonding (Packaging) (chip designed)
- ④ final test . Is chip working or not. (Reliability Test)

LAB WORK -

electrically probes connected at various parts of chip



Chips are electrically tested under varying environmental ~~test~~ conditions

small size → capacitance effect, Interference, power consump<sup>n</sup> high,

## OXIDATION -

Thermal oxidation -

$\text{SiO}_2$  and the  $\text{Si}/\text{SiO}_2$  interface are the principal reasons for silicon's dominance in the technology.

$\text{SiO}_2$ :

Easily selectively etched using lithography  
Masks most common impurities (B, P, As, Sb)  
→ All out-to-touch Si Layer

Excellent Insulator ( $\tau > 10^{16} \Omega \text{ cm}$ , Eg  $> 9 \text{ eV}$ )  
passivation device is masked with  $\text{SiO}_2$

$\text{SiO}_2$  blocks electric current flow between  
High voltage is Required ( $10^7 \text{ V/cm}^2$ )

Excellent func<sup>n</sup> passivation:  
stable Bulk electrical properties.

of  $\text{SiO}_2$  - [ surface (all problems are at the surface)  
Bulk → the bulk property of  $\text{SiO}_2$  is very stable.

stable and reproducible interface

properties of  $\text{SiO}_2$

Energy Band  
is quite higher

Thermal  $\text{SiO}_2$  is amorphous

Weight Density =  $2.20 \text{ g/cm}^3$

Molecular =  $2 \times 10^{22} \text{ molecules/cm}^3$

Crystalline  $\text{SiO}_2$  [Quartz] =  $2.65 \text{ g/cm}^3$

(1) - Excellent Electrical Insulator

Resistivity  $> 10^{12} \text{ ohm-cm}$  Every  $9 \text{ eV}$

(2) - High Breakdown Electric field  $> 10 \text{ MV/cm}$

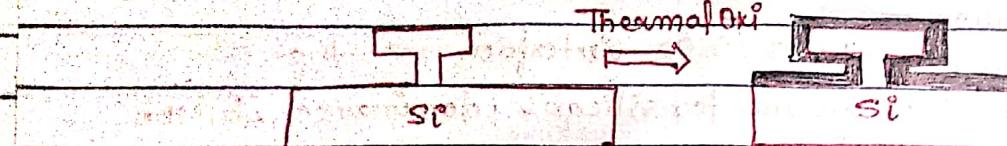
(3) - Stable and Reproducible  $\text{Si}/\text{SiO}_2$

Interface.

acc. to the shape

## Conformal oxide growth on exposed Si<sup>+</sup> surface

Thermal Oxide



$\text{SiO}_2$  is a good diffusion mask for common dopants.

$S_i \leq D_{\text{SiO}_2} < D_{\text{Si}}$ , S, B, P, As, Sb

$\text{SiO}_2$  would protect the layer below it.  
Masked Area      Masked Area

Rate of Phosphorous diffusion >> than at  $\text{SiO}_2$ .

### Properties of $\text{SiO}_2$

Very good etching selectivity betw  $\text{Si}$  &  $\text{SiO}_2$ .

Etching rate of  $\text{SiO}_2$  is very slow.

Germanium oxide can be etched very easily;

### Oxide

Thickness -

Thermally Grown Oxides

Deposited Oxide

100 Å

Field Oxides

Layers

0.14

Masking Oxides

Backed

100 Å

Gate Oxides, Pad Oxides

Insulators

10 Å

Tunneling Oxide

Between

Chemical Oxides

Metal Layers

from Cleaning Native

Masking Oxide

Electrical prop. of  $\text{SiO}_2$  would

vary with the applied

voltage due to variation

in the thickness of

oxide.