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//Tool Version: Vivado v.2015.2 (lin64) Build 1266856 Fri Jun 26 16:35:25 MDT 2015

//Date : Thu Dec 10 16:39:28 2015

//Host : apollo running 64-bit Ubuntu 12.04.3 LTS

//Command : generate\_target design\_1\_wrapper.bd

//Design : design\_1\_wrapper

//Purpose : IP block netlist

//--------------------------------------------------------------------------------

`timescale 1 ps / 1 ps

//`default\_nettype none

module design\_1\_wrapper

(DDR\_addr,

DDR\_ba,

DDR\_cas\_n,

DDR\_ck\_n,

DDR\_ck\_p,

DDR\_cke,

DDR\_cs\_n,

DDR\_dm,

DDR\_dq,

DDR\_dqs\_n,

DDR\_dqs\_p,

DDR\_odt,

DDR\_ras\_n,

DDR\_reset\_n,

DDR\_we\_n,

FIXED\_IO\_ddr\_vrn,

FIXED\_IO\_ddr\_vrp,

FIXED\_IO\_mio,

FIXED\_IO\_ps\_clk,

FIXED\_IO\_ps\_porb,

FIXED\_IO\_ps\_srstb,

locked,

pixel\_clk\_out\_p,

pixel\_clk\_out\_n,

vid\_io\_out\_active\_video\_p,

vid\_io\_out\_active\_video\_n,

vid\_io\_out\_data\_p,

vid\_io\_out\_data\_n,

//vid\_io\_out\_field,

//vid\_io\_out\_hblank,

vid\_io\_out\_hsync\_p,

vid\_io\_out\_hsync\_n,

//vid\_io\_out\_vblank,

vid\_io\_out\_vsync\_p,

vid\_io\_out\_vsync\_n

);

inout [14:0]DDR\_addr;

inout [2:0]DDR\_ba;

inout DDR\_cas\_n;

inout DDR\_ck\_n;

inout DDR\_ck\_p;

inout DDR\_cke;

inout DDR\_cs\_n;

inout [3:0]DDR\_dm;

inout [31:0]DDR\_dq;

inout [3:0]DDR\_dqs\_n;

inout [3:0]DDR\_dqs\_p;

inout DDR\_odt;

inout DDR\_ras\_n;

inout DDR\_reset\_n;

inout DDR\_we\_n;

inout FIXED\_IO\_ddr\_vrn;

inout FIXED\_IO\_ddr\_vrp;

inout [53:0]FIXED\_IO\_mio;

inout FIXED\_IO\_ps\_clk;

inout FIXED\_IO\_ps\_porb;

inout FIXED\_IO\_ps\_srstb;

output locked;

output pixel\_clk\_out\_p;

output pixel\_clk\_out\_n;

output vid\_io\_out\_active\_video\_p;

output vid\_io\_out\_active\_video\_n;

output [15:0]vid\_io\_out\_data\_p;

output [15:0]vid\_io\_out\_data\_n;

//output vid\_io\_out\_field;

//output vid\_io\_out\_hblank;

output vid\_io\_out\_hsync\_p;

output vid\_io\_out\_hsync\_n;

//output vid\_io\_out\_vblank;

output vid\_io\_out\_vsync\_p;

output vid\_io\_out\_vsync\_n;

wire [14:0]DDR\_addr;

wire [2:0]DDR\_ba;

wire DDR\_cas\_n;

wire DDR\_ck\_n;

wire DDR\_ck\_p;

wire DDR\_cke;

wire DDR\_cs\_n;

wire [3:0]DDR\_dm;

wire [31:0]DDR\_dq;

wire [3:0]DDR\_dqs\_n;

wire [3:0]DDR\_dqs\_p;

wire DDR\_odt;

wire DDR\_ras\_n;

wire DDR\_reset\_n;

wire DDR\_we\_n;

wire FIXED\_IO\_ddr\_vrn;

wire FIXED\_IO\_ddr\_vrp;

wire [53:0]FIXED\_IO\_mio;

wire FIXED\_IO\_ps\_clk;

wire FIXED\_IO\_ps\_porb;

wire FIXED\_IO\_ps\_srstb;

wire locked;

wire pixel\_clk\_out;

wire vid\_io\_out\_active\_video;

wire [15:0]vid\_io\_out\_data;

wire vid\_io\_out\_field;

wire vid\_io\_out\_hblank;

wire vid\_io\_out\_hsync;

wire vid\_io\_out\_vblank;

wire vid\_io\_out\_vsync;

wire[15:0] vid\_io\_out\_data\_p;

wire diff\_clock\_clk\_n;

wire diff\_clock\_clk\_p;

//wire locked;

wire rst\_n;

//wire vid\_io\_out\_active\_video;

// wire [15:0]vid\_io\_out\_data;

//wire vid\_io\_out\_field;

//wire vid\_io\_out\_hblank;

//wire vid\_io\_out\_hsync;

//wire vid\_io\_out\_vblank;

//wire vid\_io\_out\_vsync;

//wire pixel\_clk\_out;

wire locked\_n;

design\_1 design\_1\_i

(.DDR\_addr(DDR\_addr),

.DDR\_ba(DDR\_ba),

.DDR\_cas\_n(DDR\_cas\_n),

.DDR\_ck\_n(DDR\_ck\_n),

.DDR\_ck\_p(DDR\_ck\_p),

.DDR\_cke(DDR\_cke),

.DDR\_cs\_n(DDR\_cs\_n),

.DDR\_dm(DDR\_dm),

.DDR\_dq(DDR\_dq),

.DDR\_dqs\_n(DDR\_dqs\_n),

.DDR\_dqs\_p(DDR\_dqs\_p),

.DDR\_odt(DDR\_odt),

.DDR\_ras\_n(DDR\_ras\_n),

.DDR\_reset\_n(DDR\_reset\_n),

.DDR\_we\_n(DDR\_we\_n),

.FIXED\_IO\_ddr\_vrn(FIXED\_IO\_ddr\_vrn),

.FIXED\_IO\_ddr\_vrp(FIXED\_IO\_ddr\_vrp),

.FIXED\_IO\_mio(FIXED\_IO\_mio),

.FIXED\_IO\_ps\_clk(FIXED\_IO\_ps\_clk),

.FIXED\_IO\_ps\_porb(FIXED\_IO\_ps\_porb),

.FIXED\_IO\_ps\_srstb(FIXED\_IO\_ps\_srstb),

.locked(locked\_n),

.pixel\_clk\_out(pixel\_clk\_out),

.vid\_io\_out\_active\_video(vid\_io\_out\_active\_video),

.vid\_io\_out\_data(vid\_io\_out\_data),

.vid\_io\_out\_field(vid\_io\_out\_field),

.vid\_io\_out\_hblank(vid\_io\_out\_hblank),

.vid\_io\_out\_hsync(vid\_io\_out\_hsync),

.vid\_io\_out\_vblank(vid\_io\_out\_vblank),

.vid\_io\_out\_vsync(vid\_io\_out\_vsync));

OBUFDS #(

.IOSTANDARD("DEFAULT")

) OBUFDS\_inst[15:0] (

.O(vid\_io\_out\_data\_p),

.OB(vid\_io\_out\_data\_n),

.I(vid\_io\_out\_data)

);

OBUFDS #(

.IOSTANDARD("DEFAULT")

) OBUFDS\_inst10 (

.O(pixel\_clk\_out\_p),

.OB(pixel\_clk\_out\_n),

.I(pixel\_clk\_out)

);

OBUFDS #(

.IOSTANDARD("DEFAULT")

) OBUFDS\_inst1 (

.O(vid\_io\_out\_hsync\_p),

.OB(vid\_io\_out\_hsync\_n),

.I(vid\_io\_out\_hsync)

);

OBUFDS #(

.IOSTANDARD("DEFAULT")

) OBUFDS\_inst2 (

.O(vid\_io\_out\_active\_video\_p),

.OB(vid\_io\_out\_active\_video\_n),

.I(vid\_io\_out\_active\_video)

);

OBUFDS #(

.IOSTANDARD("DEFAULT")

) OBUFDS\_inst3 (

.O(vid\_io\_out\_vsync\_p),

.OB(vid\_io\_out\_vsync\_n),

.I(vid\_io\_out\_vsync)

);

assign locked = ~locked\_n;

endmodule