VISVESVARAYA TECHNOLOGICAL UNIVERSITY
BELGAUM,KARNATAKA

Project Report on

SORT OPTIMIZATION ALGORITHM OF MEDIAN FILTERING BASED ON FPGA

Submitted in partial fulfillment of the requirements for the award of degree

BACHELOR OF ENGINEERING

In

ELECTRONICS AND COMMUNICATION ENGINEERING

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CERTIFICATE

Certified that the project work entitled "**Sort Optimization Algorithm of Median Filtering based on FPGA**" carried out by **Mr. Srihari Prahlad (1BY18EC160), Mr. Sai Karthik M (1BY18EC141), Mr. Shubhankar R (1BY18EC434),** and **Mr. Prajwal M (1BY17EC160)** are bonafide students of **BMS Institute of Technology and Management** in partial fulfilment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** prescribed by **Visvesvaraya Technological University, Belagavi** during the academic year **2020-2021.** It is suggested that all corrections/suggestions indicated for internal assessment have been indicated in the report deposited in the departmental library. The project report has been approved asit satisfies the academic requirements in respect of project work prescribed for the said degree.

Signature of Guide	Signature of HOD	Signature of Principal
Dr. Dankan Gowda V	**Dr. Jayadeva G S**	**Dr. Mohan Babu G.N.**
Dept. of ECE	Dept. of ECE	BMSIT&M

External Viva

Name of the Examiners	Signature with Date
1.	
2.	

ABSTRACT

The traditional sorting algorithm of median filtering is optimized according to the hardware structure features of FPGA. FPGA is used to acquire the data parallelly for comparing the data of the same column in the median filtering window. Comparing results shared by adjacent filter window are saved temporarily to match the new round of median filtering by using FPGA internal resources. This method can reduce the comparing times from current 21 down to 13, and improve the algorithm efficiency nearly 40%.The experimental results prove that the optimized algorithm can filter a 1K×1K gray-level image in about 20ms, which ensure the proposed algorithm can be applied in the real-time image median filtering system.

ACKNOWLEDGEMENT

The satisfaction and euphoria that accompanies the successful completion of any task would be incomplete without the mention of the people who made it possible and whose constant encouragement and guidance has been a source of inspiration throughout the course.

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CHAPTER-1

INTRODUCTION

1.1 OVERVIEW

Median filtering is a common nonlinear image smoothing technology that has unique characteristics. It does not use convolution to process the image with a kernel of coefficients. Rather, in each position of the kernel frame, a pixel of the input image contained in the frame is selected to become the output pixel located at the coordinates of the kernel center.

The main principle of Median Filter is that consider each pixel in the image as the center, build an odd number of samples (3 × 3, 5 × 5, 7 × 7, etc.) observation window around its neighboring area, sort the gray value of each point, and then use the median value instead of the original value. The key of the median filtering algorithm is to sort the value of each pixel in the observation window to obtain the median value. The traditional median filtering algorithm is bubble algorithm, whose main purpose is comparing all data with each other to make an order. The whole processing need 36 times comparisons totally. Using this method, the hardware resource occupancy rate is high, and the processing cost is huge, it can hardly to be used in a practical engineering system.

This project introduces a real-time median filtering using pipelining processing technology according to the FPGA's work characteristics, which improved approximately 40% efficiency than Xu Da-peng's fast filtering algorithm. The proposed algorithm greatly decreases the amount of sorting, reduces the hardware resources consumption. Therefore, this algorithm has a good real-time performance even when dealing with high-resolution images.

1.2 PROBLEM STATEMENT

In the image processing system, due to imaging systems, signal transmission,

working environment and other external conditions, there would inevitably produce many kinds of noise, resulting in lower image quality. Thereby, noise can affect the effects and accuracy of subsequent image processing. To reduce this influence, we usually try the best to reduce the noise before further processing.

1.3 MOTIVATION

In recent years, many median filtering methods have been raised[3][4][5], but the real-time issue is still difficult to be solved. Xu Da-peng [6] raised a fast median filtering algorithm based on FPGA, which requires a total of 21 times comparisons. It's resource utilization and computational speed has been raised compared to the traditional method. This method can work in some common condition practicality, but when it meet to the high-resolution images (for example, 1k × 1K image) it's still hard to realize the real-time noise reducing.

Seeing all these problems we realized that we require a real time median filtering using pipelining processing technology according to FPGA's work characteristics.

CHAPTER -2

LITERATURE SURVEY

[1] Research on Image Median Filtering Algorithm and Its FPGA Implementation.

Yueli Hu says in the paper [1] "**Research on Image Median Filtering Algorithm and Its FPGA Implementation**" that image filtering plays an important role in image preprocessing. The median filters, including the standard median filter and the multi-level median filter, which can preserve image features and thin lines are introduced and discussed in detail. After that, the FPGA based solution for the algorithms of these two filters are presented. This paper also gives account to the FPGA implementation of the complete structure of a general filter including the filtering window generating module and the row-column counting module. RTL level simulation is performed in Modelsim to verify the functional correctness and system level simulation is performed in MATLAB to compare the filtering effect.

[2] J.W Tukey,"Nonlinear (Non Superposable) Methods for Smoothing Data", Proceedings of Congress Record EASCON Washington DC, 7-9 October 1974

Wanzhou Ye and Zhao Liao say in the journal "**Open Journal of Discrete Mathematics**, Vol.2 No.3, July 18, 2012" that the generalized correlativity of input signal and output signal of a stack filtering operator is defined and used for numerously measuring these filtering operators' behavior in removing noise in signals. We show that under the criterion of the generalized correlativity, of stack filtering operators the median filtering operator is optimal, which implies that this filtering operator possesses better filtering behavior than the others.

[3] JIANG Bo, HUANG Wei. Adaptive Threshold Median Filter for Multiple-Impulse Noise. Journal of Electronic Science and Technology of China 2007

Jiang Bo and Huang Wei say in their paper "**Adaptive Threshold Median Filter for Multiple-Impulse Noise**" that attenuating the noises plays an essential role in the image processing. Almost all the traditional median filters concern the

removal of impulse noise having a single layer, whose noise gray level value is constant. In this paper, a new adaptive median filter is proposed to handle those images corrupted not only by single layer noise. The adaptive threshold median filter(ATMF) has been developed by combining the adaptive median filter (AMF) and two dynamic thresholds. Because of the dynamic threshold being used, the ATMF is able to balance the removal of the multiple-impulse noise and the quality of image. Comparison of the proposed method with traditional median filters is provided. Some visual examples are given to demonstrate the performance of the proposed Filter.

[4] FPGA Implementation of Median Filter using an Improved Algorithm for Image Processing

To solve the contradiction between the noise reducing effect and the time complexity of the standard median filter algorithm, this paper proposed an improved median filter algorithm. This paper focuses on a 3x3 image window filtering in which the sorting network of the filter should be able to produce the desired result within the shortest time possible. That means, the sorting network will be able to exercise parallelism in processing the image pixel and the number of the required hardware maintained minimal. The algorithm derived shows that the sorting network will be able to produce the result within the required time. The improved filter algorithm was implemented using Hardware Description Language Verilog, simulated using Xilinx isim and was loaded on to Xilinx FPGA. The hardware result showed that this proposed algorithm has better output result as compared to standard median algorithm as well as adaptive median algorithm. It has a good application prospect in real-time image processing.

CHAPTER -3
METHODOLOGY

The sort optimization methodology consists of two section Xilinx and MATLAB simulation.

3.1 Xilinx :

The first step is to write the VHDL code in the ISE design Suite 14.5 and compile it. Then we include individual components to the top module and generate a test bench to it. After this we get the simulation result for our program in the ISE simulator window.

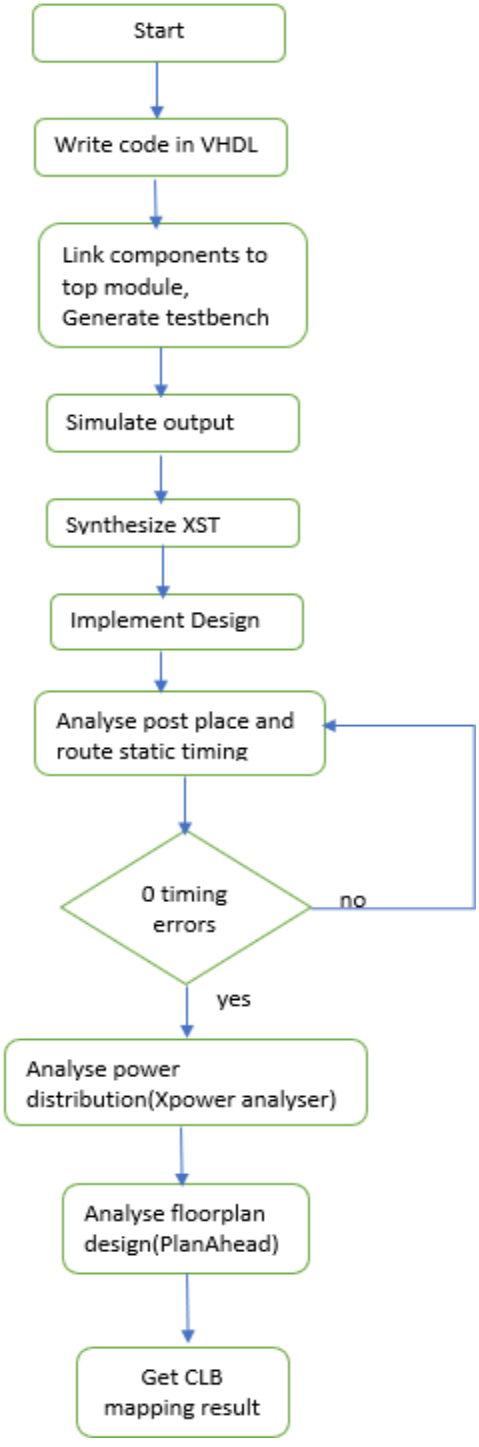
We test the code in various aspects and characteristics required for a proper circuit design. i.e Implement design, Analyzing static timing constraints, Analyzing power and Area occupied by the logic blocks in the FPGA. After every design constraint is verified, we then get the place and route design for our model.

3.2 Simulink Methodology (MATLAB) :

We use MATLAB 2012Ra as it is the only version that is compatible for running Xilinx blocks for simulation. The first step is to open the Simulink and open a new model. We include all the required block sets into the model and connect them accordingly.

Dump the VHDL code into the Blackbox.

After manipulating individual block sets according to requirements input the noisy image and run the Simulink model. We get the output image clear from noise.



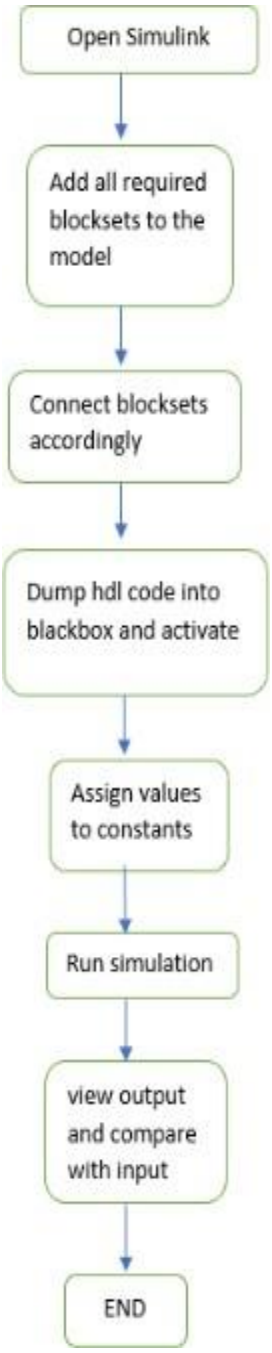


Fig (i). Xilinx Fig (ii). Simulink Methodology (MATLAB)

3.3 Proposed System:

In recent years, many median filtering methods have been raised[3][4][5], but the real-time issue is still difficult to be solved. Xu Da-peng [6] raised a fast median filtering algorithm based on FPGA, which requires a total of 21 times comparisons. Its resource utilization and computational speed has been raised compared to the traditional method. This method can work in some common condition practicality, but when it meet to the high-resolution images (for example, 1k × 1K image) it still hard to realize the real-time noise reducing. This paper introduces a real-time median filtering using pipelining processing technology according to the FPGA's work characteristics, which improved approximately 40% efficiency than Xu Da-peng's fast filtering algorithm. The proposed algorithm greatly decreases the amount of sorting, reduces the hardware resources consumption. Therefore, this algorithm has a good real-time performance even when dealing with high-resolution images.

CHAPTER -4

HARDWARE IMPLEMENTATION / SIMULATION

4.1 Sort Optimization:

The formula of median filtering can be expressed as:

G (x,y) = med f [(x-i) , (y-j)] , I , k ∈ W .....(1)

f (x, y) and g(x,y) represent for the original image and the filtered image respectively. W is a two-dimensional template, usually is 3 × 3, 5 × 5 region.

We supposed to do the 3 × 3 median filter for a 1k × 1k image. According to the work characteristics of FPGA and the transmission way of the image data, we can get the following image processing sequence:

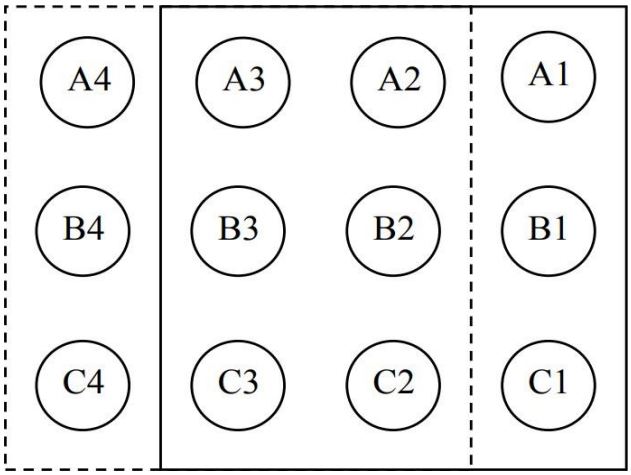


Fig 1. The sequence of Image Data Processing

In figure 1, A, B, C represent for the data of 3 different adjacent lines of the image respectively. The data in the real–line square is currently processing data and the data in the dashed square is the data will be processed in the next circle. It is easy to find out that there is 6 common data between the two processing circle. Hence, some parts of the current result can be utilized to the next processing for computation reduction.

First, we must sort the data by column. We need to do 9 comparisons to get the following result, we assume the result is:

A1>B1>C1

A2>B2>C2

A3>B3 >C3

Secondly, we need to find the maxim data in C 1, C2 and C3 by doing 2 comparisons, and find the minimum data in A1, A2 and A3 by doing 2 comparisons, and find the median data in B1, B2 and B3 by doing 3 comparisons. The formula is as following:

Amin = min (A1, A2, A3)

Bmed = med (B1, B2, B3)

Cmax = max (C1, C2, C3).....(2)

Lastly, we need to find the median data in Amin, Bmed and Cmax by doing 3 comparisons.

Fmed = med（Amin，Bmed，Cmax).....(3)

The resulted Fmed is the final result. In the next circle, the comparison results of （A2，B2，C2） and （A3，B3，C3）have been obtained, we only need to seek the sorting of the updating data A4, B4, C4, and then use (2) and (3) to calculate the required median. Obviously, in each next processing cycle, only one column data need to be sorted. According to that, the comparison times can be reduced from the original 21 down to 13, and the system's operating efficiency can be greatly improved.

4.2 Hardware implementation

The proposed algorithm is executed as the image pre-processing module on FPGA. In our project the filter is designed as 3x3 filter kernel. According to that, we need to save temporary data in 3 lines, which are line n-1, line n and line n+1. We can define 3 first input first output (FIFO) memory to store these data. When the data of line n have been processed, we drop the data of line n-1 and acquire the data of line n+2 to begin a new round processing.

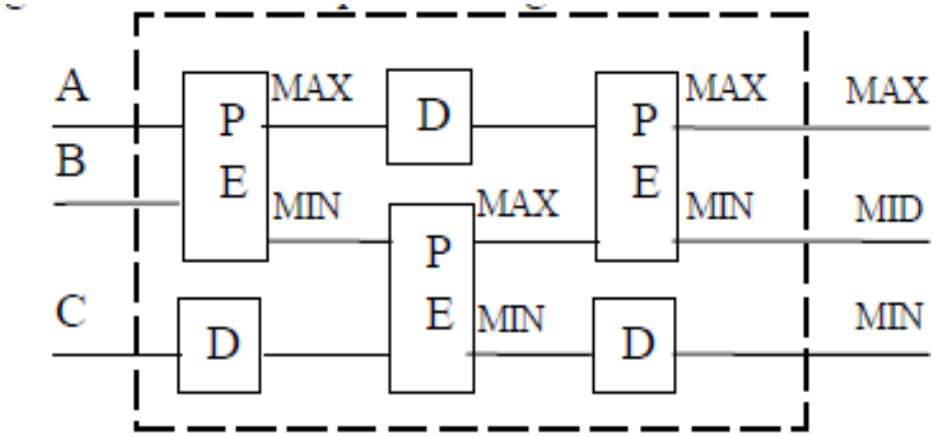


Figure 2(a) Ordering Comparator

Fig 2(a) .Ordering Comparator

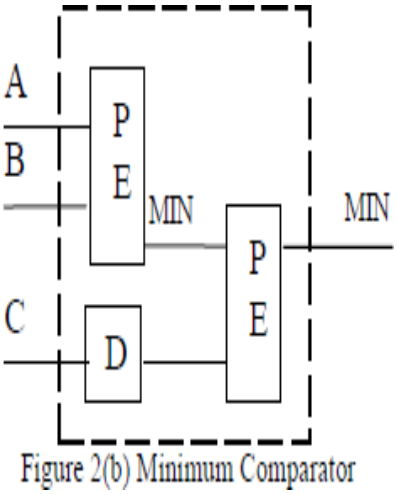


Figure 2(b) Minimum Comparator

Fig 2(b) Minimum Comparator

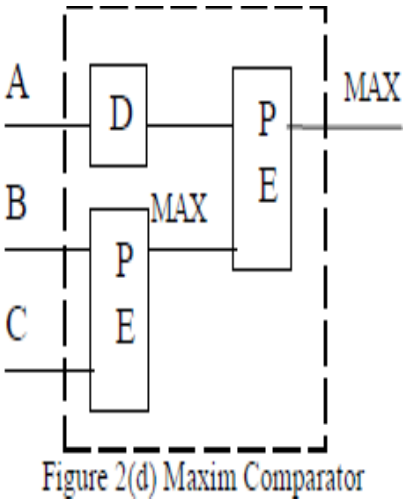


Figure 2(d) Maxim Comparator

Fig 2(d) Maxim Comparator

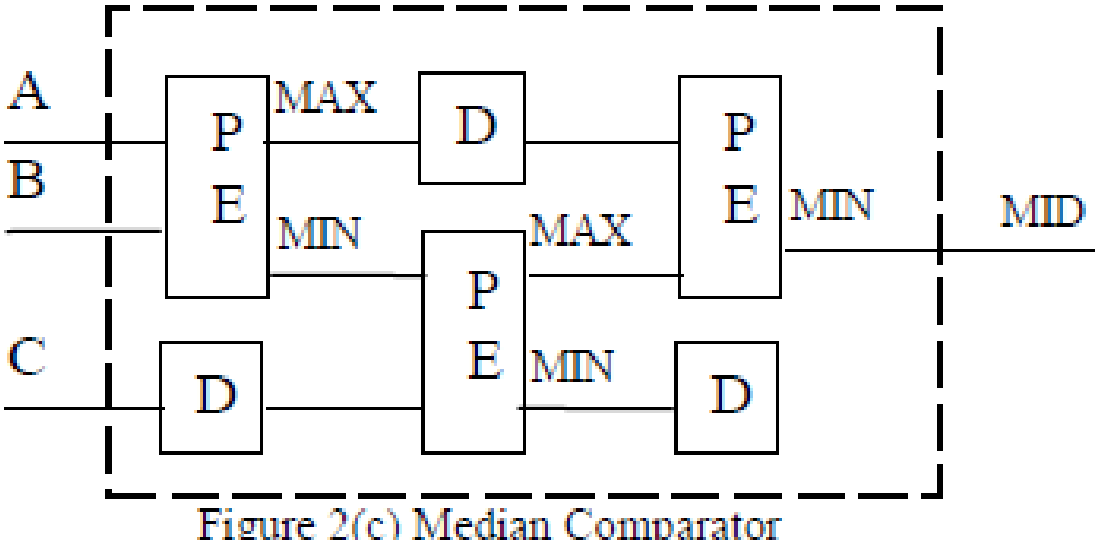


Figure 2(c) Median Comparator

Fig 2(c) Median Comparator

Because we can get the maxim value or the minimum value of 3 data by doing 2 comparisons, and get the median value or the ordering of 3 data by doing 3 comparisons, we designed 4 different comparators, such as ordering comparator, minimum comparator, median comparator and maxim comparator. The hardware structures of the 4 comparators are given in figure 2: In figure 2, the processing element (PE) is basic processing unit, which is designed for comparing 2 input data. D stands for D flip-flop, whose function is to make a single-circle delay. It is used for synchronizing the calculation here. Because the proposed algorithm needs to storage two groups temporary data in current processing, we design two D flip-flops to realize this function. The hardware structure of this system is shown as following:

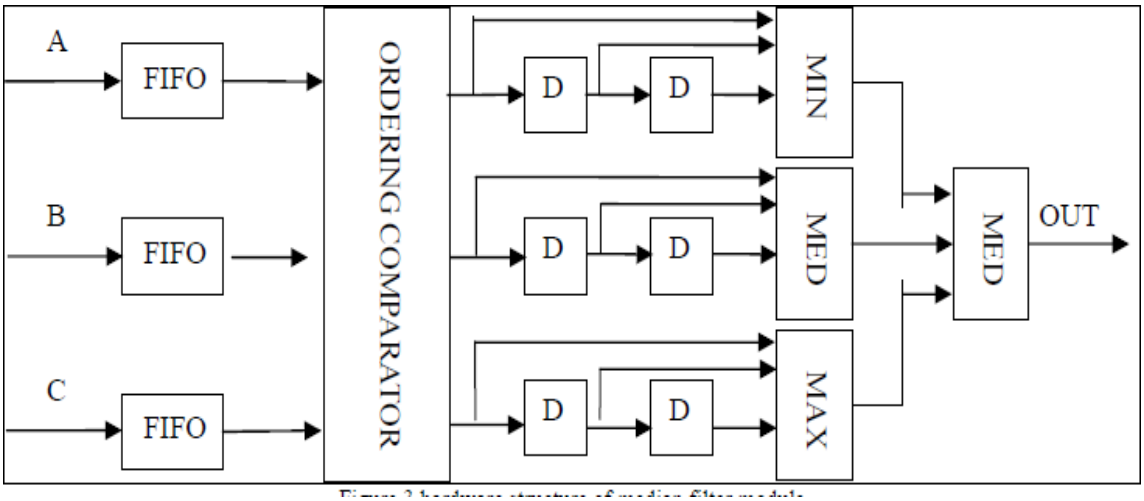


Fig 3 Hardware Structure of Median Filter Module

As shown in figure 3, the workflow of the median filtering module is that: firstly, three lines of data are wrote into the internal FIFO of FPGA, and when the third FIFO turn into half full state, the median filtering system begin to work. The data in the 3 FIFO will be sent to the ordering comparator ordinally for data ordering, and the results will be send to next different comparators. Before the second comparing, the data need 2 circle delay to distinguish the circle order of input data by two D flip-flops. The second comparing results will be sent to the final median comparator to get the final result.

CHAPTER – 5

RESULT AND DISCUSSIONS

This experiment's hardware environment is a self-built circuit board, the software environment is based on the **ISE Design Suite 14.5** software. The FPGA used in system is Altera's Cyclone II FPGA chip, EP2C20, whose main frequency is 50MHz. The experiment's target image is a 1024 × 1024 × 8bits image. Under ISE Design Suite 14.5 software simulating, timing simulation result is shown in below figures, it shows that the median filter program operated on the FPGA runs in a pipelining way. Each clock cycle the FPGA completes a median filtering calculation of a pixel. The main frequency of the FPGA is 50MHz, so every 20ns the FPGA completes a median filtering calculation of a pixel. For a 1024 × 1024 image, the processing time cost is about 20ns × 1000 × 1000 = 20ms, and the time required for processing 25 images is about 20ms × 25 = 500ms = 0.5s. It is obvious that the algorithm can achieve the real-time processing.

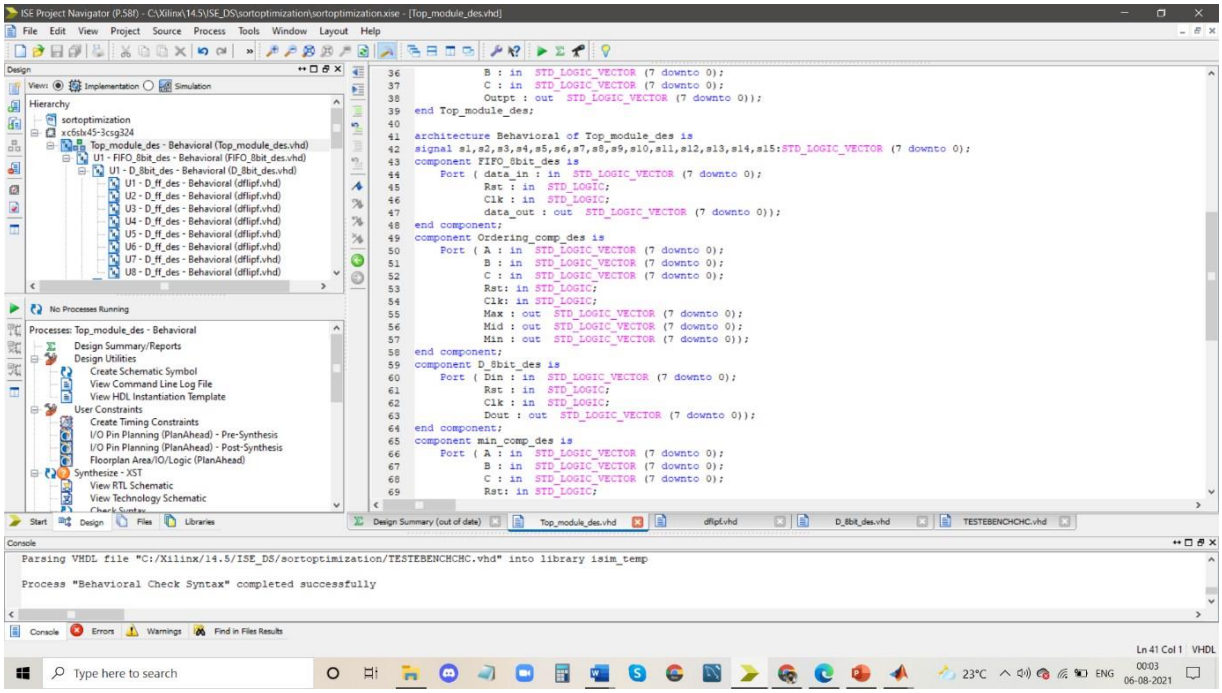


Fig 4: Sort Optimisation Top module designed in VHDL on thr ISE design suite 14.5

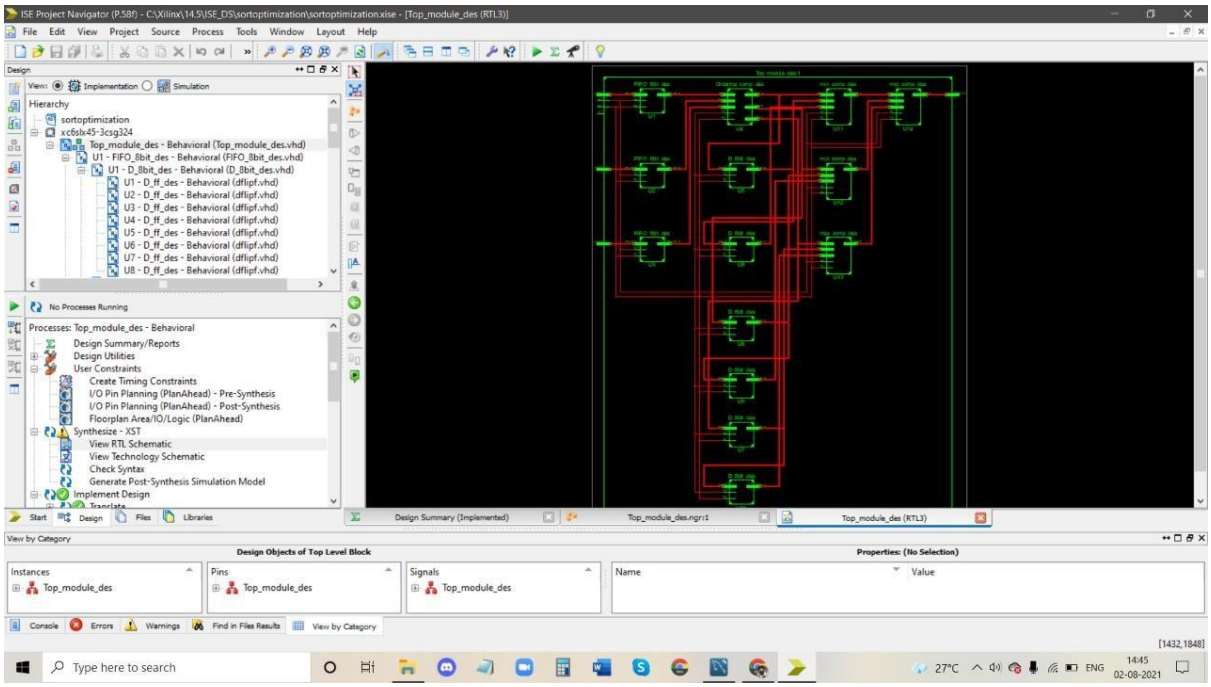


Fig 5: Sort optimisation RTL schematic showing connections between individual components

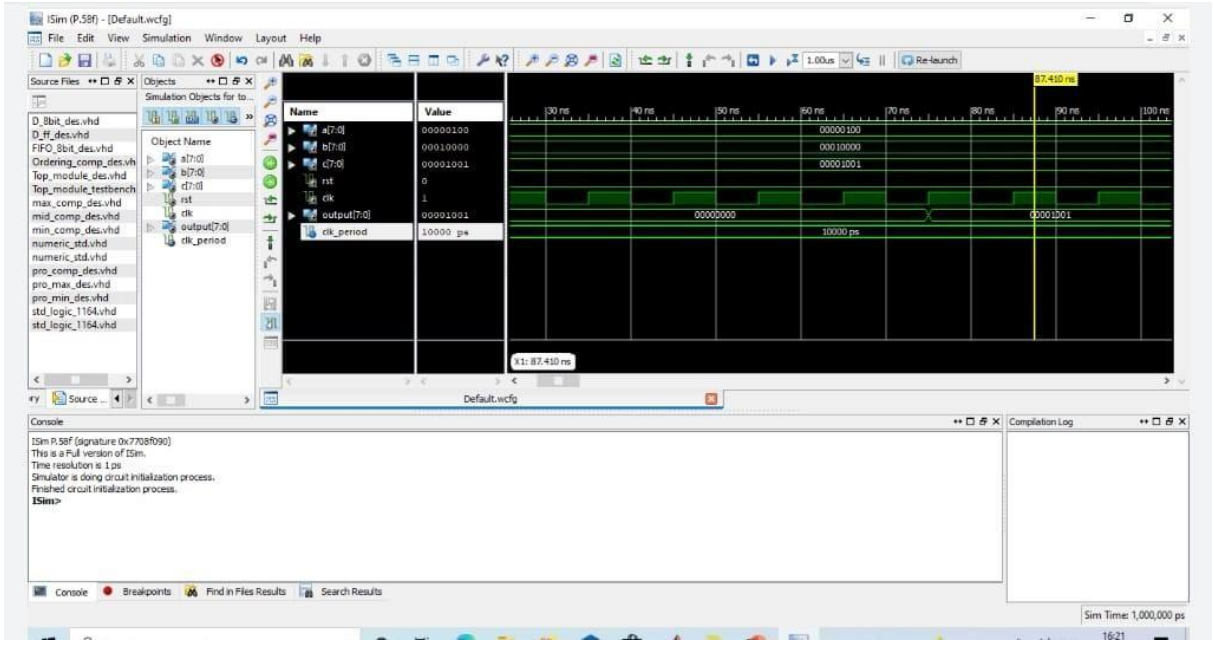


Fig 6: Simulation window

```
Timing summary:
---------------

Timing errors: 0  Score: 0  (Setup/Max: 0, Hold: 0)

Constraints cover 2040262197 paths, 0 nets, and 2137 connections

Design statistics:
   Minimum period:  12.387ns{1}   (Maximum frequency:  80.730MHz)
   Minimum input required time before clock:   3.048ns
   Minimum output required time after clock:  26.851ns


------------------------------------Footnotes-----------------------------------
1)  The minimum period statistic assumes all single cycle delays.

Analysis completed Mon Aug 02 14:44:09 2021
--------------------------------------------------------------------------------

Trace Settings:
-------------------------
Trace Settings

Peak Memory Usage: 4607 MB
```

```
================================================================================
Timing constraint: TS_clk = PERIOD TIMEGRP "Clk" 13 ns HIGH 7 ns;
For more information, see Period Analysis in the Timing Closure User Guide (UG612).
 26558981 paths analysed, 339 endpoints analysed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors, 0 component switching limit errors)
 Minimum period is  12.387ns.
--------------------------------------------------------------------------------
```

Fig 7: Timing summary and timing constraints

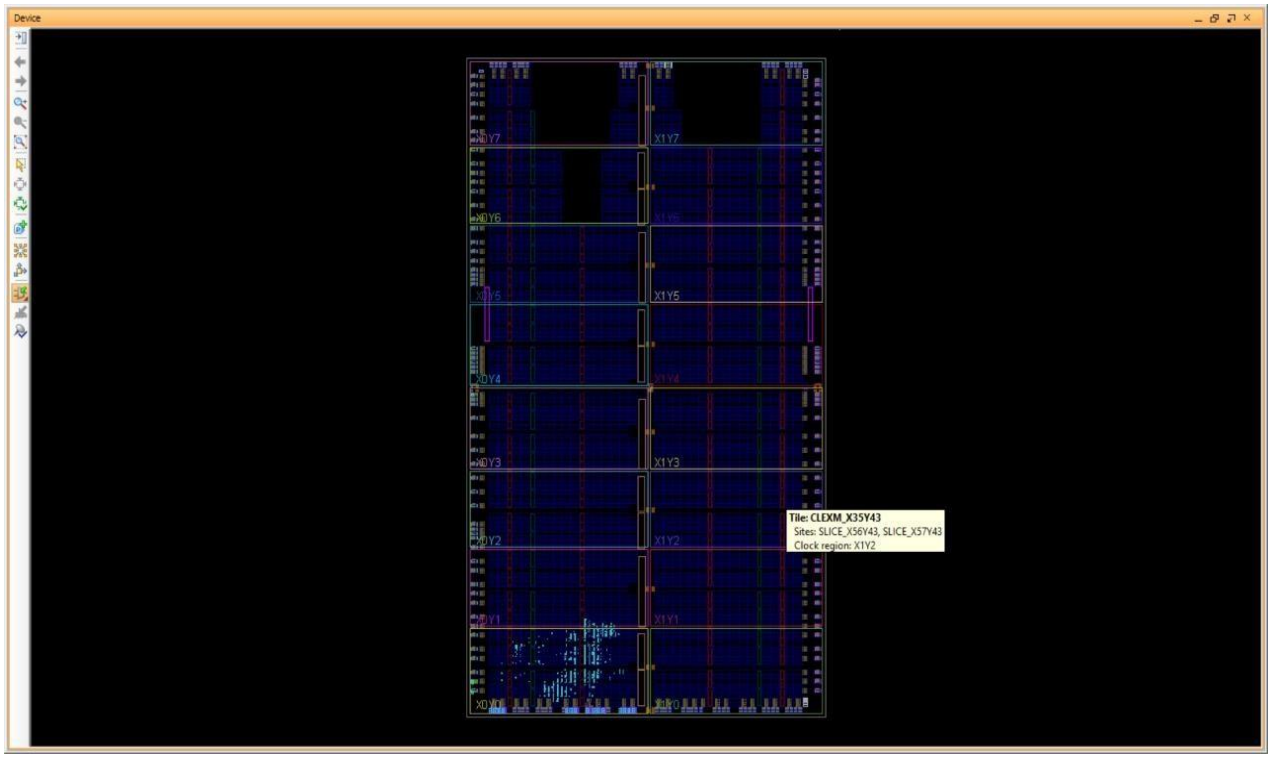


Fig 8: Place and route results. Blue dots show logic block mapping on fpga

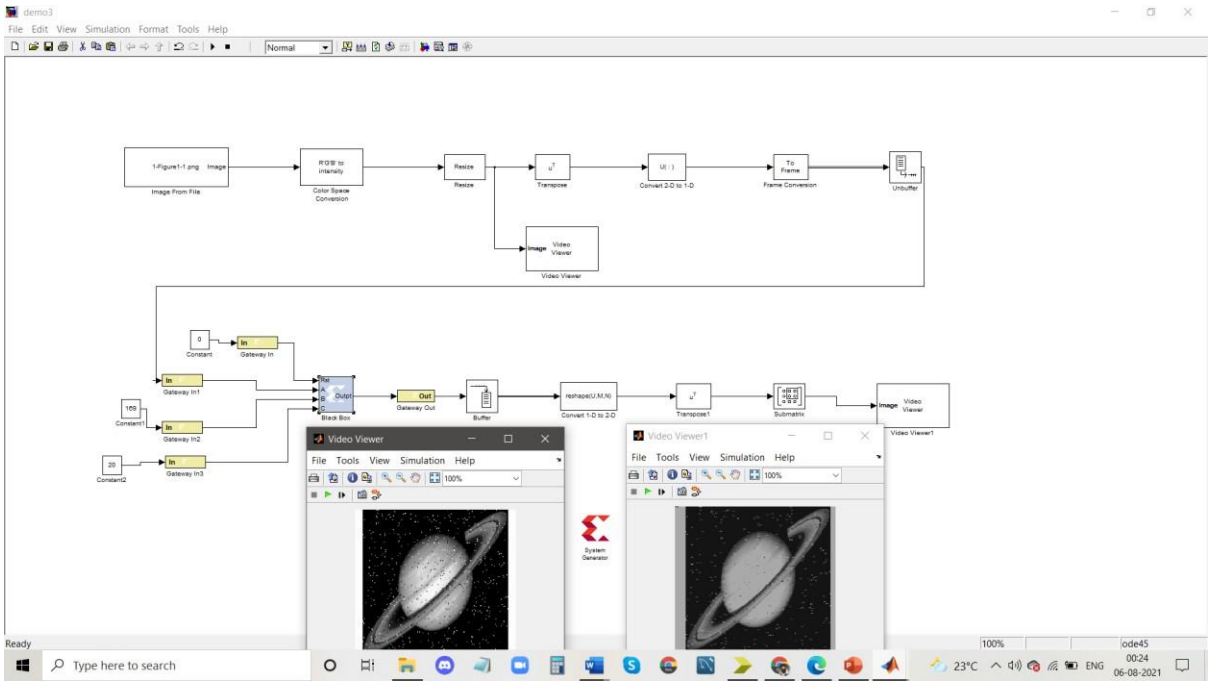


Fig 9: Simulink model showing various blocksets included into the model for simulation of output. Video viewer and video viewer1 show input Gray image with noise and clear image respectively

Figure 5(a) Original image

Fig 10(a) : Original image filled with salt and pepper noise

Figure 5(b) Processed image

Fig 10(b): Output image from the median filter.

5.1 Advantages

1. The median filter is normally used to reduce noise in an image, somewhat like the mean filter. However, it often does a better job than the mean filter of preserving useful detail in the image.
2. The median is a more robust average than the mean and so a single very unrepresentative pixel in a neighbourhood will not affect the median value significantly.
3. Since the median value must actually be the value of one of the pixels in the neighbourhood, the median filter does not create new unrealistic pixel values when the filter straddles an edge. For this reason the median filter is much better at preserving sharp edges than the mean filter.

5.2 Disadvantages:

1. Median filtering is a non-linear filtering technique which is sometimes useful as it can preserve sharp features (e.g. lines) in an image whilst filtering noise.
2. The disadvantage is that it is difficult to treat analytically the effect of a median filter. There is no error propagation.
3. Efficiency is just 80%. Hence it is not suitable to remove fine noises in the image.

5.3 Applications:

1. Median filter is the most common method of clearing image noise. This paper proposes improved algorithm of median filter to remove sale and pepper noise of image.
2. Median filtering is useful in reducing noise while preserving signal jumps. The extent of the noise reduction depends on the noise distribution. The heavier the distribution tail, the better the filter performs in reducing noise.
3. Matlab experiments show that improved median filter can greatly reduce the time of clears image noise and it performs better than median filters on noise reduction while retaining edges of an image.

CHAPTER – 6

CONCLUSION

This paper introduces a real-time image median filter based on FPGA structure. The proposed system has good real-time performance and extensibility. The Simulink model results are accurate with almost 80% noise correct compared to input image. Taking up a project in the field of electronics and communication and specifically in the VLSI domain we are currently studying made us better learners of the subject, its importance in the current technological developments and overall applications of the same around the world. It makes us feel proud as engineering students to contribute something towards the society and wish to continue to embark on the successful completion of this project.

6.1 Future Scope:

It can be connected with the DSP to process more complex and larger images. Because the system occupation is small and leave more resources to help DSP for image pre-processing, the future image processing system can run more efficiently.

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