Design of BGR for VCSEL Current Driver for CSAC in CMOS 90nm
BTP Presentation (CP302)

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CSAC Introduction

A **Chip-Scale Atomic Clock (CSAC)** is a miniaturized atomic clock that provides highly accurate timekeeping in a compact, low-power package.
It is based on atomic resonance principles including *coherent population trapping* (CPT) techniques. CSACs are widely used in applications where precise timing is essential, such as GPS-denied navigation, secure communications, and scientific measurements.

Desired Characteristics of CSAC

1. **High Accuracy** – Provides precise timekeeping with minimal drift, featuring a frequency stability of 2.2×10^{-12} over 10^5 seconds.
2. **Miniaturized Size** – Compact form factor, suitable for portable and embedded systems, with a volume as small as 15 cm^3.
3. **Low Power Consumption** –Operates with very low power, consuming up to 59.9 mW.
4. **Resistance to Environmental Factors** – Performs reliably under varying temperatures, vibrations, and electromagnetic conditions.

Reference: H. Zhang et al., “Ultra-Low-Power Atomic Clock for Satellite Constellation Using Cesium CPT,” ISSCC, 2019, pp. 462–464

Performance Edge of CSAC over Traditional Methods

Chip-Scale Atomic Clocks (CSACs) use quantum atomic resonance, locking frequency to the fundamental atomic transition of **Cs-133** at **9.192631770 GHz** [4], unlike Quartz/MEMS which rely on *mechanical vibrations prone to drift from aging, temperature, and stress*.

Atomic transitions offer an intrinsically stable reference with high Q-factor, resulting in much lower short-term frequency noise and **Allan deviation (ADEV) values around 6.8786×10^{-12}** [4], compared to quartz oscillators' 10^{-9} to 10^{-8}. CSACs also achieve ultra-low size and power consumption (under 100 mW and 10–20 cm^3), making them 10–50 times more power-efficient and 5–50 times smaller than traditional rubidium clocks [5].

Reference:[3] H. Zhang et al., “Ultra-Low-Power Atomic Clock for Satellite Constellation Using Cesium CPT,” ISSCC, 2019, pp. 462–464

Architecture of CSAC

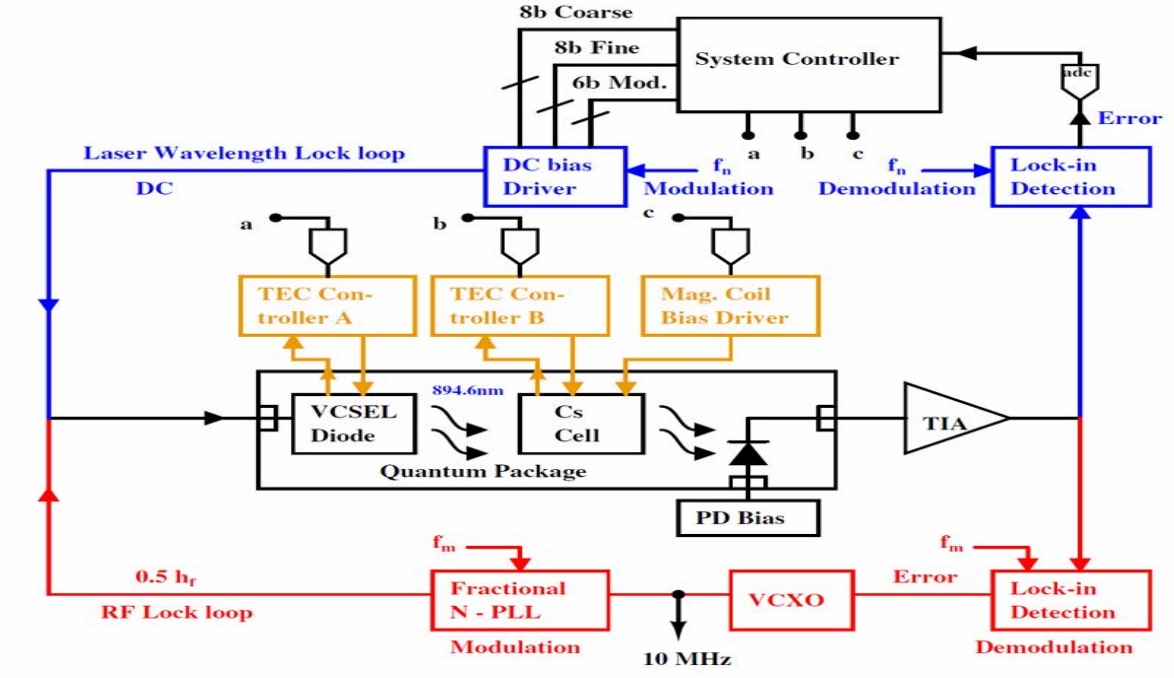


Fig.1 CSAC Architecture simplified block diagram

Reference: Azhar Yaseen, “Chip Scale Atomic Clock - Architecture Technical Report” [unpublished manuscript as on 27th November 2025]

VCSEL Driver modulated waves from CP301

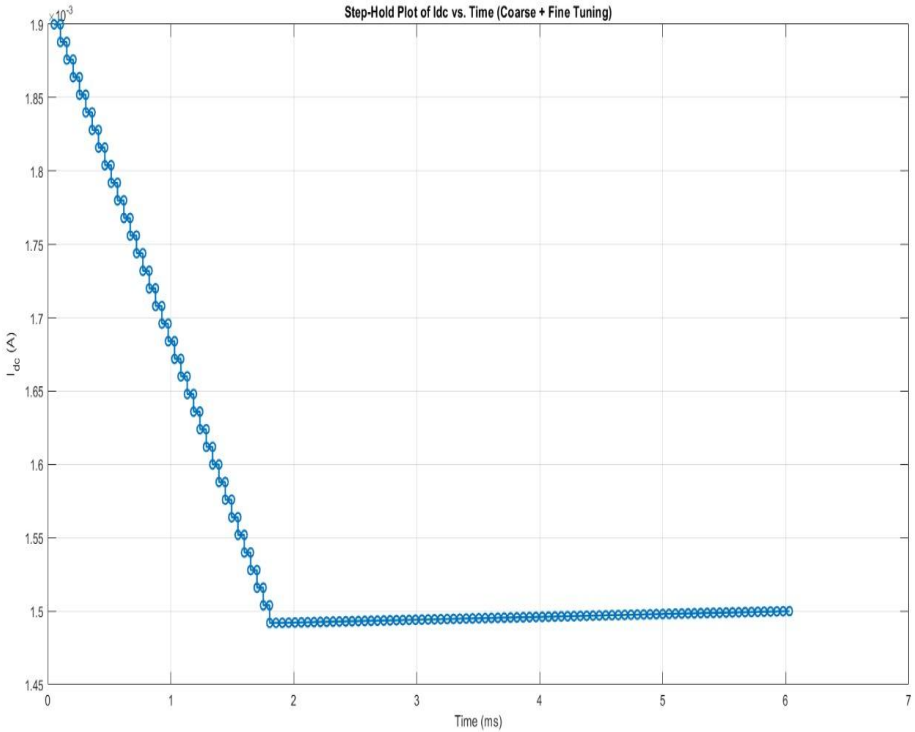


Fig.2 MATLAB simulation of I_{DC} with time as each loop iterates

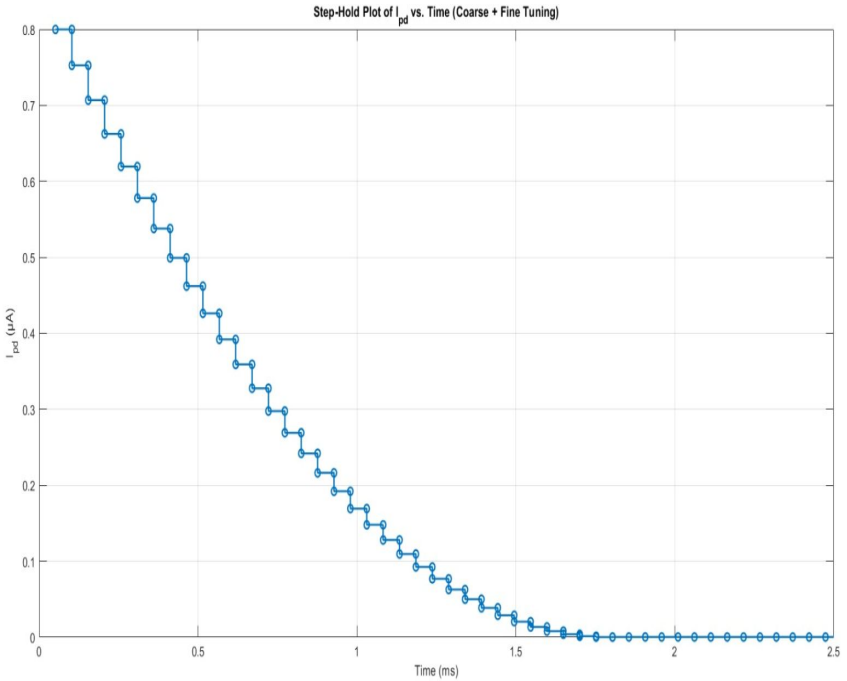


Fig.3 MATLAB simulation of I_{PD} with time as each loop iterates

$$I_{PD} = 5(I_{DC}\text{-}1.5mA)^2$$

Need of Biasing Voltage for Current Mirror Banks

- Current-mirror banks generate ultra-precise currents on the order of μA. Without a stable bias voltage, external temperature variations shift the transistor operating point and induce significant current errors.
- A bandgap reference provides a constant, temperature-independent voltage. This ensures that all current-mirror branches operate invariant to temperature fluctuations.
- As a result, the circuit produces reliable, stable, and accurate currents for VCSEL biasing and modulation.

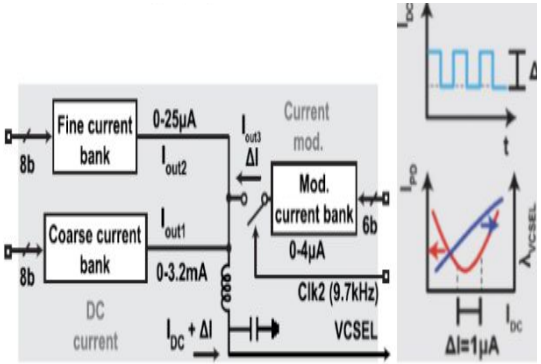
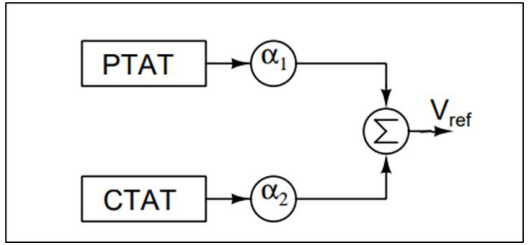


Fig.4 Current Banks in System Controller

Need of BGR for Driver Module

A bandgap reference generates a stable output voltage that **remains nearly constant across temperature variations** by combining two complementary temperature coefficients.



The first term is a *proportional-to-absolute-temperature* (*PTAT*) voltage which increases with temperature. The second term is a *complementary-to-absolute-temperature (CTAT)* voltage , which decreases with temperature.

$$V_{ref} = a_1 V_{PTAT} + a_2 V_{CTAT}$$

By scaling and summing these terms, the ***overall temperature dependence can be nulled.***

We first implemented BGR as proposed in Banba et al., "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE JSSC*, 1999.

CTAT Circuit for H.Banba BGR

The voltage across the diode V_D is given by:

$$V_D = V_T \ln\left(\frac{I_0}{I_S}\right) \quad (1)$$

where

$$V_T = \frac{kT}{q}$$

is a PTAT voltage with

$$\frac{\partial V_T}{\partial T} = \frac{k}{q},$$

and I_S is the reverse saturation current given by:

$$I_S = bT^m \exp\left(\frac{-E_g}{kT}\right) \quad (2)$$

where b is a constant, $m = 1.5$, and E_g is the energy gap between the conduction and valence bands of silicon.

B. Razavi, "The bandgap reference: A circuit for all seasons," IEEE Solid-State Circuits Magazine [2]

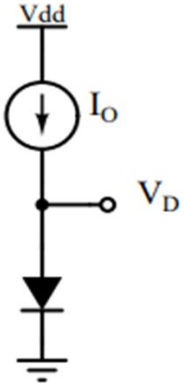


Fig.4 Diode CTAT Circuit [2]

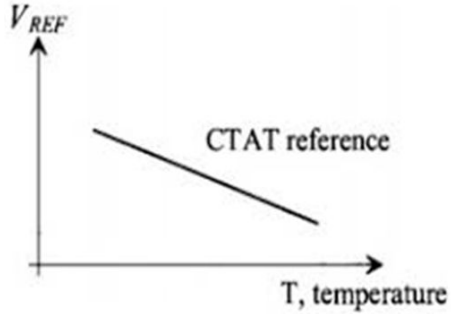


Fig.5 Typical CTAT Temperature profile

V_D has two temperature dependent components V_T and I_S. Let us first find the dependency of I_S on temperature:

$$\frac{1}{I_S}\frac{\partial I_S}{\partial T} = b\left[T^{m+1} + mT^m \exp\left(\frac{-E_g}{kT}\right)\right]\frac{E_g}{kT^2} \tag{3}$$

$$= \frac{I_S\left[(4+m)T + \frac{E_g}{k}\right]}{T^2} \tag{4}$$

Now to find the temperature dependency of V_D, differentiate equation (1) w.r.t T:

$$\frac{\partial V_D}{\partial T} = \frac{\partial V_T}{\partial T}\ln\left(\frac{I_0}{I_S}\right) + V_T\frac{\partial}{\partial T}\ln\left(\frac{I_0}{I_S}\right) \tag{5}$$

$$= \frac{k}{q}\ln\left(\frac{I_0}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} \tag{6}$$

$$= \frac{V_T}{T}\ln\left(\frac{I_0}{I_S}\right) - \frac{V_T}{T}\left[(4+m) + \frac{E_g}{kT}\right] \tag{7}$$

$$= \frac{V_D}{T} - \frac{V_T}{T}\left[(4+m) - \frac{E_g}{qT}\right] \tag{8}$$

If we substitute typical values,

$$\frac{\partial V_D}{\partial T} \approx -2.75\ \text{mV/K}.$$

Reference[1]]:B. Razavi,“The bandgap reference: A circuit for all seasons,” *IEEE Solid-State Circuits Magazine[2]*

PTAT Circuit for Banba BGR

The current in a multiple-diodes circuit is given by

$$I_0 = nI = nI_S \exp\left(\frac{V_{D1}}{V_T}\right).$$

Hence, the voltage across the parallel diodes is

$$V_{D1} = V_T \ln\left(\frac{I_0}{nI_S}\right).$$

If we subtract the voltage across a single diode from that across the parallel diodes, we get

$$V_D - V_{D1} = V_T\left(\ln\frac{I_0}{I_S} - \ln\frac{I_0}{nI_S}\right) = V_T \ln(n).$$

$$V_D = I_0 R_1 + V_{D1},$$

$$I_0 R_1 = V_D - V_{D1} = V_T \ln(n).$$

Thus, the **voltage across R_1 is a PTAT voltage**.

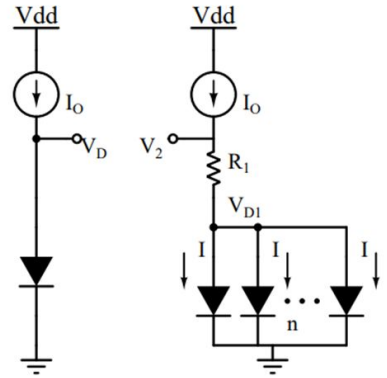


Fig.6 PTAT Circuit [1]

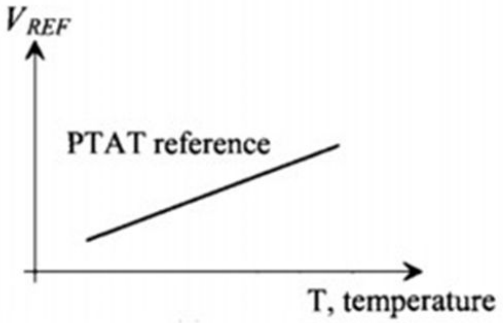


Fig.7 Typical PTAT Temperature profile

Reference: [1] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*

Bandgap Reference Circuit

An op-amp with equal resistances ($R_1 = R_2$) forces

$$V_a = V_b, \quad I_1 = I_2 = I_3.$$

Currents split as

$$I_{2a} = \frac{\Delta V_f}{R_3}, \quad I_{2b} = \frac{V_{f1}}{R_2},$$

where $\Delta V_f = V_{f1} - V_{f2} = V_T \ln N$. Thus

$$I_2 = I_{2a} + I_{2b}, \quad I_3 = I_2.$$

The output reference voltage is

$$V_{\text{ref}} = R_4 \left(\frac{V_{f1}}{R_2} + \frac{\Delta V_f}{R_3} \right).$$

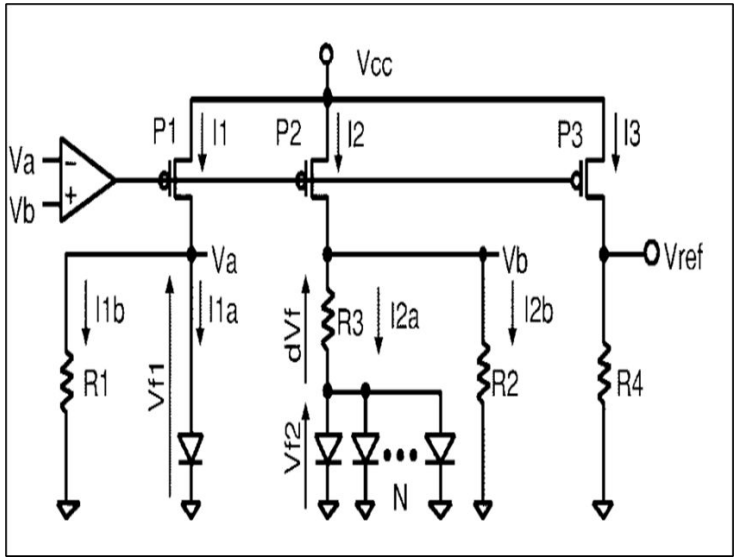


Fig.8 Bandgap Reference Circuit [1]

Reference: [1]H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*

CALCULATIONS

We assume the number of diodes $N = 10$ (in PTAT circuit). The voltage difference across the diodes is given by:

$$\Delta V_f = \frac{kT}{q} \ln N = \frac{kT}{q} \ln 10$$

The reference voltage expression is:

$$V_{\text{ref}} = R_4 \left(\frac{V_{f1}}{R_2} + \frac{\Delta V_f}{R_3} \right)$$

Taking the partial derivative with respect to temperature and setting it to zero for temperature independence:

$$\frac{\partial V_{\text{ref}}}{\partial T} = \frac{R_4}{R_2} \frac{\partial V_{f1}}{\partial T} + \frac{R_4}{R_3} \frac{\partial \Delta V_f}{\partial T} = 0 \quad \Rightarrow \quad \frac{\partial V_{f1}}{\partial T} = -\frac{R_2}{R_3} \frac{\partial \Delta V_f}{\partial T}$$

Substituting the known values:

$$-2.75 \times 10^{-3} = -\frac{R_2}{R_3} \left(\frac{k}{q} \ln 10 \right) \quad \Rightarrow \quad R_2 = 13.85 R_3$$

Let $R_2 = 1\ \text{k}\Omega$, then $R_3 = 72.21\ \Omega$. Since $R_1 = R_2$, therefore $R_1 = 1\ \text{k}\Omega$.

Plot of feedback voltages in Cadence

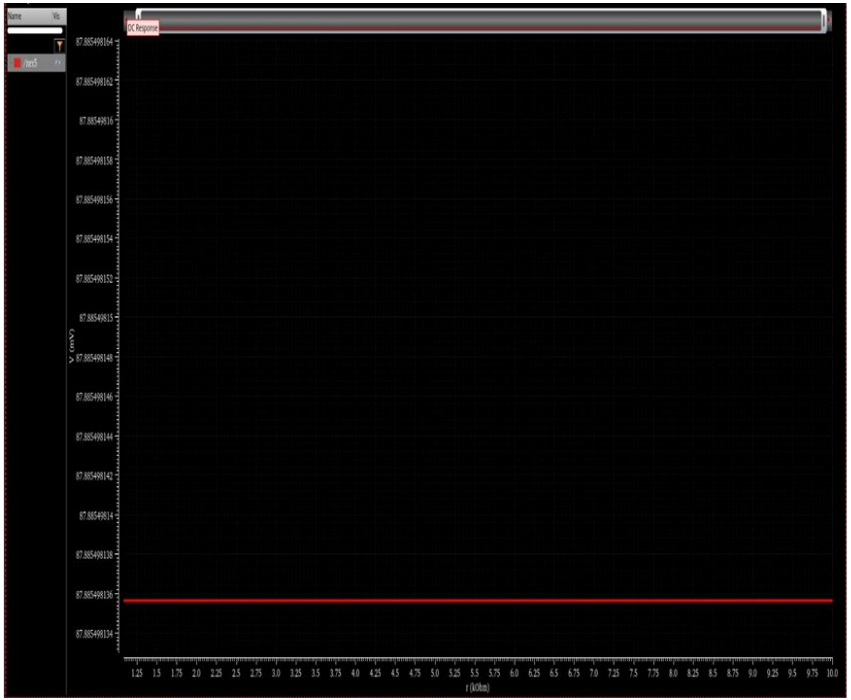


Fig.9 V_{f1} remains constant for R_4 varied from 1 kΩ to 10kΩ.

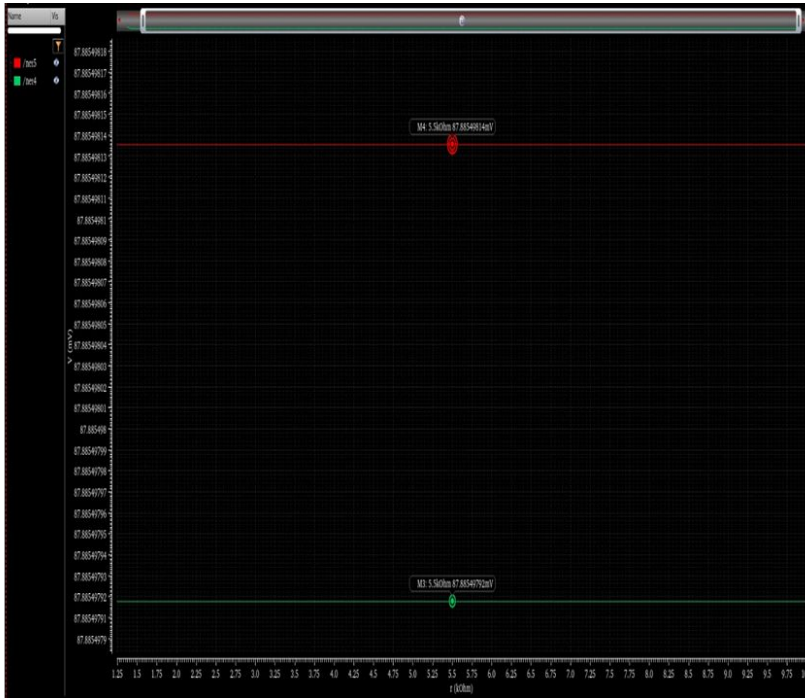


Fig 10. $V_{f1}(\text{net5}) - V_{f2}(\text{net4}) = \Delta V_f = 220\,\text{nV}$

From DC sweep of R_4, $\Delta V_f \approx 220\,\text{mV}$ (constant). The reference voltage equation:

$$R_4\left(\frac{V_{f1}}{R_2}+\frac{\Delta V_f}{R_3}\right)=V_{\text{ref}}$$

For $V_{\text{ref}} = 500\,\text{mV}$:

$$R_4\left(\frac{87.885\times10^{-3}}{1000}+\frac{220\times10^{-9}}{72.21}\right)=0.5$$

Solving: $R_4 = 6.14\,\text{k}\Omega$

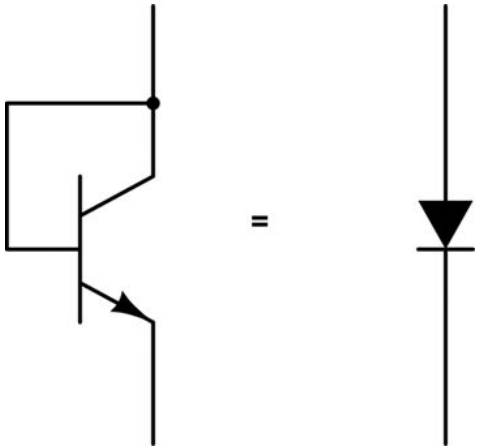


Fig.11 Diode connected BJT as a substitute to pn junction diode.

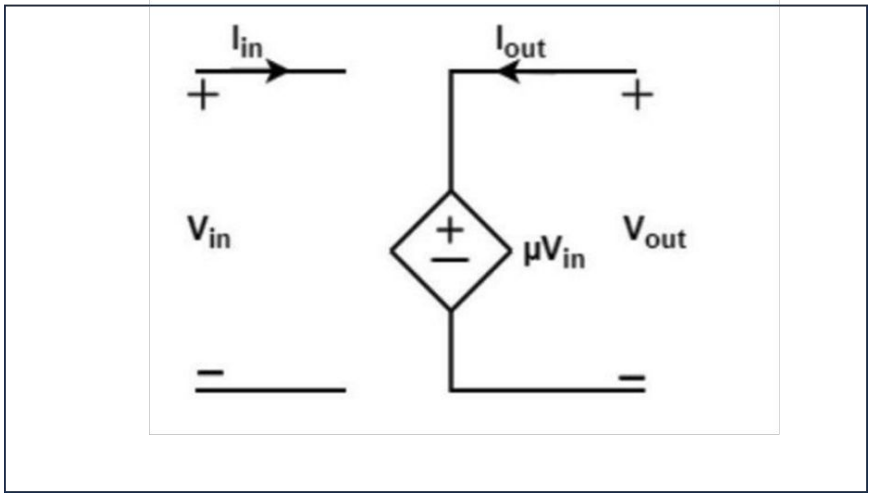
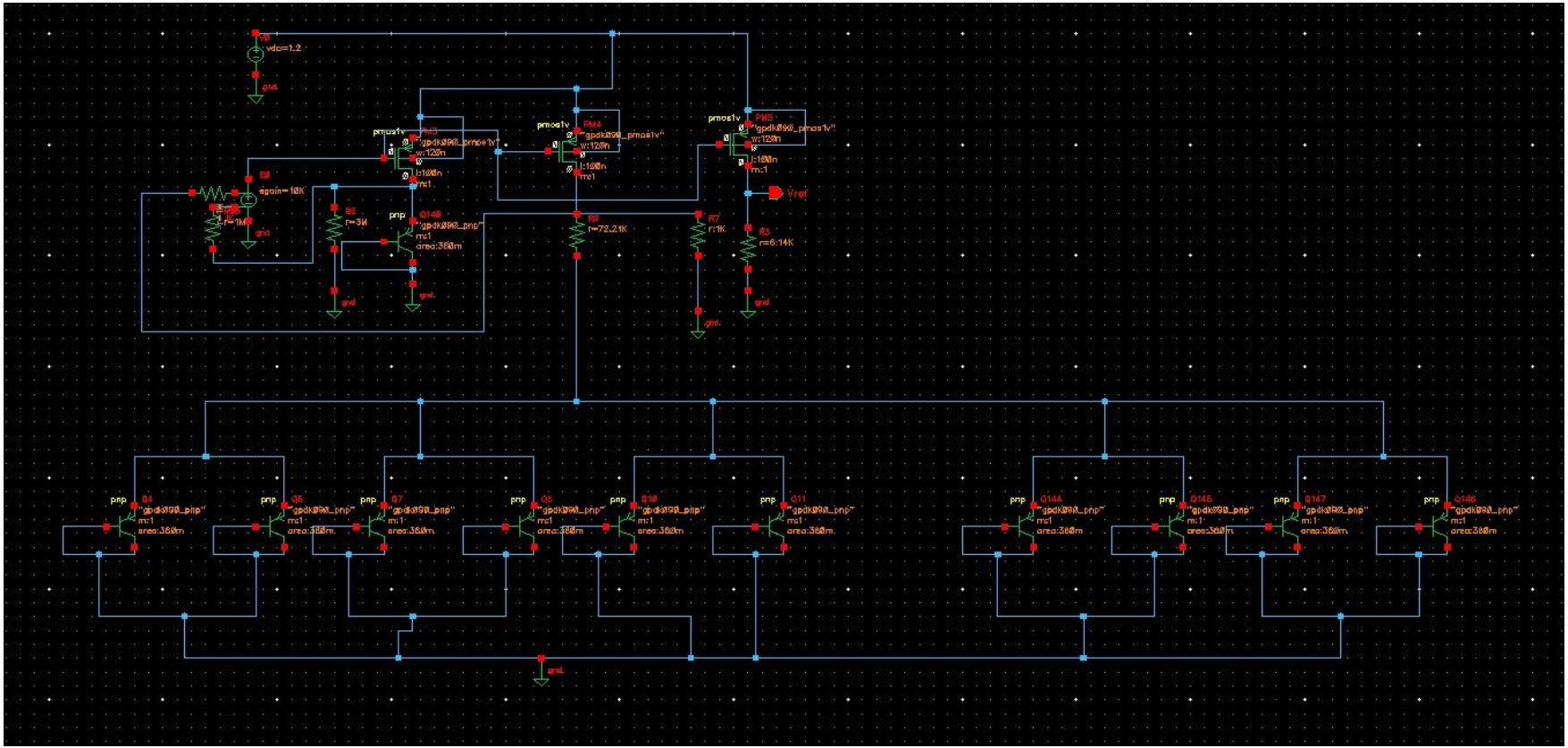


Fig.12 Ideal OP-Amp has been modelled as VCVS

We have taken a nominal gain of 40dB (i.e. 100V/V) for the op-amp

Schematic of BGR Circuit in Cadence



$$R_1 = R_2 = 1\,\mathrm{k}\Omega,\ R_3 = 72.21\,\Omega\ , R_4 = 6.14\,\mathrm{k}\Omega$$

Parametric Plot of Reference Voltage vs Supply Voltage

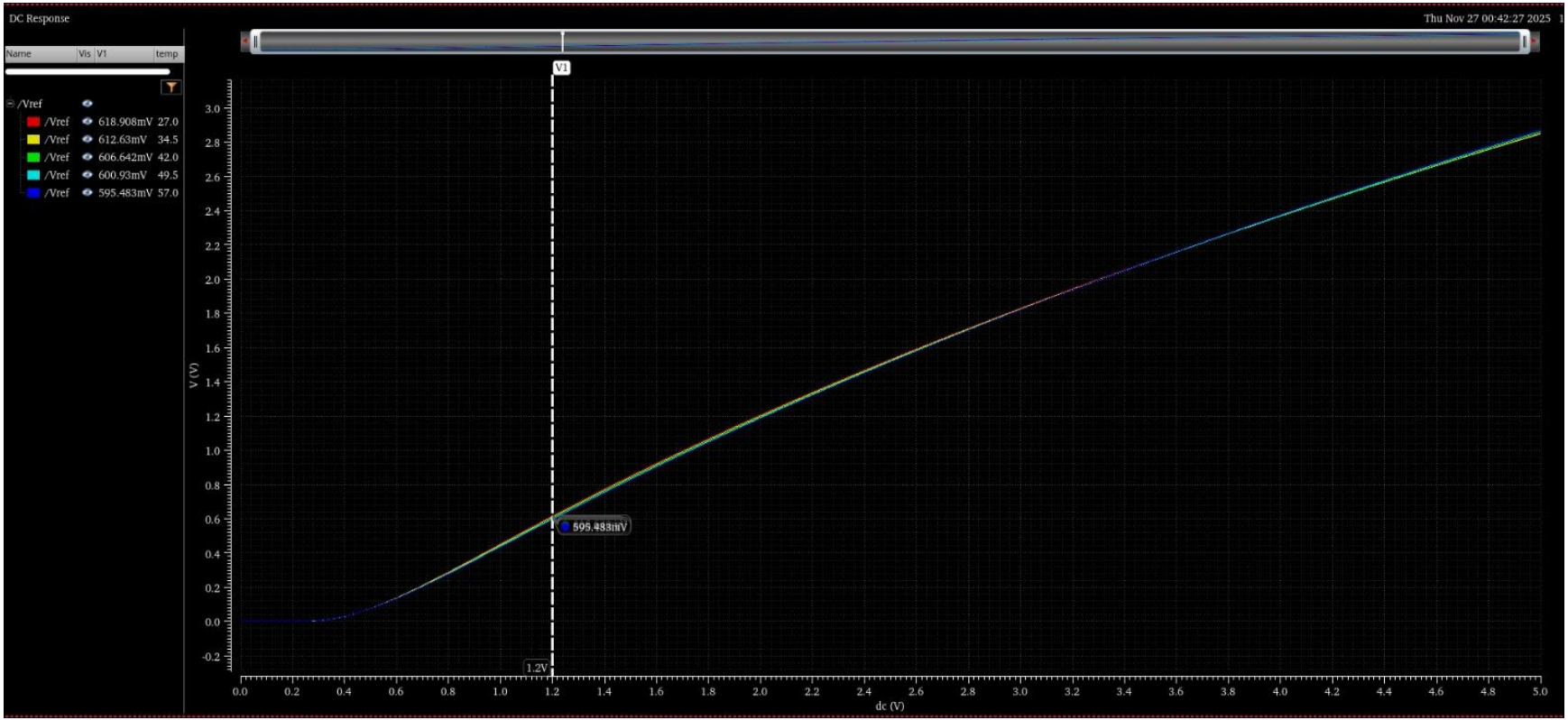


Fig.14 Supply voltage being varied from 0V to 5V. At Vcc = 1.2V, we have got a nominal value of 0.6V ***independent of temperature***

Temperature profile of BGR proposed by H. Banba[1]

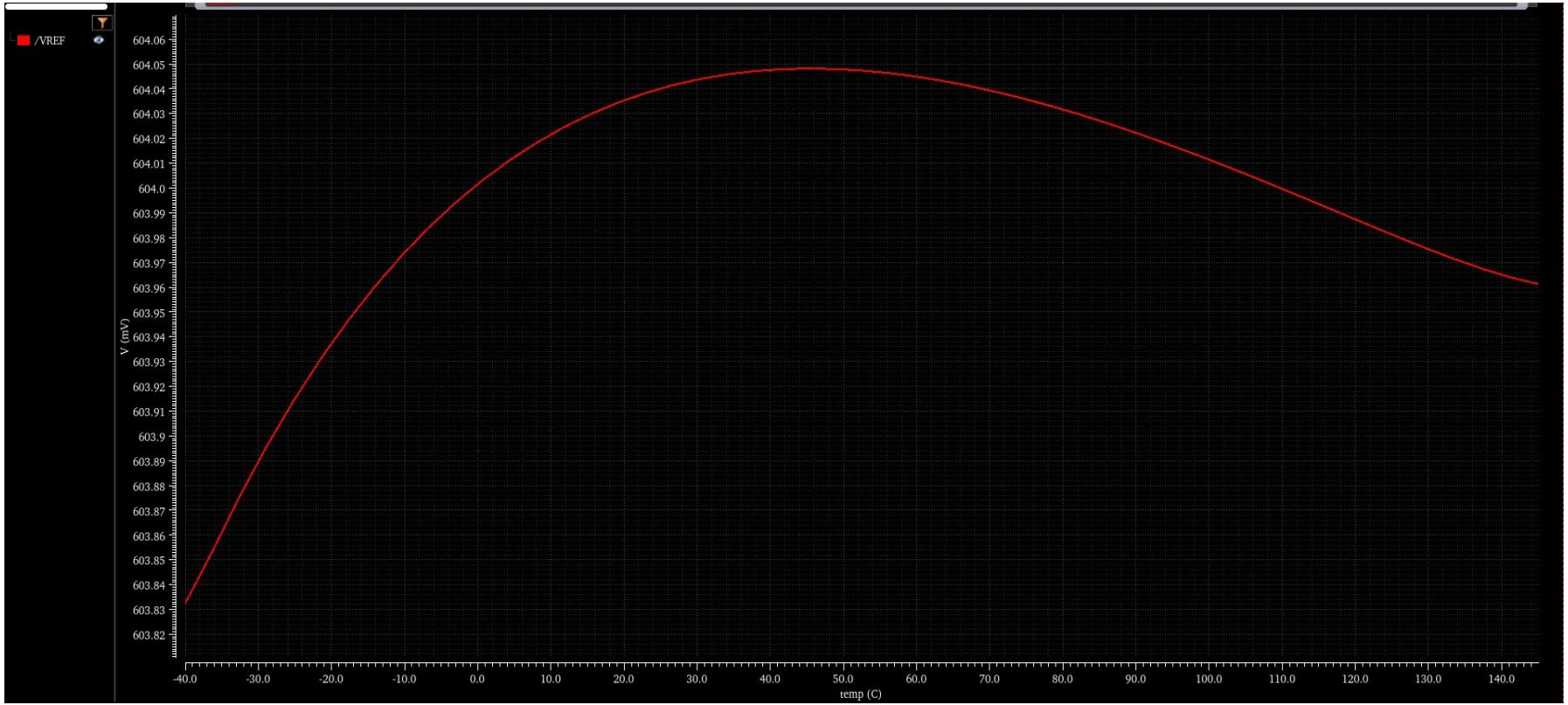


Fig.15 Dc Analysis of of Banba BGR's Output Voltage varying with temperature

Op-amp Based BGR

1. CTAT Component: Base-emitter voltage exhibits negative temperature coefficient.

2. PTAT Generation: Two BJTs with area ratio N carry equal current. The voltage difference:

$$\Delta V_{BE} = V_T \ln N = \frac{kT}{q} \ln N$$

exhibits positive temperature dependence: $\frac{d(\Delta V_{BE})}{dT} = \frac{k}{q} \ln N > 0.$

3. BGR Compensation: Feedback establishes PTAT current $I_{PTAT} = \frac{\Delta V_{BE}}{R_1}$, creating scaled PTAT voltage across R_2:

$$V_{BG} = V_{BE} + \frac{R_2}{R_1} \Delta V_{BE} = \text{const} \approx 0.6\,\text{V}$$

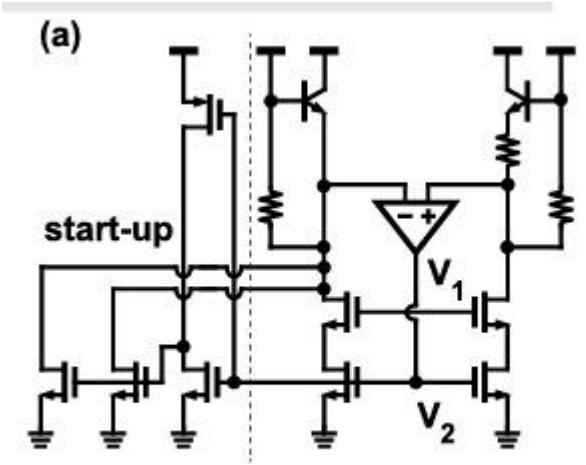


Fig. 16 Op-amp based BGR[1]

Reference[1]]:B. Razavi,“The bandgap reference: A circuit for all seasons,” *IEEE Solid-State Circuits Magazine[2]*

Necessity of Starter Circuit

The bandgap reference circuit exhibits a zero-current equilibrium point. At power-up or after power loss, both the op-amp output and the main feedback loop begin from zero volts. Without external intervention, the circuit remains trapped in this stable but non-functional state.

Starter Circuit Function: A startup circuit injects an initial current to drive the circuit out of this zero-current equilibrium point, thereby enabling normal bandgap operation and establishing the desired operating point. Once steady-state is achieved, the startup circuit automatically disables.

Calculations:

$$\Delta V_{BE} \approx 26.55 \cdot \ln(8) = 0.0055\,\text{V} \text{ and } V_{BE} = 0.541\,\text{V}.$$

From $V_{BG} = V_{BE} + \frac{R_2}{R_1}\Delta V_{BE}$, rearranging:

$$\frac{R_2}{R_1} = \frac{V_{BG} - V_{BE}}{\Delta V_{BE}} = \frac{0.6 - 0.541}{0.0055} = \frac{0.059}{0.005521} \approx 10.33$$

Reference: [6] Robert J. Widlar "*New Developments in IC Voltage Regulators*," IEEE Journal of Solid-State Circuits, Feb. 1971.

OTA Based BGR

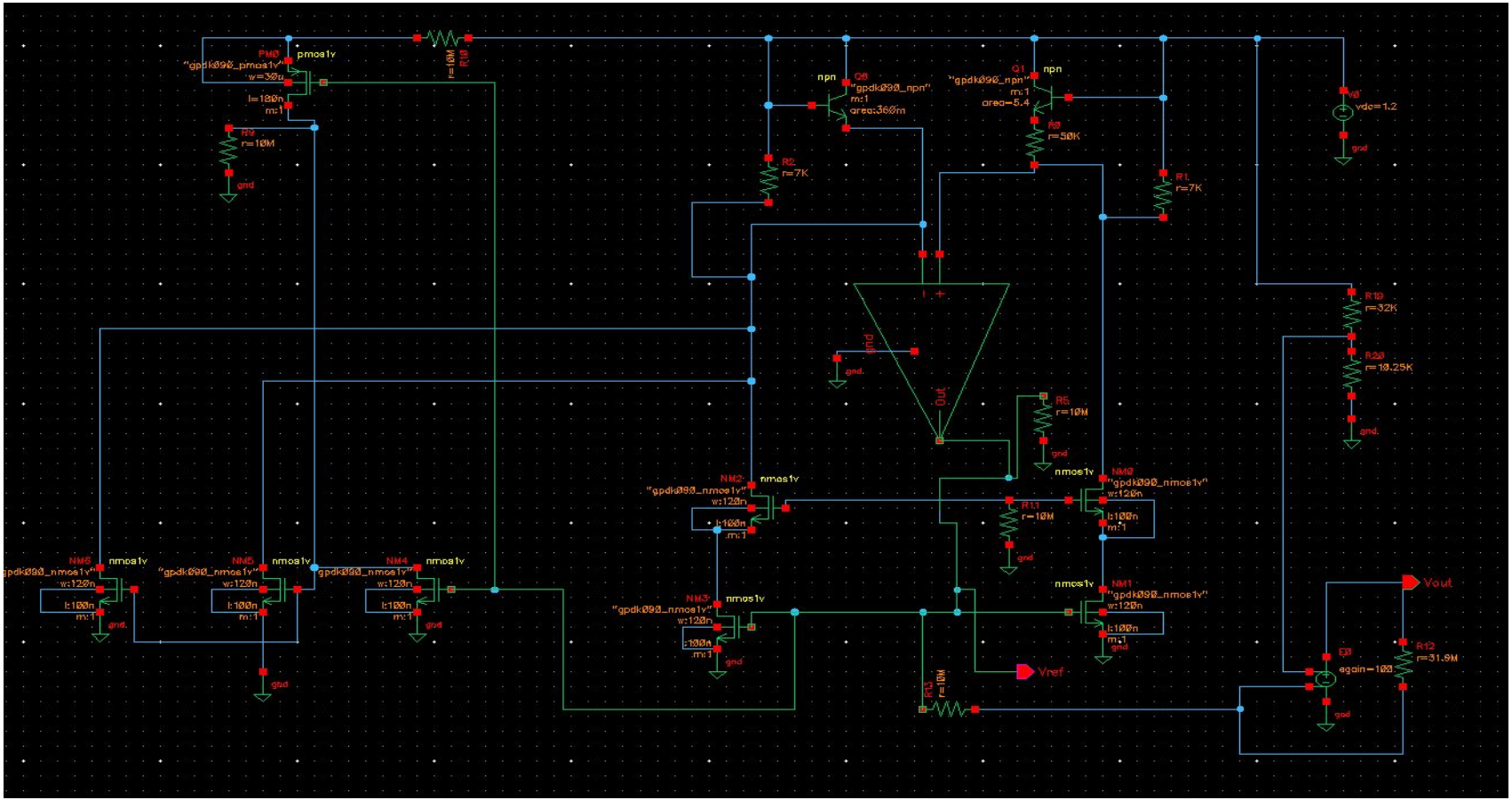


Fig.17 Cadence Schematics of OTA Based BGR with Op-amp as an ideal VCVS of gain 100V/V

Reference Voltage Temperature Profile with Op-amp as an Ideal VCVS

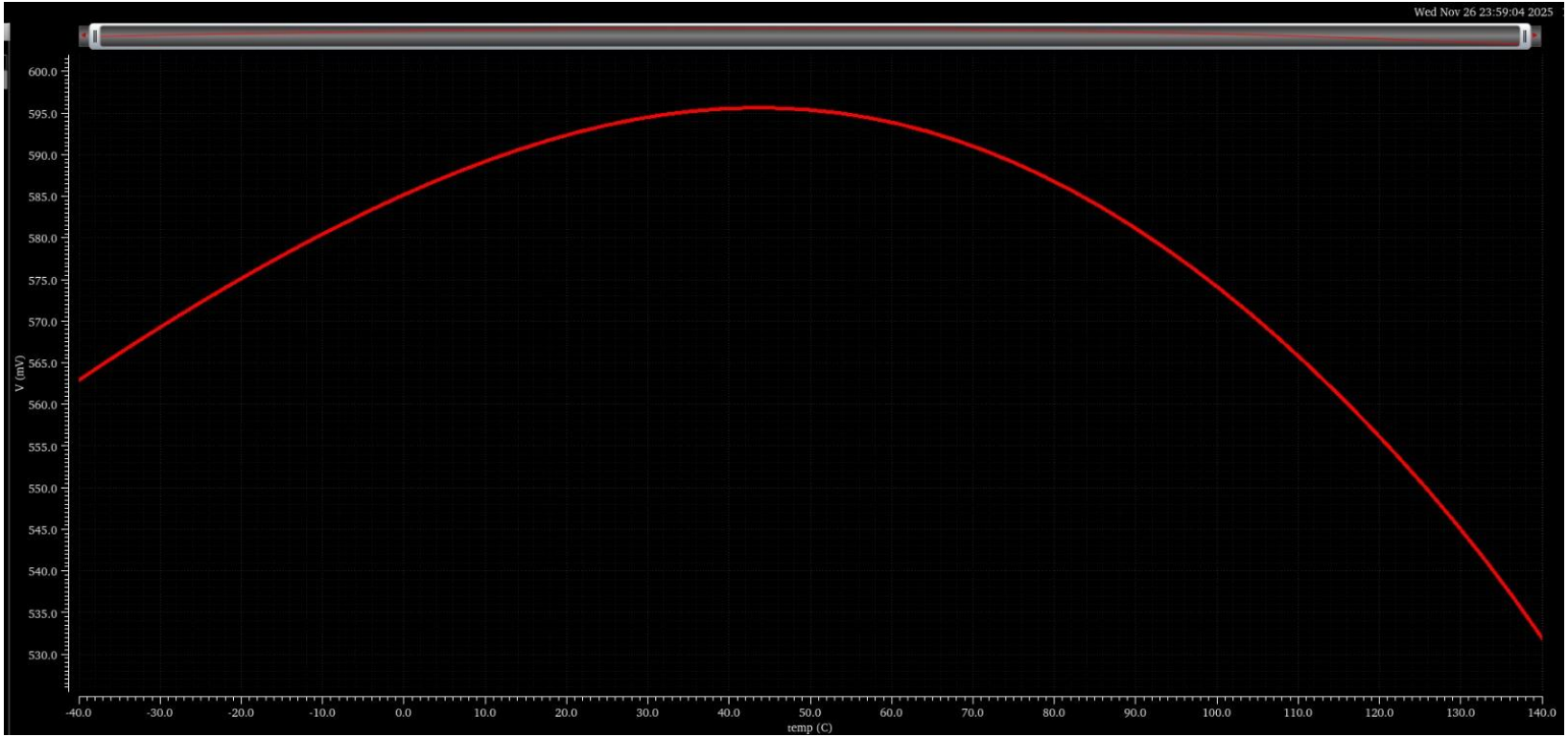


Fig.18 Dc Analysis of Output Voltage of OTA Based BGR with gain set at 100V/V (or 40dB)

Miller Compensated 5T OTA Design

Need of miller compensation:

1. Stability Challenge: Multistage amplifiers exhibit multiple poles, and low-frequency non-dominant poles compromise phase margin, risking instability.

2. Dominant Pole Compensation: A capacitor C_C connected between output and intermediate node achieves pole splitting:

$$C_{\text{eff}} = C_C(1 + A_v),$$

reducing the dominant pole frequency to 1.4 kHz while non-dominant poles remain at approximately 12.5 MHz.

3. Result: Single dominant pole ensures improved phase margin (86), stable operation, and predictable frequency response.

5T Op-Amp with Miller Compensation

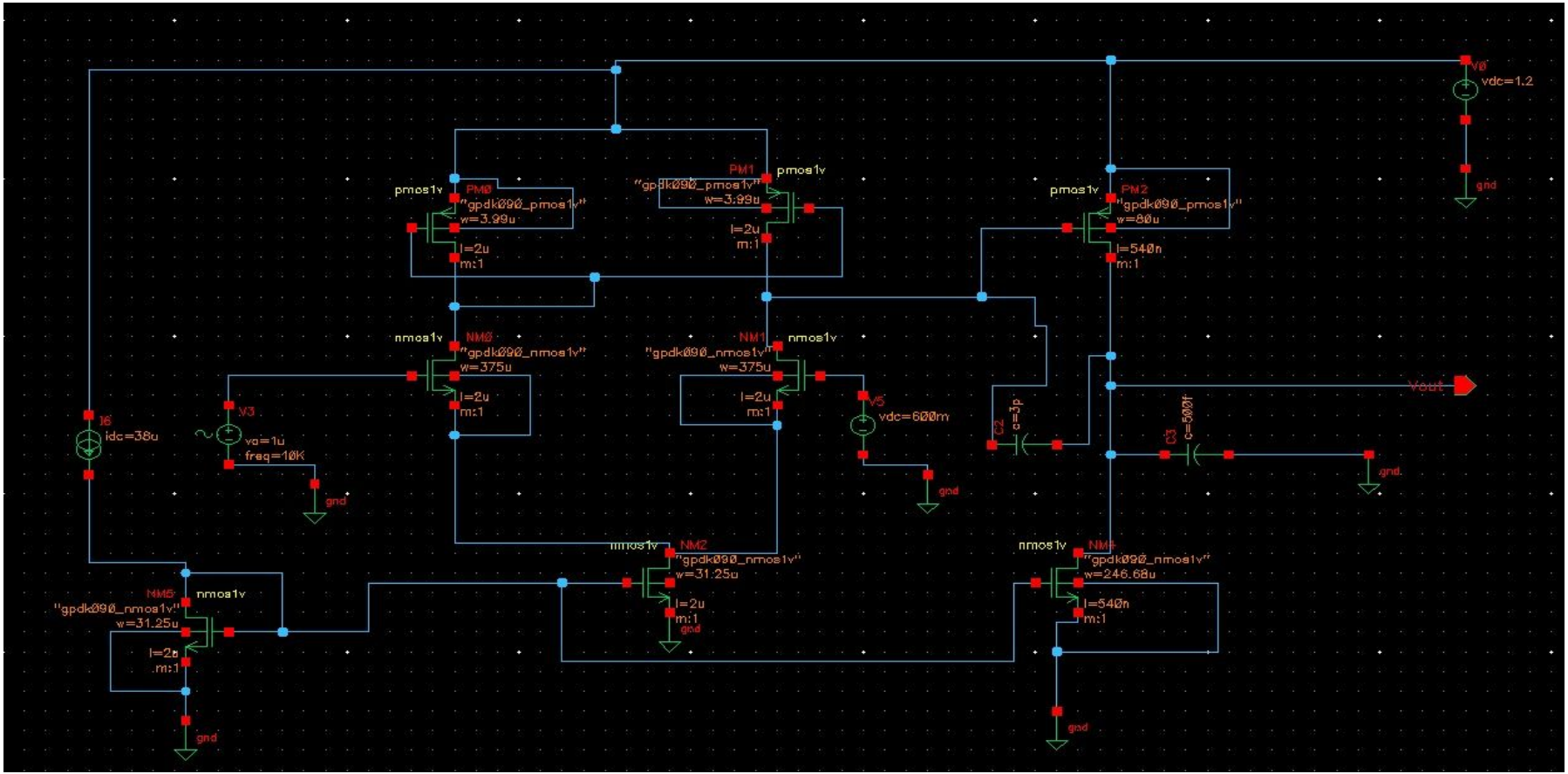
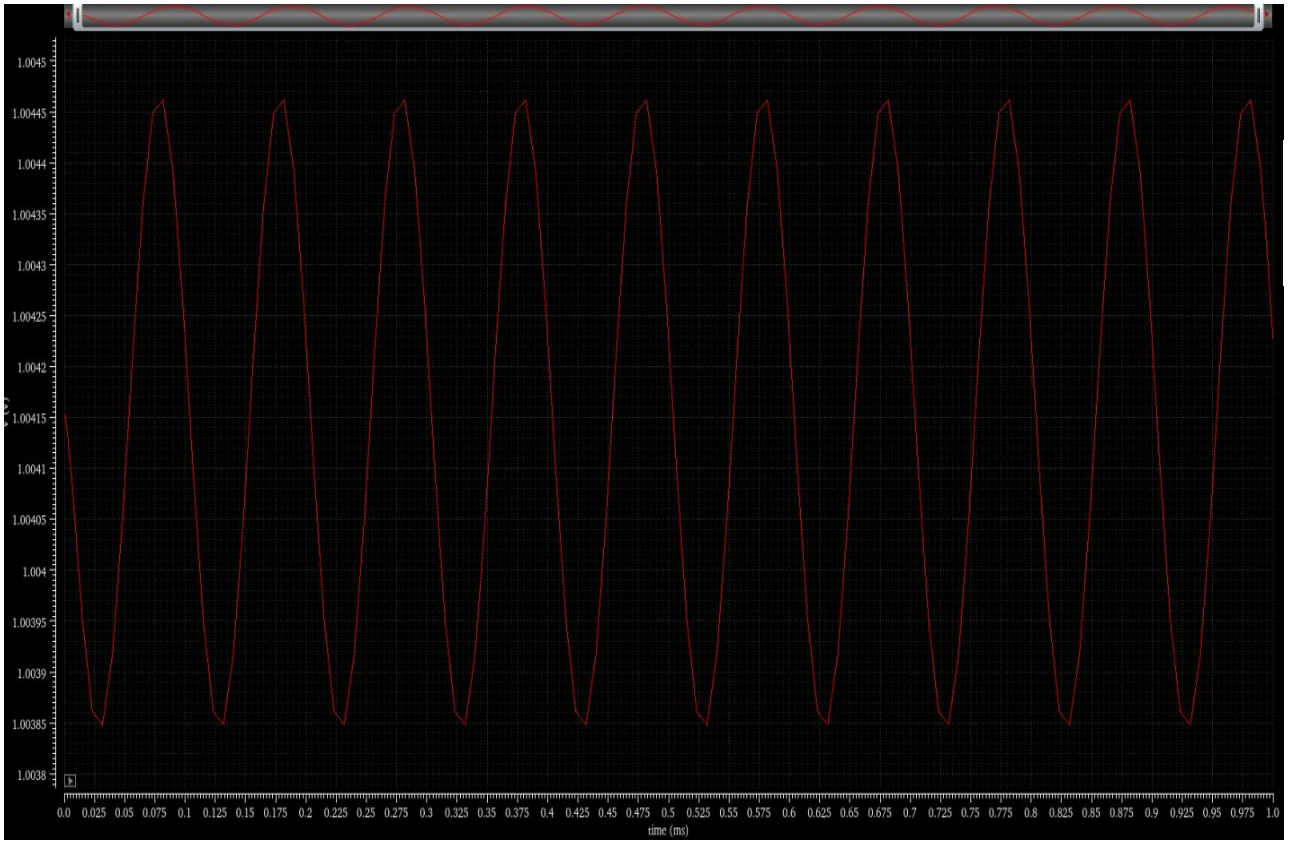


Fig.19 Cadence Schematic of 5T OTA with miller capacitance of 3pF

5T OTA Output Voltage Gain



$$V_{\text{pp}} = 1.00445\,\text{V} - 1.00385\,\text{V}$$
$$V_{\text{pp}} = 0.00060\,\text{V} = 600\,\mu\text{V}$$

$$\frac{\partial V_0}{\partial V_i} = 150\ \text{V/V}$$

Fig.20 Output voltage plot with time.

5T Op-Amp with Miller Compensation

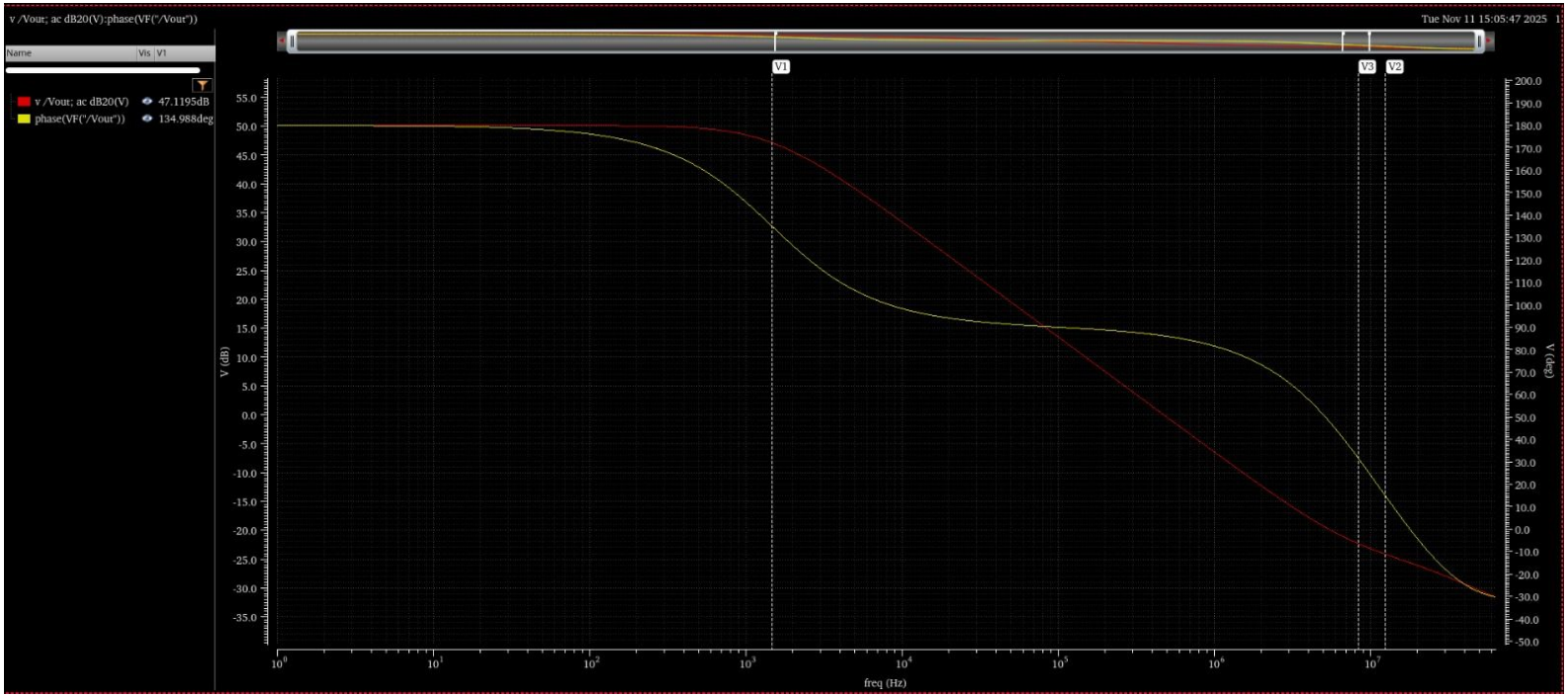


Fig.21 Bode plot and phase plot showing p1 = 1.4 kHz, p2 = 12.52MHz & z1 = 8.35 MHz

5T Op-Amp with Miller Compensation

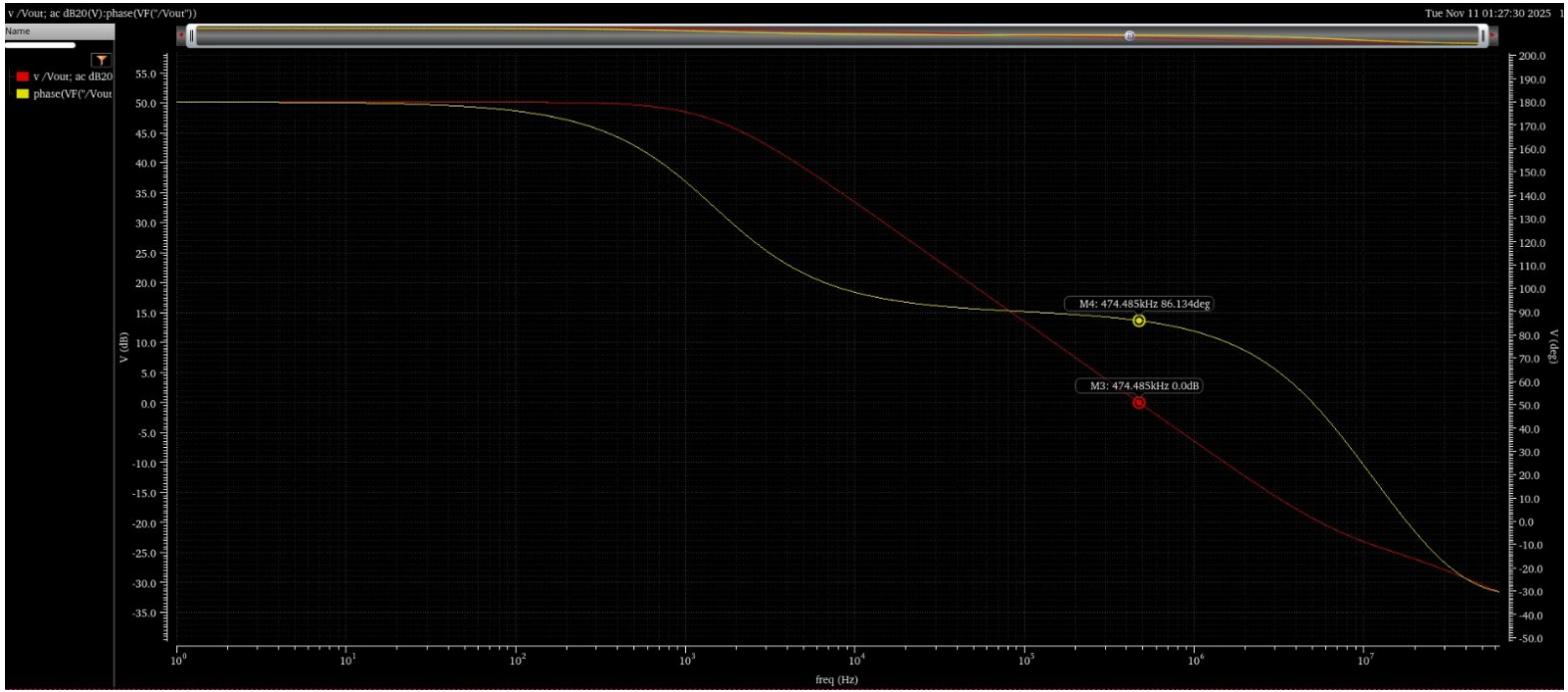


Fig.22 Bode plot and phase plot of reference voltage showing gain crossover frequency of 0.47MHz and phase margin of 86.134º

Conclusion and Future Work

This work successfully designed and simulated the Banba-based bandgap reference circuit for the CSAC driver module. Through Cadence implementation, the BGR achieved stable 0.6V output voltage independent of temperature at 1.2V supply.
A 5T OTA with Miller compensation provided improved stability margins.

Further, we will be integrating the *Miller compensated 5T-OTA* in the op-amp based BGR circuit to deliver the precision voltage reference required for VCSEL driver stability in atomic clock applications

REFERENCES

[1] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*

[2] B. Razavi, "The bandgap reference: A circuit for all seasons," *IEEE Solid-State Circuits Magazine*

[3] Azhar Yaseen, "Chip Scale Atomic Clock - Architecture Technical Report" [unpublished manuscript as on 9th October 2025]

[4] H. Zhang *et al*., "29.4 Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10-12 Long-Term Allan Deviation Using Cesium Coherent Population Trapping," *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2019, pp. 462-464

[5] wikipedia.org/wiki/Bandgap_voltage_reference

[6] Robert J. Widlar "*New Developments in IC Voltage Regulators*," IEEE Journal of Solid-State Circuits, Feb. 1971.

THANK YOU