ULPAC: A Miniaturized Ultralow-Power Atomic Clock

DEP Report (CP301)

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1. Introduction

A Chip-Scale Atomic Clock (CSAC) is an ultra-compact atomic timekeeping device designed to deliver exceptional precision while consuming minimal power. Utilizing atomic resonance methods such as coherent population trapping (CPT), CSACs achieve highly accurate timing performance in a remarkably small footprint.

These clocks are ideal for applications that demand reliable timekeeping in challenging conditions, including *GPS-denied navigation*, secure communications, and scientific instrumentation. Key characteristics of CSACs include outstanding frequency stability (as precise as 2.2×10^{-12} over 10^5 seconds), compact dimensions (as small as 15 cm^3), low power requirements (as little as 59.9 mW) and robust performance in diverse conditions [1,8].

Figure 1 illustrates a simplified block diagram of an atomic clock. At its core is the physics package, which contains the atomic reference—typically a vapor cell filled with cesium atoms. This package produces a microwave signal precisely aligned with the atoms' natural resonance frequency of 9.192631770 GHz, serving as a highly stable time reference..This is the frequency of the microwave radiation corresponding to the transition between two hyperfine energy levels of the ground state of the cesium-133 atom.

A local oscillator also generates a microwave signal, which is compared to the atomic reference signal. The difference between these two, referred to as the error signal, is processed by control electronics. These electronics adjust the local oscillator's frequency via a DC tuning input to keep it locked to the atomic reference.

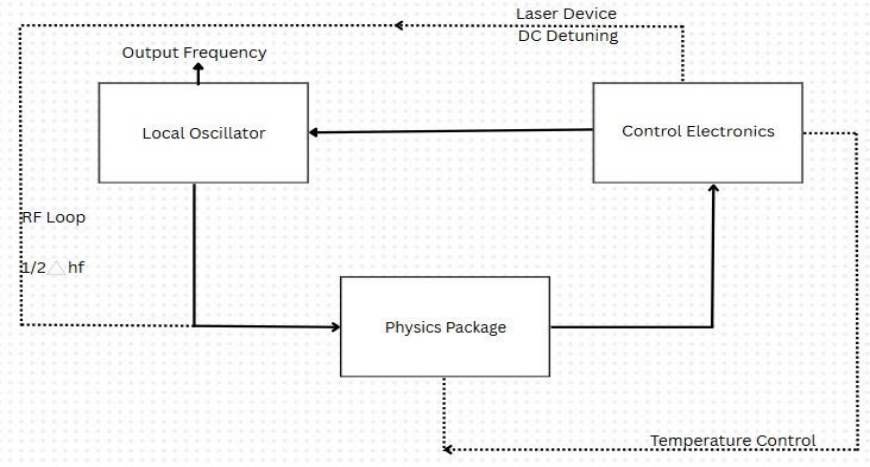


Fig1. Top-level block diagram of an atomic clock [9]

Supporting components like the laser driver and temperature control system maintain ideal conditions for the atomic medium, preserving its accuracy and stability. Additionally, an RF feedback loop continuously fine-tunes the local oscillator's frequency, further enhancing the precision of the atomic clock.

1.1 Ultra-low-power atomic clock architecture

The simplified ultra-low-power atomic clock (ULPAC) architecture is shown in Fig. 6. An RF signal-modulated vertical-cavity surface-emitting laser (VCSEL) is used to produce the interference light for the atom cell containing Cs-133 atoms, which provides an atomic frequency reference based on the coherent population trapping (CPT) resonance. The VCSEL operates at a wavelength of 894.6 nm and is modulated at 4.596 GHz, corresponding to half the cesium hyperfine frequency of 9.192631770 GHz. The resonance signal detected by a photodetector (PD) is then used to correct and stabilize the voltage-controlled crystal oscillator (VCXO) frequency. The estimated S/N ratio is approximately 100 from the measured output of the lock-in amplifier [1,2].

A phase-locked loop (PLL) locks the modulation RF signal to half the hyperfine frequency by applying frequency multiplication. When the dip in the CPT resonance signal—characterized by a narrow linewidth of 1.5 kHz and a quality factor (Q) of approximately 3.06×10^6—is detected and locked via feedback loops, the 10-MHz output from the VCXO inherits the frequency stability of the Cs atomic transition, achieving a measured Allan deviation of 2.2×10^{-12} at an averaging time of 10^5 seconds [1,14].

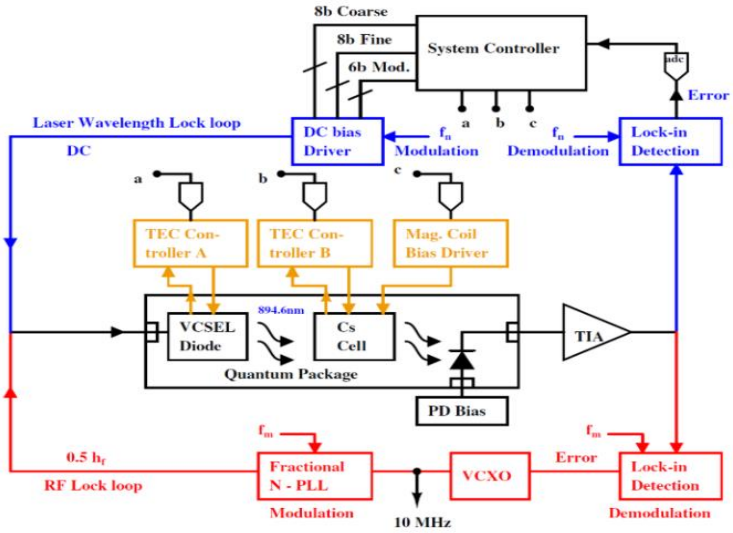


Fig 2. CSAC Architecture simplified block diagram [14].

2. Device Physics and Working

In this section we will have a deep insight of the devices used in feed-forward path of the wavelength locking loop. This includes modelling, structure, operation & simulations of VCSEL block, CPT phenomena (need for CPT resonance) and finally mathematical formulations, SIMULINK simulation results of Lock in detector.

2.1. VCSEL Diode

The VCSEL (Vertical Cavity Surface Emitting Laser) in the ULPAC system plays a critical role in generating the optical signal required for coherent population trapping (CPT) with cesium-133 atoms. It operates at a wavelength of 894.6 nm (D1 line of Cs) and is modulated at 4.596 GHz, precisely half the Cs hyperfine transition frequency (9.192 GHz). This light intensity is optimized for strong signal contrast without excessive heating or optical pumping [1,5].

2.1.1. VCSEL Structure and Operation

Power efficiency and thermal stability are also emphasized in the VCSEL block design. The total power consumption of the VCSEL subsystem is approximately 9.5 mW, with 2.5 mW allocated for temperature regulation via a heater and thermistor-controlled feedback loop [1]. Overall, the VCSEL block is optimized for ultra-low power operation while maintaining the narrow linewidth and stable optical output necessary for reliable atomic clock performance.

2.1.2. Mathematical modelling of VCSEL Block

The VCSEL wavelength shift is given by $\Delta\lambda = \beta I$, where β combines thermal resistance, voltage, and the temperature dependence of wavelength. This captures the electro-thermal-optical coupling, where thermal resistance and voltage convert electrical power into a wavelength-dependent temperature rise [14]

Wavelength shift,

$$\Delta\lambda = \alpha \Delta T \ldots (1)$$

where, α is temperature co-efficient.

The heating of VCSEL can be described by thermal resistance,

$$R_{th} = \Delta T / P_{diss} \ldots (2)$$

where P = IV and neglecting all other power losses in VCSEL.
From (1) and (2)

$$\Delta T = R_{th} \times IV \ldots (3)$$

From (3) and (1)

$$\Delta\lambda = \alpha R_{th} \times IV \ldots (4)$$

$$\Delta\lambda = \boldsymbol{\beta I \ldots (5)}$$

where $\beta = \alpha R_{th} V$.

The above set of equations just provide a mathematical modelling for VCSEL wavelength shift using the analogy of power flow corresponding to temperature difference to current flow due to potential difference [14].

2.1.3. VCSEL Current Modulation: Mathematics

The goal is to generate a unipolar (positive-only) square wave current modulation for a VCSEL:

1. The current is defined as $I(t) = I_{DC} + \Delta I(t)$, where $\Delta I(t)$ is the AC modulation.
2. A square wave can be approximated by an odd-harmonic sine series:

$$\Delta I(t) = \frac{2\Delta I}{\pi} \sum_{n=1,3,5,\ldots} \frac{\sin(n\omega_0 t)}{n}$$

   This produces a bipolar waveform oscillating between $+\Delta I$ and $-\Delta I$.

3. To shift the waveform into a unipolar range (0 to ΔI), the expression is adjusted by adding $\frac{\Delta I}{2}$, resulting in:

$$\Delta I(t) = \frac{2\Delta I}{\pi} \sum_{n=1,3,\ldots} \frac{\sin(n\omega_0 t)}{n} + \frac{\Delta I}{2}$$

   Now, the waveform ranges from 0 to ΔI, as required.

So, the note explains how to construct a unipolar square-wave-like signal using a sine series and DC shift, useful for modulating VCSEL current without negative drive levels.

2.1.4. VCSEL Current Modulation: Modelling and Simulation

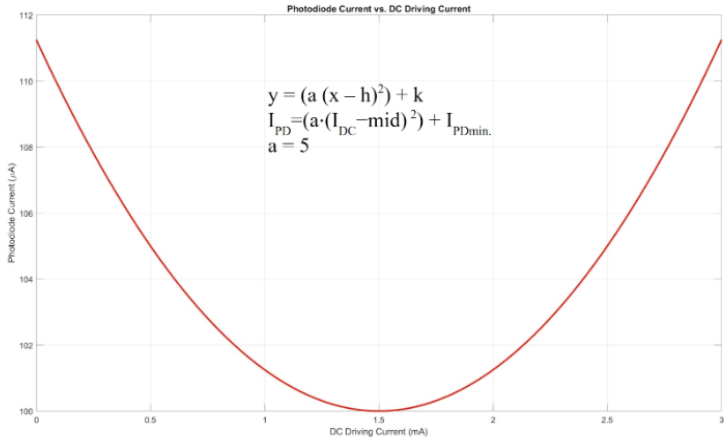


Fig.3 MATLAB Plot of I_{PD} as I_{DC} varies from 0 to 3mA

In order to lock the wavelength of the VCSEL to 894.6 nm, a modulated dc current source is used. **The maximum light absorption is the locking point for the VCSEL wavelength**

when the RF modulation is not applied. Here, a small modulated current is combined with a dc current to produce I_{DCo} and $I_{DCo}+\Delta I$ as two search values.
For our general mathematical modelling, we have taken I_{DC0}=2mA and I= Δ5μA. The averaging error signal after demodulation indicates the direction of next step movement of the dc current. In this way, the wavelength of the VCSEL is well locked at 894.6nm.

As we can see that I_{pd} and I_{dc} share a parabolic relationship so if I_{dc} is a square wave of the following type then I_{pd} will also be a square wave (as shown in Fig below)

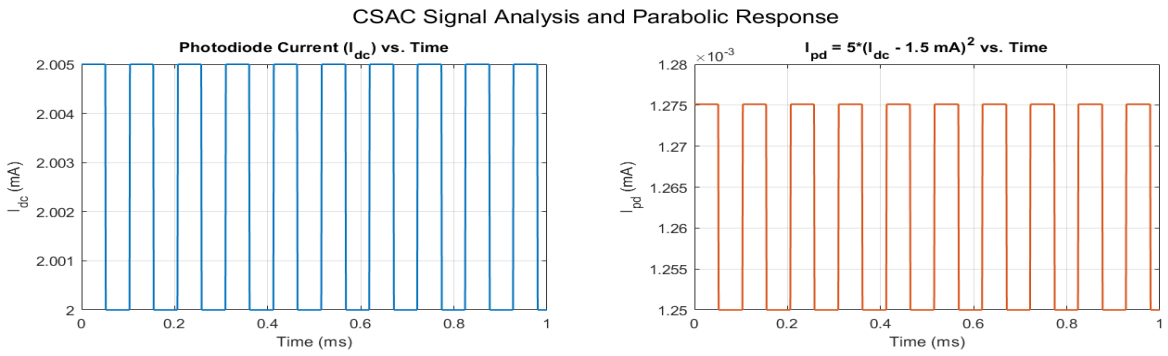


Fig.4 MATLAB simulation of the VCSEL current modulation.

Here, we have taken a parabolic function defined as $I_{PD} = 5(I_{DC}\text{-}1.5mA)^2$. The reason for the same is exclusively mention in System Controller Design (Section 3) as it will help use connect things better.

2.2. Coherent population trapping

In this section, we have a look at Coherent Population Trapping (CPT) which is a quantum interference phenomenon where atoms enter a dark state, enabling ultra-stable resonance used in atomic clocks for precise frequency standards.

2.2.1. CPT phenomena

The Three-Level Λ Model of Coherent Population Trapping is considered in the base research paper [1].

A *modulated laser* generates two optical fields:

- One tuned to the transition $F = 3 \rightarrow 6^2P_{1/2}$ (frequency ω_{31})
- Another tuned to $F = 4 \rightarrow 6^2P_{1/2}$ (frequency ω_{32})

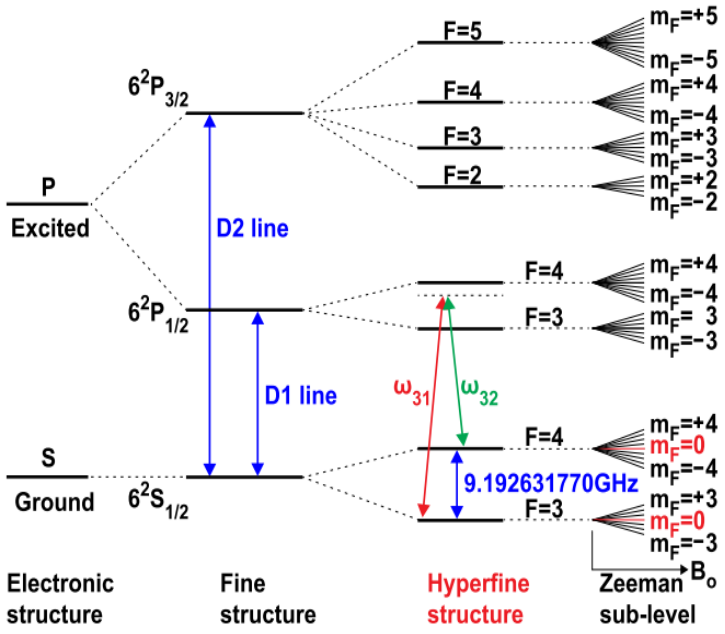


Fig.5 Energy levels of the valence electron in a Cs atom [1].

2.2.2. CPT Resonance

- Laser frequencies are tuned so the two excitation paths to $|3\rangle$ cancel via destructive interference.
- This results in **no net excitation** from the dark state to the excited state.
- The atom is **trapped** in this **dark state** — this is **Coherent Population Trapping**.

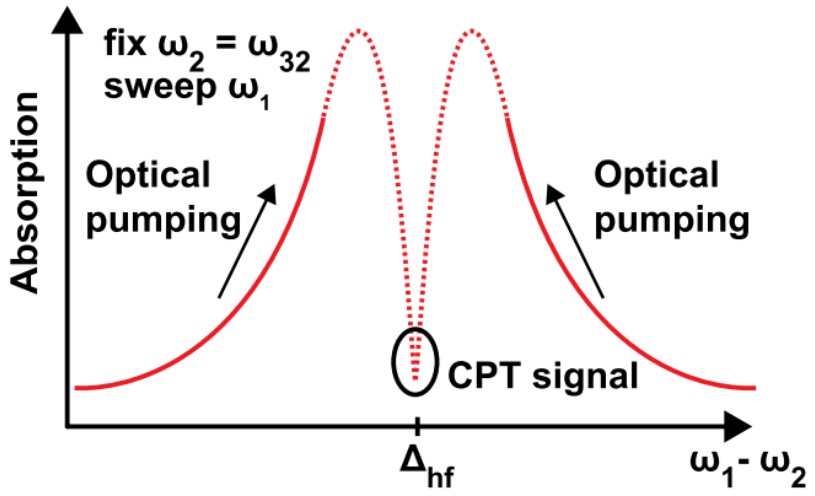


Fig.6 Illustration of optical pumping and CPT resonance [1].

2.3. Lock-in Detection

In this section we will have a look at the need of Lock-in detector. We will also have a look at mathematical formulations and SIMULINK simulation results of a Lock-in detector followed by verification of output of the detector.

2.3.1. Modelling and Purpose

A lock-in amplifier isolates a specific weak input signal from noise by multiplying it with a reference signal at the **s**ame desired frequency and filtering out 'unwanted' components. This enhances the desired signal's detectabilit**y** for the system controller. The following is the basic topology of a lock-in detector:

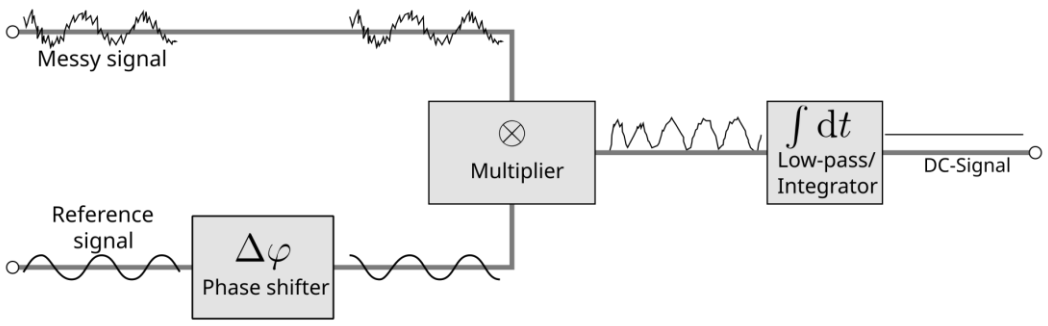


Fig.7 Topology of a Lock-in Detector [15]

2.3.2. Simulation Results

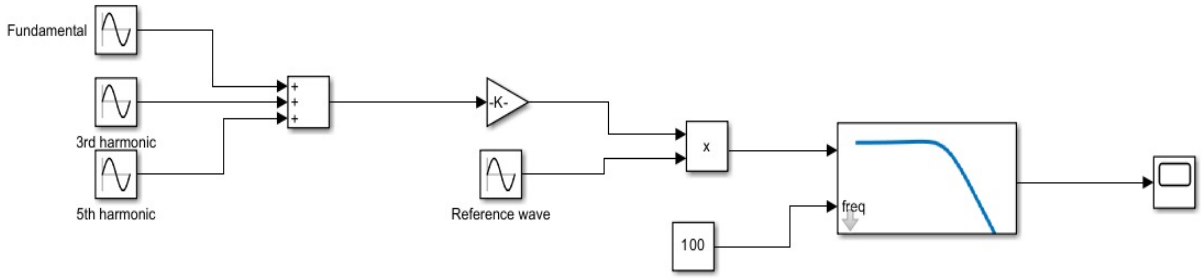
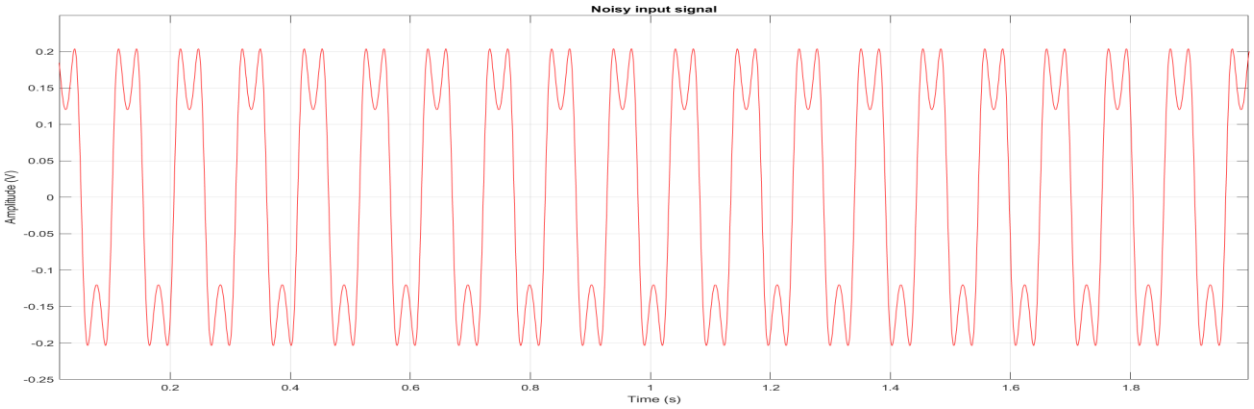
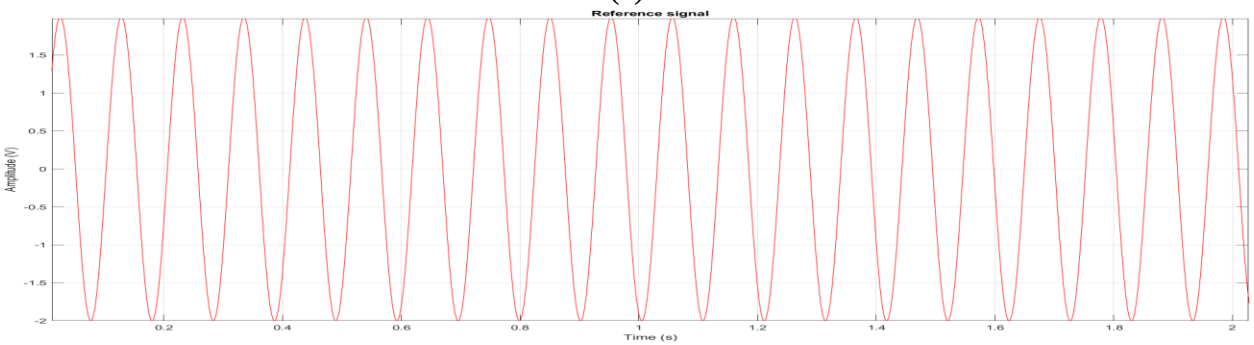


Fig.8 SIMULINK Block diagram of Lock-in detector

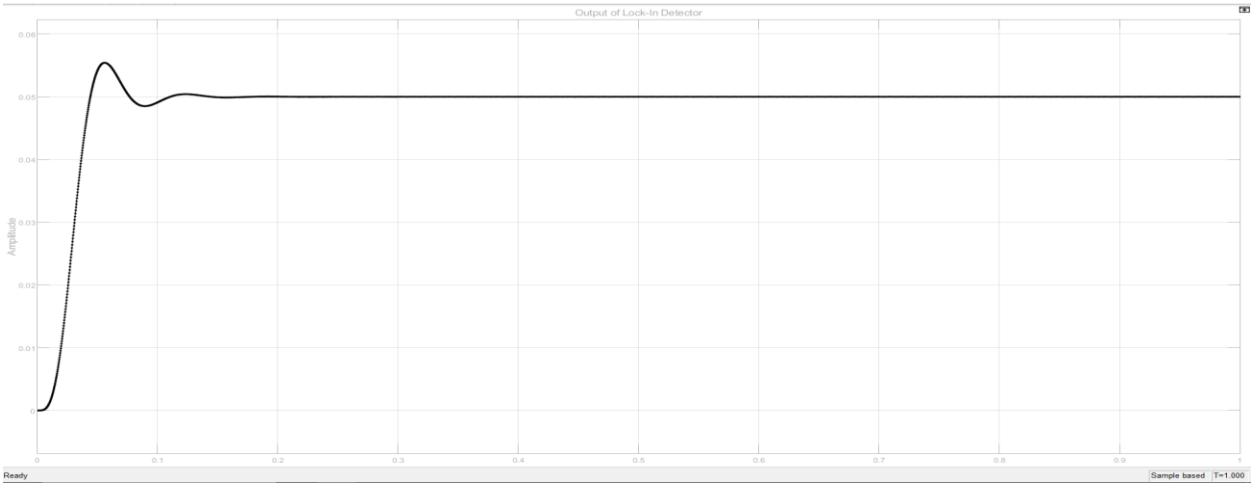
Note: Here, we have used an in-built *low pass Butterworth filter* of Simulink and have set the specifications of order 2 and cut-off frequency of 0.1KHz (as seen from '100' in above block diagram) in order to remove 9.7KHz and its higher order multiples.



(a)



(b)



(c)

Fig.9 (a) MATLAB simulation of I_{DC} vs time when I_{DC} is considered upto 5^{th} harmonic.
(b) Plot of reference signal of desired frequency of 9.7KHz
(c) SIMULINK simulation of output of Lock in amplifier

Here, we have assumed only the first 3 odd harmonics of the I_{DC} which is modelled as a square wave. As we know from the basics of fourier series that the fourier coefficients decay *inversely proportional to* n^2 as n varies, so choosing only first 3 harmonic i.e. fundamental, 3^{rd} and 5^{th} is a quite *practical* choice.

2.3.3. Mathematical Formulations of Lock-in Detector

Let the input and reference signals be

$$V_{\text{in}}(t) = A_1 \sin(\omega_0 t) + A_3 \sin(3\omega_0 t) + A_5 \sin(5\omega_0 t),$$
$$V_{\text{ref}}(t) = B \sin(\omega_0 t).$$

The mixer output is

$$V_{\text{mix}}(t) = V_{\text{in}}(t)\, V_{\text{ref}}(t) = B\left[A_1 \sin(\omega_0 t) + A_3 \sin(3\omega_0 t) + A_5 \sin(5\omega_0 t)\right] \sin(\omega_0 t).$$

Using the identity

$$\sin a \, \sin b = \tfrac{1}{2}\left[\cos(a-b) - \cos(a+b)\right],$$

we get

$$V_{\text{mix}}(t) = \frac{A_1 B}{2}\left[\cos(0) - \cos(2\omega_0 t)\right] + \frac{A_3 B}{2}\left[\cos(2\omega_0 t) - \cos(4\omega_0 t)\right] + \frac{A_5 B}{2}\left[\cos(4\omega_0 t) - \cos(6\omega_0 t)\right].$$

Grouping terms,

$$V_{\text{mix}}(t) = \frac{A_1 B}{2} + \frac{B}{2}\Big[(A_3 - A_1)\cos(2\omega_0 t) + (A_5 - A_3)\cos(4\omega_0 t) - A_5 \cos(6\omega_0 t)\Big].$$

Passing through an ideal low-pass filter removes all AC terms, leaving only the DC term:

$$\boxed{V_{\text{out,DC}} = \frac{A_1 B}{2}.}$$

Here, we know B i.e. the amplitude of the reference wave of desired frequency which we generated by ourselves. From this we found the amplitude (and hence, power) of the desired frequency of 9.7KHz harmonic in the noisy signal of I_{DC}.

Given:

- $x_{\text{in}} = A_1 \sin(\omega t)$
- $\mathrm{V}_{\text{ref}} = B_1 \sin(\omega t)$

Case 1 Parameters:

- $A_1 = 1$
- $f = 9.7\ \text{kHz} \Rightarrow \omega = 2\pi \times 9700$
- $B_1 = 0.1$

Expected Output:

$$V_{\text{out}} = \frac{A_1 B_1}{2} = \frac{1 \times 0.1}{2} = 0.05\ \text{V}$$

We can check that the lock-in detector 'settles' at $A_1B / 2 = 0.05$V as apparent from the Fig. 9 (c) of *low pass Butterworth filter of order 2 with cutoff frequency of 100Hz*.

3. System Controller Design

The main purpose that system controller will serve w.r.t. the wavelength locking loop is to find I_{PD} minima. The lock-in detection *demodulates* the discriminator signal from the TIA at 9.7 kHz. The averaging error signal after demodulation indicates the direction of the next step movement of the DC current. ***The maximum light absorption is the locking point***. The modulated DC current source ensures slight variations to lock the I_{DC} to produce $\lambda = 894.6$nm. [1,5]

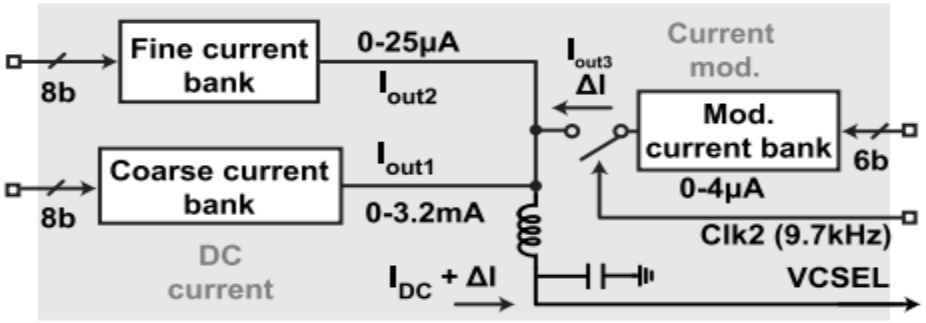


Fig.10 Circuits of the wavelength-locking loop [1]

Note: Here, we have taken the I_{DC} i.e. the VCSEL driving current as 1.5mA. This is so because choosing 1.5 mA places the bias point approximately mid-range of coarse bank, which offers **maximum headroom** for modulation and tuning thereby allowing increment or decrement of the current as required. This indeed avoids saturation near upper/lower limits of the driver.

3.1. Methodology of I_{PD} minimization:

1. Starting Points

    a. Two initial current values are chosen:

        i. $x_{1,initial}$: A baseline value (e.g., 2 mA)

        ii. $x_{2,initial}$: A slightly higher value (e.g., $x_{1,initial}$ + 5µA)

2. Parabolic Function

    a. These current values are passed through a parabolic function defined as:

$$I_{PD} = 5(I_{DC}\text{-}1.5\text{mA})^2$$

    b. This yields two outputs y_1 and y_2, corresponding to $x_{1,initial}$ and $x_{2,initial}$, respectively.

3. Comparison: The script compares and to determine how the system should shift:

a. If $y_1 > y_2$, it implies $x_{1,initial}$ is on the left side of the parabola (before the minimum), and the system should shift accordingly.
b. If $y_1 < y_2$, it implies $x_{1,initial}$ is on the right side of the parabola (after the minimum), and the system should adjust in the *opposite* direction.

4. Loop Process: Depending on the determined side, both x_1 and x_2 are incremented (or decremented) by the coarse step. The outputs y_1 and y_2 are recalculated after each step. The process continues iteratively until the ordering of y_1 and y_2 reverses, indicating that the operating point has passed through the optimal region.

5. Recording History: Each iteration's values of x_1 , x_2 and y_1, y_2 are stored. This historical data is later used for plotting the tuning process.

6. Fine Tuning (Two-Point Method)

a. Precision Adjustment
   - Uses a much smaller step size (100 nA) compared to coarse tuning (12 A).
   - Starts from the final coarse tuning value and defines $x_{2,fine}$ slightly offset from it.
b. Iterative Refinement
   - Adjusts x_1 and $x_{2,fine}$ in the same direction as coarse tuning.
   - Stops when the output response y_1-y_2 changes sign, indicating the *optimal point is reached*

3.2. VCSEL Bias Current Driving Calculation:

Coarse Current Bank (8 bits)

$$1 \text{ step} = \frac{3.2\,\text{mA}}{2^8} = \frac{3.2 \times 10^{-3}}{256} = 12.5\,\mu\text{A}$$

Fine Current Bank (8 bits)

$$1 \text{ step} = \frac{25\,\mu\text{A}}{2^8} = \frac{25 \times 10^{-6}}{256} = 97.6\,\text{nA} \approx 100\,\text{nA}$$

Modulating Current Bank (6 bits)

$$1 \text{ step} = \frac{4\,\mu\text{A}}{2^6} = \frac{4 \times 10^{-6}}{64} = 62.5\,\text{nA} \approx 60\,\text{nA}$$

3.3. Simulation Results:

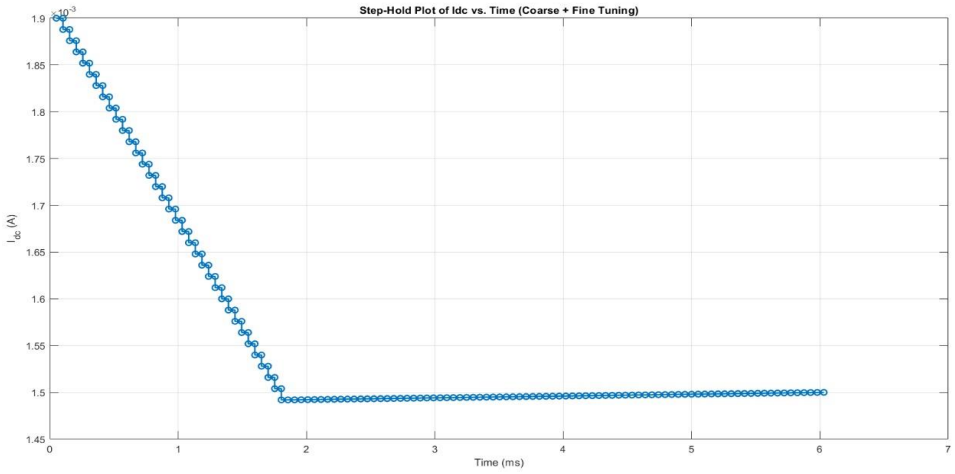


Fig.11 MATLAB Plot of I_{DC} versus time

We can see from Fig.11that initial the algorithm detects that I_{DC} is at right side of minima and therefore starts decreasing I_{DC} in coarse steps of 12.5µA and after crossing minima at 1.5mA it starts increasing in fine steps of 100nA followed by amplitude modulation of modulating wave.

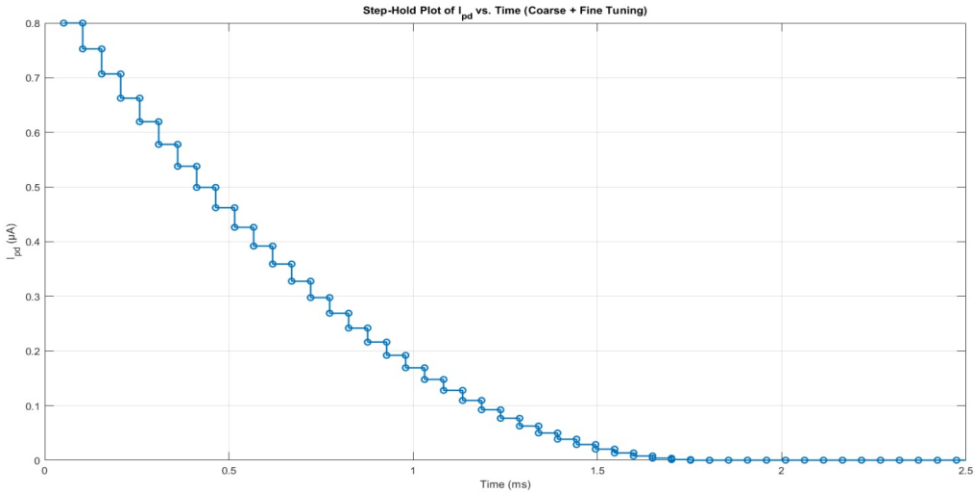


Fig.12 MATLAB Plot of I_{PD} with time

For mathematical modelling, we have just taken the transimpedance amplifier (TIA) of gain $2000VA^{-1}$. Hence, the following plot of TIA just shows that the scaled version of I_{PD}:

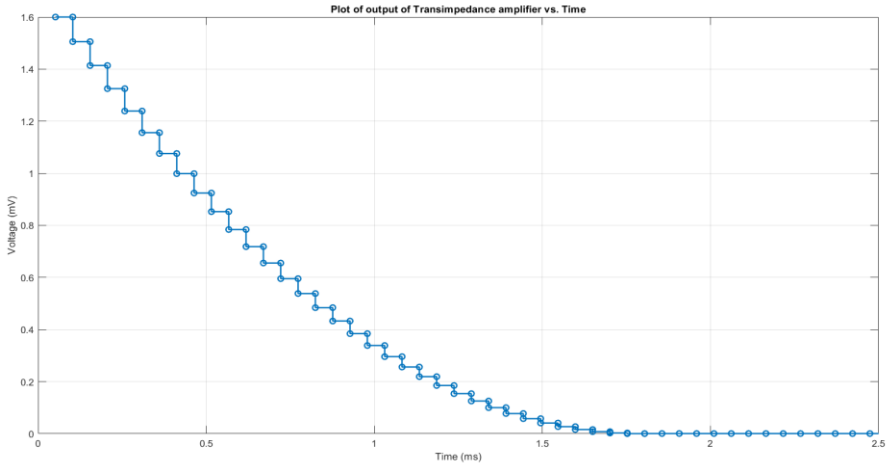


Fig.13 MATLAB Plot of TIA output with time

Now, let's do a **disturbance-rejection** or **noise-immunity test** for the CSAC's bias current, I_{DC}. By artificially stepping I_{DC} up or down (e.g. here, +0.25 mA at 1.9 ms) and then re-running our two-point coarse-and-fine tuning algorithm, *we simulate how the control loop responds to sudden perturbations*. In a real CSAC, I_{DC} can drift or jump because of temperature changes, supply-ripple, radiation effects, or component aging.

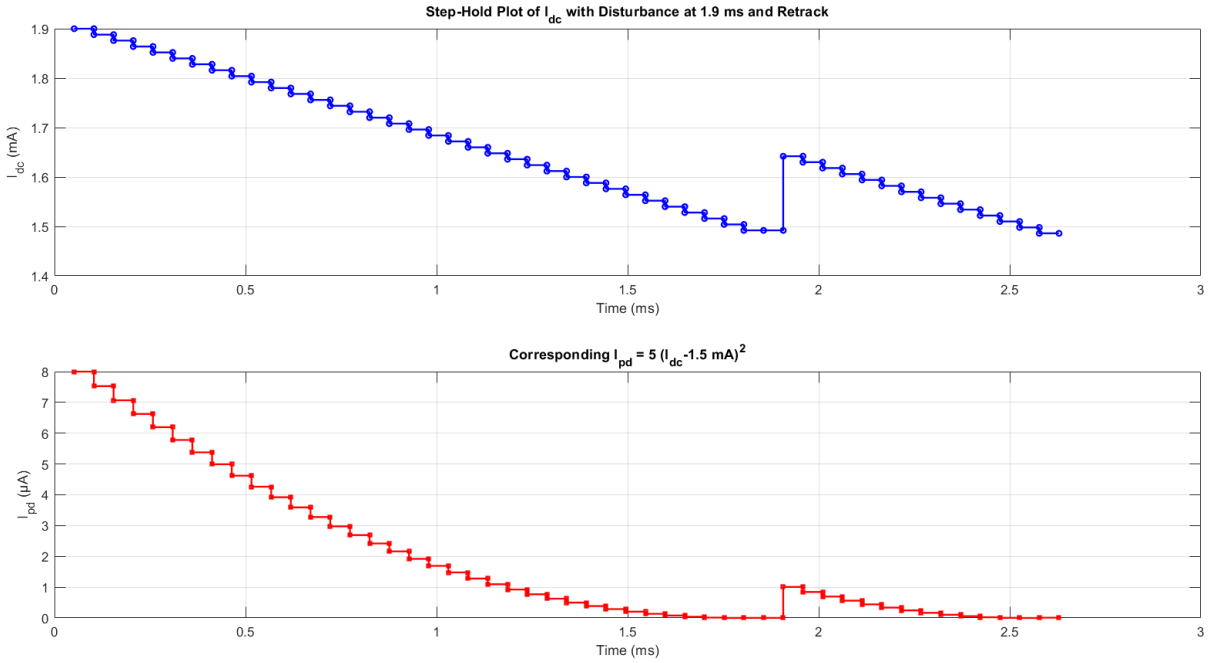


Fig.14 MATLAB Plot of I_{DC} and corresponding I_{PD} for a step perturbation of mA in I_{DC} at 1.9ms

Testing with a step disturbance verifies that the system can “re-lock” itself—first coarsely, then finely—back to the optimal operating point (≈1.5 mA), demonstrating robustness against practical noise and bias variations.

4. Conclusion

This study successfully demonstrates the implementation of a compact CPT-based frequency reference using a directly modulated VCSEL emitting at 894.6 nm, resonant with the Cs D_1 line. By precisely tuning the bias current, the VCSEL generates coherent optical sidebands separated by the Cs hyperfine ground-state splitting (9.192 GHz), enabling population trapping and formation of a dark state.

The resulting dip in photodetector current (I_{PD}) confirms CPT resonance. The integration of VCSEL technology offers a power-efficient (consumes 59.9 mW), tunable, stable to perturbations (as seen from Fig.14) and miniaturized platform (downsizing to 15 cm^3) ideal for chip-scale atomic clocks. The proposed ULPAC can also be adopted in GPS-denied environments to maintain navigation or improve the performance of high-speed datalinks, and so on [1,9]

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