Synopsys Controller IP

LPDDR5X/5/4X Memory Controller

Reference Manual

DWC LPDDR5X/5/4X Controller - Product Code: H507-0
DWC LPDDR5X/5/4X Controller AFP - Product Code: H508-0

Version 1.60a-lca00
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Revision History

The following table lists the revision history of the LPDDR5X/5/4X Memory Controller. For a detailed description of updates, refer to the LPDDR5X/5/4X Memory Controller Databook.

Note In some instances, documentation-only updates occur. The Synopsys IP product (https://www.synopsys.com/designware-ip/interface-ip.html) contains the latest information.

Version	Date	Description
1.60a-lca00	May, 2024	For a list of functional changes, refer to the Revision History in the LPDDR5X/5/4X Memory Controller Databook.

Preface

This Reference Manual describes the implementation and use of the Synopsys DDR Memory Controller (DDRCTL), which is a part of a complete LPDDR5X/5/4X interface solution.

This chapter contains the following sections:

Reference Manual Organization

The chapters of this Reference Manual are organized as follows:

- "Parameter Descriptions" provides details about DDRCTL configuration parameters.
- "Signal Descriptions" provides details about I/O signals of the DDRCTL.
- "Register Descriptions" provides details about registers of the DDRCTL.
- "Internal Parameter Descriptions" provides details about registers of the DDRCTL.

Reference Documentation

For details about reference documentation refer to the "Reference Documentation" section of the LPDDR5X/5/4X Databook.

JEDEC Specifications are available at http://www.jedec.org/.

Web Resources

- Synopsys IP product information: https://www.synopsys.com/designware-ip.html
- Your custom Synopsys IP page: https://www.synopsys.com/dw/mydesignware.php

- Documentation through SolvNetPlus: https://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing.html

STAR on the Web (SotW)

You must review all STARs on the Web (SotWs) associated with your product. SotWs are considered a part of the Synopsys documentation suite, and show critical information related to your product. To review product SotWs, refer to the Synopsys IP product information:

https://www.synopsys.com/designware-ip.html

Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

Customer Support

To obtain support for your product:

- First, prepare the following debug information, if applicable:
  - For environment setup problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, use the following menu entry:

    File > Build Debug Tar-file.

    Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file <coreTool startup directory>/debug.tar.gz.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the Design Under Test (DUT).
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. Go to the SolvNetPlus website: https://solvnetplus.synopsys.com

  SolvNetPlus does not support Internet Explorer.

  b. Click the **Cases** menu and then click the link **Create a New Case** (which is below the list of cases).

c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

Make sure to include the following:

Product L1: DesignWare Cores

Product L2: Memory Controller

d. After creating the case, attach any debug files you created. For more general usage information, refer to the following article in SolvNetPlus:

https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and manually routed to the correct support engineer on a first-come, first-served basis):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.
  - Attach any debug files you created.
- Or, telephone your local support center:
  - **North America:** Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - **All other countries:** https://www.synopsys.com/support/global-support-centers.html

1 Parameter Descriptions

This chapter details all the configuration parameters. **You can use the coreConsultant GUI configuration reports to determine the complete configuration state of the controller.** Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

The parameter descriptions in this chapter include the **Enabled:** attribute which indicates the values required to be set on other parameters before you can change the value of this parameter.

These tables define all of the configuration options for this component.

1.1 HW Configuration / Product Parameters

Table 1-1 HW Configuration / Product Parameters

Label	Description
Product Choice	
DDR Controller Product	This parameter specifies the type of DDR memory controller. For each product, a license is required as specified: ■ DWC LPDDR5/4/4X Controller (LPDDR54) requires DWC-LPDDR54-CONTROLLER license. ■ DWC DDR5/4 Controller (DDR54) requires DWC-DDR54-CONTROLLER license. ■ DWC AP LPDDR5/4/4X Controller (AP_LPDDR54) requires DWC-AP-LPDDR54-CONTROLLER license. ■ DWC AP DDR5/4 Controller (AP_DDR54) requires DWC-AP-DDR54-CONTROLLER license. ■ DWC LPDDR5/4/4X Controller AFP (AFP_LPDDR54) requires DWC-LPDDR54-CONTROLLER-AFP license. ■ DWC DDR5/4 Controller AFP (AFP_DDR54) requires DWC-DDR54-CONTROLLER-AFP license. ■ DWC DDR5/4 Controller with CHI (_replace_P80001562-505275_) requires DWC-DDR54-CONTROLLER-CHI license. ■ DWC DDR5/4 Controller AFP with CHI (_replace_P80001562-505275_) requires DWC-DDR54-CONTROLLER-AFP-CHI license. ■ DWC DDR5 Low Latency Controller AFP (AFP_DDR5_LLC) requires DWC-DDR54-LL-CONTROLLER-AFP license. ■ DWC DDR5 Controller AFP (AFP_DDR5) requires DWC-DDR5-CONTROLLER-AFP license. ■ DWC DDR5 Controller AFP with CHI (AFP_DDR5_CHI) requires DWC-DDR5-CONTROLLER-AFP-CHI license. ■ DWC DDR5 Secure Controller AFP (AFP_DDR5_SECURE) requires DWC-DDR5-SECURE-CTL-AFP license. ■ DWC DDR5 Secure Controller AFP with CHI (AFP_DDR5_SECURE_CHI) requires DWC-DDR5-SECURE-CTL-AFP-CHI license. ■ DWC LPDDR5X/5/4X Controller (LPDDR5X) requires DWC-LPDDR5X-CONTROLLER license. ■ DWC AP LPDDR5X/5/4X Controller (AP_LPDDR5X) requires DWC-AP-LPDDR5X-CONTROLLER license. ■ DWC LPDDR5X/5/4X Controller AFP (AFP_LPDDR5X) requires DWC-LPDDR5X-CONTROLLER-AFP license. **Values:** ■ DWC_LPDDR54_CONTROLLER (0) ■ DWC_DDR54_CONTROLLER (1) ■ DWC_AP_LPDDR54_CONTROLLER (2) ■ DWC_AP_DDR54_CONTROLLER (3) ■ DWC_LPDDR54_CONTROLLER_AFP (4)
DDR Controller Product ...(cont.)	■ DWC_DDR54_CONTROLLER_AFP (5) ■ DWC_DDR54_CONTROLLER_CHI (6) ■ DWC_DDR54_CONTROLLER_AFP_CHI (7) ■ DWC_DDR5_LL_CONTROLLER_AFP (8) ■ DWC_DDR5_CONTROLLER_AFP (9)

Table 1-1 HW Configuration / Product Parameters (continued)

Label	Description
	■ DWC_DDR5_CONTROLLER_AFP_CHI (10) ■ DWC_DDR5_SECURE_CONTROLLER_AFP (11) ■ DWC_DDR5_SECURE_CONTROLLER_AFP_CHI (12) ■ DWC_LPDDR5X_CONTROLLER (13) ■ DWC_AP_LPDDR5X_CONTROLLER (14) ■ DWC_LPDDR5X_CONTROLLER_AFP (15) **Default Value:** =<DWC-LPDDR54-CONTROLLER feature authorize> ? 0 : (<DWC-DDR54-CONTROLLER feature authorize> ? 1 : (<DWC-AP-LPDDR54-CONTROLLER feature authorize> ? 2 : (<DWC-AP-DDR54-CONTROLLER feature authorize> ? 3 : (<DWC-LPDDR54-CONTROLLER-AFP feature authorize> ? 4 : (<DWC-DDR54-CONTROLLER-AFP feature authorize> ? 5 : (<DWC-DDR54-CONTROLLER-CHI feature authorize> ? 6 : (<DWC-DDR54-CONTROLLER-AFP-CHI feature authorize> ? 7 :(<DWC-DDR54-LL-CONTROLLER-AFP feature authorize> ? 8 :(<DWC-DDR5-CONTROLLER-AFP feature authorize> ? 9 : (<DWC-DDR5-CONTROLLER-AFP-CHI feature authorize> ? 10 : (<DWC-DDR5-SECURE-CTL-AFP feature authorize> ? 11 : (<DWC-DDR5-SECURE-CTL-AFP-CHI feature authorize> ? 12 : (<DWC-LPDDR5X-CONTROLLER feature authorize> ? 13 : (<DWC-AP-LPDDR5X-CONTROLLER feature authorize> ? 14 : (<DWC-LPDDR5X-CONTROLLER-AFP feature authorize> ? 15 : 0)))))))))))))) **Enabled:**
DDR Controller Product ...(cont..)	(<DWC-LPDDR54-CONTROLLER feature authorize> || <DWC-DDR54-CONTROLLER feature authorize> || <DWC-AP-LPDDR54-CONTROLLER feature authorize> || <DWC-AP-DDR54-CONTROLLER feature authorize> || <DWC-LPDDR54-CONTROLLER-AFP feature authorize> || <DWC-DDR54-CONTROLLER-AFP feature authorize> || <DWC-DDR54-CONTROLLER-CHI feature authorize> || <DWC-DDR54-CONTROLLER-AFP-CHI feature authorize> || <DWC-DDR54-LL-CONTROLLER-AFP feature authorize> || <DWC-DDR5-CONTROLLER-AFP feature authorize> || <DWC-DDR5-CONTROLLER-AFP-CHI feature authorize> || <DWC-DDR5-SECURE-CTL-AFP feature authorize> || <DWC-DDR5-SECURE-CTL-AFP-CHI feature authorize> || <DWC-LPDDR5X-CONTROLLER feature authorize> || <DWC-AP-LPDDR5X-CONTROLLER feature authorize> || <DWC-LPDDR5X-CONTROLLER-AFP feature authorize>) == 1 **Parameter Name:** DDRCTL_PRODUCT_NAME

Table 1-1 HW Configuration / Product Parameters (continued)

Label	Description
System Interface : Include	Select the System Interface for DDRC. ■ HIF : Uses DDRC's HIF IF as system Interface ■ Arbiter (AXI) : Uses Multi-Port AXI as the System Interface ■ CHI : Uses CHI as the System Interface **Values:** ■ HIF (0) ■ AXI (1) ■ CHI (2) **Default Value:** (MEMC_DRAM_DATA_WIDTH == 8 || MEMC_DRAM_DATA_WIDTH == 16 || MEMC_DRAM_DATA_WIDTH == 32 || MEMC_DRAM_DATA_WIDTH == 64) ? 1 : 0 **Enabled:** Always **Parameter Name:** DDRCTL_SYS_INTF

1.2 HW Configuration / DDRC Parameters

Table 1-2 HW Configuration / DDRC Parameters

Label	Description
Host Interface Configuration Options	
Enable Dual HIF	Enables the support for Dual HIF command feature. ■ This feature converts HIF single command channel into separate HIF command channels for Read and Write commands. RMW commands are performed on the Write HIF command channel. ■ Read/Write arbitration performed by the PA does not occur as there are separate Read and Write channels for the PA to drive. This feature can only be enabled if the logic to optimize timing over scheduling efficiency is enabled (MEMC_OPT_TIMING==1). Enabling this logic improves the SDRAM utilization, depending on your traffic profile. However, it increases the overall area due to additional logic. . This feature is not supported in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller. **Values:** 0, 1 **Default Value:** 0 **Enabled:** MEMC_OPT_TIMING ==1 && UMCTL2_INCL_ARB == 0 **Parameter Name:** UMCTL2_DUAL_HIF
Burst Length Supported	Defines the supported burst length. This parameter specifies the size of a transaction on the host interface (HIF). This can be equivalent to a SDRAM burst length of either 16 or 32. The actual SDRAM burst length to be used can be set separately, using the register MSTR0.burst_rdwr. **Values:** ■ BL16 - HIF transaction size corresponds to SDRAM burst length 16 (16) ■ BL32 - HIF transaction size corresponds to SDRAM burst length 32 (32) **Default Value:** BL16 - HIF transaction size corresponds to SDRAM burst length 16 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** MEMC_BURST_LENGTH
Performance Interface Configuration Options	
Performance log on	Enables performance logging interface. When enabled, the performance logging signals are added to the list of output ports of the IIP. **Values:** 0, 1 **Default Value:** 0 **Enabled:** Always **Parameter Name:** MEMC_PERF_LOG_ON

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
APB Configuration options	
APB Clock Asynchronous to Core Clock	Defines the pclk clock to be synchronous or asynchronous with respect to the controller core_ddrc_core_clk. If specified to be asynchronous, clock domain crossing logic is included in the design, which increases the latency and area. pclk clock is considered synchronous when: ■ It is phase aligned and ■ Equal frequency to the controller core_ddrc_core_clk Note: The core_ddrc_core_clk frequency has to be greater or equal to pclk frequency. **Values:** ■ Synchronous (0) ■ Asynchronous (1) **Default Value:** Asynchronous **Enabled:** Always **Parameter Name:** UMCTL2_P_ASYNC_EN
APB Number of Synchronizers	This parameter defines the number of synchronization stages for APB synchronizers. ■ 2: Double synchronized ■ 3: Triple synchronized ■ 4: Quadruple synchronized **Values:** 2, 3, 4 **Default Value:** 2 **Enabled:** UMCTL2_AP_ANY_ASYNC == 1 **Parameter Name:** UMCTL2_ASYNC_REG_N_SYNC
Clock gating options	
Enable extra clock inputs for APB register	Add extra two clock inputs which can be gated when there are no APB read/write access. core_ddrc_core_clk_apbrw and pclk_apbrw **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** DDRCTL_EXTRA_CLK_APB_EN
Enable external clock gating in Teengine	This parameter enables external clock gating in Tenegine module. Set this parameter to 1 to enable clock gating for teengine. Set this parameter to 0 to disable clock gating for teengine module. **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** DDRCTL_CLK_GATE_TE_EN

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
Memory System Interface Parameters	
Memory Data Width (Bits)	This parameter specifies the memory data width of the DQ signal to SDRAM in bits. For HIF configurations, this can be any multiple of 8, with a maximum of 72. For AXI configurations, it must be a power of 2 (8, 16, 32, 64). ■ If ECC is enabled, this parameter must be set to 16, 32 or 64, and the ECC byte is additional to the width specified here. ■ If ECC is disabled, a non-power-of-2 configuration allows you to inject your own ECC at the HIF interface if required. Note that this parameter must be set to 16,32 or 64 in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller (Other memory data width is not supported). **Values:** 8, 16, 24, 32, 40, 48, 56, 64, 72 **Default Value:** 32 **Enabled:** Always **Parameter Name:** MEMC_DRAM_DATA_WIDTH
Number of Ranks Supported	This parameter specifies the maximum number of ranks supported by DWC_ddrctl (that is, the maximum number of independently-controllable chip selects). The setting of 4 is not supported in the LPDDRx Controller Products. **Values:** ■ 1 (1) ■ 2 (2) ■ 4 (4) **Default Value:** (DDRCTL_DDR == 1) ? 2 : 1 **Enabled:** Always **Parameter Name:** MEMC_NUM_RANKS
Bus Width Mode support	Selects the supported Bus Width Mode options. 0- Full, Half & Quarter bus width mode 1- Only Full & Half bus width modes 2- Only Full bus width mode **Values:** ■ Full, Half & Quarter Bus Width (0) ■ Only Full & Half Bus Width (1) ■ Only Full Bus Width (2) **Default Value:** (MEMC_BURST_LENGTH==32 && UMCTL2_INCL_ARB==1) ? 2 : 0 **Enabled:** Always **Parameter Name:** DDRCTL_PBW_MODE_SUPPORT

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
Bank Hashing Enable	Enables the Bank Hashing feature. The Bank Hashing function is performed on the mapped DRAM row, bank and BG bits. It generates new Bank and BG bits.These bits will be used to access the DRAM location. **Values:** 0, 1 **Default Value:** 0 **Enabled:** Always **Parameter Name:** DDRCTL_BANK_HASH
LPDDR Mixed Packages Enable	DDRCTL_LPDDR_MIXED_PKG Enables Mixed Package mode **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((DDRCTL_LPDDR==1) && (MEMC_NUM_RANKS==2) && (MEMC_INLINE_ECC==0) && (UMCTL2_SBR_EN==0) && (MEMC_DRAM_DATA_WIDTH==16)) **Parameter Name:** DDRCTL_LPDDR_MIXED_PKG
DFI Interface Widths	
Number of DFI Interfaces	It is an internal parameter provided in the GUI for information purposes. For DWC DDR5/4 Controller This parameter specifies the number of DFI interfaces depending on UMCTL2_DUAL_CHANNEL. 1: Single channel configuration 2: Dual channel or Shared-AC configuration For DWC LPDDR5/4/4X Controller and DWC LPDDR5X/5/4X Controller This parameter specifies the number of DFI interfaces depending on UMCTL2_DUAL_CHANNEL and MEMC_DRAM_DATA_WIDTH. 1: Single DDRC Single DFI configuration (MEMC_DRAM_DATA_WIDTH==16 and UMCTL2_DUAL_CHANNEL==0) 2: Single DDRC Dual DFI configuration (MEMC_DRAM_DATA_WIDTH==32 or UMCTL2_DUAL_CHANNEL==1) 4: Single DDRC Quad DFI configuration (MEMC_DRAM_DATA_WIDTH==64 and UMCTL2_DUAL_CHANNEL==0) Note that Dual DDRC Dual DFI configuration (i.e.Dual Channel configuration) is not supported. Note that Single DDRC Quad DFI configuration is supported only in limited configurations. **Values:** 1, ..., 4 **Default Value:** (DDRCTL_1DDRC_4DFI == 1) ? 4 : ((DDRCTL_1DDRC_2DFI == 1) || (UMCTL2_DUAL_CHANNEL == 1)) ? 2 : 1 **Enabled:** 0 **Parameter Name:** UMCTL2_NUM_DFI

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
DFI Data Width With ECC (Bits)	This parameter specifies the width of DFI data bus including ECC (if any). It is an internal parameter provided in the GUI for information purposes. **Values:** 16, 32, 48, 64, 80, 96, 112, 128, 144, 160, 192, 224, 256, 288, 320, 512, 576 **Default Value:** MEMC_FREQ_RATIO * (MEMC_DRAM_DATA_WIDTH + MEMC_DRAM_ECC_WIDTH) * 2 **Enabled:** 0 **Parameter Name:** MEMC_DFI_TOTAL_DATA_WIDTH
Width of dfi_wrdata_en/dfi_rddata_en/dfi_rddata_valid	This parameter specifies the width of dfi_wrdata_en, dfi_rddata_en, and dfi_rddata_valid. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** MEMC_DFI_TOTAL_DATA_WIDTH / 16 **Enabled:** 0 **Parameter Name:** MEMC_DFI_TOTAL_DATAEN_WIDTH
Width of dfi_wrdata_mask	This parameter specifies the width of dfi_wrdata_mask. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** UMCTL2_DFI_MASK_PER_NIBBLE ? (MEMC_DFI_DATA_WIDTH + MEMC_DFI_ECC_WIDTH)/4 : (MEMC_DFI_DATA_WIDTH + MEMC_DFI_ECC_WIDTH)/8 **Enabled:** 0 **Parameter Name:** MEMC_DFI_TOTAL_MASK_WIDTH
CAM Configuration Options	
CAM Depth	This parameter specifies the depth (number of entries) of each CAM (read CAM and write CAM). **Values:** 16, 32, 64 **Default Value:** 32 **Enabled:** DDRCTL_HET_CAM == 0 **Parameter Name:** MEMC_NO_OF_ENTRY
Read CAM Depth	This parameter specifies the depth (number of entries) of each read CAM. **Values:** 16, 32, 64, 96, 128, 160, 192, 224, 256 **Default Value:** MEMC_NO_OF_ENTRY **Enabled:** DDRCTL_HET_CAM **Parameter Name:** MEMC_NO_OF_RD_ENTRY

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
Write CAM Depth	This parameter specifies the depth (number of entries) of Write CAM. **Values:** 16, 32, 64, 96, 128, 160, 192, 224, 256, 384, 512 **Default Value:** MEMC_NO_OF_ENTRY **Enabled:** DDRCTL_HET_CAM **Parameter Name:** MEMC_NO_OF_WR_ENTRY
Tag bits - width of token bus	Specifies the width of token bus. By default, the CAM depth determines the width of the token bus. If an arbiter is present, you can increase the width of the token bus to accommodate port and AXI IDs. **Values:** UMCTL2_TOKENW, ..., 128 **Default Value:** MEMC_NO_OF_MAX_ENTRY > 256 ? 9 : (MEMC_NO_OF_MAX_ENTRY > 128 ? 8 : (MEMC_NO_OF_MAX_ENTRY > 64 ? 7 : (MEMC_NO_OF_MAX_ENTRY == 64 ? 6 : (MEMC_NO_OF_MAX_ENTRY == 32 ? 5 : 4)))) **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 0 **Parameter Name:** MEMC_HIF_TAGBITS
Write pointer width	Specifies the number of bits provided for write pointers (sent to the controller with write commands, and later returned to the interface to enable data fetches). If an arbiter is present, you can override the width of the write pointer to accommodate port and AXI IDs. **Values:** 1, ..., 128 **Default Value:** 1 **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 0 **Parameter Name:** MEMC_HIF_WDATA_PTR_BITS
Write data SRAM Configuration Options	
Use External SRAM for Write Data	This parameter specifies the controller to use external or internal SRAM for write data. **Values:** 0, 1 **Default Value:** 1 **Enabled:** Always **Parameter Name:** UMCTL2_WDATA_EXTRAM
DDRC Internal Configuration Options	
Register DFI Outputs	This parameter enables registering of all DFI output signals. By default, all the DFI output signals are registered to ensure that timing on the DFI interface is easily met. However, by setting this parameter to 0, it is possible to remove this registering stage, which improves the latency through the controller by one cycle. Set this parameter to 0 only if it can be guaranteed that the synthesis timing of the DFI output signals between controller and PHY can be met in a single cycle. If ECC support is desired (MEMC_ECC_SUPPORT > 0), the DFI outputs are required to be registered (MEMC_REG_DFI_OUT = 1).

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
	It is possible to exclude DFI Write data signals from the registering stage by setting MEMC_REG_DFI_OUT_WR_DATA to 0. For more information, see the "Latency Analysis" section in Appendix B, "Controller Performance Details". The setting of 0 is not supported in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller. **Values:** 0, 1 **Default Value:** 1 **Enabled:** MEMC_ECC_SUPPORT == 0 **Parameter Name:** MEMC_REG_DFI_OUT
Register DFI Write Data Outputs	This parameter enables registering of DFI write data outputs. By default, all the DFI outputs are registered to ensure that timing on the DFI interface is easily met. However, by setting this parameter to 0, it is possible to remove the registering stage of the DFI Write data signals (dfi_wrdata_en, dfi_wrdata and dfi_wrdata_mask), while maintaining the registering stage of all the other DFI output signals. Set this parameter to 0 only if DFI Write Data signals can meet the single cycle synthesis timing requirement between the controller and the PHY. This parameter has a meaning only when MEMC_REG_DFI_OUT is set to 1. **Values:** 0, 1 **Default Value:** MEMC_REG_DFI_OUT==1 ? 1 : 0 **Enabled:** MEMC_REG_DFI_OUT == 1 **Parameter Name:** MEMC_REG_DFI_OUT_WR_DATA
Register DFI Read Data Inputs	This parameter enables registering of DFI read data inputs. By default, all the DFI read data input signals (dfi_rddata, dfi_rddata_valid, dfi_rddata_dbi) are not registered. When this parameter is set to 1, an extra registering stage of the DFI read data signals is added. Setting this parameter to 1 helps to meet synthesis timing requirement on read data path. **Values:** 0, 1 **Default Value:** 0 **Enabled:** MEMC_LINK_ECC==1 **Parameter Name:** MEMC_REG_DFI_IN_RD_DATA
DDRC Number of Synchronizers	This parameter specifies the number of synchronization stages for DDRC synchronizers (for asynchronous inputs directly to DDRC). ■ 2: Double synchronized ■ 3: Triple synchronized ■ 4: Quadruple synchronized **Values:** 2, 3, 4 **Default Value:** 2 **Enabled:** Always **Parameter Name:** UMCTL2_ASYNC_DDRC_N_SYNC

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
Maximum Number of Banks Supported	This parameter specifies the maximum number of banks supported with a given hardware configuration. **Values:** 0x8, 0x10, 0x20, 0x40, 0x80, 0x100, 0x200, 0x400, 0x800 **Default Value:** 1<<MEMC_RANKBANK_BITS **Enabled:** 0 **Parameter Name:** MEMC_NUM_TOTAL_BANKS
Refresh Management (RFM)	DDRCTL_HW_RFM_CTRL Enables internal Refresh Management control in DDRCTL. **Values:** 0, 1 **Default Value:** ((DDRCTL_LPDDR==1) || (MEMC_DDR5==1)) ? 1 : 0 **Enabled:** ((DDRCTL_LPDDR==1) || (MEMC_DDR5==1)) **Parameter Name:** DDRCTL_HW_RFM_CTRL
DDR4 Specific Configuration Options	
DDRCTL_DDR4_PINS	Define whether DDR4 specific DFI interface signals exist or not **Values:** 0, 1 **Default Value:** (DDRCTL_DDR==1 && DDRCTL_DDR4==1) ? 1 : 0 **Enabled:** DDRCTL_DDR==1 && DDRCTL_DDR4==0 **Parameter Name:** DDRCTL_DDR4_PINS
LPDDR Specific Configuration Options	
Refresh Management single-bank counters (RFMSBC)	DDRCTL_LPDDR_RFMSBC Enables LPDDR5 Refresh Management Single-Bank Counters **Values:** 0, 1 **Default Value:** (DDRCTL_LPDDR == 1 && DDRCTL_HW_RFM_CTRL == 1) ? 1 : 0 **Enabled:** ((DDRCTL_LPDDR==1) && (DDRCTL_HW_RFM_CTRL==1)) **Parameter Name:** DDRCTL_LPDDR_RFMSBC
Enable LPDDR5 Post Package Repair (PPR) feature	Enable LPDDR5 Post Package Repair (PPR) feature **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** DDRCTL_LPDDR5_PPR

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
Fast Frequency Change Support	
Number of Frequency Sets Supported	This parameter specifies the number of operational frequencies. **Values:** 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 **Default Value:** 1 **Enabled:** Always **Parameter Name:** UMCTL2_FREQUENCY_NUM
Enable Hardware Fast Frequency Change	This parameter provides optional hardware to enable Hardware Fast Frequency Change. **Values:** 0, 1 **Default Value:** 0 **Enabled:** (DDRCTL_LPDDR==1) && ((DDRCTL_PRODUCT_NAME==4) || (DDRCTL_PRODUCT_NAME==15)) && (UMCTL2_FREQUENCY_NUM>1) **Parameter Name:** UMCTL2_HWFFC_EN
QOS	
Enable Variable Priority Read and Write Feature	This parameter enables Variable Priority Read (VPR) and Variable Priority Write (VPW) features. On the read side, this feature allows the use of VPR in addition to Low Priority Read (LPR) and High Priority Read (HPR) priority classes. These three priority classes are intended to be mapped to three traffic classes as follows: ■ HPR (High Priority Read): Low Latency ■ VPR (Variable Priority Read): High Bandwidth ■ LPR (Low Priority Read): Best Effort The VPR commands start out behaving like LPR traffic. But, VPR commands have down-counting latency timers associated with them. When the timer reaches 0, the commands marked with VPR are given higher priority over HPR and LPR traffic. On the write side, this feature allows the use of two priority classes in the controller: ■ VPW ■ NPW These two priority classes are intended to be mapped to two traffic classes as follows: ■ VPW (Variable Priority Write) High Bandwidth ■ NPW (Normal Priority Write): Best Effort The VPW traffic class commands start out behaving like NPW traffic. But, VPW commands have down-counting latency timers associated with them. When the timer reaches 0, the commands marked with VPW are given higher priority over NPW traffic. **Values:** 0, 1 **Default Value:** 0

Table 1-2 HW Configuration / DDRC Parameters (continued)

Label	Description
	Enabled: (((UMCTL2_INCL_ARB==1) && (THEREIS_AXI_PORT==1)) || (UMCTL2_INCL_ARB==0)) **Parameter Name:** UMCTL2_VPRW_EN
Timing Optimizations	
Multi-cycle path	DDRCTL_MCP_INCLUDE Enables multicycle paths in synthesis. It is suggested to disable them whenever there are only single cycle paths. For example in LBIST applications **Values:** ■ Disable (0) ■ Enable (1) **Default Value:** Enable **Enabled:** Always **Parameter Name:** DDRCTL_MCP_INCLUDE

1.3 HW Configuration / Multiport Parameters

Table 1-3 HW Configuration / Multiport Parameters

Label	Description
Application Ports	
Number of Host Ports	When specified, this parameter includes logic to implement 1 to 16 host ports. Host port 0 is always included. **Values:** ■ 1 (1) ■ 2 (2) ■ 3 (3) ■ 4 (4) ■ 5 (5) ■ 6 (6) ■ 7 (7) ■ 8 (8) ■ 9 (9) ■ 10 (10) ■ 11 (11) ■ 12 (12) ■ 13 (13) ■ 14 (14) ■ 15 (15) ■ 16 (16) **Default Value:** DDRCTL_INCL_CHB==1 && UMCTL2_DUAL_DATA_CHANNEL==1 ? 2 : 1 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_A_NPORTS
Application Address Width	Specifies the width of the application address. A minimum value equal to UMCTL2_MIN_ADDRW is required to be able to address the maximum supported memory size. If a value higher than UMCTL2_MIN_ADDRW is set and system address regions are not enabled, the exceeding MSBs are ignored. **Values:** MEMC_HIF_MIN_ADDR_WIDTH, ..., 60 **Default Value:** UMCTL2_MIN_ADDRW **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_A_ADDRW
Application ID Width	Specifies the width of the application ID. **Values:** 1, ..., 32 **Default Value:** 8 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_A_IDW

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Application Burst Length Width	Specifies the width of the application burst length. **Values:** 4, 5, 6, 7, 8 **Default Value:** (THEREIS_AXI4_PORT == 1) ? 8 : 4 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_A_LENW
Number of AXI Exclusive Access Monitors	This parameter specifies the number of AXI Exclusive Access Monitors. ■ 0: Exclusive Access Monitoring is not supported. ■ 1-16: Exclusive Access Monitoring is supported with the selected number of monitors. **Values:** 0, ..., 16 **Default Value:** 0 **Enabled:** ((UMCTL2_INCL_ARB==1) && (THEREIS_AXI_PORT==1)) **Parameter Name:** UMCTL2_EXCL_ACCESS
Enable External Port Priorities	This parameter enables dynamic setting of port priorities externally through the AXI QoS signals (awqos_n and arqos_n). **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB==1 && UMCTL2_A_NPORTS > 1 **Parameter Name:** UMCTL2_EXT_PORTPRIO
AXI Burst Address Boundary	Specifies the AXI address boundary restriction. AXI transactions must not cross 2**AXI_ADDR_BOUNDARY bytes. The default value of 12 matches the AXI specification of 4K boundary. **Values:** 12, ..., 32 **Default Value:** 12 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_AXI_ADDR_BOUNDARY
AXI User Signal Width	This parameter specifies the width of the application user signals. **Values:** 0, ..., 8 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_AXI_USER_WIDTH

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Port 0	
Port n Type (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter defines the interface type for the controller; application port n. **Values:** ■ AXI4 (3) **Default Value:** AXI4 **Enabled:** UMCTL2_PORT_n == 1 && UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_A_TYPE_n
Port n Data Width (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter defines the data width of the controller application port n. Valid ranges for AXI4 are 32 to 512. **Values:** 8, 16, 32, 64, 128, 256, 512 **Default Value:** UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_n!=0 ? MEMC_DFI_DATA_WIDTH : 32 **Enabled:** UMCTL2_A_NPORTS >= (n+1) && UMCTL2_INCL_ARB == 1 && UMCTL2_A_TYPE_n != 0 **Parameter Name:** UMCTL2_PORT_DW_n
Port n Clock (for n = 0; n <= UMCTL2_A_NPORTS-1)	Defines the port n clock to be synchronous or asynchronous with respect to the controller core_ddrc_core_clk. If specified to be asynchronous, clock domain crossing logic is included in the design, which increases the latency and area. A port's clock (aclk_n or hclk_n) is considered synchronous when: ■ It is phase aligned and ■ Equal frequency to the controller core_ddrc_core_clk **Values:** ■ Asynchronous (0) ■ Synchronous (1) **Default Value:** UMCTL2_INCL_ARB==1) ? 0 : (DDRCTL_CHB_SYNC_MODE **Enabled:** UMCTL2_A_NPORTS>n && UMCTL2_INCL_ARB==1 **Parameter Name:** UMCTL2_A_SYNC_n
Port n Number of Synchronizers (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter defines the number of synchronization stages for the asynchronous FIFOs of port n. Applies to both the pop side and the push side. ■ 2: Double synchronized ■ 3: Triple synchronized ■ 4: Quadruple synchronized **Values:** 2, 3, 4 **Default Value:** 2 **Enabled:** UMCTL2_A_NPORTS>n && UMCTL2_A_SYNC_n==0 && UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_ASYNC_FIFO_N_SYNC_n

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Port n Static Virtual Channels Mapping (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter enables static virtual channels mapping for port n. **Values:** ■ No (0) ■ Yes (1) **Default Value:** No **Enabled:** UMCTL2_A_NPORTS>n && (UMCTL2_A_TYPE_n == 1 || UMCTL2_A_TYPE_n == 3) && UMCTL2_INCL_ARB == 1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==0 && (UMCTL2_XPI_USE2RAQ_n == 0 || UMCTL2_READ_DATA_INTERLEAVE_EN_n == 1) **Parameter Name:** UMCTL2_STATIC_VIR_CH_n
Port n Number of Virtual Channels (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter defines the number of virtual channels for port n. **Values:** 1, ..., 64 **Default Value:** (UMCTL2_XPI_USE2RAQ_n == 1 && UMCTL2_READ_DATA_INTERLEAVE_EN_n == 0) ? MEMC_NO_OF_ENTRY : (UMCTL2_XPI_SMALL_SIZED_PORT_n==1 && UMCTL2_XPI_USE2RAQ_n ==1) ? MEMC_NO_OF_ENTRY/2 : 32 **Enabled:** UMCTL2_A_NPORTS>n && (UMCTL2_A_TYPE_n == 1 || UMCTL2_A_TYPE_n == 3) && UMCTL2_INCL_ARB == 1 && (UMCTL2_XPI_USE2RAQ_n == 0 || UMCTL2_READ_DATA_INTERLEAVE_EN_n == 1) **Parameter Name:** UMCTL2_NUM_VIR_CH_n
Port n Enable External RAM for RRB (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter enables the external RAM for Read Reorder Buffer (RRB) of port n. **Values:** ■ Disable (0) ■ Enable (1) **Default Value:** (UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 1 && UMCTL2_A_NPORTS >= (n+1) && UMCTL2_INCL_ARB == 1 && UMCTL2_A_TYPE_n != 0) ? 1 : 0 **Enabled:** UMCTL2_A_NPORTS >= (n+1) && UMCTL2_INCL_ARB == 1 && UMCTL2_A_TYPE_n != 0 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 0 **Parameter Name:** UMCTL2_RRB_EXTRAM_n

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Port n Enable Retime for External RRB RAM (for n = 0; n <= UMCTL2_A_NPORTS-1)	When selected, Retime registers are implemented to register the RRB RAM data outputs before being used elsewhere in the design. **Values:** ■ Disabled (0) ■ Enabled (1) **Default Value:** Disabled **Enabled:** UMCTL2_RRB_EXTRAM_n == 1 **Parameter Name:** UMCTL2_RRB_EXTRAM_RETIME_n
Port n Preserve Read and Write Transaction Ordering (for n = 0; n <= UMCTL2_A_NPORTS-1)	If set, this parameter preserves the ordering between a read transaction and a write transaction on Port n. Additional logic is instantiated in the XPI to transport all read and write commands from the application port interface to the HIF interface in the order of acceptance. **Values:** ■ 0 (0) ■ 1 (1) **Default Value:** 0 **Enabled:** (UMCTL2_A_NPORTS>0 && (UMCTL2_A_TYPE_0 == 3) && (UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_ANY_0==0)) **Parameter Name:** UMCTL2_RDWR_ORDERED_n
Port n Read Address Queues (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter enables the dual read address queue for the controller application port n. Each dual address queue XPI consumes two consecutive PA ports. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_A_AXI_n == 1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN== 0 **Parameter Name:** UMCTL2_XPI_USE2RAQ_n
Port n Enable threshold based VC selection (for n = 0; n <= UMCTL2_A_NPORTS-1)	Enables threshold based VC selection for Read Reorder Buffer (RRB) of port n in configurations that disable read data interleaving. RRB considers a VC for selection only when the number of HIF bursts received from DDRC exceeds the value specified in PCFGR_n.rrb_lock_threshold, or all corresponding HIF bursts for the AXI transaction are returned by DDRC. This feature provides better performance when one AXI burst is translated to multiple DDR bursts but requires more area and might impact on synthesis timing depending process and so on. The size of extra area depends on number of CAM entries. UMCTL2_NUM_VIR_CH_n > 1 is required to get benefit of the feature. **Values:** ■ Disable (0) ■ Enable (1)

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
	Default Value: (UMCTL2_A_NPORTS >= (n+1) && UMCTL2_INCL_ARB == 1 && UMCTL2_A_TYPE_n != 0 && UMCTL2_READ_DATA_INTERLEAVE_EN_n == 0 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 0) ? 1 : 0 **Enabled:** UMCTL2_A_NPORTS >= (n+1) && UMCTL2_INCL_ARB == 1 && UMCTL2_A_TYPE_n != 0 && UMCTL2_READ_DATA_INTERLEAVE_EN_n == 0 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 0 **Parameter Name:** UMCTL2_RRB_THRESHOLD_EN_n
Port Arbiter	
Port Arbiter Type	Specifies the type of optimization required for the Port Arbiter block The options are: 1) two-cycle arbitration (1 cycle of idle latency) 2) combinatorial (0 cycle of idle latency) Selecting a value of 2 for this parameter in multi-port configurations can have a significant impact on timing closure. **Values:** ■ Two cycle (1) ■ Combinatorial (2) **Default Value:** (UMCTL2_INT_NPORTS < 5) ? 2 : 1 **Enabled:** Always **Parameter Name:** UMCTL2_PA_OPT_TYPE
Enable Port Arbiter Pagematch feature	This parameter enables the Port Arbiter (PA) pagematch feature in the hardware. This feature is not recommended if there is a timing closure challenge due to PA. For instance, when there are many ports, the pagematch feature can be disabled to improve synthesis timing. **Values:** 0, 1 **Default Value:** 1 **Enabled:** UMCTL2_INCL_ARB==1 **Parameter Name:** UMCTL2_PAGEMATCH_EN

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
External RAM Interface (information only)	
Write Data RAM Data Width	This parameter specifies the data width of the external write data SRAM. It is an internal parameter provided in the GUI for information purposes and is derived from MEMC_DRAM_DATA_WIDTH, MEMC_FREQ_RATIO, and MEMC_ECC_SUPPORT. **Values:** -2147483648, ..., 2147483647 **Default Value:** UMCTL2_INCL_ARB_OR_CHB == 0 && MEMC_SIDEBAND_ECC_EN==1 && UMCTL2_ECC_TEST_MODE_EN==1) ? (MEMC_OPT_WDATARAM == 1)? (MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO*2+MEMC_DFI_ECC_WIDTH *2) : (MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO*2+MEMC_DFI_ECC_WIDT H) : (MEMC_OPT_WDATARAM == 1 && MEMC_DRAM_DATA_WIDTH == 72)? ((MEMC_DRAM_DATA_WIDTH+8)*MEMC_FREQ_RATIO*2) : (MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO*2 **Enabled:** 0 **Parameter Name:** UMCTL2_WDATARAM_DW
Write Data RAM OCPAR/OCECC Width	Specifies the parity length of the external write data SRAM. It is an internal parameter provided in the GUI for information purpose. **Values:** -2147483648, ..., 2147483647 **Default Value:** (UMCTL2_OCPAR_EN == 1 || UMCTL2_OCECC_EN == 1) ? UMCTL2_WDATARAM_PAR_DW : 0 **Enabled:** 0 **Parameter Name:** UMCTL2_WDATARAM_PAR_DW_GUI
Write Data RAM Depth	This parameter specifies the depth of the external write data SRAM. It is an internal parameter provided in the GUI for information purposes and is derived from the address width of the external write data SRAM (UMCTL2_WDATARAM_AW). **Values:** -2147483648, ..., 2147483647 **Default Value:** 1<< UMCTL2_WDATARAM_AW **Enabled:** 0 **Parameter Name:** UMCTL2_WDATARAM_DEPTH

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Write Data RAM Address Width	This parameter specifies the address width of the external write data SRAM. It is an internal parameter provided in the GUI for information purposes and is derived from the CAM size (MEMC_NO_OF_ENTRY), MEMC_BURST_LENGTH, and MEMC_FREQ_RATIO. **Values:** -2147483648, ..., 2147483647 **Default Value:** MEMC_OPT_WDATARAM == 1)? ((MEMC_WRDATA_8_CYCLES == 1) ? (MEMC_WRCMD_ENTRY_BITS + 2) : (MEMC_WRDATA_4_CYCLES == 1) ? (MEMC_WRCMD_ENTRY_BITS + 1) : (MEMC_WRCMD_ENTRY_BITS)) : ((MEMC_WRDATA_8_CYCLES == 1) ? (MEMC_WRCMD_ENTRY_BITS + 3) : (MEMC_WRDATA_4_CYCLES == 1) ? (MEMC_WRCMD_ENTRY_BITS + 2) : (MEMC_WRCMD_ENTRY_BITS + 1) **Enabled:** 0 **Parameter Name:** UMCTL2_WDATARAM_AW
Read Reorder Buffer Data Width	This parameter specifies the Read Reorder Buffer (RRB) External Data RAM Interface Data Width. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** MEMC_DRAM_DATA_WIDTH * MEMC_FREQ_RATIO * 2 **Enabled:** 0 **Parameter Name:** UMCTL2_RDATARAM_DW
Read Reorder Buffer OCPAR/OCECC Width	Specifies the Read Reorder Buffer (RRB) External Data RAM Interface Parity Width. It is an internal parameter provided in the GUI for information purpose. **Values:** -2147483648, ..., 2147483647 **Default Value:** (UMCTL2_OCPAR_EN == 1 || UMCTL2_OCECC_EN == 1) ? UMCTL2_DATARAM_PAR_DW : 0 **Enabled:** 0 **Parameter Name:** UMCTL2_DATARAM_PAR_DW_GUI
Read Reorder Buffer Data Width for channel 1	This parameter specifies the Read Reorder Buffer (RRB) External Data RAM Interface Data Width for 2nd channel. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** DDRCTL_DCH1_RDATARAM_OPT == 0) ? UMCTL2_RDATARAM_DW : (UMCTL2_RDATARAM_DW/2 **Enabled:** 0 **Parameter Name:** UMCTL2_RDATARAM_DW_DCH1

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Read Reorder Buffer OCPAR/OCECC Width for channel 1	Specifies the Read Reorder Buffer (RRB) External Data RAM Interface Parity Width for channel 1. It is an internal parameter provided in the GUI for information purpose. **Values:** -2147483648, ..., 2147483647 **Default Value:** (UMCTL2_OCPAR_EN == 1 || UMCTL2_OCECC_EN == 1) ? UMCTL2_DATARAM_PAR_DW_DCH1 : 0 **Enabled:** 0 **Parameter Name:** UMCTL2_DATARAM_PAR_DW_GUI_DCH1
Read Reorder Buffer Depth	This parameter specifies the Read Reorder Buffer (RRB) External Data RAM Interface Depth. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** MEMC_NO_OF_RD_ENTRY * (MEMC_BURST_LENGTH/(MEMC_FREQ_RATIO*2)) **Enabled:** 0 **Parameter Name:** UMCTL2_RDATARAM_DEPTH
Read Reorder Buffer Address Width	This parameter specifies the Read Reorder Buffer (RRB) External Data RAM Interface Address Width. It is an internal parameter provided in the GUI for information purposes. **Values:** -2147483648, ..., 2147483647 **Default Value:** [<functionof> MEMC_NO_OF_RD_ENTRY MEMC_BURST_LENGTH MEMC_FREQ_RATIO] **Enabled:** 0 **Parameter Name:** UMCTL2_RDATARAM_AW
Timing Optimizations	
Enable XPI Write Address Retime	This parameter enables the XPI write address retime (that is, pipelines XPI write address output to PA). This parameter introduces extra cycle of latency on the write address channel. It can be used for multi-port configurations to improve timing. A retime is automatically instantiated in the xpi RMW generator. Therefore, when RMW is used, this parameter is disabled. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 && UMCTL2_XPI_USE_RMW == 0 **Parameter Name:** UMCTL2_XPI_USE_WAR

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Enable XPI Read Address Output Retime	This parameter enables the XPI read address output retime (that is, pipelines XPI write address output to PA). This parameter introduces an extra cycle of latency on the read address channel. It can be used for multi-port configurations to improve timing. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 && THEREIS_USE2RAQ == 0 **Parameter Name:** UMCTL2_XPI_USE_RAR
Enable XPI Read Address Input Retime	This parameter enables the XPI read address input retime (that is, pipelines XPI write address input before the QoS mapper). This parameter introduces an extra cycle of latency on the read address channel. It can be used to improve timing. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_XPI_USE_INPUT_RAR
Enable XPI RRB Data Retime	This parameter enables the XPI RRB data retime (that is, pipelines XPI at the output of RRB). This parameter introduces an extra cycle of latency on the read data channel. It can be used in dual data channel configurations to improve timing. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 1 **Parameter Name:** UMCTL2_XPI_USE_RDR
Enable XPI Read Parity Retime	This parameter enables the XPI read data/parity retime (that is, pipelines XPI data and parity at the AXI interface). This parameter introduces an extra cycle of latency on the read data channel. It can be used in on-chip parity configurations to improve timing. **Values:** 0, 1 **Default Value:** 0 **Enabled:** (UMCTL2_INCL_ARB == 1 && (UMCTL2_OCPAR_EN == 1 || UMCTL2_OCECC_EN == 1)) **Parameter Name:** UMCTL2_XPI_USE_RPR

Table 1-3 HW Configuration / Multiport Parameters (continued)

Label	Description
Disable XPI RMW Bypass Path	This parameter is used to enable/disable the bypass path for command and data in XPI RMW module. 1: The bypass path in XPI RMW is disabled. XPI RMW module introduces 1 cycle additional latency for write commands and data. 0: The Bypass path is included in XPI RMW parallel to the Store and Forward logic. Bypass path will be active if ECC is disabled, Data Mask (DM) is enabled and Programmable SnF is disabled. The bypass path is active/inactive depending on the register configuration. **Values:** 0, 1 **Default Value:** ((UMCTL2_PA_OPT_TYPE==1) && (UMCTL2_INT_NPORTS<3)) ? 0 : 1 **Enabled:** DDRCTL_SYS_INTF==1 **Parameter Name:** DDRCTL_XPI_USE_RMWR

1.4 HW Configuration / AXI Parameters

Table 1-4 HW Configuration / AXI Parameters

Label	Description
AXI Interface Ports - Low Power	
AXI Low Power Idle Wait	This parameter specifies the number of cycles after the last active transaction to de-assertion of the cactive signal. **Values:** 0, ..., 1048576 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB == 1 **Parameter Name:** UMCTL2_AXI_LOWPWR_NOPX_CNT
AXI Interface Ports - System Address Regions	
Number of System Address Regions	Specifies the number of System Address Regions. Specifies how many distinct address regions to be decoded in the application system address space. ■ Minimum value 0 ■ Maximum value 4 ■ Default value 0 If set to 0, no regions are specified and addresses are assumed from the address 0. **Values:** 0, ..., 4 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==0 **Parameter Name:** UMCTL2_A_NSAR
System Address Regions Minimum Block Size	Specifies the minimum block size for system address regions, ranging from 256 MB to 32GB. Determines the number of most significant system address bits that are used to decode address regions. Base addresses for each region must be aligned to this minimum block size. **Values:** ■ 256MB (1) ■ 512MB (2) ■ 1GB (3) ■ 2GB (4) ■ 4GB (5) ■ 8GB (6) ■ 16GB (7) ■ 32GB (8) **Default Value:** 256MB **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 1 && UMCTL2_A_NSAR > 0 **Parameter Name:** UMCTL2_SARMINSIZE

Table 1-4 HW Configuration / AXI Parameters (continued)

Label	Description
Clock gating	
External clock gating in ARB_Top	DDRCTL_CLK_GATE_ARB Clock gating for core_clk in ARB_Top module. **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR == 1 && DDRCTL_SYS_INTF==1 **Parameter Name:** DDRCTL_CLK_GATE_ARB
Port 0	
Port n AXI Read Address Queue Depth (for n = 0; n <= UMCTL2_A_NPORTS-1)	Determines how many AXI addresses can be stored in the read address buffer of Port n. Each address represents an AXI burst transaction. **Values:** 2, ..., 32 **Default Value:** 4 **Enabled:** UMCTL2_A_AXI_n == 1 **Parameter Name:** UMCTL2_AXI_RAQD_n
Port n AXI Write Address Queue Depth (for n = 0; n <= UMCTL2_A_NPORTS-1)	Determines how many AXI addresses can be stored in the write address buffer of Port n. Each address represents an AXI burst transaction. **Values:** 2, ..., 32 **Default Value:** 4 **Enabled:** UMCTL2_A_AXI_n == 1 **Parameter Name:** UMCTL2_AXI_WAQD_n
Port n AXI Read Data Queue Depth (for n = 0; n <= UMCTL2_A_NPORTS-1)	Determines how many AXI burst beats can be stored in the read data buffer of Port n. Set the read data buffer to an appropriate depth to allow continuous streaming of read data in the end application. If set too small, the interface will be functional, but performance might be impacted as the buffer might not have sufficient storage to permit a continuous stream of read commands. For configurations where UMCTL2_A_SYNC_n = 1, the minimum value to permit continuous streaming is 2. A higher value may be required depending on your application. For configurations where UMCTL2_A_SYNC_n = 0, the minimum value to permit continuous streaming is 10. A higher value might be required depending on the AXI to core clock ratio, as well as your application. **Values:** 2, ..., 128 **Default Value:** (UMCTL2_A_SYNC_n == 1)? 2 : 10 **Enabled:** UMCTL2_A_AXI_n == 1 **Parameter Name:** UMCTL2_AXI_RDQD_n
Port n AXI Write Data Queue Depth (for n = 0; n <= UMCTL2_A_NPORTS-1)	Determines how many AXI burst beats can be stored in the write data buffer of Port n. Set the write data buffer to an appropriate depth to allow continuous streaming of write data in the end application. If set too small, the interface will be functional, but performance might be impacted as the buffer might not have sufficient storage to permit a continuous stream of write commands.

Table 1-4 HW Configuration / AXI Parameters (continued)

Label	Description
	For configurations where UMCTL2_A_SYNC_n = 1, the minimum value to permit continuous streaming is 2. A higher value might be required depending on your application. For configurations where UMCTL2_A_SYNC_n = 0, the minimum value to permit continuous streaming is 10. Increase by at least one if AXI master issues AWVALID and corresponding WVALID on the same cycle. Increase by at least one when UMCTL2_XPI_USE_WAR=1 A higher value might be required depending on the AXI to core clock ratio as well as your application. **Values:** 2, ..., 128 **Default Value:** (UMCTL2_A_SYNC_n == 1)? 2 : 10 **Enabled:** UMCTL2_A_AXI_n == 1 **Parameter Name:** UMCTL2_AXI_WDQD_n
Port n AXI Write Response Queue Depth (for n = 0; n <= UMCTL2_A_NPORTS-1)	UMCTL2_AXI_WRQD_n: Determines how many AXI write responses can be stored in the write response buffer of Port n. Each entry represents a response to an AXI write burst transaction. Set the write response buffer to: ■ 2 for configurations where UMCTL2_A_SYNC_n = 1. ■ 10 for configurations where UMCTL2_A_SYNC_n = 0. This allows the controller to store enough write responses in the write response buffer so that the controller does not stall a continuous stream of short write transactions (with awlen = 0) to wait for free storage space in the write response buffer. May be increased if additional write response buffering in the controller is required. If set to value less than 10, the interface will be functional, but performance might be impacted as the buffer might not have sufficient storage to permit a continuous stream of write transactions. Note: the performance impact may be hidden if awlen is greater than 0. **Values:** 2, ..., 64 **Default Value:** (UMCTL2_A_SYNC_n == 1)? 2 : 10 **Enabled:** UMCTL2_A_AXI_n == 1 **Parameter Name:** UMCTL2_AXI_WRQD_n

Table 1-4 HW Configuration / AXI Parameters (continued)

Label	Description
Port n Read Data Interleaving Enable (for n = 0; n <= UMCTL2_A_NPORTS-1)	This parameter enables the interleaving of the read data of transactions with different ARID fields. ■ Read data interleaving may occur at memory burst boundaries. ■ Read data interleaving can be disabled if this parameter is set to 0. If read data interleaving is disabled, read data reordering in Read Reorder Buffer may introduce further latency. For example, a short AXI burst stays in the RRB buffer and does not interrupt a longer burst that has started earlier. ■ It is recommended to enable read data interleaving for improved read data latency. **Values:** ■ No (0) ■ Yes (1) **Default Value:** (UMCTL2_A_AXI_n==0) ? 0 : 1 **Enabled:** ((UMCTL2_A_AXI_n==0) || (UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==1)) ? 0 : 1 **Parameter Name:** UMCTL2_READ_DATA_INTERLEAVE_EN_n

1.5 HW Configuration / Multi-channel Parameters

Table 1-5 HW Configuration / Multi-channel Parameters

Label	Description
Multi-channel Specific Configuration Options	
Enable Dual Channel Support	This parameter enables Dual Channel support. The setting of 1 is not supported in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller. This feature is under access control. For more information, contact Synopsys. **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((DDRCTL_DDR==1) || ((DDRCTL_LPDDR==1) && (MEMC_ECC_SUPPORT==0) && (UMCTL2_SBR_EN==0) && (UMCTL2_DUAL_HIF==0) && (UMCTL2_NUM_LRANKS_TOTAL<8))) **Parameter Name:** UMCTL2_DUAL_CHANNEL
Number of LPDDR4 Initialization Handshake Interface Synchronizers	This parameter specifies the number of synchronization stages for LPDDR4 Initialization Handshake Interface synchronizers. ■ 2: Double synchronized ■ 3: Triple synchronized ■ 4: Quadruple synchronized **Values:** 2, 3, 4 **Default Value:** 2 **Enabled:** DDRCTL_LPDDR==1 && UMCTL2_LPDDR4_DUAL_CHANNEL==0 **Parameter Name:** UMCTL2_ASYNC_LP4DCI_N_SYNC
DDRCTL_DDR_DCH_HBW	Enables half bus width operation for DFI data signals in DDR dual channel configurations ■ When this is 0, output full bus width signals from both channels to DFI data interface ■ When this is 1, output half bus width signals from both channels to DFI data interface The setting of 1 is not supported in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller. **Values:** 0, 1 **Default Value:** (DDRCTL_DDR_DUAL_CHANNEL == 1 && MEMC_DDR5_ONLY==0) ? 1 : 0 **Enabled:** DDRCTL_DDR_DUAL_CHANNEL == 1 **Parameter Name:** DDRCTL_DDR_DCH_HBW

Table 1-5 HW Configuration / Multi-channel Parameters (continued)

Label	Description
Enable Data Channel interleaving	Enables the Data Channel interleaving in XPI: ■ When enabled, each port drives dynamically both data channels based on the address. ■ When disabled, each port statically drives only one data channel based on software settings. Note: AXI Port width restrictions apply when enabled. **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((UMCTL2_DUAL_DATA_CHANNEL==1 || SNPS_RSVDPARAM_655==1) && (UMCTL2_INCL_ARB == 1)) **Parameter Name:** UMCTL2_DATA_CHANNEL_INTERLEAVE_EN
Enable LPDDR 2MC+1PHY support	This parameter enables LPDDR 2MC+1PHY Support **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** LPDDR_2MC1PHY

1.6 HW Configuration / CHI Bridge settings Parameters

Table 1-6 HW Configuration / CHI Bridge settings Parameters

Label	Description
AXI Interface Ports - System Address Regions	
Number of System Address Regions	Specifies the number of System Address Regions. Specifies how many distinct address regions to be decoded in the application system address space. ■ Minimum value 0 ■ Maximum value 4 ■ Default value 0 If set to 0, no regions are specified and addresses are assumed from the address 0. **Values:** 0, ..., 4 **Default Value:** 0 **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==0 **Parameter Name:** UMCTL2_A_NSAR
System Address Regions Minimum Block Size	Specifies the minimum block size for system address regions, ranging from 256 MB to 32GB. Determines the number of most significant system address bits that are used to decode address regions. Base addresses for each region must be aligned to this minimum block size. **Values:** ■ 256MB (1) ■ 512MB (2) ■ 1GB (3) ■ 2GB (4) ■ 4GB (5) ■ 8GB (6) ■ 16GB (7) ■ 32GB (8) **Default Value:** 256MB **Enabled:** UMCTL2_INCL_ARB_OR_CHB == 1 && UMCTL2_A_NSAR > 0 **Parameter Name:** UMCTL2_SARMINSIZE
Realm Management Extension	
RME Support	Enabling Realm Management Extension **Values:** 0, 1 **Default Value:** 0 **Enabled:** (DDRCTL_CHB_CHIF_EN==1)? 1 : 0 **Parameter Name:** DDRCTL_CHB_RME_EN

1.7 HW Configuration / Reliability Features Parameters

Table 1-7 HW Configuration / Reliability Features Parameters

Label	Description
Memory ECC	
ECC Supported	This parameter enables ECC support. This feature is available only when the DRAM bus width is 16, 32, or 64 bits. The following are the supported ECC types: ■ SECDED ECC ■ Advanced ECC ECC is available in the following modes: ■ Full Bus Width (FBW) ■ Half Bus Width (HBW) ■ Quarter Bus Width (QBW) The following ECC codes apply for Single-beat Sideband SECDED ECC: ■ 64-bit MEMC_DRAM_DATA_WIDTH: SDRAM data + ECC width is 64(FBW)+8, 32(HBW)+8 and 16(QBW)+8 with 8-bit ECC calculated over 64-bit data ■ 32-bit MEMC_DRAM_DATA_WIDTH: SDRAM data + ECC width is 32(FBW)+7, 16(HBW)+7 and 8(QBW)+7 with 7-bit ECC calculated over 32-bit data ■ 16-bit MEMC_DRAM_DATA_WIDTH: SDRAM data + ECC width is 16(FBW)+6 and 8(HBW)+6 with 6-bit ECC calculated over 16-bit data The following ECC codes apply for Multi-beat Sideband SECDED ECC: ■ 64-bit MEMC_DRAM_DATA_WIDTH: SDRAM data + ECC width is 32(HBW)+4 with 8-bit ECC calculated over 64-bit data ■ 32-bit MEMC_DRAM_DATA_WIDTH: SDRAM data + ECC width is 32(FBW)+4 with 8-bit ECC calculated over 64-bit data For Advanced ECC: ■ The ECC code is always 256(Data)+32(ECC). ■ For DDR4 64+8 device, ECC is calculated over 256-bit data ■ For DDR5 32+8/ch device, ECC is calculated over 128-bit data + padded 0's ■ For DDR5 32+4/ch device, ECC is calculated over 256-bit data (supported when DDRCTL_BF_ECC_EN =1) ■ It is applicable when sideband ECC is enabled for DDR4/DDR5 devices For Inline ECC: ■ No addition ECC lanes are required ■ ECC is calculated over every 64-bit data The advanced ECC feature is under access control. For more information, contact Synopsys. **Values:** ■ No ECC (0) ■ SECDED ECC (1) ■ SECDED ECC + Advanced ECC (3) **Default Value:** No ECC **Enabled:**

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
ECC Supported ...(cont.)	MEMC_DRAM_DATA_WIDTH == 16 || MEMC_DRAM_DATA_WIDTH == 32 || MEMC_DRAM_DATA_WIDTH == 64 **Parameter Name:** MEMC_ECC_SUPPORT
Enable RMW	This parameter enables read-modify-write commands. By default, this parameter is set for ECC configurations and unset for non-ECC configurations. If read-modify-write commands are disabled, sub-sized write accesses of sizes less than the full memory width are not allowed. ■ For LPDDR4 HIF configurations, if MEMC_USE_RMW is disabled, only full BL16/BL8/BC4 bursts are allowed if data masks are disabled (DBICTL.dm_en = 0). ■ For LPDDR4 AXI configurations, MEMC_USE_RMW must be enabled if data masks are disabled (DBICTL.dm_en = 0). **Values:** 0, 1 **Default Value:** 1 **Enabled:** DDRCTL_SYS_INTF !=1 **Parameter Name:** MEMC_USE_RMW
Enable Sideband ECC	This parameter enables Sideband ECC. When enabled, an additional data bus for ECC is used; therefore, the actual DRAM data width is greater than MEMC_DRAM_DATA_WIDTH. The setting of 1 is not supported in LPDDR5/4/4X Controller and LPDDR5X/5/4X Controller. **Values:** 0, 1 **Default Value:** MEMC_ECC_SUPPORT>0 **Enabled:** MEMC_ECC_SUPPORT>0 **Parameter Name:** MEMC_SIDEBAND_ECC
Enable Inline ECC	This parameter enables Inline ECC. When enabled, an additional data bus for ECC is not required, therefore, the actual DRAM data width is equal to MEMC_DRAM_DATA_WIDTH. ECC parity is stored with the data without using a dedicated sideband memory device. This feature is under access control. For more information, contact Synopsys. **Values:** 0, 1 **Default Value:** 0 **Enabled:** MEMC_ECC_SUPPORT==1 && UMCTL2_PARTIAL_WR==1 && UMCTL2_DUAL_HIF==0 && MEMC_BYPASS==0 && UMCTL2_DDR4_MRAM_EN==0 && MEMC_OPT_TIMING==1 **Parameter Name:** MEMC_INLINE_ECC

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
Block Interleaving Depth	This parameter indicates the number of blocks that can be interleaved at DDRC input (HIF). This parameter is enabled in Inline ECC mode. **Values:** 4, 8, 16, 32 **Default Value:** 4 **Enabled:** (MEMC_INLINE_ECC_EN == 1) ? 1 : 0 **Parameter Name:** MEMC_NO_OF_BLK_CHANNEL
Enable ECC Scrubber Block	This parameter enables the ECC scrubber block. When set, this parameter instantiates the ECC scrubber block (SBR) that executes periodic background read commands to the DDRC. If enabled, In AXI configurations SBR consumes one of the ports of the Port Arbiter (PA). Internally, SBR is always the last port. ECC support must be enabled to use this feature. Scrubber support in HIF configurations is limited to DUAL_HIF configurations **Values:** 0, 1 **Default Value:** 0 **Enabled:** (UMCTL2_INCL_ARB_OR_CHB==1 || (DDRCTL_DDR==1 && DDRCTL_SYS_INTF==0 && UMCTL2_DUAL_HIF==1)) && MEMC_ECC_SUPPORT>0 && MEMC_USE_RMW==1 **Parameter Name:** UMCTL2_SBR_EN
SBR RMW FIFO Depth	In Sideband ECC Configurations, the RMW FIFO is instantiated in the Scrubber to hold the addresses of the correctable error responses. **Values:** 4, ..., 32 **Default Value:** 4 **Enabled:** MEMC_ECC_SUPPORT>0&&MEMC_SIDEBAND_ECC==1&&UMCTL2_SBR_EN==1&&DDRCTL_UMCTL5==1 **Parameter Name:** DDRCTL_SBR_RMW_FIFO_DEPTH
ADVECC Decoder Pipeline Enable	Instantiates logic to break the timing for ADVECC RSD decoder by adding 1 pipeline stage. When enabled, it introduced one more level of pipeline register for the decoded read data, thereby, increasing the read latency by 1 more clock cycle **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((MEMC_ECC_SUPPORT==2) || (MEMC_ECC_SUPPORT==3)) && (DDRCTL_LLC==0) **Parameter Name:** DDRCTL_RSD_PIPELINE

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
Enhanced ECC Error Reporting	This parameter will enable the following: ■ Per rank CE counters ■ Programmable CE threshold ■ Threshold based CE interrupt ■ Leaky bucket algorithm for CE counters. **Values:** 0, 1 **Default Value:** 0 **Enabled:** (MEMC_ECC_SUPPORT>0)&&(MEMC_SIDEBAND_ECC_EN==1)&&(DDRCTL_DDR==1) **Parameter Name:** DDRCTL_ENH_ECC_REPORT_EN
On-chip Reliability	
Enable On-Chip Parity	This parameter enables the On-Chip Parity feature. When enabled, the controller instantiates the necessary logic to enable on-chip parity protection: address and data paths. This feature is available only in designs where the arbiter is used (UMCTL2_INCL_ARB=1) and external WDATA RAM is used (UMCTL2_WDATA_EXTRAM=1). **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((UMCTL2_INCL_ARB==1) && (UMCTL2_WDATA_EXTRAM==1)) **Parameter Name:** UMCTL2_OCPAR_EN
On-Chip Parity Address Width	This parameter specifies the address parity width at AXI. The options are: ■ Single parity bit ■ One bit per byte of address **Values:** ■ Single bit (0) ■ One bit per byte (1) **Default Value:** Single bit **Enabled:** UMCTL2_OCPAR_OR_OCECC_EN_1==1 **Parameter Name:** UMCTL2_OCPAR_ADDR_PARITY_WIDTH

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
Enable On-Chip ECC	This parameter enables the On-Chip ECC feature. When enabled, the controller instantiates necessary logic to enable on-chip ECC protection. This feature is available only in designs where the Arbiter is used (UMCTL2_INCL_ARB=1); there are no upsized or downsized ports, Inline-ECC (MEMC_INLINE_ECC=1) and external WDATA RAM (UMCTL2_WDATA_EXTRAM=1) are used. This feature is not supported if the following conditions are true: ■ OCPAR is enabled. ■ Dual Channel is enabled. This feature is under access control. For more information, contact Synopsys. **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((UMCTL2_INCL_ARB==1) && (THEREIS_PORT_DSIZE==0) && (THEREIS_PORT_USIZE==0) && (UMCTL2_DUAL_CHANNEL==0) && ((DDRCTL_PRODUCT_NAME==2) || (DDRCTL_PRODUCT_NAME==14)) && (UMCTL2_OCPAR_EN==0) && (MEMC_INLINE_ECC==1) && (UMCTL2_WDATA_EXTRAM==1)) **Parameter Name:** UMCTL2_OCECC_EN
Enable Register Parity	This parameter enables the Register Parity feature. When enabled, the controller instantiates the necessary logic to enable register parity protection. This feature is under access control. For more information, contact Synopsys. **Values:** 0, 1 **Default Value:** 0 **Enabled:** (DDRCTL_LPDDR==1 && (DDRCTL_PRODUCT_NAME==2 || DDRCTL_PRODUCT_NAME==14)) **Parameter Name:** UMCTL2_REGPAR_EN
Register Parity Type	This parameter is the Register Parity type: ■ 0: 1 bit parity, calculated for all 32 bits ■ 1: 4 bit parity, one parity bit for each byte **Values:** ■ 1 bit parity, calculated for all 32 bits (0) ■ 4 bit parity, one parity bit for each byte (1) **Default Value:** 1 bit parity, calculated for all 32 bits **Enabled:** UMCTL2_REGPAR_EN==1 **Parameter Name:** UMCTL2_REGPAR_TYPE

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
Enable On-Chip Command/Address Protection	This parameter enables the On-Chip Command/Address Path Protection feature. When enabled, the controller instantiates necessary logic to enable on-chip command and address protection. This feature is under access control. For more information, contact Synopsys. **Values:** 0, 1 **Default Value:** 0 **Enabled:** (((UMCTL2_INCL_ARB==1 && UMCTL2_DUAL_CHANNEL==0) || UMCTL2_OCCAP_DDRC_INTERNAL_TESTING==1) && (DDRCTL_PRODUCT_NAME==2 || DDRCTL_PRODUCT_NAME==14)) **Parameter Name:** UMCTL2_OCCAP_EN
Enable Pipelining for checkers of On-Chip Command/Address Protection feature	Enable Pipelining for checkers of On-Chip Command/Address Protection feature Also includes an additional pipeline for parity checker in rd_ie_rdata_ctl module when OCPAR/OCECC is enabled with Inline ECC. **Values:** 0, 1 **Default Value:** 0 **Enabled:** UMCTL2_OCCAP_EN==1 && DDRCTL_INCL_CHB==0 **Parameter Name:** UMCTL2_OCCAP_PIPELINE
Enable On-Chip SRAM Address Protection	This parameter enables the On-Chip SRAM Address Protection . When enabled, the controller instantiates necessary logic to enable external On-Chip external SRAM Address Protection. This feature is reserved only for the automotive product with either support for OCECC (UMCTL2_OCECC_EN=1) or OCPAR (UMCTL2_OCPAR_EN=1). **Values:** 0, 1 **Default Value:** 0 **Enabled:** (((DDRCTL_PRODUCT_NAME==2) || (DDRCTL_PRODUCT_NAME==14)) && ((UMCTL2_OCPAR_EN==1) || (UMCTL2_OCECC_EN==1)) && (MEMC_INLINE_ECC==1)) **Parameter Name:** DDRCTL_OCSAP_EN
Link Reliability	
Enable Link ECC	This parameter enables the support for the link ECC feature. **Values:** 0, 1 **Default Value:** 0 **Enabled:** ((DDRCTL_LPDDR==1) && (MEMC_FREQ_RATIO==4)) && (DDRCTL_PRODUCT_NAME==2 || DDRCTL_PRODUCT_NAME==4 || DDRCTL_PRODUCT_NAME==14 || DDRCTL_PRODUCT_NAME==15) **Parameter Name:** MEMC_LINK_ECC

Table 1-7 HW Configuration / Reliability Features Parameters (continued)

Label	Description
DFI Sideband Protection	
Use DFI Sideband Watchdog timers	This parameter specifies the Controller to include DFI Sideband Watchdog Timer safety mechanism **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** DDRCTL_DFI_SB_WDT
Use DFI Error Interface	This parameter specifies the Controller to include DFI Error Interface **Values:** 0, 1 **Default Value:** 0 **Enabled:** DDRCTL_LPDDR==1 **Parameter Name:** DDRCTL_DFI_ERROR

1.8 HW Configuration / RTL Assertions Parameters

Table 1-8 HW Configuration / RTL Assertions Parameters

Label	Description
RTL Assertions Choice	
Enable All RTL SystemVerilog Assertions	This parameter enables all user executable RTL SystemVerilog assertions. This parameter is enabled by default; it is recommended to keep it enabled, especially in your testbenches. These assertions are helpful to identify unexpected input stimulus, wrong register values and bad programming sequences that can commonly occur in your environments. You can disable this parameter, if the RTL fails when running gate-level simulations or when using unsupported simulators. **Values:** 0, 1 **Default Value:** 1 **Enabled:** Always **Parameter Name:** UMCTL2_RTL_ASSERTIONS_ALL_EN

2

Signal Descriptions

This chapter details all possible I/O signals in the IP. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the controller. It is for reference purposes only.

When you configure the controller in coreConsultant, you must access the I/O signals for your actual configuration at workspace/report/IO.html or workspace/report/IO.xml after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the I/O signals that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the widths might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- **Active State:** Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the inactive state (opposite of the active state).
- **Registered:** Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of *No* does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:** Indicates which clocks in the IP sample this input (drive for an output). This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook. The presence of the postfix SuperList indicates a list of all possible clocks over all possible configs. Consult coreConsultant report for which clock applies to your specific configuration.

- **Exists:** Name of configuration parameter that populates this signal in your configuration.
- **Power Domain:** Name of power/voltage domain that this signal is part of when power/voltage islands are used. The SINGLE_DOMAIN value indicates that there are no islands.

The I/O signals are grouped as follows:

2.1 Clocks and Resets Signals

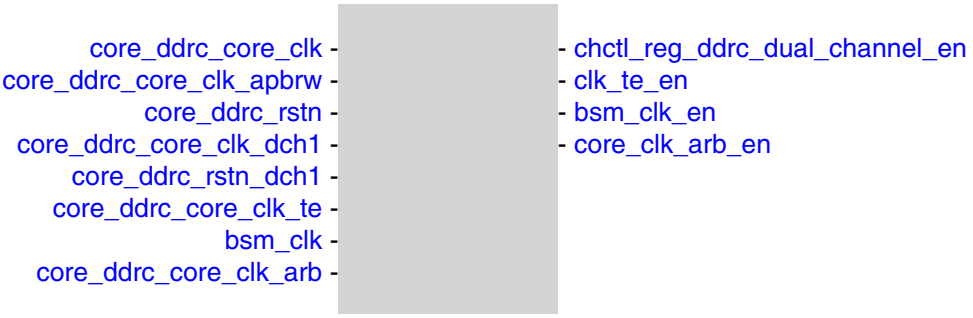


Table 2-1 Clocks and Resets Signals

Port Name	I/O	Description
core_ddrc_core_clk	I	DDRC clock. The DDRC logic, including the DFI interface, runs on this clock. ■ For 1:2 frequency ratio mode, this is at half the frequency as the SDRAM clock. ■ For 1:4 frequency ratio mode, this is at quarter the frequency of the SDRAM clock. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_ddrc_core_clk_apbrw	I	Same clock (synchronous to) as core_ddrc_core_clk. This clock can be gated when there are no APB RD/WR access. **Exists:** DDRCTL_EXTRA_CLK_APB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-1 Clocks and Resets Signals (continued)

Port Name	I/O	Description
core_ddrc_rstn	I	Active low reset signal. The controller must be taken out of reset only after all registers have been programmed. Synchronous to core_ddrc_core_clk on de-assertion, asynchronous on assertion. ■ 0 - Resets the controller ■ 1 - Takes the controller out of reset **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_ddrc_core_clk_dch1	I	DDRC DCH1 clock. The DDRC Channel 1 logic runs on this clock. Must be connected to the same clock source (synchronous to) as core_ddrc_core_clk. **Exists:** DDRCTL_DDR_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_ddrc_rstn_dch1	I	Active low reset signal for DDRC Channel 1. DDRCTL DDRC Channel 1 must be taken out of reset only after all registers have been programmed. Synchronous to core_ddrc_core_clk_dch1 on de-assertion, asynchronous on assertion. ■ 0 - Resets the DDRCTL DDRC Channel 1 ■ 1 - Takes the DDRCTL DDRC Channel 1 out of reset. **Exists:** DDRCTL_DDR_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-1 Clocks and Resets Signals (continued)

Port Name	I/O	Description
chctl_reg_ddrc_dual_channel_en	O	Equivalent to CHCTL.dual_channel_en register. This signal can be used to gate core_ddrc_core_clk_dch1 clock. **Exists:** DDRCTL_DDR_DUAL_CHANNEL__OR__SINGLE_INST_DUALCH **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_ddrc_core_clk_te	I	gated clock for teengine. When clock gating is enabled for teengine, teengine runs on this clock. **Exists:** DDRCTL_CLK_GATE_TE **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
clk_te_en	O	When value of output signal clk_te_en is 1 means clock gating for teengine can be enable to save power. **Exists:** DDRCTL_CLK_GATE_TE **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
bsm_clk[(MEMC_NUM_RANKS-1):0]	I	LPDDR gated BSM clock This clock is in the same clock domain with core_ddrc_core_clk. This clock bsm_clk[i] can be gated only when bsm_clk_en[i] is 0. **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-1 Clocks and Resets Signals (continued)

Port Name	I/O	Description
bsm_clk_en[(MEMC_NUM_RANKS-1):0]	O	LPDDR BSM clock enable **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_ddrc_core_clk_arb	I	This is gated core_ddrc_core_clk for arb_top when there is no AXI transcation. **Exists:** DDRCTL_CLK_GATE_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
core_clk_arb_en	O	This is enable signal for core_ddrc_core_clk_arb. **Exists:** DDRCTL_CLK_GATE_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.2 AXI Port n Global Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Table 2-2 AXI Port n Global Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Port Name	I/O	Description
aresetn_n	I	AXI Asynchronous Reset. Active-low pin that asynchronously resets the AXI logic to its default state. Synchronous to aclk_n on de-assertion, asynchronous on assertion. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
aclk_n	I	AXI Input Clock. All signals in the AXI host port n logic are sampled on the rising edge of this clock. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysreq_n	I	AXI Low-Power Request. Request from the system clock controller for the peripheral (Port n) to enter a low-power state. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysack_n	O	AXI Low-Power Request Acknowledge. Acknowledgement from the peripheral (Port n) of a system low-power request. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-2 AXI Port n Global Signals (for n = 0; n <= UMCTL2_A_NPORTS-1) (continued)

Port Name	I/O	Description
cactive_n	O	AXI Clock Active. Indicates that the peripheral (Port n) requires its clock signal. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
awid_n[(UMCTL2_A_IDW-1):0]	I	AXI Write Address ID. Identification tag for the write address group of signals. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awaddr_n[(UMCTL2_A_ADDRW-1):0]	I	AXI Write Address. The address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in a burst. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
awlen_n[(UMCTL2_A_LENW-1):0]	I	AXI Write Burst Length. The number of transfers in a burst associated with the write address. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awsize_n[2:0]	I	AXI Write Burst Size. The size of each transfer in a burst. Byte lane strobes indicate exactly which byte lanes to update. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awburst_n[1:0]	I	AXI Write Burst Type. Coupled with the size, burst type details how the address for each transfer within a burst is calculated. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awlock_n[`UMCTL2_AXI_LOCK_WIDTH_n-1:0]	I	AXI Write Lock Type. Provides additional information about the atomic characteristics of the transfer. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
awcache_n[3:0]	I	AXI Write Cache Type. Indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awprot_n[2:0]	I	AXI Write Protection Type. Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awuser_n[(AXI_USERW-1):0]	I	AXI Write Address User. Travels with the write transaction and back to buser with the write response. **Exists:** UMCTL2_A_AXI_n && UMCTL2_AXI_USER_WIDTH > 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awvalid_n	I	AXI Write Address Valid. Indicates that valid write address and control information are available. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
awready_n	O	AXI Write Address Ready. Indicates that the subordinate is ready to accept an address and associated control signals. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awqos_n[3:0]	I	AXI Write Quality of Service. Sideband signal to indicate the quality of service attributes of the write transaction. The awqos_n signalling is sticky, that is, it must remain stable when awvalid_n is asserted and awready_n is de-asserted. If enabled by UMCTL2_EXT_PORTPRIO hardware parameter, this signal determines the transaction priority for port arbitration. Higher values signify higher priority. For single-port configurations, this signal has no effect. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awurgent_n	I	AXI Write Urgent. Sideband signal to indicate a write urgent transaction. When asserted, if wr_port_urgent_en register is set, causes the port arbiter to switch immediately to write. It can be asserted anytime, and is not associated to any particular command. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
awpoison_n	I	AXI Write poison. Off-band signal to indicate an invalid write transaction. When asserted, no data is written to the memory. If not needed, signal must be tied to zero. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awpoison_intr_n	O	Write transaction poisoning interrupt. Cleared by register wr_poison_intr_clr. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awregion_n[3:0]	I	AXI 4 Write Address REGION signal. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI4_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
waq_wcount_n[XPI_WAQD_LG2_n-1:0]	O	Number of used positions in the Write address FIFO (synchronous to core_ddrc_core_clk). Width XPI_WAQD_LG2_n = RoundUp(log2(`UMCTL2_AXI_WAQD_n)). **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-3 AXI Port n Write Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
waq_pop_n	O	Transaction read from the Write address FIFO (synchronous to core_ddrc_core_clk). **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
waq_push_n	O	Transaction written to the Write address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
waq_split_n	O	First portion of a wrap burst going to the Write address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
awautopre_n	I	AXI auto-precharge signal for write command. This port is for write address channel signal. hif_cmd_autopre(hif_wcmd_autopre) is asserted when this signal is high. This signal is valid when awvalid_n is high. This port is available with DDR4 only. This port can not be used with LPDDR5, LPDDR4 and DDR5. In such protocols, this should be kept low. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.4 AXI Port n Write Address On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

awparity_n -

Table 2-4 AXI Port n Write Address On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Port Name	I/O	Description
awparity_n[(OCPAR_ADDR_PARITY_WIDTH-1):0]	I	AXI Write address parity. **Exists:** UMCTL2_A_AXI_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.5 AXI Port n Write Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

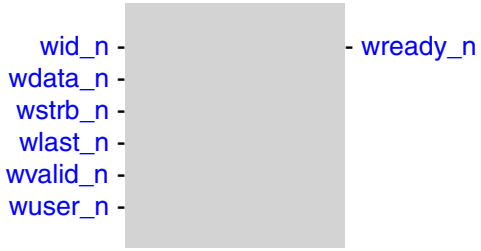


Table 2-5 AXI Port n Write Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
wid_n[(UMCTL2_A_IDW-1):0]	I	AXI Write ID. ID tag of the write data transfer. Must match the awid value of the write transaction. This signal is not used by the controller. **Exists:** IUMCTL2_A_AXI4_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdata_n[`UMCTL2_PORT_DW_n-1:0]	I	AXI Write Data. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wstrb_n[`UMCTL2_PORT_NBYTES_n-1:0]	I	AXI Write Strobe. Indicates which byte lanes to update in memory. There is one data strobe for each eight bits of the write bus, that is, wstrb[i] corresponds to wdata[8*i+7:8*i]. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-5 AXI Port n Write Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
wlast_n	I	AXI Write Last. Indicates the last transfer in a write burst. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wvalid_n	I	AXI Write Valid. Indicates that valid write data and strobes are available. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wready_n	O	AXI Write Ready. Indicates that the subordinate can accept the write data. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wuser_n[(AXI_USERW-1):0]	I	AXI Write Data User. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI_n && UMCTL2_AXI_USER_WIDTH > 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.6 AXI Port n Write Data On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

wparity_n -

Table 2-6 AXI Port n Write Data On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Port Name	I/O	Description
wparity_n[`UMCTL2_PORT_NBYTES_n-1:0]	I	AXI Write Parity/ECC. **Exists:** UMCTL2_A_AXI_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.7 AXI Port n Write Response Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Table 2-7 AXI Port n Write Response Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
bid_n[(UMCTL2_A_IDW-1):0]	O	AXI Write Response ID. Must match the awid value of the write transaction to which the subordinate is responding. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
bresp_n[(AXI_RESPW-1):0]	O	AXI Write Response. Indicates the status of the write transaction. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
buser_n[(AXI_USERW-1):0]	O	AXI Write Response User. Mirror of awuser sent with write transaction. **Exists:** UMCTL2_A_AXI_n && UMCTL2_AXI_USER_WIDTH > 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
bvalid_n	O	AXI Write Respnse Valid. Indicates that a valid write response is available. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-7 AXI Port n Write Response Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
bready_n	I	AXI Write Response Ready. Indicates that the master can accept the write response information. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
arid_n[(UMCTL2_A_IDW-1):0]	I	AXI Read Address ID. Identification tag for the read address group of signals. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
araddr_n[(UMCTL2_A_ADDRW-1):0]	I	AXI Read Address. The address of the first transfer in a read burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in a burst. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
arlen_n[(UMCTL2_A_LENW-1):0]	I	AXI Read Burst Length. The number of transfers in a burst associated with the read address. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arsize_n[(AXI_SIZEW-1):0]	I	AXI Read Burst Size. The size of each transfer in a burst. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arburst_n[(AXI_BURSTW-1):0]	I	AXI Read Burst Type. Coupled with the size, burst type details how the address for each transfer within a burst is calculated. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arlock_n[`UMCTL2_AXI_LOCK_WIDTH_n -1:0]	I	AXI Read Lock Type. Provides additional information about the atomic characteristics of the transfer. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
arcache_n[(AXI_CACHEW-1):0]	I	AXI Read Cache Type. Provides additional information about the cacheable characteristics of the transfer. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arprot_n[(AXI_PROTW-1):0]	I	AXI Read Protection Type. Provides protection unit information for the transaction. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
aruser_n[(AXI_USERW-1):0]	I	AXI Read Address User. Travels with the read transaction and back to ruser with the read response. **Exists:** UMCTL2_A_AXI_n && UMCTL2_AXI_USER_WIDTH > 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arvalid_n	I	AXI Read Address Valid. Indicates that valid read address and control information are available. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
arready_n	O	AXI Read Address Ready. Indicates that the subordinate is ready to accept an address and associated control signals. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arqos_n[(AXI_QOSW-1):0]	I	AXI Read Quality of Service. Sideband signal to indicate the quality of service attributes of the read transaction. The arqos_n signalling is sticky, that is, it must remain stable when arvalid_n is asserted and arready_n is de-asserted. If enabled by UMCTL2_EXT_PORTPRIO hardware parameter, this signal determines the transaction priority for port arbitration. Higher values signify higher priority. This signal determines also the priority of the read transfer going into the CAM depending on the programming of the PCFGQOS0_n register. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arpoison_n	I	AXI Read poison. Sideband signal to indicate an invalid read transaction. When asserted, all zeros are returned at the output. If not needed, signal must be tied to zero. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
arpoison_intr_n	O	Read transaction poisoning interrupt. Cleared by register rd_poison_intr_clr. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arregion_n[(UMCTL2_AXI_REGION_WIDTH-1):0]	I	AXI 4 Read Address REGION signal. This signal is not used by the controller. **Exists:** UMCTL2_A_AXI4_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arurgentb_n	I	AXI Read Urgent Blue Queue. Off-band signal to indicate a blue queue urgent transaction. When asserted, if rd_port_urgent_en register is set, causes the port arbiter to switch immediately to read. It can be asserted anytime, it is not associated to any particular command. **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arurgentr_n	I	AXI Read Urgent Red Queue. Off-band signal to indicate a red queue urgent transaction. When asserted, if rd_port_urgent_en register is set, causes the port arbiter to switch immediately to read. It can be asserted anytime, it is not associated to any particular command. **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
raqb_wcount_n[XPI_RAQD_LG2_n-1:0]	O	Number of used positions in the Blue Read address FIFO (synchronous to core_ddrc_core_clk). Width XPI_RAQD_LG2_n = RoundUp(log2(`UMCTL2_AXI_RAQD_n)). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raqr_wcount_n[XPI_RAQD_LG2_n-1:0]	O	Number of used positions in the Red Read address FIFO (synchronous to core_ddrc_core_clk). Width XPI_RAQD_LG2_n = RoundUp(log2(`UMCTL2_AXI_RAQD_n)). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raqb_pop_n	O	Transaction read from the Blue Read address FIFO (synchronous to core_ddrc_core_clk). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raqb_push_n	O	Transaction written to the Blue Read address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
raqr_pop_n	O	Transaction read from the Red Read address FIFO (synchronous to core_ddrc_core_clk). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raqr_push_n	O	Transaction written to the Red Read address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_XPI_USE2RAQ_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arurgent_n	I	AXI Read Urgent. Off-band signal to indicate a read urgent transaction. When asserted, if rd_port_urgent_en register is set, causes the port arbiter to switch immediately to read. It can be asserted anytime, it is not associated to any particular command. **Exists:** UMCTL2_A_AXI_n && UMCTL2_XPI_USE2RAQ_n == 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raq_wcount_n[XPI_RAQD_LG2_n-1:0]	O	Number of used positions in the Read address FIFO (synchronous to core_ddrc_core_clk). XPI_RAQD_LG2_n = RoundUp(log2(`UMCTL2_AXI_RAQD_n)). **Exists:** UMCTL2_A_AXI_n && UMCTL2_XPI_USE2RAQ_n == 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-8 AXI Port n Read Address Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
raq_pop_n	O	Transaction read from the Read address FIFO (synchronous to core_ddrc_core_clk). **Exists:** UMCTL2_A_AXI_n && UMCTL2_XPI_USE2RAQ_n == 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raq_push_n	O	Transaction written to the Read address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_A_AXI_n && UMCTL2_XPI_USE2RAQ_n == 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
raq_split_n	O	First portion of a wrap burst going to the Read address FIFO (synchronous to aclk_n). **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
arautopre_n	I	AXI auto-precharge signal for read command. This port is for read address channel signal. The hif_cmd_autopre(hif_rcmd_autopre) is asserted when this signal is high. This signal is valid when arvalid_n is high. This port is available with DDR4 only. This port can not be used with LPDDR5, LPDDR4 and DDR5. In such protocols, this should be kept low. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.9 AXI Port n Read Address On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

arparity_n -

Table 2-9 AXI Port n Read Address On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Port Name	I/O	Description
arparity_n[(OCPAR_ADDR_PARITY_WIDTH-1):0]	I	AXI Read address parity. **Exists:** UMCTL2_A_AXI_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.10 AXI Port n Read Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

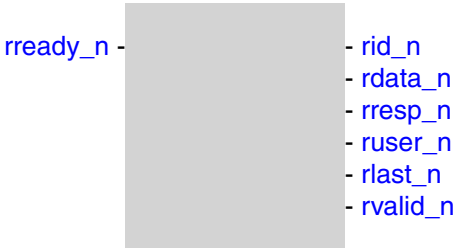


Table 2-10 AXI Port n Read Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
rid_n[(UMCTL2_A_IDW-1):0]	O	AXI Read ID. Must match the arid value of the read transaction to which the subordinate is responding. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdata_n[`UMCTL2_PORT_DW_n-1:0]	O	AXI Read Data. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rresp_n[(AXI_RESPW-1):0]	O	AXI Read Response. Indicates the status of the read transfer. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ruser_n[(AXI_USERW-1):0]	O	AXI Read Response User. Mirror of aruser sent with read transaction. **Exists:** UMCTL2_A_AXI_n && UMCTL2_AXI_USER_WIDTH > 0 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-10 AXI Port n Read Data Channel (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
rlast_n	O	AXI Read Last. Indicates the last transfer in a read burst. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rvalid_n	O	AXI Read Valid. Indicates that the required read data is available and the read transfer can complete. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rready_n	I	AXI Read Ready. Indicates that the master can accept the read data and response information. **Exists:** UMCTL2_A_AXI_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.11 AXI Port n Read Data On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Table 2-11 AXI Port n Read Data On-Chip Parity Signals (for n = 0; n <= UMCTL2_A_NPORTS-1)

Port Name	I/O	Description
rparity_n[`UMCTL2_PORT_NBYTES_n-1 :0]	O	AXI Read parity/ECC. **Exists:** UMCTL2_A_AXI_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.12 Read Reorder Buffer Data RAM Interface (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

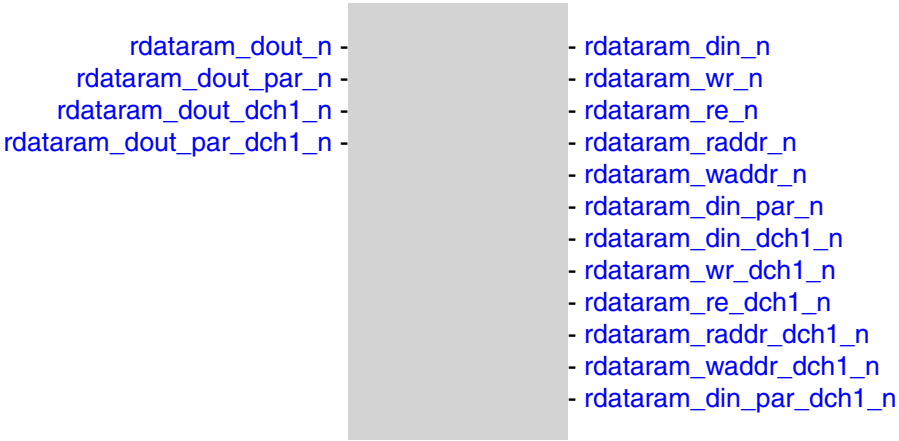


Table 2-12 Read Reorder Buffer Data RAM Interface (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals

Port Name	I/O	Description
rdataram_dout_n[(UMCTL2_RDATARAM_DW-1):0]	I	Read data coming from the Read Reorder Buffer Data RAM. Valid data comes out one clock after rdataram_re = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_din_n[(UMCTL2_RDATARAM_DW-1):0]	O	Data for the write operation. Valid with rdataram_wr = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_wr_n	O	Write signal to the RRB data RAM. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-12 Read Reorder Buffer Data RAM Interface (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
rdataram_re_n	O	Read signal to the RRB data RAM. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_raddr_n[(UMCTL2_RDATARAM_AW-1):0]	O	Read address to the RRB data RAM. Valid with rdataram_re = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_waddr_n[(UMCTL2_RDATARAM_AW-1):0]	O	Write address for the write operation. Valid with rdataram_wr = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_dout_par_n[(UMCTL2_DATARAM_PAR_DW-1):0]	I	Read data parity/ECC for rdataram_dout. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_din_par_n[(UMCTL2_DATARAM_PAR_DW-1):0]	O	Read data parity/ECC for rdataram_din. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-12 Read Reorder Buffer Data RAM Interface (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
rdataram_dout_dch1_n[(UMCTL2_RDATARAM_DW_DCH1-1):0]	I	Read data coming from the Read Reorder Buffer Data RAM (channel 1). Valid data comes out one clock after rdataram_re_dch1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_din_dch1_n[(UMCTL2_RDATARAM_DW_DCH1-1):0]	O	Data for the write operation (channel 1). Valid with rdataram_wr_dch1 = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_wr_dch1_n	O	Write signal to the RRB data RAM (channel 1). **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_re_dch1_n	O	Read signal to the RRB data RAM (channel 1). **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-12 Read Reorder Buffer Data RAM Interface (for n = 0; n <= UMCTL2_A_NPORTS-1) Signals (continued)

Port Name	I/O	Description
rdataram_raddr_dch1_n[(UMCTL2_RDATARAM_AW-1):0]	O	Read address to the RRB data RAM (channel 1). Valid with rdataram_re_dch1 = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_waddr_dch1_n[(UMCTL2_RDATARAM_AW-1):0]	O	Write address for the write operation (channel 1). Valid with rdataram_wr_dch1 = 1. **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_dout_par_dch1_n[(UMCTL2_DATARAM_PAR_DW_DCH1-1):0]	I	Read data parity for rdataram_dout_dch1 (channel 1). **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rdataram_din_par_dch1_n[(UMCTL2_DATARAM_PAR_DW_DCH1-1):0]	O	Read data parity for rdataram_din_dch1 (channel 1). **Exists:** UMCTL2_RRB_EXTRAM_ENABLED_n && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1 && UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.13 Write Data Parity Signals

- par_wdata_err_intr
- par_wdata_err_intr_fault
- par_wdata_err_intr_dch1
- par_wdata_err_intr_fault_dch1

Table 2-13 Write Data Parity Signals

Port Name	I/O	Description
par_wdata_err_intr	O	On-Chip Write data parity error interrupt. **Exists:** UMCTL2_OCPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_wdata_err_intr_fault[1:0]	O	On-Chip Write data parity error fault. This is a version of par_wdata_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_wdata_err_intr_dch1	O	On-Chip Write data parity error interrupt (channel 1). **Exists:** (UMCTL2_OCPAR_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-13 Write Data Parity Signals (continued)

Port Name	I/O	Description
par_wdata_err_intr_fault_dch1[1:0]	O	On-Chip Write data parity error fault (channel 1). This is a version of par_wdata_err_intr_dch1 which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** (UMCTL2_OCPAR_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.14 Read Data Parity Signals

- par_rdata_err_intr
- par_rdata_err_intr_fault
- par_rdata_err_intr_dch1
- par_rdata_err_intr_fault_dch1

Table 2-14 Read Data Parity Signals

Port Name	I/O	Description
par_rdata_err_intr	O	On-Chip Read data parity error interrupt. **Exists:** UMCTL2_OCPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_rdata_err_intr_fault[1:0]	O	On-Chip Read data parity error fault. This is a version of par_rdata_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_rdata_err_intr_dch1	O	On-Chip Read data parity error interrupt (channel 1). **Exists:** (UMCTL2_OCPAR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-14 Read Data Parity Signals (continued)

Port Name	I/O	Description
par_rdata_err_intr_fault_dch1[1:0]	O	On-Chip Read data parity error fault (channel 1). This is a version of par_rdata_err_intr_dch1 which can not be disabled or forced through register.It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** (UMCTL2_OCPAR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.15 Write Address Parity Signals

- par_waddr_err_intr
- par_waddr_err_intr_fault

Table 2-15 Write Address Parity Signals

Port Name	I/O	Description
par_waddr_err_intr	O	AXI Write address parity error interrupt. **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_waddr_err_intr_fault[1:0]	O	AXI Write address parity error fault. This is a version of par_waddr_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.16 Read Address Parity Signals

- par_raddr_err_intr
- par_raddr_err_intr_fault

Table 2-16 Read Address Parity Signals

Port Name	I/O	Description
par_raddr_err_intr	O	AXI Read address parity error interrupt. **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
par_raddr_err_intr_fault[1:0]	O	AXI Read address parity error fault. This is a version of par_raddr_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.17 On-Chip Command/Address Path Protection Signals

- occap_arb_err_intr
- occap_arb_err_intr_fault
- occap_ddrc_ctrl_err_intr
- occap_ddrc_ctrl_err_intr_fault
- occap_ddrc_ctrl_err_intr_dch1
- occap_ddrc_ctrl_err_intr_fault_dch1
- occap_ddrc_data_err_intr
- occap_ddrc_data_err_intr_fault
- occap_ddrc_data_err_intr_dch1
- occap_ddrc_data_err_intr_fault_dch1
- occap_dfiic_err_intr
- occap_dfiic_err_intr_fault

Table 2-17 On-Chip Command/Address Path Protection Signals

Port Name	I/O	Description
occap_arb_err_intr	O	On-Chip Command/Address Path Protection Arbiter interrupt. **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_arb_err_intr_fault[1:0]	O	On-Chip Command/Address Path Protection Arbiter fault. This is a version of occap_arb_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_ctrl_err_intr	O	On-Chip Command/Address Path Protection DDRC_CTRL interrupt. **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-17 On-Chip Command/Address Path Protection Signals (continued)

Port Name	I/O	Description
occap_ddrc_ctrl_err_intr_fault[1:0]	O	On-Chip Command/Address Path Protection DDRC_CTRL fault. This is a version of occap_ddrc_ctrl_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_ctrl_err_intr_dch1	O	On-Chip Command/Address Path Protection DDRC_CTRL interrupt (channel 1). **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_ctrl_err_intr_fault_dch1[1:0]	O	On-Chip Command/Address Path Protection DDRC_CTRL fault (channel 1). This is a version of occap_ddrc_ctrl_err_intr_dch1 which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_data_err_intr	O	On-Chip Command/Address Path Protection DDRC Data interrupt. **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-17 On-Chip Command/Address Path Protection Signals (continued)

Port Name	I/O	Description
occap_ddrc_data_err_intr_fault[1:0]	O	On-Chip Command/Address Path Protection DDRC Data fault. This is a version of occap_ddrc_data_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_data_err_intr_dch1	O	On-Chip Command/Address Path Protection DDRC Data interrupt (channel 1). **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_ddrc_data_err_intr_fault_dch1[1:0]	O	On-Chip Command/Address Path Protection DDRC Data fault (channel 1). This is a version of occap_ddrc_data_err_intr_dch1 which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** (UMCTL2_OCCAP_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
occap_dfiic_err_intr	O	On-Chip Command/Address Path Protection DFI interconnect interrupt. **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-17 On-Chip Command/Address Path Protection Signals (continued)

Port Name	I/O	Description
occap_dfiic_err_intr_fault[1:0]	O	On-Chip Command/Address Path Protection DFI interconnect fault. This is a version of occap_dfiic_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCCAP_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.18 On-Chip ECC Signals

- ococc_uncorrected_err_intr
- ococc_uncorrected_err_intr_fault

Table 2-18 On-Chip ECC Signals

Port Name	I/O	Description
ococc_uncorrected_err_intr	O	On-Chip ECC uncorrected error interrupt. Asserted when a 2-bit error or an odd number of bit errors is detected by any of the ECC decoders or when a parity error is detected by any of the parity checkers. **Exists:** UMCTL2_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ococc_uncorrected_err_intr_fault[1:0]	O	On-Chip ECC uncorrected error fault. This is a version of ococc_uncorrected_err_intr which can not be disabled or forced via register. It is a 2-bit antivalent signal with encoding of ■ 01 - No Fault ■ 10 - Fault Detected **Exists:** UMCTL2_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.19 HIF Read Command Interface Signals

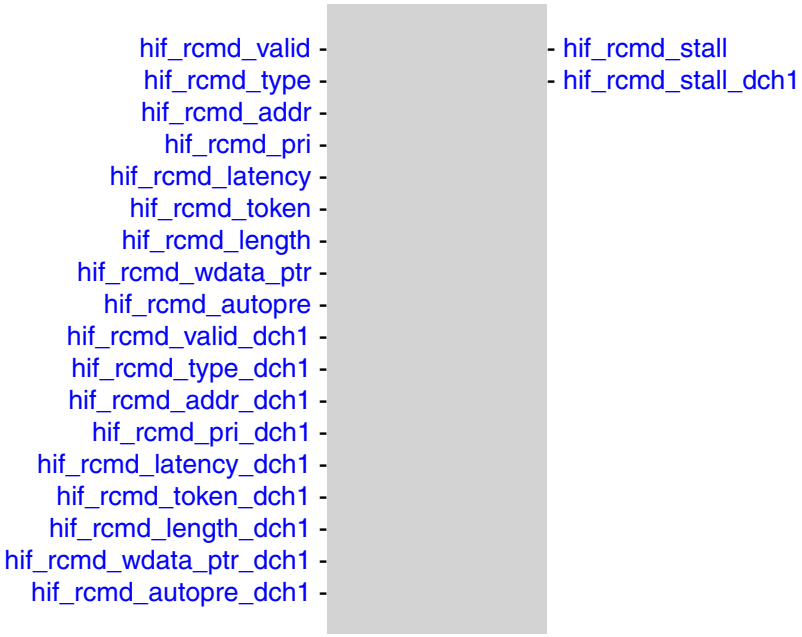


Table 2-19 HIF Read Command Interface Signals

Port Name	I/O	Description
hif_rcmd_valid	I	Valid Read command request to the controller. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_type[1:0]	I	Valid when hif_rcmd_valid is high. Determines the type of command being issued: ■ 00 - Reserved ■ 01 - Read ■ 10 - Reserved ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_addr[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_rcmd_valid is high. Word address of the read or write request being made. Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the DDRCTL, though several of the upper-most bits are generally be unused. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_pri[UMCTL2_VPR_EN_VAL:0]	I	Valid when hif_rcmd_valid is high. Determines the priority of command being issued. If UMCTL2_VPRW_EN=0, valid when hif_rcmd_type indicates a read. Don't care for writes. Must be set to 0 for RMWs. ■ 0 - Low priority read ■ 1 - High priority read ■ If UMCTL2_VPRW_EN=1 Indicates the priority of a read/write request. hif_rcmd_pri[1] must be set to 0 for RMWs. ■ 00 - Low priority read/write ■ 01 - Variable priority read/write ■ 10 - High priority read ■ 11 - Reserved (High priority read pushed into LPR CAM. Contact Synopsys for more info.) **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_latency[(HIF_RQOS_TW-1):0]	I	Valid when hif_rcmd_valid is high and hif_rcmd_pri indicates variable priority read (VPR). Don't care for other priority types. Specifies the timeout value of VPR request. The controller start down counting VPR timer when the request is accepted in the controller. If VPR timeout value is set to 0, the VPR request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_token[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_rcmd_valid is high and hif_rcmd_type indicates a read. Don't care for writes. Token bits are provided with read requests and returned later with read data. For DDRCTL, common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_length[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_rcmd_valid is high and hif_rcmd_type indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data words (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_wdata_ptr[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Don't care for reads. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_autopre	I	Valid when hif_rcmd_valid is high. Indicates that the command should be issued to memory with an auto-precharge. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_stall	O	HIF Read commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_valid_dch1	I	Valid Read command request to the controller (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_type_dch1[1:0]	I	Valid when hif_rcmd_valid_dch1 is high. Determines the type of command being issued (channel 1): ■ 00 - Reserved ■ 01 - Read ■ 10 - Reserved ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_addr_dch1[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_rcmd_valid=1. Word address of the read or write request being made (channel 1). Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the controller, though several of the upper-most bits are generally be unused. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_pri_dch1[UMCTL2_VPR_EN_VAL:0]	I	For DDRCTL, Valid when hif_rcmd_valid_dch1 is high and hif_rcmd_type_dch1 indicates a read (channel 1). Don't care for writes. Must be set to 0 for RMWs Indicates the priority of a read request. ■ 1 - High priority read ■ 0 - Low priority read **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_latency_dch1[(HIF_RQOS_TW-1):0]	I	Valid when hif_rcmd_valid_dch1 is high and hif_rcmd_pri_dch1 indicates variable priority read/write (VPR/VPW) (channel 1). Don't care for other priority types. Specifies the timeout value of VPR/VPW request. The controller start down counting VPR/VPW timer when the request is accepted in the controller. If VPR/VPW timeout value is set to 0, the VPR/VPW request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_token_dch1[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_rcmd_valid_dch1 and hif_rcmd_type_dch1 indicates a read (channel 1). Don't care for writes. Token bits are provided with read requests and returned later with read data. Common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_length_dch1[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_rcmd_valid_dch1 is high and hif_rcmd_type_dch1 indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data word (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-19 HIF Read Command Interface Signals (continued)

Port Name	I/O	Description
hif_rcmd_wdata_ptr_dch1[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Valid when hif_rcmd_valid_dch1 is high and hif_rcmd_type indicates a write. Pointer bits are provided with write requests and returned later with write pointer return corresponding to the write command issued (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_autopre_dch1	I	Valid when hif_rcmd_valid_dch1 is high. Indicates that the command should be issued to memory with an auto-precharge (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rcmd_stall_dch1	O	HIF Read commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.20 HIF Write Command Interface Signals

Table 2-20 HIF Write Command Interface Signals

Port Name	I/O	Description
hif_wcmd_valid	I	Valid Write command request to the controller. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_type[1:0]	I	Valid when hif_wcmd_valid is high. Determines the type of command being issued: ■ 00 - Write ■ 01 - Reserved ■ 10 - RMW (DDRCTL only) ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_addr[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_wcmd_valid is high. Word address of the read or write request being made. Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the DDRCTL, though several of the upper-most bits are generally be unused. hif_wcmd_addr[3:0] refer to the critical word if MEMC_BURST_LENGTH=16. When critical word is not zero, interleaved/sequential ordering is used for writing data or returning read responses. See JEDEC specification for information on interleaved/sequential data ordering. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_pri[UMCTL2_VPR_EN_VAL:0]	I	Valid when hif_wcmd_valid is high. Determines the priority of command being issued. If UMCTL2_VPRW_EN=0, this signal is meaningless. If UMCTL2_VPRW_EN=1, indicates the priority of a write request. hif_wcmd_pri[1] must be set to 0 for RMWs. ■ 00 - Normal priority write ■ 01 - Variable priority write ■ 10 - Reserved ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_latency[(HIF_RQOS_TW-1):0]	I	Valid when hif_wcmd_valid is high and hif_wcmd_pri indicates variable priority write (VPW). Don't care for other priority types. Specifies the timeout value of VPW request. The controller start down counting VPW timer when the request is accepted in the controller. If VPW timeout value is set to 0, the VPW request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_token[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_wcmd_valid is high and hif_wcmd_type indicates a read. Don't care for writes. Token bits are provided with read requests and returned later with read data. For DDRCTL, common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_length[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_wcmd_valid is high and hif_wcmd_type indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data words (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_wdata_ptr[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Valid when hif_wcmd_valid is high and hif_wcmd_type indicates a write. Pointer bits are provided with write requests and returned later with write pointer return corresponding to the write command issued. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_autopre	I	Valid when hif_wcmd_valid is high. Indicates that the command should be issued to memory with an auto-precharge. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_stall	O	HIF Write commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_valid_dch1	I	Valid Write command request to the controller (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_type_dch1[1:0]	I	Valid when hif_wcmd_valid_dch1 is high. Determines the type of command being issued (channel 1): ■ 00 - Write ■ 01 - Reserved ■ 10 - RMW (DDRCTL only) ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_addr_dch1[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_wcmd_valid=1. Word address of the read or write request being made (channel 1). Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the controller, though several of the upper-most bits are generally be unused. hif_wcmd_addr[3:0] refer to the critical word if MEMC_BURST_LENGTH=16. When critical word is not zero, interleaved/sequential ordering is used for writing data or returning read responses. See JEDEC specification for information on interleaved/sequential data ordering. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_pri_dch1[UMCTL2_VPR_EN_VAL:0]	I	For DDRCTL, Valid when hif_wcmd_valid_dch1 is high and hif_wcmd_type_dch1 indicates a read (channel 1). Don't care for writes. Must be set to 0 for RMWs. Indicates the priority of a read request. ■ 1 - High priority read ■ 0 - Low priority read **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_latency_dch1[(HIF_RQOS_TW-1):0]	I	Valid when hif_wcmd_valid_dch1 is high and hif_wcmd_pri_dch1 indicates variable priority read/write (VPR/VPW) (channel 1). Don't care for other priority types. Specifies the timeout value of VPR/VPW request. The controller start down counting VPR/VPW timer when the request is accepted in the controller. If VPR/VPW timeout value is set to 0, the VPR/VPW request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_token_dch1[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_wcmd_valid_dch1 and hif_wcmd_type_dch1 indicates a read (channel 1). Don't care for writes. Token bits are provided with read requests and returned later with read data. Common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_length_dch1[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_wcmd_valid_dch1 is high and hif_wcmd_type_dch1 indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data words (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_wdata_ptr_dch1[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Valid when hif_wcmd_valid_dch1 is high and hif_wcmd_type indicates a write. Pointer bits are provided with write requests and returned later with write pointer return corresponding to the write command issued (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wcmd_autopre_dch1	I	Valid when hif_wcmd_valid_dch1 is high. Indicates that the command should be issued to memory with an auto-precharge (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-20 HIF Write Command Interface Signals (continued)

Port Name	I/O	Description
hif_wcmd_stall_dch1	O	HIF Write commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.21 HIF Command Interface Signals

Table 2-21 HIF Command Interface Signals

Port Name	I/O	Description
hif_cmd_valid	I	Valid command request to the controller. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_type[1:0]	I	Valid when hif_cmd_valid is high. Determines the type of command being issued: ■ 00 - Write ■ 01 - Read ■ 10 - RMW ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_addr[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_cmd_valid is high. Word address of the read or write request being made. Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the DDRCTL, though several of the upper-most bits are generally be unused. hif_cmd_addr[3:0] refer to the critical word if MEMC_BURST_LENGTH=16. When critical word is not zero, interleaved/sequential ordering is used for writing data or returning read responses. See JEDEC specification for information on interleaved/sequential data ordering. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_pri[UMCTL2_VPR_EN_VAL:0]	I	Valid when hif_cmd_valid is high. Determines the priority of command being issued. If UMCTL2_VPRW_EN=0, valid when hif_cmd_type indicates a read. Don't care for writes. Must be set to 0 for RMWs. ■ 0 - Low priority read ■ 1 - High priority read ■ If UMCTL2_VPRW_EN=1, indicates the priority of a read/write request hif_cmd_pri[1] must be set to 0 for RMWs ■ 00 - Low priority read/write ■ 01 - Variable priority read/write ■ 10 - High priority read ■ 11 - Reserved (High priority read pushed into LPR CAM. Cnotact Synopsys for more info.) **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_latency[(HIF_RQOS_TW-1):0]	I	Valid when hif_cmd_valid is high and hif_cmd_pri indicates variable priority read/write (VPR/VPW). Don't care for other priority types. Specifies the timeout value of VPR/VPW request. The controller start down counting VPR/VPW timer when the request is accepted in the controller. If VPR/VPW timeout value is set to 0, the VPR/VPW request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_token[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_cmd_valid is high and hif_cmd_type indicates a read. Don't care for writes. Token bits are provided with read requests and returned later with read data. For DDRCTL, common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_length[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_cmd_valid is high and hif_cmd_type indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b01 and 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data word (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_wdata_ptr[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Valid when hif_cmd_valid is high and hif_cmd_type indicates a write. Pointer bits are provided with write requests and returned later with write pointer return corresponding to the write command issued. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_autopre	I	Valid when hif_cmd_valid is high. Indicates that the command should be issued to memory with an auto-precharge. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_wdata_mask_full[(WRDATA_CYCLES-1):0]	I	When 1, all bytes for the relevant HIF data beat are to be written. When 0, some or all of the bytes for the relevant HIF data beat are masked. Each bit corresponds to each HIF data beat in turn that is, hif_cmd_wdata_mask_full[0] corresponds to the 1st HIF data beat, hif_cmd_wdata_mask_full[1] corresponds to the 2nd HIF data beat, and so on. Used to determine if Masked Write (MWR) command is required or not. Valid only if LPDDR4 enabled, Valid only if posted write is enabled, Valid if Inline ECC enabled. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_HIF_CMD_WDATA_MASK_FULL_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_go2critical_hpr	I	For DDRCTL, asserting this causes the HPR queue to go to the Critical state immediately, bypassing the starvation mechanism. This also causes the Controller to switch to Read mode, if it is currently in Write mode. This signal is provided to externally control the Read/Write switching in the Controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the Controller start to fill up. See the section "Command Scheduling in DDRC" for more details on the read queue and write queue. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_go2critical_lpr	I	For DDRCTL, asserting this causes the LPR queue to go to the Critical state immediately, bypassing the starvation mechanism. This also causes the controller to switch to Read mode, if it is currently in Write mode. This signal is provided to externally control the Read/Write switching in the controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the controller start to fill up. For more information on the read queue and write queue, see "Command Scheduling in DDRC" section. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_go2critical_wr	I	For DDRCTL, asserting this causes the WR queue to go to the Critical state immediately, bypassing the starvation mechanism. This does not explicitly cause the controller to switch to Write mode, if it is currently in Read mode. The switch happens only if the LPR and HPR queues are not currently in critical state. This signal is provided to externally control the Read/Write switching in the controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the controller start to fill up. For more information on the read queue and write queue,, see "Command Scheduling in DDRC" section. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_stall	O	HIF commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_ptr[(MEMC_HIF_WDATA_PTR_BITS-1):0]	O	Valid when hif_wdata_ptr_valid is high. Write pointer bits are returned to indicate that SoC can send the corresponding write data. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_wdata_ptr_valid	O	Valid indication for the hif_wdata_ptr signal. This goes high when a write command is received. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_ptr_addr_err	O	Valid when hif_wdata_ptr_valid is high. A 1 on this signal indicates that the HIF write request, denoted by pointer hif_wdata_ptr, has invalid address. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_ADDR_ERR_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_lpr_credit[(MEMC_HIF_CREDIT_BITS -1):0]	O	Indicates that a low priority read request has been scheduled to the DDR and the SoC must increment the credit value associated with low priority reads. **Note:**In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is reserved in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. In Inline ECC configuration, it is expend to 2 bits. Bit0 indicate that credit increment pulse from the CAM; Bit1 indicate credit increment pulse from the IH whenever the command does not need to inject an overhead command. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_wr_credit	O	Indicates that a write request and write data have been scheduled to the DDR, or that a Write Combine has occurred, and the SoC must increment the credit value associated with writes. **Note:**In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is reserved in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_hpr_credit[(MEMC_HIF_CREDIT_BITS-1):0]	O	For DDRCTL, indicates that a high priority read request has been scheduled to the DDR and the SoC must increment the credit value associated with high priority reads. In Inline ECC configuration, it is expend to 2 bits. ■ Bit0 indicates that credit increment pulse from the CAM. ■ Bit1 indicates that credit increment pulse from the IH whenever the command does not need to inject an overhead command. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_wrecc_credit[1:0]	O	Indicates that an ECC write request has been scheduled to the DDR and the SoC must increment the credit value associated with ECC writes. This is there only with Inline ECC configuration, it is 2 bits. ■ Bit0 indicates that credit increment pulse from the CAM. ■ Bit1 indicates that credit increment pulse from the IH whenever the command does not need to inject an overhead command due to address error. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_q_not_empty	O	If asserted, indicates that the write and/or read CAMs in the controller are not empty. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_valid_dch1	I	Valid command request to the controller (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_type_dch1[1:0]	I	Valid when hif_cmd_valid_dch1 is high. Determines the type of command being issued (channel 1): ■ 00 - Write ■ 01 - Read ■ 10 - RMW (DDRCTL only) ■ 11 - Reserved **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_addr_dch1[(MEMC_HIF_ADDR_WIDTH_MAX-1):0]	I	Valid when hif_cmd_valid=1. Word address of the read or write request being made (channel 1). Word size (in bits) is defined as the configuration parameter MEMC_DRAM_DATA_WIDTH. This bus is MEMC_HIF_ADDR_WIDTH_MAX bits into the controller, though several of the upper-most bits are generally be unused. hif_cmd_addr[3:0] refer to the critical word if MEMC_BURST_LENGTH=16. When critical word is not zero, interleaved/sequential ordering is used for writing data or returning read responses. See JEDEC specification for information on interleaved/sequential data ordering. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_pri_dch1[UMCTL2_VPR_EN_VAL:0]	I	For DDRCTL, Valid when hif_cmd_valid_dch1 is high and hif_cmd_type_dch1 indicates a read (channel 1). Don't care for writes. Must be set to 0 for RMWs Indicates the priority of a read request. ■ 1 - High priority read ■ 0 - Low priority read **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_latency_dch1[(HIF_RQOS_TW-1):0]	I	Valid when hif_cmd_valid_dch1 is high and hif_cmd_pri_dch1 indicates variable priority read/write (VPR/VPW) (channel 1). Don't care for other priority types. Specifies the timeout value of VPR/VPW request. The controller start down counting VPR/VPW timer when the request is accepted in the controller. If VPR/VPW timeout value is set to 0, the VPR/VPW request expires immediately as it enter the controller, thereby making it highest priority transaction class within the device. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_token_dch1[(MEMC_HIF_TAGBITS-1):0]	I	Valid when hif_cmd_valid_dch1 and hif_cmd_type_dch1 indicates a read (channel 1). Don't care for writes. Token bits are provided with read requests and returned later with read data. Common uses for these bits include identifying the requester and re-ordering read data which may be returned out-of-order. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_length_dch1[(UMCTL2_CMD_LEN_BITS-1):0]	I	Valid when hif_cmd_valid_dch1 is high and hif_cmd_type_dch1 indicates a Read. This signal is ignored for Write or RMW. Indicates the number of requested words **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 4** ■ 2'b00 - Full RD of 2 HIF data words ■ 2'b10 - Partial (Half) RD of 1 HIF data words ■ 2'b01 and 2'b11 - Invalid **If MEMC_BURST_LENGTH = 16 and MEMC_FREQ_RATIO = 2** ■ 2'b00 - Full RD of 4 HIF data words ■ 2'b10 - Partial (Half) RD of 2 HIF data words ■ 2'b11 - Partial (Quarter) RD of 1 HIF data words (Not supported for ECCCFG0.ecc_mode=5 and ECCCFG0.ecc_type=1) ■ 2'b01 - Invalid **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_wdata_ptr_dch1[(MEMC_HIF_WDATA_PTR_BITS-1):0]	I	Valid when hif_cmd_valid_dch1 is high and hif_cmd_type_dch1 indicates a write. Pointer bits are provided with write requests and returned later with write pointer return corresponding to the write command issued (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_autopre_dch1	I	Valid when hif_cmd_valid_dch1 is high. Indicates that the command should be issued to memory with an auto-precharge (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_wdata_mask_full_dch1[(WRDATA_CYCLES-1):0]	I	When 1, all bytes for the relevant HIF data beat are to be written (channel 1). When 0, some or all of the bytes for the relevant HIF data beat are masked. Each bit corresponds to each HIF data beat in turn that is, hif_cmd_wdata_mask_full_dch1[0] corresponds to the 1st HIF data beat, hif_cmd_wdata_mask_full_dch1[1] corresponds to the 2nd HIF data beat, and so on. Used to determine if Masked Write (MWR) command is required or not. Valid only if LPDDR4 enabled, Valid only if posted write is enabled, Valid if Inline ECC enabled. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_HIF_CMD_WDATA_MASK_FULL_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_go2critical_hpr_dch1	I	For DDRCTL, asserting this causes the HPR queue to go to the Critical state immediately, bypassing the starvation mechanism (channel 1). This also causes the controller to switch to Read mode, if it is currently in Write mode. This signal is provided to externally control the Read/Write switching in the controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the controller start to fill up. For more information on the read queue and write queue, see the section "Command Scheduling in DDRC" section. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_go2critical_lpr_dch1	I	For DDRCTL, asserting this causes the LPR queue to go to the Critical state immediately, bypassing the starvation mechanism (channel 1). This also causes the controller to switch to Read mode, if it is currently in Write mode. This signal is provided to externally control the Read/Write switching in the controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the controller start to fill up. For more information on the read queue and write queue, see the section "Command Scheduling in DDRC" section. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_go2critical_wr_dch1	I	For DDRCTL, asserting this causes the WR queue to go to the Critical state immediately, bypassing the starvation mechanism (channel 1). This does not explicitly cause the controller to switch to Write mode, if it is currently in Read mode. The switch happens only if the LPR and HPR queues are not currently in critical state. This signal is provided to externally control the Read/Write switching in the controller. This can be used by the external logic to switch the Read/Write mode if the read or write command queues outside the controller start to fill up. For more information on the read queue and write queue, see the section "Command Scheduling in DDRC" section. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_cmd_stall_dch1	O	HIF commands are not accepted starting from the first clock edge after the stall goes high until the clock edge on which stall is detected low (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_ptr_dch1[(MEMC_HIF_WDATA_PTR_BITS-1):0]	O	Valid when hif_wdata_ptr_valid_dch1 is high (channel 1). Write pointer bits are returned to indicate that SoC can send the corresponding write data. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_ptr_valid_dch1	O	Valid indication for the hif_wdata_ptr_dch1 signal (channel 1). This goes high when a write command is received. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_ptr_addr_err_dch1	O	Valid when hif_wdata_ptr_valid_dch1 is high. A 1 on this signal indicates that the HIF write request, denoted by pointer hif_wdata_ptr, has invalid address (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ADDR_ERR_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_lpr_credit_dch1[(MEMC_HIF_CREDIT_BITS-1):0]	O	Indicates that a low priority read request has been scheduled to the DDR and the SoC must increment the credit value associated with low priority reads (channel 1). **Note:**In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is reserved in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. In Inline ECC configuration, it is expend to 2 bits. ■ Bit0 indicates that the credit increment pulse from the CAM ■ Bit1 indicates that the credit increment pulse from the IH whenever the command does not need to inject an overhead command. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wr_credit_dch1	O	Indicates that a write request and write data have been scheduled to the DDR, or that a Write Combine has occurred, and the SoC must increment the credit value associated with writes (channel 1). **Note:**In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is reserved in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. In Inline ECC configuration, it is expend to 2 bits. ■ Bit0 indicates that the credit increment pulse from the CAM. ■ Bit1 indicates that the credit increment pulse from the IH whenever the command does not need to inject an overhead command. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-21 HIF Command Interface Signals (continued)

Port Name	I/O	Description
hif_hpr_credit_dch1[(MEMC_HIF_CREDIT_BITS-1):0]	O	Indicates that a high priority read request has been scheduled to the DDR and the SoC must increment the credit value associated with high priority reads (channel 1). In Inline ECC configuration, it is expend to 2 bits. ■ Bit0 indicates that the credit increment pulse from the CAM. ■ Bit1 indicates that the credit increment pulse from the IH whenever the command does not need to inject an overhead command. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wrecc_credit_dch1[1:0]	O	Indicates that an ECC write request has been scheduled to the DDR and the SoC must increment the credit value associated with ECC writes (channel 1). This is there only with Inline ECC configuration, it is 2 bits. ■ Bit0 indicates that the credit increment pulse from the CAM. ■ Bit1 indicates that the credit increment pulse from the IH whenever the command does not need to inject an overhead command due to address error. Both bits can be assert at the same time, and in that case the SoC needs to increment credits by 2. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_cmd_q_not_empty_dch1	O	If asserted, indicates that the write and/or read CAMs in the controller are not empty (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.22 HIF Write Data Interface Signals

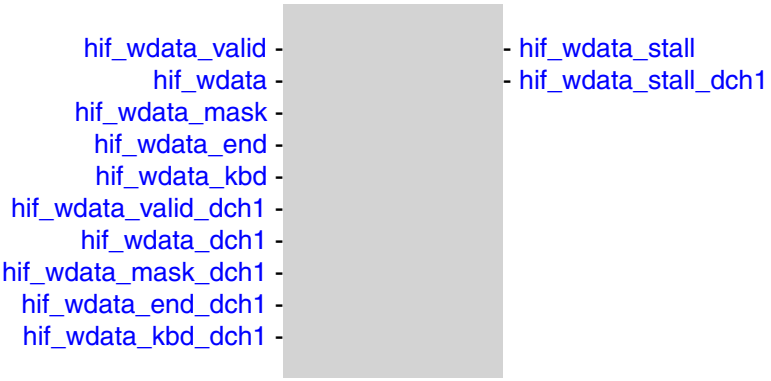


Table 2-22 HIF Write Data Interface Signals

Port Name	I/O	Description
hif_wdata_valid	I	Valid for the write data bus (hif_wdata) **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata[(((MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO)*2)-1):0]	I	Write data bus. Valid when hif_wdata_valid is high. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-22 HIF Write Data Interface Signals (continued)

Port Name	I/O	Description
hif_wdata_mask[((((MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO)*2)/8)-1):0]	I	Write data mask bus. One bit of hif_wdata_mask signal is for each byte of data. ■ hif_wdata_mask[0] is for hif_wdata[7:0] ■ hif_wdata_mask[1] is for hif_wdata[15:8] (and so on.) ■ 1: The byte is written to SDRAM ■ 0: The byte is not written to SDRAM Valid when hif_wdata_valid = 1 When DDR4 SDRAM is used and data mask is disabled, this signal must set to all 1 in Write command. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_end	I	Valid when hif_wdata_valid is high. Indicates the final write data phase for a write command. For MEMC_BURST_LENGTH = 16, MEMC_FREQ_RATIO = 4, this is asserted on the second clock for a normal write command, or the first clock for a partial write command. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_kbd[(DDRCTL_HIF_KBD_WIDTH-1):0]	I	Write data KBD. Valid when hif_wdata_valid is high. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (DDRCTL_KBD_SBECC_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-22 HIF Write Data Interface Signals (continued)

Port Name	I/O	Description
hif_wdata_stall	O	Data and mask presented on the data interface is accepted by the controller, when hif_wdata_valid is detected high and hif_wdata_stall is detected low on the same positive edge of the clock. ■ For DDRCTL, hif_wdata_stall is asserted during a RMW operation. When the DDRC writes the read data for the RMW into the write data SRAM, it blocks the HIF from sending any write data during those cycles. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_valid_dch1	I	Valid for the write data bus (hif_wdata) (channel 1) **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_dch1[(((MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO)*2)-1):0]	I	Write data bus (channel 1). Valid when hif_wdata_valid_dch1 is high. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-22 HIF Write Data Interface Signals (continued)

Port Name	I/O	Description
hif_wdata_mask_dch1[((((MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO)*2)/8)-1):0]	I	Write data mask bus (channel 1). One bit of hif_wdata_mask_dch1 signal is for each byte of data. ■ hif_wdata_mask_dch1[0] is for hif_wdata_dch1[7:0] ■ hif_wdata_mask_dch1[1] is for hif_wdata_dch1[15:8] (and so on.) ■ 1: The byte is written to SDRAM ■ 0: The byte is not written to SDRAM Valid when hif_wdata_valid_dch1 = 1. When DDR4 SDRAM is used and data mask is disabled, this signal must set to all 1 in Write command. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_end_dch1	I	Valid when hif_wdata_valid_dch1 is 1. Indicates the final write data phase for a write command (channel 1). For MEMC_BURST_LENGTH = 16, MEMC_FREQ_RATIO = 4, this is asserted on the second clock for a normal write command, or the first clock for a partial write command. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_wdata_kbd_dch1[(DDRCTL_HIF_KBD_WIDTH-1):0]	I	Write data KBD (channel 1). Valid when hif_wdata_valid_dch1 is high. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_KBD_SBECC_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-22 HIF Write Data Interface Signals (continued)

Port Name	I/O	Description
hif_wdata_stall_dch1	O	Data and mask presented on the data interface is accepted by the controller, when hif_wdata_valid_dch1 is detected high and hif_wdata_stall_dch1 is detected low on the same positive edge of the clock (channel 1). ■ For uMCLT2, hif_wdata_stall_dch1 is asserted during a RMW operation. When the DDRC writes the read data for the RMW into the write data SRAM, it blocks the HIF from sending any write data during those cycles. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.23 HIF Read Data Interface Signals

Table 2-23 HIF Read Data Interface Signals

Port Name	I/O	Description
hif_rdata_valid	O	Valid for the read response data. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_end	O	Valid when hif_rdata_valid is high. Indicates the final write data phase for a read command. For MEMC_BURST_LENGTH = 16, MEMC_FREQ_RATIO = 4, this is asserted on the second clock for a normal read command, or the first clock for a partial read command. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-23 HIF Read Data Interface Signals (continued)

Port Name	I/O	Description
hif_rdata_token[(MEMC_HIF_TAGBITS-1):0]	O	Token associated with the read command and the read data that is going out. Valid with hif_rdata_valid. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata[(((MEMC_DRAM_DATA_WIDTH *MEMC_FREQ_RATIO)*2)-1):0]	O	Read data. Valid when hif_rdata_valid is high. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_uncorr_ecc_err	O	A 1 on this signal indicates that the read data returned on 'hif_rdata_rdata' bus has uncorrectable ECC error on it. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_eapar_err	O	A 1 on this signal indicates that the read data returned on 'hif_rdata_rdata' bus has EAPAR error on it. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (DDRCTL_EAPAR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-23 HIF Read Data Interface Signals (continued)

Port Name	I/O	Description
hif_rdata_uncorr_linkecc_err	O	A 1 on this signal indicates that the read data returned on 'hif_rdata' bus has LinkECC uncorrectable error on it. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_LINK_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_addr_err	O	Valid when hif_rdata_valid is high. A 1 on this signal indicates that the read token returned on hif_rdata_token was associated with an invalid address. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (MEMC_ADDR_ERR_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_valid_dch1	O	Valid for the read response data (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_end_dch1	O	Indicates the end of the read data for a read command (channel 1). For MEMC_BURST_LENGTH = 16, MEMC_FREQ_RATIO = 4, this is asserted on the second clock for a full read command, or the first clock for a partial (half) read command. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-23 HIF Read Data Interface Signals (continued)

Port Name	I/O	Description
hif_rdata_token_dch1[(MEMC_HIF_TAGBITS-1):0]	O	Token associated with the read command and the read data that is going out (channel 1). SoC must use this for re-assembling the read data in order. Valid with hif_rdata_valid_dch1. **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_dch1[(((MEMC_DRAM_DATA_WIDTH*MEMC_FREQ_RATIO)*2)-1):0]	O	Read data. Valid when hif_rdata_valid_dch1 is high (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_uncorr_ecc_err_dch1	O	A 1 on this signal indicates that the read data returned on 'hif_rdata_rdata' bus has uncorrectable ECC error on it (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_rdata_eapar_err_dch1	O	A 1 on this signal indicates that the read data returned on 'hif_rdata_rdata' bus has EAPAR error on it (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_EAPAR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-23 HIF Read Data Interface Signals (continued)

Port Name	I/O	Description
hif_rdata_addr_err_dch1	O	Valid when hif_rdata_valid_dch1 is high. A 1 on this signal indicates that the read token returned on hif_rdata_token was associated with an invalid address (channel 1). **Exists:** (!UMCTL2_INCL_ARB_OR_CHB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ADDR_ERR_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.24 Write Data RAM Interface Signals

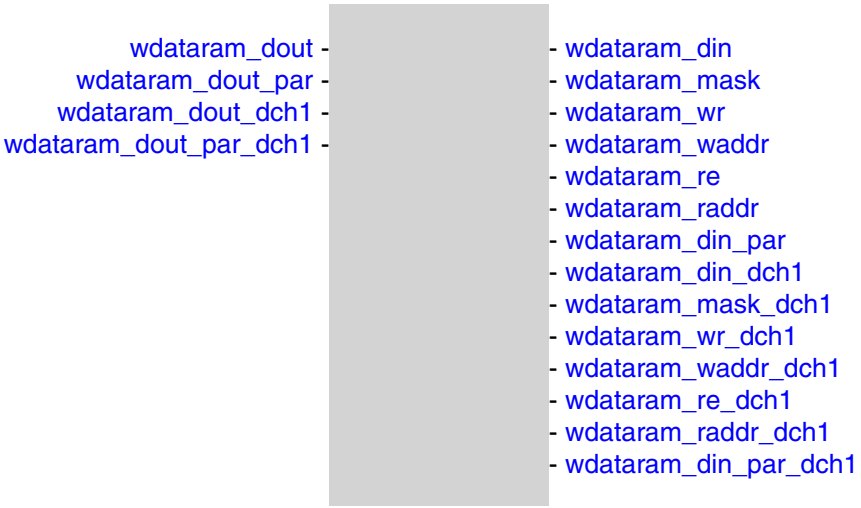


Table 2-24 Write Data RAM Interface Signals

Port Name	I/O	Description
wdataram_din[(UMCTL2_WDATARAM_DW-1):0]	O	Data for the write operation. Valid with wdataram_wr. In HIF configurations with ECC enabled, the width of this bus increases to include the ECC byte. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_dout[(UMCTL2_WDATARAM_DW-1):0]	I	Read data coming from the write data RAM. Valid data comes out one clock after wdataram_re = 1. In HIF configurations with ECC enabled, the width of this bus increases to include the ECC byte. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_mask[((UMCTL2_WDATARAM_DW/8)-1):0]	O	Mask for the write operation. One bit of wdataram_mask signal is for each byte of data. wdataram_mask[0] is for wdataram_din[7:0] wdataram_mask[1] is for wdataram_din[15:8] (and so on.) For On Chip Parity configurations (UMCTL2_OCPAR_EN==1) wdataram_mask[0] is for wdataram_din_par[0] wdataram_mask[1] is for wdataram_din_par[1]

Table 2-24 Write Data RAM Interface Signals (continued)

Port Name	I/O	Description
		(and so on.) For On Chip Parity configurations (UMCTL2_OCPAR_EN==1) with DDRCTL_OCSAP_EN=1 wdataram_mask[0] is for wdataram_din_par[1:0] wdataram_mask[1] is for wdataram_din_par[3:2] (and so on.) For On Chip ECC configurations (UMCTL2_OCECC_EN==1) wdataram_mask[0] is for wdataram_din_par[4:0] wdataram_mask[1] is for wdataram_din_par[9:5] (and so on.) ■ 1: The byte should be written to the write data RAM ■ 0: The byte should not be written to the write data RAM Valid with wdataram_wr = 1. In HIF configurations with ECC enabled, the width of this bus increases to include the mask for the ECC byte. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_wr	O	Write signal to write data RAM. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_waddr[(UMCTL2_WDATARAM_AW-1):0]	O	Write address for the write operation. Valid with wdataram_wr = 1. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-24 Write Data RAM Interface Signals (continued)

Port Name	I/O	Description
wdataram_re	O	Read signal to the write data RAM. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_raddr[(UMCTL2_WDATARAM_AW-1):0]	O	Read address to the write data RAM. Valid with wdataram_re = 1. **Exists:** UMCTL2_WDATA_EXTRAM **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_din_par[(UMCTL2_WDATARAM_PAR_DW_EXT-1):0]	O	Parity/ECC of the data for the write operation. **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_dout_par[(UMCTL2_WDATARAM_PAR_DW_EXT-1):0]	I	Parity/ECC of the read data coming from the write data RAM. **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-24 Write Data RAM Interface Signals (continued)

Port Name	I/O	Description
wdataram_din_dch1[(UMCTL2_WDATARAM_DW-1):0]	O	Data for the write operation (data channel 1). Valid with wdataram_wr_dch1. In HIF configurations with ECC enabled, the width of this bus increases to include the ECC byte. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_dout_dch1[(UMCTL2_WDATARAM_DW-1):0]	I	Read data coming from the write data RAM (data channel 1). Valid data comes out one clock after wdataram_re_dch1 = 1. In HIF configurations with ECC enabled, the width of this bus increases to include the ECC byte. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_mask_dch1[((UMCTL2_WDATARAM_DW/8)-1):0]	O	Mask for the write operation. One bit of wdataram_mask_dch1 signal is for each byte of data and corresponding parity if any. wdataram_mask_dch1[0] is for wdataram_din_dch1[7:0] wdataram_mask_dch1[1] is for wdataram_din_dch1[15:8] (and so on.) For On Chip Parity configurations (UMCTL2_OCPAR_EN==1) wdataram_mask_dch1[0] is for wdataram_din_par_dch1[0] wdataram_mask_dch1[1] is for wdataram_din_par_dch1[1] (and so on.) ■ 1: The byte should be written to the write data RAM ■ 0: The byte should not be written to the write data RAM Valid with wdataram_wr_dch1 = 1. In HIF configurations with ECC enabled, the width of this bus increases to include the mask for the ECC byte. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-24 Write Data RAM Interface Signals (continued)

Port Name	I/O	Description
wdataram_wr_dch1	O	Write signal to write data RAM (data channel 1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_waddr_dch1[(UMCTL2_WDATARAM_AW-1):0]	O	Write address for the write operation (data channel 1). Valid with wdataram_wr_dch1 = 1. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_re_dch1	O	Read signal to the write data RAM (data channel 1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_raddr_dch1[(UMCTL2_WDATARAM_AW-1):0]	O	Read address to the write data RAM (data channel 1). Valid with wdataram_re_dch1 = 1. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_WDATA_EXTRAM) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-24 Write Data RAM Interface Signals (continued)

Port Name	I/O	Description
wdataram_din_par_dch1[(UMCTL2_WDATARAM_PAR_DW_EXT-1):0]	O	Parity of the data for the write operation (data channel 1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_OCPAR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wdataram_dout_par_dch1[(UMCTL2_WDATARAM_PAR_DW_EXT-1):0]	I	Parity of the read data coming from the write data RAM (data channel 1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_OCPAR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.25 Mode Register Read/Write Signals

- hif_mrr_data
- hif_mrr_data_valid
- hif_mrr_data_dch1
- hif_mrr_data_valid_dch1

Table 2-25 Mode Register Read/Write Signals

Port Name	I/O	Description
hif_mrr_data[(MEMC_MRR_DATA_TOTAL_DATA_WIDTH-1):0]	O	LPDDR4/5: Mode register read data. This signal is valid when hif_mrr_data_valid is high and present only in designs configured to support LPDDR4/5. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_mrr_data_valid	O	When asserted high, this signal indicates that data on hif_mrr_data is valid. This signal is present only in designs configured to support LPDDR4/5. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_mrr_data_dch1[(MEMC_DFI_TOTAL_DATA_WIDTH-1):0]	O	LPDDR4/5: Mode register read data. This signal is valid when hif_mrr_data_valid_dch1 is high and present only in designs configured to support LPDDR4/5 for Channel 1. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-25 Mode Register Read/Write Signals (continued)

Port Name	I/O	Description
hif_mrr_data_valid_dch1	O	When asserted high, this signal indicates that data on hif_mrr_data_dch1 is valid for Channel 1. This signal is present only in designs configured to support LPDDR4/5. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.26 DDRC Hardware Low Power Signals

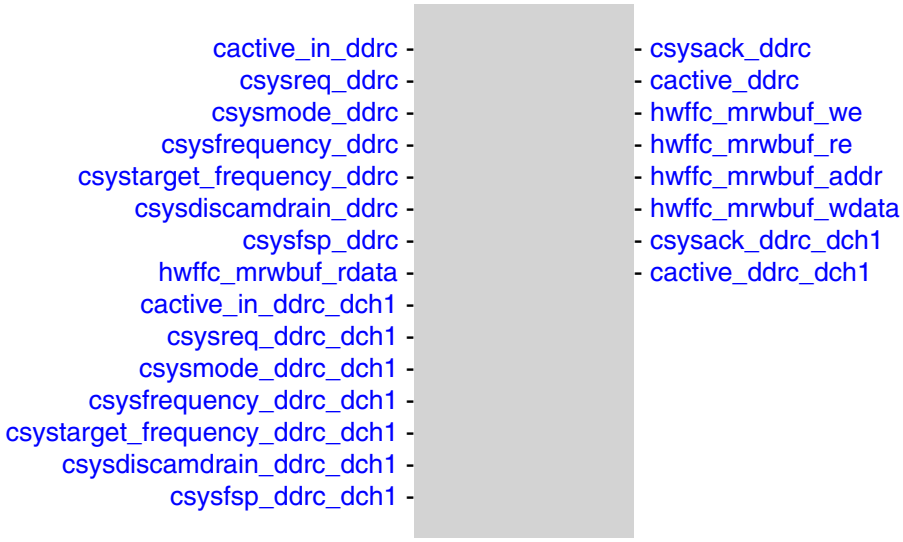


Table 2-26 DDRC Hardware Low Power Signals

Port Name	I/O	Description
cactive_in_ddrc[(NPORTS-1):0]	I	DDRC Hardware Low-Power Clock Active In. External asynchronous signal from the system that flags if a hardware low power request can be accepted or should always be denied. ■ 0 - Accepted ■ 1 - Denied Can also be used to exit the auto clock stop, power down, self refresh states modes. Driving c_active_in to 1 exits these modes. Note PWRCTL.hw_lp_exit_idle_en needs to be programmed to 1 to enable this functionality. For a system that does not generate this signal, it is recommended that this signal should be tied low to avoid issues due to undriven input. As this signal is an asynchronous input, it is required that it be glitch free. **Exists:** !UMCTL2_INCL_ARB_OR_CHB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
csysreq_ddrc	I	DDRC Hardware Low-Power Request. Request from the system clock controller for the peripheral (DDRC) to enter a low-power state. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysmode_ddrc	I	DDRC Hardware Fast Frequency Change mode. ■ 0 - Hardware Low-Power is requested ■ 1 - Hardware Fast Frequency Change is requested This signal should remain stable during csysreq_ddrc=0. **Exists:** UMCTL2_HWFFC_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysfrequency_ddrc[4:0]	I	In case hardware parameter DDRCTL_HWFFC_EXT is defined, this signal is used to specify target PHY power state selection number for DDRC hardware fast frequency change. In case that parameter is not defined, this signal is shared to specify target PHY power state selection number and target frequency register set number, for DDRC hardware fast frequency change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1). **Exists:** UMCTL2_HWFFC_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
csystarget_frequency_ddrc[(TARGET_FREQUENCY_WIDTH-1):0]	I	Target frequency register set number for DDRC Hardware Fast Frequency Change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1). **Exists:** (UMCTL2_HWFFC_EN) && (DDRCTL_HWFFC_EXT) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysdiscamdrain_ddrc	I	Disable CAM draining for DDRC Hardware Fast Frequency Change. When asserted, Self-Refresh can be entered without draining CAM. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1). **Exists:** UMCTL2_HWFFC_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysfsp_ddrc	I	Target frequency set point for DDRC Hardware Fast Frequency Change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1). **Exists:** (UMCTL2_HWFFC_EN) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysack_ddrc	O	DDRC Hardware Low-Power Request Acknowledge. Acknowledgement from the peripheral (DDRC) of a system low-power request. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
cactive_ddrc	O	DDRC Hardware Low-Power Clock Active. Indicates that the peripheral (DDRC) requires its clock signal. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hwffc_mrwbuf_we	O	Write signal to HWFFC MRW Buffer **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hwffc_mrwbuf_re	O	Read signal to HWFFC MRW Buffer **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hwffc_mrwbuf_addr[((HWFFC_MRWBUF_ADDR_WIDTH+HWFFC_MRWBUF_SELECT_WIDTH)-1):0]	O	Read/Write address for the read/write operation. Valid with hwffc_mrwbuf_re = 1 or hwffc_mrwbuf_we = 1 **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hwffc_mrwbuf_wdata[(HWFFC_MRWBUF_WDATA_WIDTH-1):0]	O	Data for the write operation. Valid with hwffc_mrwbuf_we = 1 **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
hwffc_mrwbuf_rdata[(HWFFC_MRWBUF_WDATA_WIDTH-1):0]	I	Data for the read operation. Valid data comes out two clock after hwffc_mrwbuf_re = 1 **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
cactive_in_ddrc_dch1[(NPORTS-1):0]	I	DDRC Hardware Low-Power Clock Active In (channel 1). External asynchronous signal from the system that flags if a hardware low power request can be accepted or should always be denied. ■ 0 - Accepted ■ 1 - Denied Can also be used to exit the auto clock stop, power down, self refresh states modes. Driving c_active_in to 1 exits these modes. Note PWRCTL.hw_lp_exit_idle_en needs to be programmed to 1 to enable this functionality. For a system that does not generate this signal, it is recommended that this signal should be tied low to avoid issues due to undriven input. As this signal is an asynchronous input, it is required that it be glitch free. **Exists:** (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_INCL_ARB_OR_CHB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysreq_ddrc_dch1	I	DDRC Hardware Low-Power Request. Request from the system clock controller for the peripheral (DDRC_dch1) to enter a low-power state. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
csysmode_ddrc_dch1	I	DDRC Hardware Fast Frequency Change mode (channel 1). ■ 0 - Hardware Low-Power is requested ■ 1 - Hardware Fast Frequency Change is requested This signal should remain stable during csysreq_ddrc_dch1=0. **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_HWFFC_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysfrequency_ddrc_dch1[4:0]	I	In case hardware parameter DDRCTL_HWFFC_EXT is defined, this signal is used to specify target PHY power state selection number for DDRC hardware fast frequency change. In case that parameter is not defined, this signal is shared to specify target PHY power state selection number and target frequency register set number, for DDRC hardware fast frequency change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc_dch1=0 and csysmode_ddrc_dch1=1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_HWFFC_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csystarget_frequency_ddrc_dch1[(TARGET_FREQUENCY_WIDTH-1):0]	I	Target frequency register set number for DDRC Hardware Fast Frequency Change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc_dch1=0 and csysmode_ddrc_dch1=1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_HWFFC_EN) && (DDRCTL_HWFFC_EXT) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-26 DDRC Hardware Low Power Signals (continued)

Port Name	I/O	Description
csysdiscamdrain_ddrc_dch1	I	Disable CAM draining for DDRC Hardware Fast Frequency Change. When asserted, Self-Refresh can be entered without draining CAM. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc_dch1=0 and csysmode_ddrc_dch1=1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_HWFFC_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysfsp_ddrc_dch1	I	Target frequency set point for DDRC Hardware Fast Frequency Change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc_dch1=0 and csysmode_ddrc_dch1=1). **Exists:** (UMCTL2_DUAL_CHANNEL) && (UMCTL2_HWFFC_EN) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
csysack_ddrc_dch1	O	DDRC Hardware Low-Power Request Acknowledge. Acknowledgement from the peripheral (DDRC_dch1) of a system low-power request. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
cactive_ddrc_dch1	O	DDRC Hardware Low-Power Clock Active. Indicates that the peripheral (DDRC_dch1) requires its clock signal. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.27 DDRC Self Refresh Signals

- stat_ddrc_reg_selfref_type
- stat_ddrc_dch1_reg_selfref_type

Table 2-27 DDRC Self Refresh Signals

Port Name	I/O	Description
stat_ddrc_reg_selfref_type[(SELFREF_TYPE_WIDTH-1):0]	O	DDRC 0 Self Refresh status and type. Equivalent to STAT.selfref_type register. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
stat_ddrc_dch1_reg_selfref_type[(SELFREF_TYPE_WIDTH-1):0]	O	DDRC 1 Self Refresh status and type. Equivalent to STAT.selfref_type register. **Exists:** UMCTL2_DUAL_CHANNEL **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.28 Inline ECC Debug Signals

- dbg_dfi_ie_cmd_type
- dbg_dfi_ie_cmd_type_dch1

Table 2-28 Inline ECC Debug Signals

Port Name	I/O	Description
dbg_dfi_ie_cmd_type[2:0]	O	DDRC 0 Inline ECC Debug signal. This signal is valid when dfi command/address is RD/RDA/WR/WRA, otherwise don't care. With RD/RDA commands ■ 000: RD_N (RD Data for non-ECC region) ■ 001: RD_E (RD Data for ECC region) ■ 010: RE_B (RD ECC in block read/write) ■ 111: MPR read (DDR4 only) With WR/WRA commands ■ 000: WD_N (WR Data for non-ECC region) ■ 001: WD_E (WR Data for ECC region) ■ 010: WE_BW (WR ECC in block write) ■ 111: MPR write (DDR4 only) DEBUG ONLY **Exists:** MEMC_INLINE_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-28 Inline ECC Debug Signals (continued)

Port Name	I/O	Description
dbg_dfi_ie_cmd_type_dch1[2:0]	O	DDRC 1 Inline ECC Debug signal. This signal is valid when dfi command/address is RD/RDA/WR/WRA, otherwise don't care. With RD/RDA commands ■ 000: RD_N (RD Data for non-ECC region) ■ 001: RD_E (RD Data for ECC region) ■ 010: RE_B (RD ECC in block read/write) ■ 111: MPR read (DDR4 only) With WR/WRA commands ■ 000: WD_N (WR Data for non-ECC region) ■ 001: WD_E (WR Data for ECC region) ■ 010: WE_BW (WR ECC in block write) ■ 111: MPR write (DDR4 only) DEBUG ONLY **Exists:** (MEMC_INLINE_ECC) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.29 Performance Logging Signals

- perf_hif_rd_or_wr
- perf_hif_wr
- perf_hif_rd
- perf_hif_rmw
- perf_hif_hi_pri_rd
- perf_read_bypass
- perf_act_bypass
- perf_dfi_wr_data_cycles
- perf_dfi_rd_data_cycles
- perf_hpr_xact_when_critical
- perf_lpr_xact_when_critical
- perf_wr_xact_when_critical
- perf_op_is_activate
- perf_op_is_rd_or_wr
- perf_op_is_rd_activate
- perf_op_is_rd
- perf_op_is_wr
- perf_op_is_mwr
- perf_op_is_wr16
- perf_op_is_wr32
- perf_op_is_rd16
- perf_op_is_rd32
- perf_op_is_cas
- perf_op_is_cas_ws
- perf_op_is_cas_ws_off
- perf_op_is_cas_wck_sus
- perf_op_is_enter_dsm
- perf_op_is_rfm
- perf_op_is_precharge
- perf_precharge_for_rdwr
- perf_precharge_for_other
- perf_rdwr_transitions
- perf_write_combine
- perf_write_combine_noecc
- perf_write_combine_wrecc
- perf_war_hazard
- perf_raw_hazard
- perf_waw_hazard
- perf_ie_blk_hazard
- perf_op_is_enter_selfref
- perf_op_is_enter_powerdown
- perf_selfref_mode
- perf_op_is_refresh
- perf_op_is_crit_ref
- perf_op_is_spec_ref
- perf_op_is_load_mode
- perf_rank
- perf_bank
- perf_bg
- perf_cid
- perf_hpr_req_with_nocredit

- perf_lpr_req_with_nocredit
- perf_visible_window_limit_reached_rd
- perf_visible_window_limit_reached_wr
- perf_op_is_dqsosc_mpc
- perf_op_is_dqsosc_mrr
- perf_op_is_tcr_mrr
- perf_op_is_zqstart
- perf_op_is_zqlatch
- perf_hif_rd_or_wr_dch1
- perf_hif_wr_dch1
- perf_hif_rd_dch1
- perf_hif_rmw_dch1
- perf_hif_hi_pri_rd_dch1
- perf_read_bypass_dch1
- perf_act_bypass_dch1
- perf_dfi_wr_data_cycles_dch1
- perf_dfi_rd_data_cycles_dch1
- perf_hpr_xact_when_critical_dch1
- perf_lpr_xact_when_critical_dch1
- perf_wr_xact_when_critical_dch1
- perf_op_is_activate_dch1
- perf_op_is_rd_or_wr_dch1
- perf_op_is_rd_activate_dch1
- perf_op_is_rd_dch1
- perf_op_is_wr_dch1
- perf_op_is_mwr_dch1
- perf_op_is_wr16_dch1
- perf_op_is_wr32_dch1
- perf_op_is_rd16_dch1
- perf_op_is_rd32_dch1
- perf_op_is_cas_dch1
- perf_op_is_cas_ws_dch1
- perf_op_is_cas_ws_off_dch1
- perf_op_is_cas_wck_sus_dch1
- perf_op_is_enter_dsm_dch1
- perf_op_is_rfm_dch1
- perf_op_is_precharge_dch1
- perf_precharge_for_rdwr_dch1
- perf_precharge_for_other_dch1
- perf_rdwr_transitions_dch1
- perf_write_combine_dch1
- perf_write_combine_noecc_dch1
- perf_write_combine_wrecc_dch1
- perf_war_hazard_dch1
- perf_raw_hazard_dch1
- perf_waw_hazard_dch1
- perf_ie_blk_hazard_dch1
- perf_op_is_enter_selfref_dch1
- perf_op_is_enter_powerdown_dch1
- perf_selfref_mode_dch1
- perf_op_is_refresh_dch1
- perf_op_is_crit_ref_dch1
- perf_op_is_spec_ref_dch1
- perf_op_is_load_mode_dch1

- perf_rank_dch1
- perf_bank_dch1
- perf_bg_dch1
- perf_cid_dch1
- perf_hpr_req_with_nocredit_dch1
- perf_lpr_req_with_nocredit_dch1
- perf_visible_window_limit_reached_rd_dch1
- perf_visible_window_limit_reached_wr_dch1
- perf_op_is_dqsosc_mpc_dch1
- perf_op_is_dqsosc_mrr_dch1
- perf_op_is_tcr_mrr_dch1
- perf_op_is_zqstart_dch1
- perf_op_is_zqlatch_dch1

Table 2-29 Performance Logging Signals

Port Name	I/O	Description
perf_hif_rd_or_wr	O	Asserts for every Read or Write command send to DDRC. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_wr	O	Asserts for every Write command send to DDRC. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_rd	O	Asserts for every Read command send to DDRC. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_hif_rmw	O	Asserts for every RMW command send to DDRC. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_hi_pri_rd	O	Asserts for every High-Priority Read command send to DDRC. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_read_bypass	O	Asserts for every Read command that is send through the Bypass path. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_RD_BYPASS) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_act_bypass	O	Asserts for every Activate command that is send through the Bypass path. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_ACT_BYPASS) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_dfi_wr_data_cycles	O	Asserts for every write data beat transfer on the DFI interface going to DRAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_dfi_rd_data_cycles	O	Asserts for every read data beat transfer on the DFI interface coming from DRAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hpr_xact_when_critical	O	Asserts for every High Priority Read transaction that is scheduled when the High Priority Queue is in Critical state. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_lpr_xact_when_critical	O	Asserts for every Low Priority Read transaction that is scheduled when the Low Priority Queue is in Critical state. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_wr_xact_when_critical	O	Asserts for every Write transaction that is scheduled when the Write Queue is in Critical state. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_activate	O	Asserts for every Activate that is issued for commands going through CAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd_or_wr	O	Asserts for every Read or Write that is issued for commands going through CAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd_activate	O	Asserts for every Read Activate that is issued for commands going through CAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd	O	Asserts for every Read that is issued for commands going through CAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_wr	O	Asserts for every Write that is issued for commands going through CAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_mwr	O	Asserts for every Masked Write that is issued for commands going through CAM. Not Applicable for DDR4 DRAM. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_wr16	O	Asserts for every WR16 command that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_wr32	O	Asserts for every WR32 command that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd16	O	Asserts for every RD16 command that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_rd32	O	Asserts for every RD32 command that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas	O	Asserts for every CAS command that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas_ws	O	Asserts for every CAS-WS_RD/CAS-WS_WR/CAS-WS_FS that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas_ws_off	O	Asserts for every CAS-WS_OFF that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (DDRCTL_LPDDR) && (DDRCTL_ENHANCED_WCK) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_cas_wck_sus	O	Asserts for every CAS-WCK_SUSPEND that is issued by the controller. **Exists:** (MEMC_PERF_LOG_ON) && (DDRCTL_LPDDR) && (DDRCTL_ENHANCED_WCK) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_enter_dsm	O	Asserts for every entry into Deep Sleep Mode. **Exists:** (MEMC_PERF_LOG_ON) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rfm	O	Asserts for every RFM that is issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_precharge	O	Asserts for every Precharge that is issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_precharge_for_rdwr	O	Asserts for every Precharge that is issued for Read or Write commands. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_precharge_for_other	O	Asserts for every Precharge that is issued due to requests other than Read or Write (for example: Refresh, ZQ Calib, MRW, MRR, tRAS(max)). **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_rdwr_transitions	O	Asserts for every Read to Write and Write to Read bus-turn-around that happens in the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_write_combine	O	Asserts for every Write Combine operation that happens in the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_write_combine_noecc	O	Asserts for every Write Combine (for Normal Write) operation that happens in the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_write_combine_wrecc	O	Asserts for every Write Combine (for WRECC Overhead Combine) operation that happens in the controller. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_war_hazard	O	Asserts for every Write-after-Read collision that happens in the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_raw_hazard	O	Asserts for every Read-after-Write collision that happens in the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_waw_hazard	O	Asserts for every Write-after-Write collision that happens in the controller. Valid only when Write Combine is turned off. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_ie_blk_hazard	O	Asserts for every BLock Address collision (Inline ECC) that happens in the controller. When this is asserted, perf_raw/war/waw_hazard are don't care. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_enter_selfref[(MEMC_NUM_RANKS-1):0]	O	Asserts for every entry into Self-Refresh mode. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_enter_powerdown[(MEMC_NUM_RANKS-1):0]	O	Asserts for every entry into Power Down mode. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_selfref_mode[(MEMC_NUM_RANKS-1):0]	O	Asserts for the entire duration for which the controller stays in Self-Refresh mode. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_refresh	O	Asserts for every Refresh command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0). **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_crit_ref	O	Asserts for every critical Refresh command that is issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_spec_ref	O	Asserts for every speculative Refresh command that is issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_load_mode	O	Asserts for every Load Mode operation (MRW or MRR) that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0). **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_rank[(MEMC_RANK_BITS-1):0]	O	Gives the rank number for every scheduled command in DDRC through CAM path. Validated by the signals: perf_op_is_rd_or_wr or perf_op_is_rd or perf_op_is_wr. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_NUM_RANKS_GT_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_bank[(MEMC_BANK_BITS-1):0]	O	Gives the bank number for every scheduled command in DDRC through CAM path. Validated by the signals: perf_op_is_rd_or_wr or perf_op_is_rd or perf_op_is_wr. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_bg[(MEMC_BG_BITS-1):0]	O	Gives the bank group number for every scheduled command in DDRC through CAM path. Validated by the signals: perf_op_is_rd_or_wr or perf_op_is_rd or perf_op_is_wr. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_cid[(CID_WIDTH-1):0]	O	Gives the chip ID number for every scheduled command in DDRC through CAM path. Validated by the signals: perf_op_is_rd_or_wr or perf_op_is_rd or perf_op_is_wr. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_CID_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_hpr_req_with_nocredit	O	Asserts when there is a High Priority Read (HPR) request (from XPI to PA) not served due to no available credit. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_lpr_req_with_nocredit	O	Asserts when there is a Low Priority Read (LPR) request (from XPI to PA) not served due to no available credit. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_visible_window_limit_reached_rd	O	Indicates that at least one RD CAM entry reaches visible window limit at this cycle. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_ENH_CAM_PTR) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_visible_window_limit_reached_wr	O	Indicates that at least one WR CAM entry reaches visible window limit at this cycle. **Exists:** (MEMC_PERF_LOG_ON) && (MEMC_ENH_CAM_PTR) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_dqsosc_mpc	O	Asserted for every DQSOSC MPC command issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_dqsosc_mrr	O	Asserted for every DQSOSC MRR command issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_tcr_mrr	O	Asserted for every TCR MRR command issued by the controller. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_zqstart	O	Asserts for every ZQcal start command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0). This signal is applicable for DDR5/LPDDR4. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_zqlatch	O	Asserts for every ZQcal latch Short command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0). This signal is applicable for DDR5/LPDDR4/LPDDR5. **Exists:** MEMC_PERF_LOG_ON **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_rd_or_wr_dch1	O	Asserts for every Read or Write command send to DDRC (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_wr_dch1	O	Asserts for every Write command send to DDRC (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_rd_dch1	O	Asserts for every Read command send to DDRC (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hif_rmw_dch1	O	Asserts for every RMW command send to DDRC (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_hif_hi_pri_rd_dch1	O	Asserts for every High-Priority Read command send to DDRC (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_read_bypass_dch1	O	Asserts for every Read command that is send through the Bypass path (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_RD_BYPASS) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_act_bypass_dch1	O	Asserts for every Activate command that is send through the Bypass path (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ACT_BYPASS) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_dfi_wr_data_cycles_dch1	O	Asserts for every write data beat transfer on the DFI interface going to DRAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_dfi_rd_data_cycles_dch1	O	Asserts for every read data beat transfer on the DFI interface coming from DRAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hpr_xact_when_critical_dch1	O	Asserts for every High Priority Read transaction that is scheduled when the High Priority Queue is in Critical state (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_lpr_xact_when_critical_dch1	O	Asserts for every Low Priority Read transaction that is scheduled when the Low Priority Queue is in Critical state (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_wr_xact_when_critical_dch1	O	Asserts for every Write transaction that is scheduled when the Write Queue is in Critical state (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_activate_dch1	O	Asserts for every Activate that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd_or_wr_dch1	O	Asserts for every Read or Write that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd_activate_dch1	O	Asserts for every Read Activate that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd_dch1	O	Asserts for every Read that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_wr_dch1	O	Asserts for every Write that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_mwr_dch1	O	Asserts for every Masked Write that is issued for commands going through CAM (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_wr16_dch1	O	Asserts for every WR16 command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_wr32_dch1	O	Asserts for every WR32 command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_rd16_dch1	O	Asserts for every RD16 command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rd32_dch1	O	Asserts for every RD32 command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_BURST_LENGTH_32) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas_dch1	O	Asserts for every CAS command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas_ws_dch1	O	Asserts for every CAS-WS_RD/CAS-WS_WR/CAS-WS_FS that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_cas_ws_off_dch1	O	Asserts for every CAS-WS_OFF that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_LPDDR) && (DDRCTL_ENHANCED_WCK) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_cas_wck_sus_dch1	O	Asserts for every CAS-WCK_SUSPEND that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_LPDDR) && (DDRCTL_ENHANCED_WCK) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_enter_dsm_dch1	O	Asserts for every entry into Deep Sleep Mode (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_rfm_dch1	O	Asserts for every RFM that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_precharge_dch1	O	Asserts for every Precharge that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_precharge_for_rdwr_dch1	O	Asserts for every Precharge that is issued for Read or Write commands (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_precharge_for_other_dch1	O	Asserts for every Precharge that is issued due to requests other than Read or Write (for example, Refresh, ZQ Calib, MRW, MRR, tRAS(max)) (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_rdwr_transitions_dch1	O	Asserts for every Read to Write and Write to Read bus-turn-around that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_write_combine_dch1	O	Asserts for every Write Combine operation that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_write_combine_noecc_dch1	O	Asserts for every Write Combine (for Normal Write) operation that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_write_combine_wrecc_dch1	O	Asserts for every Write Combine (for WRECC Overhead Combine) operation that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_war_hazard_dch1	O	Asserts for every Write-after-Read collision that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_raw_hazard_dch1	O	Asserts for every Read-after-Write collision that happens in the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_waw_hazard_dch1	O	Asserts for every Write-after-Write collision that happens in the controller (Channel 1). Is valid only when Write Combine is turned off. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_ie_blk_hazard_dch1	O	Asserts for every BLock Address collision (Inline ECC) that happens in the controller (Channel 1). When this is asserted, perf_raw/war/waw_hazard are don't care. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_enter_selfref_dch1[(MEMC_NUM_RANKS-1):0]	O	Asserts for every entry into Self-Refresh mode (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_enter_powerdown_dch1[(MEMC_NUM_RANKS-1):0]	O	Asserts for every entry into PowerDown mode (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_selfref_mode_dch1[(MEMC_NUM_RANKS-1):0]	O	Asserts for the entire duration for which the controller stays in Self-Refresh mode (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_refresh_dch1	O	Asserts for every Refresh command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0) (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_crit_ref_dch1	O	Asserts for every critical Refresh command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_spec_ref_dch1	O	Asserts for every speculative Refresh command that is issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_load_mode_dch1	O	Asserts for every Load Mode operation (MRW or MRR) that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0) (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_rank_dch1[(MEMC_RANK_BITS-1) :0]	O	Gives the rank number for every scheduled command in DDRC through CAM path (Channel 1). Validated by the signals: perf_op_is_rd_or_wr_dch1 or perf_op_is_rd_dch1 or perf_op_is_wr_dch1. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_NUM_RANKS_GT_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_bank_dch1[(MEMC_BANK_BITS-1) :0]	O	Gives the bank number for every scheduled command in DDRC through CAM path (Channel 1). Validated by the signals: perf_op_is_rd_or_wr_dch1 or perf_op_is_rd_dch1 or perf_op_is_wr_dch1. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_bg_dch1[(MEMC_BG_BITS-1):0]	O	Gives the bank group number for every scheduled command in DDRC through CAM path (Channel 1). Validated by the signals: perf_op_is_rd_or_wr_dch1 or perf_op_is_rd_dch1 or perf_op_is_wr_dch1. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_cid_dch1[(CID_WIDTH-1):0]	O	Gives the chip ID number for every scheduled command in DDRC through CAM path (Channel 1). Validated by the signals: perf_op_is_rd_or_wr_dch1 or perf_op_is_rd_dch1 or perf_op_is_wr_dch1. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_CID_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_hpr_req_with_nocredit_dch1	O	Asserts when there is a High Priority Read (HPR) request (from XPI to PA) not served due to no available credit (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_lpr_req_with_nocredit_dch1	O	Asserts when there is a Low Priority Read (LPR) request (from XPI to PA) not served due to no available credit (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_INCL_ARB) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_visible_window_limit_reached_rd_dch1	O	Indicates that at least one RD CAM entry reaches visible window limit at this cycle (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ENH_CAM_PTR) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_visible_window_limit_reached_wr_dch1	O	Indicates that at least one WR CAM entry reaches visible window limit at this cycle (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) && (MEMC_ENH_CAM_PTR) && (UMCTL2_VPRW_EN) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_dqsosc_mpc_dch1	O	Asserted for every DQSOSC MPC command issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_dqsosc_mrr_dch1	O	Asserted for every DQSOSC MRR command issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-29 Performance Logging Signals (continued)

Port Name	I/O	Description
perf_op_is_tcr_mrr_dch1	O	Asserted for every TCR MRR command issued by the controller (Channel 1). **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_zqstart_dch1	O	Asserts for every ZQcal start command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0) (Channel 1). This signal is applicable for DDR5/LPDDR4. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
perf_op_is_zqlatch_dch1	O	Asserts for every ZQcal latch Short command that is issued by the controller after initialization is complete (that is, when STAT.operating_mode != 0) (Channel 1). This signal is applicable for DDR5/LPDDR4/LPDDR5. **Exists:** (MEMC_PERF_LOG_ON) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.30 Credit Counters Signals

- lpr_credit_cnt
- hpr_credit_cnt
- wr_credit_cnt
- wrecc_credit_cnt
- lpr_credit_cnt_dch1
- hpr_credit_cnt_dch1
- wr_credit_cnt_dch1
- wrecc_credit_cnt_dch1

Table 2-30 Credit Counters Signals

Port Name	I/O	Description
lpr_credit_cnt[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available Low priority read CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the read CAM (LPR store). **Exists:** UMCTL2_INCL_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hpr_credit_cnt[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available High priority read CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the read CAM (HPR store). **Exists:** UMCTL2_INCL_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-30 Credit Counters Signals (continued)

Port Name	I/O	Description
wr_credit_cnt[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available write CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the write CAM. **Exists:** UMCTL2_INCL_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wrecc_credit_cnt[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available write ECC CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the write ECC CAM. **Exists:** (UMCTL2_INCL_ARB) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
lpr_credit_cnt_dch1[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available Low priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (LPR store). **Exists:** (UMCTL2_INCL_ARB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-30 Credit Counters Signals (continued)

Port Name	I/O	Description
hpr_credit_cnt_dch1[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available High priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (HPR store). **Exists:** (UMCTL2_INCL_ARB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wr_credit_cnt_dch1[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available write CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the write CAM. **Exists:** (UMCTL2_INCL_ARB) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
wrecc_credit_cnt_dch1[(DDRCTL_CHB_HIF_CRDT_CNT_WIDTH-1):0]	O	Indicates the number of available write ECC CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the write ECC CAM. **Exists:** (UMCTL2_INCL_ARB) && (UMCTL2_DUAL_CHANNEL) && (MEMC_INLINE_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.31 Port Arbiter Signals

pa_rmask -
pa_wmask -

Table 2-31 Port Arbiter Signals

Port Name	I/O	Description
pa_rmask[((2*NPORTS)-1):0]	I	When asserted (active high), this signal masks (prevents) the corresponding application port read address channel from requesting to the PA. An external agent can control the port arbitration by throttling certain XPI ports based on traffic class, queue status and other dynamic criteria. There are 2 bits for each port, first one for the blue queue, second for the red queue (Bit 0 drives blue queue of Port 0, Bit 1 drives red queue of Port 0, Bit 2 drives blue queue of Port 1 and so on.). If dual queue is not used for a specific port, red input is unused. If not used, tie-off all bits to 0. **Exists:** UMCTL2_INCL_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pa_wmask[(NPORTS-1):0]	I	When asserted (active high), this signal masks (prevents) the corresponding application port write address channel from requesting to the PA. An external agent can control the port arbitration by throttling certain XPI ports based on traffic class, queue status and other dynamic criteria. Each bit position corresponds to a port index (Bit 0 drives Port 0 and so on). If not used, tie-off all bits to 0. **Exists:** UMCTL2_INCL_ARB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.32 ECC Scrubber Signals

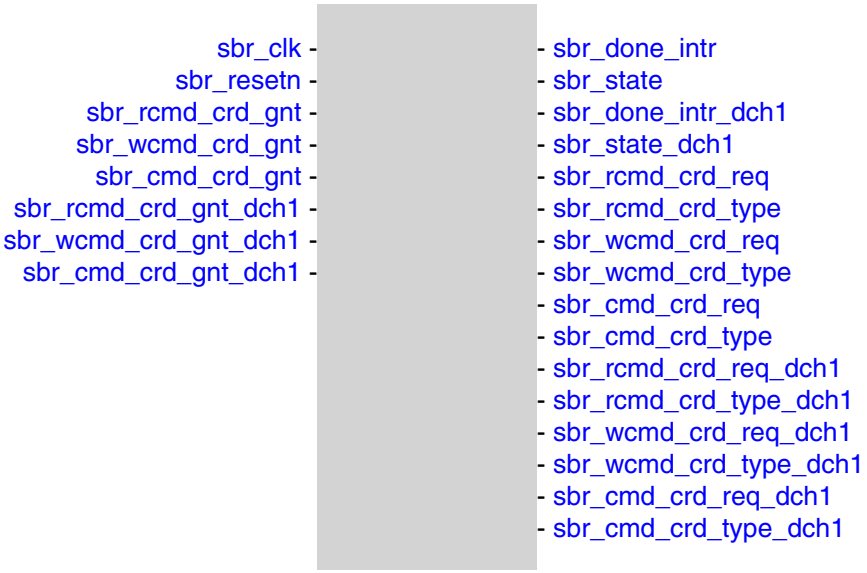


Table 2-32 ECC Scrubber Signals

Port Name	I/O	Description
sbr_clk	I	Scrubber Clock. Same clock (synchronous to) as core_ddrc_core_clk. The SBR can continue to function that is, count and request exit from low power - even if the core controller clock is gated. **Exists:** UMCTL2_SBR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_resetn	I	Scrubber Reset. Same as core_ddrc_rstn. Active-low pin that asynchronously resets the SBR logic to its default state. Synchronous to sbr_clk on de-assertion, asynchronous on assertion. **Exists:** UMCTL2_SBR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_done_intr	O	Scrubber interrupt indicating one full address range sweep; only asserted in certain conditions. Behaves identical to SBRSTAT.scrub_done register. **Exists:** UMCTL2_SBR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_state[2:0]	O	Scrubber FSM state indicating what state the Scrubber is in (Disabled, Normal Mode, Low Power). ■ 001 - Disabled ■ 010 - Normal Operatin Mode ■ 100 - HW Controlled Low Power Mode **Exists:** (UMCTL2_SBR_EN_1) && (DDRCTL_HIF_SBR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_done_intr_dch1	O	Scrubber interrupt indicating one full address range sweep. Only asserted in certain conditions. Behaves identical to SBRSTAT.scrub_done register (Channel 1). **Exists:** (UMCTL2_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_state_dch1[2:0]	O	Scrubber FSM state indicating what state the Scrubber (DCH1) is in (Disabled, Normal Mode, Low Power). ■ 001 - Disabled ■ 010 - Normal Operatin Mode ■ 100 - HW Controlled Low Power Mode **Exists:** (UMCTL2_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (DDRCTL_HIF_SBR_EN_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_rcmd_crd_req	O	This signal is the read credit request made by the Scrubber in dual HIF configurations. ■ 0 - Idle ■ 1 - Scrubber requests read credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_rcmd_crd_type[1:0]	O	This signal is the read credit type requested by the Scrubber in dual HIF configurations. ■ 00 - Reserved ■ 01 - LPR (Low Priority Read) ■ 10 - Reserved ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_rcmd_crd_gnt	I	This signal is the read credit grant provided to the Scrubber in dual HIF configurations. ■ 0 - Idle ■ 1 - Scrubber is granted read credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_wcmd_crd_req	O	This signal is the write credit request made by the Scrubber in dual HIF configurations. ■ 0 - Idle ■ 1 - Scrubber requests write credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_wcmd_crd_type[1:0]	O	This signal is the write credit type requested by the Scrubber in dual HIF configurations. ■ 00 - WR (Write) ■ 01 - Reserved ■ 10 - RMW (1WR + 1LPR), Read Modify Write ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_wcmd_crd_gnt	I	This signal is the write credit grant provided to the Scrubber in dual HIF configurations. ■ 0 - Idle ■ 1 - Scrubber is granted write credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_cmd_crd_req	O	This signal is the credit request made by the Scrubber in single HIF configurations. ■ 0 - Idle ■ 1 - Scrubber requests credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_cmd_crd_type[1:0]	O	This signal is the credit type requested by the Scrubber in single HIF configurations. ■ 00 - WR (Write) ■ 01 - LPR (Low Priority Read) ■ 10 - RMW (1WR + 1LPR), Read Modify Write ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_cmd_crd_gnt	I	This signal is the credit grant provided to the Scrubber in single HIF configurations. ■ 0 - Idle ■ 1 - Scrubber is granted credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_rcmd_crd_req_dch1	O	This signal is the read credit request made by the Scrubber in dual HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber requests read credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_rcmd_crd_type_dch1[1:0]	O	This signal is the read credit type requested by the Scrubber in dual HIF configurations, channel 1. ■ 00 - Reserved ■ 01 - LPR (Low Priority Read) ■ 10 - Reserved ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_rcmd_crd_gnt_dch1	I	This signal is the read credit grant provided to the Scrubber in dual HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber is granted read credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_wcmd_crd_req_dch1	O	This signal is the write credit request made by the Scrubber in dual HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber requests write credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_wcmd_crd_type_dch1[1:0]	O	This signal is the write credit type requested by the Scrubber in dual HIF configurations, channel 1. ■ 00 - WR (Write) ■ 01 - Reserved ■ 10 - RMW (1WR + 1LPR), Read Modify Write ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_wcmd_crd_gnt_dch1	I	This signal is the write credit grant provided to the Scrubber in dual HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber is granted write credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_cmd_crd_req_dch1	O	This signal is the credit request made by the Scrubber in single HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber requests credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
sbr_cmd_crd_type_dch1[1:0]	O	This signal is the credit type requested by the Scrubber in single HIF configurations, channel 1. ■ 00 - WR (Write) ■ 01 - LPR (Low Priority Read) ■ 10 - RMW (1WR + 1LPR), Read Modify Write ■ 11 - Reserved **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-32 ECC Scrubber Signals (continued)

Port Name	I/O	Description
sbr_cmd_crd_gnt_dch1	I	This signal is the credit grant provided to the Scrubber in single HIF configurations, channel 1. ■ 0 - Idle ■ 1 - Scrubber is granted credit **Exists:** (DDRCTL_HIF_SBR_EN_1) && (UMCTL2_DUAL_CHANNEL) && (!UMCTL2_DUAL_HIF_1) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.33 DFI Command Interface Signals

- dfin_address_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_cke_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_cs_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_dram_clk_disable_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfi_reset_n

Table 2-33 DFI Command Interface Signals

Port Name	I/O	Description
dfin_address_Pp[(MEMC_DFI_ADDR_WIDTH_P0-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the controller-to-PHY address on phase *p*for DFIn channel. This signal is 14 bits for *p*=0. 6 bits for *p*=1,2,3. The CA bus for DFIn channel is mapped to dfin_address. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_cke_Pp[(DDRCTL_INST_DFI0_CS_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the controller-to-PHY clock enable on phase *p*for the DFIn channel. It is active high. **Exists:** DDRCTL_LPDDR_OR_DDR4_PINS **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_cs_Pp[(DDRCTL_INST_DFI0_CS_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the controller-to-PHY chip select on phase *p*for DFIn channel. This signal is active high or low, depending on the SDRAM device in use. When LPDDR4/LPDDR5 SDRAM device is used, this signal is active high. When other SDRAM device is used, this signal is active low. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-33 DFI Command Interface Signals (continued)

Port Name	I/O	Description
dfin_dram_clk_disable_Pp[(MEMC_NUM_CLKS-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the SDRAM clock disable signal on phase *p*for the DFIn channel. When active, this indicates to the PHY that the clocks to the SDRAM devices must be disabled such that the clock signals hold a constant value. When the dfin_dram_clk_disable signal is inactive, the SDRAMs must be clocked normally. One bit per rank. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_reset_n[(UMCTL2_RESET_WIDTH-1):0]	O	This signal is the controller-to-PHY reset (active low) for memory. Initial value of this signal is 0. For DDR4, LPDDR4 and LPDDR5, this signal is controlled by DFIMISC.dfi_reset_n register. For DDR5, this signal is kept asserted (becomes 0) after core_ddrc_rstn is released, until it's de-asserted by Software Command Interface. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.34 DFI Write Data Interface Signals

- dfin_wrdata_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_wrdata_en_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_wrdata_mask_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_wrdata_cs_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dfin_wrdata_ecc_Pp (for n = 0; n <= 3)(for p = 0; p <= 3)

Table 2-34 DFI Write Data Interface Signals

Port Name	I/O	Description
dfin_wrdata_Pp[(DDRCTL_INST_DFI_DATA_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the write data on phase *p*for the DFIn channel. The write data stream is valid for the number of cycles that the dfin_wrdata_en_Pp signal is asserted. The latency between dfin_wrdata_en_Pp and dfin_wrdata_Pp is defined by DFITMG0.dfi_tphy_wrdata. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_wrdata_en_Pp[(DDRCTL_INST_DFI_DATAEN_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the write data and data mask valid signal on phase *p*for the DFIn channel. This signal indicates the number of cycles of data and data mask to be sent on the DFI interface. The latency between the write command and dfin_wrdata_en_Pp is defined by DFITMG0.dfi_tphy_wrlat. When the dfin_wrdata_en_Pp signal is asserted, it remains asserted for the number of contiguous cycles of write data passed through the DFI write data interface. There is a single dfi_wrdata_en bit for each slice of memory data. The dfin_wrdata_en_Pp[0] signal corresponds with the lowest segment of dfin_wrdata_Pp signals. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_wrdata_mask_Pp[(DDRCTL_INST_DFI_MASK_WIDTH-1):0]	O	This signal is used to transfer either the write data mask or the write data inversion (DBI) information on phase *p*for the DFIn channel, depending on the system and DRAM settings.

Table 2-34 DFI Write Data Interface Signals (continued)

Port Name	I/O	Description
(for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)		When the DM feature is enabled: ■ Write data byte mask signal. The timing is the same as for the dfin_wrdata_Pp bus. The dfin_wrdata_mask_Pp[0] signal defines masking for dfin_wrdata_Pp[7:0]; dfin_wrdata_mask[1] defines masking for dfin_wrdata_Pp[15:8]; and so on. ■ This signal is active high or low, depending on the SDRAM device in use. When the Write DBI feature is enabled: ■ Write DBI signal. The timing is the same as for the dfi0_wrdata_P0 bus. The dfi0_wdata_mask_P0[0] signal defines the DBI information for dfi0_wrdata_P0[7:0]; dfi0_wrdata_mask_P0[1] defines DBI information for dfi0_wrdata_P0[15:8]; and so on. ■ This signal is active high or low, depending on SDRAM device in use. When DDR4/DDR5 SDRAM device is used, this signal is active low. When LPDDR4/LPDDR5 SDRAM device is used, this signal is active high. When the DM and Write DBI features are enabled: ■ If the total count of '1' data bits on dfi0_wrdata_P0[2:7] is equal to or greater than five and dfi0_wdata_mask_P0[0] is low, write data is masked. If the count of '1' is less than five, dfi0_wdata_mask_P0[0] defines the DBI information for dfi0_wrdata_P0[7:0], and so on. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_wrdata_cs_Pp[((DDRCTL_INST_DFI_DATAEN_WIDTH*DDRCTL_INST_DFI0_CS_WIDTH)-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the DFI write data chip select on phase *p*for the DFIn channel. The dfin_wrdata_cs_Pp signal is asserted DFITMG2.dfi_tphy_wrcslat cycles after the assertion of a write command on the DFI control interface. The polarity of this signal is set by DFIMISC.dfi_data_cs_polarity. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-34 DFI Write Data Interface Signals (continued)

Port Name	I/O	Description
dfin_wrdata_ecc_Pp[((DDRCTL_INST_DFI_DATA_WIDTH/8)-1):0] (for n = 0; n <= 3)(for p = 0; p <= 3)	O	This signal is to used to transfer the write Link-ECC code, depending on the DRAM setting. This signal is valid for the number of cycles that the dfi _wrdata_en signal is asserted. The latency between dfi_wrdata_en and this signal is defined by DFITMG0.dfi_tphy_wrdata. **Exists:** MEMC_LINK_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.35 DFI Read Data Interface Signals

dfin_rddata_Wp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) - dfin_rddata_dbi_Wp (for n = 0; n <= 3)(for p = 0; p <= 3) - dfin_rddata_valid_Wp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) - dfin_rddata_cs_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) - dfin_rddata_en_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)

Table 2-35 DFI Read Data Interface Signals

Port Name	I/O	Description
dfin_rddata_Wp[(DDRCTL_INST_DFI_DATA_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	This signal is the read data on phase *p*from the DFIn channel. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_rddata_cs_Pp[((DDRCTL_INST_DFI_DATAEN_WIDTH*DDRCTL_INST_DFI0_CS_WIDTH)-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the DFI read data chip select on phase *p*for the DFIn channel. The dfin_rddata_cs_Pp signal is asserted DFITMG2.dfi_tphy_rdcslat cycles after the assertion of a read command on the DFI control interface. The polarity of this signal is set by DFIMISC.dfi_data_cs_polarity. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_rddata_dbi_Wp[((DDRCTL_INST_DFI_DATA_WIDTH/8)-1):0] (for n = 0; n <= 3)(for p = 0; p <= 3)	I	This signal is sent with DFI read data (dfin_rddata_Wp) on phase *p*from the DFIn channel, indicating data bus inversion functionality. It is valid with dfin_rddata_valid_Pp. There is 1 bit of this signal for every 8 bits of the read data bus. This signal is active high or low, depending on SDRAM device in use. When a LPDDR4/LPDDR5 SDRAM device is used, this signal is active high. **Exists:** (DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-35 DFI Read Data Interface Signals (continued)

Port Name	I/O	Description
dfin_rddata_en_Pp[(DDRCTL_INST_DFI_DATAEN_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the read data enable on phase *p*for the DFIn channel. The dfin_rddata_en_Pp signal is asserted DFITMG.dfi_t_rddata_en cycles after the assertion of a read command on the DFI control interface and remains valid for the duration of read data expected on the dfin_rddata_Pp bus. There is a single dfin_rddata_en_Pp bit for each slice of memory data. The dfin_rddata_en_Pp [0] signal corresponds with the lowest segment of dfin_rddata_Pp signals. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_rddata_valid_Wp[(DDRCTL_INST_DFI_DATAEN_WIDTH-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	This signal is the read data valid indicator on phase *p*from the DFIn channel. The dfin_rddata_valid_Wp signal is asserted with the read data for the number of cycles that data is being sent. The timing is the same as dfin_rddata_Wp bus. **Exists:** DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.36 DFI Update Interface Signals

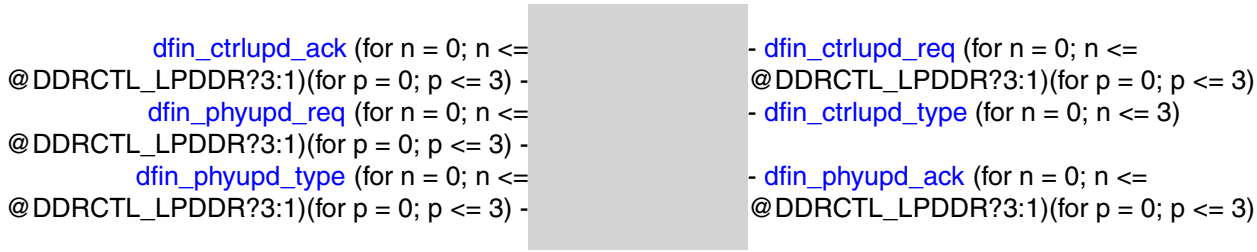


Table 2-36 DFI Update Interface Signals

Port Name	I/O	Description
dfin_ctrlupd_req (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is used to trigger a controller-initiated update for the DFIn channel. This indicates that the DFI is idle for some time, during which the PHY may perform an update. The dfin_ctrlupd_req signal is asserted for a minimum of DFIUPDTMG0.dfi_t_ctrlup_min cycles and a maximum of DFIUPDTMG0.dfi_t_ctrlup_max cycles. A dfin_ctrlupd_req signal assertion is an invitation for the PHY to update and does not require a response. The behavior of the dfin_ctrlupd_req signal is dependent on the dfin_ctrlupd_ack signal: ■ If the update is acknowledged by the PHY, the dfin_ctrlupd_req signal remains asserted as long as the dfin_ctrlupd_ack signal is asserted, but is de-asserted before DFIUPDTMG0.dfi_t_ctrlup_max expires. While this signal is asserted, the DFI bus remains idle other than any transactions specifically associated with the update process. ■ If the update is not acknowledged, the dfin_ctrlupd_req signal is de-asserted at any time after DFIUPDTMG0.dfi_t_ctrlup_min and before DFIUPDTMG0.dfi_t_ctrlup_max. The maximum number of clock cycles that the controller may wait between assertions of the dfin_ctrlupd_req is determined by DFIUPD1.dfi_ctrlupd_interval_max_x1024. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-36 DFI Update Interface Signals (continued)

Port Name	I/O	Description
dfin_ctrlupd_ack (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	This signal is asserted to acknowledge a controller-initiated update request from the DFI0 channel. The PHY is not required to acknowledge this request. While this signal is asserted, the DFI bus remains idle other than any transactions specifically associated with the update process. ■ If the PHY acknowledges the request, the dfin_ctrlupd_ack signal must be asserted before the dfin_ctrlupd_req signal de-asserts. ■ If PHY ignores the request, the dfin_ctrlupd_ack signal must remain de-asserted until the dfin_ctrlupd_req signal is de-asserted. The dfin_ctrlupd_req signal is guaranteed to be asserted for at least DFIUPDTMG0.dfi_t_ctrlup_min cycles. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_ctrlupd_type[1:0] (for n = 0; n <= 3)	O	This signal is the DFI controller-initiated update select from the DFIn channel. This signal indicates which one of the four types of DFI MC-Initiated Update is being requested by the dfin_ctrlupd_req signal. The valid values are as follows: ■ 00: ctrlupd_type0 ■ 01: ctrlupd_type1 ■ 10: ctrlupd_type2 (not used) ■ 11: ctrlupd_type3 (not used) This signal is not yet in DFI standard. Possibly renamed later. **Exists:** DDRCTL_PPT2 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-36 DFI Update Interface Signals (continued)

Port Name	I/O	Description
dfin_phyupd_req (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	This signal is the DFI PHY-initiated update request from the DFIn channel. If set, this signal indicates that the PHY requires the DFI to be idle; that is, for the DFI command, read data channel and write data channel are inactive for a specified period of time. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_phyupd_type[1:0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	This signal is the DFI PHY-initiated update select from the DFIn channel. This signal indicates which one of the four types of PHY update times is being requested by the dfin_phyupd_req signal. The valid values are as follows: ■ 00: Tphyupd_type0 ■ 01: Tphyupd_type1 (not used) ■ 10: Tphyupd_type2 (not used) ■ 11: Tphyupd_type3 (not used) **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_phyupd_ack (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is the DFI PHY-initiated update acknowledge for the DFIn channel: This signal indicates that the DFI is idle and will remain so until the dfin_phyupd_req signal de-asserts. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.37 DFI Status Interface Signals

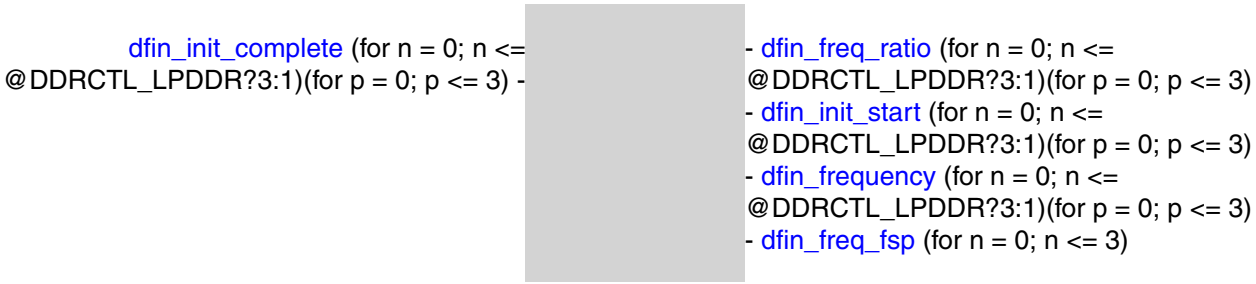


Table 2-37 DFI Status Interface Signals

Port Name	I/O	Description
dfin_freq_ratio[1:0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal indicates the frequency ratio for the DFIn channel. ■ 01: 1:2 Frequency Ratio ■ 10: 1:4 Frequency Ratio ■ 00/11: Reserved **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_init_complete (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	I	The signal is the PHY initialization complete for the DFIn channel. The dfin_init_complete signal indicates that the PHY is able to respond to any proper stimulus on the DFI. All DFI signals are held at their default values until the dfin_init_complete signal asserts. This signal will be ignored by the controller if DFIMISC.dfi_init_complete_en is set to 0. This signal is also used as part of the DFI frequency change protocol. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-37 DFI Status Interface Signals (continued)

Port Name	I/O	Description
dfin_init_start (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	The signal is the PHY initialization start and DFI frequency change request for DFIn channel from the DFIMISC.dfi_init_start APB register. When asserted, this signal triggers the PHY initialization start and DFI frequency change request and then the DFISTAT.dfi_init_complete flag is polled to know when the initialization and frequency change is done. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_frequency[4:0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal indicates the operating frequency of the system for the DFIn channel from the DFIMISC.dfi_frequency APB register. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_freq_fsp[1:0] (for n = 0; n <= 3)	O	This signal indicates the FSP-OP for the DFIn channel from the DFIMISC.dfi_freq_fsp APB register. **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.38 DFI PHY Master Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals

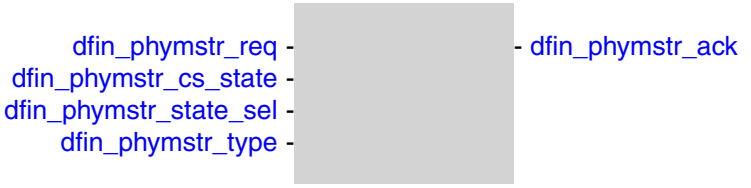


Table 2-38 DFI PHY Master Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals

Port Name	I/O	Description
dfin_phymstr_req	I	This signal is the DFI PHY master request for the DFIn channel. If set, this signal indicates that the PHY requests control on the DFI bus. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_phymstr_cs_state[(MEMC_NUM_RANKS-1):0]	I	This signal is the DFI PHY master CS state for the DFIn channel. This signal indicates the state of the DRAM when the PHY becomes the master: ■ 0: The PHY specifies the required state, using the dfin_phymstr_state_sel signal. ■ 1: The PHY does not specify the state. This signal is valid only when dfin_phymstr_req is asserted. Each memory rank uses one bit. Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfin_phymstr_req. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-38 DFI PHY Master Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals (continued)

Port Name	I/O	Description
dfin_phymstr_state_sel	I	This signal is the DFI PHY master state select for the DFIn channel. This signal indicates the state requested by the PHY: ■ 0: IDLE ■ 1: Self-Refresh Note: This input port is not used internally as the DDRCTL puts all ranks of SDRAM into Self Refresh in response to dfin_phymstr_req. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_phymstr_type[1:0]	I	This signal is the DFI PHY master type for the DFIn channel. This signal indicates which of the four types of PHY master interface times the dfin_phymstr_req signal is requesting: ■ 00: tphymstr_type0 ■ 01: tphymstr_type1 ■ 10: tphymstr_type2 ■ 11: tphymstr_type3 **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_phymstr_ack	O	This signal is the DFI PHY master acknowledge for the DFIn channel: When asserted, the PHY is the master of the DRAM bus. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.39 DFI Low Power Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals

Table 2-39 DFI Low Power Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals

Port Name	I/O	Description
dfin_lp_ctrl_req	O	This signal is the DFI low-power control request for the DFIn channel: This controller uses this signal to inform the PHY of an opportunity to switch to a low-power mode. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_lp_ctrl_ack	I	This signal is the DFI low-power control acknowledge for the DFIn channel: This PHY asserts this signal to acknowledge the controller low-power opportunity request. The PHY is not required to acknowledge the request. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-39 DFI Low Power Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals (continued)

Port Name	I/O	Description
dfin_lp_ctrl_wakeup[(DFI_LP_WAKEUP_PD_WIDTH-1):0]	O	This signal is the DFI low-power control wake-up for the DFIn channel: This signal indicates which one of the 16 wake-up times the controller is requesting the PHY. The valid values for the PHY and the PHY respective low-power action are as follows: ■ 00000: 1 cycle ■ 00001: 2 cycles ■ 00010: 4 cycles ■ 00011: 8 cycles ■ 00100: 16 cycles ■ 00101: 32 cycles ■ 00110: 64 cycles ■ 00111: 128 cycles ■ 01000: 256 cycles ■ 01001: 512 cycles ■ 01010: 1024 cycles ■ 01011: 2048 cycles ■ 01100: 4096 cycles ■ 01101: 8192 cycles ■ 01110: 16384 cycles ■ 01111: 32768 cycles ■ 10000: 65536 cycles ■ 10001: 131072 cycles ■ 10010: 262144 cycles ■ 10011: Unlimited **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_lp_data_req	O	This signal is the DFI low-power data request the for DFIn channel: This controller uses this signal to inform the PHY of an opportunity to switch to a low-power mode. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-39 DFI Low Power Interface (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3) Signals (continued)

Port Name	I/O	Description
dfin_lp_data_ack	I	This signal is the DFI Low Power Data Acknowledge for DFIn channel: DFI low power data acknowledge. This signal is asserted by the PHY to acknowledge the Controller controller low power opportunity request. The PHY is not required to acknowledge the request **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_lp_data_wakeup[(DFI_LP_WAKEUP_PD_WIDTH-1):0]	O	This signal is the DFI low-power data wake-up for the DFIn channel. This signal indicates which one of the 16 wake-up times the controller is requesting for the PHY. The valid values for the PHY and the PHY respective low-power action are as follows: ■ 00000: 1 cycle ■ 00001: 2 cycles ■ 00010: 4 cycles ■ 00011: 8 cycles ■ 00100: 16 cycles ■ 00101: 32 cycles ■ 00110: 64 cycles ■ 00111: 128 cycles ■ 01000: 256 cycles ■ 01001: 512 cycles ■ 01010: 1024 cycles ■ 01011: 2048 cycles ■ 01100: 4096 cycles ■ 01101: 8192 cycles ■ 01110: 16384 cycles ■ 01111: 32768 cycles ■ 10000: 65536 cycles ■ 10001: 131072 cycles ■ 10010: 262144 cycles ■ 10011: Unlimited **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.40 DFI MC to PHY Message Interface (for n = 0; n <= 3) Signals

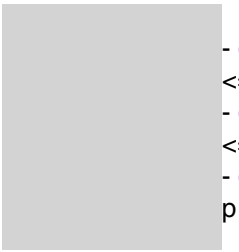
Table 2-40 DFI MC to PHY Message Interface (for n = 0; n <= 3) Signals

Port Name	I/O	Description
dfin_ctrlmsg_req	O	This signal is the DFI controller message request for the DFIn channel. When asserted, this signal indicates a valid MC-to-PHY message. If acknowledged, the request must remain asserted until the dfin_ctrlmsg_ack signal.If not acknowledged within dfi_t_ctrlmsg_resp cycles, the request is de-asserted. **Exists:** DDRCTL_DFI_CTRLMSG **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_ctrlmsg[7:0]	O	This signal is the DFI controller message command for the DFIn channel. It is valid only when the dfin_ctrlmsg_req signal is asserted. This signal encodes messages from the MC to the PHY. **Exists:** DDRCTL_DFI_CTRLMSG **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_ctrlmsg_data[15:0]	O	This signal is the DFI Controller message data for the DFIn channel. It is valid only when the dfin_ctrlmsg_req signal is asserted. Data associated with the information command transfers from the MC to the PHY. **Exists:** DDRCTL_DFI_CTRLMSG **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-40 DFI MC to PHY Message Interface (for n = 0; n <= 3) Signals (continued)

Port Name	I/O	Description
dfin_ctrlmsg_ack	I	This signal is the DFI Controller message acknowledge for the DFIn channel: When asserted, this signal indicates that the PHY received the MC message. If the message is to be acknowledged, the dfin_ctrlmsg_ack signal must assert within dfi_t_ctrlmsg_resp clock cycles. Once asserted, the dfin_ctrlmsg_ack signal must de-assert within dfi_t_ctrlmsg_max clock cycles. **Exists:** DDRCTL_DFI_CTRLMSG **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.41 DFI WCK Control Interface Signals



- dfin_wck_cs_Pp (for n = 0; n <= 3)(for p = 0; p <= 3)
- dfin_wck_en_Pp (for n = 0; n <= 3)(for p = 0; p <= 3)
- dfin_wck_toggle_Pp (for n = 0; n <= 1)(for p = 0; p <= 3)

Table 2-41 DFI WCK Control Interface Signals

Port Name	I/O	Description
dfin_wck_cs_Pp[(MEMC_NUM_RANKS-1):0] (for n = 0; n <= 3)(for p = 0; p <= 3)	O	This signal is the WCK chip select on phase *p*for the DFIn channel. This signal indicates which chip selects currently have the WCK active. More than one chip select can be active at a time. There is one bit per chip select. This signal is only valid when the dfin_wck_en_Pp signal is asserted. **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_wck_en_Pp[((DDRCTL_INST_DFI_DATA_WIDTH/16)-1):0] (for n = 0; n <= 3)(for p = 0; p <= 3)	O	This signal is the WCK clock enable on phase *p*for the DFIn channel. This signal defines when the WCK clock is driven or disabled (tri-state). **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_wck_toggle_Pp[1:0] (for n = 0; n <= 1)(for p = 0; p <= 3)	O	This signal is the WCK toggle on phase *p*for the DFIn channel. This is a 2-bit encoded value defining the state of the WCK clock. This signal is only valid when the dfin_wck_en_Pp signal is asserted. **Exists:** DDRCTL_LPDDR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.42 DFI Error Interface (for n = 0; n <= 3) Signals

Table 2-42 DFI Error Interface (for n = 0; n <= 3) Signals

Port Name	I/O	Description
dfin_error	I	DFI Error. This signal indicates that PHY has detected an error condition. **Exists:** DDRCTL_DFI_ERROR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfin_error_info[3:0]	I	DFI Error Source. Provides additional information about the source of the error detected. Only considered valid when dfi_error is asserted. Please see the relevant PHY databook for details of the error reported in this signal. **Exists:** DDRCTL_DFI_ERROR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.43 Non-DFI DDRCTL PHY Sideband Interface Signals

- dwc_lpddr5xphyn_snoop_en_Pp (for n = 0; n <= 3)(for p = 0; p <= 3)
- dwc_lpddr5xphyn_snoop_osc_running (for n = 0; n <= 3)
- dwc_ddrphyn_snoop_en_Pp (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)
- dwc_ddrphyn_snoop_osc_running (for n = 0; n <= 3)

Table 2-43 Non-DFI DDRCTL PHY Sideband Interface Signals

Port Name	I/O	Description
dwc_lpddr5xphyn_snoop_en_Pp[((DDRCTL_INST_DFI_DATAEN_WIDTH*4)-1):0] (for n = 0; n <= 3)(for p = 0; p <= 3)	O	This signal is used to indicate when the PHY snoops the MR read data on phase *p*for the DFIn channel. For LPDDR5X/5/4X PHY, The dwc_lpddr5xphyn_snoop_en_Pp is 4-bit wide for each bit of dfin_rddata_en_Pp and follows the timing of the corresponding dfin_rddata_en_Pp. Each bit in every 4-bit of dwc_lpddr5xphyn_snoop_en_Pp signals indicates the MR register to be snooped as follows: ■ dwc_lpddr5xphyn_snoop_en_Pp[4*i]: Asserted when MR18(LPDDR4) or MR35(LPDDR5) is read by controller ■ dwc_lpddr5xphyn_snoop_en_Pp[4*i+1]: Asserted when MR19(LPDDR4) or MR36(LPDDR5) is read by controller ■ dwc_lpddr5xphyn_snoop_en_Pp[4*i+2]: Asserted when MR38(LPDDR5) is read by controller ■ dwc_lpddr5xphyn_snoop_en_Pp[4*i+3]: Asserted when MR39(LPDDR5) is read by controller **Exists:** MEMC_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dwc_lpddr5xphyn_snoop_osc_running (for n = 0; n <= 3)	O	For LPDDR5X/5/4X PHY, This signal is used to indicate when the LPDDR5 device is running the DQS Oscillator on phase *p*for the DFIn channel. **Exists:** MEMC_LPDDR5X **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-43 Non-DFI DDRCTL PHY Sideband Interface Signals (continued)

Port Name	I/O	Description
dwc_ddrphyn_snoop_en_Pp[((DDRCTL_INST_DFI_DATAEN_WIDTH*4)-1):0] (for n = 0; n <= @DDRCTL_LPDDR?3:1)(for p = 0; p <= 3)	O	This signal is used to indicate when the PHY snoops the MR read data on phase *p*for the DFIn channel. For LPDDR5/4/4X PHY, The dwc_ddrphyn_snoop_en_Pp is 4-bit wide for each bit of dfin_rddata_en_Pp and follows the timing of the corresponding dfin_rddata_en_Pp. Each bit in every 4-bit of dwc_ddrphyn_snoop_en_Pp signals indicates the MR register to be snooped as follows: ■ dwc_ddrphyn_snoop_en_Pp[4*i]: Asserted when MR18(LPDDR4) or MR35(LPDDR5) is read by controller ■ dwc_ddrphyn_snoop_en_Pp[4*i+1]: Asserted when MR19(LPDDR4) or MR36(LPDDR5) is read by controller ■ dwc_ddrphyn_snoop_en_Pp[4*i+2]: Asserted when MR38(LPDDR5) is read by controller ■ dwc_ddrphyn_snoop_en_Pp[4*i+3]: Asserted when MR39(LPDDR5) is read by controller **Exists:** (!MEMC_LPDDR5X) && (DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dwc_ddrphyn_snoop_osc_running (for n = 0; n <= 3)	O	For LPDDR5/4/4X PHY, This signal is used to indicate when the LPDDR5 device is running the DQS Oscillator on phase *p*for the DFIn channel. **Exists:** (!MEMC_LPDDR5X) && (DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA) && (DDRCTL_LPDDR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.44 LPDDR4 Initialization Handshake Interface Signals

Table 2-44 LPDDR4 Initialization Handshake Interface Signals

Port Name	I/O	Description
dfi_reset_n_in	I	This signal is the DFI reset reference signal and is active low. Connect this signal to the dfi_reset_n_ref port of the other controller. If not used, tie the signal to 1. This signal is supported in LPDDR4 mode only. **Exists:** (DDRCTL_LPDDR) && (!UMCTL2_LPDDR4_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_reset_n_ref	O	This signal is the DFI reset reference signal and is active low. Connect this signal to the dfi_reset_n_in port of the other controller. This signal is supported in LPDDR4 mode only. **Exists:** (DDRCTL_LPDDR) && (!UMCTL2_LPDDR4_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
init_mr_done_in	I	This signal indicates the MRW section of the initialization is done. It is active high. Connect this signal to the init_mr_done_out port of the other controller. If not used, tie the signal to 1. This signal is supported in LPDDR4 mode only. **Exists:** (DDRCTL_LPDDR) && (!UMCTL2_LPDDR4_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-44 LPDDR4 Initialization Handshake Interface Signals (continued)

Port Name	I/O	Description
init_mr_done_out	O	This signal indicates the MRW section of the initialization is done.It is active high. Connect this signal to the init_mr_done_in port of the other controller. This signal is supported in LPDDR4 mode only. **Exists:** (DDRCTL_LPDDR) && (!UMCTL2_LPDDR4_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.45 Register Visibility Control Signals

dis_regs_ecc_syndrome -

Table 2-45 Register Visibility Control Signals

Port Name	I/O	Description
dis_regs_ecc_syndrome	I	Signal used to hide the value of ECCCSYN* and ECCUSYN* registers, e.g. for security purposes. When this value is set to 1, reading registers ECCCSYN*/ECCUSYN* returns value 0 always, otherwise it returns appropriate value. If this feature is not used, this port can be tied to 0. The value of dis_regs_ecc_syndrome signal cannot change outside of reset (presetn=0 && core_ddrc_core_rstn=0). **Exists:** MEMC_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.46 Interrupts Signals

- ecc_corrected_err_intr
- ecc_corrected_err_intr_fault
- ecc_uncorrected_err_intr
- ecc_uncorrected_err_intr_fault
- ecc_ap_err_intr
- ecc_ap_err_intr_fault
- rd_linkecc_uncorr_err_intr
- rd_linkecc_uncorr_err_intr_fault
- rd_linkecc_corr_err_intr
- rd_linkecc_corr_err_intr_fault
- ecc_corrected_err_intr_dch1
- ecc_corrected_err_intr_dch1_fault
- ecc_uncorrected_err_intr_dch1
- ecc_uncorrected_err_intr_dch1_fault
- ecc_ap_err_intr_dch1
- ecc_ap_err_intr_dch1_fault
- rd_linkecc_uncorr_err_intr_dch1
- rd_linkecc_uncorr_err_intr_fault_dch1
- rd_linkecc_corr_err_intr_dch1
- rd_linkecc_corr_err_intr_fault_dch1
- dfi_sideband_timer_err_intr
- dfi_sideband_timer_err_intr_fault
- dfi_error_intr
- dfi_error_intr_fault
- dfi_sideband_timer_err_intr_dch1
- dfi_sideband_timer_err_intr_fault_dch1
- dfi_error_intr_dch1
- dfi_error_intr_fault_dch1
- derate_temp_limit_intr
- derate_temp_limit_intr_fault
- derate_temp_limit_intr_dch1
- derate_temp_limit_intr_fault_dch1

Table 2-46 Interrupts Signals

Port Name	I/O	Description
ecc_corrected_err_intr	O	This signal is the ECC corrected error interrupt. This interrupt is asserted when a correctable ECC error is detected at the DFI. **Exists:** MEMC_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
ecc_corrected_err_intr_fault[1:0]	O	This signal is the ECC corrected error fault. This is a version of ecc_corrected_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** MEMC_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_uncorrected_err_intr	O	This signal is the ECC uncorrected error interrupt. This interrupt is asserted when an uncorrectable ECC error is detected. **Exists:** MEMC_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_uncorrected_err_intr_fault[1:0]	O	This signal is the ECC uncorrected error fault. This is a version of ecc_uncorrected_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** MEMC_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_ap_err_intr	O	This signal is the ECC address protection interrupt. This interrupt is asserted when the number of ECC errors within a burst exceeds the value set in ECCCFG1.ecc_ap_err_threshold. **Exists:** MEMC_ECCAP **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
ecc_ap_err_intr_fault[1:0]	O	This signal is the ECC address protection fault. This is a version of ecc_ap_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** MEMC_ECCAP **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_uncorr_err_intr	O	This signal is the Read Link-ECC uncorrected error interrupt. This interrupt is asserted when an uncorrectable Link-ECC error is detected. **Exists:** MEMC_LINK_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_uncorr_err_intr_fault[1:0]	O	This signal is the Read Link-ECC uncorrected error fault. This is a version of rd_linkecc_uncorr_err_intr, which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** MEMC_LINK_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_corr_err_intr	O	This signal is the Read Link-ECC corrected error interrupt. This interrupt is asserted when a correctable Link-ECC error is detected. **Exists:** MEMC_LINK_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
rd_linkecc_corr_err_intr_fault[1:0]	O	This signal is the Read Link-ECC corrected error fault. This is a version of rd_linkecc_corr_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding of ■ 01: No Fault ■ 10: Fault Detected **Exists:** MEMC_LINK_ECC **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_corrected_err_intr_dch1	O	This signal is the ECC corrected error interrupt (Channel 1). This interrupt is asserted when a correctable ECC error is detected at the DFI. **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_corrected_err_intr_dch1_fault[1:0]	O	This signal is the ECC corrected error fault (Channel 1). This is a version of ecc_corrected_err_intr_dch1 which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
ecc_uncorrected_err_intr_dch1	O	This signal is the ECC uncorrected error interrupt (Channel 1). This interrupt is asserted when a uncorrectable ECC error is detected at the DFI. **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_uncorrected_err_intr_dch1_fault[1:0]	O	This signal is the ECC uncorrected error fault (Channel 1). This is a version of ecc_uncorrected_err_intr_dch1 which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10:: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
ecc_ap_err_intr_dch1	O	This signal is the ECC address protection interrupt (Channel 1). This interrupt is asserted when a number of ECC errors within a burst exceeds the value set in ECCCFG1.ecc_ap_err_threshold. **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECCAP) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
ecc_ap_err_intr_dch1_fault[1:0]	O	This signal is the ECC address protection fault (Channel 1). This is a version of ecc_ap_err_intr_dch1 which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_ECCAP) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_uncorr_err_intr_dch1	O	This signal is the Read Link-ECC uncorrected error interrupt (Channel 1). This interrupt is asserted when a uncorrectable Link-ECC error is detected. **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_LINK_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_uncorr_err_intr_fault_dch1[1:0]	O	This signal is the Read Link-ECC uncorrected error fault (Channel 1). This is a version of rd_linkecc_uncorr_err_intr_dch1 which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_LINK_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
rd_linkecc_corr_err_intr_dch1	O	This signal is the Read Link-ECC corrected error interrupt (Cahnnel 1). This interrupt is asserted when a correctable Link-ECC error is detected. **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_LINK_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
rd_linkecc_corr_err_intr_fault_dch1[1:0]	O	This signal is the Read Link-ECC corrected error fault (Channel 1). This is a version of rd_linkecc_corr_err_intr_dch1 which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (MEMC_LINK_ECC) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_sideband_timer_err_intr	O	This signal is the DFI sideband watchdog timer interrupt. This interrupt is asserted when an error is detected on any of the DFI Sideband watchdog timers. **Exists:** DDRCTL_DFI_SB_WDT **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
dfi_sideband_timer_err_intr_fault[1:0]	O	This signal is the DFI sideband watchdog timer error fault. This is a version of dfi_sideband_timer_err_intr which cannot be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** DDRCTL_DFI_SB_WDT **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_error_intr	O	This signal is the DFI Error interface interrupt. This interrupt is asserted when an error is detected on the DFI Error interface input coming from PHY. **Exists:** DDRCTL_DFI_ERROR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_error_intr_fault[1:0]	O	This signal is the DFI Error interface fault. This is a version of dfi_error_intr which cannot be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** DDRCTL_DFI_ERROR **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
dfi_sideband_timer_err_intr_dch1	O	This signal is the DFI sideband watchdog timer interrupt (Channel 1). This interrupt is asserted when an error is detected on any of the DFI Sideband watchdog timers. **Exists:** (UMCTL2_DUAL_CHANNEL) && (DDRCTL_DFI_SB_WDT) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_sideband_timer_err_intr_fault_dch1[1:0]	O	This signal is the DFI sideband watchdog timer error fault (Channel 1). This is a version of dfi_sideband_timer_err_intr_dch1 which cannot be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (DDRCTL_DFI_SB_WDT) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
dfi_error_intr_dch1	O	This signal is the DFI Error interface interrupt (Channel 1). This interrupt is asserted when an error is detected on the DFI Error interface input coming from PHY. **Exists:** (UMCTL2_DUAL_CHANNEL) && (DDRCTL_DFI_ERROR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
dfi_error_intr_fault_dch1[1:0]	O	This signal is the DFI Error interface fault (Channel 1). This is a version of dfi_error_intr_dch1 which cannot be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (UMCTL2_DUAL_CHANNEL) && (DDRCTL_DFI_ERROR) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
derate_temp_limit_intr	O	This signal is the derate temperature limit interrupt indicating that the LPDDR4/5 SDRAM temperature operating limit is exceeded. It is cleared by the DERATECTL.derate_temp_limit_intr_clr register. **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
derate_temp_limit_intr_fault[1:0]	O	This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-46 Interrupts Signals (continued)

Port Name	I/O	Description
derate_temp_limit_intr_dch1	O	This signal is the derate temperature limit interrupt indicating that the LPDDR4/5 SDRAM temperature operating limit is exceeded (channel1). This signal is cleared by the DERATECTL.derate_temp_limit_intr_clr register. **Exists:** (DDRCTL_DDR_OR_MEMC_LPDDR4) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
derate_temp_limit_intr_fault_dch1[1:0]	O	This signal is the derate temperature limit fault (channel 1). This is a version of derate_temp_limit_intr which can not be disabled or forced by a register. It is a 2-bit antivalent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** (DDRCTL_DDR_OR_MEMC_LPDDR4) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.47 APB Device Interface Signals

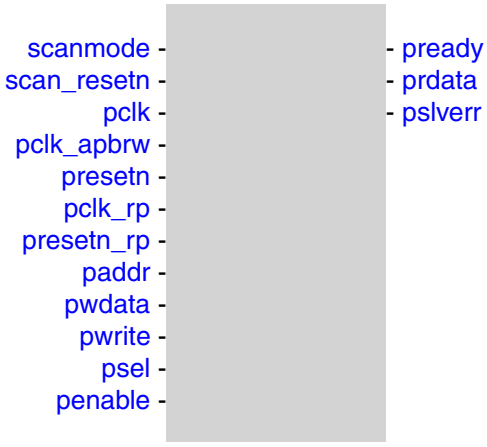


Table 2-47 APB Device Interface Signals

Port Name	I/O	Description
scanmode	I	This signal is indicates that the controller is in scan mode. **Exists:** UMCTL2_USE_SCANMODE **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
scan_resetn	I	This signal is the reset used when the controller is in scan mode. **Exists:** UMCTL2_USE_SCANMODE **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pclk	I	This signal is the APB clock. It is used in the APB interface to program registers. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-47 APB Device Interface Signals (continued)

Port Name	I/O	Description
pclk_apbrw	I	Same clock (synchronous to) as pclk, which can be gated when there are no APB Read/Write access. **Exists:** DDRCTL_EXTRA_CLK_APB **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
presetn	I	APB reset. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pclk_rp	I	This signal is the free-running APB clock. It is used in Register Parity Protection. **Exists:** UMCTL2_REGPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
presetn_rp	I	This signal is the free-running APB reset. It is used in Register Parity Protection. **Exists:** UMCTL2_REGPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
paddr[(UMCTL2_APB_AW-1):0]	I	This signal is the APB address. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-47 APB Device Interface Signals (continued)

Port Name	I/O	Description
pwdata[(UMCTL2_APB_DW-1):0]	I	This signal is the APB write data. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pwrite	I	This signal is the APB direction. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
psel	I	This signal is the APB peripheral select. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
penable	I	This signal is the APB enable. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pready	O	This signal is the APB ready. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

Table 2-47 APB Device Interface Signals (continued)

Port Name	I/O	Description
prdata[(UMCTL2_APB_DW-1):0]	O	This signal is the APB read data. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pslverr	O	This signal is the APB error. This signal is asserted only when APB address is out of range. **Exists:** Always **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.48 APB4 Device Interface Signals

Table 2-48 APB4 Device Interface Signals

Port Name	I/O	Description
pprot[2:0]	I	APB4 PPROT input. **Exists:** DDRCTL_APB4_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
pstrb[((UMCTL2_APB_DW/8)-1):0]	I	APB4 PSTRB input. **Exists:** DDRCTL_APB4_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.49 APB5 Device Interface Signals

pnse -

Table 2-49 APB5 Device Interface Signals

Port Name	I/O	Description
pnse	I	APB5 PNSE input. **Exists:** DDRCTL_APB5_EN **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.50 Per-bank refresh Bank number Signals

- hif_refresh_req_bank
- hif_refresh_req_bank_dch1

Table 2-50 Per-bank refresh Bank number Signals

Port Name	I/O	Description
hif_refresh_req_bank[((MEMC_NUM_RANKS*MEMC_BANK_BITS)-1):0]	O	This signal indicates the next bank that is refreshed; for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal. DEBUG ONLY **Exists:** SNPS_RSVDPARAM_666 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
hif_refresh_req_bank_dch1[((MEMC_NUM_RANKS*MEMC_BANK_BITS)-1):0]	O	This signal indicates the next bank that is refreshed (channel 1); for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal. DEBUG_ONLY **Exists:** (SNPS_RSVDPARAM_666) && (UMCTL2_DUAL_CHANNEL) **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

2.51 Register Parity Protection Signals

- reg_par_err_intr
- reg_par_err_intr_fault

Table 2-51 Register Parity Protection Signals

Port Name	I/O	Description
reg_par_err_intr	O	This signal is the register parity error interrupt. This interrupt is asserted when a register parity error is detected. It may be cleared by writing to the REGPARCFG.reg_par_err_intr_clr register. **Exists:** UMCTL2_REGPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN
reg_par_err_intr_fault[1:0]	O	This signal is the register parity error fault. This is a version of reg_par_err_intr which cannot be disabled or forced through a register. It is a 2-bit anti-valent signal with encoding as follows: ■ 01: No Fault ■ 10: Fault Detected **Exists:** UMCTL2_REGPAR_EN_1 **Synchronous To:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Registered:** For the exact value for your configuration, see coreConsultant IO report/IPXACT. **Power Domain:** DDRCTL_DOMAIN

3

Register Descriptions

This chapter details all possible registers in the controller. They are arranged hierarchically into maps and blocks (banks). For configurable IP titles, your actual configuration might not contain all of these registers.

Attention: For configurable IP titles, do not use this document to determine the exact attributes of your register map. It is for reference purposes only.

When you configure the controller in coreConsultant, you must access the register attributes for your actual configuration at `workspace/report/ComponentRegisters.html` or `workspace/report/ComponentRegisters.xml` after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the registers that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the Offset and Memory Access values might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

Exists Expressions

These expressions indicate the combination of configuration parameters required for a register, field, or block to exist in the memory map. The expression is only valid in the local context and does not indicate the conditions for existence of the parent. For example, the expression for a bit field in a register assumes that the register exists and does not include the conditions for existence of the register.

Offset

The term *Offset* is synonymous with *Address.*

Memory Access Attributes

The Memory Access attribute is defined as `<ReadBehavior>/<WriteBehavior>` which are defined in the following table.

Table 3-1 Possible Read and Write Behaviors

Read (or Write) Behavior	Description
RC	A read clears this register field.
RS	A read sets this register field.
RM	A read modifies the contents of this register field in a manner not described by any of the above.
Wo	You can only write once to this register field.
W1C	A write of 1 clears this register field.
W1S	A write of 1 sets this register field.
W1T	A write of 1 toggles this register field.
W0C	A write of 0 clears this register field.
W0S	A write of 0 sets this register field.
W0T	A write of 0 toggles this register field.
WC	Any write clears this register field.
WS	Any write sets this register field.
WM	A write modifies this register field in a manner not described by any of the above.
no Read Behavior attribute	You cannot read this register. It is Write-Only.
no Write Behavior attribute	You cannot write to this register. It is Read-Only.

Table 3-2 Memory Access Examples

Memory Access	Description
R	Read-only register field.
W	Write-only register field.
R/W	Read/write register field.
R/W1C	You can read this register field. Writing 1 clears it.
RC/W1C	Reading this register field clears it. Writing 1 clears it.
R/Wo	You can read this register field. You can only write to it once.

Special Optional Attributes

Some register fields might use the following optional attributes.

Table 3-3 Optional Attributes

Attribute	Description
Volatile	As defined by the IP-XACT specification. If true, indicates in the case of a write followed by read, or in the case of two consecutive reads, there is no guarantee as to what is returned by the read on the second transaction or that this return value is consistent with the write or read of the first transaction. The element implies there is some additional mechanism by which this field can acquire new values other than by reads/writes/resets and other access methods known to IP-XACT. For example, when the controller updates the register field contents.
Testable	As defined by the IP-XACT specification. Possible values are unconstrained, untestable, readOnly, writeAsRead, restore. Untestable means that this field is untestable by a simple automated register test. For example, the read-write access of the register is controlled by a pin or another register. readOnly means that you should not write to this register; only read from it. This might apply for a register that modifies the contents of another register.
Reset Mask	As defined by the IP-XACT specification. Indicates that this register field has an unknown reset value. For example, the reset value is set by another register or an input pin; or the register is implemented using RAM.
* Varies	Indicates that the memory access (or reset) attribute (read, write behavior) is not fixed. For example, the read-write access of the register is controlled by a pin or another register. Or when the access depends on some configuration parameter; in this case the post-configuration report in coreConsultant gives the actual access value.

Note: For more information about programming the registers, refer to the "Programming" Chapter of the Databook.

The Programming Mode Field:

The "Programming Mode" field in the description column of the register tables specifies the type of register. The DDRCTL registers belong to one of the following types:

- Static: Can be written only when the controller is in reset.
- Dynamic: Can be written at any time during operation.
- Quasi Dynamic: Can be written when the controller is in reset and some specific conditions outside reset. There are four groups this type.

Note:

Programming mode describes software responsibility – when software is allowed to update the register field. If software is trying to update the register fields while it is not allowed, the register field may or may not be updated and it can cause unexpected behavior.

For example, Static register may or may not be written outside of reset or SWCTLSTATIC.sw_static_unlock=0, but it is not allowed unless Synopsys explicitly suggests doing that. Similarly, Quasi-dynamic register may or may not be written outside of reset or SWCTL.sw_done=1, but it is not allowed unless Synopsys explicitly suggests doing that.

For more information about the dynamic and quasi dynamic registers, see the "Programming" Chapter of the Databook.

Notes on Timing Registers:

Note 1:

This note refers to register fields whose names include "x32", or "x1024". Computation for these registers are in units of 32, or 1024 clocks.

The DDRCTL contains a timer which issues a pulse once every 32 clock cycles, another which issues a pulse once every 1024 clock cycles. "x32" register fields count pulses of the 32-cycle timer, and "x1024" register fields count pulses of the 1024-cycle timer. These timers are shared by the logic for all of these register fields, and the various periods start without any guaranteed relation to the phase of this timer.

Therefore for "x32" register fields:

- A programmed value of 0 gives 0 clock cycles
- A programmed value of 1 gives a 1 to 32 cycle delay
- A programmed value of 2 gives a 33 to 64 cycle delay and so on

For "x1024" register fields:

- A programmed value of 0 gives no delay
- A programmed value of 1 gives a 1 to 1,024 cycle delay
- A programmed value of 2 gives a 1,025 to 2,048 cycle delay and so on

For minimum delays, the control signal must be set to the smallest number for which the resulting delay is ALWAYS greater than or equal to the required delay; for maximum delays or nominal refresh, this must be set such that the delay is ALWAYS lesser than or equal to the required delay.

This scheme is used to reduce the gate count that would be required to enforce these constraints more precisely.

Note 2

Most of the SDRAM timing registers are in terms of clock cycles. But the value given in an SDRAM datasheet may be in terms of ns/ps. These are primarily minimum timings. Before using them to calculate value to program in the register, it is expected that these are divided by tCK (SDRAM clock period) and rounded up to the next integer value if division does not result in a whole integer value.

Exceptions to this rule are related to maximum timings, where these should be rounded down rather than rounded up, if division does not result in a whole integer value.

These include:

- RFSHSET1TMG0.t_refi_x1_x32
- RFSHSET2TMG0.t_ras_max

Certain SDRAM timing registers clarify this by using the following functions in their descriptions:

- RoundUp (X/Y) means that if X divided by Y does not result in a whole integer value, the result should be rounded up to the next integer value. For example, RoundUp(1000/150) = 7, RoundUp(1050/150) = 7.
- RoundDown (X/Y) means that if X divided by Y does not result in a whole integer value, the result should be rounded down to the next integer value. For example, RoundDown(1000/150) = 6, RoundDown(1050/150) = 7.

The DDRCTL can support up to 4 different sets of frequency sets. Each frequency set is divided in 4 blocks as shown in Figure 1.

- FREQ block includes registers storing all timings required for correct operations of the controller
- DDRC block has all control registers required by the DDR controller
- ARB block stores XPI port configuration
- ADDR block has registers that define the address map.

The FREQ block is the only block that is currently replicated in every frequency set.

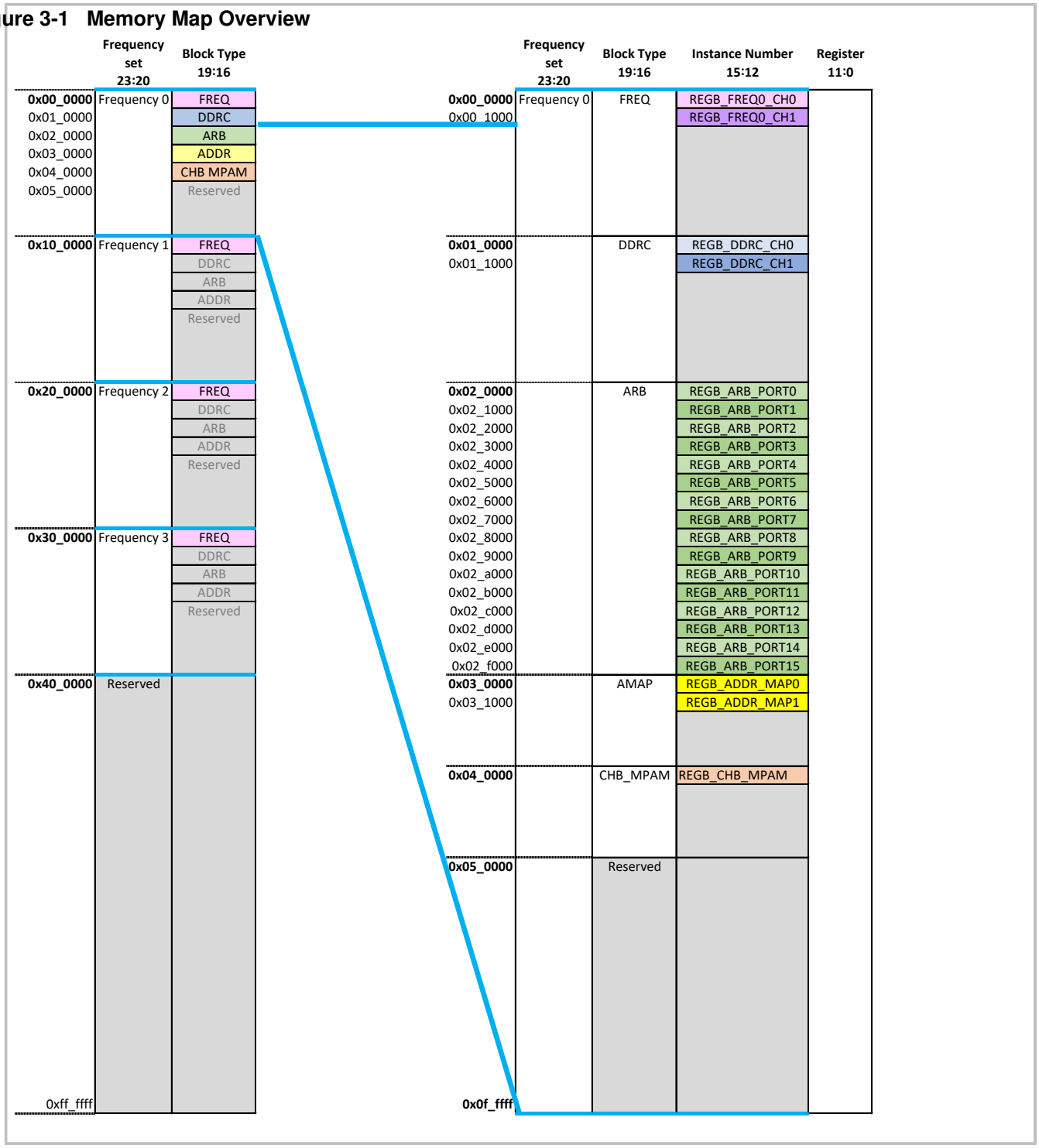
Each region has an equal dedicated address space and internally it can have up to 16 instances of register blocks.

Only instances required for a given configuration are present in the design. For example, a single channel configuration will not have neither REG_FREQ0_CH1 nor REGB_DDRC_CH1. This will ultimately save silicon area when not needed.

Note 3

Most timing registers are in CK cycle units. In LPDDR5, some timing registers use WCK cycles. If it is unclear, use the following table to translate clock names in this document.

Figure 3-1 Memory Map Overview



Register definitions for each component memory map.

Table 3-4 Registers for the DWC_ddrctl_map Memory Map

Register	Offset	Description
Frequency set f Channel c Registers REGB_FREQf_CHc (for f = 0; f <= 14)(for c = 0; c <= 1) Exists: UMCTL2_FREQUENCY_NUM>f && UMCTL2_NUM_DATA_CHANNEL>c		
"DRAMSET1TMG0" on page 272	0x0+f*0x100000+c*0x1000	SDRAM Timing Register 0 belonging to Timing Set 1
"DRAMSET1TMG1" on page 275	0x4+f*0x100000+c*0x1000	SDRAM Timing Register 1 belonging to Timing Set 1
"DRAMSET1TMG2" on page 277	0x8+f*0x100000+c*0x1000	SDRAM Timing Register 2 belonging to Timing Set 1
"DRAMSET1TMG3" on page 281	0xc+f*0x100000+c*0x1000	SDRAM Timing Register 3 belonging to Timing Set 1
"DRAMSET1TMG4" on page 283	0x10+f*0x100000+c*0x1000	SDRAM Timing Register 4 belonging to Timing Set 1
"DRAMSET1TMG5" on page 285	0x14+f*0x100000+c*0x1000	SDRAM Timing Register 5 belonging to Timing Set 1
"DRAMSET1TMG6" on page 287	0x18+f*0x100000+c*0x1000	SDRAM Timing Register 6 belonging to Timing Set 1
"DRAMSET1TMG7" on page 288	0x1c+f*0x100000+c*0x1000	SDRAM Timing Register 7 belonging to Timing Set 1
"DRAMSET1TMG9" on page 289	0x24+f*0x100000+c*0x1000	SDRAM Timing Register 9 belonging to Timing Set 1
"DRAMSET1TMG12" on page 291	0x30+f*0x100000+c*0x1000	SDRAM Timing Register 12 belonging to Timing Set 1
"DRAMSET1TMG13" on page 292	0x34+f*0x100000+c*0x1000	SDRAM Timing Register 13 belonging to Timing Set 1
"DRAMSET1TMG14" on page 294	0x38+f*0x100000+c*0x1000	SDRAM Timing Register 14 belonging to Timing Set 1
"DRAMSET1TMG17" on page 295	0x44+f*0x100000+c*0x1000	SDRAM Timing Register 17 belonging to Timing Set 1
"DRAMSET1TMG23" on page 296	0x5c+f*0x100000+c*0x1000	SDRAM Timing Register 23 belonging to Timing Set 1
"DRAMSET1TMG24" on page 297	0x60+f*0x100000+c*0x1000	SDRAM Timing Register 24 belonging to Timing Set 1
"DRAMSET1TMG25" on page 299	0x64+f*0x100000+c*0x1000	SDRAM Timing Register 25 belonging to Timing Set 1

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"DRAMSET1TMG30" on page 301	0x78+f*0x100000+c*0x1000	SDRAM Timing Register 30 belonging to Timing Set 1
"DRAMSET1TMG32" on page 302	0x80+f*0x100000+c*0x1000	SDRAM Timing Register 32 belonging to Timing Set 1
"DRAMSET1TMG34" on page 304	0x88+f*0x100000+c*0x1000	SDRAM Timing Register 34 belonging to Timing Set 1
"DRAMSET1TMG35" on page 307	0x8c+f*0x100000+c*0x1000	SDRAM Timing Register 35 belonging to Timing Set 1
"DRAMSET1TMG36" on page 309	0x90+f*0x100000+c*0x1000	SDRAM Timing Register 36 belonging to Timing Set 1
"DRAMSET1TMG37" on page 311	0x94+f*0x100000+c*0x1000	SDRAM Timing Register 37 belonging to Timing Set 1
"DRAMSET1TMG38" on page 313	0x90+f*0x100000+c*0x1000	SDRAM Timing Register 38 belonging to Timing Set 1
"INITMR0" on page 316	0x500+f*0x100000+c*0x1000	SDRAM Initialization MR Setting Register 0
"INITMR1" on page 317	0x504+f*0x100000+c*0x1000	SDRAM Initialization MR Setting Register 1
"INITMR2" on page 318	0x508+f*0x100000+c*0x1000	SDRAM Initialization MR Setting Register 2
"INITMR3" on page 319	0x50c+f*0x100000+c*0x1000	SDRAM Initialization MR Setting Register 3
"DFITMG0" on page 320	0x580+f*0x100000+c*0x1000	DFI Timing Register 0
"DFITMG1" on page 322	0x584+f*0x100000+c*0x1000	DFI Timing Register 1
"DFITMG2" on page 324	0x588+f*0x100000+c*0x1000	DFI Timing Register 2
"DFITMG4" on page 326	0x590+f*0x100000+c*0x1000	DFI Timing Register 4
"DFITMG5" on page 328	0x594+f*0x100000+c*0x1000	DFI Timing Register 5
"DFITMG6" on page 330	0x598+f*0x100000+c*0x1000	DFI Timing Register 6
"DFITMG7" on page 332	0x59c+f*0x100000+c*0x1000	DFI Timing Register 7
"DFILPTMG0" on page 333	0x5a0+f*0x100000+c*0x1000	DFI Low Power Timing Register 0
"DFILPTMG1" on page 337	0x5a4+f*0x100000+c*0x1000	DFI Low Power Timing Register 1
"DFIUPDTMG0" on page 339	0x5a8+f*0x100000+c*0x1000	DFI Update Timing Register 0
"DFIUPDTMG1" on page 340	0x5ac+f*0x100000+c*0x1000	DFI Update Timing Register 1
"DFIMSGTMG0" on page 342	0x5b0+f*0x100000+c*0x1000	DFI MC-PHY Message Timing Register 0
"DFIUPDTMG2" on page 343	0x5b4+f*0x100000+c*0x1000	DFI Update Timing Register 2

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"DFIUPDTMG3" on page 346	0x5b8+f*0x100000+c*0x1000	DFI Update Timing Register 3
"RFSHSET1TMG0" on page 347	0x600+f*0x100000+c*0x1000	Refresh Timing Register 0 belonging to Timing Set 1
"RFSHSET1TMG1" on page 351	0x604+f*0x100000+c*0x1000	Refresh Timing Register 1 belonging to Timing Set 1
"RFSHSET1TMG2" on page 353	0x608+f*0x100000+c*0x1000	Refresh Timing Register 2 belonging to Timing Set 1
"RFSHSET1TMG3" on page 354	0x60c+f*0x100000+c*0x1000	Refresh Timing Register 3 belonging to Timing Set 1
"RFSHSET1TMG4" on page 355	0x610+f*0x100000+c*0x1000	Refresh Timing Register 4 belonging to Timing Set 1
"RFSHSET1TMG5" on page 357	0x614+f*0x100000+c*0x1000	Refresh Timing Register 5 belonging to Timing Set 1
"RFSHSET1TMG11" on page 359	0x62c+f*0x100000+c*0x1000	Refresh Timing Register 11 belonging to Timing Set 1
"RFSHSET1TMG12" on page 360	0x630+f*0x100000+c*0x1000	Refresh Timing Register 12 belonging to Timing Set 1
"RFMSET1TMG0" on page 362	0x650+f*0x100000+c*0x1000	RFM Timing Register 0 belonging to Timing Set 1
"RFMSET1TMG1" on page 363	0x654+f*0x100000+c*0x1000	RFM Timing Register 1 belonging to Timing Set 1
"ZQSET1TMG0" on page 364	0x800+f*0x100000+c*0x1000	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
"ZQSET1TMG1" on page 365	0x804+f*0x100000+c*0x1000	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
"ZQSET1TMG2" on page 366	0x808+f*0x100000+c*0x1000	ZQ Timing Register 2 belonging to DRAM ZQ timing set 1
"DQSOSCCTL0" on page 367	0xa80+f*0x100000+c*0x1000	DQS/WCK Oscillator Control Register 0
"DERATEINT" on page 369	0xb00+f*0x100000+c*0x1000	Temperature Derate Interval Register
"DERATEVAL0" on page 370	0xb04+f*0x100000+c*0x1000	Temperature Derate Timing Register 0
"DERATEVAL1" on page 372	0xb08+f*0x100000+c*0x1000	Temperature Derate Timing Register 1
"HWLPTMG0" on page 374	0xb80+f*0x100000+c*0x1000	Hardware Low Power Timing Register 0
"DVFSCTL0" on page 376	0xb84+f*0x100000+c*0x1000	Dynamic Voltage and Frequency Scaling (DVFS) Control Register

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"SCHEDTMG0" on page 377	0xc00+f*0x100000+c*0x1000	Scheduler Control Register
"PERFHPR1" on page 379	0xc80+f*0x100000+c*0x1000	High Priority Read CAM Register 1
"PERFLPR1" on page 381	0xc84+f*0x100000+c*0x1000	Low Priority Read CAM Register 1
"PERFWR1" on page 383	0xc88+f*0x100000+c*0x1000	Write CAM Register 1
"TMGCFG" on page 385	0xd00+f*0x100000+c*0x1000	Timing Configuration Register
"RANKTMG0" on page 386	0xd04+f*0x100000+c*0x1000	Rank Control Timing 0
"RANKTMG1" on page 389	0xd08+f*0x100000+c*0x1000	Rank Timing Register 1
"PWRTMG" on page 391	0xd0c+f*0x100000+c*0x1000	Low Power Timing Register
"DDR4PPRTMG0" on page 393	0xd30+f*0x100000+c*0x1000	PPR Timing 0
"DDR4PPRTMG1" on page 395	0xd34+f*0x100000+c*0x1000	PPR Timing 1
"LNKECCCTL0" on page 396	0xd80+f*0x100000+c*0x1000	Link-ECC Control Register 0
DDRC Channel 0 Registers REGB_DDRC_CH0 Exists: Always		
"MSTR0" on page 397	0x10000	Master Register0
"MSTR2" on page 401	0x10008	Master Register2
"MSTR4" on page 402	0x10010	Master Register4
"STAT" on page 404	0x10014	Operating Mode Status Register
"MRCTRL0" on page 407	0x10080	Mode Register Read/Write Control Register 0.
"MRCTRL1" on page 411	0x10084	Mode Register Read/Write Control Register 1
"MRSTAT" on page 412	0x10090	Mode Register Read/Write Status Register
"MRRDATA0 " on page 414	0x10094	Mode Register Read Data 0
"MRRDATA1 " on page 415	0x10098	Mode Register Read Data 1
"DERATECTL0" on page 416	0x10100	Temperature Derate Control Register 0
"DERATECTL1" on page 419	0x10104	Temperature Derate Control Register 1
"DERATECTL2" on page 421	0x10108	Temperature Derate Control Register 2
"DERATECTL3" on page 423	0x1010c	Temperature Derate Control Register 3
"DERATECTL4" on page 424	0x10110	Temperature Derate Control Register 4
"DERATECTL5" on page 425	0x10114	Temperature Derate Control Register 5

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"DERATECTL6" on page 427	0x10118	Temperature Derate Control Register 6
"DERATESTAT0 " on page 429	0x10120	Temperature Derate Status Register 0
"DERATEDBGCTL" on page 430	0x10128	Temperature Derate Debug Contrl Register
"DERATEDBGSTAT " on page 431	0x1012c	Temperature Derate Debug Status Register
"PWRCTL" on page 433	0x10180	Low Power Control Register
"HWLPCTL" on page 437	0x10184	Hardware Low Power Control Register
"CLKGATECTL" on page 438	0x1018c	clock gate control
"RFSHMOD0" on page 440	0x10200	Refresh Mode Register 0
"RFSHCTL0" on page 443	0x10208	Refresh Control Register 0
"RFMMOD0" on page 445	0x10220	RFM Mode Register 0
"RFMMOD1" on page 447	0x10224	RFM Mode Register 1
"RFMCTL" on page 448	0x10228	RFM Control Register
"RFMSTAT" on page 449	0x1022c	RFM Status Register
"ZQCTL0" on page 450	0x10280	ZQ Control Register 0
"ZQCTL1" on page 452	0x10284	ZQ Control Register 1
"ZQCTL2" on page 453	0x10288	ZQ Control Register 2
"ZQSTAT" on page 455	0x1028c	ZQ Status Register
"DQSOSCRUNTIME" on page 456	0x10300	DQS/WCK Oscillator Runtime Register
"DQSOSCSTAT0 " on page 459	0x10304	DQS/WCK Oscillator Status Register 0
"DQSOSCCFG0" on page 461	0x10308	DQSOSC Config Register 0
"SCHED0" on page 462	0x10380	Scheduler Control Register 0
"SCHED1" on page 469	0x10384	Scheduler Control Register 1
"SCHED3" on page 473	0x1038c	Scheduler Control Register 3
"SCHED4" on page 475	0x10390	Scheduler Control Register 4
"SCHED5" on page 477	0x10394	Scheduler Control Register 5.
"HWFFCCTL" on page 479	0x10400	Hardware Fast Frequency Change (HWFFC) Control Register.

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"HWFFCSTAT" on page 482	0x10404	Hardware Fast Frequency Change (HWFFC) Status Register
"HWFFC_MRWBUF_CTRL0" on page 484	0x10410	Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
"HWFFC_MRWBUF_CTRL1" on page 486	0x10414	Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
"HWFFC_MRWBUF_STAT" on page 487	0x10418	Hardware Fast Frequency Change (HWFFC) MRW buffer status register
"DFILPCFG0" on page 488	0x10500	DFI Low Power Configuration Register 0
"DFIUPD0" on page 491	0x10508	DFI Update Register 0
"DFIMISC" on page 493	0x10510	DFI Miscellaneous Control Register
"DFISTAT" on page 496	0x10514	DFI Status Register
"DFIPHYMSTR" on page 497	0x10518	DFI PHY Master
"DFI0MSGCTL0" on page 498	0x10520	DFI0 Message Control Register 0.
"DFI0MSGSTAT0 " on page 500	0x10524	DFI0 Message Status Register 0
"DFISBINTRPTCFG" on page 501	0x10528	DFI Sideband Watchdog Timer Interrupt Configuration Register
"DFISBPOISONCFG" on page 503	0x10530	DFI Sideband Watchdog Timer Poison Control Register
"DFISBTIMERSTAT" on page 507	0x10538	DFI Sideband Watchdog Timer Status Register
"DFISBTIMERSTAT1 " on page 509	0x10540	DFI Sideband Watchdog Timer Status Register 1
"DFIERRINTRPTCFG" on page 510	0x10548	DFI Error Interface Interrupt Configuration Register
"DFIERRORSTAT" on page 512	0x10550	DFI Error Interface Status Register
"DFIERRORSTAT1 " on page 513	0x10558	DFI Error Interface Status Register 1
"POISONCFG" on page 514	0x10580	AXI Poison Configuration Register. Common for all AXI ports
"POISONSTAT" on page 516	0x10584	AXI Poison Status Register
"ECCCFG0" on page 525	0x10600	ECC Configuration Register 0
"ECCCFG1" on page 529	0x10604	ECC Configuration Register 1

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"ECCSTAT" on page 533	0x10608	SECDED ECC Status Register
"ECCCTL" on page 535	0x1060c	ECC Clear Register
"ECCERRCNT" on page 539	0x10610	ECC Error Counter Register
"ECCCADDR0" on page 540	0x10614	ECC Corrected Error Address Register 0
"ECCCADDR1" on page 541	0x10618	ECC Corrected Error Address Register 1
"ECCCSYN0" on page 543	0x1061c	ECC Corrected Syndrome Register 0
"ECCCSYN1" on page 544	0x10620	ECC Corrected Syndrome Register 1
"ECCCSYN2" on page 545	0x10624	ECC Corrected Syndrome Register 2
"ECCBITMASK0" on page 547	0x10628	ECC Corrected Data Bit Mask Register 0
"ECCBITMASK1" on page 548	0x1062c	ECC Corrected Data Bit Mask Register 1
"ECCBITMASK2" on page 549	0x10630	ECC Corrected Data Bit Mask Register 2
"ECCUADDR0" on page 550	0x10634	ECC Uncorrected Error Address Register 0
"ECCUADDR1" on page 551	0x10638	ECC Uncorrected Error Address Register 1
"ECCUSYN0" on page 553	0x1063c	ECC Uncorrected Syndrome Register 0
"ECCUSYN1" on page 554	0x10640	ECC Uncorrected Syndrome Register 1
"ECCUSYN2" on page 555	0x10644	ECC Uncorrected Syndrome Register 2
"ECCPOISONADDR0" on page 557	0x10648	ECC Data Poisoning Address Register 0.
"ECCPOISONADDR1" on page 559	0x1064c	ECC Data Poisoning Address Register 1.
"ECCAPSTAT" on page 561	0x10664	Address protection within ECC Status Register
"OCPARCFG0" on page 562	0x10680	On-Chip Parity Configuration Register 0
"OCPARCFG1" on page 566	0x10684	On-Chip Parity Configuration Register 1
"OCPARSTAT0 " on page 568	0x10688	On-Chip Parity Status Register 0
"OCPARSTAT1 " on page 574	0x1068c	On-Chip Parity Status Register 1
"OCPARSTAT2 " on page 581	0x10690	On-Chip Parity Status Register 2
"OCPARSTAT3 " on page 583	0x10694	On-Chip Parity Read Data Log Register 0
"OCPARSTAT4 " on page 584	0x10698	On-Chip Parity Write Address Log Register 0
"OCPARSTAT5 " on page 585	0x1069c	On-Chip Parity Write Address Log Register 1

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"OCPARSTAT6 " on page 586	0x106a0	On-Chip Parity Read Address Log Register 0
"OCPARSTAT7 " on page 587	0x106a4	On-Chip Parity Read Address Log Register 1
"OCPARSTAT8 " on page 588	0x106a8	On-Chip Parity Read Data Log Register 1
"OCSAPCFG0" on page 589	0x106b0	On-Chip external SRAM Address Protection Configuration Register 0
"OCECCCFG0" on page 591	0x10700	On-Chip ECC Configuration Register 0
"OCECCCFG1" on page 593	0x10704	On-Chip ECC Configuration Register 1
"OCECCSTAT0 " on page 596	0x10708	On-Chip ECC Status Register 0
"OCECCSTAT1 " on page 597	0x1070c	On-Chip ECC Status Register 1
"OCECCSTAT2 " on page 601	0x10710	On-Chip ECC Status Register 2
"OCCAPCFG" on page 602	0x10780	On-Chip command/Address Protection Configuration Register
"OCCAPSTAT" on page 605	0x10784	On-Chip command/Address Protection Status Register
"OCCAPCFG1" on page 607	0x10788	On-Chip command/Address Protection Configuration Register 1
"OCCAPSTAT1 " on page 611	0x1078c	On-Chip command/Address Protection Status Register 1
"OCCAPCFG2" on page 614	0x10790	On-Chip command/Address Protection Configuration Register 2
"OCCAPSTAT2 " on page 615	0x10794	On-Chip command/Address Protection Status Register 2
"REGPARCFG" on page 616	0x10880	Register Parity Configuration Register
"REGPARSTAT " on page 618	0x10884	Register Parity Status Register
"LNKECCCTL1" on page 619	0x10984	Link-ECC Control Register 1
"LNKECCPOISONCTL0" on page 621	0x10988	Link-ECC Poison Control Register 0
"LNKECCPOISONSTAT" on page 623	0x1098c	Link-ECC Poison Status Register
"LNKECCINDEX" on page 624	0x10990	Link-ECC Index Register
"LNKECCERRCNT0" on page 625	0x10994	Link-ECC Error Status Register 0
"LNKECCERRSTAT" on page 626	0x10998	Link-ECC Error Status Register 1

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"LNKECCCADDR0" on page 627	0x109e0	Link ECC Corrected Error Address Register 0
"LNKECCCADDR1" on page 628	0x109e4	Link ECC Corrected Error Address Register 1
"LNKECCUADDR0" on page 630	0x109e8	Link ECC Uncorrected Error Address Register 0
"LNKECCUADDR1" on page 631	0x109ec	Link ECC Uncorrected Error Address Register 1
"OPCTRL0" on page 633	0x10b80	Operation Control Register 0
"OPCTRL1" on page 635	0x10b84	Operation Control Register 1
"OPCTRLCAM" on page 636	0x10b88	CAM Operation Control Register
"OPCTRLCMD" on page 639	0x10b8c	Command Operation Control Register
"OPCTRLSTAT" on page 641	0x10b90	Status Operation Control Register
"OPCTRLCAM1" on page 643	0x10b94	CAM Operation Control Register 1
"OPREFCTRL0" on page 644	0x10b98	Refresh Operation Control Register 0
"OPREFCTRL1" on page 656	0x10b9c	Refresh Operation Control Register 1
"OPREFSTAT0 " on page 668	0x10ba0	Refresh Operation Status Register 0
"OPREFSTAT1 " on page 680	0x10ba4	Refresh Operation Status Register 1
"SWCTL" on page 692	0x10c80	Software Register Programming Control Enable
"SWSTAT" on page 693	0x10c84	Software Register Programming Control Status
"RANKCTL" on page 694	0x10c90	Rank Control Register
"DBICTL" on page 698	0x10c94	DM/DBI Control Register
"ODTMAP" on page 700	0x10c9c	ODT/Rank Map Register
"DATACTL0 " on page 704	0x10ca0	Data Control register 0
"SWCTLSTATIC " on page 706	0x10ca4	Static Registers Write Enable
"CGCTL" on page 707	0x10cb0	External clock gate control register
"INITTMG0" on page 708	0x10d00	SDRAM Initialization Timing Register 0
"PPT2CTRL0" on page 710	0x10f00	PPT2 Control Register
"PPT2STAT0 " on page 712	0x10f10	Status PPT2 Control Register

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"DDRCTL_VER_NUMBER" on page 714	0x10ff8	DDRCTL Version Number Register
"DDRCTL_VER_TYPE" on page 715	0x10ffc	DDRCTL Version Type Register
DDRC Channel 1 Registers REGB_DDRC_CH1 Exists: UMCTL2_DUAL_DATA_CHANNEL==1		
"MSTR4" on page 716	0x11010	Master Register4
"STAT" on page 718	0x11014	Operating Mode Status Register
"MRCTRL0" on page 721	0x11080	Mode Register Read/Write Control Register 0.
"MRCTRL1" on page 725	0x11084	Mode Register Read/Write Control Register 1
"MRSTAT" on page 726	0x11090	Mode Register Read/Write Status Register
"MRRDATA0 " on page 728	0x11094	Mode Register Read Data 0
"MRRDATA1 " on page 729	0x11098	Mode Register Read Data 1
"DERATECTL5" on page 730	0x11114	Temperature Derate Control Register 5
"DERATESTAT0 " on page 732	0x11120	Temperature Derate Status Register 0
"DERATEDBGCTL" on page 733	0x11128	Temperature Derate Debug Contrl Register
"DERATEDBGSTAT " on page 734	0x1112c	Temperature Derate Debug Status Register
"PWRCTL" on page 736	0x11180	Low Power Control Register
"HWLPCTL" on page 740	0x11184	Hardware Low Power Control Register
"ZQCTL1" on page 741	0x11284	ZQ Control Register 1
"ZQSTAT" on page 742	0x1128c	ZQ Status Register
"DQSOSCSTAT0 " on page 743	0x11304	DQS/WCK Oscillator Status Register 0
"HWFFCSTAT" on page 745	0x11404	Hardware Fast Frequency Change (HWFFC) Status Register
"HWFFC_MRWBUF_CTRL0" on page 747	0x11410	Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
"HWFFC_MRWBUF_CTRL1" on page 749	0x11414	Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
"HWFFC_MRWBUF_STAT" on page 750	0x11418	Hardware Fast Frequency Change (HWFFC) MRW buffer status register
"DFISTAT" on page 751	0x11514	DFI Status Register

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"DFI0MSGCTL0" on page 752	0x11520	DFI0 Message Control Register 0.
"DFI0MSGSTAT0 " on page 754	0x11524	DFI0 Message Status Register 0
"DFISBINTRPTCFG" on page 755	0x11528	DFI Sideband Watchdog Timer Interrupt Configuration Register
"DFISBPOISONCFG" on page 757	0x11530	DFI Sideband Watchdog Timer Poison Control Register
"DFISBTIMERSTAT" on page 761	0x11538	DFI Sideband Watchdog Timer Status Register
"DFISBTIMERSTAT1 " on page 763	0x11540	DFI Sideband Watchdog Timer Status Register 1
"DFIERRINTRPTCFG" on page 764	0x11548	DFI Error Interface Interrupt Configuration Register
"DFIERRORSTAT" on page 766	0x11550	DFI Error Interface Status Register
"DFIERRORSTAT1 " on page 767	0x11558	DFI Error Interface Status Register 1
"ECCSTAT" on page 768	0x11608	SECDED ECC Status Register
"ECCCTL" on page 770	0x1160c	ECC Clear Register
"ECCERRCNT" on page 774	0x11610	ECC Error Counter Register
"ECCCADDR0" on page 775	0x11614	ECC Corrected Error Address Register 0
"ECCCADDR1" on page 776	0x11618	ECC Corrected Error Address Register 1
"ECCCSYN0" on page 778	0x1161c	ECC Corrected Syndrome Register 0
"ECCCSYN1" on page 779	0x11620	ECC Corrected Syndrome Register 1
"ECCCSYN2" on page 780	0x11624	ECC Corrected Syndrome Register 2
"ECCBITMASK0" on page 782	0x11628	ECC Corrected Data Bit Mask Register 0
"ECCBITMASK1" on page 783	0x1162c	ECC Corrected Data Bit Mask Register 1
"ECCBITMASK2" on page 784	0x11630	ECC Corrected Data Bit Mask Register 2
"ECCUADDR0" on page 785	0x11634	ECC Uncorrected Error Address Register 0
"ECCUADDR1" on page 786	0x11638	ECC Uncorrected Error Address Register 1
"ECCUSYN0" on page 788	0x1163c	ECC Uncorrected Syndrome Register 0
"ECCUSYN1" on page 789	0x11640	ECC Uncorrected Syndrome Register 1
"ECCUSYN2" on page 790	0x11644	ECC Uncorrected Syndrome Register 2

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"ECCAPSTAT" on page 792	0x11664	Address protection within ECC Status Register
"OCPARCFG0" on page 793	0x11680	On-Chip Parity Configuration Register 0
"OCPARSTAT2 " on page 795	0x11690	On-Chip Parity Status Register 2
"OCCAPCFG1" on page 796	0x11788	On-Chip command/Address Protection Configuration Register 1
"OCCAPSTAT1 " on page 800	0x1178c	On-Chip command/Address Protection Status Register 1
"OCCAPCFG2" on page 803	0x11790	On-Chip command/Address Protection Configuration Register 2
"OCCAPSTAT2 " on page 804	0x11794	On-Chip command/Address Protection Status Register 2
"LNKECCCTL1" on page 805	0x11984	Link-ECC Control Register 1
"LNKECCPOISONCTL0" on page 807	0x11988	Link-ECC Poison Control Register 0
"LNKECCPOISONSTAT" on page 809	0x1198c	Link-ECC Poison Status Register
"LNKECCINDEX" on page 810	0x11990	Link-ECC Index Register
"LNKECCERRCNT0" on page 811	0x11994	Link-ECC Error Status Register 0
"LNKECCERRSTAT" on page 812	0x11998	Link-ECC Error Status Register 1
"LNKECCCADDR0" on page 813	0x119e0	Link ECC Corrected Error Address Register 0
"LNKECCCADDR1" on page 814	0x119e4	Link ECC Corrected Error Address Register 1
"LNKECCUADDR0" on page 816	0x119e8	Link ECC Uncorrected Error Address Register 0
"LNKECCUADDR1" on page 817	0x119ec	Link ECC Uncorrected Error Address Register 1
"OPCTRL1" on page 819	0x11b84	Operation Control Register 1
"OPCTRLCAM" on page 820	0x11b88	CAM Operation Control Register
"OPCTRLCMD" on page 823	0x11b8c	Command Operation Control Register
"OPCTRLSTAT" on page 825	0x11b90	Status Operation Control Register
"OPCTRLCAM1" on page 827	0x11b94	CAM Operation Control Register 1

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"OPREFCTRL0" on page 828	0x11b98	Refresh Operation Control Register 0
"OPREFCTRL1" on page 840	0x11b9c	Refresh Operation Control Register 1
"OPREFSTAT0 " on page 852	0x11ba0	Refresh Operation Status Register 0
"OPREFSTAT1 " on page 864	0x11ba4	Refresh Operation Status Register 1
"DBICTL" on page 876	0x11c94	DM/DBI Control Register
"ODTMAP" on page 878	0x11c9c	ODT/Rank Map Register
"INITTMG0" on page 882	0x11d00	SDRAM Initialization Timing Register 0
Arbiter Port p Registers REGB_ARB_PORTp (for p = 0; p <= 15) Exists: UMCTL2_A_NPORTS>p && DDRCTL_ARB_OR_CHB_OR_HIF_SBR_EN_1==1		
"PCCFG" on page 884	0x20000+p*0x1000	Port Common Configuration Register.
"PCFGR" on page 885	0x20004+p*0x1000	Configuration Read Register
"PCFGW" on page 888	0x20008+p*0x1000	Configuration Write Register
"PCFGIDMASKCHc(for c = 0; c <= 15)" on page 891	0x20010+p*0x1000+c*0x8	Channel 0 Configuration ID mask register
"PCFGIDVALUECHc (for c = 0; c <= 15)" on page 892	0x20014+p*0x1000+c*0x8	Channel 0 Configuration ID value register
"PCTRL" on page 893	0x20090+p*0x1000	Port Control Register
"PCFGQOS0" on page 894	0x20094+p*0x1000	Port n Read QoS Configuration Register 0
"PCFGQOS1" on page 897	0x20098+p*0x1000	Port n Read QoS Configuration Register 1
"PCFGWQOS0" on page 898	0x2009c+p*0x1000	Port n Write QoS Configuration Register 0
"PCFGWQOS1" on page 900	0x200a0+p*0x1000	Port n Write QoS Configuration Register 1
"SARBASEs(for s = 0; s <= 3)" on page 901	0x200c0+p*0x1000+s*0x8	SAR Base Address Register 0.
"SARSIZEs(for s = 0; s <= 3)" on page 902	0x200c4+p*0x1000+s*0x8	SAR Size Register 0.
"SBRCTL" on page 903	0x200e0+p*0x1000	Scrubber Control Register
"SBRSTAT" on page 908	0x200e4+p*0x1000	Scrubber Status Register
"SBRWDATA0 " on page 910	0x200e8+p*0x1000	Scrubber Write Data Pattern0
"SBRWDATA1 " on page 911	0x200ec+p*0x1000	Scrubber Write Data Pattern1
"SBRSTART0" on page 912	0x200f0+p*0x1000	Scrubber Start Address Mask Register 0

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"SBRSTART1" on page 913	0x200f4+p*0x1000	Scrubber Start Address Mask Register 1
"SBRRANGE0" on page 914	0x200f8+p*0x1000	Scrubber Address Range Mask Register 0
"SBRRANGE1" on page 915	0x200fc+p*0x1000	Scrubber Address Range Mask Register 1
"SBRSTART0DCH1" on page 916	0x20100+p*0x1000	Scrubber Start Address Mask Register 0 for Data Channel 1
"SBRSTART1DCH1" on page 917	0x20104+p*0x1000	Scrubber Start Address Mask Register 1 for Data Channel 1
"SBRRANGE0DCH1" on page 918	0x20108+p*0x1000	Scrubber Address Range Mask Register 0 for Data Channel 1
"SBRRANGE1DCH1" on page 919	0x2010c+p*0x1000	Scrubber Address Range Mask Register 1 for Data Channel 1
"PDCH" on page 920	0x20110+p*0x1000	Port Data Channel
"PSTAT" on page 924	0x20114+p*0x1000	Port Status Register
Address Map 0 Registers REGB_ADDR_MAP0 Exists: Always		
"ADDRMAP0" on page 928	0x30000	Address Map Register 0
"ADDRMAP1" on page 929	0x30004	Address Map Register 1
"ADDRMAP3" on page 931	0x3000c	Address Map Register 3
"ADDRMAP4" on page 933	0x30010	Address Map Register 4
"ADDRMAP5" on page 935	0x30014	Address Map Register 5
"ADDRMAP6" on page 939	0x30018	Address Map Register 6
"ADDRMAP7" on page 941	0x3001c	Address Map Register 7
"ADDRMAP8" on page 943	0x30020	Address Map Register 8
"ADDRMAP9" on page 945	0x30024	Address Map Register 9
"ADDRMAP10" on page 947	0x30028	Address Map Register 10
"ADDRMAP11" on page 949	0x3002c	Address Map Register 11
"ADDRMAP12" on page 950	0x30030	Address Map Register 12
"ADDRMAPLUTCFG" on page 953	0x30080	Addr CS map LUT config register
"ADDRMAPLUTCTRL" on page 955	0x30084	Addr CS map LUT control register

Table 3-4 Registers for the DWC_ddrctl_map Memory Map (continued)

Register	Offset	Description
"ADDRMAPLUTRDATA" on page 957	0x30088	Addr CS map LUT read data register

3.1 REGB_FREQf_CHc Registers

This register block contains registers related to timings in the DDRC controller. Registers shared by all blocks are only duplicated for every channel, hence they only reside in REGB_FREQ0_CHc.

3.1.1 DRAMSET1TMG0

- **Name:** SDRAM Timing Register 0 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 0 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x0+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

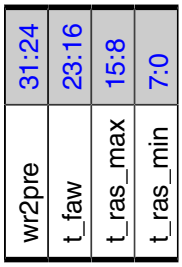


Table 3-5 Fields for Register: DRAMSET1TMG0

Bits	Name	Memory Access	Description
31:24	wr2pre	R/W	Minimum time between write and precharge to same bank. ■ DDR4: WL + BL/2 + tWR ■ DDR5: CWL + WBL/2 + tWR ■ LPDDR4: WL + BL/2 + tWR + 1 ■ LPDDR5(16B mode): WL + BL/n + tWR + 1 ■ LPDDR5(BG mode) : WL + BL/n_min + tWR + 1 Where: ■ WL = write latency ■ BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. ■ WBL = Write burst length associated with Write command. ■ tWR = Write recovery time. This comes directly from the SDRAM specification. For DDR5, the round-up value of tRx_DQS2DQ need to be added. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
23:16	t_faw	R/W	tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. **Value After Reset:** 0x10 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	t_ras_max	R/W	tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open. t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Note: This field is not used for DDR5. Unit: 1024 DRAM clock cycles. **Value After Reset:** 0x1b **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-5 Fields for Register: DRAMSET1TMG0 (continued)

Bits	Name	Memory Access	Description
7:0	t_ras_min	R/W	tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.2 DRAMSET1TMG1

- **Name:** SDRAM Timing Register 1 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 1 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x4+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

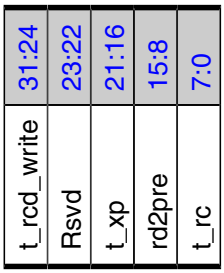


Table 3-6 Fields for Register: DRAMSET1TMG1

Bits	Name	Memory Access	Description
31:24	t_rcd_write	R/W	tRCD: Minimum time from activate to write command to the same bank in LPDDR5X mode. Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
23:22			**Reserved Field:** Yes

Table 3-6 Fields for Register: DRAMSET1TMG1 (continued)

Bits	Name	Memory Access	Description
21:16	t_xp	R/W	tXP: Minimum time after power-down exit to any operation. ■ DDR4 (C/A parity not enabled): tXP ■ DDR4 (C/A parity enabled): (tXP+PL) ■ DDR5: tXP ■ DDR5 (L)RDIMM: max (tXP, tRPDX) ■ LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. ■ LPDDR4 (tCKELPD is not defined in spec): tXP. ■ LPDDR5 (MR17.OP[4] ODTD-CS is enabled): max (tXP, tPDXCSODTON) ■ LPDDR5 (MR17.OP[4] ODTD-CS is disabled): tXP Unit: DRAM clock cycles. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	rd2pre	R/W	tRTP: Minimum time from read to precharge of same bank. ■ DDR4: Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). ■ DDR5: tRTP ■ LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 ■ LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) ■ LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
7:0	t_rc	R/W	tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. **Value After Reset:** 0x14 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.3 DRAMSET1TMG2

- **Name:** SDRAM Timing Register 2 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 2 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x8+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

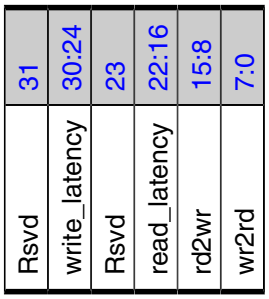


Table 3-7 Fields for Register: DRAMSET1TMG2

Bits	Name	Memory Access	Description
31			**Reserved Field:** Yes
30:24	write_latency	R/W	Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. **Value After Reset:** 0x3 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
23			**Reserved Field:** Yes

Table 3-7 Fields for Register: DRAMSET1TMG2 (continued)

Bits	Name	Memory Access	Description
22:16	read_latency	R/W	Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. In addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
15:8	rd2wr	R/W	Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. ■ DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL ■ DDR5: CL - CWL + RBL/2 + 2 - (Read DQS offset) + (RD_POSTAMBLE-0.5) + WR_PREAMBLE ■ LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - WDQS_on + 2 ■ LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 6 ■ LPDDR5(BG mode): tRTW for same/different banks in same bank group ■ LPDDR5(16B mode): tRTW for 16B mode Where: ■ WL = write latency ■ BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM ■ RBL = Read burst length associated with Read command ■ RL = read latency = CAS latency ■ WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). ■ RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). ■ tRTW = Read to Write timing. This comes directly from the SDRAM specification.

Table 3-7 Fields for Register: DRAMSET1TMG2 (continued)

Bits	Name	Memory Access	Description
			For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. **Value After Reset:** 0x6 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
7:0	wr2rd	R/W	DDR4: minimum time from write command to read command for same bank group. DDR5/LPDDR4/LPDDR5: minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. ■ DDR4: CWL + PL + BL/2 + tWTR_L ■ DDR5: CWL + WBL/2 + tWTR_L ■ LPDDR4: WL + BL/2 + tWTR + 1 ■ LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) ■ LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) Where: ■ CWL = CAS write latency ■ WL = Write latency ■ PL = Parity latency ■ BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM ■ WBL = Write burst length associated with Write command ■ tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. ■ tWTR = internal write to read command delay. This comes directly from the SDRAM specification. For LPDDR4, add one extra cycle. For DDR4, WTR_L must be increased by one if 2tCK write preamble is used. For DDR5, the round-up value of tRx_DQS2DQ need to be added. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation.

Table 3-7 Fields for Register: DRAMSET1TMG2 (continued)

Bits	Name	Memory Access	Description
			Unit: DRAM clock cycles. **Value After Reset:** 0xd **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

3.1.4 DRAMSET1TMG3

- **Name:** SDRAM Timing Register 3 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 3 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xc+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

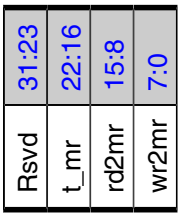


Table 3-8 Fields for Register: DRAMSET1TMG3

Bits	Name	Memory Access	Description
31:23			**Reserved Field:** Yes
22:16	t_mr	R/W	Time from MRW/MRS/VrefCA/VrefCS to valid command. ■ DDR4: Set this to the larger of tMOD + AL and tMRD. If C/A parity is enabled, tMOD_PAR(tMOD+PL) + AL and tMRD_PAR(tMOD+PL) and used instead. If CAL mode is enabled, tCAL must be added to the above. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2. ■ DDR5: Set this to the larger of tMRR, tMRW, tMRWPD, tMRD, tMPC_DELAY, tVrefCA_Delay and tVrefCS_Delay. ■ LPDDR4:Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. ■ LPDDR5:Set this to the larger of (tMRR + tMRW) and tMRD. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-8 Fields for Register: DRAMSET1TMG3 (continued)

Bits	Name	Memory Access	Description
15:8	rd2mr	R/W	Time from Read to MRW/MRR command. ■ LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 ■ LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:0	wr2mr	R/W	Time from Write to MRW/MRR command. ■ LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR ■ LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.5 DRAMSET1TMG4

- **Name:** SDRAM Timing Register 4 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 4 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

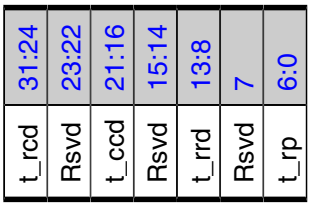


Table 3-9 Fields for Register: DRAMSET1TMG4

Bits	Name	Memory Access	Description
31:24	t_rcd	R/W	DDR4: Minimum time from activate to read or write command to the same bank. DDR5/LPDDR4/LPDDR5: Minimum time from activate to read or write or masked write command to the same bank. LPDDR5X: Minimum time from activate to read or masked write command to the same bank. ■ DDR4: tRCD-tAL ■ DDR5: tRCD For DDR5 2N mode, it is recommended to set this value as multiple of MEMC_FREQ_RATIO to improve the performance. Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
23:22			**Reserved Field:** Yes

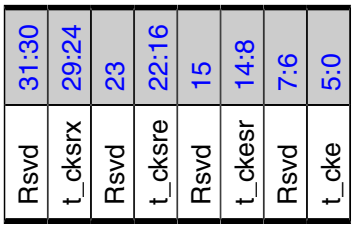
Table 3-9 Fields for Register: DRAMSET1TMG4 (continued)

Bits	Name	Memory Access	Description
21:16	t_ccd	R/W	This is the minimum time between two reads or two writes. ■ DDR4: tCCD_L ■ LPDDR4: tCCD ■ LPDDR5: BL/n Don't Care for DDR5 (see DRAMSET1TMG26.t_ccd_r/t_ccd_w in DDR5). Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:14			**Reserved Field:** Yes
13:8	t_rrd	R/W	DDR4/DDR5/LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". ■ DDR4/5: tRRD_L ■ LPDDR4: RU(tRRD/tCK) ■ LPDDR5(BG mode): RU(tRRD_L/tCK) ■ LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7			**Reserved Field:** Yes
6:0	t_rp	R/W	tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.6 DRAMSET1TMG5

- **Name:** SDRAM Timing Register 5 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 5 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x14+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:30	29:24	23	22:16	15	14:8	7:6	5:0
Rsvd	t_cksrx	Rsvd	t_cksre	Rsvd	t_ckesr	Rsvd	t_cke

Table 3-10 Fields for Register: DRAMSET1TMG5

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:24	t_cksrx	R/W	This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: ■ LPDDR4: tCKCKEH ■ LPDDR5: tCKCSH ■ DDR4: tCKSRX ■ DDR5: tCKSRX Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
23			**Reserved Field:** Yes

Table 3-10 Fields for Register: DRAMSET1TMG5 (continued)

Bits	Name	Memory Access	Description
22:16	t_cksre	R/W	This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: ■ LPDDR4: tCKELCK ■ LPDDR5: tCSLCK ■ DDR4: tCKSRE (+ PL(parity latency)(*)) ■ DDR5: tCKLCS (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15			**Reserved Field:** Yes
14:8	t_ckesr	R/W	Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: ■ LPDDR4: max(tCKE, tSR) ■ LPDDR5: tSR ■ DDR4: tCKESR (+ PL(parity latency)(*)) ■ DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:6			**Reserved Field:** Yes
5:0	t_cke	R/W	Delay time between PDE and PDX. ■ LPDDR4: tCKE ■ LPDDR5: tCSPD ■ DDR4: tPD (+ PL(parity latency)(*)) ■ DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. **Value After Reset:** 0x3 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.7 DRAMSET1TMG6

- **Name:** SDRAM Timing Register 6 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 6 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x18+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories

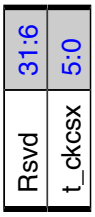


Table 3-11 Fields for Register: DRAMSET1TMG6

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:0	t_ckcsx	R/W	This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: ■ LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.8 DRAMSET1TMG7

- **Name:** SDRAM Timing Register 7 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 7 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories

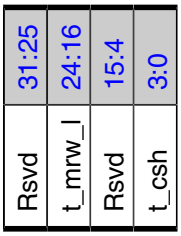


Table 3-12 Fields for Register: DRAMSET1TMG7

Bits	Name	Memory Access	Description
31:25			**Reserved Field:** Yes
24:16	t_mrw_l	R/W	Stretched MODE Register Write command period ■ LPDDR5: tMRW_L Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:4			**Reserved Field:** Yes
3:0	t_csh	R/W	CS High Pulse width at PDX ■ LPDDR5: tCSH Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.9 DRAMSET1TMG9

- **Name:** SDRAM Timing Register 9 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 9 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x24+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

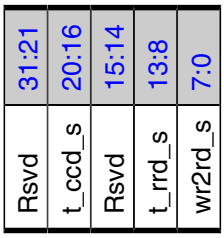


Table 3-13 Fields for Register: DRAMSET1TMG9

Bits	Name	Memory Access	Description
31:21			**Reserved Field:** Yes
20:16	t_ccd_s	R/W	tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting DDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:14			**Reserved Field:** Yes
13:8	t_rrd_s	R/W	tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-13 Fields for Register: DRAMSET1TMG9 (continued)

Bits	Name	Memory Access	Description
7:0	wr2rd_s	R/W	Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. ■ DDR4: CWL + PL + BL/2 + tWTR_S ■ DDR5: CWL + WBL/2 + tWTR_S ■ LPDDR5: WL + BL/n_min + RU(tWTR_S/tCK) Where: ■ CWL = CAS write latency ■ PL = Parity latency ■ BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM ■ WBL = Write burst length associated with Write command ■ tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. ■ WL = Write Latency ■ BL/n_min = Effective Burst Length For DDR4, WTR_S must be increased by one if 2tCK write preamble is used. For DDR5, the round-up value of tRx_DQS2DQ need to be added. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0xd **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

3.1.10 DRAMSET1TMG12

- **Name:** SDRAM Timing Register 12 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 12 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

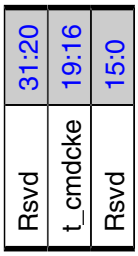


Table 3-14 Fields for Register: DRAMSET1TMG12

Bits	Name	Memory Access	Description
31:20			**Reserved Field:** Yes
19:16	t_cmdcke	R/W	tCMDCKE: Delay from valid command to PDE ■ LPDDR4: max(tESCKE, tCMDCKE) ■ LPDDR5: max(tESPD, tCMDPD) Unit: DRAM clock cycles. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:0			**Reserved Field:** Yes

3.1.11 DRAMSET1TMG13

- **Name:** SDRAM Timing Register 13 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 13 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x34+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

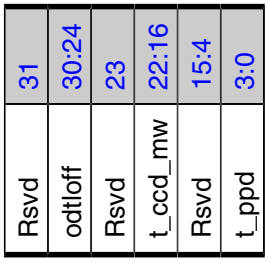


Table 3-15 Fields for Register: DRAMSET1TMG13

Bits	Name	Memory Access	Description
31			**Reserved Field:** Yes
30:24	odtloff	R/W	LPDDR4: ODTLoff: This is the latency from CAS-2 command to tODToff reference. LPDDR5: ODTLoff: This is the latency from the Write or Mask Write command (the rising edge of the clock) to tODToff reference. Unit: DRAM clock cycles. **Value After Reset:** 0x1c **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
23			**Reserved Field:** Yes
22:16	t_ccd_mw	R/W	This is the minimum time from write or masked write to masked write command for same bank. ■ LPDDR4: tCCDMW ■ LPDDR5(BG mode): 4*BL/n_max ■ LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x20 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-15 Fields for Register: DRAMSET1TMG13 (continued)

Bits	Name	Memory Access	Description
15:4			**Reserved Field:** Yes
3:0	t_ppd	R/W	LPDDR4/5 and DDR5: tPPD: This is the minimum time from precharge to precharge command. Note: This register is not applicable for DDR4 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.12 DRAMSET1TMG14

- **Name:** SDRAM Timing Register 14 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 14 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x38+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

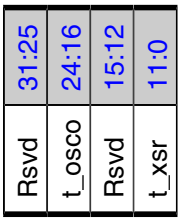


Table 3-16 Fields for Register: DRAMSET1TMG14

Bits	Name	Memory Access	Description
31:25			**Reserved Field:** Yes
24:16	t_osco	R/W	Minimum time from DQS Oscillator (LPDDR4) or WCK2DQI/WCK2DQO Oscillator(LPDDR5) stop to Mode register readout. LPDDR4 : tOSCO = max(40ns,8nCK) LPDDR5 : tOSCODQI = tOSCODQO = max(40ns,8nCK) Unit: DRAM clock cycles. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:12			**Reserved Field:** Yes
11:0	t_xsr	R/W	tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. **Value After Reset:** 0xa0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.13 DRAMSET1TMG17

- **Name:** SDRAM Timing Register 17 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 17 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x44+f*0x100000+c*0x1000
- **Exists:** UMCTL2_HWFFC_EN==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

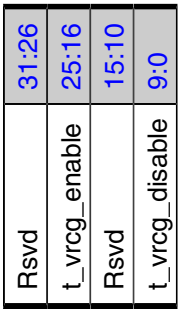


Table 3-17 Fields for Register: DRAMSET1TMG17

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25:16	t_vrcg_enable	R/W	LPDDR4: tVRCG_ENABLE: VREF high current mode enable time. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
15:10			**Reserved Field:** Yes
9:0	t_vrcg_disable	R/W	LPDDR4: tVRCG_DISABLE: VREF high current mode disable time. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

3.1.14 DRAMSET1TMG23

- **Name:** SDRAM Timing Register 23 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 23 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

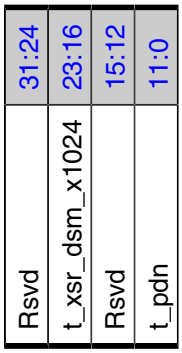


Table 3-18 Fields for Register: DRAMSET1TMG23

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	t_xsr_dsm_x1024	R/W	Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
15:12			**Reserved Field:** Yes
11:0	t_pdn	R/W	Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related

3.1.15 DRAMSET1TMG24

- **Name:** SDRAM Timing Register 24 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 24 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x60+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

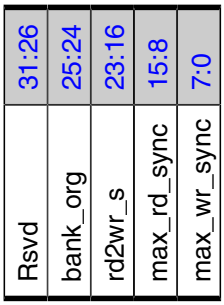


Table 3-19 Fields for Register: DRAMSET1TMG24

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25:24	bank_org	R/W	Select Bank/ Bank group organization: ■ 00: 4 Banks/ 4 Bank groups ■ 01: 8 Banks (Reserved) ■ 10: 16 Banks ■ 11: Reserved **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

Table 3-19 Fields for Register: DRAMSET1TMG24 (continued)

Bits	Name	Memory Access	Description
23:16	rd2wr_s	R/W	Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. ■ LPDDR5(BG mdoe): tRTW for different banks in different bank group where: ■ tRTW = Read to Write timing. This comes directly from the SDRAM specification. Note: This register field is only applicable for LPDDR5 BG mode. Unit: DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
15:8	max_rd_sync	R/W	Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RD(tWCKPST/tCK) Unit: DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
7:0	max_wr_sync	R/W	Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max + RD(tWCKPST/tCK) Unit: DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

3.1.16 DRAMSET1TMG25

- **Name:** SDRAM Timing Register 25 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 25 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x64+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

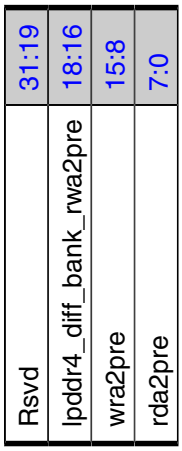


Table 3-20 Fields for Register: DRAMSET1TMG25

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18:16	lpddr4_diff_bank_rwa2pre	R/W	Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. ■ LPDDR4 JESD209-4A requires 4 cycles ■ LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

Table 3-20 Fields for Register: DRAMSET1TMG25 (continued)

Bits	Name	Memory Access	Description
15:8	wra2pre	R/W	Time between write with AP and precharge to same bank. ■ LPDDR4: WL + BL/2 + nWR + 1 ■ LPDDR5: WL + BL/n_min + nWR + 1 ■ DDR4: WL + BL/2 + WR Don't care for DDR5. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4
7:0	rda2pre	R/W	Time between read with AP and precharge to same bank. ■ LPDDR4: nRTP ■ LPDDR5: BL/n_min + nRBTP ■ DDR4: RTP Don't care for DDR5. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

3.1.17 DRAMSET1TMG30

- **Name:** SDRAM Timing Register 30 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 30 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x78+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

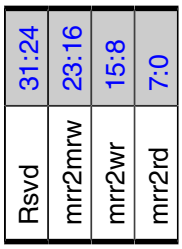


Table 3-21 Fields for Register: DRAMSET1TMG30

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	mrr2mrw	R/W	MRR to MRW delay Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	mrr2wr	R/W	MRR to WR delay Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:0	mrr2rd	R/W	MRR to RD delay Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.18 DRAMSET1TMG32

- **Name:** SDRAM Timing Register 32 belonging to Timing Set 1
- **Description:** SDRAM Timing Register 32 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x80+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1 && MEMC_NUM_RANKS_GT_1==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

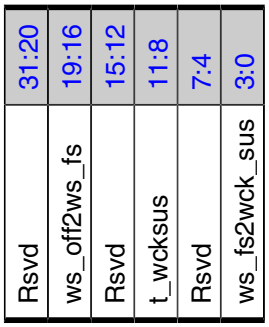


Table 3-22 Fields for Register: DRAMSET1TMG32

Bits	Name	Memory Access	Description
31:20			**Reserved Field:** Yes
19:16	ws_off2ws_fs	R/W	Delay from CAS-WS_OFF to next CAS_WS-FS command. Unit: DRAM clock cycles. **Value After Reset:** 0x3 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:12			**Reserved Field:** Yes
11:8	t_wcksus	R/W	tWCKSUS: Delay from CAS-WCK_SUSPEND command to next READ/WRITE/MASK WRITE command. Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:4			**Reserved Field:** Yes

Table 3-22 Fields for Register: DRAMSET1TMG32 (continued)

Bits	Name	Memory Access	Description
3:0	ws_fs2wck_sus	R/W	Delay from CAS-WS_FS command to next CAS-WCK_SUSPEND command. Unit: DRAM clock cycles. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.19 DRAMSET1TMG34

- **Description:** SDRAM Timing Register 34 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x88+f*0x100000+c*0x1000
- **Exists:** DDRCTL_BURST_LENGTH_X2==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting BL32 and LPDDR4/LPDDR5 SDRAM memories

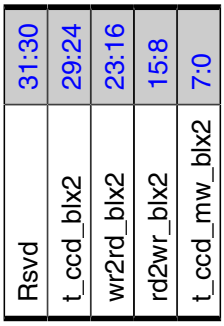


Table 3-23 Fields for Register: DRAMSET1TMG34

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:24	t_ccd_blx2	R/W	This is the minimum time from BL32 read to read or from BL32 write to write command. ■ LPDDR4 : tCCD ■ LPDDR5 : BL/n Unit: DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-23 Fields for Register: DRAMSET1TMG34 (continued)

Bits	Name	Memory Access	Description
23:16	wr2rd_blx2	R/W	This is the minimum time from BL32 write to read command. ■ LPDDR4 : WL + BL/2 + tWTR + 1 ■ LPDDR5(BG mode) : WL + BL/n_max + RU(tWTR_L/tCK) ■ LPDDR5(16B mode) : WL + BL/n + RU(tWTR/tCK) Where: ■ WL : write latency ■ BL : burst length. ■ tWTR_L : internal write to read command delay for same bank group. This comes directly from the SDRAM specification ■ tWTR : internal write to read command delay. This comes directly from the SDRAM specification Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	rd2wr_blx2	R/W	This is the minimum time from BL32 read to write or mask write command. ■ LPDDR4(DQ ODT is disabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL ■ LPDDR4(DQ ODT is enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 ■ LPDDR5 : tRTW Where: ■ WL : read latency ■ WL : write latency ■ BL : burst length. ■ tWTR_L : internal write to read command delay for same bank group. This comes directly from the SDRAM specification ■ tWTR : internal write to read command delay. This comes directly from the SDRAM specification ■ WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). ■ RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-23 Fields for Register: DRAMSET1TMG34 (continued)

Bits	Name	Memory Access	Description
7:0	t_ccd_mw_blx2	R/W	This is the minimum time from BL32 write to mask write command for same bank. ■ LPDDR4: tCCDMW + 8 ■ LPDDR5(BG mode): 2.5*BL/n_max ■ LPDDR5(16B mode): 2.5*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.20 DRAMSET1TMG35

- **Description:** SDRAM Timing Register 35 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x8c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_BURST_LENGTH_X2==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting BL32 and LPDDR4/LPDDR5 SDRAM memories

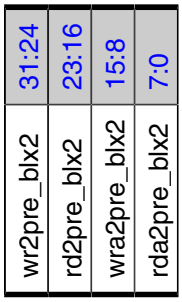


Table 3-24 Fields for Register: DRAMSET1TMG35

Bits	Name	Memory Access	Description
31:24	wr2pre_blx2	R/W	This is the minimum time from BL32 write to precharge of same bank. ■ LPDDR4 : WL + 1 + BL/2 + RU(tWR/tCK) ■ LPDDR5(BG mode): WL + BL/n_min + 1 + RU(tWR/tCK) ■ LPDDR5(16B mode): WL + BL/n + 1 + RU(tWR/tCK) Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
23:16	rd2pre_blx2	R/W	This is the minimum time from BL32 read to precharge of same bank. ■ LPDDR4 : BL/2 + max(RoundUp(tRTP/tCK),8) - 8 ■ LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) ■ LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-24 Fields for Register: DRAMSET1TMG35 (continued)

Bits	Name	Memory Access	Description
15:8	wra2pre_blx2	R/W	This is the minimum time from BL32 write with AP to precharge for same bank. ■ LPDDR4: WL + BL/2 + nWR + 1 ■ LPDDR5(BG mode): WL + BL/n_min + nWR + 1 ■ LPDDR5(16B mode): WL + BL/n + nWR + 1 Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:0	rda2pre_blx2	R/W	This is the minimum time from BL32 read with AP to precharge command for same bank. ■ LPDDR4: nRTP + 8 ■ LPDDR5(BG mode): BL/n_min + nRBTP ■ LPDDR5(16B mode): BL/n + nRBTP Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.21 DRAMSET1TMG36

- **Description:** SDRAM Timing Register 36 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x90+f*0x100000+c*0x1000
- **Exists:** DDRCTL_BURST_LENGTH_X2==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting BL32 and LPDDR4/LPDDR5 SDRAM memories

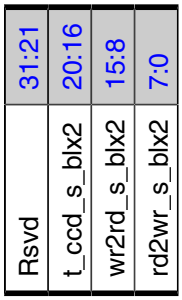


Table 3-25 Fields for Register: DRAMSET1TMG36

Bits	Name	Memory Access	Description
31:21			**Reserved Field:** Yes
20:16	t_ccd_s_blx2	R/W	This is the minimum time from BL32 read to read or from BL32 write to write for different bank group. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	wr2rd_s_blx2	R/W	This is the minimum time from BL32 write to read command for different bank group. ■ LPDDR5(BG mode) : WL + BL/n_max + RU(tWTR_S/tCK) Where: ■ WL : write latency ■ tWTR_S : internal write to read command delay for same bank group. This comes directly from the SDRAM specification Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-25 Fields for Register: DRAMSET1TMG36 (continued)

Bits	Name	Memory Access	Description
7:0	rd2wr_s_blx2	R/W	This is the minimum time from BL32 read to write command for same bank. Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.22 DRAMSET1TMG37

- **Description:** SDRAM Timing Register 37 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x94+f*0x100000+c*0x1000
- **Exists:** DDRCTL_BURST_LENGTH_X2==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting BL32 and LPDDR4/LPDDR5 SDRAM memories

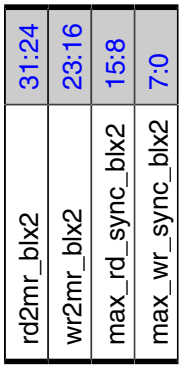


Table 3-26 Fields for Register: DRAMSET1TMG37

Bits	Name	Memory Access	Description
31:24	rd2mr_blx2	R/W	Minimum time from BL32 read to MRW/MRR command. ■ LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 ■ LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
23:16	wr2mr_blx2	R/W	Minimum time from BL32 write command to MRW/MRR command. ■ LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR ■ LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-26 Fields for Register: DRAMSET1TMG37 (continued)

Bits	Name	Memory Access	Description
15:8	max_rd_sync_blx2	R/W	Minimum time from BL32 read command to WCK2CK sync OFF. RL + BL/n_max + RD(tWCKPST/tCK) Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:0	max_wr_sync_blx2	R/W	Minimum time from BL32 write command to WCK2CK sync OFF. WL + BL/n_max + RD(tWCKPST/tCK) Note: This register field is only applicable for designs supporting LPDDR5 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.23 DRAMSET1TMG38

- **Description:** SDRAM Timing Register 38 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x90+f*0x100000+c*0x1000
- **Exists:** DDRCTL_BURST_LENGTH_X2==1 && MEMC_NUM_RANKS>1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting BL32 and LPDDR4/LPDDR5 SDRAM memories

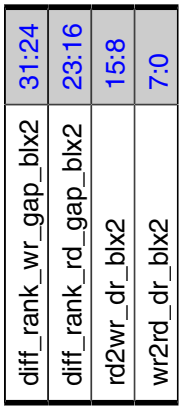


Table 3-27 Fields for Register: DRAMSET1TMG38

Bits	Name	Memory Access	Description
31:24	diff_rank_wr_gap_blx2	R/W	Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. ■ PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ■ ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap_blx2 must be a minimum of ODTLoff - ODTLon - BL/2 + 1 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation.

Table 3-27 Fields for Register: DRAMSET1TMG38 (continued)

Bits	Name	Memory Access	Description
			For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
23:16	diff_rank_rd_gap_blx2	R/W	Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. ■ PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) If read postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ■ ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads. Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:8	rd2wr_dr_blx2	R/W	Minimum time from BL32 read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-27 Fields for Register: DRAMSET1TMG38 (continued)

Bits	Name	Memory Access	Description
7:0	wr2rd_dr_blx2	R/W	Minimum time from BL32 write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.24 INITMR0

- **Name:** SDRAM Initialization MR Setting Register 0
- **Description:** SDRAM Initialization MR Setting Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x500+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

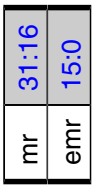


Table 3-28 Fields for Register: INITMR0

Bits	Name	Memory Access	Description
31:16	mr	R/W	■ DDR4: Value loaded into MR0 register. ■ DDR5: Don't care ■ LPDDR4: Value to write to MR1 register ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
15:0	emr	R/W	■ DDR4: Value to write to MR1 register Set bit 7 to 0. ■ DDR5: Don't care ■ LPDDR4: Value to write to MR2 register ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x510 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

3.1.25 INITMR1

- **Name:** SDRAM Initialization MR Setting Register 1
- **Description:** SDRAM Initialization MR Setting Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x504+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

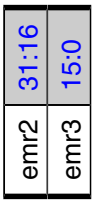


Table 3-29 Fields for Register: INITMR1

Bits	Name	Memory Access	Description
31:16	emr2	R/W	■ DDR4: Value to write to MR2 register ■ DDR5: Don't care ■ LPDDR4: Value to write to MR3 register ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
15:0	emr3	R/W	■ DDR4: Value to write to MR3 register ■ DDR5: Don't care ■ LPDDR4: Value to write to MR13 register ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.26 INITMR2

- **Name:** SDRAM Initialization MR Setting Register 2
- **Description:** SDRAM Initialization MR Setting Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x508+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

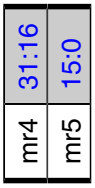


Table 3-30 Fields for Register: INITMR2

Bits	Name	Memory Access	Description
31:16	mr4	R/W	■ DDR4: Value to be loaded into SDRAM MR4 registers. ■ DDR5: Don't care ■ LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed) ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15:0	mr5	R/W	■ DDR4: Value to be loaded into SDRAM MR5 registers. ■ DDR5: Don't care ■ LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed) ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

3.1.27 INITMR3

- **Name:** SDRAM Initialization MR Setting Register 3
- **Description:** SDRAM Initialization MR Setting Register 3
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x50c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

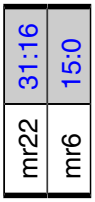


Table 3-31 Fields for Register: INITMR3

Bits	Name	Memory Access	Description
31:16	mr22	R/W	■ LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed) ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
15:0	mr6	R/W	■ DDR4 Value to be loaded into SDRAM MR6 registers. ■ DDR5: Don't care ■ LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed) ■ LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send MRW commands to initialize MR in the SDRAM even if INITTMG0.skip_dram_init=0) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

3.1.28 DFITMG0

- **Name:** DFI Timing Register 0
- **Description:** DFI Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x580+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

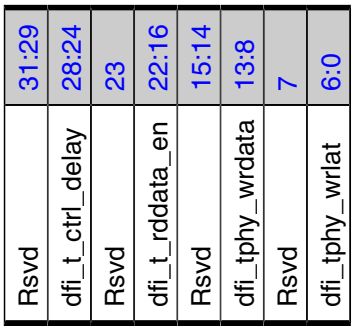


Table 3-32 Fields for Register: DFITMG0

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	dfi_t_ctrl_delay	R/W	Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. **Value After Reset:** 0x7 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
23			**Reserved Field:** Yes

Table 3-32 Fields for Register: DFITMG0 (continued)

Bits	Name	Memory Access	Description
22:16	dfi_t_rddata_en	R/W	Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For DDR5 2N mode, this register is adjusted to use the DFI timing (trddata_en-1). Unit: DFI data clock cycles. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
15:14			**Reserved Field:** Yes
13:8	dfi_tphy_wrdata	R/W	Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DFI data clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
7			**Reserved Field:** Yes
6:0	dfi_tphy_wrlat	R/W	Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For DDR5/4, note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For DDR5 2N mode, this register is adjusted to use the DFI timing (tphy_wrlat-1). For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI data clock cycles. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.29 DFITMG1

- **Name:** DFI Timing Register 1
- **Description:** DFI Timing Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x584+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

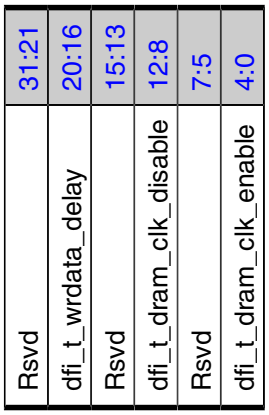


Table 3-33 Fields for Register: DFITMG1

Bits	Name	Memory Access	Description
31:21			**Reserved Field:** Yes
20:16	dfi_t_wrdata_delay	R/W	Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When TMGCFG.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When TMGCFG.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

Table 3-33 Fields for Register: DFITMG1 (continued)

Bits	Name	Memory Access	Description
15:13			**Reserved Field:** Yes
12:8	dfi_t_dram_clk_disable	R/W	Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Note: For SNPS DDR54 PHY, the dfi_t_dram_clk_disable should always be equal to dfi_t_ctrl_delay. Please see the PHY databook. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
7:5			**Reserved Field:** Yes
4:0	dfi_t_dram_clk_enable	R/W	Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Note: For SNPS DDR54 PHY, the dfi_t_dram_clk_enable should always be equal to dfi_t_ctrl_delay. Please see the PHY databook. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

3.1.30 DFITMG2

- **Name:** DFI Timing Register 2
- **Description:** DFI Timing Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x588+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31:22	21:16	15	14:8	7	6:0
Rsvd	dfi_twck_delay	Rsvd	dfi_tphy_rdcslat	Rsvd	dfi_tphy_wrcslat

Table 3-34 Fields for Register: DFITMG2

Bits	Name	Memory Access	Description
31:22			**Reserved Field:** Yes
21:16	dfi_twck_delay	R/W	Number of DFI data clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on the DRAM bus. Refer to PHY specification for correct value. Unit: DFI data clock cycles. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15			**Reserved Field:** Yes

Table 3-34 Fields for Register: DFITMG2 (continued)

Bits	Name	Memory Access	Description
14:8	dfi_tphy_rdcslat	R/W	Number of DFI data clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. For DDR5 2N mode, this register is adjusted to use the DFI timing (tphy_rdcslat-1). Unit: DFI data clock cycles. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7			**Reserved Field:** Yes
6:0	dfi_tphy_wrcslat	R/W	Number of DFI data clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. For DDR5 2N mode, this register is adjusted to use the DFI timing (tphy_wrcslat-1). Unit: DFI data clock cycles. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.31 DFITMG4

- **Name:** DFI Timing Register 4
- **Description:** DFI Timing Register 4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x590+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

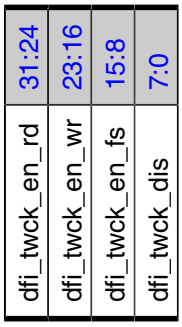


Table 3-35 Fields for Register: DFITMG4

Bits	Name	Memory Access	Description
31:24	dfi_twck_en_rd	R/W	Defines the number of clocks between the CAS_WS_RD command to when the dfi_wck_en signal is driven. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
23:16	dfi_twck_en_wr	R/W	Defines the number of clocks between the CAS_WS_WR command to when the dfi_wck_en signal is driven. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
15:8	dfi_twck_en_fs	R/W	Defines the number of clocks between the CAS_WS_FS command to when the dfi_wck_en signal is driven. Unit: WCK cycles **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1, Group 4

Table 3-35 Fields for Register: DFITMG4 (continued)

Bits	Name	Memory Access	Description
7:0	dfi_twck_dis	R/W	Defines the number of clock cycles between the last command (LAST CMD) without a WCK synchronization required (assuming no command issued) or any command that disables the WCK to when the dfi_wck_en signal is disabled. If SNPS PHY is used, please set to the following value. ■ Roundup(tWCKPST/tWCK) - 4 when MSTR4.wck_on=0. ■ Max[Roundup(tWCKSTOP/tWCK),Roundup(tCSLCK/tWCK)] - 3 when MSTR4.wck_on=1. The value may need to be adjusted if the SNPS PHY is used. For more detail, please refer to the SNPS PHY databook. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

3.1.32 DFITMG5

- **Name:** DFI Timing Register 5
- **Description:** DFI Timing Register 5
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x594+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5 SDRAM memories

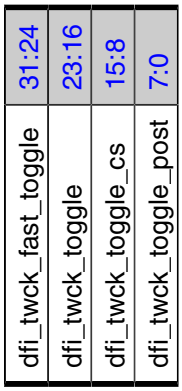


Table 3-36 Fields for Register: DFITMG5

Bits	Name	Memory Access	Description
31:24	dfi_twck_fast_toggle	R/W	Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
23:16	dfi_twck_toggle	R/W	Defines the number of clock cycles between the dfi_wck_en signal being enabled to when the dfi_wck_toggle signal is driven to TOGGLE. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

Table 3-36 Fields for Register: DFITMG5 (continued)

Bits	Name	Memory Access	Description
15:8	dfi_twck_toggle_cs	R/W	Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. This timing is applicable when the WCK is synchronized for multiple CS's and commands are to different CS's. During WCK synchronization, the CS should be static from the CAS command to the completion of the synchronization sequence. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4
7:0	dfi_twck_toggle_post	R/W	Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. During this time, the dfi_wck_cs signal must also remain stable. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

3.1.33 DFITMG6

- **Name:** DFI Timing Register 6
- **Description:** DFI Timing Register 6
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x598+f*0x100000+c*0x1000
- **Exists:** MEMC_LPDDR5X==1

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting LPDDR5X SDRAM memories

Table 3-37 Fields for Register: DFITMG6

Bits	Name	Memory Access	Description
31:9			**Reserved Field:** Yes
8	dfi_twck_toggle_post_rd_en	R/W	When this register is set to 1, the controller uses DFITMG6.dfi_twck_toggle_post_rd which defines WCK remaining period after read data burst completion. When this register is set to 0, the controller uses DFITMG5.dfi_twck_toggle_post for the WCK remaining period after both read and write data burst completion. This register shall be set to 0 unless SNPS LPDDR5X/5/4X PHY is used and the data rate is higher than 3200 Mbps. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

Table 3-37 Fields for Register: DFITMG6 (continued)

Bits	Name	Memory Access	Description
7:0	dfi_twck_toggle_post_rd	R/W	Defines the number of clock cycles after a read command data burst completion during which the WCK must remain in the current toggle state. During this time, the dfi_wck_cs signal must also remain stable. This register shall be set to "DFITMG5.dfi_twck_toggle_post + 8" if SNPS LPDDR5X/5/4X PHY is used and the data rate is higher than 3200 Mpbs. Unit: WCK cycles **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 4

3.1.34 DFITMG7

- **Name:** DFI Timing Register 7
- **Description:** DFI Timing Register 7
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x59c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DFI_SB_WDT_OR_MEMC_DDR5==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

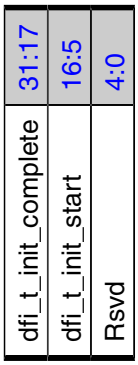


Table 3-38 Fields for Register: DFITMG7

Bits	Name	Memory Access	Description
31:17	dfi_t_init_complete	R/W	■ t_init_complete. Specifies the maximum number of DFI clock cycles after the de-assertion of the dfi_init_start signal to the re-assertion of the dfi_init_complete signal during a frequency change operation. Unit: DFI clock cycles. **Value After Reset:** 0x2edc **Volatile:** true **Programming Mode:** Static
16:5	dfi_t_init_start	R/W	■ t_init_start. Specifies maximum time from assertion of dfi_init_start to de- assertion of dfi_init_complete for a frequency change operation. Unit: DFI clock cycles. **Value After Reset:** 0x100 **Volatile:** true **Programming Mode:** Static
4:0			**Reserved Field:** Yes

3.1.35 DFILPTMG0

- **Name:** DFI Low Power Timing Register 0
- **Description:** DFI Low Power Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5a0+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

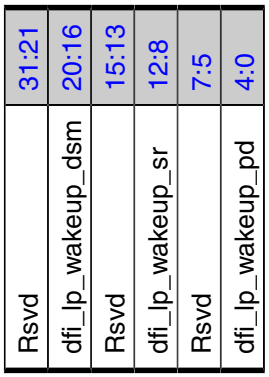


Table 3-39 Fields for Register: DFILPTMG0

Bits	Name	Memory Access	Description
31:21			**Reserved Field:** Yes

Table 3-39 Fields for Register: DFILPTMG0 (continued)

Bits	Name	Memory Access	Description
20:16	dfi_lp_wakeup_dsm	R/W	Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Deep Sleep Mode is entered. Determines the DFI's tlp_wakeup time: ■ 0x00 - 1 cycle ■ 0x01 - 2 cycles ■ 0x02 - 4 cycles ■ 0x03 - 8 cycles ■ 0x04 - 16 cycles ■ 0x05 - 32 cycles ■ 0x06 - 64 cycles ■ 0x07 - 128 cycles ■ 0x08 - 256 cycles ■ 0x09 - 512 cycles ■ 0x0A - 1024 cycles ■ 0x0B - 2048 cycles ■ 0x0C - 4096 cycles ■ 0x0D - 8192 cycles ■ 0x0E - 16384 cycles ■ 0x0F - 32768 cycles ■ 0x10 - 65536 cycles ■ 0x11 - 131072 cycles ■ 0x12 - 262144 cycles ■ 0x13 - Unlimited This is only present for designs supporting LPDDR5 devices. Unit: DFI clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes

Table 3-39 Fields for Register: DFILPTMG0 (continued)

Bits	Name	Memory Access	Description
12:8	dfi_lp_wakeup_sr	R/W	Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: ■ 0x00 - 1 cycle ■ 0x01 - 2 cycles ■ 0x02 - 4 cycles ■ 0x03 - 8 cycles ■ 0x04 - 16 cycles ■ 0x05 - 32 cycles ■ 0x06 - 64 cycles ■ 0x07 - 128 cycles ■ 0x08 - 256 cycles ■ 0x09 - 512 cycles ■ 0x0A - 1024 cycles ■ 0x0B - 2048 cycles ■ 0x0C - 4096 cycles ■ 0x0D - 8192 cycles ■ 0x0E - 16384 cycles ■ 0x0F - 32768 cycles ■ 0x10 - 65536 cycles ■ 0x11 - 131072 cycles ■ 0x12 - 262144 cycles ■ 0x13 - Unlimited Note: For Synopsys DDR54 PHY, this field must be set greater than 0 (0x01-0x0F is recommended currently). Unit: DFI clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes

Table 3-39 Fields for Register: DFILPTMG0 (continued)

Bits	Name	Memory Access	Description
4:0	dfi_lp_wakeup_pd	R/W	Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Power Down mode is entered. Determines the DFI's tlp_wakeup time: ■ 0x00 - 1 cycle ■ 0x01 - 2 cycles ■ 0x02 - 4 cycles ■ 0x03 - 8 cycles ■ 0x04 - 16 cycles ■ 0x05 - 32 cycles ■ 0x06 - 64 cycles ■ 0x07 - 128 cycles ■ 0x08 - 256 cycles ■ 0x09 - 512 cycles ■ 0x0A - 1024 cycles ■ 0x0B - 2048 cycles ■ 0x0C - 4096 cycles ■ 0x0D - 8192 cycles ■ 0x0E - 16384 cycles ■ 0x0F - 32768 cycles ■ 0x10 - 65536 cycles ■ 0x11 - 131072 cycles ■ 0x12 - 262144 cycles ■ 0x13 - Unlimited Note: For Synopsys DDR54 PHY, this field must be set greater than 0 (0x01-0x0F is recommended currently). Unit: DFI clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static

3.1.36 DFILPTMG1

- **Name:** DFI Low Power Timing Register 1
- **Description:** DFI Low Power Timing Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5a4+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

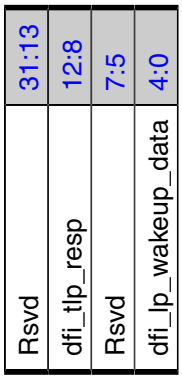


Table 3-40 Fields for Register: DFILPTMG1

Bits	Name	Memory Access	Description
31:13			**Reserved Field:** Yes
12:8	dfi_tlp_resp	R/W	Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Sleep Mode and Maximum Power Saving modes. Refer to PHY databook for recommended values Unit: DFI clock cycles. **Value After Reset:** 0x7 **Programming Mode:** Static
7:5			**Reserved Field:** Yes

Table 3-40 Fields for Register: DFILPTMG1 (continued)

Bits	Name	Memory Access	Description
4:0	dfi_lp_wakeup_data	R/W	Indicates the value in DFI clock cycles to drive on dfi_lp_data_wakeup signal when data bus is idle. Determines the DFI's tlp_wakeup time: ■ 0x00 - 1 cycle ■ 0x01 - 2 cycles ■ 0x02 - 4 cycles ■ 0x03 - 8 cycles ■ 0x04 - 16 cycles ■ 0x05 - 32 cycles ■ 0x06 - 64 cycles ■ 0x07 - 128 cycles ■ 0x08 - 256 cycles ■ 0x09 - 512 cycles ■ 0x0A - 1024 cycles ■ 0x0B - 2048 cycles ■ 0x0C - 4096 cycles ■ 0x0D - 8192 cycles ■ 0x0E - 16384 cycles ■ 0x0F - 32768 cycles ■ 0x10 - 65536 cycles ■ 0x11 - 131072 cycles ■ 0x12 - 262144 cycles ■ 0x13 - Unlimited Unit: DFI clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static

3.1.37 DFIUPDTMG0

- **Name:** DFI Update Timing Register 0
- **Description:** DFI Update Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5a8+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

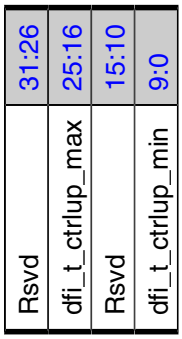


Table 3-41 Fields for Register: DFIUPDTMG0

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25:16	dfi_t_ctrlup_max	R/W	Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Refer to the PHY databook for recommended values Unit: DFI clock cycles. **Value After Reset:** 0x40 **Programming Mode:** Static
15:10			**Reserved Field:** Yes
9:0	dfi_t_ctrlup_min	R/W	Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The DDRCTL expects the PHY to respond within this time. If the PHY does not respond, the DDRCTL will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. **Value After Reset:** 0x3 **Programming Mode:** Static

3.1.38 DFIUPDTMG1

- **Name:** DFI Update Timing Register 1
- **Description:** DFI Update Timing Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5ac+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

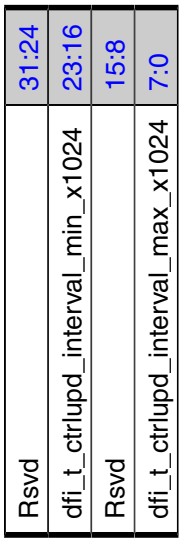


Table 3-42 Fields for Register: DFIUPDTMG1

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	dfi_t_ctrlupd_interval_min_x1024	R/W	This is the minimum amount of time between DDRCTL initiated DFI update type0 requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x1 **Programming Mode:** Static
15:8			**Reserved Field:** Yes

Table 3-42 Fields for Register: DFIUPDTMG1 (continued)

Bits	Name	Memory Access	Description
7:0	dfi_t_ctrlupd_interval_max_x1024	R/W	This is the maximum amount of time between DDRCTL initiated DFI update type0 requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPDTMG1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPDTMG1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x1 **Programming Mode:** Static

3.1.39 DFIMSGTMG0

- **Name:** DFI MC-PHY Message Timing Register 0
- **Description:** DFI MC-PHY Message Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5b0+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DFI_CTRLMSG==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-43 Fields for Register: DFIMSGTMG0

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7:0	dfi_t_ctrlmsg_resp	R/W	This is the maximum amount in DFI clock cycles between the assertion of the dfi{0/1}_ctrlmsg_req signal to the assertion of the dfi{0/1}_ctrlmsg_ack signal. If the PHY does not acknowledge the request within dfi_t_ctrlmsg_resp cycles, the PHY must not acknowledge the request at all. In this case, the controller should de-assert the corresponding dfi{0/1}_ctrlmsg_req signal. The timing values might vary based on the frequency ratio and user must reprogram if there is any change in the frequency ratio. Refer to PHY databook for recommended values. Minimum allowed value for this field is 2. Unit: DFI clock cycles. **Value After Reset:** 0x4 **Programming Mode:** Static

3.1.40 DFIUPDTMG2

- **Name:** DFI Update Timing Register 2
- **Description:** DFI Update Timing Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5b4+f*0x100000+c*0x1000
- **Exists:** DDRCTL_PPT2==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-44 Fields for Register: DFIUPDTMG2

Bits	Name	Memory Access	Description
31:30	dfi_t_ctrlupd_interval_type1_unit	R/W	DFI update type1 (PPT2) interval unit. Specifies the unit for counting interval. The value can be changed while DFIUPDTMG2.ppt2_en=0 and PPT2STAT0.ppt2_burst_busy=0 ■ 0: x32 DFI clock cycles (FOR DEBUG ONLY) ■ 1: x1k DFI clock cycles ■ 2: x16k DFI clock cycles ■ 3: x256k DFI clock cycles **Value After Reset:** 0x3 **Programming Mode:** Dynamic

Table 3-44 Fields for Register: DFIUPDTMG2 (continued)

Bits	Name	Memory Access	Description
29	ppt2_en	R/W	This register indicates if Normal PPT2 enable is enabled or disabled. ■ 0: Disable Normal PPT2 ■ 1: Enable Normal PPT2 The value can be changed while DDRCTL is in Normal mode **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	ppt2_override	R/W	This register indicates if PPT2 override is enabled or disabled. ■ 0: Disable PPT2 override ■ 1: Enable PPT2 override This bit should be set to 1 only when DFIUPDTMG2.ppt2_en=1. **Value After Reset:** 0x0 **Programming Mode:** Static
27	ctrlupd_after_dqsosc	R/W	This register indicates if ctrlupd, that is from PPT2 Override, is scheduled right after DQS ocsillator run. ■ 0: Don't schedule ctrlupd right after DQSOSC ■ 1: Schedule ctrlupd right after DQSOSC This bit is applicable when DFIUPDTMG2.ppt2_en=1, DFIUPDTMG2.ppt2_override=1 and DQSOSCCTL0.dqsosc_enable=1. **Value After Reset:** 0x0 **Programming Mode:** Static
26:12			**Reserved Field:** Yes

Table 3-44 Fields for Register: DFIUPDTMG2 (continued)

Bits	Name	Memory Access	Description
11:0	dfi_t_ctrlupd_interval_type1	R/W	This is the amount of time between DDRCTL initiated DFI update type1 (PPT2) requests. The timer resets with each update request. Set this number higher to reduce the frequency of update requests; when the timer expires, dfi_ctrlupd_req is sent and traffic is blocked for 500ns at most until DDRCTL receives dfi_ctrlupd_ack from PHY. PHY can use this idle time to retrain the DQ, DQS and WCK bus. Updates are required to maintain calibration over PVT, but too frequent updates may impact performance. Minimum allowed value for this field is 1. The value can be changed while DFIUPDTMG2.ppt2_en=0 and PPT2STAT0.ppt2_burst_busy=0 Unit: determined by DFIUPDTMG2.dfi_t_ctrlupd_interval_type1_unit Please refer to "Retraining interval" at the start of "PPT2 - Enhanced incremental periodic phase training" chapter for details on how to program this register field. **Value After Reset:** 0x12c **Programming Mode:** Dynamic

3.1.41 DFIUPDTMG3

- **Name:** DFI Update Timing Register 3
- **Description:** DFI Update Timing Register 3
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x5b8+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

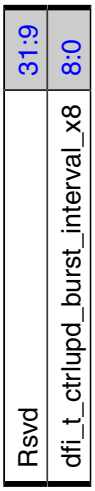


Table 3-45 Fields for Register: DFIUPDTMG3

Bits	Name	Memory Access	Description
31:9			**Reserved Field:** Yes
8:0	dfi_t_ctrlupd_burst_interval_x8	R/W	This is the maximum amount of time between DFI update type0 requests in burst. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfii_ctrlupd_ack is received. PHY can use this idle time to calibrate the delay lies to the DLLs. This register should be programmed DFI update inverval. Unit: Multiples of 8 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x1 **Programming Mode:** Static

3.1.42 RFSHSET1TMG0

- **Name:** Refresh Timing Register 0 belonging to Timing Set 1
- **Description:** Refresh Timing Register 0 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x600+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

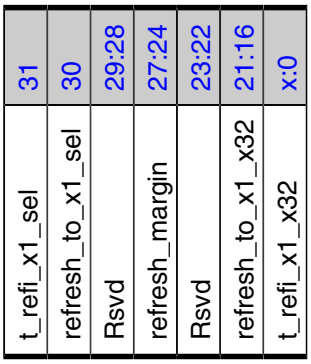


Table 3-46 Fields for Register: RFSHSET1TMG0

Bits	Name	Memory Access	Description
31	t_refi_x1_sel	R/W	Specifies whether RFSHSET1TMG0.t_refi_x1_x32 register values are x1 or x32. ■ 0 - x32 register values are used, ■ 1 - x1 register values are used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
30	refresh_to_x1_sel	R/W	Specifies whether RFSHSET1TMG0.refresh_to_x1_x32 register values are x1 or x32. ■ 0 - x32 register values are used, ■ 1 - x1 register values are used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
29:28			**Reserved Field:** Yes

Table 3-46 Fields for Register: RFSHSET1TMG0 (continued)

Bits	Name	Memory Access	Description
27:24	refresh_margin	R/W	Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32 * 32 if RFSHSET1TMG0.t_refi_x1_sel = 0. If RFSHSET1TMG0.t_refi_x1_sel = 1, internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. **Value After Reset:** 0x2 **Programming Mode:** Dynamic - Refresh Related
23:22			**Reserved Field:** Yes
21:16	refresh_to_x1_x32	R/W	If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this RFSHSET1TMG0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) or DDR5 same-bank refresh (REFsb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. When LPDDR REFpb is enabled and dynamic REFpb bank mode is selected (RFSHMOD0.fixed_crit_refpb_bank_en==0), this must be greater than (DRAMSET1TMG0.t_ras_min + DRAMSET1TMG4.t_rp) so that the target bank will be unchanged until the REFpb will be issued (the worst case is that ACT is issued just before REFpb requested). For non-DDR5, this should be programmed to tREFI based value in controller's current refresh mode. For DDR5, this should be always programmed to tREFI1 based value even in FGR mode. The controller calculates this according to current refresh mode.

Table 3-46 Fields for Register: RFSHSET1TMG0 (continued)

Bits	Name	Memory Access	Description
			Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles. For DDR54, the unit is always multiples of 32 DRAM clock cycles. For LPDDR54, the unit is speficied by RFSHSET1TMG0.refresh_to_x1_sel. **Value After Reset:** 0x10 **Programming Mode:** Dynamic - Refresh Related
x:0	t_refi_x1_x32	R/W	Average time interval between refreshes per rank (Specification: 7.8us for DDR4, 3.9us for DDR5. See JEDEC specification for LPDDR4/LPDDR5). set this register to RoundDown(tREFI/tCK) if RFSHSET1TMG0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: ■ if using all-bank refreshes (RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations ■ if using Not optimized per-bank refreshes (RFSHMOD0.per_bank_refresh = 1, RFSHMOD0.per_bank_refresh_opt_en = 0), use tREFIpb in the above calculations ■ if using optimized per-bank refreshes (RFSHMOD0.per_bank_refresh = 1, RFSHMOD0.per_bank_refresh_opt_en = 1), use tREFIab in the above calculations For DDR controller, tREFI value is different depending on FGR mode. ■ In DDR4 mode, if using FGR 1x mode (RFSHMOD1.fgr_mode = 000), use tREFI1 in the above calculations ■ In DDR4 mode, if using FGR 2x mode (RFSHMOD1.fgr_mode = 001), use tREFI2 in the above calculations ■ In DDR4 mode, if using FGR 4x mode (RFSHMOD1.fgr_mode = 010), use tREFI4 in the above calculations ■ In DDR5 mode, always use tREFI1 in the above calculations Note that: ■ RFSHSET1TMG0.t_refi_x1_x32 must be greater than 0x1. ■ if RFSHSET1TMG0.t_refi_x1_sel == 1, RFSHSET1TMG0.t_refi_x1_x32 must be greater than RFSHSET1TMG1.t_rfc_min

Table 3-46 Fields for Register: RFSHSET1TMG0 (continued)

Bits	Name	Memory Access	Description
			■ if RFSHSET1TMG0.t_refi_x1_sel == 0, RFSHSET1TMG0.t_refi_x1_x32 * 32 must be greater than RFSHSET1TMG1.t_rfc_min ■ In non-DDR4 or DDR4 Fixed 1x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0xFFE.
x:0...(cont.)	t_refi_x1_x32.	R/W	■ In DDR4 Fixed 2x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x7FF. ■ In DDR4 Fixed 4x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x3FF. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles. For LPDDR54,the unit is speficied by RFSHSET1TMG0.t_refi_x1_sel. For DDR54, the unit is always multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x62 **Programming Mode:** Dynamic - Refresh Related **Range Variable[x]:** "(SNPS_RSVDPARAM_657==1) ? 14 : 12" - 1

3.1.43 RFSHSET1TMG1

- **Name:** Refresh Timing Register 1 belonging to Timing Set 1
- **Description:** Refresh Timing Register 1 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x604+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

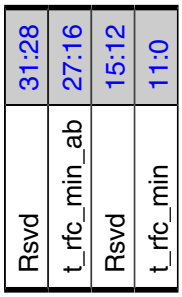


Table 3-47 Fields for Register: RFSHSET1TMG1

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27:16	t_rfc_min_ab	R/W	tRFCab: Minimum time from refresh to refresh or activate, for all-bank refreshes. When RFSHMOD0.auto_refab_en > 0 and RFSHMOD0.per_bank_refresh == 1, the controller will use this value when switching automatically from per-bank refresh to all-bank refresh if the derated refresh period is too small. t_rfc_min_ab must be set to RoundUp(tRFCab/tCK). Must be set for LPDDR5 2Gb, 6Gb, and 8Gb. Must be set to 0 for other device densities. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
15:12			**Reserved Field:** Yes

Table 3-47 Fields for Register: RFSHSET1TMG1 (continued)

Bits	Name	Memory Access	Description
11:0	t_rfc_min	R/W	tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: ■ if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab ■ if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4/DDR5 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user must program the appropriate value from the spec based on the 'fgr_mode' and the device density that is used. Unit: DRAM clock cycles. **Value After Reset:** 0x8c **Programming Mode:** Dynamic - Refresh Related

3.1.44 RFSHSET1TMG2

- **Name:** Refresh Timing Register 2 belonging to Timing Set 1
- **Description:** Refresh Timing Register 2 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x608+f*0x100000+c*0x1000
- **Exists:** MEMC_LPDDR4_OR_UMCTL2_CID_EN==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

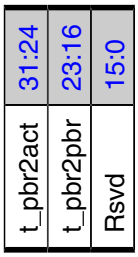


Table 3-48 Fields for Register: RFSHSET1TMG2

Bits	Name	Memory Access	Description
31:24	t_pbr2act	R/W	Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act **Value After Reset:** 0x8c **Programming Mode:** Dynamic - Refresh Related
23:16	t_pbr2pbr	R/W	LPDDR4/LPDDR5: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). **Value After Reset:** 0x8c **Programming Mode:** Dynamic - Refresh Related
15:0			**Reserved Field:** Yes

3.1.45 RFSHSET1TMG3

- **Name:** Refresh Timing Register 3 belonging to Timing Set 1
- **Description:** Refresh Timing Register 3 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x60c+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register is only applicable for designs supporting DDR5 or LPDDR54 SDRAM memories

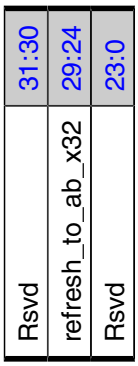


Table 3-49 Fields for Register: RFSHSET1TMG3

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:24	refresh_to_ab_x32	R/W	When the DDRCTL switches automatically from per-bank to all-bank refresh (if enabled by RFSHMOD0.auto_refab_en), it will use this register to determine when to perform speculative all-bank refreshes. If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHSET1TMG3.refresh_to_ab_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x10 **Programming Mode:** Dynamic - Refresh Related
23:0			**Reserved Field:** Yes

3.1.46 RFSHSET1TMG4

- **Name:** Refresh Timing Register 4 belonging to Timing Set 1
- **Description:** Refresh Timing Register 4 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x610+f*0x100000+c*0x1000
- **Exists:** MEMC_NUM_RANKS>1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-50 Fields for Register: RFSHSET1TMG4

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27:16	refresh_timer1_start_value_x32	R/W	Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
15:12			**Reserved Field:** Yes

Table 3-50 Fields for Register: RFSHSET1TMG4 (continued)

Bits	Name	Memory Access	Description
11:0	refresh_timer0_start_value_x32	R/W	Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related

3.1.47 RFSHSET1TMG5

- **Name:** Refresh Timing Register 5 belonging to Timing Set 1
- **Description:** Refresh Timing Register 5 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x614+f*0x100000+c*0x1000
- **Exists:** MEMC_NUM_RANKS>2

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-51 Fields for Register: RFSHSET1TMG5

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27:16	refresh_timer3_start_value_x32	R/W	Refresh timer start for rank 3 (only present in 4-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
15:12			**Reserved Field:** Yes

Table 3-51 Fields for Register: RFSHSET1TMG5 (continued)

Bits	Name	Memory Access	Description
11:0	refresh_timer2_start_value_x32	R/W	Refresh timer start for rank 2 (only present in 4-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related

3.1.48 RFSHSET1TMG11

- **Name:** Refresh Timing Register 11 belonging to Timing Set 1
- **Description:** Refresh Timing Register 11 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x62c+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR_MIXED_PKG==1

This register is in block REGB_FREQf_CHc.

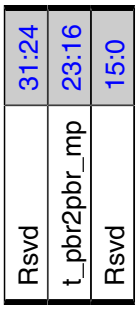


Table 3-52 Fields for Register: RFSHSET1TMG11

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	t_pbr2pbr_mp	R/W	LPDDR4/LPDDR5: tpbR2pbR,for upper ranks in mixed packages. Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). **Value After Reset:** 0x8c **Programming Mode:** Dynamic - Refresh Related
15:0			**Reserved Field:** Yes

3.1.49 RFSHSET1TMG12

- **Name:** Refresh Timing Register 12 belonging to Timing Set 1
- **Description:** Refresh Timing Register 12 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x630+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR_MIXED_PKG==1

This register is in block REGB_FREQf_CHc.

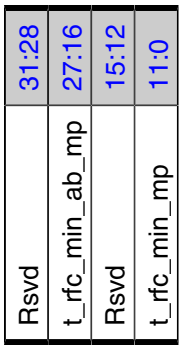


Table 3-53 Fields for Register: RFSHSET1TMG12

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27:16	t_rfc_min_ab_mp	R/W	tRFCab: Minimum time from refresh to refresh or activate, for all-bank refreshes,for upper ranks in mixed packages. When RFSHMOD0.auto_refab_en > 0 and RFSHMOD0.per_bank_refresh == 1, the controller will use this value when switching automatically from per-bank refresh to all-bank refresh if the derated refresh period is too small. t_rfc_min_ab must be set to RoundUp(tRFCab/tCK). Must be set for LPDDR5 2Gb, 6Gb, and 8Gb. Must be set to 0 for other device densities. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
15:12			**Reserved Field:** Yes

Table 3-53 Fields for Register: RFSHSET1TMG12 (continued)

Bits	Name	Memory Access	Description
11:0	t_rfc_min_mp	R/W	tRFC (min): Minimum time from refresh to refresh or activate,for upper ranks in mixed packages. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: ■ if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab ■ if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb Unit: DRAM clock cycles. **Value After Reset:** 0x8c **Programming Mode:** Dynamic - Refresh Related

3.1.50 RFMSET1TMG0

- **Name:** RFM Timing Register 0 belonging to Timing Set 1
- **Description:** RFM Timing Register 0 belonging to Timing Set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x650+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR_RFM==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

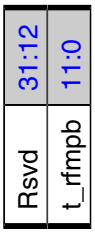


Table 3-54 Fields for Register: RFMSET1TMG0

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11:0	t_rfmpb	R/W	tRFMpb: Refresh Management Cycle (per-bank). Unit: DRAM clock cycles. **Value After Reset:** 0x8c **Programming Mode:** Static

3.1.51 RFMSET1TMG1

- **Name:** RFM Timing Register 1 belonging to Timing Set 1
- **Description:** RFM Timing Register 1 belonging to Timing Set 1
- **Size:** 32 bits
- **Offset:** 0x654+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR_RFM==1 && DDRCTL_LPDDR_MIXED_PKG==1

This register is in block REGB_FREQf_CHc.

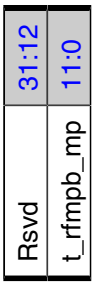


Table 3-55 Fields for Register: RFMSET1TMG1

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11:0	t_rfmpb_mp	R/W	tRFMpb: Refresh Management Cycle (per-bank), for upper ranks in mixed packages. Unit: DRAM clock cycles. **Value After Reset:** 0x8c **Programming Mode:** Static

3.1.52 ZQSET1TMG0

- **Name:** ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
- **Description:** ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x800+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

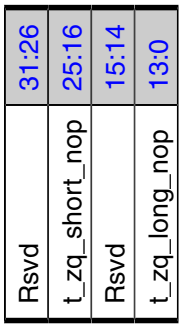


Table 3-56 Fields for Register: ZQSET1TMG0

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25:16	t_zq_short_nop	R/W	tZQCS for DD4, tZQLAT for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. **Value After Reset:** 0x40 **Programming Mode:** Static
15:14			**Reserved Field:** Yes
13:0	t_zq_long_nop	R/W	tZQoper for DDR4, tZQCAL for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. **Value After Reset:** 0x200 **Programming Mode:** Static

3.1.53 ZQSET1TMG1

- **Name:** ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
- **Description:** ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x804+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

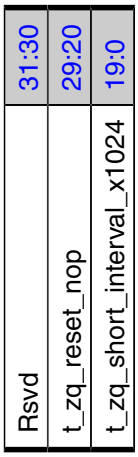


Table 3-57 Fields for Register: ZQSET1TMG1

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:20	t_zq_reset_nop	R/W	tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. **Value After Reset:** 0x20 **Programming Mode:** Static
19:0	t_zq_short_interval_x1024	R/W	Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR4/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x100 **Programming Mode:** Static

3.1.54 ZQSET1TMG2

- **Name:** ZQ Timing Register 2 belonging to DRAM ZQ timing set 1
- **Description:** ZQ Timing Register 2 belonging to DRAM ZQ timing set 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x808+f*0x100000+c*0x1000
- **Exists:** UMCTL2_HWFFC_EN==1 && DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

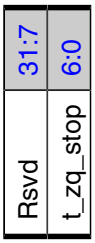


Table 3-58 Fields for Register: ZQSET1TMG2

Bits	Name	Memory Access	Description
31:7			**Reserved Field:** Yes
6:0	t_zq_stop	R/W	tZQSTOP for LPDDR5: Number of DRAM clock cycles of delay time from ZQ Stop bit set to ZQ resistor available. This field is ignored for LPDDR4. Unit: DRAM clock cycles. **Value After Reset:** 0x18 **Programming Mode:** Static

3.1.55 DQSOSCCTL0

- **Name:** DQS/WCK Oscillator Control Register 0
- **Description:** DQS/WCK Oscillator Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xa80+f*0x100000+c*0x1000
- **Exists:** LPDDR45_DQSOSC_EN==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

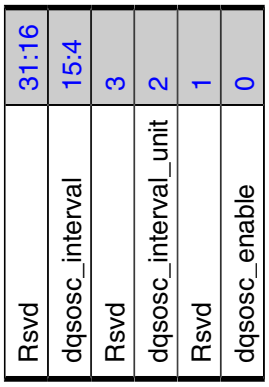


Table 3-59 Fields for Register: DQSOSCCTL0

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15:4	dqsosc_interval	R/W	DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles **Value After Reset:** 0x7 **Programming Mode:** Dynamic
3			**Reserved Field:** Yes
2	dqsosc_interval_unit	R/W	DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval.The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1: x2K DFI clock cycles 0: x32K DFI clock cycles **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1			**Reserved Field:** Yes

Table 3-59 Fields for Register: DQSOSCCTL0 (continued)

Bits	Name	Memory Access	Description
0	dqsosc_enable	R/W	DQS/WCK Oscillator Enable 1: Enable DQS Oscillator 0: Disable DQS Oscillator **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.1.56 DERATEINT

- **Name:** Temperature Derate Interval Register
- **Description:** Temperature Derate Interval Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xb00+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-60 Fields for Register: DERATEINT

Bits	Name	Memory Access	Description
31:0	mr4_read_interval	R/W	Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. **Value After Reset:** 0x800000 **Volatile:** true **Programming Mode:** Static

3.1.57 DERATEVAL0

- **Name:** Temperature Derate Timing Register 0
- **Description:** Temperature Derate Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xb04+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

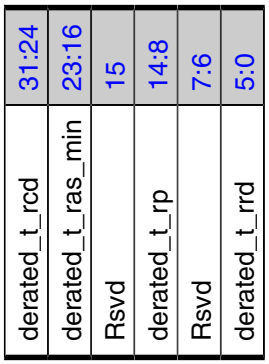


Table 3-61 Fields for Register: DERATEVAL0

Bits	Name	Memory Access	Description
31:24	derated_t_rcd	R/W	Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-61 Fields for Register: DERATEVAL0 (continued)

Bits	Name	Memory Access	Description
23:16	derated_t_ras_min	R/W	Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
15			**Reserved Field:** Yes
14:8	derated_t_rp	R/W	Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
7:6			**Reserved Field:** Yes
5:0	derated_t_rrd	R/W	Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.58 DERATEVAL1

- **Name:** Temperature Derate Timing Register 1
- **Description:** Temperature Derate Timing Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xb08+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

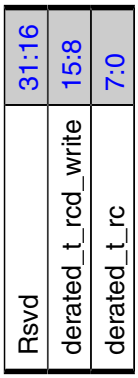


Table 3-62 Fields for Register: DERATEVAL1

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15:8	derated_t_rcd_write	R/W	Derated value for DRAMSET1TMG1.t_rcd_write. This register field is used only in LPDDR5X mode For LPDDR5X, the required period with derating is DRAMSET1TMG1.t_rcd_write + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0x5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-62 Fields for Register: DERATEVAL1 (continued)

Bits	Name	Memory Access	Description
7:0	derated_t_rc	R/W	Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. **Value After Reset:** 0x14 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.1.59 HWLPTMG0

- **Name:** Hardware Low Power Timing Register 0
- **Description:** Hardware Low Power Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xb80+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

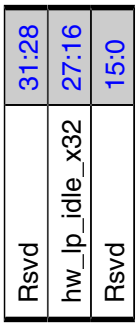


Table 3-63 Fields for Register: HWLPTMG0

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes

Table 3-63 Fields for Register: HWLPTMG0 (continued)

Bits	Name	Memory Access	Description
27:16	hw_lp_idle_x32	R/W	Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. FOR PERFORMANCE ONLY. Note: When there is no traffic from channel 0 (and also channel 1 if it's dual channel configuration) and cactive_in_ddrc is de-asserted, controller IP starts to count for a period defined by HWLPTMG0.hw_lp_idle_x32. After the period ends, the controller drives cactive_ddrc output low. So customer should decide how soon they want controller IP to indicate the controller has been idle for enough time, and how frequently they want the system to go into power-saving mode. The value of this register really depends on system low power requirement. General suggestion is to set to a value no smaller than 4 (128 DFI cycles). Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
15:0			**Reserved Field:** Yes

3.1.60 DVFSCTL0

- **Name:** Dynamic Voltage and Frequency Scaling (DVFS) Control Register
- **Description:** Dynamic Voltage and Frequency Scaling (DVFS) Control Register
  This register only affects HWFFC with HWFFCCTL.hwffc_mode=1 behavior
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xb84+f*0x100000+c*0x1000
- **Exists:** UMCTL2_HWFFC_EN==1 && DDRCTL_LPDDR==1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

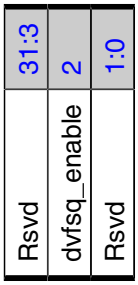


Table 3-64 Fields for Register: DVFSCTL0

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dvfsq_enable	R/W	Enable LPDDR5 DVFSQ feature. DVFSQ High-to-Low and Low-to-High steps will be inserted to HWFFC sequence if dvfsq_enable toggle detected between currnet and next frequency sets. **Value After Reset:** 0x0 **Programming Mode:** Static
1:0			**Reserved Field:** Yes

3.1.61 SCHEDTMG0

- **Name:** Scheduler Control Register
- **Description:** Scheduler Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xc00+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

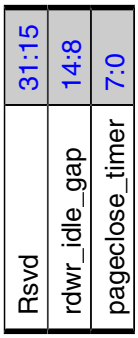


Table 3-65 Fields for Register: SCHEDTMG0

Bits	Name	Memory Access	Description
31:15			**Reserved Field:** Yes
14:8	rdwr_idle_gap	R/W	When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-65 Fields for Register: SCHEDTMG0 (continued)

Bits	Name	Memory Access	Description
7:0	pageclose_timer	R/W	This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explicit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static

3.1.62 PERFHPR1

- **Name:** High Priority Read CAM Register 1
- **Description:** High Priority Read CAM Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xc80+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

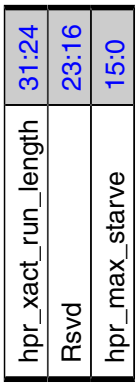


Table 3-66 Fields for Register: PERFHPR1

Bits	Name	Memory Access	Description
31:24	hpr_xact_run_length	R/W	Number of transactions that are serviced once the HPR queue goes critical is the smaller of: ■ This number ■ Number of transactions available Unit: Transaction. FOR PERFORMANCE ONLY. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
23:16			**Reserved Field:** Yes

Table 3-66 Fields for Register: PERFHPR1 (continued)

Bits	Name	Memory Access	Description
15:0	hpr_max_starve	R/W	Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.1.63 PERFLPR1

- **Name:** Low Priority Read CAM Register 1
- **Description:** Low Priority Read CAM Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xc84+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

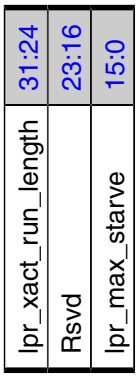


Table 3-67 Fields for Register: PERFLPR1

Bits	Name	Memory Access	Description
31:24	lpr_xact_run_length	R/W	Number of transactions that are serviced once the LPR queue goes critical is the smaller of: ■ This number ■ Number of transactions available Unit: Transaction. FOR PERFORMANCE ONLY. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
23:16			**Reserved Field:** Yes

Table 3-67 Fields for Register: PERFLPR1 (continued)

Bits	Name	Memory Access	Description
15:0	lpr_max_starve	R/W	Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. **Value After Reset:** 0x7f **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.1.64 PERFWR1

- **Name:** Write CAM Register 1
- **Description:** Write CAM Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xc88+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

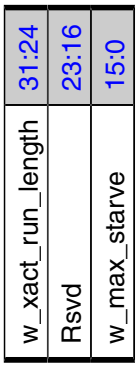


Table 3-68 Fields for Register: PERFWR1

Bits	Name	Memory Access	Description
31:24	w_xact_run_length	R/W	Number of transactions that are serviced once the WR queue goes critical is the smaller of: ■ (a) This number ■ (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
23:16			**Reserved Field:** Yes

Table 3-68 Fields for Register: PERFWR1 (continued)

Bits	Name	Memory Access	Description
15:0	w_max_starve	R/W	Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. **Value After Reset:** 0x7f **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.1.65 TMGCFG

- **Name:** Timing Configuration Register
- **Description:** Timing Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd00+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

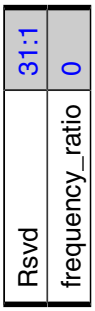


Table 3-69 Fields for Register: TMGCFG

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	frequency_ratio	R/W	Selects the Frequency Ratio For DDR4/DDR5/LPDDR4: ■ 0: 1:2 Mode ■ 1: 1:4 Mode For DDR54 controller product, set it to 0 in DDR4 mode, set it to 1 in DDR5 mode. For LL controller product, this value is not cared but recommended to set to 0. For DDR5 controller product, this value is not cared but recommended to set to 1. For LPDDR5: ■ 0: 1:1:2 Mode ■ 1: 1:1:4 Mode **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 2

3.1.66 RANKTMG0

- **Name:** Rank Control Timing 0
- **Description:** Rank Control Timing 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd04+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1 && MEMC_NUM_RANKS>1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

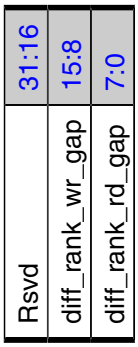


Table 3-70 Fields for Register: RANKTMG0

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15:8	diff_rank_wr_gap	R/W	Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. ■ PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. If write preamble is set to 2tCK(DDR4 only), must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ■ ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1

Table 3-70 Fields for Register: RANKTMG0 (continued)

Bits	Name	Memory Access	Description
			For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x6 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

Table 3-70 Fields for Register: RANKTMG0 (continued)

Bits	Name	Memory Access	Description
7:0	diff_rank_rd_gap	R/W	Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. ■ PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) If read preamble is set to 2tCK(DDR4 only), must be increased by 1. If read postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ■ ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: diff_rank_rd_gap must be a minimum of ODTCFG.rd_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TRDRD timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. **Value After Reset:** 0x6 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

3.1.67 RANKTMG1

- **Name:** Rank Timing Register 1
- **Description:** Rank Timing Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd08+f*0x100000+c*0x1000
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1 && MEMC_NUM_RANKS>1

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-71 Fields for Register: RANKTMG1

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15:8	rd2wr_dr	R/W	Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr(LPDDR4 or LPDDR5 16B mode) or DRAMSET1TMG24.rd2wr_s(LPDDR5 BG mode). For LPDDR4, Please set to the same value as DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

Table 3-71 Fields for Register: RANKTMG1 (continued)

Bits	Name	Memory Access	Description
7:0	wr2rd_dr	R/W	Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR4, Please set to Max(4, WDQS_off - (RL + RD(tDQSCKmin/tCK) - RU(tRPRE/tCK)) + 8) For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles **Value After Reset:** 0xf **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1, Group 2, Group 4

3.1.68 PWRTMG

- **Name:** Low Power Timing Register
- **Description:** Low Power Timing Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd0c+f*0x100000+c*0x1000
- **Exists:** Always

This register is in block REGB_FREQf_CHc.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

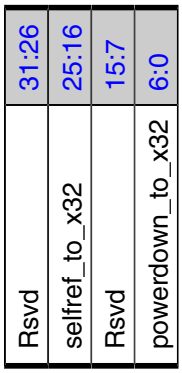


Table 3-72 Fields for Register: PWRTMG

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25:16	selfref_to_x32	R/W	After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. selfref_to_x32=0 is an illegal value. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x40 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4
15:7			**Reserved Field:** Yes

Table 3-72 Fields for Register: PWRTMG (continued)

Bits	Name	Memory Access	Description
6:0	powerdown_to_x32	R/W	After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. For LPDDR54 and DDR4, this value should be greater than 2 when the controller is in 1:2 mode and 4 when the controller is in 1:4 mode. For DDR5, this value should be greater than 0. The DDRCTL starts to count down from this value when the DDRC command channel is idle and in normal state. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x10 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 4

3.1.69 DDR4PPRTMG0

- **Name:** PPR Timing 0
- **Description:** PPR Timing 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd30+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR5_PPR_OR_DDRCTL_DDR4_PPR==1

This register is in block REGB_FREQf_CHc.
Note: This register is for PPR timing. Register name contains 'DDR4' for historical reason but is also applicable to LPDDR5 PPR. This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

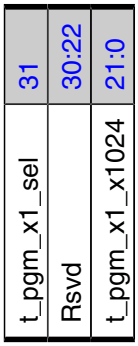


Table 3-73 Fields for Register: DDR4PPRTMG0

Bits	Name	Memory Access	Description
31	t_pgm_x1_sel	R/W	Specifies whether DDR4PPRTMG0.t_pgm_x1_x1024 is x1 or x1024 ■ 0 - x1024 register values are used ■ 1 - x1 register values are used For DDR4 hPPR, use value of 0 For DDR4 sPPR, use value of 1 For LPDDR5 PPR, always use value of 0 This register is used only for DDR4 or LPDDR5 PPR **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
30:22			**Reserved Field:** Yes

Table 3-73 Fields for Register: DDR4PPRTMG0 (continued)

Bits	Name	Memory Access	Description
21:0	t_pgm_x1_x1024	R/W	tPGM for DDR4 or LPDDR5 PPR ■ For DDR4 hPPR, set tPGMa or tPGMb based on device type ■ For DDR4 sPPR, WL + 4tCK + tWR ■ For LPDDR5 PPR, set tPGM This register is used only for DDR4 or LPDDR5 PPR In both DDR4 and LPDDR5 PPR, when this is x1024 register (DDR4PPRTMG0.t_pgm_x1_sel=0), this register must be programmed as below roundup(tPGM/tCK/1024)+2 In LPDDR5 PPR, this is always x1024 register. Unit: Multiples of 1024 DRAM clock cycles or DRAM clock cycles **Value After Reset:** 0x2faf09 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.1.70 DDR4PPRTMG1

- **Name:** PPR Timing 1
- **Description:** PPR Timing 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd34+f*0x100000+c*0x1000
- **Exists:** DDRCTL_LPDDR5_PPR_OR_DDRCTL_DDR4_PPR==1

This register is in block REGB_FREQf_CHc.
Note: This register is for PPR timing. Register name contains 'DDR4' for historical reason but is also applicable to LPDDR5 PPR. This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

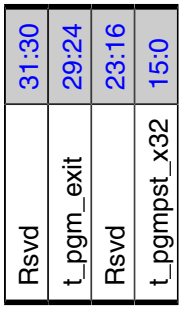


Table 3-74 Fields for Register: DDR4PPRTMG1

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:24	t_pgm_exit	R/W	tPGM_Exit for DDR4 or LPDDR5 PPR Unit: DRAM clock cycle **Value After Reset:** 0x18 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
23:16			**Reserved Field:** Yes
15:0	t_pgmpst_x32	R/W	tPGMPST for DDR4 or LPDDR5 PPR Unit: Multiples of 32 DRAM clock cycles **Value After Reset:** 0x9c5 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.1.71 LNKECCCTL0

- **Name:** Link-ECC Control Register 0
- **Description:** Link-ECC Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0xd80+f*0x100000+c*0x1000
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_FREQf_CHc.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

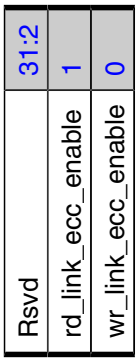


Table 3-75 Fields for Register: LNKECCCTL0

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	rd_link_ecc_enable	R/W	Enable LPDDR5 Read Link ECC feature. ■ 0 - Disabel LPDDR5 Read Link ECC ■ 1 - Enable LPDDR5 Read Link ECC When non-LPDDR5 devices are used, this register must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
0	wr_link_ecc_enable	R/W	Enable LPDDR5 Write Link ECC feature. ■ 0 - Disabel LPDDR5 Write Link ECC ■ 1 - Enable LPDDR5 Write Link ECC When non-LPDDR5 devices are used, this register must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

3.2 REGB_DDRC_CH0 Registers

This register block contains registers related to the control of functionality and the configuration of the DDRC controller. Registers shared by both channels are only present in REGB_DDRC_CH0.

3.2.1 MSTR0

- **Name:** Master Register0
- **Description:** Master Register0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10000
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

x:24	23:21	20:16	15:14	13:12	11	10:9	8	7:4	3	2	1	0
active_ranks	Rsvd	burst_rdwr	Rsvd	data_bus_width	lpddr5x	Rsvd	burst_mode	Rsvd	lpddr5	Rsvd	lpddr4	Rsvd

Table 3-76 Fields for Register: MSTR0

Bits	Name	Memory Access	Description
x:24	active_ranks	R/W	Only present for multi-rank configurations. Each bit represents one rank. For two-rank configurations, only bits[25:24] are present. ■ 1 - populated ■ 0 - unpopulated LSB is the lowest rank number. For 2 ranks following combinations are legal: ■ 01 - One rank ■ 11 - Two ranks ■ Others - Reserved. For 4 ranks following combinations are legal: ■ 0001 - One rank ■ 0011 - Two ranks ■ 0101 - Two ranks are populated in Rank0 and Rank2 (DDR5 Only). ■ 1111 - Four ranks Note: the four rank populated config 4'b0101 can only be supported with heterogeneous rank support enable. **Value After Reset:** "(MEMC_NUM_RANKS==4) ? 0xF :((MEMC_NUM_RANKS==2) ? 0x3 : 0x1)" **Programming Mode:** Static **Range Variable[x]:** "(MEMC_NUM_RANKS==2) ? 2 : 4" + 23
23:21			**Reserved Field:** Yes
20:16	burst_rdwr	R/W	SDRAM burst length used: ■ 00100 - Burst length of 8 ■ 01000 - Burst length of 16 ■ 10000 - Burst length of 32 All other values are reserved. This controls the burst size used to access the SDRAM. This must match the burst length mode register setting in the SDRAM. For DDR4, this must be set to 5'b00100 (BL8). For DDR5, this must be set to 5'b01000 (BL16). For LPDDR4/LPDDR5, this must be set to 5'b01000 (BL16) if MEMC_BURST_LENGTH=16 or to 5'b10000 (BL32) if MEMC_BURST_LENGTH=32. **Value After Reset:** 0x4 **Programming Mode:** Static
15:14			**Reserved Field:** Yes

Table 3-76 Fields for Register: MSTR0 (continued)

Bits	Name	Memory Access	Description
13:12	data_bus_width	R/W	Selects proportion of DQ bus width that is used by the SDRAM ■ 00 - Full DQ bus width to SDRAM ■ 01 - Half DQ bus width to SDRAM ■ 10 - Quarter DQ bus width to SDRAM ■ 11 - Reserved. Note that half bus width mode is only supported when the SDRAM bus width (DQ bus width) is a multiple of 16, and quarter bus width mode is only supported when the SDRAM bus width (DQ bus width) is a multiple of 32 and the configuration parameter MEMC_QBUS_SUPPORT is set. Bus width refers to DQ bus width (excluding any ECC width). However, MEMC_DRAM_DATA_WIDTH = 72 represents 64-bit DQ bus width plus 8-bit ECC and hence supports half and quarter bus width mode. **Value After Reset:** 0x0 **Programming Mode:** Static
11	lpddr5x	R/W	Select LPDDR5X SDRAM ■ 1 - LPDDR5X SDRAM device in use. ■ 0 - non-LPDDR5X device in use Note that MSTR0.lpddr5 should also be set to 1 whenever MSTR0.lpddr5x is set to 1. Present only in designs configured to support LPDDR5X SDRAM memories. **Value After Reset:** 0x0 **Programming Mode:** Static
10:9			**Reserved Field:** Yes
8	burst_mode	R/W	Indicates burst mode. ■ 0 - Sequential burst mode ■ 1 - Interleaved burst mode For LPDDR4 and DDR5 usage, this must be set to 0 (sequential mode). **Value After Reset:** 0x0 **Programming Mode:** Static
7:4			**Reserved Field:** Yes

Table 3-76 Fields for Register: MSTR0 (continued)

Bits	Name	Memory Access	Description
3	lpddr5	R/W	Select LPDDR5 SDRAM ■ 1 - LPDDR5 or LPDDR5X SDRAM device in use. ■ 0 - non-LPDDR5 and non-LPDDR5X device in use Present only in designs configured to support LPDDR5 or LPDDR5X SDRAM memories. **Value After Reset:** 0x0 **Programming Mode:** Static
2			**Reserved Field:** Yes
1	lpddr4	R/W	Select LPDDR4 SDRAM ■ 1 - LPDDR4 SDRAM device in use. ■ 0 - non-LPDDR4 device in use Present only in designs configured to support LPDDR4 SDRAM memories. **Value After Reset:** 0x0 **Programming Mode:** Static
0			**Reserved Field:** Yes

3.2.2 MSTR2

- **Name:** Master Register2
- **Description:** Master Register2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10008
- **Exists:** UMCTL2_FREQUENCY_NUM>1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-77 Fields for Register: MSTR2

Bits	Name	Memory Access	Description
x:0	target_frequency	R/W	This field specifies the target frequency. ■ 0 - Frequency 0/Normal ■ 1 - Frequency 1/FREQ1 ■ 2 - Frequency 2/FREQ2 ■ 3 - Frequency 3/FREQ3 ■ 4 - Frequency 4/FREQ4 ■ 5 - Frequency 5/FREQ5 ■ 6 - Frequency 6/FREQ6 ■ 7 - Frequency 7/FREQ7 ■ 8 - Frequency 8/FREQ8 ■ 9 - Frequency 9/FREQ9 ■ 10 - Frequency 10/FREQ10 ■ 11 - Frequency 11/FREQ11 ■ 12 - Frequency 12/FREQ12 ■ 13 - Frequency 13/FREQ13 ■ 14 - Frequency 14/FREQ14 ■ All other values are reserved. Note: If the target frequency can be changed through Hardware Low Power Interface only, this field is not needed. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2 **Range Variable[x]:** "DDRCTL_FREQUENCY_BITS" - 1

3.2.3 MSTR4

- **Name:** Master Register4
- **Description:** Master Register4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10010
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

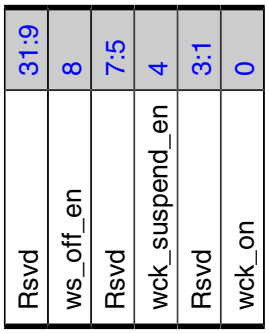


Table 3-78 Fields for Register: MSTR4

Bits	Name	Memory Access	Description
31:9			**Reserved Field:** Yes
8	ws_off_en	R/W	CAS-WS_OFF enable. If this bit is set to 1, the controller actively issues CAS-WS_OFF command. This register is valid only if MSTR4.wck_on is set to 1. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
7:5			**Reserved Field:** Yes
4	wck_suspend_en	R/W	Enhanced WCK always on mode. If this register is set to 1, the controller issues CAS-WCK_SUSPEND command. This register is valid only if MSTR4.wck_on is set to 1. Note: CAS-WCK_SUSPEND command is valid only when MR0 OP[2]=1b(Enhanced WCK Always On mode supported) and MR18 OP[4]=1b(WCK Always On mode enabled). **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
3:1			**Reserved Field:** Yes

Table 3-78 Fields for Register: MSTR4 (continued)

Bits	Name	Memory Access	Description
0	wck_on	R/W	WCK always ON mode ■ 0: WCK Always On mode disabled ■ 1: WCK Always On mode enabled In case of multi-rank system, the controller issues CAS-WS_FS to all ranks to sets DRAM in sync state simultaneously. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

3.2.4 STAT

- **Name:** Operating Mode Status Register
- **Description:** Operating Mode Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10014
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

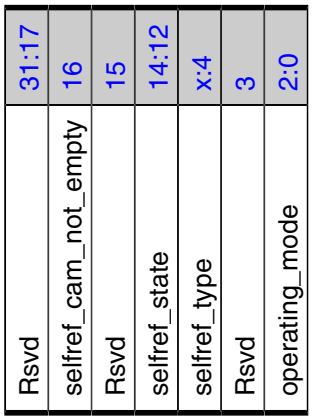


Table 3-79 Fields for Register: STAT

Bits	Name	Memory Access	Description
31:17			**Reserved Field:** Yes
16	selfref_cam_not_empty	R	Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. FOR DEBUG ONLY. Use OPCTRLCAM.dbg_wr_q_empty, OPCTRLCAM.dbg_rd_q_empty, STAT.selfref_state and STAT.selfref_type instead. **Value After Reset:** 0x0 **Programming Mode:** Static
15			**Reserved Field:** Yes

Table 3-79 Fields for Register: STAT (continued)

Bits	Name	Memory Access	Description
14:12	selfref_state	R	Self refresh state. This indicates self refresh or self refresh power down state or Deep Sleep Mode (LPDDR5 only). This register is used for frequency change and MRR/MRW access during self refresh. ■ 000 - SDRAM is not in Self Refresh. ■ 001 - Self refresh 1 ■ 010 - Self refresh power down ■ 011 - Self refresh 2 ■ 100 - Deep Sleep Mode (LPDDR5 only) **Value After Reset:** 0x0 **Programming Mode:** Static
x:4	selfref_type	R	Flags if Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5) is entered and if it was under Automatic Self Refresh control only or not. ■ 00 - SDRAM is not in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5). If CA parity retry is enabled by RETRYCTL0.capar_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. ■ 11 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. ■ 10 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. ■ 01 - SDRAM is in Self Refresh, which was caused by PHY Master Request or Normal PPT2. For LPDDR54 and DDR4, only bit[5:4] are used. For DDR5, self-refresh per rank control is supported. ■ bit[5:4] - rank 0 selfref_type ■ bit[7:6] - rank 1 selfref_type ■ bit[9:8] - rank 2 selfref_type ■ bit[11:10] - rank 3 selfref_type **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? (MEMC_NUM_RANKS*2) : 2" + 3
3			**Reserved Field:** Yes

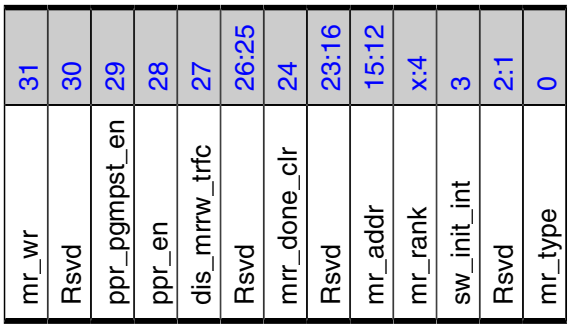
Table 3-79 Fields for Register: STAT (continued)

Bits	Name	Memory Access	Description
2:0	operating_mode	R	Operating mode. **DDR4/DDR5 designs:** ■ 000 - Init ■ 001 - Normal ■ 010 - Power-down (For DDR4, this means all ranks are in power-down state. For DDR5, this means at least one rank is in power-down state, check powerdown_state for details) ■ 011 - Self refresh (For DDR4/DDR5, this means all ranks are in self refresh state, check selfref_type for details) ■ 1XX - Maximum Power Saving Mode (For DDR4 only) **LPDDR4/LPDDR5designs:** ■ 000 - Init ■ 001 - Normal ■ 010 - Power-down ■ 011 - Self refresh / Self refresh power-down **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.5 MRCTRL0

- **Name:** Mode Register Read/Write Control Register 0.
- **Description:** Mode Register Read/Write Control Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10080
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31	30	29	28	27	26:25	24	23:16	15:12	x:4	3	2:1	0
mr_wr	Rsvd	ppr_pgmpst_en	ppr_en	dis_mrrw_trfc	Rsvd	mrr_done_clr	Rsvd	mr_addr	mr_rank	sw_init_int	Rsvd	mr_type

Table 3-80 Fields for Register: MRCTRL0

Bits	Name	Memory Access	Description
31	mr_wr	R/W1S	Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the DDRCTL automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30			**Reserved Field:** Yes
29	ppr_pgmpst_en	R/W	If this is set to one, writing MRCTRL0.mr_wr will insert a command gap of DDR4PPRTMG1.t_pgmpst_x32 after an MRS/MRW issued by MRCTRL0.mr_wr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-80 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
28	ppr_en	R/W	If this is set to one, writing MRCTRL0.mr_wr will trigger part of DDR4 or LPDDR5 PPR sequence i.e. ACT/WR/PRE if DDR4 PPR. ACT/PRE if LPDDR5 PPR. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
27	dis_mrrw_trfc	R/W	When this is set to 1, the DDRCTL does not perform the mode register operation during refresh operation (tRFC). In LPDDR4, MRR, MRW and MPC can be issued during tRFC. Thus this should be always set to 0. In LPDDR5/5X, MRW to change RFM level (MR57:OP[7:6]) is prohibited during tRFC. This needs to be set to 1 at that time. For all other LPDDR5/5X MRR, MRW and MPC which the DDRCTL currently supports, this should be set to 0. Note: Setting this to '1' is limited in Changing RFM level (ARFM) sequence only. Please contact Synopsys if you wish to use this for other purpose. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26:25			**Reserved Field:** Yes
24	mrr_done_clr	R/W1C	If this bit is set, mrr_done will be cleared by the controller. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:16			**Reserved Field:** Yes

Table 3-80 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
15:12	mr_addr	R/W	Address of the mode register that is to be written to. ■ 0000 - MR0 ■ 0001 - MR1 ■ 0010 - MR2 ■ 0011 - MR3 ■ 0100 - MR4 ■ 0101 - MR5 ■ 0110 - MR6 ■ 0111 - MR7 This signal is also used for writing to control words of the register chip on RDIMMs/LRDIMMs. In that case, it corresponds to the bank address bits sent to the RDIMM/LRDIMM. In case of DDR4, the bit[3:2] corresponds to the bank group bits. Therefore, the bit[3] as well as the bit[2:0] must be set to an appropriate value which is considered both the Address Mirroring of UDIMMs/RDIMMs/LRDIMMs and the Output Inversion of RDIMMs/LRDIMMs. Don't Care for LPDDR4/5 if PPR is not used. (see MRCTRL1.mr_data for mode register addressing in LPDDR4/5). If LPDDR5 PPR is used, 3 LSB bits of this field represents Bank and/or Bank group i.e., {BA2, BA1, BA0} in 16B mode and {BG0, BA1, BA0} in BG mode. Other bits don't take effect and should be 0. Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW/MRR access in DDR5). **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:4	mr_rank	R/W	Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits must be set to 1. However, for multi-rank UDIMMs/RDIMMs/LRDIMMs which implement address mirroring, it may be necessary to access ranks individually. Examples (assume DDRCTL is configured for 4 ranks): ■ 0x1 - select rank 0 only ■ 0x2 - select rank 1 only ■ 0x5 - select ranks 0 and 2 ■ 0xA - select ranks 1 and 3 ■ 0xF - select ranks 0, 1, 2 and 3 Don't Care for DDR5. **Value After Reset:** "(MEMC_NUM_RANKS==4) ? 0xF :((MEMC_NUM_RANKS==2) ? 0x3 : 0x1)" **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_NUM_RANKS" + 3

Table 3-80 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
3	sw_init_int	R/W	Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4/5, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. In LPDDR4 dual channel mode, note that this must be programmed to both channels beforehand. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. ■ 0 - Software intervention is not allowed ■ 1 - Software intervention is allowed Don't Care for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2:1			**Reserved Field:** Yes
0	mr_type	R/W	Indicates whether the mode register operation is read or write. ■ 0 - Write ■ 1 - Read Only used for LPDDR4/LPDDR5/DDR4. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.6 MRCTRL1

- **Name:** Mode Register Read/Write Control Register 1
- **Description:** Mode Register Read/Write Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10084
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

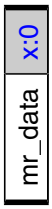


Table 3-81 Fields for Register: MRCTRL1

Bits	Name	Memory Access	Description
x:0	mr_data	R/W	Mode register write data for DDR4 mode. For LPDDR4/5, MRCTRL1[15:0] are interpreted as ■ [15:8] MR Address ■ [7:0] MR data for writes, don't care for read For PPR, this is used for row address field in the ACT command of the PPR sequence. Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW access in DDR5). **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.7 MRSTAT

- **Name:** Mode Register Read/Write Status Register
- **Description:** Mode Register Read/Write Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10090
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

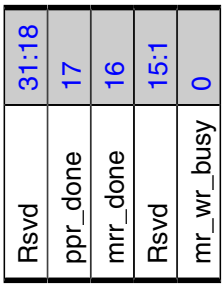


Table 3-82 Fields for Register: MRSTAT

Bits	Name	Memory Access	Description
31:18			**Reserved Field:** Yes
17	ppr_done	R	Indicate part of DDR4 or LPDDR5 PPR operation which is triggered by MRCTRL0.ppr_en is done. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	mrr_done	R	This signal goes high when the controller received MRR data which is triggered by MRCTRL0.mr_wr. This signal is cleared by mrr_done_clr **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:1			**Reserved Field:** Yes

Table 3-82 Fields for Register: MRSTAT (continued)

Bits	Name	Memory Access	Description
0	mr_wr_busy	R	The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when 'MRSTAT.mr_wr_busy' is high. ■ 0 - Indicates that the SoC core can initiate a mode register write operation ■ 1 - Indicates that mode register write operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.8 MRRDATA0

- **Name:** Mode Register Read Data 0
- **Description:** Mode Register Read Data 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10094
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

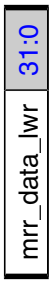


Table 3-83 Fields for Register: MRRDATA0

Bits	Name	Memory Access	Description
31:0	mrr_data_lwr	R	MRR data for DQ[31:0] This register is updated when the controller issued MRR command triggered by MRCTRL register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.9 MRRDATA1

- **Name:** Mode Register Read Data 1
- **Description:** Mode Register Read Data 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10098
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

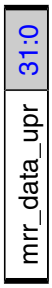


Table 3-84 Fields for Register: MRRDATA1

Bits	Name	Memory Access	Description
31:0	mrr_data_upr	R	MRR data for DQ[63:32] This register is updated when the controller issued MRR command triggered by MRCTRL register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.10 DERATECTL0

- **Name:** Temperature Derate Control Register 0
- **Description:** Temperature Derate Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10100
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

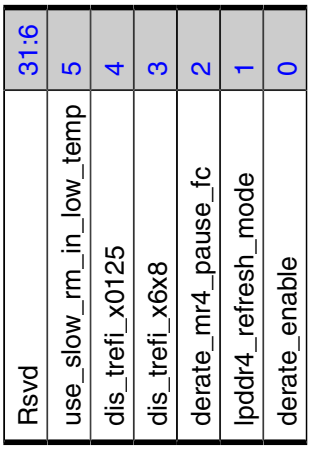


Table 3-85 Fields for Register: DERATECTL0

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5	use_slow_rm_in_low_temp	R/W	Select the refresh multiplier in low temperature operating limit exceeded. - 0 - Use 1x refresh multiplier - 1 - Use slow refresh multiplier In LPDDR5 mode, if this register value is 1 and DERATECTL0.dis_trefi_x6x8 is 0, the controller behaves as the refresh multiplier is 8x when MR4 OP[4:0]=5'b00000. If this register value is 1 and DERATECTL0.dis_trefi_x6x8 is 1, the controller behaves as the refresh multiplier is 4x when MR4 OP[4:0]=5'b00000 In LPDDR4 mode, if this register value is 1, the controller behaves as the refresh multiplier is 4x when MR4 OP[2:0]=3'b000 This register is valid only when DERATECTL0.derate_enable=1. **Value After Reset:** 0x1 **Programming Mode:** Static

Table 3-85 Fields for Register: DERATECTL0 (continued)

Bits	Name	Memory Access	Description
4	dis_trefi_x0125	R/W	Disables 0.125 x tREFI refresh rate for derating. When this register field is set to 1, controller behaves like 0.25 x tREFI refresh rate mode although in 0.125 x tREFI refresh rate mode. And controller asserts interrupt signal "derate_temp_limit_intr" when receives MR4 OP[4:0] = 01110 or 01111. ■ 0 - Enable 0.125 x tREFI refresh rate ■ 1 - Disable 0.125 x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. If RFSHMOD0.per_bank_refresh=1 and DERATECTL0.derate_enable=1 in LPDDR5, RFSHMOD0.auto_refab_en must be greater than '0' to set this register to '0'. Contact Synopsys for more information. **Value After Reset:** 0x0 **Programming Mode:** Static
3	dis_trefi_x6x8	R/W	Disables 8x tREFI and 6x tREFI refresh rate for derating. When this register field is set to 1, controller behaves like 4x tREFI refresh rate mode even though in 8x tREFI and 6x tREFI mode. ■ 0 - Enable 6x tREFI and 8x tREFI refresh rate ■ 1 - Disable 6x tREFI and 8x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. This register bit is recommended to be '0' if device supports JESD209-5A or later. For device only supports JESD209-5, set to '1'. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related
2	derate_mr4_pause_fc	R/W	Pauses automatic MRR to MR4. For more details, see description of DERATECTL0.derate_enable. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	lpddr4_refresh_mode	R/W	Selects the LPDDR4 refresh mode ■ 0 - Legacy refresh mode ■ 1 - Modified refresh mode (Unsupported) **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-85 Fields for Register: DERATECTL0 (continued)

Bits	Name	Memory Access	Description
0	derate_enable	R/W	Enables derating ■ 0 - Timing parameter derating is disabled ■ 1 - Timing parameter derating is enabled using MR4 read value. Note that, once DERATECTL0.derate_enable is set to 1, it has to keep 1. Otherwise, the refresh rate and other timing parameters revert to their nominal values. To stop automatic MRR to MR4 temporarily after setting DERATECTL0.derate_enable =1, DERATECTL0.derate_mr4_pause_fc needs to be set to 1 without changing DERATECTL0.derate_enable. Setting DERATECTL0.derate_mr4_pause_fc=0 without changing DERATECTL0.derate_enable restarts automatic MRR to MR4. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.11 DERATECTL1

- **Name:** Temperature Derate Control Register 1
- **Description:** Temperature Derate Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10104
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

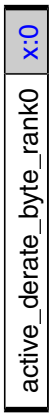


Table 3-86 Fields for Register: DERATECTL1

Bits	Name	Memory Access	Description
x:0	active_derate_byte_rank0	R/W	Indicates which byte of the MRR data is used for derating in rank0. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them This register only supports LPDDR4, LPDDR5 and DDR5. For LPDDR4 and LPDDR5: Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DERATECTL0.derate_enable=1. For DDR5: Valid width is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. The bit[n]=1 means the corresponding DDR5 device is enabled for TCR check, while 0 means disabled. Note: When data_bus_width Half or Quarter, only half or Quarter of MEMC_DRAM_TOTAL_DATA_WIDTH are valid. Note: In Dual Channel configuration, this register applies to both channels, and each channel take in charge its DQ respectively. Note: DERATECTL0 is not applicable for DDR5/4. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/4" - 1

3.2.12 DERATECTL2

- **Name:** Temperature Derate Control Register 2
- **Description:** Temperature Derate Control Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10108
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1 && MEMC_NUM_RANKS>1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

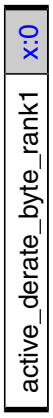


Table 3-87 Fields for Register: DERATECTL2

Bits	Name	Memory Access	Description
x:0	active_derate_byte_rank1	R/W	Indicates which byte of the MRR data is used for derating in rank1. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them. This register only supports LPDDR4, LPDDR5 and DDR5. For LPDDR4 and LPDDR5 : Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DERATECTL0.derate_enable=1. For DDR5 : Valid width is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. The bit[n]=1 means the corresponding DDR5 device is enabled for TCR check, while 0 means disabled. Note: When data_bus_width Half or Quarter, only half or Quarter of MEMC_DRAM_TOTAL_DATA_WIDTH are valid. Note: In Dual Channel configuration, this register applies to both channels, and each channel take in charge its DQ respectively. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/4" - 1

3.2.13 DERATECTL3

- **Name:** Temperature Derate Control Register 3
- **Description:** Temperature Derate Control Register 3
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1010c
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1 && MEMC_NUM_RANKS>2

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

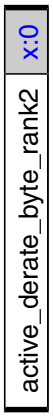


Table 3-88 Fields for Register: DERATECTL3

Bits	Name	Memory Access	Description
x:0	active_derate_byte_rank2	R/W	Indicates which byte of the MRR data is used for derating in rank2. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them. This register only supports DDR5/LPDDR. Valid width for DDR5/LPDDR is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. The bit[n]=1 means the corresponding DDR5/LPDDR device is enabled for TCR check, while 0 means disabled. Note: When data_bus_width Half or Quarter, only half or Quarter of MEMC_DRAM_TOTAL_DATA_WIDTH are valid. Note: In Dual Channel configuration, this register applies to both channels, and each channel take in charge its DQ respectively. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/4" - 1

3.2.14 DERATECTL4

- **Name:** Temperature Derate Control Register 4
- **Description:** Temperature Derate Control Register 4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10110
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1 && MEMC_NUM_RANKS>2

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

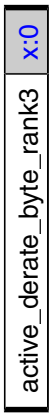


Table 3-89 Fields for Register: DERATECTL4

Bits	Name	Memory Access	Description
x:0	active_derate_byte_rank3	R/W	Indicates which byte of the MRR data is used for derating in rank3. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them. This register only supports DDR5/LPDDR. Valid width for DDR5/LPDDR is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. The bit[n]=1 means the corresponding DDR5/LPDDR device is enabled for TCR check, while 0 means disabled. Note: When data_bus_width Half or Quarter, only half or Quarter of MEMC_DRAM_TOTAL_DATA_WIDTH are valid. Note: In Dual Channel configuration, this register applies both channels, and each channel take in charge its DQ respectively. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/4" - 1

3.2.15 DERATECTL5

- **Name:** Temperature Derate Control Register 5
- **Description:** Temperature Derate Control Register 5
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10114
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

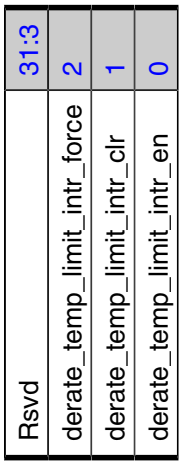


Table 3-90 Fields for Register: DERATECTL5

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	derate_temp_limit_intr_force	R/W1C	Interrupt force bit for derate_temp_limit_intr. Setting this register to 1 will cause the derate_temp_limit_intr output pin to be asserted. At the end of the interrupt force operation, the DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	derate_temp_limit_intr_clr	R/W1C	Interrupt clear bit for derate_temp_limit_intr. At the end of the interrupt clear operation, the DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-90 Fields for Register: DERATECTL5 (continued)

Bits	Name	Memory Access	Description
0	derate_temp_limit_intr_en	R/W	Interrupt enable bit for derate_temp_limit_intr output pin. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.16 DERATECTL6

- **Name:** Temperature Derate Control Register 6
- **Description:** Temperature Derate Control Register 6
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10118
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

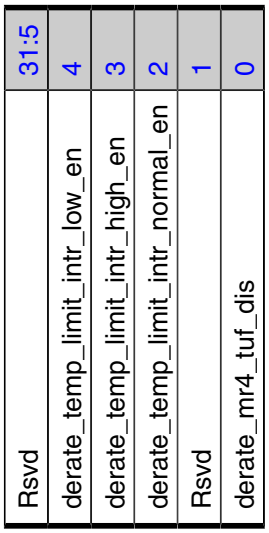


Table 3-91 Fields for Register: DERATECTL6

Bits	Name	Memory Access	Description
31:5			**Reserved Field:** Yes
4	derate_temp_limit_intr_low_en	R/W	Enable low temperature limit interrupt programmed by DERATECTL6.derate_low_temp_limit. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

Table 3-91 Fields for Register: DERATECTL6 (continued)

Bits	Name	Memory Access	Description
3	derate_temp_limit_intr_high_en	R/W	Enable high temperature limit interrupt programmed by DERATECTL6.derate_high_temp_limit. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
2	derate_temp_limit_intr_normal_en	R/W	Enable normal temperature interrupt when detected temperature is back to normal status from either high temperature limit or low temperature limit. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4
1			**Reserved Field:** Yes
0	derate_mr4_tuf_dis	R/W	Disable use of MR4 TUF flag (MR4[7]) bit. ■ 0 - Use MR4 TUF flag (MR4[7]) ■ 1 - Do not use MR4 TUF Flag (MR4[7]) It is recommended to set this register to 1. This affects both the periodic refresh rate update and asserting interrupt signal derate_temp_limit_intr. (i.e. In derate_mr4_tuf_dis==1, the controller can update the refresh rate, and assert the derate_temp_limit_intr if it exceeds the thresholds irrespective of the value of TUF flag.) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.2.17 DERATESTAT0

- **Name:** Temperature Derate Status Register 0
- **Description:** Temperature Derate Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10120
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

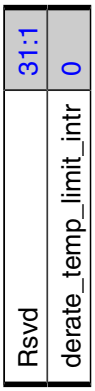


Table 3-92 Fields for Register: DERATESTAT0

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	derate_temp_limit_intr	R	Derate temperature interrupt indicating SDRAM temperature operating limit is exceeded. In LPDDR4, this register field is set to 1 when the value read from MR4[2:0] is 3'b000 or 3'b111. In LPDDR5, this register field is set to 1 when the value read from MR4[4:0] is 5'b00000 or 5'b11111 or invalid value. In DDR5, this register field is set to 1 when the value read from MR4[2:0] is the thresholds programmed by DERATECTL6.derate_low_temp_limit and DERATECTL6.derate_high_temp_limit. Cleared by register DERATECTL5.derate_temp_limit_intr_clr. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Static

3.2.18 DERATEDBGCTL

- **Name:** Temperature Derate Debug Contrl Register
- **Description:** Temperature Derate Debug Contrl Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10128
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

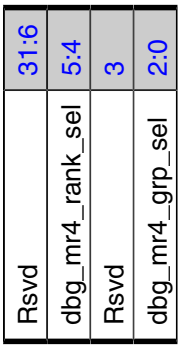


Table 3-93 Fields for Register: DERATEDBGCTL

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:4	dbg_mr4_rank_sel	R/W	MR4 rank select in case of multi ranks **Value After Reset:** 0x0 **Programming Mode:** Static
3			**Reserved Field:** Yes
2:0	dbg_mr4_grp_sel	R/W	For DDR5, MR4 data group select based on 4 device MRR read data. For LPDDR54, this is used to select MR4 data on the upper side device or the lower side device to display on DERATEDBGSTAT register. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.19 DERATEDBGSTAT

- **Name:** Temperature Derate Debug Status Register
- **Description:** Temperature Derate Debug Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1012c
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

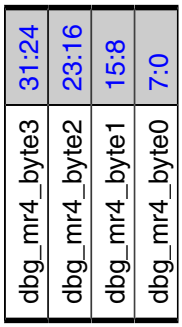


Table 3-94 Fields for Register: DERATEDBGSTAT

Bits	Name	Memory Access	Description
31:24	dbg_mr4_byte3	R	Byte 3 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 7 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

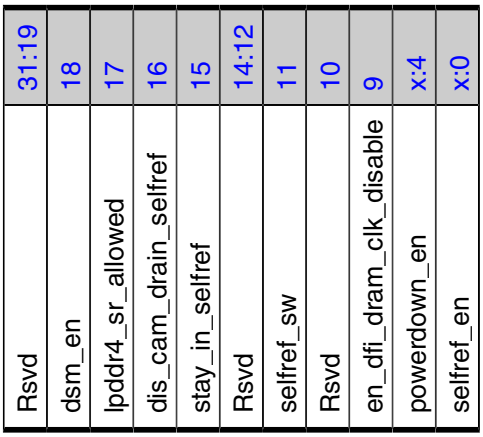
Table 3-94 Fields for Register: DERATEDBGSTAT (continued)

Bits	Name	Memory Access	Description
23:16	dbg_mr4_byte2	R	Byte 2 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 6 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8	dbg_mr4_byte1	R	Byte 1 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1). This register shows the byte 5 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:0	dbg_mr4_byte0	R	Byte 0 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 4 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.20 PWRCTL

- **Name:** Low Power Control Register
- **Description:** Low Power Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10180
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:19	18	17	16	15	14:12	11	10	9	x:4	x:0
Rsvd	dsm_en	lpddr4_sr_allowed	dis_cam_drain_selfref	stay_in_selfref	Rsvd	selfref_sw	Rsvd	en_dfi_dram_clk_disable	powerdown_en	selfref_en

Table 3-95 Fields for Register: PWRCTL

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	dsm_en	R/W	A value of 1 to this register causes system to move to Deep Sleep Mode state immediately. ■ 1 - Entry to Deep Sleep Mode ■ 0 - Exit from Deep Sleep Mode **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-95 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
17	lpddr4_sr_allowed	R/W	Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register should be set to '1' if any of PHYMSTR, PPT or HWFFC feature is enabled. This register field cannot be modified while PWRCTL.selfref_sw==1. ■ 0 - SR-PD -> SR -> SR-PD not allowed ■ 1 - SR-PD -> SR -> SR-PD allowed Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	dis_cam_drain_selfref	R/W	Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. ■ 0 - CAMs must be empty before entering SR ■ 1 - CAMs are not emptied before entering SR (unsupported) Note, PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. PWRCTL.dis_cam_drain_selfref=0 is required. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15	stay_in_selfref	R/W	Self refresh state is an intermediate state to enter to Self refresh power down state or exit Self refresh power down state for LPDDR4/5. This register controls transition from the Self refresh state. ■ 1 - Prohibit transition from Self refresh state ■ 0 - Allow transition from Self refresh state **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14:12			**Reserved Field:** Yes
11	selfref_sw	R/W	A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating mode. This is referred to as Software Entry/Exit to Self Refresh. ■ 1 - Software Entry to Self Refresh ■ 0 - Software Exit from Self Refresh **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-95 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
10			**Reserved Field:** Yes
9	en_dfi_dram_clk_disable	R/W	Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR4, can be asserted in following: ■ in Self Refresh ■ in Maximum Power Saving Mode In LPDDR4/LPDDR5, can be asserted in following: ■ in Self Refresh Power Down ■ in Power Down ■ during Normal operation (Clock Stop) In DDR5, can be asserted in following: ■ in Self Refresh In DDR5 (L)RDIMM, the value of this field need to be same as DIMMCTL.dimm_selfref_clock_stop_mode. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:4	powerdown_en	R/W	If true then the DDRCTL goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[4] is used. For DDR5, powerdown per rank enable is supported. ■ bit[4] - rank 0 powerdown_en ■ bit[5] - rank 1 powerdown_en ■ bit[6] - rank 2 powerdown_en ■ bit[7] - rank 3 powerdown_en **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? MEMC_NUM_RANKS : 1" + 3

Table 3-95 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
x:0	selfref_en	R/W	If true then the DDRCTL puts the SDRAM per rank into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[0] is used. For DDR5, self-refresh per rank enable is provided. Current self-refresh need to be enabled for all ranks. For DDR5 (L)RDIMM, self-refresh need to be enabled for all ranks of both channels. ■ bit[0] - rank 0 selfref_en ■ bit[1] - rank 1 selfref_en ■ bit[2] - rank 2 selfref_en ■ bit[3] - rank 3 selfref_en **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? MEMC_NUM_RANKS : 1" - 1

3.2.21 HWLPCTL

- **Name:** Hardware Low Power Control Register
- **Description:** Hardware Low Power Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10184
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

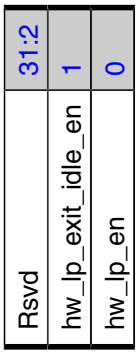


Table 3-96 Fields for Register: HWLPCTL

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	hw_lp_exit_idle_en	R/W	When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). **Value After Reset:** 0x1 **Testable:** readOnly **Programming Mode:** Static
0	hw_lp_en	R/W	Enable for Hardware Low Power Interface. This field should be updated only when system in SW self-refresh. Please follow Programming guide for configure this field. Please refer to the section of Hardware Low-Power Interfaces in databook. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.22 CLKGATECTL

- **Name:** clock gate control
- **Description:** clock gate control
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1018c
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

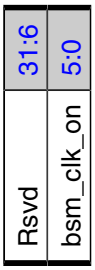


Table 3-97 Fields for Register: CLKGATECTL

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:0	bsm_clk_on	R/W	Indicates whether the output signal bsm_clk_en [MEMC_NUM_RANKS-1:0] become 0 for each corresponding DDRCTL internal state: ■ 0: bsm_clk_en become 0 in case where DDRCTL is in corresponding state described below ■ 1: bsm_clk_en remain 1 in case where DDRCTL is in corresponding state The bsm_clk_en [MEMC_NUM_RANKS-1:0] indicates that clock can be removed when corresponding rank of this signal is 0. Each corresponding DDRCTL internal state is as follows: ■ [0] Unpopulated rank control ■ [1] Controller initialization state (until dfi0_init_start/dfi0_init_complete handshake is done) ■ [2] Self Refresh mode ■ [3] Self Refresh Powerdown mode ■ [4] Powerdown mode ■ [5] Deep Sleep Mode (LPDDR5 Only) bit[5:1] indicates behavior of the bsm_clk_en for each corresponding DDRCTL internal state. For example, if this field is set to 6'b00_0100, bsm_clk_en becomes 1 when it is in self refresh mode. This implies that bsm_clk is not removed while it is in self refresh mode, but the bsm_clk is removed by external clock gating logic in other modes above.

Table 3-97 Fields for Register: CLKGATECTL (continued)

Bits	Name	Memory Access	Description
			If bit 0 (Unpopulated rank control) is set to 1, behavior of the bsm_clk_en is determined by other fields in this register irrespective of MSTR.active_ranks. If the bsm_clk_en[1]=0 is needed in case of single rank (MSTR.active_ranks=1), bit 0 has to be set to 0. To maximize power-saving, this field needs to be set to 6'b00_0000. **Value After Reset:** 0x3f **Programming Mode:** Static

3.2.23 RFSHMOD0

- **Name:** Refresh Mode Register 0
- **Description:** Refresh Mode Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10200
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

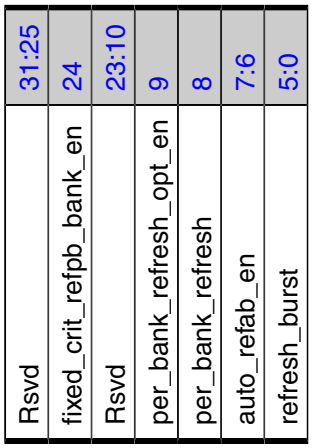


Table 3-98 Fields for Register: RFSHMOD0

Bits	Name	Memory Access	Description
31:25			**Reserved Field:** Yes
24	fixed_crit_refpb_bank_en	R/W	Target bank selection mode for critical per-bank refresh (REFpb). When this is set to 1, the target bank is fixed until the REFPb is scheduled. When this is set to 0, the target bank is immediately updated if higher priority bank is found even before the REFpb is scheduled. Any transaction to the target bank blocks any transaction. ■ 0 - Disabled (bank address for critical REFpb is updated dynamic) ■ 1 - Enabled (bank address for critical REFpb is fixed) This register field is valid when RFSHMOD0.per_bank_refresh=1 FOR PERFORMANCE ONLY **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-98 Fields for Register: RFSHMOD0 (continued)

Bits	Name	Memory Access	Description
23:10			**Reserved Field:** Yes
9	per_bank_refresh_opt_en	R/W	■ 1 - Enable Per bank refresh optimization ■ 0 - Disable Per bank refresh optimization This register field is valid when RFSHMOD0.per_bank_refresh=1 **Value After Reset:** 0x0 **Programming Mode:** Static
8	per_bank_refresh	R/W	■ 1 - Per bank refresh ■ 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. **Value After Reset:** 0x0 **Programming Mode:** Static
7:6	auto_refab_en	R/W	Enables automatic switching from per-bank to all-bank refresh when the derated refresh period is small. ■ 0 - Disable automatic switching ■ 1 - Enable automatic switching when the derated refresh period is tREFI/2 or lower ■ 2 - Enable automatic switching when the derated refresh period is tREFI/4 or lower ■ 3 - Enable automatic switching when the derated refresh period is tREFI/8 Automatically switches back to per-bank refresh when the derated refresh period is no longer small. This register should be programmed to 2'b00 if RFSHMOD0.per_bank_refresh = 1'b0. **Value After Reset:** 0x0 **Programming Mode:** Static
5:0	refresh_burst	R/W	The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. ■ 0 - single refresh ■ 1 - burst-of-2 refresh ■ 7 - burst-of-8 refresh In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode.

Table 3-98 Fields for Register: RFSHMOD0 (continued)

Bits	Name	Memory Access	Description
			In DDR5 mode, according to Fine Granularity feature, 4 refreshes can be postponed in 1X mode and 8 refreshes can be postponed in 2X mode. In DDR5 mode, if self-refresh operation is expected, then this field shall not be set to the maximum number, for example, according to Fine Granularity feature, it should be smaller than 8 in 2X mode. In LPDDR5 mode, RFSHMOD0.refresh_burst should be greater than or equal to 1 (If RFSHMOD0.per_bank_refresh=1 and RFSHMOD0.auto_refab_en>0 then RFSHMOD0.refresh_burst>7) when DERATECTL0.derate_enable=1 and 24Gb or 32Gb device. In LPDDR4 or LPDDR5 mode, If RFSHMOD0.per_bank_refresh=1 ,RFSHMOD0.refresh_burst should be greater than or equal to 7. In per-bank refresh mode of LPDDR4/5 (RFSHMOD0.per_bank_refresh = 1), 56 refreshes can be postponed. If using PHY-initiated updates or PPT2 (LPDDR only), care must be taken in the setting of RFSHMOD0.refresh_burst, to ensure that tRFCmax and tREFI are not violated due to PHY-initiated updates or PPT2 occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until they complete. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related

3.2.24 RFSHCTL0

- **Name:** Refresh Control Register 0
- **Description:** Refresh Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10208
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

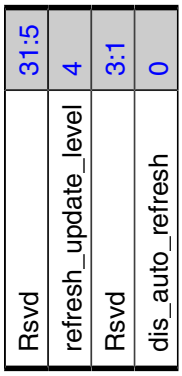


Table 3-99 Fields for Register: RFSHCTL0

Bits	Name	Memory Access	Description
31:5			**Reserved Field:** Yes
4	refresh_update_level	R/W	Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). In DDR5 mode, this can be toggled during self-refresh mode and MPSM in OPS state. The refresh register(s) are automatically updated when exiting reset. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3:1			**Reserved Field:** Yes

Table 3-99 Fields for Register: RFSHCTL0 (continued)

Bits	Name	Memory Access	Description
0	dis_auto_refresh	R/W	When '1', disable auto-refresh generated by the DDRCTL. When auto-refresh is disabled, the SoC core must generate refreshes using the registers OPREFCTRL*.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the DDRCTL. If DDR4 CA parity retry is enabled (RETRYCTL0.capar_retry_enable = 1), disable auto-refresh is not supported, and this bit must be set to '0'. If FGR mode is enabled (RFSHMOD1.fgr_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly in non-DDR5 mode, and changeable during INIT/DBG/BIST state or self-refresh mode and MPSM during OPS state in DDR5 mode. **Value After Reset:** 0x0 **Programming Mode:** Dynamic - Refresh Related

3.2.25 RFMMOD0

- **Name:** RFM Mode Register 0
- **Description:** RFM Mode Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10220
- **Exists:** DDRCTL_LPDDR_RFM==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31:29	28:24	23:20	19:18	17:16	15:13	12:8	7:5	4	3:1	0
Rsvd	rfmth_rm_thr	Rsvd	raadec	raamult	Rsvd	raaimt	Rsvd	rfmsbc	Rsvd	rfm_en

Table 3-100 Fields for Register: RFMMOD0

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	rfmth_rm_thr	R/W	Threshold of RM (Refresh Multiplier) to disable RFM command. When current RM which is read from MR4:OP[4:0] in LPDDR5 or Refresh rate which is read from MR4:OP[2:0] in LPDDR4 is greater than or equal to this, RFM command is disabled irrespective of RAA count. This is calculated from max. interval between two REF <= RFMTH requirement. **Value After Reset:** 0xa **Programming Mode:** Quasi-dynamic Group 3
23:20			**Reserved Field:** Yes
19:18	raadec	R/W	RAADEC: RAA Count Decrement per RFM Command as programmed in MR57:OP[1:0] of LPDDR5 or MR36:OP[1:0] of LPDDR4. ■ 2'b00: RAAIMT ■ 2'b01: RAAIMT * 1.5 ■ 2'b10: RAAIMT * 2 ■ 2'b11: RAAIMT * 4 (LPDDR5 only) **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 3

Table 3-100 Fields for Register: RFMMOD0 (continued)

Bits	Name	Memory Access	Description
17:16	raamult	R/W	RAAMULT: Rolling Accumulated ACT Multiplier as programmed in MR27:OP[7:6] of LPDDR5 or MR24:OP[7:6] of LPDDR4. ■ 2'b00: 2X ■ 2'b01: 4X ■ 2'b10: 6X ■ 2'b11: 8X **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 3
15:13			**Reserved Field:** Yes
12:8	raaimt	R/W	RAAIMT: Rolling Accumulated ACT Initial Management Threshold as programmed in MR27:OP[5:1] of LPDDR5 or MR24:OP[5:1] of LPDDR4. ■ 5'b00000: Invalid ■ 5'b00001: 8 ■ 5'b00010: 16 : ■ 5'b11110: 240 ■ 5'b11111: 248 **Value After Reset:** 0x1 **Programming Mode:** Quasi-dynamic Group 3
7:5			**Reserved Field:** Yes
4	rfmsbc	R/W	RFMSBC: Single-Bank Counters Implemented (LPDDR5 only). The value should be determined based on MR57:OP[5:4] of LPDDR5. ■ 1'b0: One RAA counter per two banks (1 of 8), MR57:OP[5:4]==2'b00 ■ 1'b1: One RAA counter per one bank (1 of 16), MR57:OP[5:4]==2'b01 **Value After Reset:** 0x0 **Programming Mode:** Static
3:1			**Reserved Field:** Yes
0	rfm_en	R/W	RFM enable in LPDDR5/4 mode. This should be programmed based on MR27:OP[0] (RFM Required) of LPDDR5 or MR24:OP[0] (RFM Required) of LPDDR4. If ARFM is used, this should be set to 1 regardless of MR27:OP[0]. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 3

3.2.26 RFMMOD1

- **Name:** RFM Mode Register 1
- **Description:** RFM Mode Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10224
- **Exists:** DDRCTL_LPDDR_RFM==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

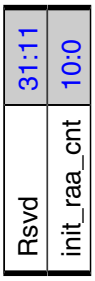


Table 3-101 Fields for Register: RFMMOD1

Bits	Name	Memory Access	Description
31:11			**Reserved Field:** Yes
10:0	init_raa_cnt	R/W	Initial value of RAA counters in the controller. Valid range of this value is between 0 and RAAMMT. If this is set to greater than 0, the DDRCTL issues RFM command before RAA counter in the SDRAM reaches up to RAAMMT. This is basically set to 0 (default value), and set to RAAMMT in power-removal sequence (See Power Removal Flog section for details). **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.27 RFMCTL

- **Name:** RFM Control Register
- **Description:** RFM Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10228
- **Exists:** DDRCTL_LPDDR_RFM==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

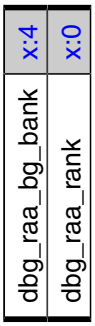


Table 3-102 Fields for Register: RFMCTL

Bits	Name	Memory Access	Description
x:4	dbg_raa_bg_bank	R/W	BG/bank address for status register RFMSTAT.dbg_raa_cnt. This register is debug purpose only. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "(DDRCTL_LPDDR_RFMSBC_EN==1) ? MEMC_BG_BANK_BITS : (MEMC_BG_BANK_BITS-1)" + 3
x:0	dbg_raa_rank	R/W	Rank address for status register RFMSTAT.dbg_raa_cnt. This register is debug purpose only. Bit assignment is defined as below. LPDDR5 not single-bank mode: ■ {BG0, BA1, BA0} (BG mode) ■ {BA2, BA1, BA0} (16B mode) LPDDR5 single-bank mode: ■ {BG1, BG0, BA1, BA0} (BG mode) ■ {BA3, BA2, BA1, BA0} (16B mode) LPDDR4: ■ {BA2, BA1, BA0} **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" - 1

3.2.28 RFMSTAT

- **Name:** RFM Status Register
- **Description:** RFM Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1022c
- **Exists:** DDRCTL_LPDDR_RFM==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

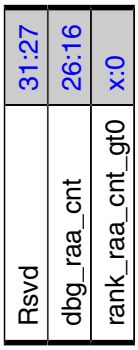


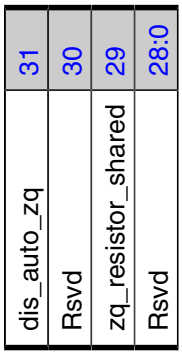
Table 3-103 Fields for Register: RFMSTAT

Bits	Name	Memory Access	Description
31:27			**Reserved Field:** Yes
26:16	dbg_raa_cnt	R	Internal value of RAA counter where rank is selected by RFMCTL.dbg_raa_rank and BG/bank is selected by RFMCTL.dbg_raa_bg_bank. This register is debug purpose only. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:0	rank_raa_cnt_gt0	R	Status of RAA counter per rank. When at least one RAA counter of all banks in rank is greater than 0, this is set to 1. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_NUM_RANKS" - 1

3.2.29 ZQCTL0

- **Name:** ZQ Control Register 0
- **Description:** ZQ Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10280
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31	30	29	28:0
dis_auto_zq	Rsvd	zq_resistor_shared	Rsvd

Table 3-104 Fields for Register: ZQCTL0

Bits	Name	Memory Access	Description
31	dis_auto_zq	R/W	■ 1 - Disable DDRCTL generation of ZQCS/MPC(ZQ calibration) command. Register OPCTRLCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. ■ 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQSET1TMG1.t_zq_short_interval_x1024. This register field only applies to DDR4, LPDDR4, and LPDDR5. For DDR5, see PASCTL7~PASCTL10 registers If LPDDR5 is used and HWFFC is not ongoing (HWFFCSTAT.hwffc_in_progress is not '1'), single ZQCal latch command will be sent right after this register is toggled to '0'. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30			**Reserved Field:** Yes
29	zq_resistor_shared	R/W	■ 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap. ■ 0 - ZQ resistor is not shared. If LPDDR5 is used, this register needs to be set to "0". **Value After Reset:** 0x0 **Programming Mode:** Static
28:0			**Reserved Field:** Yes

3.2.30 ZQCTL1

- **Name:** ZQ Control Register 1
- **Description:** ZQ Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10284
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

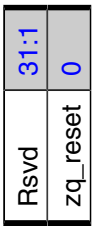


Table 3-105 Fields for Register: ZQCTL1

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	zq_reset	R/W1S	Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the DDRCTL automatically clears this bit. It is recommended NOT to set this register bit if in Init, in SR-Powerdown or Deep Sleep Modes. For SR-Powerdown it will be scheduled after SRPD has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.2.31 ZQCTL2

- **Name:** ZQ Control Register 2
- **Description:** ZQ Control Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10288
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

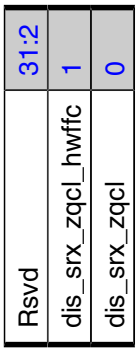


Table 3-106 Fields for Register: ZQCTL2

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	dis_srx_zqcl_hwffc	R/W	■ 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit after HWFFC with HWFFCCTL.hwffc_mode=1 procedure. ■ 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit after HWFFC with HWFFCCTL.hwffc_mode=1 procedure. This value takes effect independentliy from dis_srx_zqcl. Even if dis_srx_zqcl is 1, DDRCTL will issue ZQ calibration after the HWFFC with HWFFCCTL.hwffc_mode=1 procedure if this value is 0. This is only present for designs supporting LPDDR54 HWFFC. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 2, Group 4
0	dis_srx_zqcl	R/W	■ 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. ■ 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting DDR4 or DDR5 or LPDDR4 or LPDDR5 devices. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2, Group 4

3.2.32 ZQSTAT

- **Name:** ZQ Status Register
- **Description:** ZQ Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1028c
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-107 Fields for Register: ZQSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	zq_reset_busy	R	SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ZQ Reset operation ■ 1 - Indicates that ZQ Reset operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.33 DQSOSCRUNTIME

- **Name:** DQS/WCK Oscillator Runtime Register
- **Description:** DQS/WCK Oscillator Runtime Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10300
- **Exists:** LPDDR45_DQSOSC_EN==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

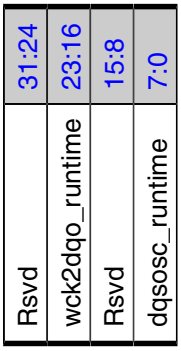


Table 3-108 Fields for Register: DQSOSCRUNTIME

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes

Table 3-108 Fields for Register: DQSOSCRUNTIME (continued)

Bits	Name	Memory Access	Description
23:16	wck2dqo_runtime	R/W	WCK2DQO interval timer run time setting as programmed in MR40 for LPDDR5.This field must be non zero. ■ 0x0 - Interval timer stop via MPC command (not supported) ■ 0x1 - Interval timer stops automatically at 16th clocks after timer start ■ 0x2 - Interval timer stops automatically at 32nd clocks after timer start ■ 0x3 - Interval timer stops automatically at 48th clocks after timer start ■ 0x4 - Interval timer stops automatically at 64th clocks after timer start ■ ----- Thru ---------- ■ 0x3F - Interval timer stops automatically at (63x16)th clocks after timer start ■ 0x40 to 0x7F - Interval timer stops automatically at 2048th clocks after timer start ■ 0x80 to 0xBF - Interval timer stops automatically at 4096th clocks after timer start ■ 0xC0 to 0xFF - Interval timer stops automatically at 8192nd clocks after timer start This register field is only applicable for designs supporting LPDDR5 SDRAM memories. It is don't care for LPDDR4 SDRAM memories. Unit: DRAM clock cycles. **Value After Reset:** 0x40 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
15:8			**Reserved Field:** Yes

Table 3-108 Fields for Register: DQSOSCRUNTIME (continued)

Bits	Name	Memory Access	Description
7:0	dqsosc_runtime	R/W	LPDDR4: DQS interval timer run time setting as programmed in MR23 LPDDR5: WCK2DQI interval timer run time setting as programmed in MR37 This field must be non zero. ■ 0x0 - Interval timer stop via MPC command (not supported) ■ 0x1 - Interval timer stops automatically at 16th clocks after timer start ■ 0x2 - Interval timer stops automatically at 32nd clocks after timer start ■ 0x3 - Interval timer stops automatically at 48th clocks after timer start ■ 0x4 - Interval timer stops automatically at 64th clocks after timer start ■ ----- Thru ---------- ■ 0x3F - Interval timer stops automatically at (63x16)th clocks after timer start ■ 0x40 to 0x7F - Interval timer stops automatically at 2048th clocks after timer start ■ 0x80 to 0xBF - Interval timer stops automatically at 4096th clocks after timer start ■ 0xC0 to 0xFF - Interval timer stops automatically at 8192nd clocks after timer start Unit: DRAM clock cycles. **Value After Reset:** 0x40 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

3.2.34 DQSOSCSTAT0

- **Name:** DQS/WCK Oscillator Status Register 0
- **Description:** DQS/WCK Oscillator Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10304
- **Exists:** LPDDR45_DQSOSC_EN==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

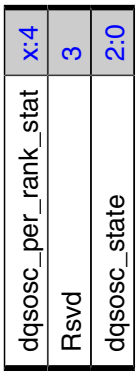


Table 3-109 Fields for Register: DQSOSCSTAT0

Bits	Name	Memory Access	Description
x:4	dqsosc_per_rank_stat	R	DQS/WCK Oscillator per rank status. This bit is set to 0 when DQSOSCCTL0.dqsosc_enable is set to 1, and set to 1 when the DQS Oscillator command sequence is started for the corresponding active rank. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** MEMC_NUM_RANKS + 3
3			**Reserved Field:** Yes

Table 3-109 Fields for Register: DQSOSCSTAT0 (continued)

Bits	Name	Memory Access	Description
2:0	dqsosc_state	R	DQS/WCK Oscillator Control State Status. ■ 000 - DQSOSC_IDLE ■ 001 - DQSOSC_START: Sending MPC ■ 010 - DQSOSC_RUNTIME: Waiting for runtime passed ■ 011 - DQSOSC_GET_RESULT1: Sending first MRR ■ 100 - DQSOSC_WAIT1: Waiting for tMRR for sending next MRR ■ 101 - DQSOSC_GET_RESULT2: Sending second MRR ■ 110 - DQSOSC_WAIT2: Waiting for tMRR or rank gap The value 0 indicates nothing is being done for DQS Oscillator. Otherwise, DQS Oscillator is running and reflects the current state of DQSOSC. It can be used for debug only to ascertain the current state of DQSOSC controller if it is stuck to one particular state. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.35 DQSOSCCFG0

- **Name:** DQSOSC Config Register 0
- **Description:** DQSOSC Config Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10308
- **Exists:** LPDDR54_DQOSC_EN_OR_MEMC_DDR5==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

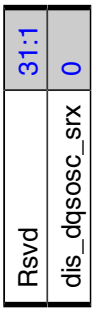


Table 3-110 Fields for Register: DQSOSCCFG0

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	dis_dqsosc_srx	R/W	■ 1 - Disable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. ■ 0 - Enable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting LPDDR4 or LPDDR5 or DDR5 devices. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

3.2.36 SCHED0

- **Name:** Scheduler Control Register 0
- **Description:** Scheduler Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10380
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

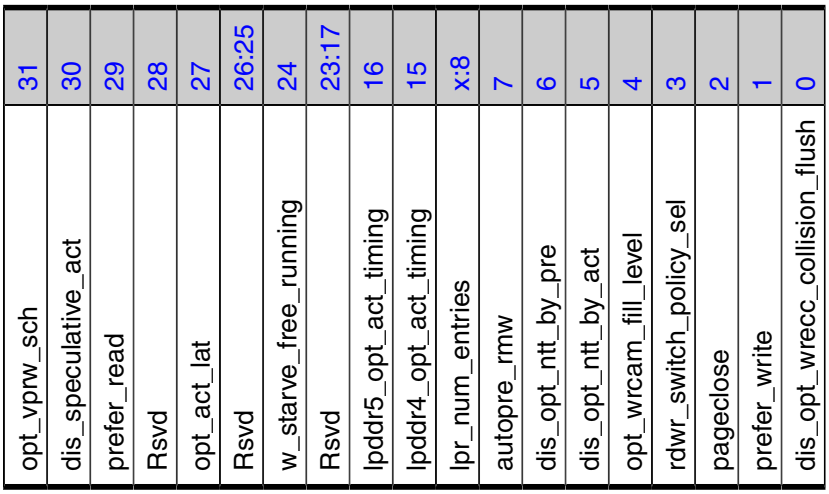


Table 3-111 Fields for Register: SCHED0

Bits	Name	Memory Access	Description
31	opt_vprw_sch	R/W	Optimize exVPR/exVPW scheduling. ■ 0 - When any exVPR/exVPW are pending on CAM, read/write command of all other traffic class are masked to be scheduled ■ 1 - When any exVPR/exVPW are pending as page-hit, read/write command of all other traffic class are masked to be scheduled Program to 1 can improve utilization as other traffic class can utilize bandwidth while pages for exVPR/exVPW are being prepared or ranks/banks for exVPR/exVPW are being refreshed, but it can delay execution of exVPR/exVPW due to delay of Activate by read/write command of other traffic class. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static

Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
30	dis_speculative_act	R/W	Disable speculative Activate. In enhanced read write switching mode, activate commands can be issued to the other direction speculatively. This may have side-effect that the page opened for RD/WR proactively may be required to be closed to serve WR/RD respectively and it can have negative impact on performance due to command bus congestion.This register can limit such a speculative activate for the other direction. ■ 0 Allow speculative activates (default) ■ 1 Limit the speculative activates This register is effective only DDR4, LPDDR4 and LPDDR5. In this version, the value 1 is not fully verified hence this register must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
29	prefer_read	R/W	Make RD preferred when RD and WR have same critical level. For better RD ltancy, it is recommended to set this register to 1 but there could be efficiency drop as a trade-off with latency. ■ 0 - Disable (Default) ■ 1 - Enable (RD is preferred when same critical level between RD and WR) This register is effective only LPDDR4 and LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
28			**Reserved Field:** Yes

Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
27	opt_act_lat	R/W	Optimize best case latency for ACT from HIF to DFI. When the register is set to 1, it may reduce ACT latency by 1 DFI clock cycle compare to the backward compatibility mode. However, as a side effect, direction selection may be inaccurate against flowchart described in databook chapter. ■ 1 - Optimized ACT latency ■ 0 - Backward compatibility mode (default) Recommended value is 0 to keep backward compatible. Please contact Synopsys if you wish to use optimized ACT latency mode. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
26:25			**Reserved Field:** Yes
24	w_starve_free_running	R/W	Write starvation timer running mode for enhance WR CAM fill level. ■ 1: Free running mode. WR starvation timer is not reset by any WR. ■ 0: Backward compatibility mode. WR starvation timer is reset by any WR. This register shall be set to 0 when SHCED0.opt_wrcam_fill_level==0 || (PERFWR1.w_max_starve==0 && SCHED0.opt_wrcam_fill_level==1). **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
23:17			**Reserved Field:** Yes

Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
16	lpddr5_opt_act_timing	R/W	Optimized ACT timing control for LPDDR5. This register is to be used for debug purpose. In LPDDR5, ACTIVATE command is composed of two commands, ACT-1 and ACT-2. When this register is set, ACT-1 can be issued "tRRD-2" cycle after previous ACT-2. If ACT-1 is issued at this timing, the controller does not issue ACT-2 at next cycle due to tRRD. ■ 0 - Disable (only for debug purpose) ■ 1 - Enable (Default) This register is ignored when MSTR0.lpddr5==0. This register field is only applicable for LPDDR5 mode. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static
15	lpddr4_opt_act_timing	R/W	Optimized ACT timing control for LPDDR4. In LPDDR4, RD/WR/ACT takes 4 cycle. To stream Read/Write, there are only 4 cycle space between Reads/Writes. If ACT is scheduled-out after RD/WR with 1, 2 or 3 cycle gap, next RD/WR may be pushed by 1, 2 or 3 cycle and create a gap on DQ. When this register is set, ACT is not scheduled-out with the gap = 1, 2 and 3 cycle. If enabled, there could be performance impact especially for random traffic. (Latency/Utilization) ■ 1 - Enable this feature ■ 0 - Disable this feature This register is ignored when MSTR0.lpddr4==0. This register field is only applicable for LPDDR4 mode. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
x:8	lpr_num_entries	R/W	Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. For HW configurations which have more than 128 deep read CAM, use SCHED6.lpr_num_entries_extend instead. **Value After Reset:** "MEMC_NO_OF_ENTRY/2" **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS" + 7
7	autopre_rmw	R/W	Select behavior of hif_cmd_autopre if a RMW is received on HIF with hif_cmd_autopre=1 ■ 1: Apply Autopre only for write part of RMW ■ 0: Apply Autopre for both read and write parts of RMW This value is not cared for CHI configuration and recommended to be set as 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
6	dis_opt_ntt_by_pre	R/W	Disable optimized NTT update by Precharge command. This register is debug purpose only. For normal operation, This register must be set to 0. ■ 1: disabled ■ 0: enabled **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
5	dis_opt_ntt_by_act	R/W	Disable optimized NTT update by Activate command. This register is debug purpose only. For normal operation, This register must be set to 0. ■ 1: disabled ■ 0: enabled **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
4	opt_wrcam_fill_level	R/W	Enable the feature of optimized write CAM fill level by switching to write when write CAM reaches certain fill level set in SCHED3.wrcam_highthresh. ■ 1: enabled ■ 0: disabled If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. It is recommended that w_max_starve is programmed as >0 value when opt_wrcam_fill_level=1 to avoid starving extremely. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static
3	rdwr_switch_policy_sel	R/W	Select read write switching policy. ■ 1: select "enhanced" read write switching policy ■ 0: select "original" read write switching policy For DDR5, only "enhanced" read write switching policy is supported. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static

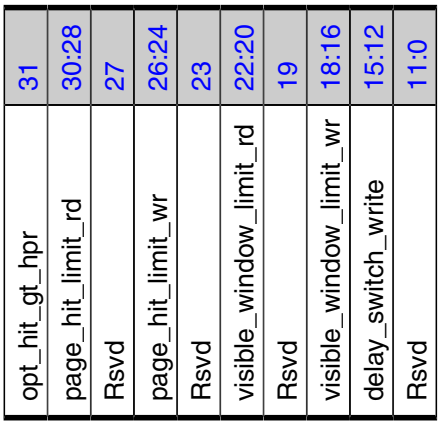
Table 3-111 Fields for Register: SCHED0 (continued)

Bits	Name	Memory Access	Description
2	pageclose	R/W	If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if SCHEDTMG0.pageclose_timer=0. Even if this register set to 1 and SCHEDTMG0.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The open page policy can be overridden by setting the per-command-autopre bit on the HIF interface (hif_cmd_autopre). The pageclose feature provides a midway between Open and Close page policies. FOR PERFORMANCE ONLY. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static
1	prefer_write	R/W	If set then the bank selector prefers writes over reads. FOR DEBUG ONLY. **Value After Reset:** 0x0 **Programming Mode:** Static
0	dis_opt_wrecc_collision_flush	R/W	In this release, this register bit is required to set to 0 in software unless otherwise advised by Synopsys. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

3.2.37 SCHED1

- **Name:** Scheduler Control Register 1
- **Description:** Scheduler Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10384
- **Exists:** MEMC_ENH_CAM_PTR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31	30:28	27	26:24	23	22:20	19	18:16	15:12	11:0
opt_hit_gt_hpr	page_hit_limit_rd	Rsvd	page_hit_limit_wr	Rsvd	visible_window_limit_rd	Rsvd	visible_window_limit_wr	delay_switch_write	Rsvd

Table 3-112 Fields for Register: SCHED1

Bits	Name	Memory Access	Description
31	opt_hit_gt_hpr	R/W	Optimize the priority between Page-hit LPR and Page-miss HPR ■ 0 - Page-miss HPR has priority (default) ■ 1 - Page-hit LPR has priority This is to choose trade-off between HPR latency and total utilization. If set to 0, HPR latency can be better than 1 because HPR has priority over LPR. If set to 1, DRAM utilization can be better than 0 because number of ACT-PRE is reduced. When this register is set to 1, recommend to enable page-hit limiter so that once page-hit limiter is expired, HPR can have priority. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-112 Fields for Register: SCHED1 (continued)

Bits	Name	Memory Access	Description
30:28	page_hit_limit_rd	R/W	Page-Hit limiter for read. When certain number of read commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. ■ 0 - Disable this feature ■ 1 - 4 commands ■ 2 - 8 commands ■ 3 - 16 commands ■ 4 - 32 commands ■ else reserved **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
27			**Reserved Field:** Yes
26:24	page_hit_limit_wr	R/W	Page-Hit limiter for write. When certain number of write commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. ■ 0 - Disable this feature ■ 1 - 4 commands ■ 2 - 8 commands ■ 3 - 16 commands ■ 4 - 32 commands ■ else reserved **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
23			**Reserved Field:** Yes

Table 3-112 Fields for Register: SCHED1 (continued)

Bits	Name	Memory Access	Description
22:20	visible_window_limit_rd	R/W	Visible window limiter for read. This is to prevent extreme starvation against other entries within a CAM. Each read CAM entry has a counter, it is set to the value programmed in this register when command is pushed and is counted-down when newer read CAM entry is scheduled-out. The counter represent starvation within RD CAM in terms of number of commands to be over taken. When the counter reaches to 0, the entry becomes expired-VPR to eliminate more starvation. ■ 0 - Disable this feature ■ 1 - 31 commands ■ 2 - 63 commands ■ 3 - 127 commands ■ 4 - 255 commands ■ 5 - 511 commands(only for RD CAM depth > 64) ■ else reserved **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
19			**Reserved Field:** Yes
18:16	visible_window_limit_wr	R/W	Visible window limiter for write. This is to prevent extreme starvation against other entries within a CAM. Each write CAM entry has a counter, it is set to the value programmed in this register when command is pushed and is counted-down when newer write CAM entry is scheduled-out. The counter represent starvation within WR CAM in terms of number of commands to be over taken. When the counter reaches to 0, the entry becomes expired-VPW to eliminate more starvation. ■ 0 - Disable this feature ■ 1 - 31 commands ■ 2 - 63 commands ■ 3 - 127 commands ■ 4 - 255 commands ■ 5 - 511 commands(only for WR CAM depth > 64) ■ else reserved **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

Table 3-112 Fields for Register: SCHED1 (continued)

Bits	Name	Memory Access	Description
15:12	delay_switch_write	R/W	delay_switch_write indicates number of cycles to delay switching read to write mode when write page-hit request is there and no read page-hit request is there. Setting higher value may reduce number of read to write switching but increase read to write turn-around time. The register indicates the number of cycles: ■ 0: no delay ■ 1: 2 cycles delay ■ 2: 4 cycles delay ■ 3: 6 cycles delay ■ 4: 8 cycles delay ■ ... ■ 15:30 cycles delay If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Unit: DFI clock **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Static
11:0			**Reserved Field:** Yes

3.2.38 SCHED3

- **Name:** Scheduler Control Register 3
- **Description:** Scheduler Control Register 3
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1038c
- **Exists:** MEMC_ENH_RDWR_SWITCH==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-113 Fields for Register: SCHED3

Bits	Name	Memory Access	Description
x:24	rd_pghit_num_thresh	R/W	Switch to read mode once number of read page-hit request exceeds the threshold set in the register during waiting tW2R. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS" + 23

Table 3-113 Fields for Register: SCHED3 (continued)

Bits	Name	Memory Access	Description
x:16	wr_pghit_num_thresh	R/W	Switch to write mode once number of write page-hit request exceeds threshold set in this register during waiting delay_switch_write timeout. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. For HW configurations which have more than 256 deep write CAM, use SCHED7.wr_pghit_num_thresh_extend instead. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS" + 15
x:8	wrcam_highthresh	R/W	The high threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_highthresh), switch to write mode and prepare banks for write direction if no Exp-VPR or read collision is there. wrcam_highthresh must be set to a smaller value than wrcam_lowthresh. This feature is enabled when opt_wrcam_fill_level is 1. For HW configurations which have more than 256 deep write CAM, use SCHED7.wrcam_highthresh_extend instead. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS" + 7
x:0	wrcam_lowthresh	R/W	The low threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_lowthresh), keep to write mode and stop to prepare banks for read direction if no Exp-VPR or read collision is there. This feature is enabled when opt_wrcam_fill_level is 1. For HW configurations which have more than 256 deep write CAM, use SCHED7.wrcam_lowthresh_extend instead. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS" - 1

3.2.39 SCHED4

- **Name:** Scheduler Control Register 4
- **Description:** Scheduler Control Register 4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10390
- **Exists:** MEMC_ENH_RDWR_SWITCH==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

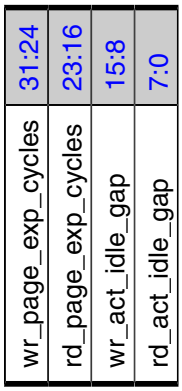


Table 3-114 Fields for Register: SCHED4

Bits	Name	Memory Access	Description
31:24	wr_page_exp_cycles	R/W	wr_page_exp_cycles indicates number of cycles to keep the bank opened for write direction in read mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Static
23:16	rd_page_exp_cycles	R/W	rd_page_exp_cycles indicates number of cycles to keep the bank opened for read direction in write mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. **Value After Reset:** 0x40 **Volatile:** true **Programming Mode:** Static

Table 3-114 Fields for Register: SCHED4 (continued)

Bits	Name	Memory Access	Description
15:8	wr_act_idle_gap	R/W	wr_act_idle_gap indicates number of cycles when write direction has no request to start preparing bank for read direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. **Value After Reset:** 0x8 **Volatile:** true **Programming Mode:** Static
7:0	rd_act_idle_gap	R/W	rd_act_idle_gap indicates number of cycles when read direction has no request to start preparing bank for write direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. **Value After Reset:** 0x10 **Volatile:** true **Programming Mode:** Static

3.2.40 SCHED5

- **Name:** Scheduler Control Register 5.
- **Description:** Scheduler Control Register 5.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10394
- **Exists:** MEMC_ENH_RDWR_SWITCH==1 && MEMC_INLINE_ECC==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

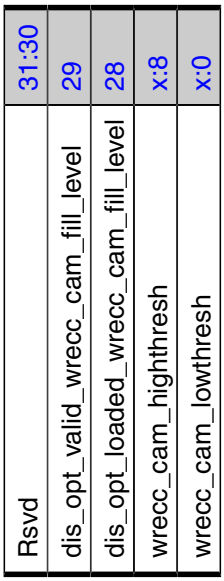


Table 3-115 Fields for Register: SCHED5

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29	dis_opt_valid_wrecc_cam_fill_level	R/W	In this release, this register bit, dis_opt_valid_wrecc_cam_fill_level, is required to set to 0 in software unless otherwise advised by Synopsys. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
28	dis_opt_loaded_wrecc_cam_fill_level	R/W	In this release, this register bit, dis_opt_loaded_wrecc_cam_fill_level, is required to set to 0 in software unless otherwise advised by Synopsys. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static

Table 3-115 Fields for Register: SCHED5 (continued)

Bits	Name	Memory Access	Description
x:8	wrecc_cam_highthresh	R/W	The high threshold used in optimized write ECC CAM fill level. When (MEMC_NO_OF_ENTRY/2 - (number of loaded entries) < wrecc_cam_highthresh), switch to write mode and prepare banks for write direction if no Exp-VPR or read collision is there. This feature is enabled when opt_wrcam_fill_level is 1. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS - 1" + 7
x:0	wrecc_cam_lowthresh	R/W	The low threshold used in optimize write ECC CAM fill level. When (MEMC_NO_OF_ENTRY/2 - (number of loaded entries) < wrecc_cam_lowthresh), keep to write mode and stop to prepare banks for read direction if no Exp-VPR or read collision is there. This feature is enabled when opt_wrcam_fill_level is 1. **Value After Reset:** 0x4 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS - 1" - 1

3.2.41 HWFFCCTL

- **Name:** Hardware Fast Frequency Change (HWFFC) Control Register.
- **Description:** Hardware Fast Frequency Change (HWFFC) Control Register.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10400
- **Exists:** UMCTL2_HWFFC_EN==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

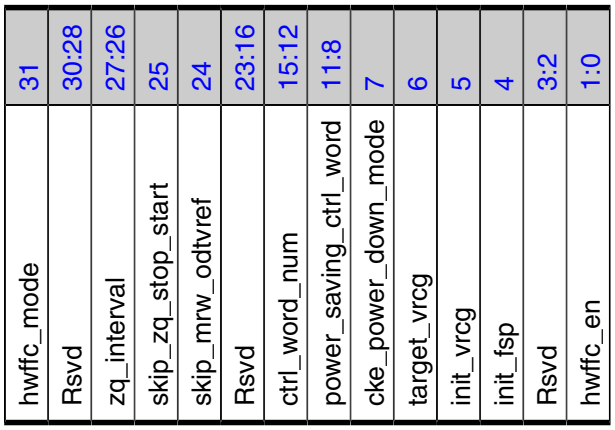


Table 3-116 Fields for Register: HWFFCCTL

Bits	Name	Memory Access	Description
31	hwffc_mode	R/W	Select HWFFC mode ■ 0 - Legacy HWFFC (default) ■ 1 - HWFFC that utilize Synopsys PHY capability i.e. support HWFFC with dfi_freq_fsp flip, HWLP driven Retraining and HWLP driven LP2. **Value After Reset:** 0x0 **Programming Mode:** Static
30:28			**Reserved Field:** Yes
27:26	zq_interval	R/W	Set ZQ interval as programmed in MR28. This field is used when ZQ command is issued during HWLP driven LP2/3 enter/exit. ■ 00 - Background Cal Interval <= 32ms ■ 01 - Background Cal Interval <= 64ms (default) ■ 10 - Background Cal Interval <= 128ms ■ 11 - Background Cal Interval <= 256ms **Value After Reset:** 0x1 **Programming Mode:** Static

Table 3-116 Fields for Register: HWFFCCTL (continued)

Bits	Name	Memory Access	Description
25	skip_zq_stop_start	R/W	If this register is set to 1, the DDRCTL will skip issuing MRW to MR28 as part of the HWLP driven LP2 sequence. If this register is 0, DDRCTL stops and re-starts LPDDR5 background ZQ calibration before and after HWLP driven LP2 operation to align with PHY/DRAM requirements. Set to 1 only if MR28 is manually controlled by the software. ZQCTL2.dis_srx_zqcl_hwffc and ZQCTL2.dis_srx_zqcl should be 1 in such case. **Value After Reset:** 0x0 **Programming Mode:** Static
24	skip_mrw_odtvref	R/W	If this register is set to 1, the DDRCTL will skip issuing MRW to MR11, MR12, MR14, and MR22 as part of the LPDDR4 legacy HWFFC (HWFFCCTL.hwffc_mode=0) procedure. In LPDDR4X SDRAM, these registers are programmed per-rank during initialization. **Value After Reset:** 0x0 **Programming Mode:** Static
23:16			**Reserved Field:** Yes
15:12	ctrl_word_num	R/W	Number of control words must be issued to RCD while DDR4 HWFFC sequence is working.If user set this register to 0, controller does not issue MR7. DDR5: Not supported. **Value After Reset:** 0x0 **Programming Mode:** Static
11:8	power_saving_ctrl_word	R/W	Indicates the value to be loaded into power saving setting control word (F0RC09). User need to set this register when change frequency using sequence A. Used in DDR4 RDIMM. DDR5: Not supported. **Value After Reset:** 0x0 **Programming Mode:** Static
7	cke_power_down_mode	R/W	Set to 1 when the DDRCTL issues MR7 for F0RC09 while DDR4 HWFFC sequence is working if necessary. Used in DDR4 RDIMM or LRDIMM. DDR5: Not supported. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-116 Fields for Register: HWFFCCTL (continued)

Bits	Name	Memory Access	Description
6	target_vrcg	R/W	LPDDR4: Set target value of VRCG (MR13 OP[3]). Only applicable for legacy HWFFC (HWFFCCTL.hwffc_mode=0) otherwise set this value to '0'. **Value After Reset:** 0x0 **Programming Mode:** Static
5	init_vrcg	R/W	Set initial value of VRCG (MR13 OP[3]). This field value is used when HWFFCCTL.hwffc_en has been changed to 2'11. Only applicable for legacy HWFFC (HWFFCCTL.hwffc_mode=0) otherwise set this value to '0'. **Value After Reset:** 0x0 **Programming Mode:** Static
4	init_fsp	R/W	Set initial value of DRAM FSP. This field value is used when HWFFCCTL.hwffc_en has been changed to 2'11. Only applicable for legacy HWFFC (HWFFCCTL.hwffc_mode=0) otherwise set this value to '1'. **Value After Reset:** 0x1 **Programming Mode:** Static
3:2			**Reserved Field:** Yes
1:0	hwffc_en	R/W	Enable HWFFC through Hardware Low Power Interface. The other fields of this register is used only when changing this field to 2'b11. ■ 00 - Disable HWFFC ■ 01 - Illegal ■ 10 - Intermediate, set only when disabling HWFFC ■ 11 - Enable legacy HWFFC or new HWFFC with HWLP driven retraining and LP2 enter support. LPDDR54 only. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.42 HWFFCSTAT

- **Name:** Hardware Fast Frequency Change (HWFFC) Status Register
- **Description:** Hardware Fast Frequency Change (HWFFC) Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10404
- **Exists:** UMCTL2_HWFFC_EN==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

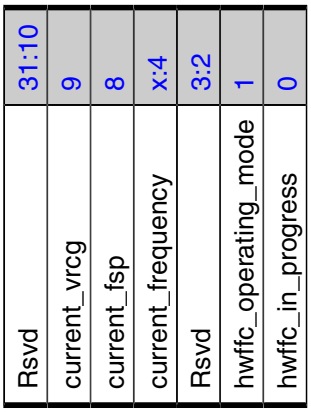


Table 3-117 Fields for Register: HWFFCSTAT

Bits	Name	Memory Access	Description
31:10			**Reserved Field:** Yes
9	current_vrcg	R	Indicates current value of VRCG (MR13 OP[3] for LPDDR4). This field is only applicable for legacy HWFFC. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
8	current_fsp	R	Indicates current value of FSP-OP (MR13 OP[7] for LPDDR4. MR16 OP[2] for LPDDR5). **Value After Reset:** 0x1 **Programming Mode:** Dynamic

Table 3-117 Fields for Register: HWFFCSTAT (continued)

Bits	Name	Memory Access	Description
x:4	current_frequency	R	Indicates the current frequency. ■ 0 - Frequency 0/Normal ■ 1 - Frequency 1/FREQ1 ■ 2 - Frequency 2/FREQ2 ■ 3 - Frequency 3/FREQ3 ■ 4 - Frequency 4/FREQ4 ■ 5 - Frequency 5/FREQ5 ■ 6 - Frequency 6/FREQ6 ■ 7 - Frequency 7/FREQ7 ■ 8 - Frequency 8/FREQ8 ■ 9 - Frequency 9/FREQ9 ■ 10 - Frequency 10/FREQ10 ■ 11 - Frequency 11/FREQ11 ■ 12 - Frequency 12/FREQ12 ■ 13 - Frequency 13/FREQ13 ■ 14 - Frequency 14/FREQ14 **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_FREQUENCY_BITS" + 3
3:2			**Reserved Field:** Yes
1	hwffc_operating_mode	R	Operating mode of HWFFC. ■ 0 - Normal ■ 1 - Self Refresh or SR-Powerdown **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	hwffc_in_progress	R	Indicates HWFFC is in progress. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.43 HWFFC_MRWBUF_CTRL0

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
- **Size:** 32 bits
- **Offset:** 0x10410
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH0.

Table 3-118 Fields for Register: HWFFC_MRWBUF_CTRL0

Bits	Name	Memory Access	Description
31	hwffc_mrwbuf_rw_start	R/W1C	Assert this bit to trigger a read/write operation to MRW buffer. This bit is self-cleared. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30	hwffc_mrwbuf_rw_type	R/W	rw type for MRW buffer, ■ 1 - write ■ 0 - read **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:24	hwffc_mrwbuf_select	R/W	PState select, select to access which PState in MRW buffer ■ 0 - PState 0 ■ 1 - PState 1 ■ 13 - PState 13 ■ 14 - PState 14 **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_FREQUENCY_BITS" + 23

Table 3-118 Fields for Register: HWFFC_MRWBUF_CTRL0 (continued)

Bits	Name	Memory Access	Description
x:16	hwffc_mrwbuf_addr	R/W	MRW buffer address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_MRWBUF_DEPTH_LOG2 - DDRCTL_FREQUENCY_BITS" + 15
15:0			**Reserved Field:** Yes

3.2.44 HWFFC_MRWBUF_CTRL1

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
- **Size:** 32 bits
- **Offset:** 0x10414
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH0.

Table 3-119 Fields for Register: HWFFC_MRWBUF_CTRL1

Bits	Name	Memory Access	Description
x:0	hwffc_mrwbuf_wdata	R/W	Encoded MRW value written into HWFFC MRW buffer. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_MRWBUF_DATA_WIDTH" - 1

3.2.45 HWFFC_MRWBUF_STAT

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer status register
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer status register
- **Size:** 32 bits
- **Offset:** 0x10418
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH0.

Table 3-120 Fields for Register: HWFFC_MRWBUF_STAT

Bits	Name	Memory Access	Description
x:0	hwffc_mrwbuf_rdata	R	Encoded MRW value returned from HWFFC MRW buffer. **Value After Reset:** 0x0 **Testable:** readOnly **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "DDRCTL_MRWBUF_DATA_WIDTH" - 1

3.2.46 DFILPCFG0

- **Name:** DFI Low Power Configuration Register 0
- **Description:** DFI Low Power Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10500
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

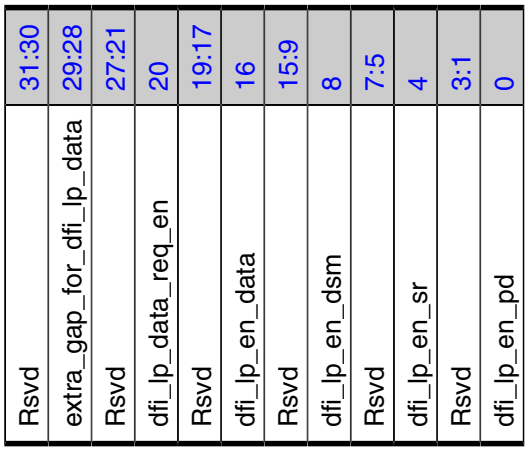


Table 3-121 Fields for Register: DFILPCFG0

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:28	extra_gap_for_dfi_lp_data	R/W	Set this to "tlp_resp + tlp_data_wakeup - 4". This reister can support up to 2. If the result is larger than 2, please set this to 0 and DFILPCFG0.dfi_lp_en_data to 0. Unit: DFI clock cycles. **Value After Reset:** 0x0 **Programming Mode:** Static
27:21			**Reserved Field:** Yes
20	dfi_lp_data_req_en	R/W	Enables DFI Data Low Power interface. ■ 0 - Disabled. dfi_lp_data_req is not asserted. ■ 1 - Enabled **Value After Reset:** 0x1 **Programming Mode:** Static
19:17			**Reserved Field:** Yes

Table 3-121 Fields for Register: DFILPCFG0 (continued)

Bits	Name	Memory Access	Description
16	dfi_lp_en_data	R/W	Enables DFI Data Low Power interface handshaking during data bus idle. ■ 0 - Disabled ■ 1 - Enabled For DDR5, this should be set to 0. For DDR4, this should be set to 0 if tphy_wrlat or trddata_en is less than "(tlp_data_resp + tlp_data_wakeup)*2 + additional gap required by PHY". Please see the PHY databook. **Value After Reset:** 0x0 **Programming Mode:** Static
15:9			**Reserved Field:** Yes
8	dfi_lp_en_dsm	R/W	Enables DFI Low Power interface handshaking during Deep Sleep Mode Entry/Exit. ■ 0 - Disabled ■ 1 - Enabled This is only present for designs supporting LPDDR5 devices. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4	dfi_lp_en_sr	R/W	Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit. If dfi_lp_en_sr is set to 1, controller will put PHY in LowPower mode through DFI LowPower interface after putting all DRAM ranks in SelfRefresh mode, and controller will wake up PHY from LowPower mode before starting SRX sequence. ■ 0 - Disabled ■ 1 - Enabled **Value After Reset:** 0x0 **Programming Mode:** Static
3:1			**Reserved Field:** Yes

Table 3-121 Fields for Register: DFILPCFG0 (continued)

Bits	Name	Memory Access	Description
0	dfi_lp_en_pd	R/W	Enables DFI Low Power interface handshaking during Power Down Entry/Exit. If dfi_lp_en_pd is set to 1, controller will put PHY in LowPower mode through DFI LowPower interface after putting all DRAM ranks in PowerDown mode, and controller will wake up PHY from LowPower mode before starting PDX sequence. ■ 0 - Disabled ■ 1 - Enabled **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.47 DFIUPD0

- **Name:** DFI Update Register 0
- **Description:** DFI Update Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10508
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

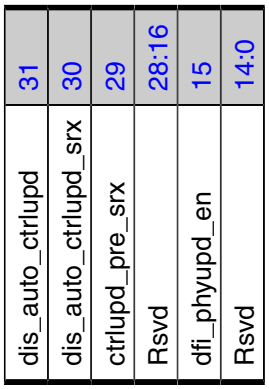


Table 3-122 Fields for Register: DFIUPD0

Bits	Name	Memory Access	Description
31	dis_auto_ctrlupd	R/W	■ 0 - DDRCTL issues dfi_ctrlupd_req periodically. ■ 1 - Disable the automatic dfi_ctrlupd_req generation by the DDRCTL. The core must issue the dfi_ctrlupd_req signal using register OPCTRLCMD.ctrlupd. Don't care for DDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
30	dis_auto_ctrlupd_srx	R/W	■ 0 - DDRCTL issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. ■ 1 - Disable the automatic dfi_ctrlupd_req generation by the DDRCTL at self-refresh exit. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static

Table 3-122 Fields for Register: DFIUPD0 (continued)

Bits	Name	Memory Access	Description
29	ctrlupd_pre_srx	R/W	Selects dfi_ctrlupd_req requirements at SRX: ■ 0 : send ctrlupd after SRX ■ 1 : send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. **Value After Reset:** 0x0 **Programming Mode:** Static
28:16			**Reserved Field:** Yes
15	dfi_phyupd_en	R/W	Enables the support for acknowledging PHY-initiated updates: ■ 0 - Disabled ■ 1 - Enabled **Value After Reset:** 0x1 **Programming Mode:** Static
14:0			**Reserved Field:** Yes

3.2.48 DFIMISC

- **Name:** DFI Miscellaneous Control Register
- **Description:** DFI Miscellaneous Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10510
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

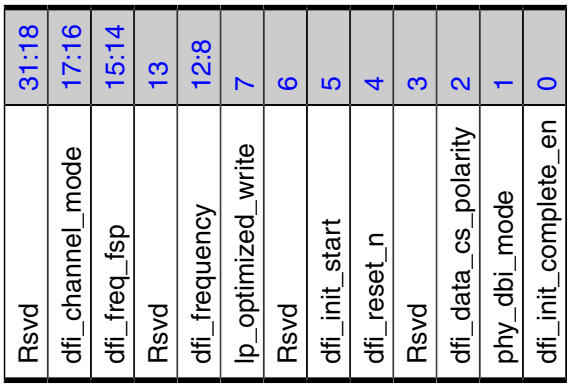


Table 3-123 Fields for Register: DFIMISC

Bits	Name	Memory Access	Description
31:18			**Reserved Field:** Yes
17:16	dfi_channel_mode	R/W	This field controls how internal DFI data is connected to dfi0_*data* and dfi1_*data*. Under the following conditions, this must be set to 2'b01: ■ When using a Synopsys DWC LPDDR54 PHY ■ Single DDRC Dual DFI configuration (MEMC_DRAM_DATA_WIDTH=32) or Single DDRC Quad DFI configuration (MEMC_DRAM_DATA_WIDTH=64) ■ Data width of each DFI channel is 16 ■ Each DFI channel corresponds to 16-bit LPDDR5/4 channel (32-bit in total when MEMC_DRAM_DATA_WIDTH=32, or 64-bit in total when MEMC_DRAM_DATA_WIDTH=64) Otherwise, this must be set to 2'b00. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-123 Fields for Register: DFIMISC (continued)

Bits	Name	Memory Access	Description
15:14	dfi_freq_fsp	R/W	This register value propagates to dfi_freq_fsp pin directly if HWFFC is disabled (hwffc_en==2'b00 or 2'b10). **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13			**Reserved Field:** Yes
12:8	dfi_frequency	R/W	Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1
7	lp_optimized_write	R/W	If this bit is 1, LPDDR4 write DQ is set to 8'hF8 if masked write with enabling DBI; otherwise, that value is set to 8'hFF **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
6			**Reserved Field:** Yes
5	dfi_init_start	R/W	PHY init start request signal.When asserted it triggers the PHY init start request **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
4	dfi_reset_n	R/W	This register value propagates to dfi_reset_n pin. Applicable for DDR4, LPDDR4 and LPDDR5. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 3
3			**Reserved Field:** Yes
2	dfi_data_cs_polarity	R/W	Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. ■ 0: Signals are active low ■ 1: Signals are active high **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-123 Fields for Register: DFIMISC (continued)

Bits	Name	Memory Access	Description
1	phy_dbi_mode	R/W	DBI implemented in DDRC or PHY. ■ 0 - DDRC implements DBI functionality. ■ 1 - PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4. **Value After Reset:** 0x0 **Programming Mode:** Static
0	dfi_init_complete_en	R/W	PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialization **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.49 DFISTAT

- **Name:** DFI Status Register
- **Description:** DFI Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10514
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

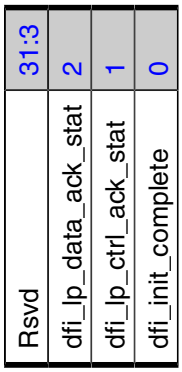


Table 3-124 Fields for Register: DFISTAT

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_lp_data_ack_stat	R	Stores the value of the dfi_lp_data_ack input to the controller. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	dfi_lp_ctrl_ack_stat	R	Stores the value of the dfi_lp_ctrl_ack input to the controller. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	dfi_init_complete	R	The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.50 DFIPHYMSTR

- **Name:** DFI PHY Master
- **Description:** DFI PHY Master
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10518
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

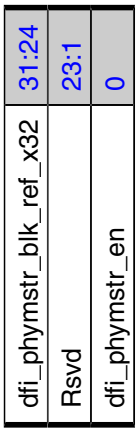


Table 3-125 Fields for Register: DFIPHYMSTR

Bits	Name	Memory Access	Description
31:24	dfi_phymstr_blk_ref_x32	R/W	The programmed value x32 is the maximum number of DFI clock cycles that allows to send pending refreshes before starting self-refresh entry process. - 0x00 - 0 DFI clock cycles, no delay - 0x01 - 32 DFI clock cycles - ... - 0xFF - 8160 DFI clock cycles Unit: Multiples of 32 DFI clock cycles. Note: Use as default value (0x80) unless Synopsys suggest to change value. **Value After Reset:** 0x80 **Programming Mode:** Static
23:1			**Reserved Field:** Yes
0	dfi_phymstr_en	R/W	Enables the PHY Master Interface: ■ 0 - Disabled ■ 1 - Enabled **Value After Reset:** 0x1 **Programming Mode:** Static

3.2.51 DFI0MSGCTL0

- **Name:** DFI0 Message Control Register 0.
- **Description:** DFI0 Message Control Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10520
- **Exists:** DDRCTL_DFI_CTRLMSG==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

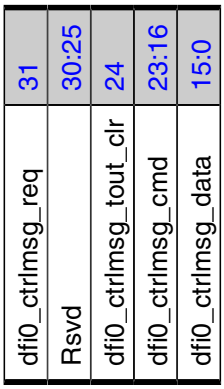


Table 3-126 Fields for Register: DFI0MSGCTL0

Bits	Name	Memory Access	Description
31	dfi0_ctrlmsg_req	R/W1S	Setting this register bit to 1 triggers a DFI controller message transmission operation. DDRCTL automatically clear this bit when the DFI controller message request (dfi0_ctrlmsg_req) is asserted at the DFI MC to PHY Message port interface . This bit must be programmed separately after programming other register fields appropriately of this register. Note: ■ DFI controller message request can be issued only if DFIPHYMSTR.dfi_phymstr_en = 1 ■ DFI controller message request must not be set during DFI LP mode due to software controlled low power entry. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30:25			**Reserved Field:** Yes

Table 3-126 Fields for Register: DFI0MSGCTL0 (continued)

Bits	Name	Memory Access	Description
24	dfi0_ctrlmsg_tout_clr	R/W1C	If this bit is set, DFI0MSGSTAT0.dfi0_ctrlmsg_resp_tout is cleared by the controller. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:16	dfi0_ctrlmsg_cmd	R/W	DFI0 controller message command. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0	dfi0_ctrlmsg_data	R/W	DFI0 controller message data. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.52 DFI0MSGSTAT0

- **Name:** DFI0 Message Status Register 0
- **Description:** DFI0 Message Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10524
- **Exists:** DDRCTL_DFI_CTRLMSG==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

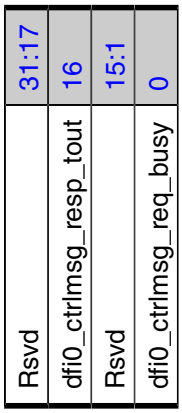


Table 3-127 Fields for Register: DFI0MSGSTAT0

Bits	Name	Memory Access	Description
31:17			**Reserved Field:** Yes
16	dfi0_ctrlmsg_resp_tout	R	This bit is set if dfi0_ctrlmsg_ack is not asserted by PHY within dfi_t_ctrlmsg_resp after asserting dfi0_ctrlmsg_req **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:1			**Reserved Field:** Yes
0	dfi0_ctrlmsg_req_busy	R	The SoC must trigger DFI controller message request only if this signal is low. This signal goes high in the clock after the DDRCTL accepts software triggered DFI controller message request by writing into DFI0MSGCTRL0.dfi0_ctrlmsg_req. It goes low when PHY deasserts dfi0_ctrlmsg_ack or dfi0_ctrlmsg_resp_tout event has triggered. ■ 0 - Indicates that the SoC core can initiate a DFI controller message request operation ■ 1 - Indicates that DFI controller message request operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.53 DFISBINTRPTCFG

- **Name:** DFI Sideband Watchdog Timer Interrupt Configuration Register
- **Description:** DFI Sideband Watchdog Timer Interrupt Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10528
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-128 Fields for Register: DFISBINTRPTCFG

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_sideband_timer_err_intr_force	R/W1C	Interrupt force bit for dfi_sideband_timer_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering and interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-128 Fields for Register: DFISBINTRPTCFG (continued)

Bits	Name	Memory Access	Description
1	dfi_sideband_timer_err_intr_clr	R/W1C	Clear DFI Sideband timer error interrupt (dfi_sideband_timer_err_intr). Setting this bit also clears all the error status bits in DFISBTIMERSTAT and DFISBTIMERSTAT1 registers. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	dfi_sideband_timer_err_intr_en	R/W	Enables interrupt generation when error is detected on any of the DFI Sideband watchdog timers. The name of the interrupt that is enabled is dfi_sideband_timer_err_intr. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.54 DFISBPOISONCFG

- **Name:** DFI Sideband Watchdog Timer Poison Control Register
- **Description:** DFI Sideband Watchdog Timer Poison Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10530
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31:28	27:24	23:20	19:16	15:12	11	10	9	8	7:6	5	4	3:2	1	0
dfi_tlp_data_resp_poison_margin	dfi_tlp_ctrl_resp_poison_margin	dfi_tinit_start_poison_margin	dfi_tctrlupd_min_poison_margin	Rsvd	dfi_tlp_data_wakeup_poison_err_inj	dfi_tlp_ctrl_wakeup_poison_err_inj	dfi_tlp_data_resp_poison_err_inj	dfi_tlp_ctrl_resp_poison_err_inj	Rsvd	dfi_tinit_complete_poison_err_inj	dfi_tinit_start_poison_err_inj	Rsvd	dfi_tctrlupd_max_poison_err_inj	dfi_tctrlupd_min_poison_err_inj

Table 3-129 Fields for Register: DFISBPOISONCFG

Bits	Name	Memory Access	Description
31:28	dfi_tlp_data_resp_poison_margin	R/W	Specifies the number of clock cycles for which dfi_lp_data_req will be asserted when doing the DFILPTMG1.dfi_tlp_resp duration poison error testing. DFISBPOISONCFG.dfi_tlp_data_resp_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFILPTMG1.dfi_tlp_resp register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1

Table 3-129 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
27:24	dfi_tlp_ctrl_resp_poison_margin	R/W	Specifies the number of clock cycles for which dfi_lp_ctrl_req will be asserted when doing the DFILPTMG1.dfi_tlp_resp duration poison error testing. DFISBPOISONCFG.dfi_tlp_ctrl_resp_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFILPTMG1.dfi_tlp_resp register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
23:20	dfi_tinit_start_poison_margin	R/W	Specifies the number of clock cycles for which dfi_init_start will be asserted when doing the minimum duration poison error testing. DFISBPOISONCFG.dfi_tinit_start_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFITMG7.dfi_t_init_start register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
19:16	dfi_tctrlupd_min_poison_margin	R/W	Specifies the number of clock cycles for which dfi_ctrlupd_req will be asserted when doing the minimum duration poison error testing. DFISBPOISONCFG.dfi_tctrlupd_min_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFIUPDTMG0.dfi_t_ctrlup_min register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
15:12			**Reserved Field:** Yes
11	dfi_tlp_data_wakeup_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum deassertion time requirement of dfi_lp_data_ack signal. This will result in the DFISBTIMERSTAT.dfi_tlp_data_wakeup_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1

Table 3-129 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
10	dfi_tlp_ctrl_wakeup_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum deassertion time requirement of dfi_lp_ctrl_ack signal. This will result in the DFISBTIMERSTAT.dfi_tlp_ctrl_wakeup_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
9	dfi_tlp_data_resp_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_lp_data_req signal. This will result in the DFISBTIMERSTAT.dfi_tlp_data_resp_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
8	dfi_tlp_ctrl_resp_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_lp_ctrl_req signal. This will result in the DFISBTIMERSTAT.dfi_tlp_ctrl_resp_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
7:6			**Reserved Field:** Yes
5	dfi_tinit_complete_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum reassertion time requirement of dfi_init_complete signal. This will result in the DFISBTIMERSTAT.dfi_tinit_complete_error bit to be set when a frequency change request is initiated by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
4	dfi_tinit_start_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum duration for which dfi_init_start signal should stay asserted once it is asserted. This will result in the DFISBTIMERSTAT.dfi_tinit_start_error bit to be set when a frequency change request is initiated by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
3:2			**Reserved Field:** Yes

Table 3-129 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
1	dfi_tctrlupd_max_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum assertion time requirement of dfi_ctrlupd_req signal. This will result in the DFISBTIMERSTAT.dfi_tctrlupd_max_error bit to be set when a Controller initiated Update request is send to PHY. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
0	dfi_tctrlupd_min_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_ctrlupd_req signal. This will result in the DFISBTIMERSTAT.dfi_tctrlupd_min_error bit to be set when a Controller initiated Update request is send to PHY. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1

3.2.55 DFISBTIMERSTAT

- **Name:** DFI Sideband Watchdog Timer Status Register
- **Description:** DFI Sideband Watchdog Timer Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10538
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

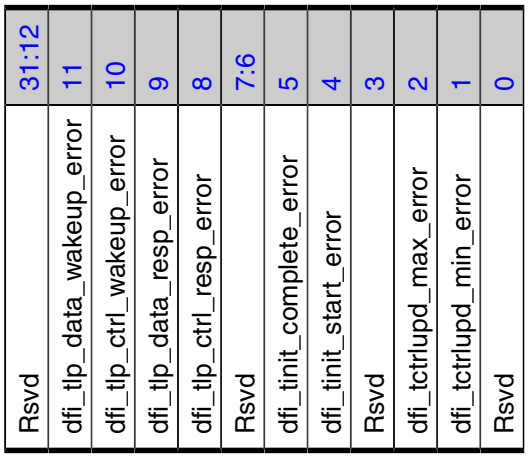


Table 3-130 Fields for Register: DFISBTIMERSTAT

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11	dfi_tlp_data_wakeup_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_data_wakeup timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	dfi_tlp_ctrl_wakeup_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_ctrl_wakeup timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
9	dfi_tlp_data_resp_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_data_resp timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-130 Fields for Register: DFISBTIMERSTAT (continued)

Bits	Name	Memory Access	Description
8	dfi_tlp_ctrl_resp_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_ctrl_resp timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:6			**Reserved Field:** Yes
5	dfi_tinit_complete_error	R	This bit is set to 1 when an error is detected on the dfi_tinit_complete_error timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	dfi_tinit_start_error	R	This bit is set to 1 when an error is detected on the dfi_tinit_start timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3			**Reserved Field:** Yes
2	dfi_tctrlupd_max_error	R	This bit is set to 1 when an error is detected on the dfi_tctrlupd_max timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	dfi_tctrlupd_min_error	R	This bit is set to 1 when an error is detected on the dfi_tctrlupd_min timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0			**Reserved Field:** Yes

3.2.56 DFISBTIMERSTAT1

- **Name:** DFI Sideband Watchdog Timer Status Register 1
- **Description:** DFI Sideband Watchdog Timer Status Register 1
- **Size:** 32 bits
- **Offset:** 0x10540
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH0.

Table 3-131 Fields for Register: DFISBTIMERSTAT1

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	dfi_sideband_timer_err_intr	R	This interrupt bit is set when any of the DFI Sideband Watchdog timers fail. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. Read all the fields of the DFISBTIMERSTAT register to get information on which timer failed before clearing the interrupt. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.57 DFIERRINTRPTCFG

- **Name:** DFI Error Interface Interrupt Configuration Register
- **Description:** DFI Error Interface Interrupt Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10548
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-132 Fields for Register: DFIERRINTRPTCFG

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_error_intr_force	R/W1C	Interrupt force bit for dfi_error_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	dfi_error_intr_clr	R/W1C	Interrupt clear bit for DFI Error Interrupt (dfi_error_intr). This also clears the following two error status fields: DFIERRORSTAT.dfi_error_intr and DFIERRORSTAT1.dfi_error_info register fields. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-132 Fields for Register: DFIERRINTRPTCFG (continued)

Bits	Name	Memory Access	Description
0	dfi_error_intr_en	R/W	Interrupt enable bit for DFI Error Interrupt (dfi_error_intr). This interrupt is set when error is detected on the dfi_error input signal coming from PHY. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.58 DFIERRORSTAT

- **Name:** DFI Error Interface Status Register
- **Description:** DFI Error Interface Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10550
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-133 Fields for Register: DFIERRORSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	dfi_error_intr	R	This bit is set to 1 when PHY asserts dfi_error signal. The bit remains set until it is cleared using the register bit DFIERRINTRPTCFG.dfi_error_intr_clr. Only one error will be captured at any time. Any error indicated on dfi_error input signal between the setting and clearing of this register bit won't be captured. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.59 DFIERRORSTAT1

- **Name:** DFI Error Interface Status Register 1
- **Description:** DFI Error Interface Status Register 1
- **Size:** 32 bits
- **Offset:** 0x10558
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH0.

Table 3-134 Fields for Register: DFIERRORSTAT1

Bits	Name	Memory Access	Description
31:4			**Reserved Field:** Yes
3:0	dfi_error_info	R	This field has the value that is send by PHY on the dfi_error_info signal. This field is valid when bit[0] of this register is 1. This bit remains set until it is cleared using the register bit DFIERRINTRPTCFG.dfi_error_intr_clr. Only one error will be captured at any time. Any error indicated on dfi_error_info input signal between the setting and clearing of this register bit won't be captured. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.60 POISONCFG

- **Name:** AXI Poison Configuration Register. Common for all AXI ports
- **Description:** AXI Poison Configuration Register. Common for all AXI ports
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10580
- **Exists:** UMCTL2_INCL_ARB==1 && UMCTL2_A_AXI==1

This register is in block REGB_DDRC_CH0.

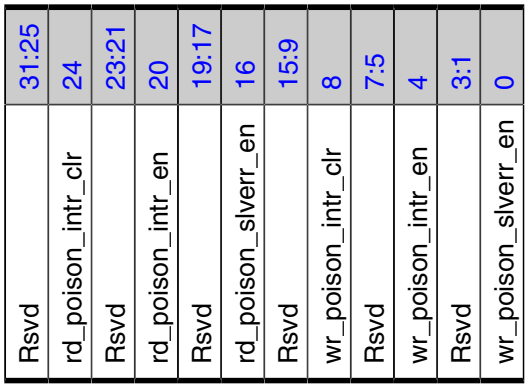


Table 3-135 Fields for Register: POISONCFG

Bits	Name	Memory Access	Description
31:25			**Reserved Field:** Yes
24	rd_poison_intr_clr	R/W1C	Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:21			**Reserved Field:** Yes
20	rd_poison_intr_en	R/W	If set to 1, enables interrupts for read transaction poisoning **Value After Reset:** 0x1 **Programming Mode:** Dynamic
19:17			**Reserved Field:** Yes
16	rd_poison_slverr_en	R/W	If set to 1, enables SLVERR response for read transaction poisoning **Value After Reset:** 0x1 **Programming Mode:** Dynamic
15:9			**Reserved Field:** Yes

Table 3-135 Fields for Register: POISONCFG (continued)

Bits	Name	Memory Access	Description
8	wr_poison_intr_clr	R/W1C	Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7:5			**Reserved Field:** Yes
4	wr_poison_intr_en	R/W	If set to 1, enables interrupts for write transaction poisoning **Value After Reset:** 0x1 **Programming Mode:** Dynamic
3:1			**Reserved Field:** Yes
0	wr_poison_slverr_en	R/W	If set to 1, enables SLVERR response for write transaction poisoning **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.61 POISONSTAT

- **Name:** AXI Poison Status Register
- **Description:** AXI Poison Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10584
- **Exists:** UMCTL2_INCL_ARB==1 && UMCTL2_A_AXI==1

This register is in block REGB_DDRC_CH0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rd_poison_intr_15	rd_poison_intr_14	rd_poison_intr_13	rd_poison_intr_12	rd_poison_intr_11	rd_poison_intr_10	rd_poison_intr_9	rd_poison_intr_8	rd_poison_intr_7	rd_poison_intr_6	rd_poison_intr_5	rd_poison_intr_4	rd_poison_intr_3	rd_poison_intr_2	rd_poison_intr_1	rd_poison_intr_0	wr_poison_intr_15	wr_poison_intr_14	wr_poison_intr_13	wr_poison_intr_12	wr_poison_intr_11	wr_poison_intr_10	wr_poison_intr_9	wr_poison_intr_8	wr_poison_intr_7	wr_poison_intr_6	wr_poison_intr_5	wr_poison_intr_4	wr_poison_intr_3	wr_poison_intr_2	wr_poison_intr_1	wr_poison_intr_0

Table 3-136 Fields for Register: POISONSTAT

Bits	Name	Memory Access	Description
31	rd_poison_intr_15	R	Read transaction poisoning error interrupt for port 15. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30	rd_poison_intr_14	R	Read transaction poisoning error interrupt for port 14. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
29	rd_poison_intr_13	R	Read transaction poisoning error interrupt for port 13. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	rd_poison_intr_12	R	Read transaction poisoning error interrupt for port 12. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
27	rd_poison_intr_11	R	Read transaction poisoning error interrupt for port 11. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26	rd_poison_intr_10	R	Read transaction poisoning error interrupt for port 10. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
25	rd_poison_intr_9	R	Read transaction poisoning error interrupt for port 9. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
24	rd_poison_intr_8	R	Read transaction poisoning error interrupt for port 8. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	rd_poison_intr_7	R	Read transaction poisoning error interrupt for port 7. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	rd_poison_intr_6	R	Read transaction poisoning error interrupt for port 6. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
21	rd_poison_intr_5	R	Read transaction poisoning error interrupt for port 5. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	rd_poison_intr_4	R	Read transaction poisoning error interrupt for port 4. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	rd_poison_intr_3	R	Read transaction poisoning error interrupt for port 3. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
18	rd_poison_intr_2	R	Read transaction poisoning error interrupt for port 2. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
17	rd_poison_intr_1	R	Read transaction poisoning error interrupt for port 1. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	rd_poison_intr_0	R	Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15	wr_poison_intr_15	R	Write transaction poisoning error interrupt for port 15. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	wr_poison_intr_14	R	Write transaction poisoning error interrupt for port 14. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
13	wr_poison_intr_13	R	Write transaction poisoning error interrupt for port 13. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
12	wr_poison_intr_12	R	Write transaction poisoning error interrupt for port 12. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	wr_poison_intr_11	R	Write transaction poisoning error interrupt for port 11. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	wr_poison_intr_10	R	Write transaction poisoning error interrupt for port 10. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
9	wr_poison_intr_9	R	Write transaction poisoning error interrupt for port 9. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	wr_poison_intr_8	R	Write transaction poisoning error interrupt for port 8. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	wr_poison_intr_7	R	Write transaction poisoning error interrupt for port 7. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
6	wr_poison_intr_6	R	Write transaction poisoning error interrupt for port 6. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
5	wr_poison_intr_5	R	Write transaction poisoning error interrupt for port 5. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	wr_poison_intr_4	R	Write transaction poisoning error interrupt for port 4. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3	wr_poison_intr_3	R	Write transaction poisoning error interrupt for port 3. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	wr_poison_intr_2	R	Write transaction poisoning error interrupt for port 2. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-136 Fields for Register: POISONSTAT (continued)

Bits	Name	Memory Access	Description
1	wr_poison_intr_1	R	Write transaction poisoning error interrupt for port 1. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	wr_poison_intr_0	R	Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.62 ECCCFG0

- **Name:** ECC Configuration Register 0
- **Description:** ECC Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10600
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

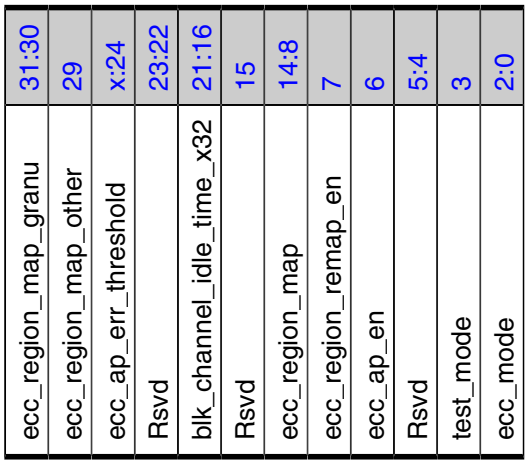


Table 3-137 Fields for Register: ECCCFG0

Bits	Name	Memory Access	Description
31:30	ecc_region_map_granu	R/W	Granularity of Selectable Protected Region. Define one region size for ECCCFG0.ecc_region_map ■ 0 - 1/8 of memory spaces ■ 1 - 1/16 of memory spaces ■ 2 - 1/32 of memory spaces ■ 3 - 1/64 of memory spaces **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-137 Fields for Register: ECCCFG0 (continued)

Bits	Name	Memory Access	Description
29	ecc_region_map_other	R/W	When ECCCFG0.ecc_region_map_granu>0, there is a region which is not controlled by ecc_region_map. This register defines the region to be protected or non-protected for Inline ECC. ■ 0 - Non-Protected ■ 1 - Protected This register is valid only when ECCCFG0.ecc_region_map_granu>0 && ECCCFG0.ecc_mode=4. **Value After Reset:** 0x0 **Programming Mode:** Static
x:24	ecc_ap_err_threshold	R/W	Set threshold for address parity error. ECCAPSTAT.ecc_ap_err is asserted if number of ECC errors (correctable/uncorrectable) within one burst exceeds this threshold. This register value must be less than "Total number of ECC checks within one burst" when this feature is used, "Total number of ECC check within one burst" is calculated by (DRAM Data width) x (DRAM BL) / 64. **Value After Reset:** "MEMC_MAX_INLINE_ECC_PER_BURST/2-1" **Programming Mode:** Static **Range Variable[x]:** "MEMC_MAX_INLINE_ECC_PER_BURST_BITS" + 23
23:22			**Reserved Field:** Yes
21:16	blk_channel_idle_time_x32	R/W	Indicates the number of cycles on HIF interface with no access to protected regions which will cause flush of all the block channels. In order to flush block channel, DDRCTL injects write ECC command (when there is no incoming HIF command) if there is any write in the block and then stop tracking the block address. ■ 0 indicates no timeout (feature is disabled, not supported with this version) ■ 1 indicates 32 cycles ■ 2 indicates 2*32 cycles, etc. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x3f **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-137 Fields for Register: ECCCFG0 (continued)

Bits	Name	Memory Access	Description
15			**Reserved Field:** Yes
14:8	ecc_region_map	R/W	Selectable Protected Region setting. Memory space is divided to 8/16/32/64 regions which is determined by ECCCFG0.ecc_region_map_granu. Note: Highest 1/8 memory space is always ECC region. Lowest 7 regions are Selectable Protected Regions. The Selectable Protected Regions can be protected/non-protected selectively by ECCCFG0.ecc_region_map[6:0]. Other upper regions are non-protected region if any. Each bit of ECCCFG0.ecc_region_map[6:0] correspond to each of lowest 7 regions respectively. In order to protect a region with ECC, set the corresponding bit to 1, otherwise set to 0. All "0"s is invalid - there must be at least one protected region if inline ECC is enabled via ECCCFG0.ecc_mode register. All regions are protected with the following setting. ■ ecc_region_map=7'b1111111 ■ ecc_region_map_granu=0 Only first 1/64 region is protected with the following setting. ■ ecc_region_map=7'b0000001 ■ ecc_region_map_granu=3 **Value After Reset:** 0x7f **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
7	ecc_region_remap_en	R/W	Enables remapping ECC region feature. Only supported when inline ECC is enabled. ■ 0 - Disable ■ 1 - Enable **Value After Reset:** 0x0 **Programming Mode:** Static
6	ecc_ap_en	R/W	Enable address protection feature. Only supported when inline ECC is enabled. ■ 0: disable ■ 1: enable **Value After Reset:** 0x1 **Programming Mode:** Static
5:4			**Reserved Field:** Yes

Table 3-137 Fields for Register: ECCCFG0 (continued)

Bits	Name	Memory Access	Description
3	test_mode	R/W	If this bit is set to 1, no ECC is performed, and the ECC byte is accessed directly from co_wu_rxdata_ecc and ra_co_resp_ecc_data. This test mode is only supported with the HIF interface (DDRCTL_SYS_INTF=0). This test mode is only supported in full and half bus width mode. In other words, if MSTR0.data_bus_width is not equal to 0 or 1, this test_mode field must be set to 0. If test_mode is set to 1, the ecc_mode field must be set to 3'b000. Note: test_mode is not supported in inline ECC mode and the register value is don't care. **Value After Reset:** 0x0 **Programming Mode:** Static
2:0	ecc_mode	R/W	ECC mode indicator ■ 000 - ECC disabled ■ 100 - ECC enabled - SEC/DED ■ 101 - ECC enabled - Advanced ECC (Illegal value when MEMC_INLINE_ECC=1); Supported only for DDR4(64+8) and DDR5(32+8)/ch devices when DDRCTL_BF_ECC_EN =0; When DDRCTL_BF_ECC_EN =1, ADVECC is supported for DDR4(64+8), DDR5(32+8)/ch and DDR5(32+4)/ch devices ■ all other settings are reserved for future use **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.63 ECCCFG1

- **Name:** ECC Configuration Register 1
- **Description:** ECC Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10604
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

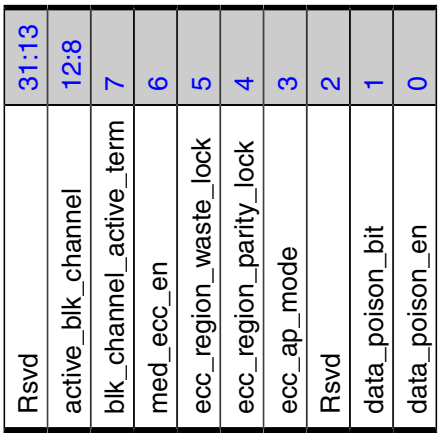


Table 3-138 Fields for Register: ECCCFG1

Bits	Name	Memory Access	Description
31:13			**Reserved Field:** Yes
12:8	active_blk_channel	R/W	Number of active block channels. Total number of ECC block channels are defined by MEMC_NO_OF_BLK_CHANNEL hardware parameter. This register can limit the number of available channels. For example, if set to 0, only one channel is active and therefore block interleaving is disabled. The valid range is from 0 to MEMC_NO_OF_BLK_CHANNEL-1. **Value After Reset:** "MEMC_NO_OF_BLK_CHANNEL-1" **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-138 Fields for Register: ECCCFG1 (continued)

Bits	Name	Memory Access	Description
7	blk_channel_active_term	R/W	Block Channel active terminate enable. If enabled, block channel is terminated when full block write or full block read is performed (all address within block are written or read) ■ 0 - Disable (only for debug purpose) ■ 1 - Enable (default) This is debug register, and this must be set to 1 for normal operation. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static
6	med_ecc_en	R/W	Determine the ECC usage in Inline ECC. ■ 0 - SECDED ECC (default) ■ 1 - SEDDED (MED) ECC In SECDED ECC mode, single-bit error is corrected, and double- bit error is detected. In more than double bit error case, it may result silent failure by mis-correction. In SEDDED (MED) mode, single-bit error correction is disabled, instead 1/2/3 bits errors and any odd-bit errors are detected as uncorrectable error. Note: When Inline ECC is not enabled by software, this register bit must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
5	ecc_region_waste_lock	R/W	Locks the remaining waste parts of the ECC region (hole) that are not locked by ecc_region_parity_lock. ■ 1: Locked; if this region is accessed, error response is generated. ■ 0: Unlocked; this region can be accessed normally, similar to non-ECC protected region. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-138 Fields for Register: ECCCFG1 (continued)

Bits	Name	Memory Access	Description
4	ecc_region_parity_lock	R/W	Locks the parity section of the ECC region (hole) which is the highest system address part of the memory that stores ECC parity for protected region. ■ 1: Locked; if this region is accessed, error response is generated. ■ 0: Unlocked; this region can be accessed normally, similar to non-ECC protected region. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
3	ecc_ap_mode	R/W	Determine the mode of ECCAP ■ 0: Legacy mode (backward compatibility mode) ■ 1: Embedded address mode Legacy mode: If ECCCFG0.ecc_ap_en=1, to generate address parity and flip two bit of ECC depending on the parity. If ECCCFG0.ecc_ap_en=0, no any ECCAP is used. Embedded address mode: ECC is calculated/checked with data address. In Embedded address mode, med_ecc_en shall be set to 1. Note: If ECCCFG0.ecc_ap_en=0, ecc_ap_mode must be set to 0. If ECCCFG1.med_ecc_en=0, ecc_ap_mode must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
2			**Reserved Field:** Yes
1	data_poison_bit	R/W	Selects whether to poison 1 or 2 bits - if 0 -> 2-bit (uncorrectable) data poisoning, if 1 -> 1-bit (correctable) data poisoning, if ECCCFG1.data_poison_en=1. Valid only when MEMC_ECC_SUPPORT==1 or 3 (in SECDED ECC mode i.e ECCCFG0.ecc_mode=3'b100) **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-138 Fields for Register: ECCCFG1 (continued)

Bits	Name	Memory Access	Description
0	data_poison_en	R/W	Enable ECC data poisoning - introduces ECC errors on writes to address specified by the ECCPOISONADDR0/1 registers This field must be set to 0 if ECC is disabled (ECCCFG0.ecc_mode = 0). **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.64 ECCSTAT

- **Name:** SECDED ECC Status Register
- **Description:** SECDED ECC Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10608
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Valid only in MEMC_ECC_SUPPORT==1 or 3 (SECDED ECC mode)

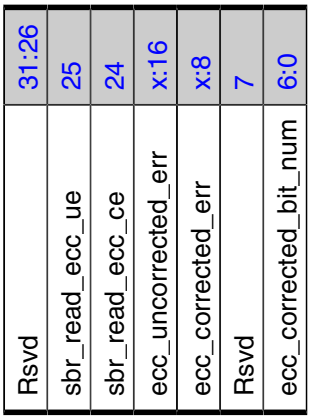


Table 3-139 Fields for Register: ECCSTAT

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25	sbr_read_ecc_ue	R	Indicates the sideband SECDED ECC uncorrectable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_uncorrected_err_clr. This bit is not applicable for Inline ECC ■ 0 - Mainline/Demand read uncorrectable error interrupt ■ 1 - Scrubber read uncorrectable error interrupt **Value After Reset:** 0x0 **Programming Mode:** Static
24	sbr_read_ecc_ce	R	Indicates the sideband SECDED ECC correctable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_corrected_err_clr. This bit is not applicable for Inline ECC ■ 0 - Mainline/Demand read correctable error interrupt ■ 1 - Scrubber read correctable error interrupt **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-139 Fields for Register: ECCSTAT (continued)

Bits	Name	Memory Access	Description
x:16	ecc_uncorrected_err	R	Double-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate uncorrectable error on any lane. When External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1, bit 16 is only valid. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(MEMC_INLINE_ECC_EN==1 && MEMC_SIDEBAND_ECC_EN==0) ? 1 : (MEMC_FREQ_RATIO==4) ? 8 : 4" + 15
x:8	ecc_corrected_err	R	Single-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate correctable error on any lane. When External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1, bit 8 is only valid. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(MEMC_INLINE_ECC_EN==1 && MEMC_SIDEBAND_ECC_EN==0) ? 1 : (MEMC_FREQ_RATIO==4) ? 8 : 4" + 7
7			**Reserved Field:** Yes
6:0	ecc_corrected_bit_num	R	Bit number corrected by single-bit ECC error. See ECC section of architecture chapter for encoding of this field. If more than one data lane has an error, the lower data lane is selected. This register is 7 bits wide in order to handle 72 bits of the data present in a single lane. This field is not applicable when External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.65 ECCCTL

- **Name:** ECC Clear Register
- **Description:** ECC Clear Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1060c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

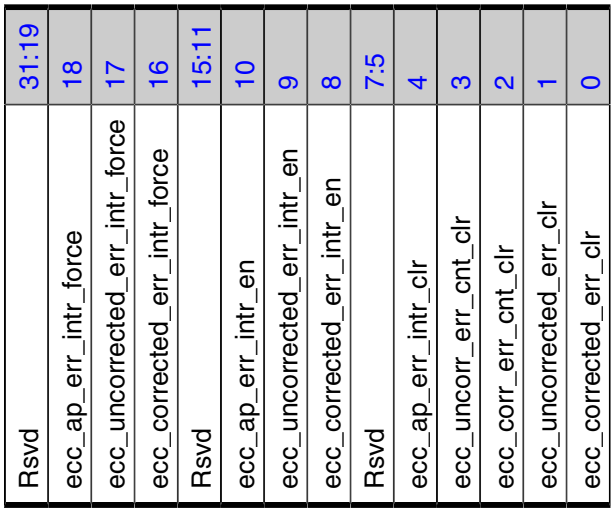


Table 3-140 Fields for Register: ECCCTL

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	ecc_ap_err_intr_force	R/W1C	Interrupt force bit for ecc_ap_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	ecc_uncorrected_err_intr_force	R/W1C	Interrupt force bit for ecc_uncorrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-140 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
16	ecc_corrected_err_intr_force	R/W1C	Interrupt force bit for ecc_corrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
15:11			**Reserved Field:** Yes
10	ecc_ap_err_intr_en	R/W	Interrupt enable bit for ecc_ap_err_intr. ■ 1: Enabled ■ 0: Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
9	ecc_uncorrected_err_intr_en	R/W	Interrupt enable bit for ecc_uncorrected_err_intr. ■ 1: Enabled ■ 0: Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
8	ecc_corrected_err_intr_en	R/W	Interrupt enable bit for ecc_corrected_err_intr. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
7:5			**Reserved Field:** Yes
4	ecc_ap_err_intr_clr	R/W1C	Interrupt clear bit for ecc_ap_err. If this bit is set, the ECCAPSTAT.ecc_ap_err/ecc_ap_err_intr will be cleared. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-140 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
3	ecc_uncorr_err_cnt_clr	R/W1C	Setting this register bit to 1 clears the currently stored uncorrected ECC error count. The ECCERRCNT.ecc_uncorr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	ecc_corr_err_cnt_clr	R/W1C	Setting this register bit to 1 clears the currently stored corrected ECC error count. The ECCERRCNT.ecc_corr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	ecc_uncorrected_err_clr	R/W1C	Setting this register bit to 1 clears the currently stored uncorrected ECC error. The following registers are cleared: ■ ECCSTAT.ecc_uncorrected_err ■ ECCSTAT.sbr_read_ecc_ue ■ ADVECCSTAT.sbr_read_advecc_ue ■ ADVECCSTAT.advecc_ue_kbd_stat ■ ADVECCSTAT.advecc_uncorrected_err ■ ECCUSYN0 ■ ECCUSYN1 ■ ECCUSYN2 ■ ECCUDATA0 ■ ECCUDATA1 ■ ECCSYMBOL.ecc_uncorr_sym_71_64 DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-140 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
0	ecc_corrected_err_clr	R/W1C	Setting this register bit to 1 clears the currently stored corrected ECC error. The following registers are cleared: ■ ECCSTAT.ecc_corrected_err ■ ECCSTAT.sbr_read_ecc_ce ■ ADVECCSTAT.sbr_read_advecc_ce ■ ADVECCSTAT.advecc_ce_kbd_stat ■ ADVECCSTAT.advecc_corrected_err ■ ADVECCSTAT.advecc_num_err_symbol ■ ADVECCSTAT.advecc_err_symbol_pos ■ ADVECCSTAT.advecc_err_symbol_bits ■ ECCCSYN0 ■ ECCCSYN1 ■ ECCCSYN2 ■ ECCBITMASK0 ■ ECCBITMASK1 ■ ECCBITMASK2 ■ ECCCDATA0 ■ ECCCDATA1 ■ ECCSYMBOL.ecc_corr_sym_71_64 DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.2.66 ECCERRCNT

- **Name:** ECC Error Counter Register
- **Description:** ECC Error Counter Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10610
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

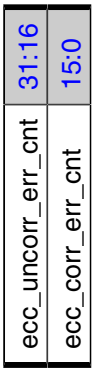


Table 3-141 Fields for Register: ECCERRCNT

Bits	Name	Memory Access	Description
31:16	ecc_uncorr_err_cnt	R	Number of uncorrectable ECC errors detected. For internal ECC or external ECC with External ECC Log disabled, it is incremented by the total number of decoders reporting UE in each cycle. For external ECC with External ECC Log enabled (DDRCTL_EXT_RAS_LOG_EN=1), It is incremented by 1 UE in each cycle. It will saturates at 0xFFFF **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0	ecc_corr_err_cnt	R	Number of correctable ECC errors detected. For internal ECC or external ECC with External ECC Log disabled, it is incremented by the total number of decoders reporting CE in each cycle. For external ECC with External ECC Log enabled (DDRCTL_EXT_RAS_LOG_EN=1), It is incremented by 1 CE in each cycle. It will saturates at 0xFFFF **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.67 ECCCADDR0

- **Name:** ECC Corrected Error Address Register 0
- **Description:** ECC Corrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10614
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

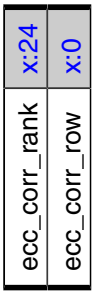


Table 3-142 Fields for Register: ECCCADDR0

Bits	Name	Memory Access	Description
x:24	ecc_corr_rank	R	Indicates the rank number of a read resulting in a corrected ECC error **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	ecc_corr_row	R	Indicates the page/row number of a read resulting in a corrected ECC error. This is 18-bits wide in configurations with LPDDR5 or DDR4 support and 16-bits in all other configurations. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.68 ECCCADDR1

- **Name:** ECC Corrected Error Address Register 1
- **Description:** ECC Corrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10618
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

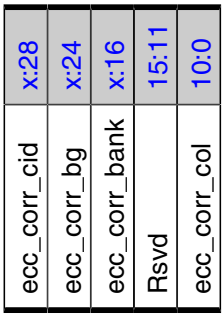


Table 3-143 Fields for Register: ECCCADDR1

Bits	Name	Memory Access	Description
x:28	ecc_corr_cid	R	CID number of a read resulting in a corrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "UMCTL2_CID_WIDTH" + 27
x:24	ecc_corr_bg	R	Bank Group number of a read resulting in a corrected ECC error. Note that when LPDDR5 16B mode is in use, this field is used as the upper bits of the bank address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	ecc_corr_bank	R	Bank number of a read resulting in a corrected ECC error. Note that when LPDDR5 16B mode is in use, {ECCCADDR1.ecc_corr_bg, ECCCADDR1.ecc_corr_bank[1:0]} shows bank number of a read resulting in a corrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-143 Fields for Register: ECCCADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	ecc_corr_col	R	Block number of a read resulting in a corrected ECC error (lowest bit not assigned here). **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.69 ECCCSYN0

- **Name:** ECC Corrected Syndrome Register 0
- **Description:** ECC Corrected Error Data Syndrome Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1061c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-144 Fields for Register: ECCCSYN0

Bits	Name	Memory Access	Description
31:0	ecc_corr_syndromes_31_0	R	Data pattern that resulted in a correctable error. For 16-bit DRAM data width, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.70 ECCCSYN1

- **Name:** ECC Corrected Syndrome Register 1
- **Description:** ECC Corrected Error Data Syndrome Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10620
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_32__OR__MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-145 Fields for Register: ECCCSYN1

Bits	Name	Memory Access	Description
31:0	ecc_corr_syndromes_63_32	R	Data pattern that resulted in a correctable error. For 32-bit and 16-bit DRAM Data width operating in single-beat SECDED or ADVECC mode, this register is not used. However, for multi-beat SECDED ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.71 ECCCSYN2

- **Name:** ECC Corrected Syndrome Register 2
- **Description:** ECC Corrected Error ECC Syndrome Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10624
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-146 Fields for Register: ECCCSYN2

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	cb_corr_syndrome	R	Indicates the Checkbit corrected error syndrome that resulted in SECDED ECC error. It is computed by XOR operation of incoming checkbits and computed checkbits of the incoming data bits. It indicates which bit is in error, or whether multiple bits are in Error. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8			**Reserved Field:** Yes

Table 3-146 Fields for Register: ECCCSYN2 (continued)

Bits	Name	Memory Access	Description
7:0	ecc_corr_syndromes_71_64	R	Indicates the data pattern that resulted in a correctable error. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, it represents the combined ECC byte spread over two DRAM beats for multibeat SECDED ECC, while for ADVECC, the upper nibble shall be ignored by the user. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.72 ECCBITMASK0

- **Name:** ECC Corrected Data Bit Mask Register 0
- **Description:** ECC Corrected Data Bit Mask Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10628
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

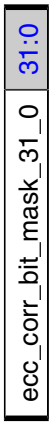


Table 3-147 Fields for Register: ECCBITMASK0

Bits	Name	Memory Access	Description
31:0	ecc_corr_bit_mask_31_0	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 16-bit DRAM data width, only bits [15:0] are used **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.73 ECCBITMASK1

- **Name:** ECC Corrected Data Bit Mask Register 1
- **Description:** ECC Corrected Data Bit Mask Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1062c
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH0.

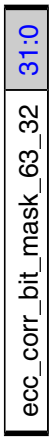


Table 3-148 Fields for Register: ECCBITMASK1

Bits	Name	Memory Access	Description
31:0	ecc_corr_bit_mask_63_32	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 32-bit DRAM data width and 16-bit DRAM data width operating in sideband SECDED or ADVECC mode, this register is not used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.74 ECCBITMASK2

- **Name:** ECC Corrected Data Bit Mask Register 2
- **Description:** ECC Corrected Data Bit Mask Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10630
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

Table 3-149 Fields for Register: ECCBITMASK2

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7:0	ecc_corr_bit_mask_71_64	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, the upper nibble shall be ignored by the user. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.75 ECCUADDR0

- **Name:** ECC Uncorrected Error Address Register 0
- **Description:** ECC Uncorrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10634
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

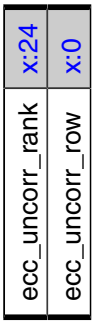


Table 3-150 Fields for Register: ECCUADDR0

Bits	Name	Memory Access	Description
x:24	ecc_uncorr_rank	R	Rank number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	ecc_uncorr_row	R	Page/row number of a read resulting in an uncorrected ECC error. This is 18-bits wide in configurations with LPDDR5 or DDR4 support and 16-bits in all other configurations. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.76 ECCUADDR1

- **Name:** ECC Uncorrected Error Address Register 1
- **Description:** ECC Uncorrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10638
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.

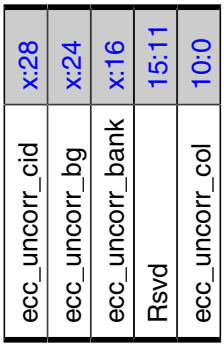


Table 3-151 Fields for Register: ECCUADDR1

Bits	Name	Memory Access	Description
x:28	ecc_uncorr_cid	R	CID number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "UMCTL2_CID_WIDTH" + 27
x:24	ecc_uncorr_bg	R	Bank Group number of a read resulting in an uncorrected ECC error. Note that when LPDDR5 16B mode is in use, this field is used as the upper bits of the bank address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	ecc_uncorr_bank	R	Bank number of a read resulting in an uncorrected ECC error. Note that when LPDDR5 16B mode is in use, {ECCUADDR1.ecc_uncorr_bg, ECCUADDR1.ecc_uncorr_bank[1:0]} shows bank number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-151 Fields for Register: ECCUADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	ecc_uncorr_col	R	Block number of a read resulting in an uncorrected ECC error (lowest bit not assigned here) **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.77 ECCUSYN0

- **Name:** ECC Uncorrected Syndrome Register 0
- **Description:** ECC Uncorrected Error Data Syndrome Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1063c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-152 Fields for Register: ECCUSYN0

Bits	Name	Memory Access	Description
31:0	ecc_uncorr_syndromes_31_0	R	Data pattern that resulted in an uncorrectable error. For 16-bit DRAM data width, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.78 ECCUSYN1

- **Name:** ECC Uncorrected Syndrome Register 1
- **Description:** ECC Uncorrected Error Data Syndrome Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10640
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_32__OR__MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-153 Fields for Register: ECCUSYN1

Bits	Name	Memory Access	Description
31:0	ecc_uncorr_syndromes_63_32	R	Data pattern that resulted in an uncorrected error. For 32-bit DRAM data width and 16-bit DRAM data width operating in single-beat SECDED or ADVECC mode, this register is not used. However, for multi-beat SECDED ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.79 ECCUSYN2

- **Name:** ECC Uncorrected Syndrome Register 2
- **Description:** ECC Uncorrected Error ECC Syndrome Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10644
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-154 Fields for Register: ECCUSYN2

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	cb_uncorr_syndrome	R	Indicates the Checkbit uncorrected error syndrome that resulted in SECDED ECC error. It is computed by XOR operation of incoming checkbits and computed checkbits of the incoming data bits. It indicates which bit is in error, or whether multiple bits are in Error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8			**Reserved Field:** Yes

Table 3-154 Fields for Register: ECCUSYN2 (continued)

Bits	Name	Memory Access	Description
7:0	ecc_uncorr_syndromes_71_64	R	Data pattern that resulted in an uncorrectable error. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, it represents the combined ECC byte spread over two DRAM beats for multibeat SECDED ECC, while for ADVECC, the upper nibble shall be ignored by the user. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.80 ECCPOISONADDR0

- **Name:** ECC Data Poisoning Address Register 0.
- **Description:** ECC Data Poisoning Address Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10648
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

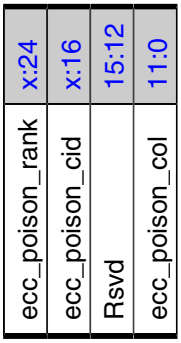


Table 3-155 Fields for Register: ECCPOISONADDR0

Bits	Name	Memory Access	Description
x:24	ecc_poison_rank	R/W	Rank address for ECC poisoning **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:16	ecc_poison_cid	R/W	Indicates the chip ID for ECC poisoning (DDR4 3DS only) This register must be set to 0 when DDR4 3DS feature is not used. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_CID_WIDTH" + 15
15:12			**Reserved Field:** Yes

Table 3-155 Fields for Register: ECCPOISONADDR0 (continued)

Bits	Name	Memory Access	Description
11:0	ecc_poison_col	R/W	Indicates the column address for ECC poisoning. Note that this column address must be burst aligned: ■ In full bus width mode, ecc_poison_col[2:0] must be set to 0 ■ In half bus width mode, ecc_poison_col[3:0] must be set to 0 ■ In quarter bus width mode, ecc_poison_col[4:0] must be set to 0 **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.81 ECCPOISONADDR1

- **Name:** ECC Data Poisoning Address Register 1.
- **Description:** ECC Data Poisoning Address Register 1.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1064c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

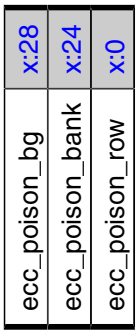


Table 3-156 Fields for Register: ECCPOISONADDR1

Bits	Name	Memory Access	Description
x:28	ecc_poison_bg	R/W	Bank Group address for ECC poisoning. Note that when LPDDR5 16B mode is in use, this field is used as the upper bits of the bank address for ECC poisoning. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "MEMC_BG_BITS" + 27
x:24	ecc_poison_bank	R/W	Bank address for ECC poisoning. Note that when LPDDR5 16B mode is in use, {ECCPOISONADDR1.ecc_poison_bg, ECCPOISONADDR1.ecc_poison_bank[1:0]} shows bank number for ECC poisoning. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "MEMC_BANK_BITS" + 23

Table 3-156 Fields for Register: ECCPOISONADDR1 (continued)

Bits	Name	Memory Access	Description
x:0	ecc_poison_row	R/W	Row address for ECC poisoning. This is 18-bits wide in configurations with LPDDR5 or DDR4 support and 16-bits in all other configurations. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.82 ECCAPSTAT

- **Name:** Address protection within ECC Status Register
- **Description:** Address protection within ECC Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10664
- **Exists:** MEMC_ECCAP==1

This register is in block REGB_DDRC_CH0.

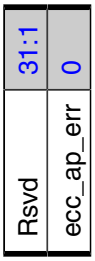


Table 3-157 Fields for Register: ECCAPSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	ecc_ap_err	R	Indicates the number of ECC errors (correctable/uncorrectable) within one burst exceeded the threshold.(ECCCFG0.ecc_ap_err_threshold) **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.83 OCPARCFG0

- **Name:** On-Chip Parity Configuration Register 0
- **Description:** On-Chip Parity Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10680
- **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

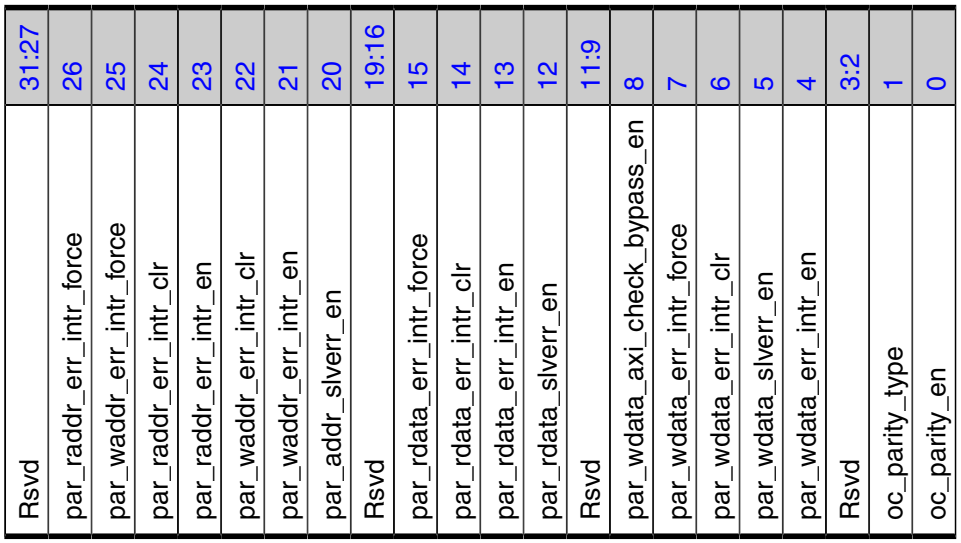


Table 3-158 Fields for Register: OCPARCFG0

Bits	Name	Memory Access	Description
31:27			**Reserved Field:** Yes
26	par_raddr_err_intr_force	R/W1C	Interrupt force bit for all par_raddr_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
25	par_waddr_err_intr_force	R/W1C	Interrupt force bit for all par_waddr_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-158 Fields for Register: OCPARCFG0 (continued)

Bits	Name	Memory Access	Description
24	par_raddr_err_intr_clr	R/W1C	Interrupt clear bit for all par_raddr_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23	par_raddr_err_intr_en	R/W	Enables interrupt generation, if set to 1, for all ports, on signal par_raddr_err_intr_n upon detection of parity error on the AXI interface. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
22	par_waddr_err_intr_clr	R/W1C	Interrupt clear bit for all par_waddr_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
21	par_waddr_err_intr_en	R/W	Enables interrupt generation, if set to 1, for all ports, on signal par_waddr_err_intr_n upon detection of parity error on the AXI interface. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
20	par_addr_slverr_en	R/W	Enables SLVERR generation on read response or write response when address parity error is detected at the AXI interface. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
19:16			**Reserved Field:** Yes
15	par_rdata_err_intr_force	R/W1C	Interrupt force bit for all par_rdata_err_intr_n and par_rdata_in_err_ecc_intr (Inline-ECC only). DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-158 Fields for Register: OCPARCFG0 (continued)

Bits	Name	Memory Access	Description
14	par_rdata_err_intr_clr	R/W1C	Interrupt clear bit for par_rdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13	par_rdata_err_intr_en	R/W	Enables interrupt generation, if set to 1, for all ports, on signal par_rdata_err_intr_n upon detection of parity error at the AXI interface. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
12	par_rdata_slverr_en	R/W	Enables SLVERR generation on read response when read data parity error is detected at the AXI interface. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
11:9			**Reserved Field:** Yes
8	par_wdata_axi_check_bypass_en	R/W	Register to bypass write data parity checker at AXI. If set to 1, write data parity checker at AXI is bypassed - incoming write data parity error or poisoned write data parity will be propagated to next block of the design. If set to 0, write data parity checker at AXI will detect the incoming write data parity error and report it onto the interrupt and bad parity is terminated - correct parity is propagated. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 3
7	par_wdata_err_intr_force	R/W1C	Interrupt force bit for par_wdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
6	par_wdata_err_intr_clr	R/W1C	Interrupt clear bit for par_wdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-158 Fields for Register: OCPARCFG0 (continued)

Bits	Name	Memory Access	Description
5	par_wdata_slverr_en	R/W	Enables SLVERR generation on write response when write data parity error is detected at the AXI interface. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
4	par_wdata_err_intr_en	R/W	Enables write data interrupt generation (par_wdata_err_intr) upon detection of parity error at the AXI or DFI interface. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Dynamic
3:2			**Reserved Field:** Yes
1	oc_parity_type	R/W	Parity type: ■ 0: Even parity ■ 1: Odd parity **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
0	oc_parity_en	R/W	Parity enable register. Enables On-Chip parity for all interfaces. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.84 OCPARCFG1

- **Name:** On-Chip Parity Configuration Register 1
- **Description:** On-Chip Parity Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10684
- **Exists:** UMCTL2_OCPAR_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

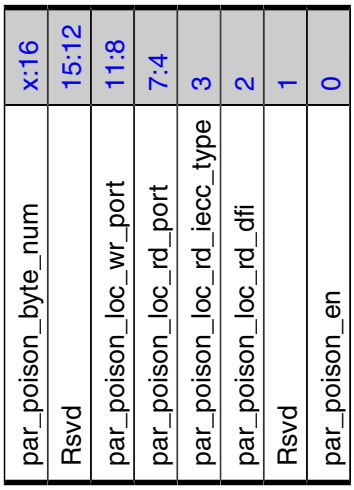


Table 3-159 Fields for Register: OCPARCFG1

Bits	Name	Memory Access	Description
x:16	par_poison_byte_num	R/W	Indicates the byte number (binary encoded) where the parity error is to be injected at the read data AXI interface. Error can be injected one byte at a time. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_DATARAM_PAR_DW_LG2" + 15
15:12			**Reserved Field:** Yes
11:8	par_poison_loc_wr_port	R/W	Enables parity poisoning on write data at the AXI interface before the input parity check logic. The value specifies the binary encoded port number of the AXI interface to be injected with parity error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-159 Fields for Register: OCPARCFG1 (continued)

Bits	Name	Memory Access	Description
7:4	par_poison_loc_rd_port	R/W	Enables parity poisoning on read data at the AXI interface after the parity check logic. The value specifies the binary encoded port number of the AXI interface to be injected with parity error. Error can be injected to one port at a time. An error injected here is not logged and does not trigger SLVERR or interrupt by the controller. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
3	par_poison_loc_rd_iecc_type	R/W	Selects which parity to poison at the DFI when inline ECC is enabled. If this register is set to 0, parity error is injected on the first read data going through the ECC path; if this register is set to 1, parity error is injected on the first read data going through the data path. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
2	par_poison_loc_rd_dfi	R/W	Enables parity poisoning on read data at the DFI interface after the parity generation logic, and when MEMC_INLINE_ECC=1 enables poisoning of ECC word after the ECC encoder at the write data interface at the DFI. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
1			**Reserved Field:** Yes
0	par_poison_en	R/W	Enables on-chip parity poisoning on the data interfaces. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.85 OCPARSTAT0

- **Name:** On-Chip Parity Status Register 0
- **Description:** On-Chip Parity Status Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10688
- **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
par_raddr_err_intr_15	par_raddr_err_intr_14	par_raddr_err_intr_13	par_raddr_err_intr_12	par_raddr_err_intr_11	par_raddr_err_intr_10	par_raddr_err_intr_9	par_raddr_err_intr_8	par_raddr_err_intr_7	par_raddr_err_intr_6	par_raddr_err_intr_5	par_raddr_err_intr_4	par_raddr_err_intr_3	par_raddr_err_intr_2	par_raddr_err_intr_1	par_raddr_err_intr_0	par_waddr_err_intr_15	par_waddr_err_intr_14	par_waddr_err_intr_13	par_waddr_err_intr_12	par_waddr_err_intr_11	par_waddr_err_intr_10	par_waddr_err_intr_9	par_waddr_err_intr_8	par_waddr_err_intr_7	par_waddr_err_intr_6	par_waddr_err_intr_5	par_waddr_err_intr_4	par_waddr_err_intr_3	par_waddr_err_intr_2	par_waddr_err_intr_1	par_waddr_err_intr_0

Table 3-160 Fields for Register: OCPARSTAT0

Bits	Name	Memory Access	Description
31	par_raddr_err_intr_15	R	Read address parity error interrupt for port 15. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
30	par_raddr_err_intr_14	R	Read address parity error interrupt for port 14. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
29	par_raddr_err_intr_13	R	Read address parity error interrupt for port 13. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-160 Fields for Register: OCPARSTAT0 (continued)

Bits	Name	Memory Access	Description
28	par_raddr_err_intr_12	R	Read address parity error interrupt for port 12. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
27	par_raddr_err_intr_11	R	Read address parity error interrupt for port 11. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
26	par_raddr_err_intr_10	R	Read address parity error interrupt for port 10. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
25	par_raddr_err_intr_9	R	Read address parity error interrupt for port 9. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
24	par_raddr_err_intr_8	R	Read address parity error interrupt for port 8. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
23	par_raddr_err_intr_7	R	Read address parity error interrupt for port 7. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
22	par_raddr_err_intr_6	R	Read address parity error interrupt for port 6. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-160 Fields for Register: OCPARSTAT0 (continued)

Bits	Name	Memory Access	Description
21	par_raddr_err_intr_5	R	Read address parity error interrupt for port 5. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
20	par_raddr_err_intr_4	R	Read address parity error interrupt for port 4. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
19	par_raddr_err_intr_3	R	Read address parity error interrupt for port 3. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
18	par_raddr_err_intr_2	R	Read address parity error interrupt for port 2. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
17	par_raddr_err_intr_1	R	Read address parity error interrupt for port 1. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
16	par_raddr_err_intr_0	R	Read address parity error interrupt for port 0. This interrupt is asserted when an on-chip read address parity error occurred on the corresponding AXI port's read address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
15	par_waddr_err_intr_15	R	Write address parity error interrupt for port 15. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-160 Fields for Register: OCPARSTAT0 (continued)

Bits	Name	Memory Access	Description
14	par_waddr_err_intr_14	R	Write address parity error interrupt for port 14. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
13	par_waddr_err_intr_13	R	Write address parity error interrupt for port 13. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
12	par_waddr_err_intr_12	R	Write address parity error interrupt for port 12. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
11	par_waddr_err_intr_11	R	Write address parity error interrupt for port 11. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
10	par_waddr_err_intr_10	R	Write address parity error interrupt for port 10. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
9	par_waddr_err_intr_9	R	Write address parity error interrupt for port 9. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-160 Fields for Register: OCPARSTAT0 (continued)

Bits	Name	Memory Access	Description
8	par_waddr_err_intr_8	R	Write address parity error interrupt for port 8. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
7	par_waddr_err_intr_7	R	Write address parity error interrupt for port 7. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
6	par_waddr_err_intr_6	R	Write address parity error interrupt for port 6. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
5	par_waddr_err_intr_5	R	Write address parity error interrupt for port 5. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
4	par_waddr_err_intr_4	R	Write address parity error interrupt for port 4. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
3	par_waddr_err_intr_3	R	Write address parity error interrupt for port 3. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
2	par_waddr_err_intr_2	R	Write address parity error interrupt for port 2. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-160 Fields for Register: OCPARSTAT0 (continued)

Bits	Name	Memory Access	Description
1	par_waddr_err_intr_1	R	Write address parity error interrupt for port 1. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static
0	par_waddr_err_intr_0	R	Write address parity error interrupt for port 0. This interrupt is asserted when an on-chip write address parity error occurred on the corresponding AXI port's write address channel. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.86 OCPARSTAT1

- **Name:** On-Chip Parity Status Register 1
- **Description:** On-Chip Parity Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1068c
- **Exists:** UMCTL2_OCPAR_EN_1==1

This register is in block REGB_DDRC_CH0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
par_rdata_err_intr_15	par_rdata_err_intr_14	par_rdata_err_intr_13	par_rdata_err_intr_12	par_rdata_err_intr_11	par_rdata_err_intr_10	par_rdata_err_intr_9	par_rdata_err_intr_8	par_rdata_err_intr_7	par_rdata_err_intr_6	par_rdata_err_intr_5	par_rdata_err_intr_4	par_rdata_err_intr_3	par_rdata_err_intr_2	par_rdata_err_intr_1	par_rdata_err_intr_0	par_wdata_in_err_intr_15	par_wdata_in_err_intr_14	par_wdata_in_err_intr_13	par_wdata_in_err_intr_12	par_wdata_in_err_intr_11	par_wdata_in_err_intr_10	par_wdata_in_err_intr_9	par_wdata_in_err_intr_8	par_wdata_in_err_intr_7	par_wdata_in_err_intr_6	par_wdata_in_err_intr_5	par_wdata_in_err_intr_4	par_wdata_in_err_intr_3	par_wdata_in_err_intr_2	par_wdata_in_err_intr_1	par_wdata_in_err_intr_0

Table 3-161 Fields for Register: OCPARSTAT1

Bits	Name	Memory Access	Description
31	par_rdata_err_intr_15	R	Read data parity error interrupt for port 15. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
30	par_rdata_err_intr_14	R	Read data parity error interrupt for port 14. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
29	par_rdata_err_intr_13	R	Read data parity error interrupt for port 13. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
28	par_rdata_err_intr_12	R	Read data parity error interrupt for port 12. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
27	par_rdata_err_intr_11	R	Read data parity error interrupt for port 11. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
26	par_rdata_err_intr_10	R	Read data parity error interrupt for port 10. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
25	par_rdata_err_intr_9	R	Read data parity error interrupt for port 9. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
24	par_rdata_err_intr_8	R	Read data parity error interrupt for port 8. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
23	par_rdata_err_intr_7	R	Read data parity error interrupt for port 7. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
22	par_rdata_err_intr_6	R	Read data parity error interrupt for port 6. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
21	par_rdata_err_intr_5	R	Read data parity error interrupt for port 5. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
20	par_rdata_err_intr_4	R	Read data parity error interrupt for port 4. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
19	par_rdata_err_intr_3	R	Read data parity error interrupt for port 3. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
18	par_rdata_err_intr_2	R	Read data parity error interrupt for port 2. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
17	par_rdata_err_intr_1	R	Read data parity error interrupt for port 1. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
16	par_rdata_err_intr_0	R	Read data parity error interrupt for port 0. This interrupt is asserted when an on-chip read data parity error occurred on the corresponding AXI port's read data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
15	par_wdata_in_err_intr_15	R	Write data parity error interrupt on input for port 15. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
14	par_wdata_in_err_intr_14	R	Write data parity error interrupt on input for port 14. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
13	par_wdata_in_err_intr_13	R	Write data parity error interrupt on input for port 13. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
12	par_wdata_in_err_intr_12	R	Write data parity error interrupt on input for port 12. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
11	par_wdata_in_err_intr_11	R	Write data parity error interrupt on input for port 11. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
10	par_wdata_in_err_intr_10	R	Write data parity error interrupt on input for port 10. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
9	par_wdata_in_err_intr_9	R	Write data parity error interrupt on input for port 9. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
8	par_wdata_in_err_intr_8	R	Write data parity error interrupt on input for port 8. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
7	par_wdata_in_err_intr_7	R	Write data parity error interrupt on input for port 7. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
6	par_wdata_in_err_intr_6	R	Write data parity error interrupt on input for port 6. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
5	par_wdata_in_err_intr_5	R	Write data parity error interrupt on input for port 5. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
4	par_wdata_in_err_intr_4	R	Write data parity error interrupt on input for port 4. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-161 Fields for Register: OCPARSTAT1 (continued)

Bits	Name	Memory Access	Description
3	par_wdata_in_err_intr_3	R	Write data parity error interrupt on input for port 3. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
2	par_wdata_in_err_intr_2	R	Write data parity error interrupt on input for port 2. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
1	par_wdata_in_err_intr_1	R	Write data parity error interrupt on input for port 1. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
0	par_wdata_in_err_intr_0	R	Write data parity error interrupt on input for port 0. This interrupt is asserted when an on-chip write data parity error occurred on the corresponding AXI port's write data channel. Bit 0 corresponds to Port 0, and so on. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.87 OCPARSTAT2

- **Name:** On-Chip Parity Status Register 2
- **Description:** On-Chip Parity Status Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10690
- **Exists:** UMCTL2_OCPAR_EN_1==1

This register is in block REGB_DDRC_CH0.

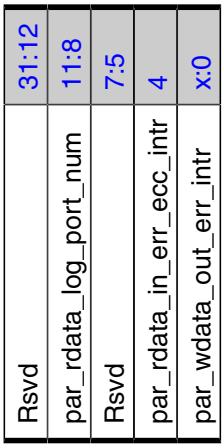


Table 3-162 Fields for Register: OCPARSTAT2

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11:8	par_rdata_log_port_num	R	Failing port number (binary encoded) of the last read data beat which resulted in on-chip parity error at the AXI interface. If there are more than one simultaneous port failures, the lower-indexed port is captured. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4	par_rdata_in_err_ecc_intr	R	Interrupt on ECC data going into inline ECC decoder. Cleared by par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-162 Fields for Register: OCPARSTAT2 (continued)

Bits	Name	Memory Access	Description
x:0	par_wdata_out_err_intr	R	Write data parity error interrupt on output. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_OCPAR_WDATA_OUT_ERR_WIDTH" - 1

3.2.88 OCPARSTAT3

- **Name:** On-Chip Parity Read Data Log Register 0
- **Description:** On-Chip Parity Read Data Log Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10694
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0

This register is in block REGB_DDRC_CH0.

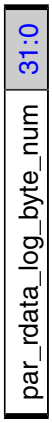


Table 3-163 Fields for Register: OCPARSTAT3

Bits	Name	Memory Access	Description
31:0	par_rdata_log_byte_num	R	Failing byte(s) number of the last read data beat which resulted in on-chip parity error at the AXI interface. This log reports failing bytes up to byte 31. In case, if the number of bytes at the AXI interface is less than 32, the unused upper par_rdata_log_byte_num bits are driven to '0' and must be ignored. For AXI interface with 64 bytes data width, the upper log byte number are reflected in OCPARSTAT8 register. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.89 OCPARSTAT4

- **Name:** On-Chip Parity Write Address Log Register 0
- **Description:** On-Chip Parity Write Address Log Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10698
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0

This register is in block REGB_DDRC_CH0.

Table 3-164 Fields for Register: OCPARSTAT4

Bits	Name	Memory Access	Description
31:0	par_waddr_log_low	R	AXI system address [31:0] of the last write transaction resulting in on-chip parity error on write address path at the AXI interface. Depending on the crossing delay, for back-to-back errors, last address may not be logged, instead the first address logged will be kept. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.90 OCPARSTAT5

- **Name:** On-Chip Parity Write Address Log Register 1
- **Description:** On-Chip Parity Write Address Log Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1069c
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0

This register is in block REGB_DDRC_CH0.

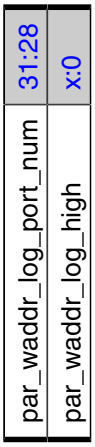


Table 3-165 Fields for Register: OCPARSTAT5

Bits	Name	Memory Access	Description
31:28	par_waddr_log_port_num	R	Failing port number (binary encoded) of the last write address transaction which resulted in on-chip parity error at the AXI interface. If there are more than one simultaneous port failures, the lower-indexed port is captured. **Value After Reset:** 0x0 **Programming Mode:** Static
x:0	par_waddr_log_high	R	AXI system address [59:32] of the last write transaction resulting in on-chip parity error on write address path at the AXI interface. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_OCPAR_ADDR_LOG_HIGH_WIDTH" - 1

3.2.91 OCPARSTAT6

- **Name:** On-Chip Parity Read Address Log Register 0
- **Description:** On-Chip Parity Read Address Log Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x106a0
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0

This register is in block REGB_DDRC_CH0.

Table 3-166 Fields for Register: OCPARSTAT6

Bits	Name	Memory Access	Description
31:0	par_raddr_log_low	R	AXI system address [31:0] of the last read transaction resulting in on-chip parity error on read address path at the AXI interface. Depending on the crossing delay, for back-to-back errors, last address may not be logged, instead the first address logged will be kept. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.92 OCPARSTAT7

- **Name:** On-Chip Parity Read Address Log Register 1
- **Description:** On-Chip Parity Read Address Log Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x106a4
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0

This register is in block REGB_DDRC_CH0.

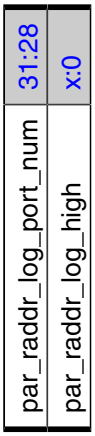


Table 3-167 Fields for Register: OCPARSTAT7

Bits	Name	Memory Access	Description
31:28	par_raddr_log_port_num	R	Failing port number (binary encoded) of the last read address transaction which resulted in on-chip parity error at the AXI interface. If there are more than one simultaneous port failures, the lower-indexed port is captured. **Value After Reset:** 0x0 **Programming Mode:** Static
x:0	par_raddr_log_high	R	AXI system address [59:32] of the last read transaction resulting in on-chip parity error on read address path at the AXI interface. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_OCPAR_ADDR_LOG_HIGH_WIDTH" - 1

3.2.93 OCPARSTAT8

- **Name:** On-Chip Parity Read Data Log Register 1
- **Description:** On-Chip Parity Read Data Log Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x106a8
- **Exists:** UMCTL2_OCPAR_EN_1==1 && MEMC_INLINE_ECC==0 && UMCTL2_MAX_XPI_PORT_DW_GTEQ_512==1

This register is in block REGB_DDRC_CH0.

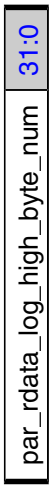


Table 3-168 Fields for Register: OCPARSTAT8

Bits	Name	Memory Access	Description
31:0	par_rdata_log_high_byte_num	R	Failing byte(s) number of the last read data beat which resulted in on-chip parity error at the AXI interface. This log reports failing bytes from byte 32 to byte 64. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.94 OCSAPCFG0

- **Name:** On-Chip external SRAM Address Protection Configuration Register 0
- **Description:** On-Chip external SRAM Address Protection Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x106b0
- **Exists:** DDRCTL_OCSAP_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

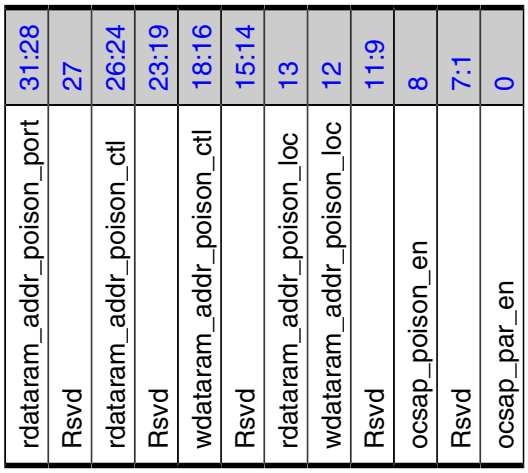


Table 3-169 Fields for Register: OCSAPCFG0

Bits	Name	Memory Access	Description
31:28	rdataram_addr_poison_port	R/W	The value specifies the binary encoded port number of the AXI interface for poisoning the associated RDATARAM address. Error can be injected to one port at a time. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
27			**Reserved Field:** Yes
26:24	rdataram_addr_poison_ctl	R/W	Selects rdataram address bit position (binary encoded) for poisoning. Note: The selected rdataram address bit position (binary encoded) shall be less than parameter value UMCTL2_RDATARAM_AW. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
23:19			**Reserved Field:** Yes

Table 3-169 Fields for Register: OCSAPCFG0 (continued)

Bits	Name	Memory Access	Description
18:16	wdataram_addr_poison_ctl	R/W	Selects wdataram address bit position (binary encoded) for poisoning. Note: The selected wdataram address bit position (binary encoded) shall be less than parameter value UMCTL2_WDATARAM_AW. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
15:14			**Reserved Field:** Yes
13	rdataram_addr_poison_loc	R/W	Selects rdataram address poisoning either for write address or read address. ■ 0 - Poison SRAM write address ■ 1 - Poison SRAM read address **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
12	wdataram_addr_poison_loc	R/W	Selects wdataram address poisoning either for write address or read address. ■ 0 - Poison SRAM write address ■ 1 - Poison SRAM read address **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
11:9			**Reserved Field:** Yes
8	ocsap_poison_en	R/W	Enables On-Chip external SRAM address poisoning. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
7:1			**Reserved Field:** Yes
0	ocsap_par_en	R/W	Enables On-Chip external SRAM address parity. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.95 OCECCCFG0

- **Name:** On-Chip ECC Configuration Register 0
- **Description:** On-Chip ECC Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10700
- **Exists:** UMCTL2_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

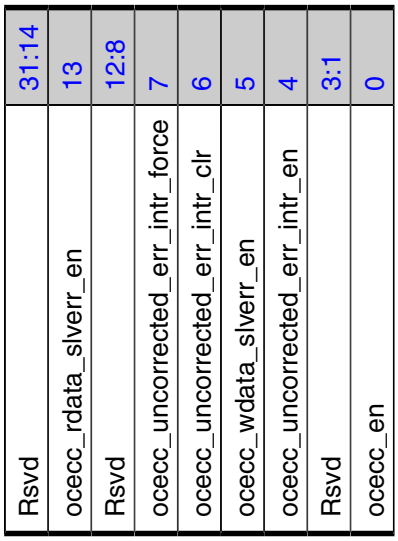


Table 3-170 Fields for Register: OCECCCFG0

Bits	Name	Memory Access	Description
31:14			**Reserved Field:** Yes
13	ocecc_rdata_slverr_en	R/W	Enables SLVERR generation on read responses. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
12:8			**Reserved Field:** Yes
7	ocecc_uncorrected_err_intr_force	R/W1C	Interrupt force bit for ocecc_uncorrected_err_intr. When this bit is set to 1, the OCECCSTAT0.ocecc_uncorrected_err field and the ocecc_uncorrected_err_intr pin will be set. The DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-170 Fields for Register: OCECCCFG0 (continued)

Bits	Name	Memory Access	Description
6	ococc_uncorrected_err_intr_clr	R/W1C	Interrupt clear bit for ococc_uncorrected_err_intr. The DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5	ococc_wdata_slverr_en	R/W	Enables SLVERR generation on write responses. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
4	ococc_uncorrected_err_intr_en	R/W	Enables uncorrected error interrupt generation. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
3:1			**Reserved Field:** Yes
0	ococc_en	R/W	OCECC enable register. Enables On-Chip ECC for all interfaces. Note - OCPARCFG0.oc_parity_en register must be set to 1 to enable On-chip ECC functionality. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.96 OCECCCFG1

- **Name:** On-Chip ECC Configuration Register 1
- **Description:** On-Chip ECC Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10704
- **Exists:** UMCTL2_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

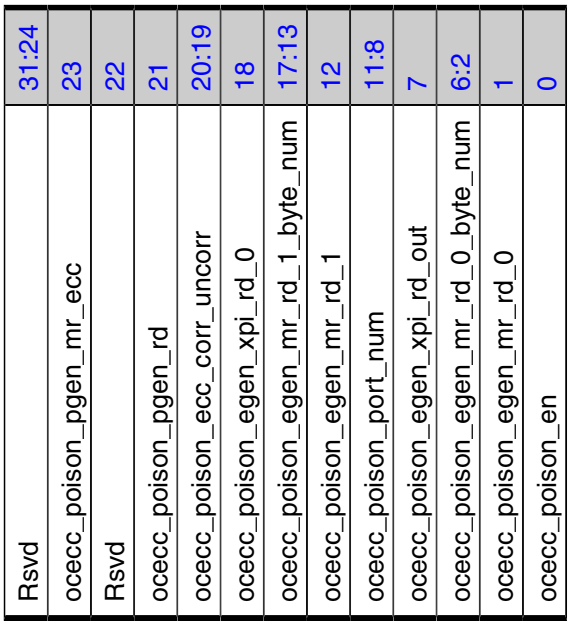


Table 3-171 Fields for Register: OCECCCFG1

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23	ocecc_poison_pgen_mr_ecc	R/W	Poisons parity for write ECC data. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
22			**Reserved Field:** Yes
21	ocecc_poison_pgen_rd	R/W	Poisons parity for read ECC data. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-171 Fields for Register: OCECCCFG1 (continued)

Bits	Name	Memory Access	Description
20:19	ocecc_poison_ecc_corr_uncorr	R/W	Selects either to inject 1 or 2 bit error in one of the ECC encoders. ■ 1 Injects single bit error ■ 2 Injects double bit error ■ 0 and 3 unused **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
18	ocecc_poison_egen_xpi_rd_0	R/W	Poisons the ECC encoder for the read data of a Read command. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
17:13	ocecc_poison_egen_mr_rd_1_byte_num	R/W	Byte number to poison for the read data of an RMW command ECC encoder. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
12	ocecc_poison_egen_mr_rd_1	R/W	Poisons the ECC encoder for the read data of an RMW command. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
11:8	ocecc_poison_port_num	R/W	Selects in which port to poison the ECC encoder. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
7	ocecc_poison_egen_xpi_rd_out	R/W	Poisons the ECC encoder at the AXI read data interface. This will not cause any interrupt to flag. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

Table 3-171 Fields for Register: OCECCCFG1 (continued)

Bits	Name	Memory Access	Description
6:2	ocecc_poison_egen_mr_rd_0_byte_num	R/W	Byte number to poison for the AXI write data interface ECC encoder. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
1	ocecc_poison_egen_mr_rd_0	R/W	Poisons the ECC encoder at the AXI write data interface. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3
0	ocecc_poison_en	R/W	Enables poisoning of ECC encoders and parity generators. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.97 OCECCSTAT0

- **Name:** On-Chip ECC Status Register 0
- **Description:** On-Chip ECC Status Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10708
- **Exists:** UMCTL2_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.

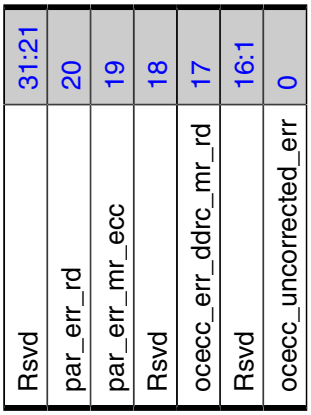


Table 3-172 Fields for Register: OCECCSTAT0

Bits	Name	Memory Access	Description
31:21			**Reserved Field:** Yes
20	par_err_rd	R	Parity error for read ECC data. **Value After Reset:** 0x0 **Programming Mode:** Static
19	par_err_mr_ecc	R	Parity error for write ECC data. **Value After Reset:** 0x0 **Programming Mode:** Static
18			**Reserved Field:** Yes
17	ocecc_err_ddrc_mr_rd	R	ECC error for write data RAM. **Value After Reset:** 0x0 **Programming Mode:** Static
16:1			**Reserved Field:** Yes
0	ocecc_uncorrected_err	R	ECC uncorrected error or parity error detected in one of the ECC decoders/Parity checkers. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.98 OCECCSTAT1

- **Name:** On-Chip ECC Status Register 1
- **Description:** On-Chip ECC Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1070c
- **Exists:** UMCTL2_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ocecc_err_xpi_rd_15	ocecc_err_xpi_rd_14	ocecc_err_xpi_rd_13	ocecc_err_xpi_rd_12	ocecc_err_xpi_rd_11	ocecc_err_xpi_rd_10	ocecc_err_xpi_rd_9	ocecc_err_xpi_rd_8	ocecc_err_xpi_rd_7	ocecc_err_xpi_rd_6	ocecc_err_xpi_rd_5	ocecc_err_xpi_rd_4	ocecc_err_xpi_rd_3	ocecc_err_xpi_rd_2	ocecc_err_xpi_rd_1	ocecc_err_xpi_rd_0	ocecc_err_xpi_wr_in_15	ocecc_err_xpi_wr_in_14	ocecc_err_xpi_wr_in_13	ocecc_err_xpi_wr_in_12	ocecc_err_xpi_wr_in_11	ocecc_err_xpi_wr_in_10	ocecc_err_xpi_wr_in_9	ocecc_err_xpi_wr_in_8	ocecc_err_xpi_wr_in_7	ocecc_err_xpi_wr_in_6	ocecc_err_xpi_wr_in_5	ocecc_err_xpi_wr_in_4	ocecc_err_xpi_wr_in_3	ocecc_err_xpi_wr_in_2	ocecc_err_xpi_wr_in_1	ocecc_err_xpi_wr_in_0

Table 3-173 Fields for Register: OCECCSTAT1

Bits	Name	Memory Access	Description
31	ocecc_err_xpi_rd_15	R	OCECC read data error detected in AXI port 15. **Value After Reset:** 0x0 **Programming Mode:** Static
30	ocecc_err_xpi_rd_14	R	OCECC read data error detected in AXI port 14. **Value After Reset:** 0x0 **Programming Mode:** Static
29	ocecc_err_xpi_rd_13	R	OCECC read data error detected in AXI port 13. **Value After Reset:** 0x0 **Programming Mode:** Static
28	ocecc_err_xpi_rd_12	R	OCECC read data error detected in AXI port 12. **Value After Reset:** 0x0 **Programming Mode:** Static
27	ocecc_err_xpi_rd_11	R	OCECC read data error detected in AXI port 11. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-173 Fields for Register: OCECCSTAT1 (continued)

Bits	Name	Memory Access	Description
26	ocecc_err_xpi_rd_10	R	OCECC read data error detected in AXI port 10. **Value After Reset:** 0x0 **Programming Mode:** Static
25	ocecc_err_xpi_rd_9	R	OCECC read data error detected in AXI port 9. **Value After Reset:** 0x0 **Programming Mode:** Static
24	ocecc_err_xpi_rd_8	R	OCECC read data error detected in AXI port 8. **Value After Reset:** 0x0 **Programming Mode:** Static
23	ocecc_err_xpi_rd_7	R	OCECC read data error detected in AXI port 7. **Value After Reset:** 0x0 **Programming Mode:** Static
22	ocecc_err_xpi_rd_6	R	OCECC read data error detected in AXI port 6. **Value After Reset:** 0x0 **Programming Mode:** Static
21	ocecc_err_xpi_rd_5	R	OCECC read data error detected in AXI port 5. **Value After Reset:** 0x0 **Programming Mode:** Static
20	ocecc_err_xpi_rd_4	R	OCECC read data error detected in AXI port 4. **Value After Reset:** 0x0 **Programming Mode:** Static
19	ocecc_err_xpi_rd_3	R	OCECC read data error detected in AXI port 3. **Value After Reset:** 0x0 **Programming Mode:** Static
18	ocecc_err_xpi_rd_2	R	OCECC read data error detected in AXI port 2. **Value After Reset:** 0x0 **Programming Mode:** Static
17	ocecc_err_xpi_rd_1	R	OCECC read data error detected in AXI port 1. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-173 Fields for Register: OCECCSTAT1 (continued)

Bits	Name	Memory Access	Description
16	ocecc_err_xpi_rd_0	R	OCECC read data error detected in AXI port 0. **Value After Reset:** 0x0 **Programming Mode:** Static
15	ocecc_err_xpi_wr_in_15	R	OCECC write data error detected in AXI port 15. **Value After Reset:** 0x0 **Programming Mode:** Static
14	ocecc_err_xpi_wr_in_14	R	OCECC write data error detected in AXI port 14. **Value After Reset:** 0x0 **Programming Mode:** Static
13	ocecc_err_xpi_wr_in_13	R	OCECC write data error detected in AXI port 13. **Value After Reset:** 0x0 **Programming Mode:** Static
12	ocecc_err_xpi_wr_in_12	R	OCECC write data error detected in AXI port 12. **Value After Reset:** 0x0 **Programming Mode:** Static
11	ocecc_err_xpi_wr_in_11	R	OCECC write data error detected in AXI port 11. **Value After Reset:** 0x0 **Programming Mode:** Static
10	ocecc_err_xpi_wr_in_10	R	OCECC write data error detected in AXI port 10. **Value After Reset:** 0x0 **Programming Mode:** Static
9	ocecc_err_xpi_wr_in_9	R	OCECC write data error detected in AXI port 9. **Value After Reset:** 0x0 **Programming Mode:** Static
8	ocecc_err_xpi_wr_in_8	R	OCECC write data error detected in AXI port 8. **Value After Reset:** 0x0 **Programming Mode:** Static
7	ocecc_err_xpi_wr_in_7	R	OCECC write data error detected in AXI port 7. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-173 Fields for Register: OCECCSTAT1 (continued)

Bits	Name	Memory Access	Description
6	ocecc_err_xpi_wr_in_6	R	OCECC write data error detected in AXI port 6. **Value After Reset:** 0x0 **Programming Mode:** Static
5	ocecc_err_xpi_wr_in_5	R	OCECC write data error detected in AXI port 5. **Value After Reset:** 0x0 **Programming Mode:** Static
4	ocecc_err_xpi_wr_in_4	R	OCECC write data error detected in AXI port 4. **Value After Reset:** 0x0 **Programming Mode:** Static
3	ocecc_err_xpi_wr_in_3	R	OCECC write data error detected in AXI port 3. **Value After Reset:** 0x0 **Programming Mode:** Static
2	ocecc_err_xpi_wr_in_2	R	OCECC write data error detected in AXI port 2. **Value After Reset:** 0x0 **Programming Mode:** Static
1	ocecc_err_xpi_wr_in_1	R	OCECC write data error detected in AXI port 1. **Value After Reset:** 0x0 **Programming Mode:** Static
0	ocecc_err_xpi_wr_in_0	R	OCECC write data error detected in AXI port 0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.99 OCECCSTAT2

- **Name:** On-Chip ECC Status Register 2
- **Description:** On-Chip ECC Status Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10710
- **Exists:** UMCTL2_OCECC_EN_1==1

This register is in block REGB_DDRC_CH0.

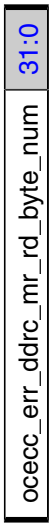


Table 3-174 Fields for Register: OCECCSTAT2

Bits	Name	Memory Access	Description
31:0	ocecc_err_ddrc_mr_rd_byte_num	R	Byte index which caused an ECC error at the write data RAM. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.100 OCCAPCFG

- **Name:** On-Chip command/Address Protection Configuration Register
- **Description:** On-Chip command/Address Protection Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10780
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

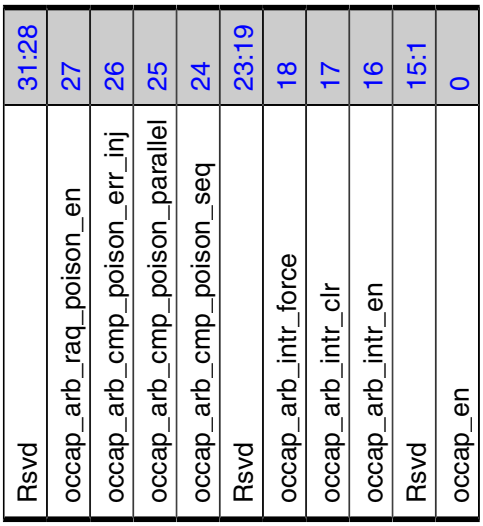


Table 3-175 Fields for Register: OCCAPCFG

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27	occap_arb_raq_poison_en	R/W	Enables poisoning for the Read Address Queues (RAQ) inside each XPI. Poisoning inverts all parity bits generated by the parity generator. Error will be flagged as soon as the first RAQ is read. This register is not cleared automatically and must be reprogrammed to 0 at the end of the operation. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-175 Fields for Register: OCCAPCFG (continued)

Bits	Name	Memory Access	Description
26	occap_arb_cmp_poison_err_inj	R/W	Enable error injection in the poisoning of OCCAP Arbiter logic Injects error into poisoning logic (either parallel or seq) such that XOR logic for one signal is not poisoned when expected. If set, it allows ability to corrupt the following register fields. ■ 1'b0: OCCAPSTAT.occap_arb_cmp_poison_parallel/seq_err=0 ■ 1'b1: OCCAPSTAT.occap_arb_cmp_poison_parallel/seq_err=1 Do not change value in same APB write as setting of occap_arb_cmp_poison_parallel/_seq **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	occap_arb_cmp_poison_parallel	R/W1C	Enables full poisoning for compare logic inside XPI. Poisoning inverts all bits of all outputs coming from the duplicated modules before the XOR comparators together. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
24	occap_arb_cmp_poison_seq	R/W1C	Enables poisoning for compare logic inside XPI. Poisoning inverts all bits coming from the duplicated modules before the XOR comparators one output at the time per each comparator. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:19			**Reserved Field:** Yes
18	occap_arb_intr_force	R/W1C	Interrupt force bit for occap_arb_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-175 Fields for Register: OCCAPCFG (continued)

Bits	Name	Memory Access	Description
17	occap_arb_intr_clr	R/W1C	Interrupt clear bit for occap_arb_err_intr and occap_arb_cmp_poison_complete. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	occap_arb_intr_en	R/W	Enables interrupt generation upon detection of OCCAP Arbiter errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
15:1			**Reserved Field:** Yes
0	occap_en	R/W	On Chip Command/Address Path Protection (OCCAP) enable register. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3

3.2.101 OCCAPSTAT

- **Name:** On-Chip command/Address Protection Status Register
- **Description:** On-Chip command/Address Protection Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10784
- **Exists:** UMCTL2_OCCAP_EN_1==1 && UMCTL2_INCL_ARB==1

This register is in block REGB_DDRC_CH0.

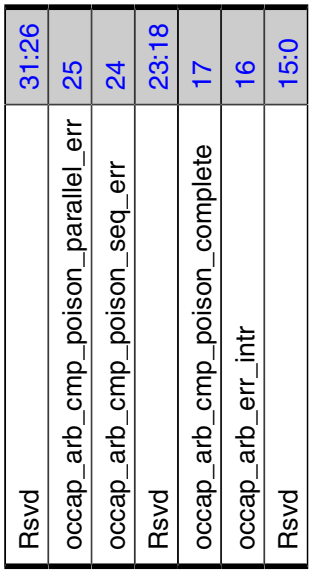


Table 3-176 Fields for Register: OCCAPSTAT

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25	occap_arb_cmp_poison_parallel_err	R	Error when occap_arb_cmp_poison_full_en was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_arb_cmp_poison_full_en. It checks for error on all of the the corresponding XOR outputs. If multi-bit, checks also that all XOR bits are set. Register is valid when occap_arb_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static

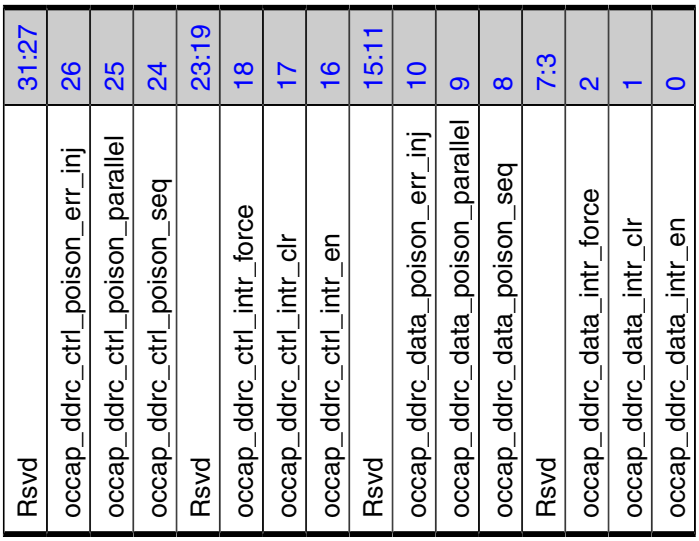
Table 3-176 Fields for Register: OCCAPSTAT (continued)

Bits	Name	Memory Access	Description
24	occap_arb_cmp_poison_seq_err	R	Error when occap_arb_cmp_poison_en was active due to incorrect no. of errors being occurring. Internal logic checks that the correct number of errors detected while poisoning one output at the time occurred for occap_arb_cmp_poison_en. It checks for error on one output at the time. Register is valid when occap_arb_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static
23:18			**Reserved Field:** Yes
17	occap_arb_cmp_poison_complete	R	OCCAP ARB comparator poisoning complete interrupt status. Register cleared by OCCAPCFG.occap_arb_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
16	occap_arb_err_intr	R	OCCAP Arbiter error interrupt status. Register cleared by OCCAPCFG.occap_arb_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
15:0			**Reserved Field:** Yes

3.2.102 OCCAPCFG1

- **Name:** On-Chip command/Address Protection Configuration Register 1
- **Description:** On-Chip command/Address Protection Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10788
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:27	26	25	24	23:19	18	17	16	15:11	10	9	8	7:3	2	1	0
Rsvd	occap_ddrc_ctrl_poison_err_inj	occap_ddrc_ctrl_poison_parallel	occap_ddrc_ctrl_poison_seq	Rsvd	occap_ddrc_ctrl_intr_force	occap_ddrc_ctrl_intr_clr	occap_ddrc_ctrl_intr_en	Rsvd	occap_ddrc_data_poison_err_inj	occap_ddrc_data_poison_parallel	occap_ddrc_data_poison_seq	Rsvd	occap_ddrc_data_intr_force	occap_ddrc_data_intr_clr	occap_ddrc_data_intr_en

Table 3-177 Fields for Register: OCCAPCFG1

Bits	Name	Memory Access	Description
31:27			**Reserved Field:** Yes
26	occap_ddrc_ctrl_poison_err_inj	R/W	Enable error injection in the poisoning of OCCAP DDRC CTRL logic Injects error into poisoning logic (either parallel or seq) such that XOR logic for one signal is not poisoned when expected. If set, it allows ability to corrupt the following register fields. ■ 1'b0: OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel/seq_err=0 ■ 1'b1: OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel/seq_err=1 Do not change value in same APB write as setting of occap_ddrc_ctrl_poison_parallel/_seq **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-177 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
25	occap_ddrc_ctrl_poison_parallel	R/W1C	Enables poisoning of OCCAP DDRC CTRL logic for all parts of comparison logic, in parallel. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting a ddrc_ctrl[0]'s signal to XOR logic. ddrc_ctrl[1] related signals are never poisoned. All signals are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
24	occap_ddrc_ctrl_poison_seq	R/W1C	Enables poisoning of OCCAP DDRC CTRL logic for all parts of comparison logic, in sequence. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting a ddrc_ctrl[0]'s signal to XOR logic. ddrc_ctrl[1] related signals are never poisoned. Each signal from ddrc_ctrl[0] is poisoned in series and checks in turn, that each signal was poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_ctrl_poison_seq_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:19			**Reserved Field:** Yes
18	occap_ddrc_ctrl_intr_force	R/W1C	Interrupt force bit for occap_ddrc_ctrl_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	occap_ddrc_ctrl_intr_clr	R/W1C	Interrupt clear bit for occap_ddrc_ctrl_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-177 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
16	occap_ddrc_ctrl_intr_en	R/W	Enables interrupt generation on signal occap_ddrc_ctrl_err_intr upon detection of OCCAP DDRC CTRL errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
15:11			**Reserved Field:** Yes
10	occap_ddrc_data_poison_err_inj	R/W	Enable error injection in the poisoning of OCCAP DDRC DATA logic Injects error into poisoning logic (either parallel or seq) such that XOR logic for one signal is not poisoned when expected. If set, it allows ability to corrupt the following register fields. ■ 1'b0: OCCAPSTAT1.occap_ddrc_data_poison_parallel/seq_err=0 ■ 1'b1: OCCAPSTAT1.occap_ddrc_data_poison_parallel/seq_err=1 Do not change value in same APB write as setting of occap_ddrc_data_poison_parallel/_seq **Value After Reset:** 0x0 **Programming Mode:** Dynamic
9	occap_ddrc_data_poison_parallel	R/W1C	Enables poisoning of OCCAP DDRC DATA logic for all parts of comparison logic, in parallel. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting all bits of a signal to XOR logic. All signals of instance[0] of the duplicated modules are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_data_poison_parallel_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-177 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
8	occap_ddrc_data_poison_seq	R/W1C	Enables poisoning of OCCAP DDRC DATA logic for all parts of comparison logic, in sequence. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting all bits of a signal to XOR logic. All signals of instance[0] of the duplicated modules are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_data_poison_seq_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7:3			**Reserved Field:** Yes
2	occap_ddrc_data_intr_force	R/W1C	Interrupt force bit for occap_ddrc_data_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	occap_ddrc_data_intr_clr	R/W1C	Interrupt clear bit for occap_ddrc_data_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	occap_ddrc_data_intr_en	R/W	Enables interrupt generation on signal occap_ddrc_data_err_intr upon detection of OCCAP DDRC DATA errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.103 OCCAPSTAT1

- **Name:** On-Chip command/Address Protection Status Register 1
- **Description:** On-Chip command/Address Protection Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1078c
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH0.

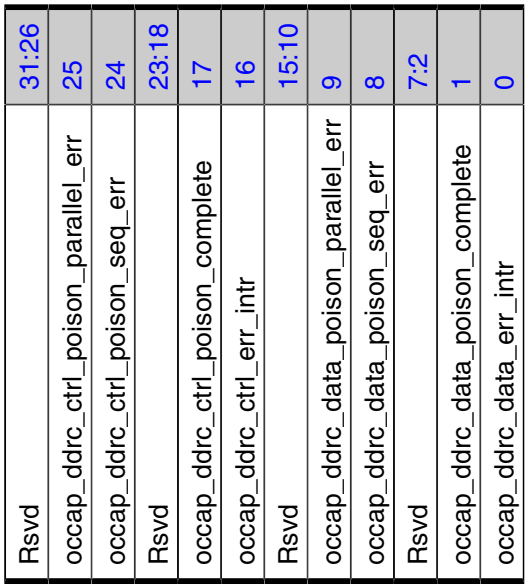


Table 3-178 Fields for Register: OCCAPSTAT1

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25	occap_ddrc_ctrl_poison_parallel_err	R	Error when occap_ddrc_ctrl_poison_parallel was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_ctrl_poison_parallel. It checks for error on all of the the corresponding XOR outputs. If multi-bit, checks also that all XOR bits are set. It checks all XOR in parallel. Register is valid only when occap_ddrc_ctrl_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-178 Fields for Register: OCCAPSTAT1 (continued)

Bits	Name	Memory Access	Description
24	occap_ddrc_ctrl_poison_seq_err	R	Error when occap_ddrc_ctrl_poison_seq was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_ctrl_poison_seq. It checks for error on all of the corresponding XOR outputs. It checks each XOR sequentially. Register is valid only when occap_ddrc_ctrl_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static
23:18			**Reserved Field:** Yes
17	occap_ddrc_ctrl_poison_complete	R	OCCAP DDRC CTRL poisoning complete interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_ctrl_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
16	occap_ddrc_ctrl_err_intr	R	OCCAP DDRC CTRL error interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_ctrl_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
15:10			**Reserved Field:** Yes
9	occap_ddrc_data_poison_parallel_err	R	Error when occap_ddrc_data_poison_parallel was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_data_poison_parallel. It checks for error on all of the the corresponding XOR outputs. If multi-bit, checks also that all XOR bits are set. It checks all XOR in parallel. This is cleared when OCCAPCFG1.occap_ddrc_data_poison_parallel=0 occurs. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-178 Fields for Register: OCCAPSTAT1 (continued)

Bits	Name	Memory Access	Description
8	occap_ddrc_data_poison_seq_err	R	Error when occap_ddrc_data_poison_seq was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_data_poison_seq. It checks for error on all of the corresponding XOR outputs. It checks each XOR sequentially. This is cleared when OCCAPCFG1.occap_ddrc_data_poison_seq=0 occurs. **Value After Reset:** 0x0 **Programming Mode:** Static
7:2			**Reserved Field:** Yes
1	occap_ddrc_data_poison_complete	R	OCCAP DDRC DATA poisoning complete interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_data_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
0	occap_ddrc_data_err_intr	R	OCCAP DDRC DATA error interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_data_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.104 OCCAPCFG2

- **Name:** On-Chip command/Address Protection Configuration Register 2
- **Description:** On-Chip command/Address Protection Configuration Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10790
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH0.

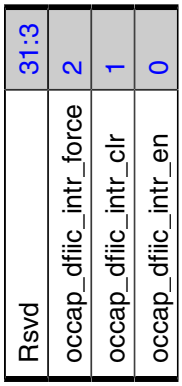


Table 3-179 Fields for Register: OCCAPCFG2

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	occap_dfiic_intr_force	R/W1C	Interrupt force bit for occap_dfiic_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	occap_dfiic_intr_clr	R/W1C	Interrupt clear bit for occap_dfiic_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	occap_dfiic_intr_en	R/W	Enables interrupt generation on signal occap_dfiic_err_intr upon detection of OCCAP DFI interconnect errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.105 OCCAPSTAT2

- **Name:** On-Chip command/Address Protection Status Register 2
- **Description:** On-Chip command/Address Protection Status Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10794
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH0.

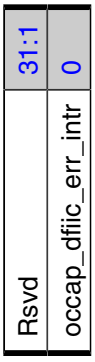


Table 3-180 Fields for Register: OCCAPSTAT2

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	occap_dfiic_err_intr	R	OCCAP DFI interconnect error interrupt status. Register cleared by OCCAPCFG2.occap_dfiic_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.106 REGPARCFG

- **Name:** Register Parity Configuration Register
- **Description:** Register Parity Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10880
- **Exists:** UMCTL2_REGPAR_EN_1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

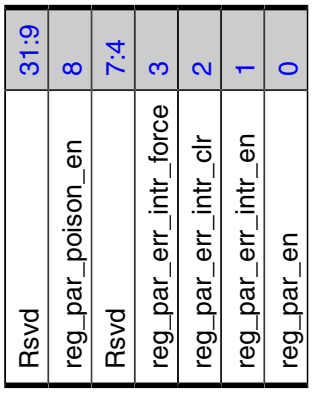


Table 3-181 Fields for Register: REGPARCFG

Bits	Name	Memory Access	Description
31:9			**Reserved Field:** Yes
8	reg_par_poison_en	R/W	Enable Register Parity poisoning. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:4			**Reserved Field:** Yes
3	reg_par_err_intr_force	R/W1C	Interrupt force bit for reg_par_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-181 Fields for Register: REGPARCFG (continued)

Bits	Name	Memory Access	Description
2	reg_par_err_intr_clr	R/W1C	Interupt clear bit for reg_par_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	reg_par_err_intr_en	R/W	Enables interrupt generation, if set to 1, on signal reg_par_err_intr upon detection of register parity error. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
0	reg_par_en	R/W	Register Parity enable register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.107 REGPARSTAT

- **Name:** Register Parity Status Register
- **Description:** Register Parity Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10884
- **Exists:** UMCTL2_REGPAR_EN_1

This register is in block REGB_DDRC_CH0.

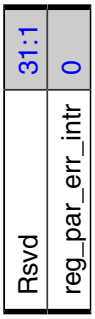


Table 3-182 Fields for Register: REGPARSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	reg_par_err_intr	R	Interrupt asserted when Register Parity error is detected. Cleared by setting REGPARCFG.reg_par_err_intr_clr to 1. **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.108 LNKECCCTL1

- **Name:** Link-ECC Control Register 1
- **Description:** Link-ECC Control Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10984
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.
Note: Do not perform any APB access to LNKECCCTL1 within 32 pclk cycles of previous access to LNKECCCTL1, as this might lead to data loss.

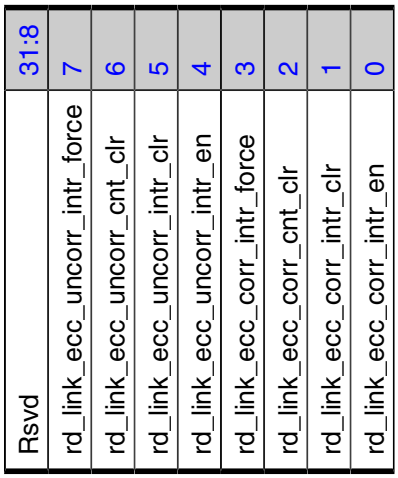


Table 3-183 Fields for Register: LNKECCCTL1

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7	rd_link_ecc_uncorr_intr_force	R/W1C	Interrupt force bit for rd_linkecc_uncorr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
6	rd_link_ecc_uncorr_cnt_clr	R/W1C	Clear all Read Link-ECC uncorrectable error count. If this bit set,LNKECCERRCNT0.rd_link_ecc_uncorr_cnt will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-183 Fields for Register: LNKECCCTL1 (continued)

Bits	Name	Memory Access	Description
5	rd_link_ecc_uncorr_intr_clr	R/W1C	Clear Read Link-ECC uncorrectable error interrupt. If this bit set, rd_linkecc_uncorr_err_intr will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rd_link_ecc_uncorr_intr_en	R/W	Interrupt enable bit for Read Link-ECC uncorrectable error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3	rd_link_ecc_corr_intr_force	R/W1C	Interrupt force bit for rd_linkecc_corr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rd_link_ecc_corr_cnt_clr	R/W1C	Clear all Read Link-ECC correctable error count. If this bit set,LNKECCERRCNT0.rd_link_ecc_corr_cnt will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rd_link_ecc_corr_intr_clr	R/W1C	Clear Read Link-ECC correctable error interrupt. If this bit set, rd_linkecc_corr_err_intr will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	rd_link_ecc_corr_intr_en	R/W	Interrupt enable bit for Read Link-ECC correctable error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.109 LNKECCPOISONCTL0

- **Name:** Link-ECC Poison Control Register 0
- **Description:** Link-ECC Poison Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10988
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

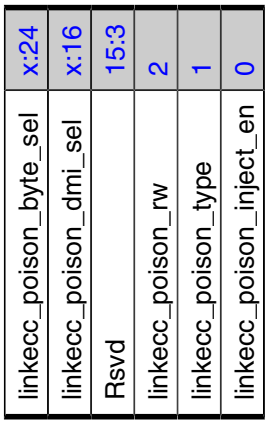


Table 3-184 Fields for Register: LNKECCPOISONCTL0

Bits	Name	Memory Access	Description
x:24	linkecc_poison_byte_sel	R/W	Select target byte(s) of Data for Read/Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to Data[N*8+:8]. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/8" + 23
x:16	linkecc_poison_dmi_sel	R/W	Select target DMI(s) of Data for Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to DMI[N]. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/8" + 15
15:3			**Reserved Field:** Yes

Table 3-184 Fields for Register: LNKECCPOISONCTL0 (continued)

Bits	Name	Memory Access	Description
2	linkecc_poison_rw	R/W	Indicates whether the Link-ECC poisoning operation is Read or Write. ■ 0 - Write ■ 1 - Read **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	linkecc_poison_type	R/W	Indicates whether the Link-ECC poisoning operation is Single-bit error or Double bit error. ■ 0 - Single bit Error ■ 1 - Double bit Error **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	linkecc_poison_inject_en	R/W	Setting this register bit to 1 triggers the Link-ECC poisoning. Once Link-ECC is poisoned to a ECC code, the ECC poisoning is completed automatically and LNKECCPOISONSTAT.linkecc_poison_complete becomes 1. Please make sure that LNKECCPOISONSTAT.linkecc_poison_complete==0 before writing this register to 1. Note: Link ECC feature must be enabled (LNKECCCTL0.wr_link_ecc_enable for Write Link ECC and LNKECCCTL0.rd_link_ecc_enable for Read Link ECC) when Link ECC poisoning feature is used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.110 LNKECCPOISONSTAT

- **Name:** Link-ECC Poison Status Register
- **Description:** Link-ECC Poison Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1098c
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

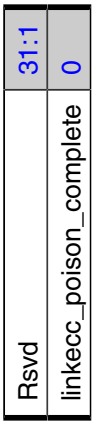


Table 3-185 Fields for Register: LNKECCPOISONSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	linkecc_poison_complete	R	Indicates Link-ECC poisoning operation is done. ■ 0 - Link-ECC poisoning is not completed ■ 1 - Link-ECC poisoning is completed **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.111 LNKECCINDEX

- **Name:** Link-ECC Index Register
- **Description:** Link-ECC Index Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10990
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

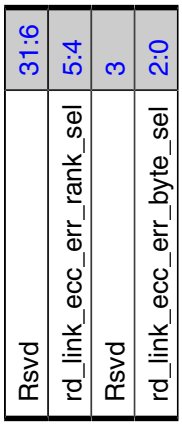


Table 3-186 Fields for Register: LNKECCINDEX

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:4	rd_link_ecc_err_rank_sel	R/W	Select of which rank status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_NUM_RANKS. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1
3			**Reserved Field:** Yes
2:0	rd_link_ecc_err_byte_sel	R/W	Select of which data byte status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_DRAM_DATA_WIDTH/8. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1

3.2.112 LNKECCERRCNT0

- **Name:** Link-ECC Error Status Register 0
- **Description:** Link-ECC Error Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10994
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

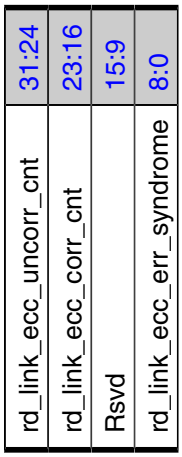


Table 3-187 Fields for Register: LNKECCERRCNT0

Bits	Name	Memory Access	Description
31:24	rd_link_ecc_uncorr_cnt	R	Indicates double bit error count. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23:16	rd_link_ecc_corr_cnt	R	Indicates single bit error count. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:9			**Reserved Field:** Yes
8:0	rd_link_ecc_err_syndrome	R	Indicates ECC syndrome from most recent single bit error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.113 LNKECCERRSTAT

- **Name:** Link-ECC Error Status Register 1
- **Description:** Link-ECC Error Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x10998
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

31:12	11:8	7:4	3:0
Rsvd	rd_link_ecc_uncorr_err_int	Rsvd	rd_link_ecc_corr_err_int

Table 3-188 Fields for Register: LNKECCERRSTAT

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11:8	rd_link_ecc_uncorr_err_int	R	Indicates double bit error for Read Link-ECC. If double bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_uncorr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) **Value After Reset:** 0x0 **Programming Mode:** Static
7:4			**Reserved Field:** Yes
3:0	rd_link_ecc_corr_err_int	R	Indicates single bit error for Read Link-ECC. If signle bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_corr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.114 LNKECCCADDR0

- **Name:** Link ECC Corrected Error Address Register 0
- **Description:** Link ECC Corrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x109e0
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

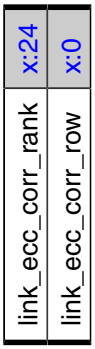


Table 3-189 Fields for Register: LNKECCCADDR0

Bits	Name	Memory Access	Description
x:24	link_ecc_corr_rank	R	Indicates the rank number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	link_ecc_corr_row	R	Indicates the page/row number of a read resulting in a corrected Read Link ECC error. This is 18-bits wide in configurations with LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.115 LNKECCCADDR1

- **Name:** Link ECC Corrected Error Address Register 1
- **Description:** Link ECC Corrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x109e4
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

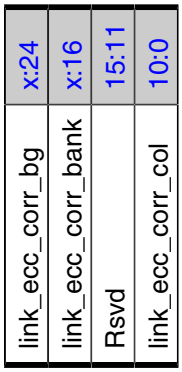


Table 3-190 Fields for Register: LNKECCCADDR1

Bits	Name	Memory Access	Description
x:24	link_ecc_corr_bg	R	Bank Group number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	link_ecc_corr_bank	R	Bank number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-190 Fields for Register: LNKECCCADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	link_ecc_corr_col	R	Block number of a read resulting in a corrected Read Link ECC error. The error address identifies that Link ECC error happens in any data beat of Read data and any data-lane, therefore the lowest 4-bits is always 4'b0000. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

3.2.116 LNKECCUADDR0

- **Name:** Link ECC Uncorrected Error Address Register 0
- **Description:** Link ECC Uncorrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x109e8
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

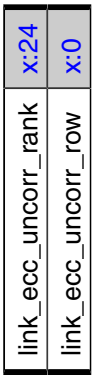


Table 3-191 Fields for Register: LNKECCUADDR0

Bits	Name	Memory Access	Description
x:24	link_ecc_uncorr_rank	R	Rank number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	link_ecc_uncorr_row	R	Page/row number of a read resulting in an uncorrected Read Link ECC error. This is 18-bits wide in configurations with LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.2.117 LNKECCUADDR1

- **Name:** Link ECC Uncorrected Error Address Register 1
- **Description:** Link ECC Uncorrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x109ec
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH0.

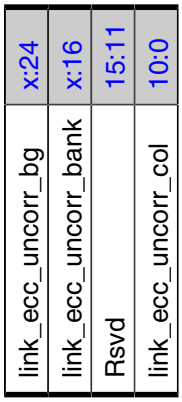


Table 3-192 Fields for Register: LNKECCUADDR1

Bits	Name	Memory Access	Description
x:24	link_ecc_uncorr_bg	R	Bank Group number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	link_ecc_uncorr_bank	R	Bank number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-192 Fields for Register: LNKECCUADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	link_ecc_uncorr_col	R	Block number of a read resulting in an uncorrected Read Link ECC error. The error address identifies that Link ECC error happens in any data beat of Read data and any data-lane, therefore the lowest 4-bits is always 4'b0000. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

3.2.118 OPCTRL0

- **Name:** Operation Control Register 0
- **Description:** Operation Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b80
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

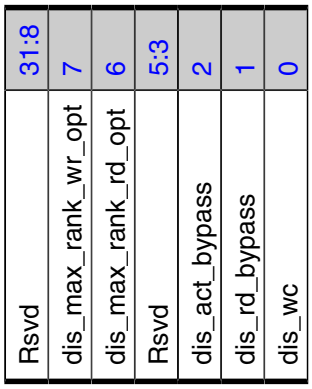


Table 3-193 Fields for Register: OPCTRL0

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7	dis_max_rank_wr_opt	R/W	Disable optimized max_rank_wr and max_logical_rank_wr feature. This register is debug purpose only. For normal operation, This register must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
6	dis_max_rank_rd_opt	R/W	Disable optimized max_rank_rd and max_logical_rank_rd feature. This register is debug purpose only. For normal operation, This register must be set to 0. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
5:3			**Reserved Field:** Yes

Table 3-193 Fields for Register: OPCTRL0 (continued)

Bits	Name	Memory Access	Description
2	dis_act_bypass	R/W	Only present in designs supporting activate bypass. When 1, disable bypass path for high priority read activates FOR DEBUG ONLY. **Value After Reset:** 0x0 **Programming Mode:** Static
1	dis_rd_bypass	R/W	Only present in designs supporting read bypass. When 1, disable bypass path for high priority read page hits FOR DEBUG ONLY. **Value After Reset:** 0x0 **Programming Mode:** Static
0	dis_wc	R/W	When 1, disable write combine. FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Static

3.2.119 OPCTRL1

- **Name:** Operation Control Register 1
- **Description:** Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b84
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

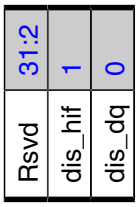


Table 3-194 Fields for Register: OPCTRL1

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	dis_hif	R/W	When 1, DDRCTL asserts the HIF command signal hif_cmd_stall. DDRCTL will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	dis_dq	R/W	When 1, DDRCTL will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the DDRCTL, which makes it safe to modify certain register fields associated with reads and writes (see Programming Chapter for details). After setting this bit, it is strongly recommended to poll OPCTRLCAM.wr_data_pipeline_empty and OPCTRLCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Note: This bit is not applicable for designs working in DDR5 mode. In DDR5 mode, use software command interface command DisDqRef to achieve the same function as this bit. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.120 OPCTRLCAM

- **Name:** CAM Operation Control Register
- **Description:** CAM Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b88
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

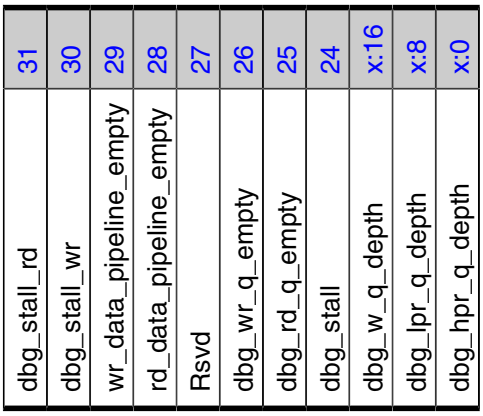


Table 3-195 Fields for Register: OPCTRLCAM

Bits	Name	Memory Access	Description
31	dbg_stall_rd	R	Stall for Read channel FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30	dbg_stall_wr	R	Stall for Write channel FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	wr_data_pipeline_empty	R	This bit indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

Table 3-195 Fields for Register: OPCTRLCAM (continued)

Bits	Name	Memory Access	Description
28	rd_data_pipeline_empty	R	This bit indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
27			**Reserved Field:** Yes
26	dbg_wr_q_empty	R	When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
25	dbg_rd_q_empty	R	When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
24	dbg_stall	R	Stall FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-195 Fields for Register: OPCTRLCAM (continued)

Bits	Name	Memory Access	Description
x:16	dbg_w_q_depth	R	Write queue depth For HW configurations which have more than 128 deep write CAM, use OPCTRLWRCAM.dbg_w_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS + 1" + 15
x:8	dbg_lpr_q_depth	R	Low priority read queue depth For HW configurations which have more than 128 deep read CAM, use OPCTRLRDCAM.dbg_lpr_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS + 1" + 7
x:0	dbg_hpr_q_depth	R	High priority read queue depth For HW configurations which have more than 128 deep read CAM, use OPCTRLRDCAM.dbg_hpr_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS + 1" - 1

3.2.121 OPCTRLCMD

- **Name:** Command Operation Control Register
- **Description:** Command Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b8c
- **Exists:** DDRCTL_DDR4_OR_LPDDR__OR__UMCTL2_REF_ZQ_IO==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

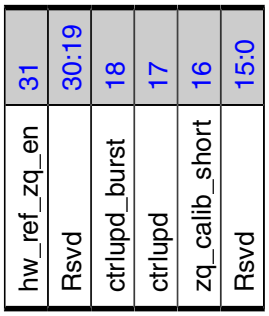


Table 3-196 Fields for Register: OPCTRLCMD

Bits	Name	Memory Access	Description
31	hw_ref_zq_en	R/W	Setting this register bit to 1 allows refresh and ZQCS/MPC(ZQ Calibration) commands to be triggered from hardware via the IOs ext_*. If set to 1, the fields OPCTRLCMD.zq_calib_short and OPREFCTRL*.rank*_refresh have no function, and are ignored by the DDRCTL logic. Setting this register bit to 0 allows refresh and ZQCS/MPC(ZQ Calibration) to be triggered from software, via the fields OPCTRLCMD.zq_calib_short and OPREFCTRL*.rank*_refresh. If set to 0, the hardware pins ext_* have no function, and are ignored by the DDRCTL logic. This register is static, and may only be changed when the DDRC reset signal, core_ddrc_rstn, is asserted (0). Note: Supporting this register field in this release is limited. Contact Synopsys if you wish to use this. Note: This field is not applicable for DDR5 ZQ Calibration. **Value After Reset:** 0x0 **Programming Mode:** Static
30:19			**Reserved Field:** Yes

Table 3-196 Fields for Register: OPCTRLCMD (continued)

Bits	Name	Memory Access	Description
18	ctrlupd_burst	R/W	While this register bit is 1, the DDRCTL issues burst DFI control update to the PHY to change core VDD. When this register bit is changed to 0 from 1, burst DFI control update will be stopped, but one DFI control update request is issued which is in progress. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Note: This field is not applicable for DDR54. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	ctrlupd	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	zq_calib_short	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init, in Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) or Deep Sleep Mode or Maximum Power Saving Mode. For Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) it will be scheduled after SR(except LPDDR4/5) or SRPD(LPDDR4/5) has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. For Maximum Power Saving Mode, it will not be scheduled, although OPCTRLSTAT.zq_calib_short_busy will be de-asserted. Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
15:0			**Reserved Field:** Yes

3.2.122 OPCTRLSTAT

- **Name:** Status Operation Control Register
- **Description:** Status Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b90
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

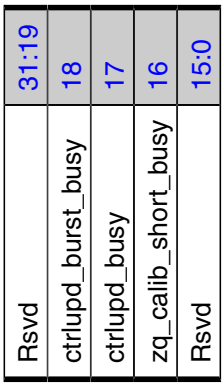


Table 3-197 Fields for Register: OPCTRLSTAT

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	ctrlupd_burst_busy	R	SoC core may initiate a burst DFI control update operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the burst control update request. It goes low when the burst control update operation is finished in the DDRCTL. It is recommended not to perform burst ctrlupd operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a burst DFI ctrol update operation ■ 1 - Indicates that burst control update operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-197 Fields for Register: OPCTRLSTAT (continued)

Bits	Name	Memory Access	Description
17	ctrlupd_busy	R	SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the DDRCTL. It is recommended not to perform ctrlupd operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ctrlupd operation ■ 1 - Indicates that ctrlupd operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	zq_calib_short_busy	R	SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the DDRCTL. It is recommended not to perform ZQCS operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ZQCS operation ■ 1 - Indicates that ZQCS operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0			**Reserved Field:** Yes

3.2.123 OPCTRLCAM1

- **Name:** CAM Operation Control Register 1
- **Description:** CAM Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b94
- **Exists:** MEMC_INLINE_ECC==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-198 Fields for Register: OPCTRLCAM1

Bits	Name	Memory Access	Description
x:0	dbg_wrecc_q_depth	R	Write ECC queue depth **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS + 1" - 1

3.2.124 OPREFCTRL0

- **Name:** Refresh Operation Control Register 0
- **Description:** Refresh Operation Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b98
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank31_refresh	rank30_refresh	rank29_refresh	rank28_refresh	rank27_refresh	rank26_refresh	rank25_refresh	rank24_refresh	rank23_refresh	rank22_refresh	rank21_refresh	rank20_refresh	rank19_refresh	rank18_refresh	rank17_refresh	rank16_refresh	rank15_refresh	rank14_refresh	rank13_refresh	rank12_refresh	rank11_refresh	rank10_refresh	rank9_refresh	rank8_refresh	rank7_refresh	rank6_refresh	rank5_refresh	rank4_refresh	rank3_refresh	rank2_refresh	rank1_refresh	rank0_refresh

Table 3-199 Fields for Register: OPREFCTRL0

Bits	Name	Memory Access	Description
31	rank31_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 31. Writing to this bit causes OPREFSTAT0.rank31_refresh_busy to be set. When OPREFSTAT0.rank31_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 31. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
30	rank30_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 30. Writing to this bit causes OPREFSTAT0.rank30_refresh_busy to be set. When OPREFSTAT0.rank30_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 30. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
29	rank29_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 29. Writing to this bit causes OPREFSTAT0.rank29_refresh_busy to be set. When OPREFSTAT0.rank29_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 29. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
28	rank28_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 28. Writing to this bit causes OPREFSTAT0.rank28_refresh_busy to be set. When OPREFSTAT0.rank28_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 28. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
27	rank27_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 27. Writing to this bit causes OPREFSTAT0.rank27_refresh_busy to be set. When OPREFSTAT0.rank27_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 27. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
26	rank26_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 26. Writing to this bit causes OPREFSTAT0.rank26_refresh_busy to be set. When OPREFSTAT0.rank26_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 26. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
25	rank25_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 25. Writing to this bit causes OPREFSTAT0.rank25_refresh_busy to be set. When OPREFSTAT0.rank25_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 25. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
24	rank24_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 24. Writing to this bit causes OPREFSTAT0.rank24_refresh_busy to be set. When OPREFSTAT0.rank24_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 24. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23	rank23_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 23. Writing to this bit causes OPREFSTAT0.rank23_refresh_busy to be set. When OPREFSTAT0.rank23_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 23. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
22	rank22_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 22. Writing to this bit causes OPREFSTAT0.rank22_refresh_busy to be set. When OPREFSTAT0.rank22_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 22. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
21	rank21_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 21. Writing to this bit causes OPREFSTAT0.rank21_refresh_busy to be set. When OPREFSTAT0.rank21_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 21. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
20	rank20_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 20. Writing to this bit causes OPREFSTAT0.rank20_refresh_busy to be set. When OPREFSTAT0.rank20_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 20. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
19	rank19_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 19. Writing to this bit causes OPREFSTAT0.rank19_refresh_busy to be set. When OPREFSTAT0.rank19_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 19. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
18	rank18_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 18. Writing to this bit causes OPREFSTAT0.rank18_refresh_busy to be set. When OPREFSTAT0.rank18_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 18. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	rank17_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 17. Writing to this bit causes OPREFSTAT0.rank17_refresh_busy to be set. When OPREFSTAT0.rank17_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 17. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	rank16_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 16. Writing to this bit causes OPREFSTAT0.rank16_refresh_busy to be set. When OPREFSTAT0.rank16_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 16. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
15	rank15_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 15. Writing to this bit causes OPREFSTAT0.rank15_refresh_busy to be set. When OPREFSTAT0.rank15_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 15. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
14	rank14_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 14. Writing to this bit causes OPREFSTAT0.rank14_refresh_busy to be set. When OPREFSTAT0.rank14_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 14. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13	rank13_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 13. Writing to this bit causes OPREFSTAT0.rank13_refresh_busy to be set. When OPREFSTAT0.rank13_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 13. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
12	rank12_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 12. Writing to this bit causes OPREFSTAT0.rank12_refresh_busy to be set. When OPREFSTAT0.rank12_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 12. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
11	rank11_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 11. Writing to this bit causes OPREFSTAT0.rank11_refresh_busy to be set. When OPREFSTAT0.rank11_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 11. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
10	rank10_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 10. Writing to this bit causes OPREFSTAT0.rank10_refresh_busy to be set. When OPREFSTAT0.rank10_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 10. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
9	rank9_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 9. Writing to this bit causes OPREFSTAT0.rank9_refresh_busy to be set. When OPREFSTAT0.rank9_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 9. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
8	rank8_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 8. Writing to this bit causes OPREFSTAT0.rank8_refresh_busy to be set. When OPREFSTAT0.rank8_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 8. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7	rank7_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 7. Writing to this bit causes OPREFSTAT0.rank7_refresh_busy to be set. When OPREFSTAT0.rank7_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 7. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
6	rank6_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 6. Writing to this bit causes OPREFSTAT0.rank6_refresh_busy to be set. When OPREFSTAT0.rank6_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 6. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5	rank5_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 5. Writing to this bit causes OPREFSTAT0.rank5_refresh_busy to be set. When OPREFSTAT0.rank5_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 5. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rank4_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 4. Writing to this bit causes OPREFSTAT0.rank4_refresh_busy to be set. When OPREFSTAT0.rank4_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 4. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
3	rank3_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 3. Writing to this bit causes OPREFSTAT0.rank3_refresh_busy to be set. When OPREFSTAT0.rank3_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 3. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rank2_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 2. Writing to this bit causes OPREFSTAT0.rank2_refresh_busy to be set. When OPREFSTAT0.rank2_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 2. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rank1_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 1. Writing to this bit causes OPREFSTAT0.rank1_refresh_busy to be set. When OPREFSTAT0.rank1_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 1. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-199 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
0	rank0_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 0. Writing to this bit causes OPREFSTAT0.rank0_refresh_busy to be set. When OPREFSTAT0.rank0_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 0. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.2.125 OPREFCTRL1

- **Name:** Refresh Operation Control Register 1
- **Description:** Refresh Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10b9c
- **Exists:** UMCTL2_NUM_LRANKS_TOTAL>32

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank63_refresh	rank62_refresh	rank61_refresh	rank60_refresh	rank59_refresh	rank58_refresh	rank57_refresh	rank56_refresh	rank55_refresh	rank54_refresh	rank53_refresh	rank52_refresh	rank51_refresh	rank50_refresh	rank49_refresh	rank48_refresh	rank47_refresh	rank46_refresh	rank45_refresh	rank44_refresh	rank43_refresh	rank42_refresh	rank41_refresh	rank40_refresh	rank39_refresh	rank38_refresh	rank37_refresh	rank36_refresh	rank35_refresh	rank34_refresh	rank33_refresh	rank32_refresh

Table 3-200 Fields for Register: OPREFCTRL1

Bits	Name	Memory Access	Description
31	rank63_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 63. Writing to this bit causes OPREFSTAT1.rank63_refresh_busy to be set. When OPREFSTAT1.rank63_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 63. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
30	rank62_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 62. Writing to this bit causes OPREFSTAT1.rank62_refresh_busy to be set. When OPREFSTAT1.rank62_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 62. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
29	rank61_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 61. Writing to this bit causes OPREFSTAT1.rank61_refresh_busy to be set. When OPREFSTAT1.rank61_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 61. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
28	rank60_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 60. Writing to this bit causes OPREFSTAT1.rank60_refresh_busy to be set. When OPREFSTAT1.rank60_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 60. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
27	rank59_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 59. Writing to this bit causes OPREFSTAT1.rank59_refresh_busy to be set. When OPREFSTAT1.rank59_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 59. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
26	rank58_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 58. Writing to this bit causes OPREFSTAT1.rank58_refresh_busy to be set. When OPREFSTAT1.rank58_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 58. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
25	rank57_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 57. Writing to this bit causes OPREFSTAT1.rank57_refresh_busy to be set. When OPREFSTAT1.rank57_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 57. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
24	rank56_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 56. Writing to this bit causes OPREFSTAT1.rank56_refresh_busy to be set. When OPREFSTAT1.rank56_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 56. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23	rank55_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 55. Writing to this bit causes OPREFSTAT1.rank55_refresh_busy to be set. When OPREFSTAT1.rank55_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 55. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
22	rank54_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 54. Writing to this bit causes OPREFSTAT1.rank54_refresh_busy to be set. When OPREFSTAT1.rank54_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 54. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
21	rank53_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 53. Writing to this bit causes OPREFSTAT1.rank53_refresh_busy to be set. When OPREFSTAT1.rank53_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 53. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
20	rank52_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 52. Writing to this bit causes OPREFSTAT1.rank52_refresh_busy to be set. When OPREFSTAT1.rank52_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 52. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
19	rank51_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 51. Writing to this bit causes OPREFSTAT1.rank51_refresh_busy to be set. When OPREFSTAT1.rank51_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 51. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
18	rank50_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 50. Writing to this bit causes OPREFSTAT1.rank50_refresh_busy to be set. When OPREFSTAT1.rank50_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 50. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	rank49_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 49. Writing to this bit causes OPREFSTAT1.rank49_refresh_busy to be set. When OPREFSTAT1.rank49_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 49. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	rank48_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 48. Writing to this bit causes OPREFSTAT1.rank48_refresh_busy to be set. When OPREFSTAT1.rank48_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 48. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
15	rank47_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 47. Writing to this bit causes OPREFSTAT1.rank47_refresh_busy to be set. When OPREFSTAT1.rank47_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 47. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
14	rank46_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 46. Writing to this bit causes OPREFSTAT1.rank46_refresh_busy to be set. When OPREFSTAT1.rank46_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 46. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13	rank45_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 45. Writing to this bit causes OPREFSTAT1.rank45_refresh_busy to be set. When OPREFSTAT1.rank45_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 45. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
12	rank44_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 44. Writing to this bit causes OPREFSTAT1.rank44_refresh_busy to be set. When OPREFSTAT1.rank44_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 44. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
11	rank43_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 43. Writing to this bit causes OPREFSTAT1.rank43_refresh_busy to be set. When OPREFSTAT1.rank43_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 43. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
10	rank42_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 42. Writing to this bit causes OPREFSTAT1.rank42_refresh_busy to be set. When OPREFSTAT1.rank42_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 42. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
9	rank41_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 41. Writing to this bit causes OPREFSTAT1.rank41_refresh_busy to be set. When OPREFSTAT1.rank41_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 41. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
8	rank40_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 40. Writing to this bit causes OPREFSTAT1.rank40_refresh_busy to be set. When OPREFSTAT1.rank40_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 40. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7	rank39_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 39. Writing to this bit causes OPREFSTAT1.rank39_refresh_busy to be set. When OPREFSTAT1.rank39_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 39. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
6	rank38_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 38. Writing to this bit causes OPREFSTAT1.rank38_refresh_busy to be set. When OPREFSTAT1.rank38_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 38. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5	rank37_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 37. Writing to this bit causes OPREFSTAT1.rank37_refresh_busy to be set. When OPREFSTAT1.rank37_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 37. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rank36_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 36. Writing to this bit causes OPREFSTAT1.rank36_refresh_busy to be set. When OPREFSTAT1.rank36_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 36. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
3	rank35_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 35. Writing to this bit causes OPREFSTAT1.rank35_refresh_busy to be set. When OPREFSTAT1.rank35_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 35. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rank34_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 34. Writing to this bit causes OPREFSTAT1.rank34_refresh_busy to be set. When OPREFSTAT1.rank34_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 34. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rank33_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 33. Writing to this bit causes OPREFSTAT1.rank33_refresh_busy to be set. When OPREFSTAT1.rank33_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 33. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-200 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
0	rank32_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 32. Writing to this bit causes OPREFSTAT1.rank32_refresh_busy to be set. When OPREFSTAT1.rank32_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 32. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.2.126 OPREFSTAT0

- **Name:** Refresh Operation Status Register 0
- **Description:** Refresh Operation Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ba0
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank31_refresh_busy	rank30_refresh_busy	rank29_refresh_busy	rank28_refresh_busy	rank27_refresh_busy	rank26_refresh_busy	rank25_refresh_busy	rank24_refresh_busy	rank23_refresh_busy	rank22_refresh_busy	rank21_refresh_busy	rank20_refresh_busy	rank19_refresh_busy	rank18_refresh_busy	rank17_refresh_busy	rank16_refresh_busy	rank15_refresh_busy	rank14_refresh_busy	rank13_refresh_busy	rank12_refresh_busy	rank11_refresh_busy	rank10_refresh_busy	rank9_refresh_busy	rank8_refresh_busy	rank7_refresh_busy	rank6_refresh_busy	rank5_refresh_busy	rank4_refresh_busy	rank3_refresh_busy	rank2_refresh_busy	rank1_refresh_busy	rank0_refresh_busy

Table 3-201 Fields for Register: OPREFSTAT0

Bits	Name	Memory Access	Description
31	rank31_refresh_busy	R	SoC core may initiate a rank31_refresh operation (refresh operation to rank 31) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank31_refresh is set to one. It goes low when the rank31_refresh operation is stored in the DDRCTL. It is recommended not to perform rank31_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank31_refresh operation ■ 1 - Indicates that rank31_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
30	rank30_refresh_busy	R	SoC core may initiate a rank30_refresh operation (refresh operation to rank 30) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank30_refresh is set to one. It goes low when the rank30_refresh operation is stored in the DDRCTL. It is recommended not to perform rank30_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank30_refresh operation ■ 1 - Indicates that rank30_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	rank29_refresh_busy	R	SoC core may initiate a rank29_refresh operation (refresh operation to rank 29) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank29_refresh is set to one. It goes low when the rank29_refresh operation is stored in the DDRCTL. It is recommended not to perform rank29_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank29_refresh operation ■ 1 - Indicates that rank29_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	rank28_refresh_busy	R	SoC core may initiate a rank28_refresh operation (refresh operation to rank 28) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank28_refresh is set to one. It goes low when the rank28_refresh operation is stored in the DDRCTL. It is recommended not to perform rank28_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank28_refresh operation ■ 1 - Indicates that rank28_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
27	rank27_refresh_busy	R	SoC core may initiate a rank27_refresh operation (refresh operation to rank 27) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank27_refresh is set to one. It goes low when the rank27_refresh operation is stored in the DDRCTL. It is recommended not to perform rank27_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank27_refresh operation ■ 1 - Indicates that rank27_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26	rank26_refresh_busy	R	SoC core may initiate a rank26_refresh operation (refresh operation to rank 26) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank26_refresh is set to one. It goes low when the rank26_refresh operation is stored in the DDRCTL. It is recommended not to perform rank26_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank26_refresh operation ■ 1 - Indicates that rank26_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	rank25_refresh_busy	R	SoC core may initiate a rank25_refresh operation (refresh operation to rank 25) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank25_refresh is set to one. It goes low when the rank25_refresh operation is stored in the DDRCTL. It is recommended not to perform rank25_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank25_refresh operation ■ 1 - Indicates that rank25_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
24	rank24_refresh_busy	R	SoC core may initiate a rank24_refresh operation (refresh operation to rank 24) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank24_refresh is set to one. It goes low when the rank24_refresh operation is stored in the DDRCTL. It is recommended not to perform rank24_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank24_refresh operation ■ 1 - Indicates that rank24_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	rank23_refresh_busy	R	SoC core may initiate a rank23_refresh operation (refresh operation to rank 23) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank23_refresh is set to one. It goes low when the rank23_refresh operation is stored in the DDRCTL. It is recommended not to perform rank23_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank23_refresh operation ■ 1 - Indicates that rank23_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	rank22_refresh_busy	R	SoC core may initiate a rank22_refresh operation (refresh operation to rank 22) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank22_refresh is set to one. It goes low when the rank22_refresh operation is stored in the DDRCTL. It is recommended not to perform rank22_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank22_refresh operation ■ 1 - Indicates that rank22_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
21	rank21_refresh_busy	R	SoC core may initiate a rank21_refresh operation (refresh operation to rank 21) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank21_refresh is set to one. It goes low when the rank21_refresh operation is stored in the DDRCTL. It is recommended not to perform rank21_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank21_refresh operation ■ 1 - Indicates that rank21_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	rank20_refresh_busy	R	SoC core may initiate a rank20_refresh operation (refresh operation to rank 20) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank20_refresh is set to one. It goes low when the rank20_refresh operation is stored in the DDRCTL. It is recommended not to perform rank20_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank20_refresh operation ■ 1 - Indicates that rank20_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	rank19_refresh_busy	R	SoC core may initiate a rank19_refresh operation (refresh operation to rank 19) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank19_refresh is set to one. It goes low when the rank19_refresh operation is stored in the DDRCTL. It is recommended not to perform rank19_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank19_refresh operation ■ 1 - Indicates that rank19_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
18	rank18_refresh_busy	R	SoC core may initiate a rank18_refresh operation (refresh operation to rank 18) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank18_refresh is set to one. It goes low when the rank18_refresh operation is stored in the DDRCTL. It is recommended not to perform rank18_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank18_refresh operation ■ 1 - Indicates that rank18_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	rank17_refresh_busy	R	SoC core may initiate a rank17_refresh operation (refresh operation to rank 17) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank17_refresh is set to one. It goes low when the rank17_refresh operation is stored in the DDRCTL. It is recommended not to perform rank17_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank17_refresh operation ■ 1 - Indicates that rank17_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	rank16_refresh_busy	R	SoC core may initiate a rank16_refresh operation (refresh operation to rank 16) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank16_refresh is set to one. It goes low when the rank16_refresh operation is stored in the DDRCTL. It is recommended not to perform rank16_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank16_refresh operation ■ 1 - Indicates that rank16_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
15	rank15_refresh_busy	R	SoC core may initiate a rank15_refresh operation (refresh operation to rank 15) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank15_refresh is set to one. It goes low when the rank15_refresh operation is stored in the DDRCTL. It is recommended not to perform rank15_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank15_refresh operation ■ 1 - Indicates that rank15_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	rank14_refresh_busy	R	SoC core may initiate a rank14_refresh operation (refresh operation to rank 14) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank14_refresh is set to one. It goes low when the rank14_refresh operation is stored in the DDRCTL. It is recommended not to perform rank14_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank14_refresh operation ■ 1 - Indicates that rank14_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13	rank13_refresh_busy	R	SoC core may initiate a rank13_refresh operation (refresh operation to rank 13) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank13_refresh is set to one. It goes low when the rank13_refresh operation is stored in the DDRCTL. It is recommended not to perform rank13_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank13_refresh operation ■ 1 - Indicates that rank13_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
12	rank12_refresh_busy	R	SoC core may initiate a rank12_refresh operation (refresh operation to rank 12) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank12_refresh is set to one. It goes low when the rank12_refresh operation is stored in the DDRCTL. It is recommended not to perform rank12_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank12_refresh operation ■ 1 - Indicates that rank12_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	rank11_refresh_busy	R	SoC core may initiate a rank11_refresh operation (refresh operation to rank 11) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank11_refresh is set to one. It goes low when the rank11_refresh operation is stored in the DDRCTL. It is recommended not to perform rank11_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank11_refresh operation ■ 1 - Indicates that rank11_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	rank10_refresh_busy	R	SoC core may initiate a rank10_refresh operation (refresh operation to rank 10) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank10_refresh is set to one. It goes low when the rank10_refresh operation is stored in the DDRCTL. It is recommended not to perform rank10_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank10_refresh operation ■ 1 - Indicates that rank10_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
9	rank9_refresh_busy	R	SoC core may initiate a rank9_refresh operation (refresh operation to rank 9) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank9_refresh is set to one. It goes low when the rank9_refresh operation is stored in the DDRCTL. It is recommended not to perform rank9_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank9_refresh operation ■ 1 - Indicates that rank9_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	rank8_refresh_busy	R	SoC core may initiate a rank8_refresh operation (refresh operation to rank 8) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank8_refresh is set to one. It goes low when the rank8_refresh operation is stored in the DDRCTL. It is recommended not to perform rank8_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank8_refresh operation ■ 1 - Indicates that rank8_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	rank7_refresh_busy	R	SoC core may initiate a rank7_refresh operation (refresh operation to rank 7) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank7_refresh is set to one. It goes low when the rank7_refresh operation is stored in the DDRCTL. It is recommended not to perform rank7_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank7_refresh operation ■ 1 - Indicates that rank7_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
6	rank6_refresh_busy	R	SoC core may initiate a rank6_refresh operation (refresh operation to rank 6) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank6_refresh is set to one. It goes low when the rank6_refresh operation is stored in the DDRCTL. It is recommended not to perform rank6_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank6_refresh operation ■ 1 - Indicates that rank6_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
5	rank5_refresh_busy	R	SoC core may initiate a rank5_refresh operation (refresh operation to rank 5) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank5_refresh is set to one. It goes low when the rank5_refresh operation is stored in the DDRCTL. It is recommended not to perform rank5_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank5_refresh operation ■ 1 - Indicates that rank5_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	rank4_refresh_busy	R	SoC core may initiate a rank4_refresh operation (refresh operation to rank 4) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank4_refresh is set to one. It goes low when the rank4_refresh operation is stored in the DDRCTL. It is recommended not to perform rank4_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank4_refresh operation ■ 1 - Indicates that rank4_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
3	rank3_refresh_busy	R	SoC core may initiate a rank3_refresh operation (refresh operation to rank 3) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank3_refresh is set to one. It goes low when the rank3_refresh operation is stored in the DDRCTL. It is recommended not to perform rank3_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank3_refresh operation ■ 1 - Indicates that rank3_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	rank2_refresh_busy	R	SoC core may initiate a rank2_refresh operation (refresh operation to rank 2) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank2_refresh is set to one. It goes low when the rank2_refresh operation is stored in the DDRCTL. It is recommended not to perform rank2_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank2_refresh operation ■ 1 - Indicates that rank2_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	rank1_refresh_busy	R	SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the DDRCTL. It is recommended not to perform rank1_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank1_refresh operation ■ 1 - Indicates that rank1_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-201 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
0	rank0_refresh_busy	R	SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the DDRCTL. It is recommended not to perform rank0_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank0_refresh operation ■ 1 - Indicates that rank0_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.127 OPREFSTAT1

- **Name:** Refresh Operation Status Register 1
- **Description:** Refresh Operation Status Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ba4
- **Exists:** UMCTL2_NUM_LRANKS_TOTAL>32

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank63_refresh_busy	rank62_refresh_busy	rank61_refresh_busy	rank60_refresh_busy	rank59_refresh_busy	rank58_refresh_busy	rank57_refresh_busy	rank56_refresh_busy	rank55_refresh_busy	rank54_refresh_busy	rank53_refresh_busy	rank52_refresh_busy	rank51_refresh_busy	rank50_refresh_busy	rank49_refresh_busy	rank48_refresh_busy	rank47_refresh_busy	rank46_refresh_busy	rank45_refresh_busy	rank44_refresh_busy	rank43_refresh_busy	rank42_refresh_busy	rank41_refresh_busy	rank40_refresh_busy	rank39_refresh_busy	rank38_refresh_busy	rank37_refresh_busy	rank36_refresh_busy	rank35_refresh_busy	rank34_refresh_busy	rank33_refresh_busy	rank32_refresh_busy

Table 3-202 Fields for Register: OPREFSTAT1

Bits	Name	Memory Access	Description
31	rank63_refresh_busy	R	SoC core may initiate a rank63_refresh operation (refresh operation to rank 63) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank63_refresh is set to one. It goes low when the rank63_refresh operation is stored in the DDRCTL. It is recommended not to perform rank63_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank63_refresh operation ■ 1 - Indicates that rank63_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
30	rank62_refresh_busy	R	SoC core may initiate a rank62_refresh operation (refresh operation to rank 62) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank62_refresh is set to one. It goes low when the rank62_refresh operation is stored in the DDRCTL. It is recommended not to perform rank62_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank62_refresh operation ■ 1 - Indicates that rank62_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	rank61_refresh_busy	R	SoC core may initiate a rank61_refresh operation (refresh operation to rank 61) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank61_refresh is set to one. It goes low when the rank61_refresh operation is stored in the DDRCTL. It is recommended not to perform rank61_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank61_refresh operation ■ 1 - Indicates that rank61_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	rank60_refresh_busy	R	SoC core may initiate a rank60_refresh operation (refresh operation to rank 60) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank60_refresh is set to one. It goes low when the rank60_refresh operation is stored in the DDRCTL. It is recommended not to perform rank60_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank60_refresh operation ■ 1 - Indicates that rank60_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
27	rank59_refresh_busy	R	SoC core may initiate a rank59_refresh operation (refresh operation to rank 59) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank59_refresh is set to one. It goes low when the rank59_refresh operation is stored in the DDRCTL. It is recommended not to perform rank59_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank59_refresh operation ■ 1 - Indicates that rank59_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26	rank58_refresh_busy	R	SoC core may initiate a rank58_refresh operation (refresh operation to rank 58) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank58_refresh is set to one. It goes low when the rank58_refresh operation is stored in the DDRCTL. It is recommended not to perform rank58_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank58_refresh operation ■ 1 - Indicates that rank58_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	rank57_refresh_busy	R	SoC core may initiate a rank57_refresh operation (refresh operation to rank 57) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank57_refresh is set to one. It goes low when the rank57_refresh operation is stored in the DDRCTL. It is recommended not to perform rank57_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank57_refresh operation ■ 1 - Indicates that rank57_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
24	rank56_refresh_busy	R	SoC core may initiate a rank56_refresh operation (refresh operation to rank 56) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank56_refresh is set to one. It goes low when the rank56_refresh operation is stored in the DDRCTL. It is recommended not to perform rank56_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank56_refresh operation ■ 1 - Indicates that rank56_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	rank55_refresh_busy	R	SoC core may initiate a rank55_refresh operation (refresh operation to rank 55) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank55_refresh is set to one. It goes low when the rank55_refresh operation is stored in the DDRCTL. It is recommended not to perform rank55_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank55_refresh operation ■ 1 - Indicates that rank55_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	rank54_refresh_busy	R	SoC core may initiate a rank54_refresh operation (refresh operation to rank 54) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank54_refresh is set to one. It goes low when the rank54_refresh operation is stored in the DDRCTL. It is recommended not to perform rank54_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank54_refresh operation ■ 1 - Indicates that rank54_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
21	rank53_refresh_busy	R	SoC core may initiate a rank53_refresh operation (refresh operation to rank 53) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank53_refresh is set to one. It goes low when the rank53_refresh operation is stored in the DDRCTL. It is recommended not to perform rank53_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank53_refresh operation ■ 1 - Indicates that rank53_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	rank52_refresh_busy	R	SoC core may initiate a rank52_refresh operation (refresh operation to rank 52) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank52_refresh is set to one. It goes low when the rank52_refresh operation is stored in the DDRCTL. It is recommended not to perform rank52_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank52_refresh operation ■ 1 - Indicates that rank52_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	rank51_refresh_busy	R	SoC core may initiate a rank51_refresh operation (refresh operation to rank 51) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank51_refresh is set to one. It goes low when the rank51_refresh operation is stored in the DDRCTL. It is recommended not to perform rank51_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank51_refresh operation ■ 1 - Indicates that rank51_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
18	rank50_refresh_busy	R	SoC core may initiate a rank50_refresh operation (refresh operation to rank 50) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank50_refresh is set to one. It goes low when the rank50_refresh operation is stored in the DDRCTL. It is recommended not to perform rank50_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank50_refresh operation ■ 1 - Indicates that rank50_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	rank49_refresh_busy	R	SoC core may initiate a rank49_refresh operation (refresh operation to rank 49) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank49_refresh is set to one. It goes low when the rank49_refresh operation is stored in the DDRCTL. It is recommended not to perform rank49_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank49_refresh operation ■ 1 - Indicates that rank49_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	rank48_refresh_busy	R	SoC core may initiate a rank48_refresh operation (refresh operation to rank 48) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank48_refresh is set to one. It goes low when the rank48_refresh operation is stored in the DDRCTL. It is recommended not to perform rank48_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank48_refresh operation ■ 1 - Indicates that rank48_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
15	rank47_refresh_busy	R	SoC core may initiate a rank47_refresh operation (refresh operation to rank 47) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank47_refresh is set to one. It goes low when the rank47_refresh operation is stored in the DDRCTL. It is recommended not to perform rank47_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank47_refresh operation ■ 1 - Indicates that rank47_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	rank46_refresh_busy	R	SoC core may initiate a rank46_refresh operation (refresh operation to rank 46) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank46_refresh is set to one. It goes low when the rank46_refresh operation is stored in the DDRCTL. It is recommended not to perform rank46_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank46_refresh operation ■ 1 - Indicates that rank46_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13	rank45_refresh_busy	R	SoC core may initiate a rank45_refresh operation (refresh operation to rank 45) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank45_refresh is set to one. It goes low when the rank45_refresh operation is stored in the DDRCTL. It is recommended not to perform rank45_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank45_refresh operation ■ 1 - Indicates that rank45_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
12	rank44_refresh_busy	R	SoC core may initiate a rank44_refresh operation (refresh operation to rank 44) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank44_refresh is set to one. It goes low when the rank44_refresh operation is stored in the DDRCTL. It is recommended not to perform rank44_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank44_refresh operation ■ 1 - Indicates that rank44_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	rank43_refresh_busy	R	SoC core may initiate a rank43_refresh operation (refresh operation to rank 43) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank43_refresh is set to one. It goes low when the rank43_refresh operation is stored in the DDRCTL. It is recommended not to perform rank43_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank43_refresh operation ■ 1 - Indicates that rank43_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	rank42_refresh_busy	R	SoC core may initiate a rank42_refresh operation (refresh operation to rank 42) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank42_refresh is set to one. It goes low when the rank42_refresh operation is stored in the DDRCTL. It is recommended not to perform rank42_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank42_refresh operation ■ 1 - Indicates that rank42_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
9	rank41_refresh_busy	R	SoC core may initiate a rank41_refresh operation (refresh operation to rank 41) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank41_refresh is set to one. It goes low when the rank41_refresh operation is stored in the DDRCTL. It is recommended not to perform rank41_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank41_refresh operation ■ 1 - Indicates that rank41_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	rank40_refresh_busy	R	SoC core may initiate a rank40_refresh operation (refresh operation to rank 40) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank40_refresh is set to one. It goes low when the rank40_refresh operation is stored in the DDRCTL. It is recommended not to perform rank40_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank40_refresh operation ■ 1 - Indicates that rank40_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	rank39_refresh_busy	R	SoC core may initiate a rank39_refresh operation (refresh operation to rank 39) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank39_refresh is set to one. It goes low when the rank39_refresh operation is stored in the DDRCTL. It is recommended not to perform rank39_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank39_refresh operation ■ 1 - Indicates that rank39_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
6	rank38_refresh_busy	R	SoC core may initiate a rank38_refresh operation (refresh operation to rank 38) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank38_refresh is set to one. It goes low when the rank38_refresh operation is stored in the DDRCTL. It is recommended not to perform rank38_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank38_refresh operation ■ 1 - Indicates that rank38_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
5	rank37_refresh_busy	R	SoC core may initiate a rank37_refresh operation (refresh operation to rank 37) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank37_refresh is set to one. It goes low when the rank37_refresh operation is stored in the DDRCTL. It is recommended not to perform rank37_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank37_refresh operation ■ 1 - Indicates that rank37_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	rank36_refresh_busy	R	SoC core may initiate a rank36_refresh operation (refresh operation to rank 36) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank36_refresh is set to one. It goes low when the rank36_refresh operation is stored in the DDRCTL. It is recommended not to perform rank36_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank36_refresh operation ■ 1 - Indicates that rank36_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
3	rank35_refresh_busy	R	SoC core may initiate a rank35_refresh operation (refresh operation to rank 35) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank35_refresh is set to one. It goes low when the rank35_refresh operation is stored in the DDRCTL. It is recommended not to perform rank35_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank35_refresh operation ■ 1 - Indicates that rank35_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	rank34_refresh_busy	R	SoC core may initiate a rank34_refresh operation (refresh operation to rank 34) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank34_refresh is set to one. It goes low when the rank34_refresh operation is stored in the DDRCTL. It is recommended not to perform rank34_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank34_refresh operation ■ 1 - Indicates that rank34_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	rank33_refresh_busy	R	SoC core may initiate a rank33_refresh operation (refresh operation to rank 33) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank33_refresh is set to one. It goes low when the rank33_refresh operation is stored in the DDRCTL. It is recommended not to perform rank33_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank33_refresh operation ■ 1 - Indicates that rank33_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-202 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
0	rank32_refresh_busy	R	SoC core may initiate a rank32_refresh operation (refresh operation to rank 32) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank32_refresh is set to one. It goes low when the rank32_refresh operation is stored in the DDRCTL. It is recommended not to perform rank32_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank32_refresh operation ■ 1 - Indicates that rank32_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.128 SWCTL

- **Name:** Software Register Programming Control Enable
- **Description:** Software Register Programming Control Enable
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10c80
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

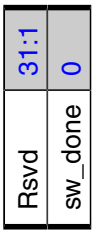


Table 3-203 Fields for Register: SWCTL

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	sw_done	R/W	Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.2.129 SWSTAT

- **Name:** Software Register Programming Control Status
- **Description:** Software Register Programming Control Status
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10c84
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-204 Fields for Register: SWSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	sw_done_ack	R	Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. **Value After Reset:** 0x1 **Programming Mode:** Static

3.2.130 RANKCTL

- **Name:** Rank Control Register
- **Description:** Rank Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10c90
- **Exists:** UMCTL2_NUM_LRANKS_TOTAL>1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

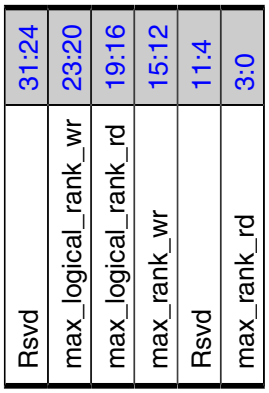


Table 3-205 Fields for Register: RANKCTL

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:20	max_logical_rank_wr	R/W	Present for DDR4/DDR5 3DS supported configurations. Background: Writes to the same logical rank can be performed back-to-back. Writes to different logical ranks may require additional gap in case DRAMSET1TMG16.t_ccd_dlr is larger than DRAMSET1TMG9.t_ccd_s. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by DRAMSET1TMG16.t_ccd_dlr - DRAMSET1TMG9.t_ccd_s) in which only writes from the same logical rank(but different bank group) are eligible to be scheduled. This prevents writes from other logical ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same logical rank(but different bank group). After this number is reached, - DDR4: a delay equal to (DRAMSET1TMG16.t_ccd_dlr - DRAMSET1TMG9.t_ccd_s) is inserted by the scheduler to allow all logical ranks a fair opportunity to be scheduled. - DDR5: writes to the same logical rank are blocked until read-write mode turn around or writes are issued to other logical ranks or other ranks. Higher numbers increase bandwidth utilization, lower numbers

Table 3-205 Fields for Register: RANKCTL (continued)

Bits	Name	Memory Access	Description
			increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same logical rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. This register setting is ignored when MSTR0.active_logical_ranks=0. **Value After Reset:** 0x0 **Programming Mode:** Static
19:16	max_logical_rank_rd	R/W	Present for DDR4/DDR5 3DS supported configurations. Background: Reads to the same logical rank can be performed back-to-back. Reads to different logical ranks may require additional gap in case DRAMSET1TMG16.t_ccd_dlr is larger than DRAMSET1TMG9.t_ccd_s. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by DRAMSET1TMG16.t_ccd_dlr - DRAMSET1TMG9.t_ccd_s) in which only reads from the same logical rank(but different bank group) are eligible to be scheduled. This prevents reads from other logical ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same logical rank(but different bank group). After this number is reached, - DDR4: a delay equal to (DRAMSET1TMG16.t_ccd_dlr - DRAMSET1TMG9.t_ccd_s) is inserted by the scheduler to allow all logical ranks a fair opportunity to be scheduled. - DDR5: reads to the same logical rank are blocked until read-write mode turn around or reads are issued to other logical ranks or other ranks. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same logical rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. This register setting is ignored when MSTR0.active_logical_ranks=0. **Value After Reset:** 0xf **Programming Mode:** Static
15:12	max_rank_wr	R/W	Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The

Table 3-205 Fields for Register: RANKCTL (continued)

Bits	Name	Memory Access	Description
			DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, - DDR4/LPDDR: a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. - DDR5: writes to the same rank are blocked until read-write mode turn around or writes are issued to other ranks. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. **Value After Reset:** 0x0 **Programming Mode:** Static
11:4			**Reserved Field:** Yes
3:0	max_rank_rd	R/W	Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, - DDR4/LPDDR: a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness.

Table 3-205 Fields for Register: RANKCTL (continued)

Bits	Name	Memory Access	Description
			- DDR5: reads to the same rank are blocked until read-write mode turn around or reads are issued to other ranks. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. **Value After Reset:** 0xf **Programming Mode:** Static

3.2.131 DBICTL

- **Name:** DM/DBI Control Register
- **Description:** DM/DBI Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10c94
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

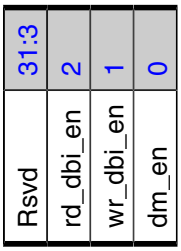


Table 3-206 Fields for Register: DBICTL

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	rd_dbi_en	R/W	Read DBI enable signal in DDRC. ■ 0 - Read DBI is disabled. ■ 1 - Read DBI is enabled. This signal must be set the same value as DRAM's mode register. ■ DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. ■ DDR5: This signal must be set to 0. ■ LPDDR4/LPDDR5: MR3[6]. In case of LPDDR5, if LNKECCCTL0.rd_link_ecc_enable is set to 1, Read DBI is disabled automatically regardless of DBICTL.rd_dbi_en value. Note that LNKECCCTL0.rd_link_ecc_enable is replicated per frequency, so if MSTR2.target_frequency or internal target_frequency for HWFFC is changed, Read DBI may also be changed automatically. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1

Table 3-206 Fields for Register: DBICTL (continued)

Bits	Name	Memory Access	Description
1	wr_dbi_en	R/W	Write DBI enable signal in DDRC. ■ 0 - Write DBI is disabled. ■ 1 - Write DBI is enabled. This signal must be set the same value as DRAM's mode register. ■ DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. ■ DDR5: This signal must be set to 0. ■ LPDDR4/LPDDR5: MR3[7]. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1
0	dm_en	R/W	DM enable signal in DDRC. ■ 0 - DM is disabled. ■ 1 - DM is enabled. This signal must be set the same logical value as DRAM's mode register. ■ DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. ■ DDR5: Set this to same value as MR5[5]. When x4 devices are used, this signal must be set to 0. ■ LPDDR4/LPDDR5: Set this to inverted value of MR13[5] which is opposite polarity from this signal. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static

3.2.132 ODTMAP

- **Name:** ODT/Rank Map Register
- **Description:** ODT/Rank Map Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10c9c
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
NOTE: Please set ODTMAP.rank*_wr/rd_odt to all zero because the ODT feature is automatically turned ON/OFF in LPDDR4/LPDDR5 SDRAM memories. In addition, the DRAMSET1TMG13.odtloff register field must be appropriately programmed.
For DDR5 SDRAM memories, this should be set based on system design requirement and training results. Controller provides customers with more flexibilities that customers have options to send or not to send the NT-ODT command to the NT-ranks for better signal integrity and/or power saving. For example, when sending Read to Rank0, customer can choose to send NT-ODT command to Rank1 and Rank3, but not to send NT-ODT command to Rank2. It's system decision. If no particular requirements, customers should enable NT-ODT to all NT-ranks by setting 4'hF (only effective to NT-ranks).

x:28	x:24	x:20	x:16	x:12	x:8	x:4	x:0
rank3_rd_odt	rank3_wr_odt	rank2_rd_odt	rank2_wr_odt	rank1_rd_odt	rank1_wr_odt	rank0_rd_odt	rank0_wr_odt

Table 3-207 Fields for Register: ODTMAP

Bits	Name	Memory Access	Description
x:28	rank3_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 3. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x8 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 27

Table 3-207 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:24	rank3_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 3. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x8 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 23
x:20	rank2_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 2. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x4 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 19
x:16	rank2_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 2. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x4 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 15

Table 3-207 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:12	rank1_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks **Value After Reset:** "(MEMC_NUM_RANKS>1) ? 0x2 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 11
x:8	rank1_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks **Value After Reset:** "(MEMC_NUM_RANKS>1) ? 0x2 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 7
x:4	rank0_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. **Value After Reset:** 0x1 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 3

Table 3-207 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:0	rank0_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. **Value After Reset:** 0x1 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" - 1

3.2.133 DATACTL0

- **Name:** Data Control register 0
- **Description:** Data Control register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ca0
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

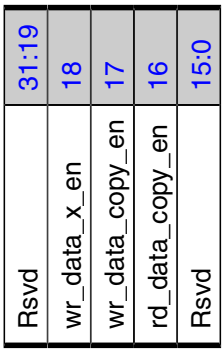


Table 3-208 Fields for Register: DATACTL0

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	wr_data_x_en	R/W	Write Data X 1: Enable Write X 0: Write X This feature is not supported at present. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
17	wr_data_copy_en	R/W	Write Data Copy 1: Enable Write Data Copy X 0: Disable Write Data Copy X This feature is not supported at present. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

Table 3-208 Fields for Register: DATACTL0 (continued)

Bits	Name	Memory Access	Description
16	rd_data_copy_en	R/W	Read Data Copy 1: Enable Read Data Copy X 0: Disable Read Data Copy X This feature is not supported at present. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
15:0			**Reserved Field:** Yes

3.2.134 SWCTLSTATIC

- **Name:** Static Registers Write Enable
- **Description:** Static Registers Write Enable
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ca4
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-209 Fields for Register: SWCTLSTATIC

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	sw_static_unlock	R/W	Enables static register programming outside reset. Program this register to 1 to enable static register programming. Set register back to 0 once programming is done. This register is provided only to be used for software workarounds and it is not meant to be used with all static registers or in all conditions. Unless Synopsys recommends explicitly for a given software sequence, do not use this method to program static registers. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.135 CGCTL

- **Name:** External clock gate control register
- **Description:** External clock gate control register
- **Size:** 32 bits
- **Offset:** 0x10cb0
- **Exists:** DDRCTL_CLK_GATE_TE_OR_ARB==1

This register is in block REGB_DDRC_CH0.

31:5	4	3:1	0
Rsvd	force_clk_arb_en	Rsvd	force_clk_te_en

Table 3-210 Fields for Register: CGCTL

Bits	Name	Memory Access	Description
31:5			**Reserved Field:** Yes
4	force_clk_arb_en	R/W	force_clk_arb_en control the behavior of output signal clk_arb_en force_clk_arb_en = 0 indicate that clk_arb_en is asserated whenever core_ddrc_core_clk_arb is needed force_clk_arb_en = 1 indicate that clk_arb_en is always asserated **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3:1			**Reserved Field:** Yes
0	force_clk_te_en	R/W	force_clk_te_en control the behavior of output signal clk_te_en force_clk_te_en = 0 indicate that output clk_te_en is asserated whenever core_ddrc_core_clk_te is needed force_clk_te_en = 1 indicate that output clk_te_en is always asserated **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.136 INITTMG0

- **Name:** SDRAM Initialization Timing Register 0
- **Description:** SDRAM Initialization Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10d00
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

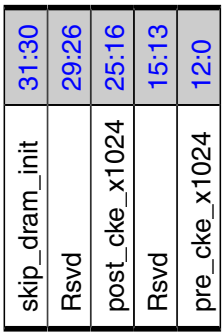


Table 3-211 Fields for Register: INITTMG0

Bits	Name	Memory Access	Description
31:30	skip_dram_init	R/W	If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed ■ 00 - SDRAM Initialization routine is run after power-up ■ 01 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Normal Mode ■ 11 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Self-refresh Mode ■ 10 - Reserved. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
29:26			**Reserved Field:** Yes

Table 3-211 Fields for Register: INITTMG0 (continued)

Bits	Name	Memory Access	Description
25:16	post_cke_x1024	R/W	Cycles to wait after driving CKE high to start the SDRAM initialization sequence. LPDDR4: typically requires this to be programmed for a delay of 2 us. LPDDR5: Don't care Not used for DDR5. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x2 **Programming Mode:** Static
15:13			**Reserved Field:** Yes
12:0	pre_cke_x1024	R/W	Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. LPDDR4: tINIT3 of 2 ms (min) LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send the first PDX command to the SDRAM - Assumption is that the first PDX is issued as part of initialization performed by PHY) For DDR4 RDIMMs, this must include the time needed to satisfy tSTAB. Not used for DDR5. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x4e **Programming Mode:** Static

3.2.137 PPT2CTRL0

- **Name:** PPT2 Control Register
- **Description:** PPT2 Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10f00
- **Exists:** DDRCTL_PPT2==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

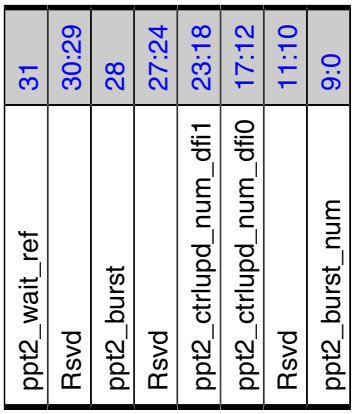


Table 3-212 Fields for Register: PPT2CTRL0

Bits	Name	Memory Access	Description
31	ppt2_wait_ref	R/W	Wait for REFab/REFpb before sending Normal PPT2. This register must be reset to '1' to bring DDRCTL out of lowest latency with Normal PPT2 enabled. The value can be changed while DFIUPDTMG2.ppt2_en=0 and PPT2STAT0.ppt2_burst_busy=0 ■ 0: Don't wait for REFab/REFpb ■ 1: Always Wait for REFab/REFpb FOR DEBUG ONLY. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
30:29			**Reserved Field:** Yes

Table 3-212 Fields for Register: PPT2CTRL0 (continued)

Bits	Name	Memory Access	Description
28	ppt2_burst	R/W1S	Setting this register bit to 1 triggers a Burst PPT2 operation. It is recommended to set this signal only if in normal operating mode. When the Burst PPT2 operation is complete, the DDRCTL automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this ppt2_burst bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
27:24			**Reserved Field:** Yes
23:18	ppt2_ctrlupd_num_dfi1	R/W	This register indicates the number of times to send ctrlupd_req for DFI1 per retraining_interval in Normal PPT2 operation. The value can be changed while DFIUPDTMG2.ppt2_en=0 and PPT2STAT0.ppt2_burst_busy=0 **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17:12	ppt2_ctrlupd_num_dfi0	R/W	This register indicates the number of times to send ctrlupd_req for DFI0 per retraining_interval in Normal PPT2 operation. The value can be changed while DFIUPDTMG2.ppt2_en=0 and PPT2STAT0.ppt2_burst_busy=0 **Value After Reset:** 0x8 **Programming Mode:** Dynamic
11:10			**Reserved Field:** Yes
9:0	ppt2_burst_num	R/W	This register indicates the number of times to send ctrlupd_req in Burst PPT2 operation. **Value After Reset:** 0x200 **Programming Mode:** Dynamic

3.2.138 PPT2STAT0

- **Name:** Status PPT2 Control Register
- **Description:** Status PPT2 Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10f10
- **Exists:** DDRCTL_PPT2==1

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

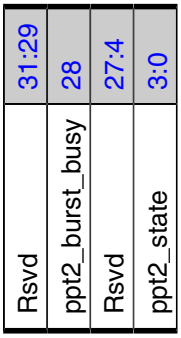


Table 3-213 Fields for Register: PPT2STAT0

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28	ppt2_burst_busy	R	SoC core may initiate a Burst PPT2 operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the Burst PPT2 request. It goes low when the Burst PPT2 operation is initiated in the DDRCTL. ■ 0 - Indicates that the SoC core can initiate a Burst PPT2 operation ■ 1 - Indicates that Burst PPT2 operation has not been initiated yet or ongoing in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
27:4			**Reserved Field:** Yes

Table 3-213 Fields for Register: PPT2STAT0 (continued)

Bits	Name	Memory Access	Description
3:0	ppt2_state	R	This register indicates the state of PPT2 scheduler. ■ 0 - Idle. Neither Normal PPT2 nor Burst PPT2 is enabled/ongoing ■ 1 - Normal PPT2 enabled. Waiting for dfi_t_ctrlupd_interval_type1 expiration ■ 2 - Normal PPT2 ongoing. Waiting for trigger condition; When DDRCTL is in Normal state, waiting for any REF command (according to PPT2CTRL0.ppt2_wait_ref). When DDRCTL is in Automatic SRPD, waiting for a PDX command. ■ 3 - Normal PPT2 ongoing. Waiting for ck stop ready ■ 4 - Normal PPT2 ongoing. Sending PPT2 request to PHY ■ 8 - Burst PPT2 ongoing **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.2.139 DDRCTL_VER_NUMBER

- **Name:** DDRCTL Version Number Register
- **Description:** DDRCTL Version Number Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ff8
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-214 Fields for Register: DDRCTL_VER_NUMBER

Bits	Name	Memory Access	Description
31:0	ver_number	R	Indicates the Device Version Number value. This is in ASCII format, with each byte corresponding to a character of the version number **Value After Reset:** "DDRCTL_VER_NUMBER_VAL" **Programming Mode:** Static

3.2.140 DDRCTL_VER_TYPE

- **Name:** DDRCTL Version Type Register
- **Description:** DDRCTL Version Type Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x10ffc
- **Exists:** Always

This register is in block REGB_DDRC_CH0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-215 Fields for Register: DDRCTL_VER_TYPE

Bits	Name	Memory Access	Description
31:0	ver_type	R	Indicates the Device Version Type value. This is in ASCII format, with each byte corresponding to a character of the version type **Value After Reset:** "DDRCTL_VER_TYPE_VAL" **Programming Mode:** Static

3.3 REGB_DDRC_CH1 Registers

This register block contains registers related to the control of functionality and the configuration of the DDRC controller. Registers shared by both channels are only present in REGB_DDRC_CH0.

3.3.1 MSTR4

- **Name:** Master Register4
- **Description:** Master Register4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11010
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

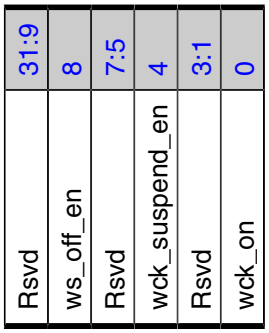


Table 3-216 Fields for Register: MSTR4

Bits	Name	Memory Access	Description
31:9			**Reserved Field:** Yes
8	ws_off_en	R/W	CAS-WS_OFF enable. If this bit is set to 1, the controller actively issues CAS-WS_OFF command. This register is valid only if MSTR4.wck_on is set to 1. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
7:5			**Reserved Field:** Yes

Table 3-216 Fields for Register: MSTR4 (continued)

Bits	Name	Memory Access	Description
4	wck_suspend_en	R/W	Enhanced WCK always on mode. If this register is set to 1, the controller issues CAS-WCK_SUSPEND command. This register is valid only if MSTR4.wck_on is set to 1. Note: CAS-WCK_SUSPEND command is valid only when MR0 OP[2]=1b(Enhanced WCK Always On mode supported) and MR18 OP[4]=1b(WCK Always On mode enabled). **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
3:1			**Reserved Field:** Yes
0	wck_on	R/W	WCK always ON mode ■ 0: WCK Always On mode disabled ■ 1: WCK Always On mode enabled In case of multi-rank system, the controller issues CAS-WS_FS to all ranks to sets DRAM in sync state simultaneously. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2

3.3.2 STAT

- **Name:** Operating Mode Status Register
- **Description:** Operating Mode Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11014
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

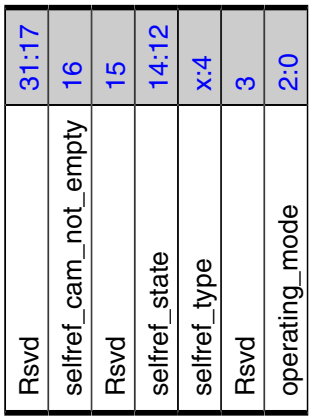


Table 3-217 Fields for Register: STAT

Bits	Name	Memory Access	Description
31:17			**Reserved Field:** Yes
16	selfref_cam_not_empty	R	Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. FOR DEBUG ONLY. Use OPCTRLCAM.dbg_wr_q_empty, OPCTRLCAM.dbg_rd_q_empty, STAT.selfref_state and STAT.selfref_type instead. **Value After Reset:** 0x0 **Programming Mode:** Static
15			**Reserved Field:** Yes

Table 3-217 Fields for Register: STAT (continued)

Bits	Name	Memory Access	Description
14:12	selfref_state	R	Self refresh state. This indicates self refresh or self refresh power down state or Deep Sleep Mode (LPDDR5 only). This register is used for frequency change and MRR/MRW access during self refresh. ■ 000 - SDRAM is not in Self Refresh. ■ 001 - Self refresh 1 ■ 010 - Self refresh power down ■ 011 - Self refresh 2 ■ 100 - Deep Sleep Mode (LPDDR5 only) **Value After Reset:** 0x0 **Programming Mode:** Static
x:4	selfref_type	R	Flags if Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5) is entered and if it was under Automatic Self Refresh control only or not. ■ 00 - SDRAM is not in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5). If CA parity retry is enabled by RETRYCTL0.capar_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. ■ 11 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. ■ 10 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. ■ 01 - SDRAM is in Self Refresh, which was caused by PHY Master Request or Normal PPT2. For LPDDR54 and DDR4, only bit[5:4] are used. For DDR5, self-refresh per rank control is supported. ■ bit[5:4] - rank 0 selfref_type ■ bit[7:6] - rank 1 selfref_type ■ bit[9:8] - rank 2 selfref_type ■ bit[11:10] - rank 3 selfref_type **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? (MEMC_NUM_RANKS*2) : 2" + 3
3			**Reserved Field:** Yes

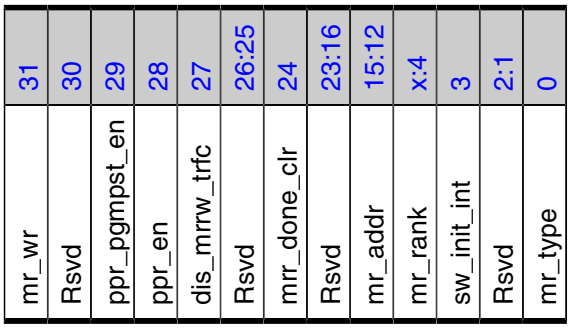
Table 3-217 Fields for Register: STAT (continued)

Bits	Name	Memory Access	Description
2:0	operating_mode	R	Operating mode. **DDR4/DDR5 designs:** ■ 000 - Init ■ 001 - Normal ■ 010 - Power-down (For DDR4, this means all ranks are in power-down state. For DDR5, this means at least one rank is in power-down state, check powerdown_state for details) ■ 011 - Self refresh (For DDR4/DDR5, this means all ranks are in self refresh state, check selfref_type for details) ■ 1XX - Maximum Power Saving Mode (For DDR4 only) **LPDDR4/LPDDR5designs:** ■ 000 - Init ■ 001 - Normal ■ 010 - Power-down ■ 011 - Self refresh / Self refresh power-down **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.3 MRCTRL0

- **Name:** Mode Register Read/Write Control Register 0.
- **Description:** Mode Register Read/Write Control Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11080
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31	30	29	28	27	26:25	24	23:16	15:12	x:4	3	2:1	0
mr_wr	Rsvd	ppr_pgmpst_en	ppr_en	dis_mrrw_trfc	Rsvd	mrr_done_clr	Rsvd	mr_addr	mr_rank	sw_init_int	Rsvd	mr_type

Table 3-218 Fields for Register: MRCTRL0

Bits	Name	Memory Access	Description
31	mr_wr	R/W1S	Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the DDRCTL automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30			**Reserved Field:** Yes
29	ppr_pgmpst_en	R/W	If this is set to one, writing MRCTRL0.mr_wr will insert a command gap of DDR4PPRTMG1.t_pgmpst_x32 after an MRS/MRW issued by MRCTRL0.mr_wr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-218 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
28	ppr_en	R/W	If this is set to one, writing MRCTRL0.mr_wr will trigger part of DDR4 or LPDDR5 PPR sequence i.e. ACT/WR/PRE if DDR4 PPR. ACT/PRE if LPDDR5 PPR. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
27	dis_mrrw_trfc	R/W	When this is set to 1, the DDRCTL does not perform the mode register operation during refresh operation (tRFC). In LPDDR4, MRR, MRW and MPC can be issued during tRFC. Thus this should be always set to 0. In LPDDR5/5X, MRW to change RFM level (MR57:OP[7:6]) is prohibited during tRFC. This needs to be set to 1 at that time. For all other LPDDR5/5X MRR, MRW and MPC which the DDRCTL currently supports, this should be set to 0. Note: Setting this to '1' is limited in Changing RFM level (ARFM) sequence only. Please contact Synopsys if you wish to use this for other purpose. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26:25			**Reserved Field:** Yes
24	mrr_done_clr	R/W1C	If this bit is set, mrr_done will be cleared by the controller. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:16			**Reserved Field:** Yes

Table 3-218 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
15:12	mr_addr	R/W	Address of the mode register that is to be written to. ■ 0000 - MR0 ■ 0001 - MR1 ■ 0010 - MR2 ■ 0011 - MR3 ■ 0100 - MR4 ■ 0101 - MR5 ■ 0110 - MR6 ■ 0111 - MR7 This signal is also used for writing to control words of the register chip on RDIMMs/LRDIMMs. In that case, it corresponds to the bank address bits sent to the RDIMM/LRDIMM. In case of DDR4, the bit[3:2] corresponds to the bank group bits. Therefore, the bit[3] as well as the bit[2:0] must be set to an appropriate value which is considered both the Address Mirroring of UDIMMs/RDIMMs/LRDIMMs and the Output Inversion of RDIMMs/LRDIMMs. Don't Care for LPDDR4/5 if PPR is not used. (see MRCTRL1.mr_data for mode register addressing in LPDDR4/5). If LPDDR5 PPR is used, 3 LSB bits of this field represents Bank and/or Bank group i.e., {BA2, BA1, BA0} in 16B mode and {BG0, BA1, BA0} in BG mode. Other bits don't take effect and should be 0. Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW/MRR access in DDR5). **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:4	mr_rank	R/W	Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits must be set to 1. However, for multi-rank UDIMMs/RDIMMs/LRDIMMs which implement address mirroring, it may be necessary to access ranks individually. Examples (assume DDRCTL is configured for 4 ranks): ■ 0x1 - select rank 0 only ■ 0x2 - select rank 1 only ■ 0x5 - select ranks 0 and 2 ■ 0xA - select ranks 1 and 3 ■ 0xF - select ranks 0, 1, 2 and 3 Don't Care for DDR5. **Value After Reset:** "(MEMC_NUM_RANKS==4) ? 0xF :((MEMC_NUM_RANKS==2) ? 0x3 : 0x1)" **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_NUM_RANKS" + 3

Table 3-218 Fields for Register: MRCTRL0 (continued)

Bits	Name	Memory Access	Description
3	sw_init_int	R/W	Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4/5, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. In LPDDR4 dual channel mode, note that this must be programmed to both channels beforehand. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. ■ 0 - Software intervention is not allowed ■ 1 - Software intervention is allowed Don't Care for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2:1			**Reserved Field:** Yes
0	mr_type	R/W	Indicates whether the mode register operation is read or write. ■ 0 - Write ■ 1 - Read Only used for LPDDR4/LPDDR5/DDR4. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.4 MRCTRL1

- **Name:** Mode Register Read/Write Control Register 1
- **Description:** Mode Register Read/Write Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11084
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

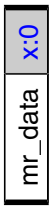


Table 3-219 Fields for Register: MRCTRL1

Bits	Name	Memory Access	Description
x:0	mr_data	R/W	Mode register write data for DDR4 mode. For LPDDR4/5, MRCTRL1[15:0] are interpreted as ■ [15:8] MR Address ■ [7:0] MR data for writes, don't care for read For PPR, this is used for row address field in the ACT command of the PPR sequence. Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW access in DDR5). **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.3.5 MRSTAT

- **Name:** Mode Register Read/Write Status Register
- **Description:** Mode Register Read/Write Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11090
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

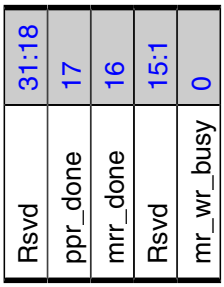


Table 3-220 Fields for Register: MRSTAT

Bits	Name	Memory Access	Description
31:18			**Reserved Field:** Yes
17	ppr_done	R	Indicate part of DDR4 or LPDDR5 PPR operation which is triggered by MRCTRL0.ppr_en is done. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	mrr_done	R	This signal goes high when the controller received MRR data which is triggered by MRCTRL0.mr_wr. This signal is cleared by mrr_done_clr **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:1			**Reserved Field:** Yes

Table 3-220 Fields for Register: MRSTAT (continued)

Bits	Name	Memory Access	Description
0	mr_wr_busy	R	The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when 'MRSTAT.mr_wr_busy' is high. ■ 0 - Indicates that the SoC core can initiate a mode register write operation ■ 1 - Indicates that mode register write operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.6 MRRDATA0

- **Name:** Mode Register Read Data 0
- **Description:** Mode Register Read Data 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11094
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

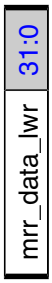


Table 3-221 Fields for Register: MRRDATA0

Bits	Name	Memory Access	Description
31:0	mrr_data_lwr	R	MRR data for DQ[31:0] This register is updated when the controller issued MRR command triggered by MRCTRL register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.7 MRRDATA1

- **Name:** Mode Register Read Data 1
- **Description:** Mode Register Read Data 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11098
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

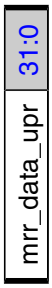


Table 3-222 Fields for Register: MRRDATA1

Bits	Name	Memory Access	Description
31:0	mrr_data_upr	R	MRR data for DQ[63:32] This register is updated when the controller issued MRR command triggered by MRCTRL register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.8 DERATECTL5

- **Name:** Temperature Derate Control Register 5
- **Description:** Temperature Derate Control Register 5
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11114
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

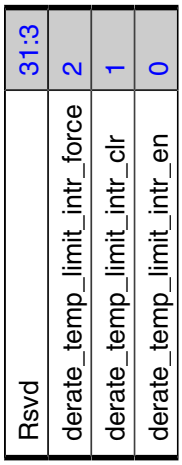


Table 3-223 Fields for Register: DERATECTL5

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	derate_temp_limit_intr_force	R/W1C	Interrupt force bit for derate_temp_limit_intr. Setting this register to 1 will cause the derate_temp_limit_intr output pin to be asserted. At the end of the interrupt force operation, the DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	derate_temp_limit_intr_clr	R/W1C	Interrupt clear bit for derate_temp_limit_intr. At the end of the interrupt clear operation, the DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-223 Fields for Register: DERATECTL5 (continued)

Bits	Name	Memory Access	Description
0	derate_temp_limit_intr_en	R/W	Interrupt enable bit for derate_temp_limit_intr output pin. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.9 DERATESTAT0

- **Name:** Temperature Derate Status Register 0
- **Description:** Temperature Derate Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11120
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

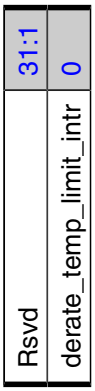


Table 3-224 Fields for Register: DERATESTAT0

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	derate_temp_limit_intr	R	Derate temperature interrupt indicating SDRAM temperature operating limit is exceeded. In LPDDR4, this register field is set to 1 when the value read from MR4[2:0] is 3'b000 or 3'b111. In LPDDR5, this register field is set to 1 when the value read from MR4[4:0] is 5'b00000 or 5'b11111 or invalid value. In DDR5, this register field is set to 1 when the value read from MR4[2:0] is the thresholds programmed by DERATECTL6.derate_low_temp_limit and DERATECTL6.derate_high_temp_limit. Cleared by register DERATECTL5.derate_temp_limit_intr_clr. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Static

3.3.10 DERATEDBGCTL

- **Name:** Temperature Derate Debug Contrl Register
- **Description:** Temperature Derate Debug Contrl Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11128
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

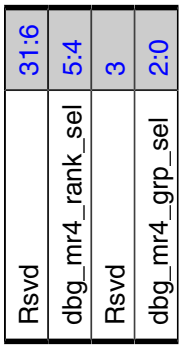


Table 3-225 Fields for Register: DERATEDBGCTL

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:4	dbg_mr4_rank_sel	R/W	MR4 rank select in case of multi ranks **Value After Reset:** 0x0 **Programming Mode:** Static
3			**Reserved Field:** Yes
2:0	dbg_mr4_grp_sel	R/W	For DDR5, MR4 data group select based on 4 device MRR read data. For LPDDR54, this is used to select MR4 data on the upper side device or the lower side device to display on DERATEDBGSTAT register. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.11 DERATEDBGSTAT

- **Name:** Temperature Derate Debug Status Register
- **Description:** Temperature Derate Debug Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1112c
- **Exists:** DDRCTL_DDR_OR_MEMC_LPDDR4==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

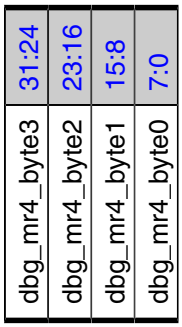


Table 3-226 Fields for Register: DERATEDBGSTAT

Bits	Name	Memory Access	Description
31:24	dbg_mr4_byte3	R	Byte 3 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 7 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-226 Fields for Register: DERATEDBGSTAT (continued)

Bits	Name	Memory Access	Description
23:16	dbg_mr4_byte2	R	Byte 2 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 6 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8	dbg_mr4_byte1	R	Byte 1 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1). This register shows the byte 5 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:0	dbg_mr4_byte0	R	Byte 0 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5 : It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1).This register shows the byte 4 of 64 bits MR4 data if DERATEDBGCTL.dbg_mr4_grp_sel=1 and MEMC_DRAM_DATA_WIDTH==64. For DDR5: It is only updated from MRR4 with TCR update enabled. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.12 PWRCTL

- **Name:** Low Power Control Register
- **Description:** Low Power Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11180
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

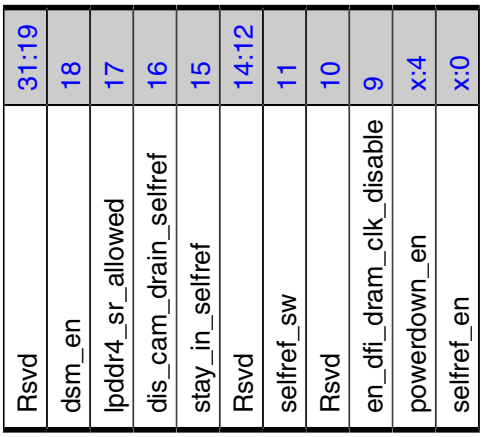


Table 3-227 Fields for Register: PWRCTL

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	dsm_en	R/W	A value of 1 to this register causes system to move to Deep Sleep Mode state immediately. ■ 1 - Entry to Deep Sleep Mode ■ 0 - Exit from Deep Sleep Mode **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-227 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
17	lpddr4_sr_allowed	R/W	Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register should be set to '1' if any of PHYMSTR, PPT or HWFFC feature is enabled. This register field cannot be modified while PWRCTL.selfref_sw==1. ■ 0 - SR-PD -> SR -> SR-PD not allowed ■ 1 - SR-PD -> SR -> SR-PD allowed Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	dis_cam_drain_selfref	R/W	Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. ■ 0 - CAMs must be empty before entering SR ■ 1 - CAMs are not emptied before entering SR (unsupported) Note, PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. PWRCTL.dis_cam_drain_selfref=0 is required. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15	stay_in_selfref	R/W	Self refresh state is an intermediate state to enter to Self refresh power down state or exit Self refresh power down state for LPDDR4/5. This register controls transition from the Self refresh state. ■ 1 - Prohibit transition from Self refresh state ■ 0 - Allow transition from Self refresh state **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14:12			**Reserved Field:** Yes
11	selfref_sw	R/W	A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating mode. This is referred to as Software Entry/Exit to Self Refresh. ■ 1 - Software Entry to Self Refresh ■ 0 - Software Exit from Self Refresh **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-227 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
10			**Reserved Field:** Yes
9	en_dfi_dram_clk_disable	R/W	Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR4, can be asserted in following: ■ in Self Refresh ■ in Maximum Power Saving Mode In LPDDR4/LPDDR5, can be asserted in following: ■ in Self Refresh Power Down ■ in Power Down ■ during Normal operation (Clock Stop) In DDR5, can be asserted in following: ■ in Self Refresh In DDR5 (L)RDIMM, the value of this field need to be same as DIMMCTL.dimm_selfref_clock_stop_mode. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:4	powerdown_en	R/W	If true then the DDRCTL goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[4] is used. For DDR5, powerdown per rank enable is supported. ■ bit[4] - rank 0 powerdown_en ■ bit[5] - rank 1 powerdown_en ■ bit[6] - rank 2 powerdown_en ■ bit[7] - rank 3 powerdown_en **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? MEMC_NUM_RANKS : 1" + 3

Table 3-227 Fields for Register: PWRCTL (continued)

Bits	Name	Memory Access	Description
x:0	selfref_en	R/W	If true then the DDRCTL puts the SDRAM per rank into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[0] is used. For DDR5, self-refresh per rank enable is provided. Current self-refresh need to be enabled for all ranks. For DDR5 (L)RDIMM, self-refresh need to be enabled for all ranks of both channels. ■ bit[0] - rank 0 selfref_en ■ bit[1] - rank 1 selfref_en ■ bit[2] - rank 2 selfref_en ■ bit[3] - rank 3 selfref_en **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "(DDRCTL_DDR_EN==1) ? MEMC_NUM_RANKS : 1" - 1

3.3.13 HWLPCTL

- **Name:** Hardware Low Power Control Register
- **Description:** Hardware Low Power Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11184
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

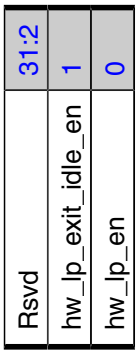


Table 3-228 Fields for Register: HWLPCTL

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	hw_lp_exit_idle_en	R/W	When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). **Value After Reset:** 0x1 **Testable:** readOnly **Programming Mode:** Static
0	hw_lp_en	R/W	Enable for Hardware Low Power Interface. This field should be updated only when system in SW self-refresh. Please follow Programming guide for configure this field. Please refer to the section of Hardware Low-Power Interfaces in databook. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.14 ZQCTL1

- **Name:** ZQ Control Register 1
- **Description:** ZQ Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11284
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

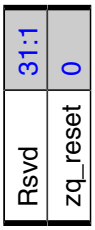


Table 3-229 Fields for Register: ZQCTL1

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	zq_reset	R/W1S	Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the DDRCTL automatically clears this bit. It is recommended NOT to set this register bit if in Init, in SR-Powerdown or Deep Sleep Modes. For SR-Powerdown it will be scheduled after SRPD has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.3.15 ZQSTAT

- **Name:** ZQ Status Register
- **Description:** ZQ Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1128c
- **Exists:** DDRCTL_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-230 Fields for Register: ZQSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	zq_reset_busy	R	SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ZQ Reset operation ■ 1 - Indicates that ZQ Reset operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.16 DQSOSCSTAT0

- **Name:** DQS/WCK Oscillator Status Register 0
- **Description:** DQS/WCK Oscillator Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11304
- **Exists:** LPDDR45_DQSOSC_EN==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

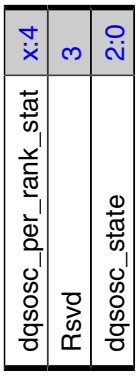


Table 3-231 Fields for Register: DQSOSCSTAT0

Bits	Name	Memory Access	Description
x:4	dqsosc_per_rank_stat	R	DQS/WCK Oscillator per rank status. This bit is set to 0 when DQSOSCCTL0.dqsosc_enable is set to 1, and set to 1 when the DQS Oscillator command sequence is started for the corresponding active rank. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** MEMC_NUM_RANKS + 3
3			**Reserved Field:** Yes

Table 3-231 Fields for Register: DQSOSCSTAT0 (continued)

Bits	Name	Memory Access	Description
2:0	dqsosc_state	R	DQS/WCK Oscillator Control State Status. ■ 000 - DQSOSC_IDLE ■ 001 - DQSOSC_START: Sending MPC ■ 010 - DQSOSC_RUNTIME: Waiting for runtime passed ■ 011 - DQSOSC_GET_RESULT1: Sending first MRR ■ 100 - DQSOSC_WAIT1: Waiting for tMRR for sending next MRR ■ 101 - DQSOSC_GET_RESULT2: Sending second MRR ■ 110 - DQSOSC_WAIT2: Waiting for tMRR or rank gap The value 0 indicates nothing is being done for DQS Oscillator. Otherwise, DQS Oscillator is running and reflects the current state of DQSOSC. It can be used for debug only to ascertain the current state of DQSOSC controller if it is stuck to one particular state. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.17 HWFFCSTAT

- **Name:** Hardware Fast Frequency Change (HWFFC) Status Register
- **Description:** Hardware Fast Frequency Change (HWFFC) Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11404
- **Exists:** UMCTL2_HWFFC_EN==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

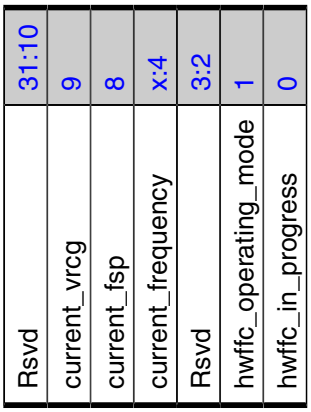


Table 3-232 Fields for Register: HWFFCSTAT

Bits	Name	Memory Access	Description
31:10			**Reserved Field:** Yes
9	current_vrcg	R	Indicates current value of VRCG (MR13 OP[3] for LPDDR4). This field is only applicable for legacy HWFFC. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
8	current_fsp	R	Indicates current value of FSP-OP (MR13 OP[7] for LPDDR4. MR16 OP[2] for LPDDR5). **Value After Reset:** 0x1 **Programming Mode:** Dynamic

Table 3-232 Fields for Register: HWFFCSTAT (continued)

Bits	Name	Memory Access	Description
x:4	current_frequency	R	Indicates the current frequency. ■ 0 - Frequency 0/Normal ■ 1 - Frequency 1/FREQ1 ■ 2 - Frequency 2/FREQ2 ■ 3 - Frequency 3/FREQ3 ■ 4 - Frequency 4/FREQ4 ■ 5 - Frequency 5/FREQ5 ■ 6 - Frequency 6/FREQ6 ■ 7 - Frequency 7/FREQ7 ■ 8 - Frequency 8/FREQ8 ■ 9 - Frequency 9/FREQ9 ■ 10 - Frequency 10/FREQ10 ■ 11 - Frequency 11/FREQ11 ■ 12 - Frequency 12/FREQ12 ■ 13 - Frequency 13/FREQ13 ■ 14 - Frequency 14/FREQ14 **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_FREQUENCY_BITS" + 3
3:2			**Reserved Field:** Yes
1	hwffc_operating_mode	R	Operating mode of HWFFC. ■ 0 - Normal ■ 1 - Self Refresh or SR-Powerdown **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	hwffc_in_progress	R	Indicates HWFFC is in progress. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.18 HWFFC_MRWBUF_CTRL0

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 0
- **Size:** 32 bits
- **Offset:** 0x11410
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH1.

Table 3-233 Fields for Register: HWFFC_MRWBUF_CTRL0

Bits	Name	Memory Access	Description
31	hwffc_mrwbuf_rw_start	R/W1C	Assert this bit to trigger a read/write operation to MRW buffer. This bit is self-cleared. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30	hwffc_mrwbuf_rw_type	R/W	rw type for MRW buffer, ■ 1 - write ■ 0 - read **Value After Reset:** 0x0 **Programming Mode:** Dynamic
x:24	hwffc_mrwbuf_select	R/W	PState select, select to access which PState in MRW buffer ■ 0 - PState 0 ■ 1 - PState 1 ■ 13 - PState 13 ■ 14 - PState 14 **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_FREQUENCY_BITS" + 23

Table 3-233 Fields for Register: HWFFC_MRWBUF_CTRL0 (continued)

Bits	Name	Memory Access	Description
x:16	hwffc_mrwbuf_addr	R/W	MRW buffer address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_MRWBUF_DEPTH_LOG2 - DDRCTL_FREQUENCY_BITS" + 15
15:0			**Reserved Field:** Yes

3.3.19 HWFFC_MRWBUF_CTRL1

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer control register 1
- **Size:** 32 bits
- **Offset:** 0x11414
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH1.

Table 3-234 Fields for Register: HWFFC_MRWBUF_CTRL1

Bits	Name	Memory Access	Description
x:0	hwffc_mrwbuf_wdata	R/W	Encoded MRW value written into HWFFC MRW buffer. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_MRWBUF_DATA_WIDTH" - 1

3.3.20 HWFFC_MRWBUF_STAT

- **Name:** Hardware Fast Frequency Change (HWFFC) MRW buffer status register
- **Description:** Hardware Fast Frequency Change (HWFFC) MRW buffer status register
- **Size:** 32 bits
- **Offset:** 0x11418
- **Exists:** DDRCTL_HWFFC_EXT_AND_LPDDR5X==1

This register is in block REGB_DDRC_CH1.

Table 3-235 Fields for Register: HWFFC_MRWBUF_STAT

Bits	Name	Memory Access	Description
x:0	hwffc_mrwbuf_rdata	R	Encoded MRW value returned from HWFFC MRW buffer. **Value After Reset:** 0x0 **Testable:** readOnly **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "DDRCTL_MRWBUF_DATA_WIDTH" - 1

3.3.21 DFISTAT

- **Name:** DFI Status Register
- **Description:** DFI Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11514
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

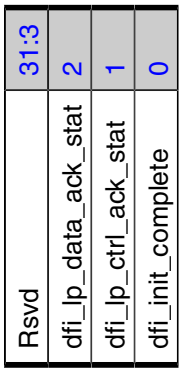


Table 3-236 Fields for Register: DFISTAT

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_lp_data_ack_stat	R	Stores the value of the dfi_lp_data_ack input to the controller. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	dfi_lp_ctrl_ack_stat	R	Stores the value of the dfi_lp_ctrl_ack input to the controller. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	dfi_init_complete	R	The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.22 DFI0MSGCTL0

- **Name:** DFI0 Message Control Register 0.
- **Description:** DFI0 Message Control Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11520
- **Exists:** DDRCTL_DFI_CTRLMSG==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

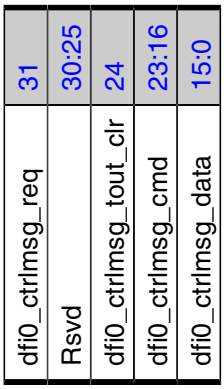


Table 3-237 Fields for Register: DFI0MSGCTL0

Bits	Name	Memory Access	Description
31	dfi0_ctrlmsg_req	R/W1S	Setting this register bit to 1 triggers a DFI controller message transmission operation. DDRCTL automatically clear this bit when the DFI controller message request (dfi0_ctrlmsg_req) is asserted at the DFI MC to PHY Message port interface . This bit must be programmed separately after programming other register fields appropriately of this register. Note: ■ DFI controller message request can be issued only if DFIPHYMSTR.dfi_phymstr_en = 1 ■ DFI controller message request must not be set during DFI LP mode due to software controlled low power entry. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
30:25			**Reserved Field:** Yes

Table 3-237 Fields for Register: DFI0MSGCTL0 (continued)

Bits	Name	Memory Access	Description
24	dfi0_ctrlmsg_tout_clr	R/W1C	If this bit is set, DFI0MSGSTAT0.dfi0_ctrlmsg_resp_tout is cleared by the controller. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:16	dfi0_ctrlmsg_cmd	R/W	DFI0 controller message command. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0	dfi0_ctrlmsg_data	R/W	DFI0 controller message data. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.23 DFI0MSGSTAT0

- **Name:** DFI0 Message Status Register 0
- **Description:** DFI0 Message Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11524
- **Exists:** DDRCTL_DFI_CTRLMSG==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

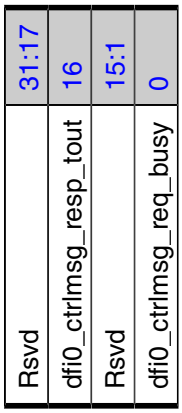


Table 3-238 Fields for Register: DFI0MSGSTAT0

Bits	Name	Memory Access	Description
31:17			**Reserved Field:** Yes
16	dfi0_ctrlmsg_resp_tout	R	This bit is set if dfi0_ctrlmsg_ack is not asserted by PHY within dfi_t_ctrlmsg_resp after asserting dfi0_ctrlmsg_req **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:1			**Reserved Field:** Yes
0	dfi0_ctrlmsg_req_busy	R	The SoC must trigger DFI controller message request only if this signal is low. This signal goes high in the clock after the DDRCTL accepts software triggered DFI controller message request by writing into DFI0MSGCTRL0.dfi0_ctrlmsg_req. It goes low when PHY deasserts dfi0_ctrlmsg_ack or dfi0_ctrlmsg_resp_tout event has triggered. ■ 0 - Indicates that the SoC core can initiate a DFI controller message request operation ■ 1 - Indicates that DFI controller message request operation is in progress **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.24 DFISBINTRPTCFG

- **Name:** DFI Sideband Watchdog Timer Interrupt Configuration Register
- **Description:** DFI Sideband Watchdog Timer Interrupt Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11528
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-239 Fields for Register: DFISBINTRPTCFG

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_sideband_timer_err_intr_force	R/W1C	Interrupt force bit for dfi_sideband_timer_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering and interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-239 Fields for Register: DFISBINTRPTCFG (continued)

Bits	Name	Memory Access	Description
1	dfi_sideband_timer_err_intr_clr	R/W1C	Clear DFI Sideband timer error interrupt (dfi_sideband_timer_err_intr). Setting this bit also clears all the error status bits in DFISBTIMERSTAT and DFISBTIMERSTAT1 registers. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	dfi_sideband_timer_err_intr_en	R/W	Enables interrupt generation when error is detected on any of the DFI Sideband watchdog timers. The name of the interrupt that is enabled is dfi_sideband_timer_err_intr. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.25 DFISBPOISONCFG

- **Name:** DFI Sideband Watchdog Timer Poison Control Register
- **Description:** DFI Sideband Watchdog Timer Poison Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11530
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31:28	27:24	23:20	19:16	15:12	11	10	9	8	7:6	5	4	3:2	1	0
dfi_tlp_data_resp_poison_margin	dfi_tlp_ctrl_resp_poison_margin	dfi_tinit_start_poison_margin	dfi_tctrlupd_min_poison_margin	Rsvd	dfi_tlp_data_wakeup_poison_err_inj	dfi_tlp_ctrl_wakeup_poison_err_inj	dfi_tlp_data_resp_poison_err_inj	dfi_tlp_ctrl_resp_poison_err_inj	Rsvd	dfi_tinit_complete_poison_err_inj	dfi_tinit_start_poison_err_inj	Rsvd	dfi_tctrlupd_max_poison_err_inj	dfi_tctrlupd_min_poison_err_inj

Table 3-240 Fields for Register: DFISBPOISONCFG

Bits	Name	Memory Access	Description
31:28	dfi_tlp_data_resp_poison_margin	R/W	Specifies the number of clock cycles for which dfi_lp_data_req will be asserted when doing the DFILPTMG1.dfi_tlp_resp duration poison error testing. DFISBPOISONCFG.dfi_tlp_data_resp_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFILPTMG1.dfi_tlp_resp register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1

Table 3-240 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
27:24	dfi_tlp_ctrl_resp_poison_margin	R/W	Specifies the number of clock cycles for which dfi_lp_ctrl_req will be asserted when doing the DFILPTMG1.dfi_tlp_resp duration poison error testing. DFISBPOISONCFG.dfi_tlp_ctrl_resp_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFILPTMG1.dfi_tlp_resp register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
23:20	dfi_tinit_start_poison_margin	R/W	Specifies the number of clock cycles for which dfi_init_start will be asserted when doing the minimum duration poison error testing. DFISBPOISONCFG.dfi_tinit_start_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFITMG7.dfi_t_init_start register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
19:16	dfi_tctrlupd_min_poison_margin	R/W	Specifies the number of clock cycles for which dfi_ctrlupd_req will be asserted when doing the minimum duration poison error testing. DFISBPOISONCFG.dfi_tctrlupd_min_poison_err_inj is set to 1 while doing this test. It is recommended to leave this register at the Reset value. But if it is changed, the value should be set smaller than DFIUPDTMG0.dfi_t_ctrlup_min register field. **Value After Reset:** 0x3 **Programming Mode:** Quasi-dynamic Group 1
15:12			**Reserved Field:** Yes
11	dfi_tlp_data_wakeup_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum deassertion time requirement of dfi_lp_data_ack signal. This will result in the DFISBTIMERSTAT.dfi_tlp_data_wakeup_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1

Table 3-240 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
10	dfi_tlp_ctrl_wakeup_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum deassertion time requirement of dfi_lp_ctrl_ack signal. This will result in the DFISBTIMERSTAT.dfi_tlp_ctrl_wakeup_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
9	dfi_tlp_data_resp_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_lp_data_req signal. This will result in the DFISBTIMERSTAT.dfi_tlp_data_resp_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
8	dfi_tlp_ctrl_resp_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_lp_ctrl_req signal. This will result in the DFISBTIMERSTAT.dfi_tlp_ctrl_resp_error bit to be set when a Low power entry request is made by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
7:6			**Reserved Field:** Yes
5	dfi_tinit_complete_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum reassertion time requirement of dfi_init_complete signal. This will result in the DFISBTIMERSTAT.dfi_tinit_complete_error bit to be set when a frequency change request is initiated by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
4	dfi_tinit_start_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum duration for which dfi_init_start signal should stay asserted once it is asserted. This will result in the DFISBTIMERSTAT.dfi_tinit_start_error bit to be set when a frequency change request is initiated by the Controller. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
3:2			**Reserved Field:** Yes

Table 3-240 Fields for Register: DFISBPOISONCFG (continued)

Bits	Name	Memory Access	Description
1	dfi_tctrlupd_max_poison_err_inj	R/W	If set to 1, poison the logic that checks the maximum assertion time requirement of dfi_ctrlupd_req signal. This will result in the DFISBTIMERSTAT.dfi_tctrlupd_max_error bit to be set when a Controller initiated Update request is send to PHY. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1
0	dfi_tctrlupd_min_poison_err_inj	R/W	If set to 1, poison the logic that checks the minimum assertion time requirement of dfi_ctrlupd_req signal. This will result in the DFISBTIMERSTAT.dfi_tctrlupd_min_error bit to be set when a Controller initiated Update request is send to PHY. **Value After Reset:** 0x0 **Programming Mode:** Quasi-dynamic Group 1

3.3.26 DFISBTIMERSTAT

- **Name:** DFI Sideband Watchdog Timer Status Register
- **Description:** DFI Sideband Watchdog Timer Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11538
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31:12	11	10	9	8	7:6	5	4	3	2	1	0
Rsvd	dfi_tlp_data_wakeup_error	dfi_tlp_ctrl_wakeup_error	dfi_tlp_data_resp_error	dfi_tlp_ctrl_resp_error	Rsvd	dfi_tinit_complete_error	dfi_tinit_start_error	Rsvd	dfi_tctrlupd_max_error	dfi_tctrlupd_min_error	Rsvd

Table 3-241 Fields for Register: DFISBTIMERSTAT

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11	dfi_tlp_data_wakeup_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_data_wakeup timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	dfi_tlp_ctrl_wakeup_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_ctrl_wakeup timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
9	dfi_tlp_data_resp_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_data_resp timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-241 Fields for Register: DFISBTIMERSTAT (continued)

Bits	Name	Memory Access	Description
8	dfi_tlp_ctrl_resp_error	R	This bit is set to 1 when an error is detected on the dfi_tlp_ctrl_resp timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:6			**Reserved Field:** Yes
5	dfi_tinit_complete_error	R	This bit is set to 1 when an error is detected on the dfi_tinit_complete_error timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	dfi_tinit_start_error	R	This bit is set to 1 when an error is detected on the dfi_tinit_start timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3			**Reserved Field:** Yes
2	dfi_tctrlupd_max_error	R	This bit is set to 1 when an error is detected on the dfi_tctrlupd_max timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	dfi_tctrlupd_min_error	R	This bit is set to 1 when an error is detected on the dfi_tctrlupd_min timer. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0			**Reserved Field:** Yes

3.3.27 DFISBTIMERSTAT1

- **Name:** DFI Sideband Watchdog Timer Status Register 1
- **Description:** DFI Sideband Watchdog Timer Status Register 1
- **Size:** 32 bits
- **Offset:** 0x11540
- **Exists:** DDRCTL_DFI_SB_WDT==1

This register is in block REGB_DDRC_CH1.

Table 3-242 Fields for Register: DFISBTIMERSTAT1

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	dfi_sideband_timer_err_intr	R	This interrupt bit is set when any of the DFI Sideband Watchdog timers fail. It remains set until cleared by DFISBINTRPTCFG.dfi_sideband_timer_err_intr_clr. Read all the fields of the DFISBTIMERSTAT register to get information on which timer failed before clearing the interrupt. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.28 DFIERRINTRPTCFG

- **Name:** DFI Error Interface Interrupt Configuration Register
- **Description:** DFI Error Interface Interrupt Configuration Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11548
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-243 Fields for Register: DFIERRINTRPTCFG

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	dfi_error_intr_force	R/W1C	Interrupt force bit for dfi_error_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	dfi_error_intr_clr	R/W1C	Interrupt clear bit for DFI Error Interrupt (dfi_error_intr). This also clears the following two error status fields: DFIERRORSTAT.dfi_error_intr and DFIERRORSTAT1.dfi_error_info register fields. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-243 Fields for Register: DFIERRINTRPTCFG (continued)

Bits	Name	Memory Access	Description
0	dfi_error_intr_en	R/W	Interrupt enable bit for DFI Error Interrupt (dfi_error_intr). This interrupt is set when error is detected on the dfi_error input signal coming from PHY. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.29 DFIERRORSTAT

- **Name:** DFI Error Interface Status Register
- **Description:** DFI Error Interface Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11550
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-244 Fields for Register: DFIERRORSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	dfi_error_intr	R	This bit is set to 1 when PHY asserts dfi_error signal. The bit remains set until it is cleared using the register bit DFIERRINTRPTCFG.dfi_error_intr_clr. Only one error will be captured at any time. Any error indicated on dfi_error input signal between the setting and clearing of this register bit won't be captured. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.30 DFIERRORSTAT1

- **Name:** DFI Error Interface Status Register 1
- **Description:** DFI Error Interface Status Register 1
- **Size:** 32 bits
- **Offset:** 0x11558
- **Exists:** DDRCTL_DFI_ERROR==1

This register is in block REGB_DDRC_CH1.

Table 3-245 Fields for Register: DFIERRORSTAT1

Bits	Name	Memory Access	Description
31:4			**Reserved Field:** Yes
3:0	dfi_error_info	R	This field has the value that is send by PHY on the dfi_error_info signal. This field is valid when bit[0] of this register is 1. This bit remains set until it is cleared using the register bit DFIERRINTRPTCFG.dfi_error_intr_clr. Only one error will be captured at any time. Any error indicated on dfi_error_info input signal between the setting and clearing of this register bit won't be captured. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.31 ECCSTAT

- **Name:** SECDED ECC Status Register
- **Description:** SECDED ECC Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11608
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.
Valid only in MEMC_ECC_SUPPORT==1 or 3 (SECDED ECC mode)

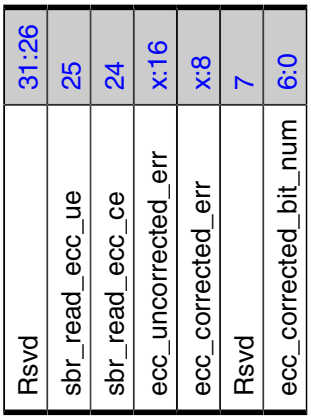


Table 3-246 Fields for Register: ECCSTAT

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25	sbr_read_ecc_ue	R	Indicates the sideband SECDED ECC uncorrectable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_uncorrected_err_clr. This bit is not applicable for Inline ECC ■ 0 - Mainline/Demand read uncorrectable error interrupt ■ 1 - Scrubber read uncorrectable error interrupt **Value After Reset:** 0x0 **Programming Mode:** Static
24	sbr_read_ecc_ce	R	Indicates the sideband SECDED ECC correctable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_corrected_err_clr. This bit is not applicable for Inline ECC ■ 0 - Mainline/Demand read correctable error interrupt ■ 1 - Scrubber read correctable error interrupt **Value After Reset:** 0x0 **Programming Mode:** Static

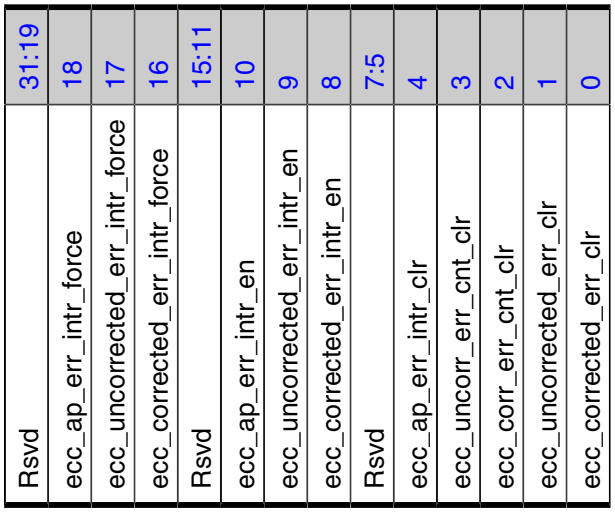
Table 3-246 Fields for Register: ECCSTAT (continued)

Bits	Name	Memory Access	Description
x:16	ecc_uncorrected_err	R	Double-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate uncorrectable error on any lane. When External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1, bit 16 is only valid. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(MEMC_INLINE_ECC_EN==1 && MEMC_SIDEBAND_ECC_EN==0) ? 1 : (MEMC_FREQ_RATIO==4) ? 8 : 4" + 15
x:8	ecc_corrected_err	R	Single-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate correctable error on any lane. When External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1, bit 8 is only valid. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "(MEMC_INLINE_ECC_EN==1 && MEMC_SIDEBAND_ECC_EN==0) ? 1 : (MEMC_FREQ_RATIO==4) ? 8 : 4" + 7
7			**Reserved Field:** Yes
6:0	ecc_corrected_bit_num	R	Bit number corrected by single-bit ECC error. See ECC section of architecture chapter for encoding of this field. If more than one data lane has an error, the lower data lane is selected. This register is 7 bits wide in order to handle 72 bits of the data present in a single lane. This field is not applicable when External ECC Log is enabled (DDRCTL_EXT_RAS_LOG_EN=1) and ECCCFG2.bypass_internal_ecc=1. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.32 ECCCTL

- **Name:** ECC Clear Register
- **Description:** ECC Clear Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1160c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.



31:19	18	17	16	15:11	10	9	8	7:5	4	3	2	1	0
Rsvd	ecc_ap_err_intr_force	ecc_uncorrected_err_intr_force	ecc_corrected_err_intr_force	Rsvd	ecc_ap_err_intr_en	ecc_uncorrected_err_intr_en	ecc_corrected_err_intr_en	Rsvd	ecc_ap_err_intr_clr	ecc_uncorr_err_cnt_clr	ecc_corr_err_cnt_clr	ecc_uncorrected_err_clr	ecc_corrected_err_clr

Table 3-247 Fields for Register: ECCCTL

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	ecc_ap_err_intr_force	R/W1C	Interrupt force bit for ecc_ap_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	ecc_uncorrected_err_intr_force	R/W1C	Interrupt force bit for ecc_uncorrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-247 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
16	ecc_corrected_err_intr_force	R/W1C	Interrupt force bit for ecc_corrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
15:11			**Reserved Field:** Yes
10	ecc_ap_err_intr_en	R/W	Interrupt enable bit for ecc_ap_err_intr. ■ 1: Enabled ■ 0: Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
9	ecc_uncorrected_err_intr_en	R/W	Interrupt enable bit for ecc_uncorrected_err_intr. ■ 1: Enabled ■ 0: Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
8	ecc_corrected_err_intr_en	R/W	Interrupt enable bit for ecc_corrected_err_intr. ■ 1 Enabled ■ 0 Disabled **Value After Reset:** 0x1 **Programming Mode:** Dynamic
7:5			**Reserved Field:** Yes
4	ecc_ap_err_intr_clr	R/W1C	Interrupt clear bit for ecc_ap_err. If this bit is set, the ECCAPSTAT.ecc_ap_err/ecc_ap_err_intr will be cleared. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-247 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
3	ecc_uncorr_err_cnt_clr	R/W1C	Setting this register bit to 1 clears the currently stored uncorrected ECC error count. The ECCERRCNT.ecc_uncorr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	ecc_corr_err_cnt_clr	R/W1C	Setting this register bit to 1 clears the currently stored corrected ECC error count. The ECCERRCNT.ecc_corr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	ecc_uncorrected_err_clr	R/W1C	Setting this register bit to 1 clears the currently stored uncorrected ECC error. The following registers are cleared: ■ ECCSTAT.ecc_uncorrected_err ■ ECCSTAT.sbr_read_ecc_ue ■ ADVECCSTAT.sbr_read_advecc_ue ■ ADVECCSTAT.advecc_ue_kbd_stat ■ ADVECCSTAT.advecc_uncorrected_err ■ ECCUSYN0 ■ ECCUSYN1 ■ ECCUSYN2 ■ ECCUDATA0 ■ ECCUDATA1 ■ ECCSYMBOL.ecc_uncorr_sym_71_64 DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-247 Fields for Register: ECCCTL (continued)

Bits	Name	Memory Access	Description
0	ecc_corrected_err_clr	R/W1C	Setting this register bit to 1 clears the currently stored corrected ECC error. The following registers are cleared: ■ ECCSTAT.ecc_corrected_err ■ ECCSTAT.sbr_read_ecc_ce ■ ADVECCSTAT.sbr_read_advecc_ce ■ ADVECCSTAT.advecc_ce_kbd_stat ■ ADVECCSTAT.advecc_corrected_err ■ ADVECCSTAT.advecc_num_err_symbol ■ ADVECCSTAT.advecc_err_symbol_pos ■ ADVECCSTAT.advecc_err_symbol_bits ■ ECCCSYN0 ■ ECCCSYN1 ■ ECCCSYN2 ■ ECCBITMASK0 ■ ECCBITMASK1 ■ ECCBITMASK2 ■ ECCCDATA0 ■ ECCCDATA1 ■ ECCSYMBOL.ecc_corr_sym_71_64 DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.3.33 ECCERRCNT

- **Name:** ECC Error Counter Register
- **Description:** ECC Error Counter Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11610
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

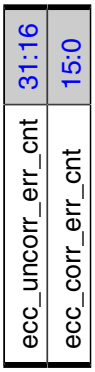


Table 3-248 Fields for Register: ECCERRCNT

Bits	Name	Memory Access	Description
31:16	ecc_uncorr_err_cnt	R	Number of uncorrectable ECC errors detected. For internal ECC or external ECC with External ECC Log disabled, it is incremented by the total number of decoders reporting UE in each cycle. For external ECC with External ECC Log enabled (DDRCTL_EXT_RAS_LOG_EN=1), It is incremented by 1 UE in each cycle. It will saturates at 0xFFFF **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0	ecc_corr_err_cnt	R	Number of correctable ECC errors detected. For internal ECC or external ECC with External ECC Log disabled, it is incremented by the total number of decoders reporting CE in each cycle. For external ECC with External ECC Log enabled (DDRCTL_EXT_RAS_LOG_EN=1), It is incremented by 1 CE in each cycle. It will saturates at 0xFFFF **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.34 ECCCADDR0

- **Name:** ECC Corrected Error Address Register 0
- **Description:** ECC Corrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11614
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

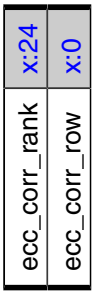


Table 3-249 Fields for Register: ECCCADDR0

Bits	Name	Memory Access	Description
x:24	ecc_corr_rank	R	Indicates the rank number of a read resulting in a corrected ECC error **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	ecc_corr_row	R	Indicates the page/row number of a read resulting in a corrected ECC error. This is 18-bits wide in configurations with LPDDR5 or DDR4 support and 16-bits in all other configurations. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.3.35 ECCCADDR1

- **Name:** ECC Corrected Error Address Register 1
- **Description:** ECC Corrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11618
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

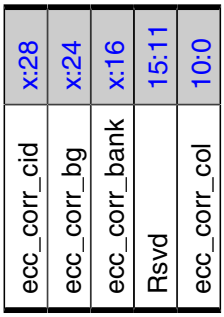


Table 3-250 Fields for Register: ECCCADDR1

Bits	Name	Memory Access	Description
x:28	ecc_corr_cid	R	CID number of a read resulting in a corrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "UMCTL2_CID_WIDTH" + 27
x:24	ecc_corr_bg	R	Bank Group number of a read resulting in a corrected ECC error. Note that when LPDDR5 16B mode is in use, this field is used as the upper bits of the bank address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	ecc_corr_bank	R	Bank number of a read resulting in a corrected ECC error. Note that when LPDDR5 16B mode is in use, {ECCCADDR1.ecc_corr_bg, ECCCADDR1.ecc_corr_bank[1:0]} shows bank number of a read resulting in a corrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-250 Fields for Register: ECCCADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	ecc_corr_col	R	Block number of a read resulting in a corrected ECC error (lowest bit not assigned here). **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.36 ECCCSYN0

- **Name:** ECC Corrected Syndrome Register 0
- **Description:** ECC Corrected Error Data Syndrome Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1161c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-251 Fields for Register: ECCCSYN0

Bits	Name	Memory Access	Description
31:0	ecc_corr_syndromes_31_0	R	Data pattern that resulted in a correctable error. For 16-bit DRAM data width, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.37 ECCCSYN1

- **Name:** ECC Corrected Syndrome Register 1
- **Description:** ECC Corrected Error Data Syndrome Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11620
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_32__OR__MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-252 Fields for Register: ECCCSYN1

Bits	Name	Memory Access	Description
31:0	ecc_corr_syndromes_63_32	R	Data pattern that resulted in a correctable error. For 32-bit and 16-bit DRAM Data width operating in single-beat SECDED or ADVECC mode, this register is not used. However, for multi-beat SECDED ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.38 ECCCSYN2

- **Name:** ECC Corrected Syndrome Register 2
- **Description:** ECC Corrected Error ECC Syndrome Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11624
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-253 Fields for Register: ECCCSYN2

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	cb_corr_syndrome	R	Indicates the Checkbit corrected error syndrome that resulted in SECDED ECC error. It is computed by XOR operation of incoming checkbits and computed checkbits of the incoming data bits. It indicates which bit is in error, or whether multiple bits are in Error. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8			**Reserved Field:** Yes

Table 3-253 Fields for Register: ECCCSYN2 (continued)

Bits	Name	Memory Access	Description
7:0	ecc_corr_syndromes_71_64	R	Indicates the data pattern that resulted in a correctable error. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, it represents the combined ECC byte spread over two DRAM beats for multibeat SECDED ECC, while for ADVECC, the upper nibble shall be ignored by the user. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. This field will be cleared when ecc_corrected_err_clr is set. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.39 ECCBITMASK0

- **Name:** ECC Corrected Data Bit Mask Register 0
- **Description:** ECC Corrected Data Bit Mask Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11628
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

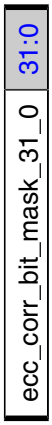


Table 3-254 Fields for Register: ECCBITMASK0

Bits	Name	Memory Access	Description
31:0	ecc_corr_bit_mask_31_0	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 16-bit DRAM data width, only bits [15:0] are used **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.40 ECCBITMASK1

- **Name:** ECC Corrected Data Bit Mask Register 1
- **Description:** ECC Corrected Data Bit Mask Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1162c
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH1.

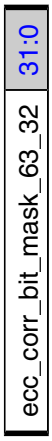


Table 3-255 Fields for Register: ECCBITMASK1

Bits	Name	Memory Access	Description
31:0	ecc_corr_bit_mask_63_32	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 32-bit DRAM data width and 16-bit DRAM data width operating in sideband SECDED or ADVECC mode, this register is not used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.41 ECCBITMASK2

- **Name:** ECC Corrected Data Bit Mask Register 2
- **Description:** ECC Corrected Data Bit Mask Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11630
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

Table 3-256 Fields for Register: ECCBITMASK2

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7:0	ecc_corr_bit_mask_71_64	R	Mask for the corrected data portion ■ 1 on any bit indicates that the bit has been corrected by the ECC logic ■ 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, even within the DFI cycle, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, the upper nibble shall be ignored by the user. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.42 ECCUADDR0

- **Name:** ECC Uncorrected Error Address Register 0
- **Description:** ECC Uncorrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11634
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

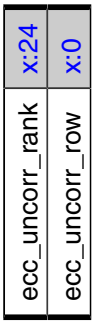


Table 3-257 Fields for Register: ECCUADDR0

Bits	Name	Memory Access	Description
x:24	ecc_uncorr_rank	R	Rank number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	ecc_uncorr_row	R	Page/row number of a read resulting in an uncorrected ECC error. This is 18-bits wide in configurations with LPDDR5 or DDR4 support and 16-bits in all other configurations. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.3.43 ECCUADDR1

- **Name:** ECC Uncorrected Error Address Register 1
- **Description:** ECC Uncorrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11638
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.

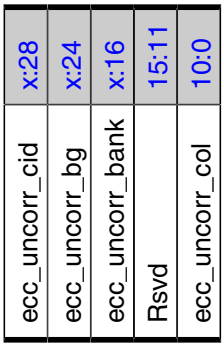


Table 3-258 Fields for Register: ECCUADDR1

Bits	Name	Memory Access	Description
x:28	ecc_uncorr_cid	R	CID number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "UMCTL2_CID_WIDTH" + 27
x:24	ecc_uncorr_bg	R	Bank Group number of a read resulting in an uncorrected ECC error. Note that when LPDDR5 16B mode is in use, this field is used as the upper bits of the bank address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	ecc_uncorr_bank	R	Bank number of a read resulting in an uncorrected ECC error. Note that when LPDDR5 16B mode is in use, {ECCUADDR1.ecc_uncorr_bg, ECCUADDR1.ecc_uncorr_bank[1:0]} shows bank number of a read resulting in an uncorrected ECC error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-258 Fields for Register: ECCUADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	ecc_uncorr_col	R	Block number of a read resulting in an uncorrected ECC error (lowest bit not assigned here) **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.44 ECCUSYN0

- **Name:** ECC Uncorrected Syndrome Register 0
- **Description:** ECC Uncorrected Error Data Syndrome Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x1163c
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-259 Fields for Register: ECCUSYN0

Bits	Name	Memory Access	Description
31:0	ecc_uncorr_syndromes_31_0	R	Data pattern that resulted in an uncorrectable error. For 16-bit DRAM data width, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.45 ECCUSYN1

- **Name:** ECC Uncorrected Syndrome Register 1
- **Description:** ECC Uncorrected Error Data Syndrome Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11640
- **Exists:** MEMC_ECC_SUPPORT>0 && (MEMC_DRAM_DATA_WIDTH_64_OR_32__OR__MEMC_INLINE_ECC==1)

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-260 Fields for Register: ECCUSYN1

Bits	Name	Memory Access	Description
31:0	ecc_uncorr_syndromes_63_32	R	Data pattern that resulted in an uncorrected error. For 32-bit DRAM data width and 16-bit DRAM data width operating in single-beat SECDED or ADVECC mode, this register is not used. However, for multi-beat SECDED ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.46 ECCUSYN2

- **Name:** ECC Uncorrected Syndrome Register 2
- **Description:** ECC Uncorrected Error ECC Syndrome Register 2
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11644
- **Exists:** MEMC_ECC_SUPPORT>0

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-261 Fields for Register: ECCUSYN2

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:16	cb_uncorr_syndrome	R	Indicates the Checkbit uncorrected error syndrome that resulted in SECDED ECC error. It is computed by XOR operation of incoming checkbits and computed checkbits of the incoming data bits. It indicates which bit is in error, or whether multiple bits are in Error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:8			**Reserved Field:** Yes

Table 3-261 Fields for Register: ECCUSYN2 (continued)

Bits	Name	Memory Access	Description
7:0	ecc_uncorr_syndromes_71_64	R	Data pattern that resulted in an uncorrectable error. This register refers to the ECC byte, which is bits [71:64] for 64-bit DRAM data width, [39:32] for 32-bit DRAM data width, or [23:16] for 16-bit DRAM data width. However, for DDR5 36b/ch devices, it represents the combined ECC byte spread over two DRAM beats for multibeat SECDED ECC, while for ADVECC, the upper nibble shall be ignored by the user. It is indirect register while operating in ADVECC mode which shall be selected by ADVECCINDEX.ecc_syndrome_sel. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.47 ECCAPSTAT

- **Name:** Address protection within ECC Status Register
- **Description:** Address protection within ECC Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11664
- **Exists:** MEMC_ECCAP==1

This register is in block REGB_DDRC_CH1.

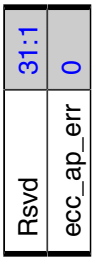


Table 3-262 Fields for Register: ECCAPSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	ecc_ap_err	R	Indicates the number of ECC errors (correctable/uncorrectable) within one burst exceeded the threshold.(ECCCFG0.ecc_ap_err_threshold) **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.48 OCPARCFG0

- **Name:** On-Chip Parity Configuration Register 0
- **Description:** On-Chip Parity Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11680
- **Exists:** UMCTL2_OCPAR_OR_OCECC_EN_1==1

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

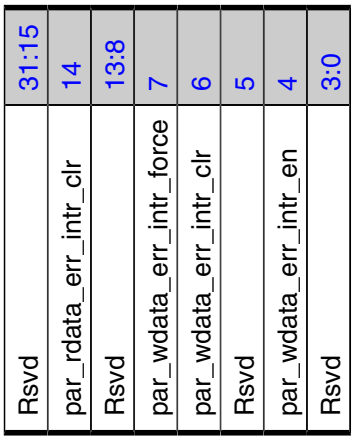


Table 3-263 Fields for Register: OCPARCFG0

Bits	Name	Memory Access	Description
31:15			**Reserved Field:** Yes
14	par_rdata_err_intr_clr	R/W1C	Interrupt clear bit for par_rdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13:8			**Reserved Field:** Yes
7	par_wdata_err_intr_force	R/W1C	Interrupt force bit for par_wdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-263 Fields for Register: OCPARCFG0 (continued)

Bits	Name	Memory Access	Description
6	par_wdata_err_intr_clr	R/W1C	Interrupt clear bit for par_wdata_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5			**Reserved Field:** Yes
4	par_wdata_err_intr_en	R/W	Enables write data interrupt generation (par_wdata_err_intr) upon detection of parity error at the AXI or DFI interface. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Dynamic
3:0			**Reserved Field:** Yes

3.3.49 OCPARSTAT2

- **Name:** On-Chip Parity Status Register 2
- **Description:** On-Chip Parity Status Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11690
- **Exists:** UMCTL2_OCPAR_EN_1==1

This register is in block REGB_DDRC_CH1.

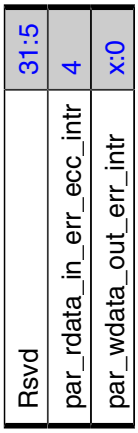


Table 3-264 Fields for Register: OCPARSTAT2

Bits	Name	Memory Access	Description
31:5			**Reserved Field:** Yes
4	par_rdata_in_err_ecc_intr	R	Interrupt on ECC data going into inline ECC decoder. Cleared by par_rdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
x:0	par_wdata_out_err_intr	R	Write data parity error interrupt on output. Cleared by register par_wdata_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_OCPAR_WDATA_OUT_ERR_WIDTH" - 1

3.3.50 OCCAPCFG1

- **Name:** On-Chip command/Address Protection Configuration Register 1
- **Description:** On-Chip command/Address Protection Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11788
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

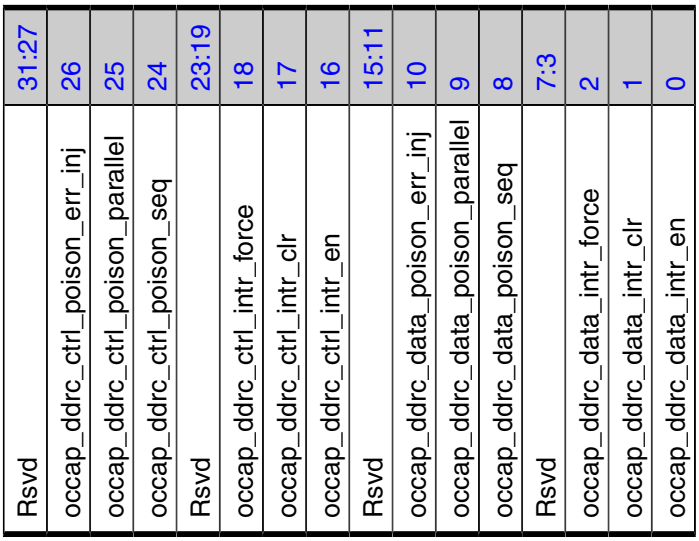


Table 3-265 Fields for Register: OCCAPCFG1

Bits	Name	Memory Access	Description
31:27			**Reserved Field:** Yes
26	occap_ddrc_ctrl_poison_err_inj	R/W	Enable error injection in the poisoning of OCCAP DDRC CTRL logic Injects error into poisoning logic (either parallel or seq) such that XOR logic for one signal is not poisoned when expected. If set, it allows ability to corrupt the following register fields. ■ 1'b0: OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel/seq_err=0 ■ 1'b1: OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel/seq_err=1 Do not change value in same APB write as setting of occap_ddrc_ctrl_poison_parallel/_seq **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-265 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
25	occap_ddrc_ctrl_poison_parallel	R/W1C	Enables poisoning of OCCAP DDRC CTRL logic for all parts of comparison logic, in parallel. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting a ddrc_ctrl[0]'s signal to XOR logic. ddrc_ctrl[1] related signals are never poisoned. All signals are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_ctrl_poison_parallel_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
24	occap_ddrc_ctrl_poison_seq	R/W1C	Enables poisoning of OCCAP DDRC CTRL logic for all parts of comparison logic, in sequence. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting a ddrc_ctrl[0]'s signal to XOR logic. ddrc_ctrl[1] related signals are never poisoned. Each signal from ddrc_ctrl[0] is poisoned in series and checks in turn, that each signal was poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_ctrl_poison_seq_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23:19			**Reserved Field:** Yes
18	occap_ddrc_ctrl_intr_force	R/W1C	Interrupt force bit for occap_ddrc_ctrl_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	occap_ddrc_ctrl_intr_clr	R/W1C	Interrupt clear bit for occap_ddrc_ctrl_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-265 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
16	occap_ddrc_ctrl_intr_en	R/W	Enables interrupt generation on signal occap_ddrc_ctrl_err_intr upon detection of OCCAP DDRC CTRL errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
15:11			**Reserved Field:** Yes
10	occap_ddrc_data_poison_err_inj	R/W	Enable error injection in the poisoning of OCCAP DDRC DATA logic Injects error into poisoning logic (either parallel or seq) such that XOR logic for one signal is not poisoned when expected. If set, it allows ability to corrupt the following register fields. ■ 1'b0: OCCAPSTAT1.occap_ddrc_data_poison_parallel/seq_err=0 ■ 1'b1: OCCAPSTAT1.occap_ddrc_data_poison_parallel/seq_err=1 Do not change value in same APB write as setting of occap_ddrc_data_poison_parallel/_seq **Value After Reset:** 0x0 **Programming Mode:** Dynamic
9	occap_ddrc_data_poison_parallel	R/W1C	Enables poisoning of OCCAP DDRC DATA logic for all parts of comparison logic, in parallel. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting all bits of a signal to XOR logic. All signals of instance[0] of the duplicated modules are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_data_poison_parallel_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-265 Fields for Register: OCCAPCFG1 (continued)

Bits	Name	Memory Access	Description
8	occap_ddrc_data_poison_seq	R/W1C	Enables poisoning of OCCAP DDRC DATA logic for all parts of comparison logic, in sequence. Poisons comparison logic for one core_ddrc_core_clk cycle by inverting all bits of a signal to XOR logic. All signals of instance[0] of the duplicated modules are poisoned in parallel and checks if all signals were poisoned correctly. If this is not the case, this is flagged by OCCAPSTAT1.occap_ddrc_data_poison_seq_err=1. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7:3			**Reserved Field:** Yes
2	occap_ddrc_data_intr_force	R/W1C	Interrupt force bit for occap_ddrc_data_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	occap_ddrc_data_intr_clr	R/W1C	Interrupt clear bit for occap_ddrc_data_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	occap_ddrc_data_intr_en	R/W	Enables interrupt generation on signal occap_ddrc_data_err_intr upon detection of OCCAP DDRC DATA errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.51 OCCAPSTAT1

- **Name:** On-Chip command/Address Protection Status Register 1
- **Description:** On-Chip command/Address Protection Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1178c
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH1.

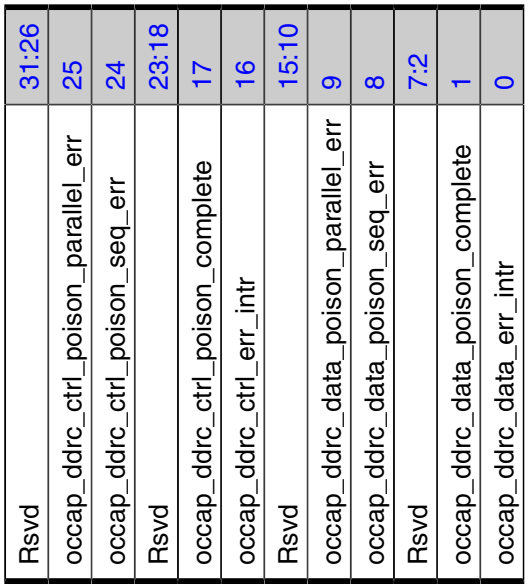


Table 3-266 Fields for Register: OCCAPSTAT1

Bits	Name	Memory Access	Description
31:26			**Reserved Field:** Yes
25	occap_ddrc_ctrl_poison_parallel_err	R	Error when occap_ddrc_ctrl_poison_parallel was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_ctrl_poison_parallel. It checks for error on all of the the corresponding XOR outputs. If multi-bit, checks also that all XOR bits are set. It checks all XOR in parallel. Register is valid only when occap_ddrc_ctrl_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-266 Fields for Register: OCCAPSTAT1 (continued)

Bits	Name	Memory Access	Description
24	occap_ddrc_ctrl_poison_seq_err	R	Error when occap_ddrc_ctrl_poison_seq was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_ctrl_poison_seq. It checks for error on all of the corresponding XOR outputs. It checks each XOR sequentially. Register is valid only when occap_ddrc_ctrl_cmp_poison_complete=1. **Value After Reset:** 0x0 **Programming Mode:** Static
23:18			**Reserved Field:** Yes
17	occap_ddrc_ctrl_poison_complete	R	OCCAP DDRC CTRL poisoning complete interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_ctrl_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
16	occap_ddrc_ctrl_err_intr	R	OCCAP DDRC CTRL error interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_ctrl_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
15:10			**Reserved Field:** Yes
9	occap_ddrc_data_poison_parallel_err	R	Error when occap_ddrc_data_poison_parallel was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_data_poison_parallel. It checks for error on all of the the corresponding XOR outputs. If multi-bit, checks also that all XOR bits are set. It checks all XOR in parallel. This is cleared when OCCAPCFG1.occap_ddrc_data_poison_parallel=0 occurs. **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-266 Fields for Register: OCCAPSTAT1 (continued)

Bits	Name	Memory Access	Description
8	occap_ddrc_data_poison_seq_err	R	Error when occap_ddrc_data_poison_seq was active due to incorrect no. of errors being occurring. Internal logic checks the number of errors detected while poisoning occurred for occap_ddrc_data_poison_seq. It checks for error on all of the corresponding XOR outputs. It checks each XOR sequentially. This is cleared when OCCAPCFG1.occap_ddrc_data_poison_seq=0 occurs. **Value After Reset:** 0x0 **Programming Mode:** Static
7:2			**Reserved Field:** Yes
1	occap_ddrc_data_poison_complete	R	OCCAP DDRC DATA poisoning complete interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_data_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static
0	occap_ddrc_data_err_intr	R	OCCAP DDRC DATA error interrupt status. Register cleared by OCCAPCFG1.occap_ddrc_data_err_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.52 OCCAPCFG2

- **Name:** On-Chip command/Address Protection Configuration Register 2
- **Description:** On-Chip command/Address Protection Configuration Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11790
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH1.

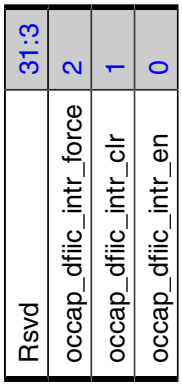


Table 3-267 Fields for Register: OCCAPCFG2

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	occap_dfiic_intr_force	R/W1C	Interrupt force bit for occap_dfiic_err_intr, setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	occap_dfiic_intr_clr	R/W1C	Interrupt clear bit for occap_dfiic_err_intr. DDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	occap_dfiic_intr_en	R/W	Enables interrupt generation on signal occap_dfiic_err_intr upon detection of OCCAP DFI interconnect errors. **Value After Reset:** 0x1 **Programming Mode:** Dynamic

3.3.53 OCCAPSTAT2

- **Name:** On-Chip command/Address Protection Status Register 2
- **Description:** On-Chip command/Address Protection Status Register 2
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11794
- **Exists:** UMCTL2_OCCAP_EN_1==1

This register is in block REGB_DDRC_CH1.

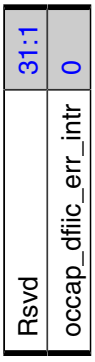


Table 3-268 Fields for Register: OCCAPSTAT2

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	occap_dfiic_err_intr	R	OCCAP DFI interconnect error interrupt status. Register cleared by OCCAPCFG2.occap_dfiic_intr_clr. **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.54 LNKECCCTL1

- **Name:** Link-ECC Control Register 1
- **Description:** Link-ECC Control Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11984
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.
Note: Do not perform any APB access to LNKECCCTL1 within 32 pclk cycles of previous access to LNKECCCTL1, as this might lead to data loss.

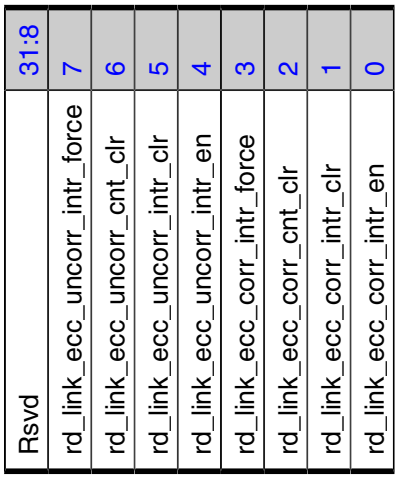


Table 3-269 Fields for Register: LNKECCCTL1

Bits	Name	Memory Access	Description
31:8			**Reserved Field:** Yes
7	rd_link_ecc_uncorr_intr_force	R/W1C	Interrupt force bit for rd_linkecc_uncorr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
6	rd_link_ecc_uncorr_cnt_clr	R/W1C	Clear all Read Link-ECC uncorrectable error count. If this bit set,LNKECCERRCNT0.rd_link_ecc_uncorr_cnt will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-269 Fields for Register: LNKECCCTL1 (continued)

Bits	Name	Memory Access	Description
5	rd_link_ecc_uncorr_intr_clr	R/W1C	Clear Read Link-ECC uncorrectable error interrupt. If this bit set, rd_linkecc_uncorr_err_intr will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rd_link_ecc_uncorr_intr_en	R/W	Interrupt enable bit for Read Link-ECC uncorrectable error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3	rd_link_ecc_corr_intr_force	R/W1C	Interrupt force bit for rd_linkecc_corr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rd_link_ecc_corr_cnt_clr	R/W1C	Clear all Read Link-ECC correctable error count. If this bit set,LNKECCERRCNT0.rd_link_ecc_corr_cnt will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rd_link_ecc_corr_intr_clr	R/W1C	Clear Read Link-ECC correctable error interrupt. If this bit set, rd_linkecc_corr_err_intr will be cleared. LPDDRCTL automatically clears this bit. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
0	rd_link_ecc_corr_intr_en	R/W	Interrupt enable bit for Read Link-ECC correctable error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.55 LNKECCPOISONCTL0

- **Name:** Link-ECC Poison Control Register 0
- **Description:** Link-ECC Poison Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11988
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

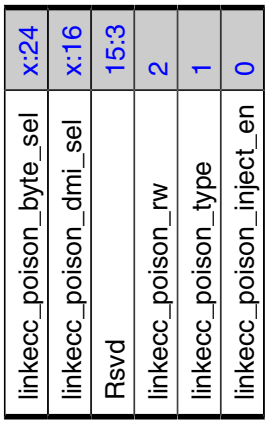


Table 3-270 Fields for Register: LNKECCPOISONCTL0

Bits	Name	Memory Access	Description
x:24	linkecc_poison_byte_sel	R/W	Select target byte(s) of Data for Read/Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to Data[N*8+:8]. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/8" + 23
x:16	linkecc_poison_dmi_sel	R/W	Select target DMI(s) of Data for Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to DMI[N]. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_DRAM_TOTAL_DATA_WIDTH/8" + 15
15:3			**Reserved Field:** Yes

Table 3-270 Fields for Register: LNKECCPOISONCTL0 (continued)

Bits	Name	Memory Access	Description
2	linkecc_poison_rw	R/W	Indicates whether the Link-ECC poisoning operation is Read or Write. ■ 0 - Write ■ 1 - Read **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	linkecc_poison_type	R/W	Indicates whether the Link-ECC poisoning operation is Single-bit error or Double bit error. ■ 0 - Single bit Error ■ 1 - Double bit Error **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	linkecc_poison_inject_en	R/W	Setting this register bit to 1 triggers the Link-ECC poisoning. Once Link-ECC is poisoned to a ECC code, the ECC poisoning is completed automatically and LNKECCPOISONSTAT.linkecc_poison_complete becomes 1. Please make sure that LNKECCPOISONSTAT.linkecc_poison_complete==0 before writing this register to 1. Note: Link ECC feature must be enabled (LNKECCCTL0.wr_link_ecc_enable for Write Link ECC and LNKECCCTL0.rd_link_ecc_enable for Read Link ECC) when Link ECC poisoning feature is used. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.56 LNKECCPOISONSTAT

- **Name:** Link-ECC Poison Status Register
- **Description:** Link-ECC Poison Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x1198c
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

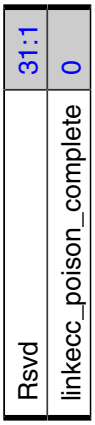


Table 3-271 Fields for Register: LNKECCPOISONSTAT

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	linkecc_poison_complete	R	Indicates Link-ECC poisoning operation is done. ■ 0 - Link-ECC poisoning is not completed ■ 1 - Link-ECC poisoning is completed **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.57 LNKECCINDEX

- **Name:** Link-ECC Index Register
- **Description:** Link-ECC Index Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11990
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

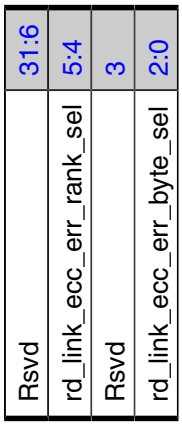


Table 3-272 Fields for Register: LNKECCINDEX

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:4	rd_link_ecc_err_rank_sel	R/W	Select of which rank status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_NUM_RANKS. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1
3			**Reserved Field:** Yes
2:0	rd_link_ecc_err_byte_sel	R/W	Select of which data byte status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_DRAM_DATA_WIDTH/8. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1

3.3.58 LNKECCERRCNT0

- **Name:** Link-ECC Error Status Register 0
- **Description:** Link-ECC Error Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11994
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

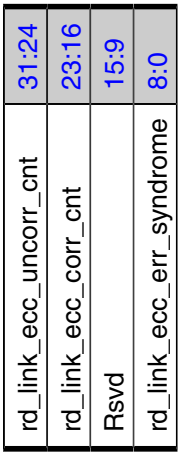


Table 3-273 Fields for Register: LNKECCERRCNT0

Bits	Name	Memory Access	Description
31:24	rd_link_ecc_uncorr_cnt	R	Indicates double bit error count. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23:16	rd_link_ecc_corr_cnt	R	Indicates single bit error count. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:9			**Reserved Field:** Yes
8:0	rd_link_ecc_err_syndrome	R	Indicates ECC syndrome from most recent single bit error. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.59 LNKECCERRSTAT

- **Name:** Link-ECC Error Status Register 1
- **Description:** Link-ECC Error Status Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x11998
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

31:12	11:8	7:4	3:0
Rsvd	rd_link_ecc_uncorr_err_int	Rsvd	rd_link_ecc_corr_err_int

Table 3-274 Fields for Register: LNKECCERRSTAT

Bits	Name	Memory Access	Description
31:12			**Reserved Field:** Yes
11:8	rd_link_ecc_uncorr_err_int	R	Indicates double bit error for Read Link-ECC. If double bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_uncorr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) **Value After Reset:** 0x0 **Programming Mode:** Static
7:4			**Reserved Field:** Yes
3:0	rd_link_ecc_corr_err_int	R	Indicates single bit error for Read Link-ECC. If signle bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_corr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) **Value After Reset:** 0x0 **Programming Mode:** Static

3.3.60 LNKECCCADDR0

- **Name:** Link ECC Corrected Error Address Register 0
- **Description:** Link ECC Corrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x119e0
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

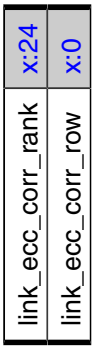


Table 3-275 Fields for Register: LNKECCCADDR0

Bits	Name	Memory Access	Description
x:24	link_ecc_corr_rank	R	Indicates the rank number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	link_ecc_corr_row	R	Indicates the page/row number of a read resulting in a corrected Read Link ECC error. This is 18-bits wide in configurations with LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.3.61 LNKECCCADDR1

- **Name:** Link ECC Corrected Error Address Register 1
- **Description:** Link ECC Corrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x119e4
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

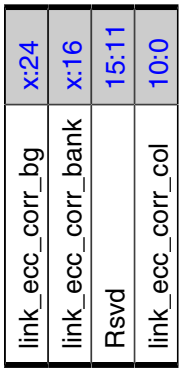


Table 3-276 Fields for Register: LNKECCCADDR1

Bits	Name	Memory Access	Description
x:24	link_ecc_corr_bg	R	Bank Group number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	link_ecc_corr_bank	R	Bank number of a read resulting in a corrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-276 Fields for Register: LNKECCCADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	link_ecc_corr_col	R	Block number of a read resulting in a corrected Read Link ECC error. The error address identifies that Link ECC error happens in any data beat of Read data and any data-lane, therefore the lowest 4-bits is always 4'b0000. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

3.3.62 LNKECCUADDR0

- **Name:** Link ECC Uncorrected Error Address Register 0
- **Description:** Link ECC Uncorrected Error Address Register 0
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x119e8
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

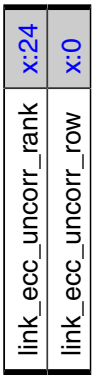


Table 3-277 Fields for Register: LNKECCUADDR0

Bits	Name	Memory Access	Description
x:24	link_ecc_uncorr_rank	R	Rank number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RANK_BITS" + 23
x:0	link_ecc_uncorr_row	R	Page/row number of a read resulting in an uncorrected Read Link ECC error. This is 18-bits wide in configurations with LPDDR5. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_PAGE_BITS" - 1

3.3.63 LNKECCUADDR1

- **Name:** Link ECC Uncorrected Error Address Register 1
- **Description:** Link ECC Uncorrected Error Address Register 1
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x119ec
- **Exists:** MEMC_LINK_ECC==1

This register is in block REGB_DDRC_CH1.

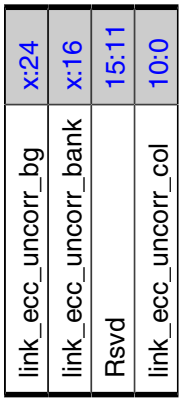


Table 3-278 Fields for Register: LNKECCUADDR1

Bits	Name	Memory Access	Description
x:24	link_ecc_uncorr_bg	R	Bank Group number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BG_BITS" + 23
x:16	link_ecc_uncorr_bank	R	Bank number of a read resulting in an uncorrected Read Link ECC error. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_BANK_BITS" + 15
15:11			**Reserved Field:** Yes

Table 3-278 Fields for Register: LNKECCUADDR1 (continued)

Bits	Name	Memory Access	Description
10:0	link_ecc_uncorr_col	R	Block number of a read resulting in an uncorrected Read Link ECC error. The error address identifies that Link ECC error happens in any data beat of Read data and any data-lane, therefore the lowest 4-bits is always 4'b0000. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

3.3.64 OPCTRL1

- **Name:** Operation Control Register 1
- **Description:** Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b84
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

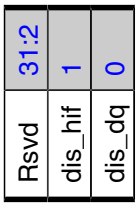


Table 3-279 Fields for Register: OPCTRL1

Bits	Name	Memory Access	Description
31:2			**Reserved Field:** Yes
1	dis_hif	R/W	When 1, DDRCTL asserts the HIF command signal hif_cmd_stall. DDRCTL will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	dis_dq	R/W	When 1, DDRCTL will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the DDRCTL, which makes it safe to modify certain register fields associated with reads and writes (see Programming Chapter for details). After setting this bit, it is strongly recommended to poll OPCTRLCAM.wr_data_pipeline_empty and OPCTRLCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Note: This bit is not applicable for designs working in DDR5 mode. In DDR5 mode, use software command interface command DisDqRef to achieve the same function as this bit. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.65 OPCTRLCAM

- **Name:** CAM Operation Control Register
- **Description:** CAM Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b88
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

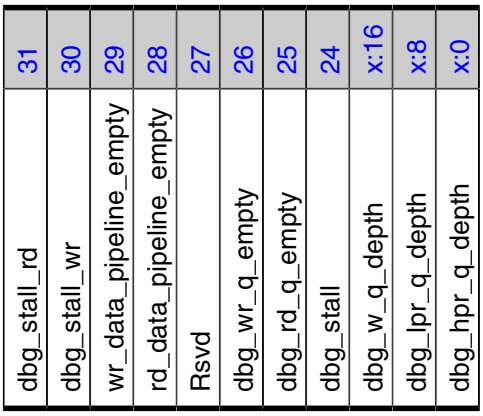


Table 3-280 Fields for Register: OPCTRLCAM

Bits	Name	Memory Access	Description
31	dbg_stall_rd	R	Stall for Read channel FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30	dbg_stall_wr	R	Stall for Write channel FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	wr_data_pipeline_empty	R	This bit indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic

Table 3-280 Fields for Register: OPCTRLCAM (continued)

Bits	Name	Memory Access	Description
28	rd_data_pipeline_empty	R	This bit indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
27			**Reserved Field:** Yes
26	dbg_wr_q_empty	R	When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
25	dbg_rd_q_empty	R	When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. **Value After Reset:** 0x0 **Reset Mask:** 0x0 **Volatile:** true **Programming Mode:** Dynamic
24	dbg_stall	R	Stall FOR DEBUG ONLY **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-280 Fields for Register: OPCTRLCAM (continued)

Bits	Name	Memory Access	Description
x:16	dbg_w_q_depth	R	Write queue depth For HW configurations which have more than 128 deep write CAM, use OPCTRLWRCAM.dbg_w_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS + 1" + 15
x:8	dbg_lpr_q_depth	R	Low priority read queue depth For HW configurations which have more than 128 deep read CAM, use OPCTRLRDCAM.dbg_lpr_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS + 1" + 7
x:0	dbg_hpr_q_depth	R	High priority read queue depth For HW configurations which have more than 128 deep read CAM, use OPCTRLRDCAM.dbg_hpr_q_depth_extend instead. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_RDCMD_ENTRY_BITS + 1" - 1

3.3.66 OPCTRLCMD

- **Name:** Command Operation Control Register
- **Description:** Command Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b8c
- **Exists:** DDRCTL_DDR4_OR_LPDDR__OR__UMCTL2_REF_ZQ_IO==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

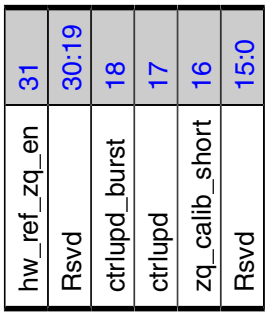


Table 3-281 Fields for Register: OPCTRLCMD

Bits	Name	Memory Access	Description
31	hw_ref_zq_en	R/W	Setting this register bit to 1 allows refresh and ZQCS/MPC(ZQ Calibration) commands to be triggered from hardware via the IOs ext_*. If set to 1, the fields OPCTRLCMD.zq_calib_short and OPREFCTRL*.rank*_refresh have no function, and are ignored by the DDRCTL logic. Setting this register bit to 0 allows refresh and ZQCS/MPC(ZQ Calibration) to be triggered from software, via the fields OPCTRLCMD.zq_calib_short and OPREFCTRL*.rank*_refresh. If set to 0, the hardware pins ext_* have no function, and are ignored by the DDRCTL logic. This register is static, and may only be changed when the DDRC reset signal, core_ddrc_rstn, is asserted (0). Note: Supporting this register field in this release is limited. Contact Synopsys if you wish to use this. Note: This field is not applicable for DDR5 ZQ Calibration. **Value After Reset:** 0x0 **Programming Mode:** Static
30:19			**Reserved Field:** Yes

Table 3-281 Fields for Register: OPCTRLCMD (continued)

Bits	Name	Memory Access	Description
18	ctrlupd_burst	R/W	While this register bit is 1, the DDRCTL issues burst DFI control update to the PHY to change core VDD. When this register bit is changed to 0 from 1, burst DFI control update will be stopped, but one DFI control update request is issued which is in progress. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Note: This field is not applicable for DDR54. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	ctrlupd	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	zq_calib_short	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init, in Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) or Deep Sleep Mode or Maximum Power Saving Mode. For Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) it will be scheduled after SR(except LPDDR4/5) or SRPD(LPDDR4/5) has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. For Maximum Power Saving Mode, it will not be scheduled, although OPCTRLSTAT.zq_calib_short_busy will be de-asserted. Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
15:0			**Reserved Field:** Yes

3.3.67 OPCTRLSTAT

- **Name:** Status Operation Control Register
- **Description:** Status Operation Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b90
- **Exists:** DDRCTL_DDR4_OR_LPDDR==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

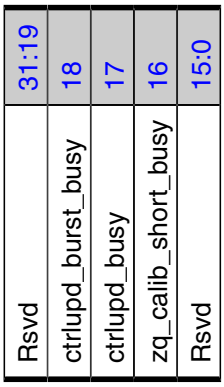


Table 3-282 Fields for Register: OPCTRLSTAT

Bits	Name	Memory Access	Description
31:19			**Reserved Field:** Yes
18	ctrlupd_burst_busy	R	SoC core may initiate a burst DFI control update operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the burst control update request. It goes low when the burst control update operation is finished in the DDRCTL. It is recommended not to perform burst ctrlupd operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a burst DFI ctrol update operation ■ 1 - Indicates that burst control update operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-282 Fields for Register: OPCTRLSTAT (continued)

Bits	Name	Memory Access	Description
17	ctrlupd_busy	R	SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the DDRCTL. It is recommended not to perform ctrlupd operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ctrlupd operation ■ 1 - Indicates that ctrlupd operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	zq_calib_short_busy	R	SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the DDRCTL. It is recommended not to perform ZQCS operations when this signal is high. ■ 0 - Indicates that the SoC core can initiate a ZQCS operation ■ 1 - Indicates that ZQCS operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:0			**Reserved Field:** Yes

3.3.68 OPCTRLCAM1

- **Name:** CAM Operation Control Register 1
- **Description:** CAM Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b94
- **Exists:** MEMC_INLINE_ECC==1

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-283 Fields for Register: OPCTRLCAM1

Bits	Name	Memory Access	Description
x:0	dbg_wrecc_q_depth	R	Write ECC queue depth **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_WRCMD_ENTRY_BITS + 1" - 1

3.3.69 OPREFCTRL0

- **Name:** Refresh Operation Control Register 0
- **Description:** Refresh Operation Control Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b98
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank31_refresh	rank30_refresh	rank29_refresh	rank28_refresh	rank27_refresh	rank26_refresh	rank25_refresh	rank24_refresh	rank23_refresh	rank22_refresh	rank21_refresh	rank20_refresh	rank19_refresh	rank18_refresh	rank17_refresh	rank16_refresh	rank15_refresh	rank14_refresh	rank13_refresh	rank12_refresh	rank11_refresh	rank10_refresh	rank9_refresh	rank8_refresh	rank7_refresh	rank6_refresh	rank5_refresh	rank4_refresh	rank3_refresh	rank2_refresh	rank1_refresh	rank0_refresh

Table 3-284 Fields for Register: OPREFCTRL0

Bits	Name	Memory Access	Description
31	rank31_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 31. Writing to this bit causes OPREFSTAT0.rank31_refresh_busy to be set. When OPREFSTAT0.rank31_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 31. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
30	rank30_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 30. Writing to this bit causes OPREFSTAT0.rank30_refresh_busy to be set. When OPREFSTAT0.rank30_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 30. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
29	rank29_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 29. Writing to this bit causes OPREFSTAT0.rank29_refresh_busy to be set. When OPREFSTAT0.rank29_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 29. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
28	rank28_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 28. Writing to this bit causes OPREFSTAT0.rank28_refresh_busy to be set. When OPREFSTAT0.rank28_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 28. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
27	rank27_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 27. Writing to this bit causes OPREFSTAT0.rank27_refresh_busy to be set. When OPREFSTAT0.rank27_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 27. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
26	rank26_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 26. Writing to this bit causes OPREFSTAT0.rank26_refresh_busy to be set. When OPREFSTAT0.rank26_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 26. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
25	rank25_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 25. Writing to this bit causes OPREFSTAT0.rank25_refresh_busy to be set. When OPREFSTAT0.rank25_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 25. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
24	rank24_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 24. Writing to this bit causes OPREFSTAT0.rank24_refresh_busy to be set. When OPREFSTAT0.rank24_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 24. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23	rank23_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 23. Writing to this bit causes OPREFSTAT0.rank23_refresh_busy to be set. When OPREFSTAT0.rank23_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 23. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
22	rank22_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 22. Writing to this bit causes OPREFSTAT0.rank22_refresh_busy to be set. When OPREFSTAT0.rank22_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 22. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
21	rank21_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 21. Writing to this bit causes OPREFSTAT0.rank21_refresh_busy to be set. When OPREFSTAT0.rank21_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 21. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
20	rank20_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 20. Writing to this bit causes OPREFSTAT0.rank20_refresh_busy to be set. When OPREFSTAT0.rank20_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 20. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
19	rank19_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 19. Writing to this bit causes OPREFSTAT0.rank19_refresh_busy to be set. When OPREFSTAT0.rank19_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 19. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
18	rank18_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 18. Writing to this bit causes OPREFSTAT0.rank18_refresh_busy to be set. When OPREFSTAT0.rank18_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 18. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	rank17_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 17. Writing to this bit causes OPREFSTAT0.rank17_refresh_busy to be set. When OPREFSTAT0.rank17_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 17. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	rank16_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 16. Writing to this bit causes OPREFSTAT0.rank16_refresh_busy to be set. When OPREFSTAT0.rank16_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 16. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
15	rank15_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 15. Writing to this bit causes OPREFSTAT0.rank15_refresh_busy to be set. When OPREFSTAT0.rank15_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 15. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
14	rank14_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 14. Writing to this bit causes OPREFSTAT0.rank14_refresh_busy to be set. When OPREFSTAT0.rank14_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 14. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13	rank13_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 13. Writing to this bit causes OPREFSTAT0.rank13_refresh_busy to be set. When OPREFSTAT0.rank13_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 13. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
12	rank12_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 12. Writing to this bit causes OPREFSTAT0.rank12_refresh_busy to be set. When OPREFSTAT0.rank12_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 12. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
11	rank11_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 11. Writing to this bit causes OPREFSTAT0.rank11_refresh_busy to be set. When OPREFSTAT0.rank11_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 11. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
10	rank10_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 10. Writing to this bit causes OPREFSTAT0.rank10_refresh_busy to be set. When OPREFSTAT0.rank10_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 10. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
9	rank9_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 9. Writing to this bit causes OPREFSTAT0.rank9_refresh_busy to be set. When OPREFSTAT0.rank9_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 9. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
8	rank8_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 8. Writing to this bit causes OPREFSTAT0.rank8_refresh_busy to be set. When OPREFSTAT0.rank8_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 8. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7	rank7_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 7. Writing to this bit causes OPREFSTAT0.rank7_refresh_busy to be set. When OPREFSTAT0.rank7_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 7. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
6	rank6_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 6. Writing to this bit causes OPREFSTAT0.rank6_refresh_busy to be set. When OPREFSTAT0.rank6_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 6. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5	rank5_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 5. Writing to this bit causes OPREFSTAT0.rank5_refresh_busy to be set. When OPREFSTAT0.rank5_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 5. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rank4_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 4. Writing to this bit causes OPREFSTAT0.rank4_refresh_busy to be set. When OPREFSTAT0.rank4_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 4. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
3	rank3_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 3. Writing to this bit causes OPREFSTAT0.rank3_refresh_busy to be set. When OPREFSTAT0.rank3_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 3. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rank2_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 2. Writing to this bit causes OPREFSTAT0.rank2_refresh_busy to be set. When OPREFSTAT0.rank2_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 2. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rank1_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 1. Writing to this bit causes OPREFSTAT0.rank1_refresh_busy to be set. When OPREFSTAT0.rank1_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 1. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-284 Fields for Register: OPREFCTRL0 (continued)

Bits	Name	Memory Access	Description
0	rank0_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 0. Writing to this bit causes OPREFSTAT0.rank0_refresh_busy to be set. When OPREFSTAT0.rank0_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 0. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.3.70 OPREFCTRL1

- **Name:** Refresh Operation Control Register 1
- **Description:** Refresh Operation Control Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11b9c
- **Exists:** UMCTL2_NUM_LRANKS_TOTAL>32

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank63_refresh	rank62_refresh	rank61_refresh	rank60_refresh	rank59_refresh	rank58_refresh	rank57_refresh	rank56_refresh	rank55_refresh	rank54_refresh	rank53_refresh	rank52_refresh	rank51_refresh	rank50_refresh	rank49_refresh	rank48_refresh	rank47_refresh	rank46_refresh	rank45_refresh	rank44_refresh	rank43_refresh	rank42_refresh	rank41_refresh	rank40_refresh	rank39_refresh	rank38_refresh	rank37_refresh	rank36_refresh	rank35_refresh	rank34_refresh	rank33_refresh	rank32_refresh

Table 3-285 Fields for Register: OPREFCTRL1

Bits	Name	Memory Access	Description
31	rank63_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 63. Writing to this bit causes OPREFSTAT1.rank63_refresh_busy to be set. When OPREFSTAT1.rank63_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 63. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
30	rank62_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 62. Writing to this bit causes OPREFSTAT1.rank62_refresh_busy to be set. When OPREFSTAT1.rank62_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 62. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
29	rank61_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 61. Writing to this bit causes OPREFSTAT1.rank61_refresh_busy to be set. When OPREFSTAT1.rank61_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 61. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
28	rank60_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 60. Writing to this bit causes OPREFSTAT1.rank60_refresh_busy to be set. When OPREFSTAT1.rank60_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 60. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
27	rank59_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 59. Writing to this bit causes OPREFSTAT1.rank59_refresh_busy to be set. When OPREFSTAT1.rank59_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 59. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
26	rank58_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 58. Writing to this bit causes OPREFSTAT1.rank58_refresh_busy to be set. When OPREFSTAT1.rank58_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 58. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
25	rank57_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 57. Writing to this bit causes OPREFSTAT1.rank57_refresh_busy to be set. When OPREFSTAT1.rank57_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 57. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
24	rank56_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 56. Writing to this bit causes OPREFSTAT1.rank56_refresh_busy to be set. When OPREFSTAT1.rank56_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 56. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
23	rank55_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 55. Writing to this bit causes OPREFSTAT1.rank55_refresh_busy to be set. When OPREFSTAT1.rank55_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 55. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
22	rank54_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 54. Writing to this bit causes OPREFSTAT1.rank54_refresh_busy to be set. When OPREFSTAT1.rank54_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 54. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
21	rank53_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 53. Writing to this bit causes OPREFSTAT1.rank53_refresh_busy to be set. When OPREFSTAT1.rank53_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 53. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
20	rank52_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 52. Writing to this bit causes OPREFSTAT1.rank52_refresh_busy to be set. When OPREFSTAT1.rank52_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 52. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
19	rank51_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 51. Writing to this bit causes OPREFSTAT1.rank51_refresh_busy to be set. When OPREFSTAT1.rank51_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 51. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
18	rank50_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 50. Writing to this bit causes OPREFSTAT1.rank50_refresh_busy to be set. When OPREFSTAT1.rank50_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 50. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
17	rank49_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 49. Writing to this bit causes OPREFSTAT1.rank49_refresh_busy to be set. When OPREFSTAT1.rank49_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 49. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
16	rank48_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 48. Writing to this bit causes OPREFSTAT1.rank48_refresh_busy to be set. When OPREFSTAT1.rank48_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 48. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
15	rank47_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 47. Writing to this bit causes OPREFSTAT1.rank47_refresh_busy to be set. When OPREFSTAT1.rank47_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 47. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
14	rank46_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 46. Writing to this bit causes OPREFSTAT1.rank46_refresh_busy to be set. When OPREFSTAT1.rank46_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 46. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
13	rank45_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 45. Writing to this bit causes OPREFSTAT1.rank45_refresh_busy to be set. When OPREFSTAT1.rank45_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 45. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
12	rank44_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 44. Writing to this bit causes OPREFSTAT1.rank44_refresh_busy to be set. When OPREFSTAT1.rank44_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 44. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
11	rank43_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 43. Writing to this bit causes OPREFSTAT1.rank43_refresh_busy to be set. When OPREFSTAT1.rank43_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 43. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
10	rank42_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 42. Writing to this bit causes OPREFSTAT1.rank42_refresh_busy to be set. When OPREFSTAT1.rank42_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 42. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
9	rank41_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 41. Writing to this bit causes OPREFSTAT1.rank41_refresh_busy to be set. When OPREFSTAT1.rank41_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 41. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
8	rank40_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 40. Writing to this bit causes OPREFSTAT1.rank40_refresh_busy to be set. When OPREFSTAT1.rank40_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 40. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
7	rank39_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 39. Writing to this bit causes OPREFSTAT1.rank39_refresh_busy to be set. When OPREFSTAT1.rank39_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 39. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
6	rank38_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 38. Writing to this bit causes OPREFSTAT1.rank38_refresh_busy to be set. When OPREFSTAT1.rank38_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 38. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
5	rank37_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 37. Writing to this bit causes OPREFSTAT1.rank37_refresh_busy to be set. When OPREFSTAT1.rank37_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 37. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
4	rank36_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 36. Writing to this bit causes OPREFSTAT1.rank36_refresh_busy to be set. When OPREFSTAT1.rank36_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 36. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
3	rank35_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 35. Writing to this bit causes OPREFSTAT1.rank35_refresh_busy to be set. When OPREFSTAT1.rank35_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 35. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
2	rank34_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 34. Writing to this bit causes OPREFSTAT1.rank34_refresh_busy to be set. When OPREFSTAT1.rank34_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 34. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic
1	rank33_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 33. Writing to this bit causes OPREFSTAT1.rank33_refresh_busy to be set. When OPREFSTAT1.rank33_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 33. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

Table 3-285 Fields for Register: OPREFCTRL1 (continued)

Bits	Name	Memory Access	Description
0	rank32_refresh	R/W1S	Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 32. Writing to this bit causes OPREFSTAT1.rank32_refresh_busy to be set. When OPREFSTAT1.rank32_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 32. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. **Value After Reset:** 0x0 **Testable:** readOnly **Programming Mode:** Dynamic

3.3.71 OPREFSTAT0

- **Name:** Refresh Operation Status Register 0
- **Description:** Refresh Operation Status Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11ba0
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank31_refresh_busy	rank30_refresh_busy	rank29_refresh_busy	rank28_refresh_busy	rank27_refresh_busy	rank26_refresh_busy	rank25_refresh_busy	rank24_refresh_busy	rank23_refresh_busy	rank22_refresh_busy	rank21_refresh_busy	rank20_refresh_busy	rank19_refresh_busy	rank18_refresh_busy	rank17_refresh_busy	rank16_refresh_busy	rank15_refresh_busy	rank14_refresh_busy	rank13_refresh_busy	rank12_refresh_busy	rank11_refresh_busy	rank10_refresh_busy	rank9_refresh_busy	rank8_refresh_busy	rank7_refresh_busy	rank6_refresh_busy	rank5_refresh_busy	rank4_refresh_busy	rank3_refresh_busy	rank2_refresh_busy	rank1_refresh_busy	rank0_refresh_busy

Table 3-286 Fields for Register: OPREFSTAT0

Bits	Name	Memory Access	Description
31	rank31_refresh_busy	R	SoC core may initiate a rank31_refresh operation (refresh operation to rank 31) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank31_refresh is set to one. It goes low when the rank31_refresh operation is stored in the DDRCTL. It is recommended not to perform rank31_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank31_refresh operation ■ 1 - Indicates that rank31_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
30	rank30_refresh_busy	R	SoC core may initiate a rank30_refresh operation (refresh operation to rank 30) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank30_refresh is set to one. It goes low when the rank30_refresh operation is stored in the DDRCTL. It is recommended not to perform rank30_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank30_refresh operation ■ 1 - Indicates that rank30_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	rank29_refresh_busy	R	SoC core may initiate a rank29_refresh operation (refresh operation to rank 29) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank29_refresh is set to one. It goes low when the rank29_refresh operation is stored in the DDRCTL. It is recommended not to perform rank29_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank29_refresh operation ■ 1 - Indicates that rank29_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	rank28_refresh_busy	R	SoC core may initiate a rank28_refresh operation (refresh operation to rank 28) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank28_refresh is set to one. It goes low when the rank28_refresh operation is stored in the DDRCTL. It is recommended not to perform rank28_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank28_refresh operation ■ 1 - Indicates that rank28_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
27	rank27_refresh_busy	R	SoC core may initiate a rank27_refresh operation (refresh operation to rank 27) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank27_refresh is set to one. It goes low when the rank27_refresh operation is stored in the DDRCTL. It is recommended not to perform rank27_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank27_refresh operation ■ 1 - Indicates that rank27_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26	rank26_refresh_busy	R	SoC core may initiate a rank26_refresh operation (refresh operation to rank 26) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank26_refresh is set to one. It goes low when the rank26_refresh operation is stored in the DDRCTL. It is recommended not to perform rank26_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank26_refresh operation ■ 1 - Indicates that rank26_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	rank25_refresh_busy	R	SoC core may initiate a rank25_refresh operation (refresh operation to rank 25) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank25_refresh is set to one. It goes low when the rank25_refresh operation is stored in the DDRCTL. It is recommended not to perform rank25_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank25_refresh operation ■ 1 - Indicates that rank25_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
24	rank24_refresh_busy	R	SoC core may initiate a rank24_refresh operation (refresh operation to rank 24) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank24_refresh is set to one. It goes low when the rank24_refresh operation is stored in the DDRCTL. It is recommended not to perform rank24_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank24_refresh operation ■ 1 - Indicates that rank24_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	rank23_refresh_busy	R	SoC core may initiate a rank23_refresh operation (refresh operation to rank 23) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank23_refresh is set to one. It goes low when the rank23_refresh operation is stored in the DDRCTL. It is recommended not to perform rank23_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank23_refresh operation ■ 1 - Indicates that rank23_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	rank22_refresh_busy	R	SoC core may initiate a rank22_refresh operation (refresh operation to rank 22) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank22_refresh is set to one. It goes low when the rank22_refresh operation is stored in the DDRCTL. It is recommended not to perform rank22_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank22_refresh operation ■ 1 - Indicates that rank22_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
21	rank21_refresh_busy	R	SoC core may initiate a rank21_refresh operation (refresh operation to rank 21) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank21_refresh is set to one. It goes low when the rank21_refresh operation is stored in the DDRCTL. It is recommended not to perform rank21_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank21_refresh operation ■ 1 - Indicates that rank21_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	rank20_refresh_busy	R	SoC core may initiate a rank20_refresh operation (refresh operation to rank 20) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank20_refresh is set to one. It goes low when the rank20_refresh operation is stored in the DDRCTL. It is recommended not to perform rank20_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank20_refresh operation ■ 1 - Indicates that rank20_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	rank19_refresh_busy	R	SoC core may initiate a rank19_refresh operation (refresh operation to rank 19) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank19_refresh is set to one. It goes low when the rank19_refresh operation is stored in the DDRCTL. It is recommended not to perform rank19_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank19_refresh operation ■ 1 - Indicates that rank19_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
18	rank18_refresh_busy	R	SoC core may initiate a rank18_refresh operation (refresh operation to rank 18) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank18_refresh is set to one. It goes low when the rank18_refresh operation is stored in the DDRCTL. It is recommended not to perform rank18_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank18_refresh operation ■ 1 - Indicates that rank18_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	rank17_refresh_busy	R	SoC core may initiate a rank17_refresh operation (refresh operation to rank 17) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank17_refresh is set to one. It goes low when the rank17_refresh operation is stored in the DDRCTL. It is recommended not to perform rank17_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank17_refresh operation ■ 1 - Indicates that rank17_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	rank16_refresh_busy	R	SoC core may initiate a rank16_refresh operation (refresh operation to rank 16) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank16_refresh is set to one. It goes low when the rank16_refresh operation is stored in the DDRCTL. It is recommended not to perform rank16_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank16_refresh operation ■ 1 - Indicates that rank16_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
15	rank15_refresh_busy	R	SoC core may initiate a rank15_refresh operation (refresh operation to rank 15) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank15_refresh is set to one. It goes low when the rank15_refresh operation is stored in the DDRCTL. It is recommended not to perform rank15_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank15_refresh operation ■ 1 - Indicates that rank15_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	rank14_refresh_busy	R	SoC core may initiate a rank14_refresh operation (refresh operation to rank 14) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank14_refresh is set to one. It goes low when the rank14_refresh operation is stored in the DDRCTL. It is recommended not to perform rank14_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank14_refresh operation ■ 1 - Indicates that rank14_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13	rank13_refresh_busy	R	SoC core may initiate a rank13_refresh operation (refresh operation to rank 13) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank13_refresh is set to one. It goes low when the rank13_refresh operation is stored in the DDRCTL. It is recommended not to perform rank13_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank13_refresh operation ■ 1 - Indicates that rank13_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
12	rank12_refresh_busy	R	SoC core may initiate a rank12_refresh operation (refresh operation to rank 12) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank12_refresh is set to one. It goes low when the rank12_refresh operation is stored in the DDRCTL. It is recommended not to perform rank12_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank12_refresh operation ■ 1 - Indicates that rank12_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	rank11_refresh_busy	R	SoC core may initiate a rank11_refresh operation (refresh operation to rank 11) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank11_refresh is set to one. It goes low when the rank11_refresh operation is stored in the DDRCTL. It is recommended not to perform rank11_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank11_refresh operation ■ 1 - Indicates that rank11_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	rank10_refresh_busy	R	SoC core may initiate a rank10_refresh operation (refresh operation to rank 10) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank10_refresh is set to one. It goes low when the rank10_refresh operation is stored in the DDRCTL. It is recommended not to perform rank10_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank10_refresh operation ■ 1 - Indicates that rank10_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
9	rank9_refresh_busy	R	SoC core may initiate a rank9_refresh operation (refresh operation to rank 9) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank9_refresh is set to one. It goes low when the rank9_refresh operation is stored in the DDRCTL. It is recommended not to perform rank9_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank9_refresh operation ■ 1 - Indicates that rank9_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	rank8_refresh_busy	R	SoC core may initiate a rank8_refresh operation (refresh operation to rank 8) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank8_refresh is set to one. It goes low when the rank8_refresh operation is stored in the DDRCTL. It is recommended not to perform rank8_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank8_refresh operation ■ 1 - Indicates that rank8_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	rank7_refresh_busy	R	SoC core may initiate a rank7_refresh operation (refresh operation to rank 7) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank7_refresh is set to one. It goes low when the rank7_refresh operation is stored in the DDRCTL. It is recommended not to perform rank7_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank7_refresh operation ■ 1 - Indicates that rank7_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
6	rank6_refresh_busy	R	SoC core may initiate a rank6_refresh operation (refresh operation to rank 6) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank6_refresh is set to one. It goes low when the rank6_refresh operation is stored in the DDRCTL. It is recommended not to perform rank6_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank6_refresh operation ■ 1 - Indicates that rank6_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
5	rank5_refresh_busy	R	SoC core may initiate a rank5_refresh operation (refresh operation to rank 5) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank5_refresh is set to one. It goes low when the rank5_refresh operation is stored in the DDRCTL. It is recommended not to perform rank5_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank5_refresh operation ■ 1 - Indicates that rank5_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	rank4_refresh_busy	R	SoC core may initiate a rank4_refresh operation (refresh operation to rank 4) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank4_refresh is set to one. It goes low when the rank4_refresh operation is stored in the DDRCTL. It is recommended not to perform rank4_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank4_refresh operation ■ 1 - Indicates that rank4_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
3	rank3_refresh_busy	R	SoC core may initiate a rank3_refresh operation (refresh operation to rank 3) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank3_refresh is set to one. It goes low when the rank3_refresh operation is stored in the DDRCTL. It is recommended not to perform rank3_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank3_refresh operation ■ 1 - Indicates that rank3_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	rank2_refresh_busy	R	SoC core may initiate a rank2_refresh operation (refresh operation to rank 2) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank2_refresh is set to one. It goes low when the rank2_refresh operation is stored in the DDRCTL. It is recommended not to perform rank2_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank2_refresh operation ■ 1 - Indicates that rank2_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	rank1_refresh_busy	R	SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the DDRCTL. It is recommended not to perform rank1_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank1_refresh operation ■ 1 - Indicates that rank1_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-286 Fields for Register: OPREFSTAT0 (continued)

Bits	Name	Memory Access	Description
0	rank0_refresh_busy	R	SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the DDRCTL. It is recommended not to perform rank0_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank0_refresh operation ■ 1 - Indicates that rank0_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.72 OPREFSTAT1

- **Name:** Refresh Operation Status Register 1
- **Description:** Refresh Operation Status Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11ba4
- **Exists:** UMCTL2_NUM_LRANKS_TOTAL>32

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rank63_refresh_busy	rank62_refresh_busy	rank61_refresh_busy	rank60_refresh_busy	rank59_refresh_busy	rank58_refresh_busy	rank57_refresh_busy	rank56_refresh_busy	rank55_refresh_busy	rank54_refresh_busy	rank53_refresh_busy	rank52_refresh_busy	rank51_refresh_busy	rank50_refresh_busy	rank49_refresh_busy	rank48_refresh_busy	rank47_refresh_busy	rank46_refresh_busy	rank45_refresh_busy	rank44_refresh_busy	rank43_refresh_busy	rank42_refresh_busy	rank41_refresh_busy	rank40_refresh_busy	rank39_refresh_busy	rank38_refresh_busy	rank37_refresh_busy	rank36_refresh_busy	rank35_refresh_busy	rank34_refresh_busy	rank33_refresh_busy	rank32_refresh_busy

Table 3-287 Fields for Register: OPREFSTAT1

Bits	Name	Memory Access	Description
31	rank63_refresh_busy	R	SoC core may initiate a rank63_refresh operation (refresh operation to rank 63) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank63_refresh is set to one. It goes low when the rank63_refresh operation is stored in the DDRCTL. It is recommended not to perform rank63_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank63_refresh operation ■ 1 - Indicates that rank63_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
30	rank62_refresh_busy	R	SoC core may initiate a rank62_refresh operation (refresh operation to rank 62) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank62_refresh is set to one. It goes low when the rank62_refresh operation is stored in the DDRCTL. It is recommended not to perform rank62_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank62_refresh operation ■ 1 - Indicates that rank62_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	rank61_refresh_busy	R	SoC core may initiate a rank61_refresh operation (refresh operation to rank 61) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank61_refresh is set to one. It goes low when the rank61_refresh operation is stored in the DDRCTL. It is recommended not to perform rank61_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank61_refresh operation ■ 1 - Indicates that rank61_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	rank60_refresh_busy	R	SoC core may initiate a rank60_refresh operation (refresh operation to rank 60) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank60_refresh is set to one. It goes low when the rank60_refresh operation is stored in the DDRCTL. It is recommended not to perform rank60_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank60_refresh operation ■ 1 - Indicates that rank60_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
27	rank59_refresh_busy	R	SoC core may initiate a rank59_refresh operation (refresh operation to rank 59) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank59_refresh is set to one. It goes low when the rank59_refresh operation is stored in the DDRCTL. It is recommended not to perform rank59_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank59_refresh operation ■ 1 - Indicates that rank59_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
26	rank58_refresh_busy	R	SoC core may initiate a rank58_refresh operation (refresh operation to rank 58) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank58_refresh is set to one. It goes low when the rank58_refresh operation is stored in the DDRCTL. It is recommended not to perform rank58_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank58_refresh operation ■ 1 - Indicates that rank58_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	rank57_refresh_busy	R	SoC core may initiate a rank57_refresh operation (refresh operation to rank 57) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank57_refresh is set to one. It goes low when the rank57_refresh operation is stored in the DDRCTL. It is recommended not to perform rank57_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank57_refresh operation ■ 1 - Indicates that rank57_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
24	rank56_refresh_busy	R	SoC core may initiate a rank56_refresh operation (refresh operation to rank 56) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank56_refresh is set to one. It goes low when the rank56_refresh operation is stored in the DDRCTL. It is recommended not to perform rank56_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank56_refresh operation ■ 1 - Indicates that rank56_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	rank55_refresh_busy	R	SoC core may initiate a rank55_refresh operation (refresh operation to rank 55) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank55_refresh is set to one. It goes low when the rank55_refresh operation is stored in the DDRCTL. It is recommended not to perform rank55_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank55_refresh operation ■ 1 - Indicates that rank55_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	rank54_refresh_busy	R	SoC core may initiate a rank54_refresh operation (refresh operation to rank 54) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank54_refresh is set to one. It goes low when the rank54_refresh operation is stored in the DDRCTL. It is recommended not to perform rank54_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank54_refresh operation ■ 1 - Indicates that rank54_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
21	rank53_refresh_busy	R	SoC core may initiate a rank53_refresh operation (refresh operation to rank 53) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank53_refresh is set to one. It goes low when the rank53_refresh operation is stored in the DDRCTL. It is recommended not to perform rank53_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank53_refresh operation ■ 1 - Indicates that rank53_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	rank52_refresh_busy	R	SoC core may initiate a rank52_refresh operation (refresh operation to rank 52) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank52_refresh is set to one. It goes low when the rank52_refresh operation is stored in the DDRCTL. It is recommended not to perform rank52_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank52_refresh operation ■ 1 - Indicates that rank52_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	rank51_refresh_busy	R	SoC core may initiate a rank51_refresh operation (refresh operation to rank 51) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank51_refresh is set to one. It goes low when the rank51_refresh operation is stored in the DDRCTL. It is recommended not to perform rank51_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank51_refresh operation ■ 1 - Indicates that rank51_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
18	rank50_refresh_busy	R	SoC core may initiate a rank50_refresh operation (refresh operation to rank 50) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank50_refresh is set to one. It goes low when the rank50_refresh operation is stored in the DDRCTL. It is recommended not to perform rank50_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank50_refresh operation ■ 1 - Indicates that rank50_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	rank49_refresh_busy	R	SoC core may initiate a rank49_refresh operation (refresh operation to rank 49) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank49_refresh is set to one. It goes low when the rank49_refresh operation is stored in the DDRCTL. It is recommended not to perform rank49_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank49_refresh operation ■ 1 - Indicates that rank49_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	rank48_refresh_busy	R	SoC core may initiate a rank48_refresh operation (refresh operation to rank 48) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank48_refresh is set to one. It goes low when the rank48_refresh operation is stored in the DDRCTL. It is recommended not to perform rank48_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank48_refresh operation ■ 1 - Indicates that rank48_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
15	rank47_refresh_busy	R	SoC core may initiate a rank47_refresh operation (refresh operation to rank 47) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank47_refresh is set to one. It goes low when the rank47_refresh operation is stored in the DDRCTL. It is recommended not to perform rank47_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank47_refresh operation ■ 1 - Indicates that rank47_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	rank46_refresh_busy	R	SoC core may initiate a rank46_refresh operation (refresh operation to rank 46) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank46_refresh is set to one. It goes low when the rank46_refresh operation is stored in the DDRCTL. It is recommended not to perform rank46_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank46_refresh operation ■ 1 - Indicates that rank46_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13	rank45_refresh_busy	R	SoC core may initiate a rank45_refresh operation (refresh operation to rank 45) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank45_refresh is set to one. It goes low when the rank45_refresh operation is stored in the DDRCTL. It is recommended not to perform rank45_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank45_refresh operation ■ 1 - Indicates that rank45_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
12	rank44_refresh_busy	R	SoC core may initiate a rank44_refresh operation (refresh operation to rank 44) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank44_refresh is set to one. It goes low when the rank44_refresh operation is stored in the DDRCTL. It is recommended not to perform rank44_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank44_refresh operation ■ 1 - Indicates that rank44_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	rank43_refresh_busy	R	SoC core may initiate a rank43_refresh operation (refresh operation to rank 43) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank43_refresh is set to one. It goes low when the rank43_refresh operation is stored in the DDRCTL. It is recommended not to perform rank43_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank43_refresh operation ■ 1 - Indicates that rank43_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	rank42_refresh_busy	R	SoC core may initiate a rank42_refresh operation (refresh operation to rank 42) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank42_refresh is set to one. It goes low when the rank42_refresh operation is stored in the DDRCTL. It is recommended not to perform rank42_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank42_refresh operation ■ 1 - Indicates that rank42_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
9	rank41_refresh_busy	R	SoC core may initiate a rank41_refresh operation (refresh operation to rank 41) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank41_refresh is set to one. It goes low when the rank41_refresh operation is stored in the DDRCTL. It is recommended not to perform rank41_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank41_refresh operation ■ 1 - Indicates that rank41_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	rank40_refresh_busy	R	SoC core may initiate a rank40_refresh operation (refresh operation to rank 40) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank40_refresh is set to one. It goes low when the rank40_refresh operation is stored in the DDRCTL. It is recommended not to perform rank40_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank40_refresh operation ■ 1 - Indicates that rank40_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	rank39_refresh_busy	R	SoC core may initiate a rank39_refresh operation (refresh operation to rank 39) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank39_refresh is set to one. It goes low when the rank39_refresh operation is stored in the DDRCTL. It is recommended not to perform rank39_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank39_refresh operation ■ 1 - Indicates that rank39_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
6	rank38_refresh_busy	R	SoC core may initiate a rank38_refresh operation (refresh operation to rank 38) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank38_refresh is set to one. It goes low when the rank38_refresh operation is stored in the DDRCTL. It is recommended not to perform rank38_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank38_refresh operation ■ 1 - Indicates that rank38_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
5	rank37_refresh_busy	R	SoC core may initiate a rank37_refresh operation (refresh operation to rank 37) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank37_refresh is set to one. It goes low when the rank37_refresh operation is stored in the DDRCTL. It is recommended not to perform rank37_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank37_refresh operation ■ 1 - Indicates that rank37_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	rank36_refresh_busy	R	SoC core may initiate a rank36_refresh operation (refresh operation to rank 36) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank36_refresh is set to one. It goes low when the rank36_refresh operation is stored in the DDRCTL. It is recommended not to perform rank36_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank36_refresh operation ■ 1 - Indicates that rank36_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
3	rank35_refresh_busy	R	SoC core may initiate a rank35_refresh operation (refresh operation to rank 35) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank35_refresh is set to one. It goes low when the rank35_refresh operation is stored in the DDRCTL. It is recommended not to perform rank35_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank35_refresh operation ■ 1 - Indicates that rank35_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	rank34_refresh_busy	R	SoC core may initiate a rank34_refresh operation (refresh operation to rank 34) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank34_refresh is set to one. It goes low when the rank34_refresh operation is stored in the DDRCTL. It is recommended not to perform rank34_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank34_refresh operation ■ 1 - Indicates that rank34_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	rank33_refresh_busy	R	SoC core may initiate a rank33_refresh operation (refresh operation to rank 33) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank33_refresh is set to one. It goes low when the rank33_refresh operation is stored in the DDRCTL. It is recommended not to perform rank33_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank33_refresh operation ■ 1 - Indicates that rank33_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-287 Fields for Register: OPREFSTAT1 (continued)

Bits	Name	Memory Access	Description
0	rank32_refresh_busy	R	SoC core may initiate a rank32_refresh operation (refresh operation to rank 32) only if this signal is low. This signal goes high in the clock after OPREFCTRL1.rank32_refresh is set to one. It goes low when the rank32_refresh operation is stored in the DDRCTL. It is recommended not to perform rank32_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank32_refresh operation ■ 1 - Indicates that rank32_refresh operation has not been stored yet in the DDRCTL **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.3.73 DBICTL

- **Name:** DM/DBI Control Register
- **Description:** DM/DBI Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11c94
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

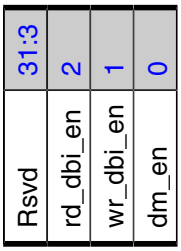


Table 3-288 Fields for Register: DBICTL

Bits	Name	Memory Access	Description
31:3			**Reserved Field:** Yes
2	rd_dbi_en	R/W	Read DBI enable signal in DDRC. ■ 0 - Read DBI is disabled. ■ 1 - Read DBI is enabled. This signal must be set the same value as DRAM's mode register. ■ DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. ■ DDR5: This signal must be set to 0. ■ LPDDR4/LPDDR5: MR3[6]. In case of LPDDR5, if LNKECCCTL0.rd_link_ecc_enable is set to 1, Read DBI is disabled automatically regardless of DBICTL.rd_dbi_en value. Note that LNKECCCTL0.rd_link_ecc_enable is replicated per frequency, so if MSTR2.target_frequency or internal target_frequency for HWFFC is changed, Read DBI may also be changed automatically. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1

Table 3-288 Fields for Register: DBICTL (continued)

Bits	Name	Memory Access	Description
1	wr_dbi_en	R/W	Write DBI enable signal in DDRC. ■ 0 - Write DBI is disabled. ■ 1 - Write DBI is enabled. This signal must be set the same value as DRAM's mode register. ■ DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. ■ DDR5: This signal must be set to 0. ■ LPDDR4/LPDDR5: MR3[7]. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 1
0	dm_en	R/W	DM enable signal in DDRC. ■ 0 - DM is disabled. ■ 1 - DM is enabled. This signal must be set the same logical value as DRAM's mode register. ■ DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. ■ DDR5: Set this to same value as MR5[5]. When x4 devices are used, this signal must be set to 0. ■ LPDDR4/LPDDR5: Set this to inverted value of MR13[5] which is opposite polarity from this signal. **Value After Reset:** 0x1 **Volatile:** true **Programming Mode:** Static

3.3.74 ODTMAP

- **Name:** ODT/Rank Map Register
- **Description:** ODT/Rank Map Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11c9c
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
NOTE: Please set ODTMAP.rank*_wr/rd_odt to all zero because the ODT feature is automatically turned ON/OFF in LPDDR4/LPDDR5 SDRAM memories. In addition, the DRAMSET1TMG13.odtloff register field must be appropriately programmed.
For DDR5 SDRAM memories, this should be set based on system design requirement and training results. Controller provides customers with more flexibilities that customers have options to send or not to send the NT-ODT command to the NT-ranks for better signal integrity and/or power saving. For example, when sending Read to Rank0, customer can choose to send NT-ODT command to Rank1 and Rank3, but not to send NT-ODT command to Rank2. It's system decision. If no particular requirements, customers should enable NT-ODT to all NT-ranks by setting 4'hF (only effective to NT-ranks).

x:28	x:24	x:20	x:16	x:12	x:8	x:4	x:0
rank3_rd_odt	rank3_wr_odt	rank2_rd_odt	rank2_wr_odt	rank1_rd_odt	rank1_wr_odt	rank0_rd_odt	rank0_wr_odt

Table 3-289 Fields for Register: ODTMAP

Bits	Name	Memory Access	Description
x:28	rank3_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 3. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x8 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 27

Table 3-289 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:24	rank3_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 3. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x8 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 23
x:20	rank2_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 2. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x4 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 19
x:16	rank2_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 2. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 4 ranks **Value After Reset:** "(MEMC_NUM_RANKS>=4) ? 0x4 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 15

Table 3-289 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:12	rank1_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks **Value After Reset:** "(MEMC_NUM_RANKS>1) ? 0x2 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 11
x:8	rank1_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks **Value After Reset:** "(MEMC_NUM_RANKS>1) ? 0x2 : 0x0" **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 7
x:4	rank0_rd_odt	R/W	Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. **Value After Reset:** 0x1 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 3

Table 3-289 Fields for Register: ODTMAP (continued)

Bits	Name	Memory Access	Description
x:0	rank0_wr_odt	R/W	Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. **Value After Reset:** 0x1 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" - 1

3.3.75 INITTMG0

- **Name:** SDRAM Initialization Timing Register 0
- **Description:** SDRAM Initialization Timing Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x11d00
- **Exists:** Always

This register is in block REGB_DDRC_CH1.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

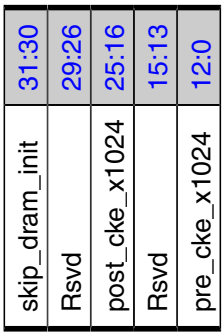


Table 3-290 Fields for Register: INITTMG0

Bits	Name	Memory Access	Description
31:30	skip_dram_init	R/W	If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed ■ 00 - SDRAM Initialization routine is run after power-up ■ 01 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Normal Mode ■ 11 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Self-refresh Mode ■ 10 - Reserved. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 2
29:26			**Reserved Field:** Yes

Table 3-290 Fields for Register: INITTMG0 (continued)

Bits	Name	Memory Access	Description
25:16	post_cke_x1024	R/W	Cycles to wait after driving CKE high to start the SDRAM initialization sequence. LPDDR4: typically requires this to be programmed for a delay of 2 us. LPDDR5: Don't care Not used for DDR5. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x2 **Programming Mode:** Static
15:13			**Reserved Field:** Yes
12:0	pre_cke_x1024	R/W	Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. LPDDR4: tINIT3 of 2 ms (min) LPDDR5: Don't care (For LPDDR5, DDRCTL doesn't send the first PDX command to the SDRAM - Assumption is that the first PDX is issued as part of initialization performed by PHY) For DDR4 RDIMMs, this must include the time needed to satisfy tSTAB. Not used for DDR5. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. **Value After Reset:** 0x4e **Programming Mode:** Static

3.4 REGB_ARB_PORTp Registers

3.4.1 PCCFG

- **Name:** Port Common Configuration Register.
- **Description:** Port Common Configuration Register.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20000+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

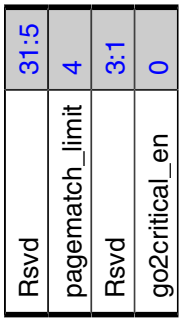


Table 3-291 Fields for Register: PCCFG

Bits	Name	Memory Access	Description
31:5			**Reserved Field:** Yes
4	pagematch_limit	R/W	Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. **Value After Reset:** 0x0 **Programming Mode:** Static
3:1			**Reserved Field:** Yes
0	go2critical_en	R/W	If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.4.2 PCFGR

- **Name:** Configuration Read Register
- **Description:** Configuration Read Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20004+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

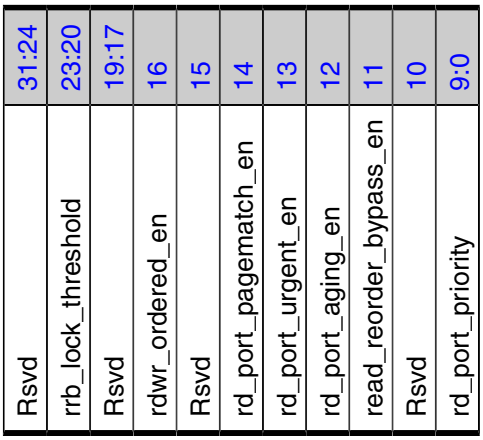


Table 3-292 Fields for Register: PCFGR

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:20	rrb_lock_threshold	R/W	Specifies the RRB lock threshold in configurations that disable read data interleaving. Threshold is specified in terms of the HIF bursts that belong to the same AXI transaction. RRB locks onto VC only when this specified number of HIF bursts are returned by DDRC. RRB lock occurs earlier in cases where the axi transaction itself is shorter and the total number of corresponding HIF bursts are below the programmed threshold and all of them are returned by DDRC. When N is programmed in this field, the threshold will be set to N+1 bursts. Max thresholding is up to 16 bursts. **Value After Reset:** 0x0 **Programming Mode:** Static
19:17			**Reserved Field:** Yes

Table 3-292 Fields for Register: PCFGR (continued)

Bits	Name	Memory Access	Description
16	rdwr_ordered_en	R/W	Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
15			**Reserved Field:** Yes
14	rd_port_pagematch_en	R/W	If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. **Value After Reset:** "(MEMC_DDR4_EN==1) ? 0x0 : 0x1" **Programming Mode:** Static
13	rd_port_urgent_en	R/W	If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). **Value After Reset:** 0x0 **Programming Mode:** Static
12	rd_port_aging_en	R/W	If set to 1, enables aging function for the read channel of the port. **Value After Reset:** 0x1 **Programming Mode:** Static

Table 3-292 Fields for Register: PCFGR (continued)

Bits	Name	Memory Access	Description
11	read_reorder_bypass_en	R/W	If set to 1, read transactions with ID not covered by any of the virtual channel ID mapping registers are not reordered. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static
10			**Reserved Field:** Yes
9:0	rd_port_priority	R/W	Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. **Value After Reset:** 0x1f **Programming Mode:** Static

3.4.3 PCFGW

- **Name:** Configuration Write Register
- **Description:** Configuration Write Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20008+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

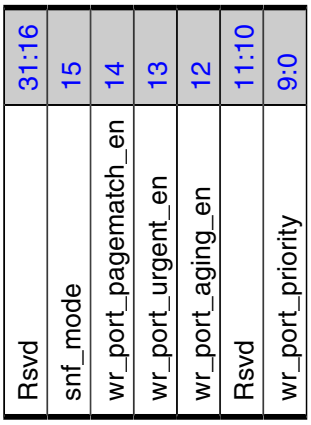


Table 3-293 Fields for Register: PCFGW

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15	snf_mode	R/W	If set to 1, enables Store & Forward Mode This bit controls the XPI port's Write Request Path. In 'Store & Forward' mode, XPI issues a HIF Write Request to the Port Arbiter only after all the respective HIF write Data beats is available. In non- 'Store & Forward' mode, XPI issues the HIF Write request to the Port Arbiter irrespective of the HIF Write Data availability within it. Values: 0 - Programmable Store & Forward is disabled 1 - Programmable Store & Forward is enabled If 'Read-Modify-Write' functionality is enabled through register programming - DBICTL.dm_en = 0/ ECCCFG0.reg_ecc_mode>0, 'Store & Forward' functionality can't be disabled. Hence, this register bit will be a don't care. **Value After Reset:** 0x1 **Programming Mode:** Static

Table 3-293 Fields for Register: PCFGW (continued)

Bits	Name	Memory Access	Description
14	wr_port_pagematch_en	R/W	If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. **Value After Reset:** 0x1 **Programming Mode:** Static
13	wr_port_urgent_en	R/W	If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). **Value After Reset:** 0x0 **Programming Mode:** Static
12	wr_port_aging_en	R/W	If set to 1, enables aging function for the write channel of the port. **Value After Reset:** 0x1 **Programming Mode:** Static
11:10			**Reserved Field:** Yes

Table 3-293 Fields for Register: PCFGW (continued)

Bits	Name	Memory Access	Description
9:0	wr_port_priority	R/W	Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. **Value After Reset:** 0x1f **Programming Mode:** Static

3.4.4 PCFGIDMASKCHc (for c = 0; c <= 15)

- **Name:** Channel 0 Configuration ID mask register
- **Description:** Channel 0 Configuration ID mask register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20010+p*0x1000+c*0x8
- **Exists:** UMCTL2_PORT_CH0_0==1 && UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

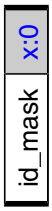


Table 3-294 Fields for Register: PCFGIDMASKCHc (for c = 0; c <= 15)

Bits	Name	Memory Access	Description
x:0	id_mask	R/W	Determines the mask used in the ID mapping function for virtual channel m. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_A_ID_MAPW" - 1

3.4.5 PCFGIDVALUECHc (for c = 0; c <= 15)

- **Name:** Channel 0 Configuration ID value register
- **Description:** Channel 0 Configuration ID value register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20014+p*0x1000+c*0x8
- **Exists:** UMCTL2_PORT_CH0_0==1 && UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

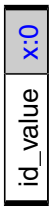


Table 3-295 Fields for Register: PCFGIDVALUECHc (for c = 0; c <= 15)

Bits	Name	Memory Access	Description
x:0	id_value	R/W	Determines the value used in the ID mapping function for virtual channel m. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Static **Range Variable[x]:** "UMCTL2_A_ID_MAPW" - 1

3.4.6 PCTRL

- **Name:** Port Control Register
- **Description:** Port Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20090+p*0x1000
- **Exists:** DDRCTL_HIF_SBR_EN_1==0

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

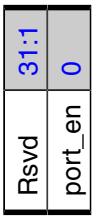


Table 3-296 Fields for Register: PCTRL

Bits	Name	Memory Access	Description
31:1			**Reserved Field:** Yes
0	port_en	R/W	Enables AXI/CHI port n. In CHI configurations RxREQ flits are received in CHB's transaction layer only when this 1 **Value After Reset:** "UMCTL2_PORT_EN_RESET_VALUE" **Programming Mode:** Dynamic

3.4.7 PCFGQOS0

- **Name:** Port n Read QoS Configuration Register 0
- **Description:** Port n Read QoS Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20094+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

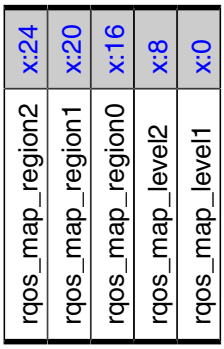


Table 3-297 Fields for Register: PCFGQOS0

Bits	Name	Memory Access	Description
x:24	rqos_map_region2	R/W	This bitfield indicates the traffic class of region2. For dual address queue configurations, region2 maps to the red address queue. Valid values are 1: VPR and 2: HPR only. When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region2 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. **Value After Reset:** 0x2 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_RW" + 23

Table 3-297 Fields for Register: PCFGQOS0 (continued)

Bits	Name	Memory Access	Description
x:20	rqos_map_region1	R/W	This bitfield indicates the traffic class of region 1. Valid values are: ■ 0 : LPR ■ 1: VPR ■ 2: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are ■ 0: LPR ■ 1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_RW" + 19
x:16	rqos_map_region0	R/W	This bitfield indicates the traffic class of region 0. Valid values are: ■ 0: LPR ■ 1: VPR ■ 2: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 0: LPR and 1: VPR only. When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_RW" + 15

Table 3-297 Fields for Register: PCFGQOS0 (continued)

Bits	Name	Memory Access	Description
x:8	rqos_map_level2	R/W	Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to arqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. **Value After Reset:** 0xe **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_MLW" + 7
x:0	rqos_map_level1	R/W	Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_MLW" - 1

3.4.8 PCFGQOS1

- **Name:** Port n Read QoS Configuration Register 1
- **Description:** Port n Read QoS Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20098+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

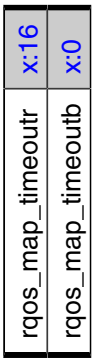


Table 3-298 Fields for Register: PCFGQOS1

Bits	Name	Memory Access	Description
x:16	rqos_map_timeoutr	R/W	Specifies the timeout value for transactions mapped to the red address queue. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_TW" + 15
x:0	rqos_map_timeoutb	R/W	Specifies the timeout value for transactions mapped to the blue address queue. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_RQOS_TW" - 1

3.4.9 PCFGWQOS0

- **Name:** Port n Write QoS Configuration Register 0
- **Description:** Port n Write QoS Configuration Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x2009c+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

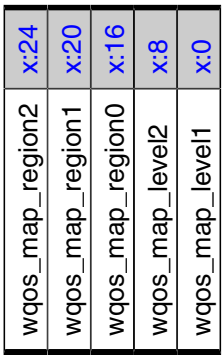


Table 3-299 Fields for Register: PCFGWQOS0

Bits	Name	Memory Access	Description
x:24	wqos_map_region2	R/W	This bitfield indicates the traffic class of region 2. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_RW" + 23
x:20	wqos_map_region1	R/W	This bitfield indicates the traffic class of region 1. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_RW" + 19

Table 3-299 Fields for Register: PCFGWQOS0 (continued)

Bits	Name	Memory Access	Description
x:16	wqos_map_region0	R/W	This bitfield indicates the traffic class of region 0. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_RW" + 15
x:8	wqos_map_level2	R/W	Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. **Value After Reset:** 0xe **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_MLW" + 7
x:0	wqos_map_level1	R/W	Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_MLW" - 1

3.4.10 PCFGWQOS1

- **Name:** Port n Write QoS Configuration Register 1
- **Description:** Port n Write QoS Configuration Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200a0+p*0x1000
- **Exists:** UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

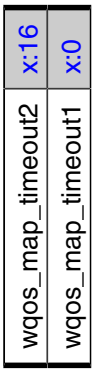


Table 3-300 Fields for Register: PCFGWQOS1

Bits	Name	Memory Access	Description
x:16	wqos_map_timeout2	R/W	Specifies the timeout value for write transactions in region 2. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_TW" + 15
x:0	wqos_map_timeout1	R/W	Specifies the timeout value for write transactions in region 0 and 1. **Value After Reset:** 0x0 **Volatile:** true **Programming Mode:** Quasi-dynamic Group 3 **Range Variable[x]:** "UMCTL2_XPI_WQOS_TW" - 1

3.4.11 SARBASEs (for s = 0; s <= 3)

- **Name:** SAR Base Address Register 0.
- **Description:** SAR Base Address Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200c0+p*0x1000+s*0x8
- **Exists:** UMCTL2_A_SAR_0==1 && UMCTL2_INCL_ARB_OR_CHB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

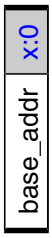


Table 3-301 Fields for Register: SARBASEs (for s = 0; s <= 3)

Bits	Name	Memory Access	Description
x:0	base_addr	R/W	Base address for address region n specified as a[w|r]addr[UMCTL2_A_ADDRW-1:x] in case of AXI configurations or rxreq.addr[DDRCTL_CHB_ADRW-1:x] in case on CHI configurations. where x is determined by the minimum block size parameter UMCTL2_SARMINSIZE: (x=log2(block size)). **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "DDRCTL_SAR_REG_BW" - 1

3.4.12 SARSIZEs (for s = 0; s <= 3)

- **Name:** SAR Size Register 0.
- **Description:** SAR Size Register 0.
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200c4+p*0x1000+s*0x8
- **Exists:** UMCTL2_A_SAR_0==1 && UMCTL2_INCL_ARB_OR_CHB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

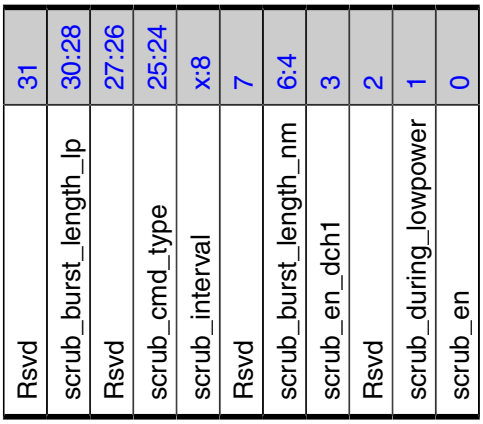
Table 3-302 Fields for Register: SARSIZEs (for s = 0; s <= 3)

Bits	Name	Memory Access	Description
x:0	nblocks	R/W	Number of blocks for address region n. This register determines the total size of the region in multiples of minimum block size as specified by the hardware parameter UMCTL2_SARMINSIZE. The register value is encoded as number of blocks = nblocks + 1. For example, if register is programmed to 0, region will have 1 block. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "DDRCTL_SAR_SW" - 1

3.4.13 SBRCTL

- **Name:** Scrubber Control Register
- **Description:** Scrubber Control Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200e0+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
This register is only present in REGB_ARB_PORT0, therefore p=0 for the offset calculation



31	30:28	27:26	25:24	x:8	7	6:4	3	2	1	0
Rsvd	scrub_burst_length_lp	Rsvd	scrub_cmd_type	scrub_interval	Rsvd	scrub_burst_length_nm	scrub_en_dch1	Rsvd	scrub_during_lowpower	scrub_en

Table 3-303 Fields for Register: SBRCTL

Bits	Name	Memory Access	Description
31			**Reserved Field:** Yes

Table 3-303 Fields for Register: SBRCTL (continued)

Bits	Name	Memory Access	Description
30:28	scrub_burst_length_lp	R/W	Scrub burst length in Low Power mode - Determines the number of back-to-back scrub read commands that can be issued together when the controller is in one of the HW controlled low power modes with Sideband ECC and Inline ECC. - During these modes, the period of the scrub burst becomes "scrub_burst_length_lp*scrub_interval" cycles. Valid values are (Sideband ECC): ■ 1: 1 read, ■ 2: 4 reads, ■ 3: 16 reads, ■ 4: 64 reads, ■ 5: 256 reads, ■ 6: 1024 reads. (Inline ECC): ■ 1: 8 reads, ■ 2: 16 reads, ■ 3: 32 reads. To program a new value to this register field, first disable Scrubber by setting SBRCTL.scrub_en = 0. Program the new value.Enable Scrubber by setting SBRCTL.scrub_en = 1. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
27:26			**Reserved Field:** Yes
25:24	scrub_cmd_type	R/W	This field determines the kind of traffic scrubber must generate. ■ 00: Read - Only periodic reads will be generated ■ 01: Write - Only back to back initialization writes will be generated. SBRCTL.scrub_interval must be programmed to 0. ■ 10: Read Modify Write - only periodic RMWs will be generated. ■ 11: reserved. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-303 Fields for Register: SBRCTL (continued)

Bits	Name	Memory Access	Description
x:8	scrub_interval	R/W	Scrub interval. (N x scrub_interval) number of clock cycles between two scrub read commands, where N is the granularity. If set to 0, scrub commands are issued back-to-back. This mode of operation (scrub_interval=0) can typically be used for scrubbing the full range of memory at once before or after SW controlled low power operations. After completing the full range of scrub while scrub_interval=0, scrub_done register is set and sbr_done_intr interrupt signal is asserted. This mode can't be used with Inline ECC: If MEMC_INLINE_ECC is 1 and scrub_interval is programmed to 0, then RMW logic inside scrubber is disabled. New programmed value will take effect only after scrubber is disabled by programming scrub_en to 0. Unit: Multiples of 256 sbr_clk cycles in Sideband ECC configurations and 512 sbr_clk cycles in Inline ECC Configurations. **Value After Reset:** 0xff **Programming Mode:** Dynamic **Range Variable[x]:** "UMCTL2_REG_SCRUB_INTERVALW" + 7
7			**Reserved Field:** Yes

Table 3-303 Fields for Register: SBRCTL (continued)

Bits	Name	Memory Access	Description
6:4	scrub_burst_length_nm	R/W	Scrub burst length in normal mode. - Determines the number of back-to-back scrub read commands that can be issued together when the controller is in normal operation in Inline ECC & Sideband ECC. - The period of the scrub burst becomes "scrub_burst_length_nm*scrub_interval" cycles. During normal operation mode of the controller with Sideband ECC (not in power-down or self refresh), scrub_burst_length_nm is ignored and only one scrub command is generated. Valid values are (Sideband ECC): ■ 1: 1 read (Inline ECC): ■ 1: 8 reads, ■ 2: 16 reads, ■ 3: 32 reads. In Sideband ECC, software must ensure that the scrub_burst_length_nm is programmed to the value of 1. Other values are not supported. To program a new value to this register field, first disable Scrubber by setting SBRCTL.scrub_en = 0. Program the new value.Enable Scrubber by setting SBRCTL.scrub_en = 1. **Value After Reset:** 0x1 **Programming Mode:** Dynamic
3	scrub_en_dch1	R/W	Enable ECC scrubber for channel 1. If set to 1, enables the scrubber to generate background read commands after the memories are initialized. If set to 0, disables the scrubber, resets the address generator to 0 and clears the scrubber status. This bitfield must be accessed separately from the other bitfields in this register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2			**Reserved Field:** Yes

Table 3-303 Fields for Register: SBRCTL (continued)

Bits	Name	Memory Access	Description
1	scrub_during_lowpower	R/W	Continue scrubbing during low power. If set to 1, burst of scrubs will be issued in HW controlled low power modes. There are two such modes: automatically initiated by idleness or initiated by Hardware low power interface. If set to 0, the scrubber will not attempt to send commands while the DDRC is in HW controlled low power modes. In this case, the scrubber will remember the last address issued and will automatically continue from there when the DDRC exits the LP mode. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	scrub_en	R/W	Enable ECC scrubber. If set to 1, enables the scrubber to generate background read commands after the memories are initialized. If set to 0, disables the scrubber, resets the address generator to 0 and clears the scrubber status. This bitfield must be accessed separately from the other bitfields in this register. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.14 SBRSTAT

- **Name:** Scrubber Status Register
- **Description:** Scrubber Status Register
- **Access Type:** Non-secure
- **Size:** 32 bits
- **Offset:** 0x200e4+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
This register is only present in REGB_ARB_PORT0, therefore p=0 for the offset calculation

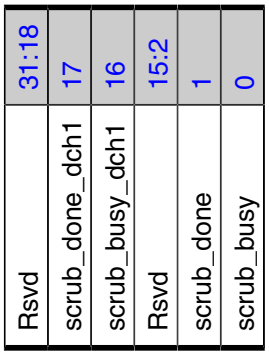


Table 3-304 Fields for Register: SBRSTAT

Bits	Name	Memory Access	Description
31:18			**Reserved Field:** Yes
17	scrub_done_dch1	R	Scrubber done for channel 1. Controller sets this bit to 1, after full range of addresses are scrubbed once while scrub_interval is set to 0. Cleared if scrub_en is set to 0 (scrubber disabled) or scrub_interval is set to a non-zero value for normal scrub operation. The interrupt signal, sbr_done_intr, is equivalent to this status bitfield. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
16	scrub_busy_dch1	R	Scrubber busy for channel 1. Controller sets this bit to 1 when the scrubber logic has outstanding read commands being executed. Cleared when there are no active outstanding scrub reads in the system. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15:2			**Reserved Field:** Yes

Table 3-304 Fields for Register: SBRSTAT (continued)

Bits	Name	Memory Access	Description
1	scrub_done	R	Scrubber done. Controller sets this bit to 1, after full range of addresses are scrubbed once while scrub_interval is set to 0. Cleared if scrub_en is set to 0 (scrubber disabled) or scrub_interval is set to a non-zero value for normal scrub operation. The interrupt signal, sbr_done_intr, is equivalent to this status bitfield. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	scrub_busy	R	Scrubber busy. Controller sets this bit to 1 when the scrubber logic has outstanding read commands being executed. Cleared when there are no active outstanding scrub reads in the system. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.15 SBRWDATA0

- **Name:** Scrubber Write Data Pattern0
- **Description:** Scrubber Write Data Pattern0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200e8+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-305 Fields for Register: SBRWDATA0

Bits	Name	Memory Access	Description
31:0	scrub_pattern0	R/W	ECC Scrubber write data pattern for data bus[31:0] **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.16 SBRWDATA1

- **Name:** Scrubber Write Data Pattern1
- **Description:** Scrubber Write Data Pattern1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200ec+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1 && MEMC_DRAM_DATA_WIDTH==64

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-306 Fields for Register: SBRWDATA1

Bits	Name	Memory Access	Description
31:0	scrub_pattern1	R/W	ECC Scrubber write data pattern for data bus[63:32] **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.17 SBRSTART0

- **Name:** Scrubber Start Address Mask Register 0
- **Description:** Scrubber Start Address Mask Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200f0+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

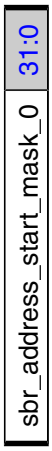


Table 3-307 Fields for Register: SBRSTART0

Bits	Name	Memory Access	Description
31:0	sbr_address_start_mask_0	R/W	sbr_address_start_mask_0 holds the bits [31:0] of the starting address the ECC scrubber generates. The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.18 SBRSTART1

- **Name:** Scrubber Start Address Mask Register 1
- **Description:** Scrubber Start Address Mask Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200f4+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

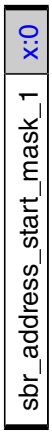


Table 3-308 Fields for Register: SBRSTART1

Bits	Name	Memory Access	Description
x:0	sbr_address_start_mask_1	R/W	sbr_address_start_mask_1 holds bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the starting address the ECC scrubber generates.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_HIF_ADDR_WIDTH_MAX - 32" - 1

3.4.19 SBRRANGE0

- **Name:** Scrubber Address Range Mask Register 0
- **Description:** Scrubber Address Range Mask Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200f8+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-309 Fields for Register: SBRRANGE0

Bits	Name	Memory Access	Description
31:0	sbr_address_range_mask_0	R/W	sbr_address_range_mask_0 holds the bits [31:0] of the scrubber address range mask. The scrubber address range mask limits the address range that the ECC scrubber can generate.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.20 SBRRANGE1

- **Name:** Scrubber Address Range Mask Register 1
- **Description:** Scrubber Address Range Mask Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x200fc+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

Table 3-310 Fields for Register: SBRRANGE1

Bits	Name	Memory Access	Description
x:0	sbr_address_range_mask_1	R/W	sbr_address_range_mask_1 holds the bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the scrubber address range mask. The scrubber address range mask limits the address range that the ECC scrubber can generate.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_HIF_ADDR_WIDTH_MAX - 32" - 1

3.4.21 SBRSTART0DCH1

- **Name:** Scrubber Start Address Mask Register 0 for Data Channel 1
- **Description:** Scrubber Start Address Mask Register 0 for Data Channel 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20100+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1 && UMCTL2_DUAL_CHANNEL==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

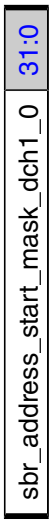


Table 3-311 Fields for Register: SBRSTART0DCH1

Bits	Name	Memory Access	Description
31:0	sbr_address_start_mask_dch1_0	R/W	sbr_address_start_mask_dch1_0 holds the bits [31:0] of the starting address the ECC scrubber generates for data channel 1.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.22 SBRSTART1DCH1

- **Name:** Scrubber Start Address Mask Register 1 for Data Channel 1
- **Description:** Scrubber Start Address Mask Register 1 for Data Channel 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20104+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1 && UMCTL2_DUAL_CHANNEL==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

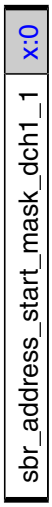


Table 3-312 Fields for Register: SBRSTART1DCH1

Bits	Name	Memory Access	Description
x:0	sbr_address_start_mask_dch1_1	R/W	sbr_address_start_mask_dch1_1 holds bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the starting address the ECC scrubber generates for data channel 1.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_HIF_ADDR_WIDTH_MAX - 32" - 1

3.4.23 SBRRANGE0DCH1

- **Name:** Scrubber Address Range Mask Register 0 for Data Channel 1
- **Description:** Scrubber Address Range Mask Register 0 for Data Channel 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20108+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1 && UMCTL2_DUAL_CHANNEL==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

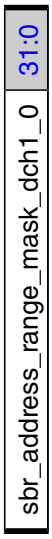


Table 3-313 Fields for Register: SBRRANGE0DCH1

Bits	Name	Memory Access	Description
31:0	sbr_address_range_mask_dch1_0	R/W	sbr_address_range_mask_dch1_0 holds bits [31:0] of the scrubber address range mask for data channel 1. The scrubber address range mask limits the address range that the ECC scrubber can generate.The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.4.24 SBRRANGE1DCH1

- **Name:** Scrubber Address Range Mask Register 1 for Data Channel 1
- **Description:** Scrubber Address Range Mask Register 1 for Data Channel 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Secure} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x2010c+p*0x1000
- **Exists:** UMCTL2_SBR_EN_1==1 && UMCTL2_DUAL_CHANNEL==1

This register is in block REGB_ARB_PORTp.
Note: This register requires secure APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

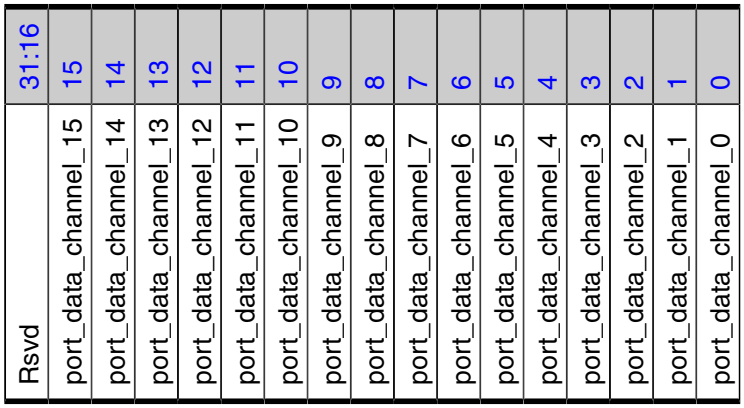
Table 3-314 Fields for Register: SBRRANGE1DCH1

Bits	Name	Memory Access	Description
x:0	sbr_address_range_mask_dch1_1	R/W	sbr_address_range_mask_dch1_1 holds bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the scrubber address range mask for data channel 1. The scrubber address range mask limits the address range that the ECC scrubber can generate. The register must be programmed as explained in Address Configuration in "Scrubber" section of DesignWare Cores DDR5/4 Memory Controller Databook. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). It is HIF address. **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "MEMC_HIF_ADDR_WIDTH_MAX - 32" - 1

3.4.25 PDCH

- **Name:** Port Data Channel
- **Description:** Port Data Channel
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20110+p*0x1000
- **Exists:** UMCTL2_DUAL_CHANNEL==1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1==0 && UMCTL2_INCL_ARB==1

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	port_data_channel_15	port_data_channel_14	port_data_channel_13	port_data_channel_12	port_data_channel_11	port_data_channel_10	port_data_channel_9	port_data_channel_8	port_data_channel_7	port_data_channel_6	port_data_channel_5	port_data_channel_4	port_data_channel_3	port_data_channel_2	port_data_channel_1	port_data_channel_0

Table 3-315 Fields for Register: PDCH

Bits	Name	Memory Access	Description
31:16			**Reserved Field:** Yes
15	port_data_channel_15	R/W	Static data channel assignment for port 15: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
14	port_data_channel_14	R/W	Static data channel assignment for port 14: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-315 Fields for Register: PDCH (continued)

Bits	Name	Memory Access	Description
13	port_data_channel_13	R/W	Static data channel assignment for port 13: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
12	port_data_channel_12	R/W	Static data channel assignment for port 12: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
11	port_data_channel_11	R/W	Static data channel assignment for port 11: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
10	port_data_channel_10	R/W	Static data channel assignment for port 10: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
9	port_data_channel_9	R/W	Static data channel assignment for port 9: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
8	port_data_channel_8	R/W	Static data channel assignment for port 8: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-315 Fields for Register: PDCH (continued)

Bits	Name	Memory Access	Description
7	port_data_channel_7	R/W	Static data channel assignment for port 7: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
6	port_data_channel_6	R/W	Static data channel assignment for port 6: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
5	port_data_channel_5	R/W	Static data channel assignment for port 5: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
4	port_data_channel_4	R/W	Static data channel assignment for port 4: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
3	port_data_channel_3	R/W	Static data channel assignment for port 3: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
2	port_data_channel_2	R/W	Static data channel assignment for port 2: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static

Table 3-315 Fields for Register: PDCH (continued)

Bits	Name	Memory Access	Description
1	port_data_channel_1	R/W	Static data channel assignment for port 1: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static
0	port_data_channel_0	R/W	Static data channel assignment for port 0: ■ 0 selects Channel 0 ■ 1 selects Channel 1 **Value After Reset:** 0x0 **Programming Mode:** Static

3.4.26 PSTAT

- **Name:** Port Status Register
- **Description:** Port Status Register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x20114+p*0x1000
- **Exists:** DDRCTL_HIF_SBR_EN_1==0

This register is in block REGB_ARB_PORTp.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
wr_port_busy_15	wr_port_busy_14	wr_port_busy_13	wr_port_busy_12	wr_port_busy_11	wr_port_busy_10	wr_port_busy_9	wr_port_busy_8	wr_port_busy_7	wr_port_busy_6	wr_port_busy_5	wr_port_busy_4	wr_port_busy_3	wr_port_busy_2	wr_port_busy_1	wr_port_busy_0	rd_port_busy_15	rd_port_busy_14	rd_port_busy_13	rd_port_busy_12	rd_port_busy_11	rd_port_busy_10	rd_port_busy_9	rd_port_busy_8	rd_port_busy_7	rd_port_busy_6	rd_port_busy_5	rd_port_busy_4	rd_port_busy_3	rd_port_busy_2	rd_port_busy_1	rd_port_busy_0

Table 3-316 Fields for Register: PSTAT

Bits	Name	Memory Access	Description
31	wr_port_busy_15	R	Indicates if there are outstanding writes for AXI/CHI port 15. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30	wr_port_busy_14	R	Indicates if there are outstanding writes for AXI/CHI port 14. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
29	wr_port_busy_13	R	Indicates if there are outstanding writes for AXI/CHI port 13. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
28	wr_port_busy_12	R	Indicates if there are outstanding writes for AXI/CHI port 12. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
27	wr_port_busy_11	R	Indicates if there are outstanding writes for AXI/CHI port 11. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-316 Fields for Register: PSTAT (continued)

Bits	Name	Memory Access	Description
26	wr_port_busy_10	R	Indicates if there are outstanding writes for AXI/CHI port 10. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
25	wr_port_busy_9	R	Indicates if there are outstanding writes for AXI/CHI port 9. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
24	wr_port_busy_8	R	Indicates if there are outstanding writes for AXI/CHI port 8. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
23	wr_port_busy_7	R	Indicates if there are outstanding writes for AXI/CHI port 7. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
22	wr_port_busy_6	R	Indicates if there are outstanding writes for AXI/CHI port 6. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
21	wr_port_busy_5	R	Indicates if there are outstanding writes for AXI/CHI port 5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
20	wr_port_busy_4	R	Indicates if there are outstanding writes for AXI/CHI port 4. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
19	wr_port_busy_3	R	Indicates if there are outstanding writes for AXI/CHI port 3. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
18	wr_port_busy_2	R	Indicates if there are outstanding writes for AXI/CHI port 2. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
17	wr_port_busy_1	R	Indicates if there are outstanding writes for AXI/CHI port 1. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-316 Fields for Register: PSTAT (continued)

Bits	Name	Memory Access	Description
16	wr_port_busy_0	R	Indicates if there are outstanding writes for AXI/CHI port 0. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
15	rd_port_busy_15	R	Indicates if there are outstanding reads for AXI/CHI port 15. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
14	rd_port_busy_14	R	Indicates if there are outstanding reads for AXI/CHI port 14. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
13	rd_port_busy_13	R	Indicates if there are outstanding reads for AXI/CHI port 13. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
12	rd_port_busy_12	R	Indicates if there are outstanding reads for AXI/CHI port 12. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
11	rd_port_busy_11	R	Indicates if there are outstanding reads for AXI/CHI port 11. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
10	rd_port_busy_10	R	Indicates if there are outstanding reads for AXI/CHI port 10. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
9	rd_port_busy_9	R	Indicates if there are outstanding reads for AXI/CHI port 9. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
8	rd_port_busy_8	R	Indicates if there are outstanding reads for AXI/CHI port 8. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7	rd_port_busy_7	R	Indicates if there are outstanding reads for AXI/CHI port 7. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-316 Fields for Register: PSTAT (continued)

Bits	Name	Memory Access	Description
6	rd_port_busy_6	R	Indicates if there are outstanding reads for AXI/CHI port 6. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
5	rd_port_busy_5	R	Indicates if there are outstanding reads for AXI/CHI port 5. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
4	rd_port_busy_4	R	Indicates if there are outstanding reads for AXI/CHI port 4. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
3	rd_port_busy_3	R	Indicates if there are outstanding reads for AXI/CHI port 3. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
2	rd_port_busy_2	R	Indicates if there are outstanding reads for AXI/CHI port 2. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
1	rd_port_busy_1	R	Indicates if there are outstanding reads for AXI/CHI port 1. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
0	rd_port_busy_0	R	Indicates if there are outstanding reads for AXI/CHI port 0. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.5 REGB_ADDR_MAP0 Registers

3.5.1 ADDRMAP0

- **Name:** Address Map Register 0
- **Description:** Address Map Register 0
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30000
- **Exists:** UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1==1

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

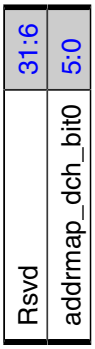


Table 3-317 Fields for Register: ADDRMAP0

Bits	Name	Memory Access	Description
31:6			**Reserved Field:** Yes
5:0	addrmap_dch_bit0	R/W	Selects the HIF address bit used as data channel address bit 0. Valid Range: 0 to 35, and 63 (Traffic constraints apply based on the register value when UMCTL2_EXCL_ACCESS>0. See Exclusive Access section for details.) Internal Base: 3 The selected address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then channel bit is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.2 ADDRMAP1

- **Name:** Address Map Register 1
- **Description:** Address Map Register 1
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30004
- **Exists:** MEMC_NUM_RANKS_GT_1==1

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

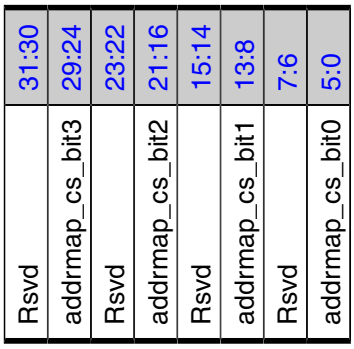


Table 3-318 Fields for Register: ADDRMAP1

Bits	Name	Memory Access	Description
31:30			**Reserved Field:** Yes
29:24	addrmap_cs_bit3	R/W	Selects the HIF address bit used as rank address bit 3. Valid Range: 0 to 26, and 63 Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 3 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
23:22			**Reserved Field:** Yes
21:16	addrmap_cs_bit2	R/W	Selects the HIF address bit used as rank address bit 2. Valid Range: 0 to 27, and 63 Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 2 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
15:14			**Reserved Field:** Yes

Table 3-318 Fields for Register: ADDRMAP1 (continued)

Bits	Name	Memory Access	Description
13:8	addrmap_cs_bit1	R/W	Selects the HIF address bit used as rank address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 1 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
7:6			**Reserved Field:** Yes
5:0	addrmap_cs_bit0	R/W	Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 33, and 63 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 0 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.3 ADDRMAP3

- **Name:** Address Map Register 3
- **Description:** Address Map Register 3
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x3000c
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

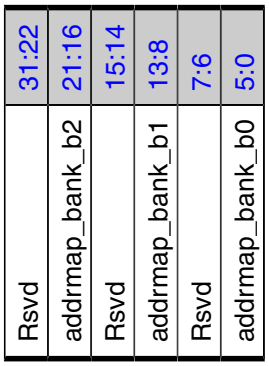


Table 3-319 Fields for Register: ADDRMAP3

Bits	Name	Memory Access	Description
31:22			**Reserved Field:** Yes
21:16	addrmap_bank_b2	R/W	Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 34, and 63 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. For LPDDR5 16B mode, this is not used and ADDRMAP4.addrmap_bg_b0 is used as BA2(bank address bit 2) instead. **Value After Reset:** 0x0 **Programming Mode:** Static
15:14			**Reserved Field:** Yes

Table 3-319 Fields for Register: ADDRMAP3 (continued)

Bits	Name	Memory Access	Description
13:8	addrmap_bank_b1	R/W	Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
7:6			**Reserved Field:** Yes
5:0	addrmap_bank_b0	R/W	Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.4 ADDRMAP4

- **Name:** Address Map Register 4
- **Description:** Address Map Register 4
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30010
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

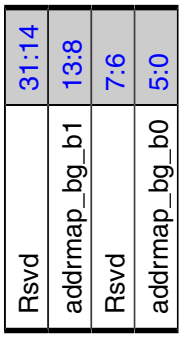


Table 3-320 Fields for Register: ADDRMAP4

Bits	Name	Memory Access	Description
31:14			**Reserved Field:** Yes
13:8	addrmap_bg_b1	R/W	Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. For LPDDR5 16B mode, this is used as BA3(bank address bit 3). **Value After Reset:** 0x0 **Programming Mode:** Static
7:6			**Reserved Field:** Yes

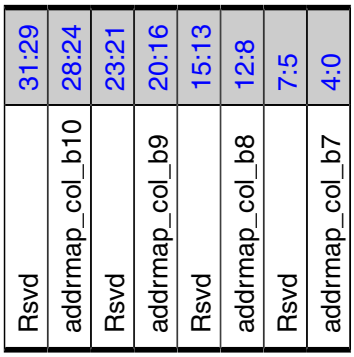
Table 3-320 Fields for Register: ADDRMAP4 (continued)

Bits	Name	Memory Access	Description
5:0	addrmap_bg_b0	R/W	Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. For LPDDR5 16B mode, this is used as BA2(bank address bit 2). **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.5 ADDRMAP5

- **Name:** Address Map Register 5
- **Description:** Address Map Register 5
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30014
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:29	28:24	23:21	20:16	15:13	12:8	7:5	4:0
Rsvd	addrmap_col_b10	Rsvd	addrmap_col_b9	Rsvd	addrmap_col_b8	Rsvd	addrmap_col_b7

Table 3-321 Fields for Register: ADDRMAP5

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes

Table 3-321 Fields for Register: ADDRMAP5 (continued)

Bits	Name	Memory Access	Description
28:24	addrmap_col_b10	R/W	Selects the HIF address bit used as column address bit 10. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 10 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
23:21			**Reserved Field:** Yes

Table 3-321 Fields for Register: ADDRMAP5 (continued)

Bits	Name	Memory Access	Description
20:16	addrmap_col_b9	R/W	Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. For LPDDR5, this is used as C5(column address bit 5). **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes
12:8	addrmap_col_b8	R/W	Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 8 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. For LPDDR5, this is used as C4(column address bit 4). **Value After Reset:** 0x0 **Programming Mode:** Static

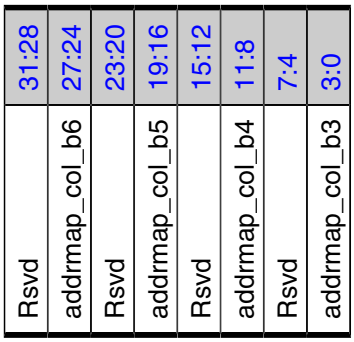
Table 3-321 Fields for Register: ADDRMAP5 (continued)

Bits	Name	Memory Access	Description
7:5			**Reserved Field:** Yes
4:0	addrmap_col_b7	R/W	Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. For LPDDR5, this is used as C3(column address bit 3). **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.6 ADDRMAP6

- **Name:** Address Map Register 6
- **Description:** Address Map Register 6
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30018
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled



31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Rsvd	addrmap_col_b6	Rsvd	addrmap_col_b5	Rsvd	addrmap_col_b4	Rsvd	addrmap_col_b3

Table 3-322 Fields for Register: ADDRMAP6

Bits	Name	Memory Access	Description
31:28			**Reserved Field:** Yes
27:24	addrmap_col_b6	R/W	Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, x and 15. x indicates a valid value in the inline ECC configuration. Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. For LPDDR5, this is used as C2(column address bit 2). **Value After Reset:** 0x0 **Programming Mode:** Static
23:20			**Reserved Field:** Yes

Table 3-322 Fields for Register: ADDRMAP6 (continued)

Bits	Name	Memory Access	Description
19:16	addrmap_col_b5	R/W	Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. For LPDDR5, this is used as C1(column address bit 1). **Value After Reset:** 0x0 **Programming Mode:** Static
15:12			**Reserved Field:** Yes
11:8	addrmap_col_b4	R/W	Selects the HIF address bit used as column address bit 4. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. For LPDDR5, this is used as C0(column address bit 0). **Value After Reset:** 0x0 **Programming Mode:** Static
7:4			**Reserved Field:** Yes
3:0	addrmap_col_b3	R/W	Selects the HIF address bit used as column address bit 3. Valid Range: 0 to 7. Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. For LPDDR5, this is used as B3(burst address bit 3). Note : In LPDDR4/5 or DDR5, it is required to program this to 0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.7 ADDRMAP7

- **Name:** Address Map Register 7
- **Description:** Address Map Register 7
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x3001c
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

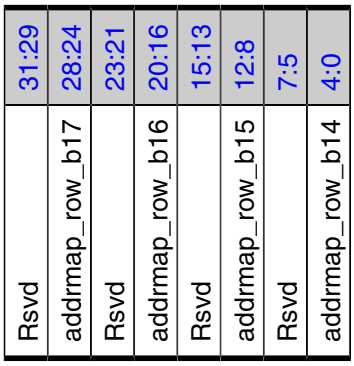


Table 3-323 Fields for Register: ADDRMAP7

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	addrmap_row_b17	R/W	Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 16, and 31 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 17 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
23:21			**Reserved Field:** Yes
20:16	addrmap_row_b16	R/W	Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 16, and 31 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 16 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes

Table 3-323 Fields for Register: ADDRMAP7 (continued)

Bits	Name	Memory Access	Description
12:8	addrmap_row_b15	R/W	Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 16, and 31 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 15 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4:0	addrmap_row_b14	R/W	Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 16, and 31 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 14 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.8 ADDRMAP8

- **Name:** Address Map Register 8
- **Description:** Address Map Register 8
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30020
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

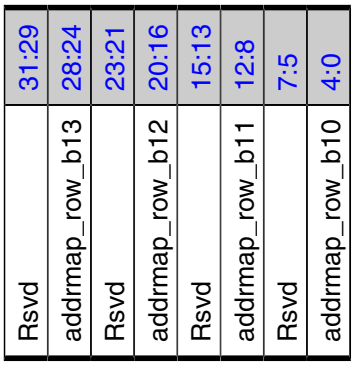


Table 3-324 Fields for Register: ADDRMAP8

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	addrmap_row_b13	R/W	Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 16, and 31 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 13 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
23:21			**Reserved Field:** Yes
20:16	addrmap_row_b12	R/W	Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 16, and 31 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 12 is set to 0. **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes

Table 3-324 Fields for Register: ADDRMAP8 (continued)

Bits	Name	Memory Access	Description
12:8	addrmap_row_b11	R/W	Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 16 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4:0	addrmap_row_b10	R/W	Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 16 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.9 ADDRMAP9

- **Name:** Address Map Register 9
- **Description:** Address Map Register 9
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30024
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

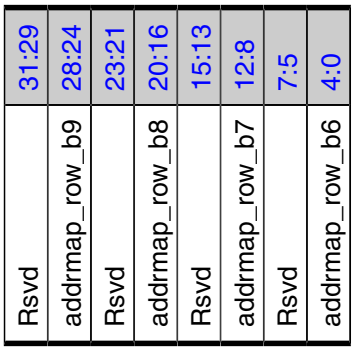


Table 3-325 Fields for Register: ADDRMAP9

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	addrmap_row_b9	R/W	Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 16 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
23:21			**Reserved Field:** Yes
20:16	addrmap_row_b8	R/W	Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 16 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes

Table 3-325 Fields for Register: ADDRMAP9 (continued)

Bits	Name	Memory Access	Description
12:8	addrmap_row_b7	R/W	Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 16 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4:0	addrmap_row_b6	R/W	Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 16 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.10 ADDRMAP10

- **Name:** Address Map Register 10
- **Description:** Address Map Register 10
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30028
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

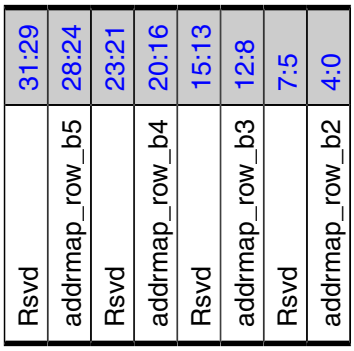


Table 3-326 Fields for Register: ADDRMAP10

Bits	Name	Memory Access	Description
31:29			**Reserved Field:** Yes
28:24	addrmap_row_b5	R/W	Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 16 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
23:21			**Reserved Field:** Yes
20:16	addrmap_row_b4	R/W	Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 16 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
15:13			**Reserved Field:** Yes

Table 3-326 Fields for Register: ADDRMAP10 (continued)

Bits	Name	Memory Access	Description
12:8	addrmap_row_b3	R/W	Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 16 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4:0	addrmap_row_b2	R/W	Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 16 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.11 ADDRMAP11

- **Name:** Address Map Register 11
- **Description:** Address Map Register 11
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x3002c
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

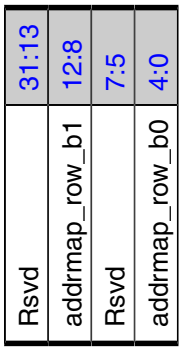


Table 3-327 Fields for Register: ADDRMAP11

Bits	Name	Memory Access	Description
31:13			**Reserved Field:** Yes
12:8	addrmap_row_b1	R/W	Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 16 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes
4:0	addrmap_row_b0	R/W	Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 16 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.12 ADDRMAP12

- **Name:** Address Map Register 12
- **Description:** Address Map Register 12
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30030
- **Exists:** Always

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

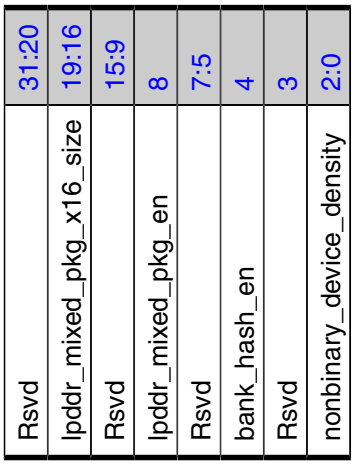


Table 3-328 Fields for Register: ADDRMAP12

Bits	Name	Memory Access	Description
31:20			**Reserved Field:** Yes

Table 3-328 Fields for Register: ADDRMAP12 (continued)

Bits	Name	Memory Access	Description
19:16	lpddr_mixed_pkg_x16_size	R/W	Indicate what type of SDRAM device is in use for x16(standard) device side if lpddr_mixed_pkg_en=1'b1. If lpddr_mixed_pkg_en=1'b0, then 5'h0 is only supported value. If lpddr_mixed_pkg_en=1'b1, then: ■ LPDDR4: ■ 5'h0: illegal setting ■ 5'h1: illegal setting ■ 5'h2: illegal setting ■ 5'h3: 2Gb ■ 5'h4: 3Gb ■ 5'h5: 4Gb ■ 5'h6: 6Gb ■ 5'h7: 8Gb ■ 5'h8: 12Gb ■ 5'h9: 16Gb ■ LPDDR5: ■ 5'h0: illegal setting ■ 5'h1: 2Gb setting ■ 5'h2: 3Gb setting ■ 5'h3: 4Gb ■ 5'h4: 6Gb ■ 5'h5: 8Gb ■ 5'h6: 12Gb ■ 5'h7: 16Gb ■ 5'h8: 24Gb ■ 5'h9: 32Gb **Value After Reset:** 0x0 **Programming Mode:** Static
15:9			**Reserved Field:** Yes
8	lpddr_mixed_pkg_en	R/W	Enables support for LPDDR mixed package. When this bit is set, ADDRMAP12.nonbinary_device_density must be set accordingly for the upper rank device density. **Value After Reset:** 0x0 **Programming Mode:** Static
7:5			**Reserved Field:** Yes

Table 3-328 Fields for Register: ADDRMAP12 (continued)

Bits	Name	Memory Access	Description
4	bank_hash_en	R/W	Enables/Disables the Bank Hashing function on the Bank,Bank-Group and row bits. ■ 1'b0: Disables the Bank Hashing function ■ 1'b1: Enables the Bank Hashing function **Value After Reset:** 0x0 **Programming Mode:** Static
3			**Reserved Field:** Yes
2:0	nonbinary_device_density	R/W	Indicates what type of SDRAM device is in use. ■ 3'b000: All addresses are valid ■ 3'b001: Every address having row[13:12]==2'b11 is considered as invalid ■ 3'b010: Every address having row[14:13]==2'b11 is considered as invalid ■ 3'b011: Every address having row[15:14]==2'b11 is considered as invalid ■ 3'b100: Every address having row[16:15]==2'b11 is considered as invalid ■ 3'b101: Every address having row[17:16]==2'b11 is considered as invalid **Value After Reset:** 0x0 **Programming Mode:** Static

3.5.13 ADDRMAPLUTCFG

- **Name:** Addr CS map LUT config register
- **Description:** Addr CS map LUT config register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30080
- **Exists:** DDRCTL_LUT_ADDRMAP==1

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

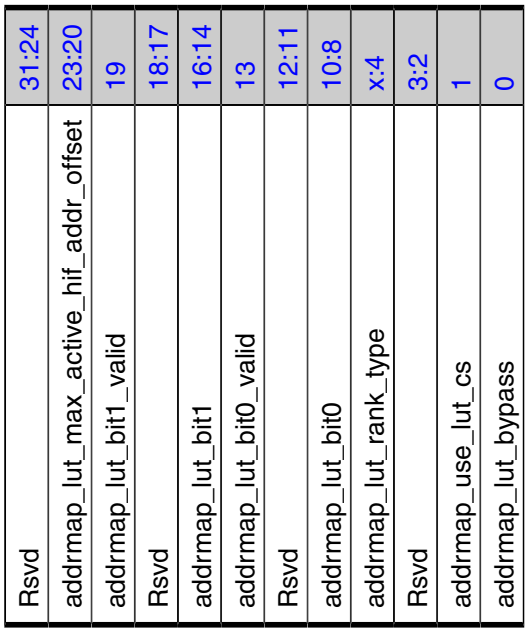


Table 3-329 Fields for Register: ADDRMAPLUTCFG

Bits	Name	Memory Access	Description
31:24			**Reserved Field:** Yes
23:20	addrmap_lut_max_active_hif_addr_offset	R/W	This register specifies the offset of maximum active width of HIF address from MEMC_HIF_ADDR_WIDTH. **Value After Reset:** 0x0 **Programming Mode:** Static
19	addrmap_lut_bit1_valid	R/W	Specify if addrmap_lut_bit1 is used. Note: Addrmap_lut_bit1 can only be used when addrmap_lut_bit0 is used. **Value After Reset:** 0x0 **Programming Mode:** Static
18:17			**Reserved Field:** Yes

Table 3-329 Fields for Register: ADDRMAPLUTCFG (continued)

Bits	Name	Memory Access	Description
16:14	addrmap_lut_bit1	R/W	The bit selection offset of the second lowest bit of LUT index. The bit1 selection valid range is [BIT1_BASE+:8] within the HIF address. Internal Bit1 Base: 7 Note: When addrmap_lut_bit1 and addrmap_lut_bit0 are used, addrmap_lut_bit1 must be equal or greater than addrmap_lut_bit0. **Value After Reset:** 0x0 **Programming Mode:** Static
13	addrmap_lut_bit0_valid	R/W	Specify if addrmap_lut_bit0 is used. **Value After Reset:** 0x0 **Programming Mode:** Static
12:11			**Reserved Field:** Yes
10:8	addrmap_lut_bit0	R/W	The bit selection offset of the lowest bit of LUT index. The bit0 selection valid range is [BIT0_BASE+:8] within the HIF address. Internal Bit0 Base: 6 **Value After Reset:** 0x0 **Programming Mode:** Static
x:4	addrmap_lut_rank_type	R/W	Select one mapping from the two settings of second level mapper. Each bit corresponds to each rank. ■ 0: Uses address mapping 0 ■ 1: Uses address mapping 1 **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 3
3:2			**Reserved Field:** Yes
1	addrmap_use_lut_cs	R/W	Set it to 1 to use the CS Map LUT design to get corresponding CS. Assert only if addr_map_lut_bypass = 0. **Value After Reset:** 0x0 **Programming Mode:** Static
0	addrmap_lut_bypass	R/W	Set it to 0 to use the remapped address from LUT in second level mapper. Set it to 1 to bypass the output of LUT. Only the legacy address mapping will take effects on the mapping from HIF address to DDR physical address. **Value After Reset:** 0x1 **Programming Mode:** Static

3.5.14 ADDRMAPLUTCTRL

- **Name:** Addr CS map LUT control register
- **Description:** Addr CS map LUT control register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30084
- **Exists:** DDRCTL_LUT_ADDRMAP==1

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

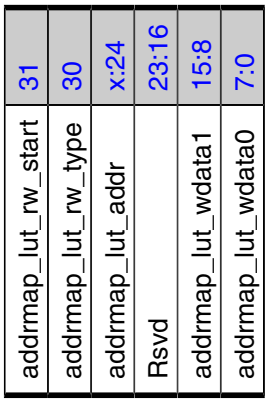


Table 3-330 Fields for Register: ADDRMAPLUTCTRL

Bits	Name	Memory Access	Description
31	addrmap_lut_rw_start	R/W1C	Set this bit to 1 to trigger a LUT Read/Write Operation. This bit is self-cleared. **Value After Reset:** 0x0 **Programming Mode:** Dynamic
30	addrmap_lut_rw_type	R/W	LUT read/write operation type. ■ 0: Indicate a read operation. The return data from LUT[ADDR] will be loaded into ADDRMAPLUTRDATA register. ■ 1: Indicates a write operation. The data of addrmap_lut_wdata1/addrmap_lut_wdata0 will be written into LUT[ADDR]. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

Table 3-330 Fields for Register: ADDRMAPLUTCTRL (continued)

Bits	Name	Memory Access	Description
x:24	addrmap_lut_addr	R/W	LUT entry Read/Write address. Notes: 1. For read operation, the ADDR shall be even. Two LUT entries will be loaded into ADDRMAP_LUT_RDATA registers 2. For write operation, the ADDR shall be even. Two entries will be written into the LUT **Value After Reset:** 0x0 **Programming Mode:** Dynamic **Range Variable[x]:** "DDRCTL_LUT_ADDRMAP_CS_WIN_BITS" + 23
23:16			**Reserved Field:** Yes
15:8	addrmap_lut_wdata1	R/W	8 bits entry data to be written to LUT[addrmap_lut_addr+1]. ■ [7]: Entry Valid. 1 - valid, 0 - invalid. ■ [6:5]: CSn[1:0], mapped corresponding CS for LUT output. ■ [DDRCTL_LUT_CS_WIN_BITS-1:0]: Mapped_addr[4:0], mapped address **Value After Reset:** 0x0 **Programming Mode:** Dynamic
7:0	addrmap_lut_wdata0	R/W	8 bits entry data to be written to LUT[addrmap_lut_addr]. ■ [7]: Entry Valid. 1 indicates that entry is used for LUT address mapping. ■ [6:5]: CSn[1:0], mapped corresponding CS for LUT output. ■ [DDRCTL_LUT_CS_WIN_BITS-1:0]: The most significant bits in the remapping address for one corresponding rank. **Value After Reset:** 0x0 **Programming Mode:** Dynamic

3.5.15 ADDRMAPLUTRDATA

- **Name:** Addr CS map LUT read data register
- **Description:** Addr CS map LUT read data register
- **Access Type:** DDRCTL_CHB_RME_EN ? {Root} : {Non-secure}
- **Size:** 32 bits
- **Offset:** 0x30088
- **Exists:** DDRCTL_LUT_ADDRMAP==1

This register is in block REGB_ADDR_MAP0.
Note: This register requires root APB accesses when APB5 is enabled, non-secure APB accesses when APB4 is enabled

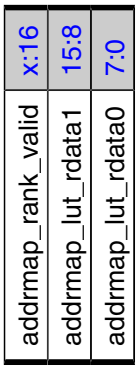


Table 3-331 Fields for Register: ADDRMAPLUTRDATA

Bits	Name	Memory Access	Description
x:16	addrmap_rank_valid	R	Present rank valid value based on rank status. Each bit corresponds each rank. **Value After Reset:** 0x0 **Programming Mode:** Static **Range Variable[x]:** "MEMC_NUM_RANKS" + 15
15:8	addrmap_lut_rdata1	R	The read-only register to store LUT[ADDRMAPLUTCTRL.addrmap_lut_addr+1] of previous LUT read operation. **Value After Reset:** 0x0 **Programming Mode:** Static
7:0	addrmap_lut_rdata0	R	The read-only register to store LUT[ADDRMAPLUTCTRL.addrmap_lut_addr] of previous LUT read operation. **Value After Reset:** 0x0 **Programming Mode:** Static

A

Internal Parameter Descriptions

Provides a description of the internal parameters that might be indirectly referenced in expressions in the Signals, Parameters, or Registers chapters. These parameters are not visible in the coreConsultant GUI and most of them are derived automatically from visible parameters.**You must not set any of these parameters directly.**

Some expressions might refer to TCL functions or procedures (sometimes identified as **function_of**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the core in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

Table A-1 Internal Parameters

Parameter Name	Equals To
AXI_ADDR_BOUNDARY	UMCTL2_AXI_ADDR_BOUNDARY
AXI_BURSTW	2
AXI_CACHEW	4
AXI_PROTW	3
AXI_QOSW	4
AXI_RESPW	2
AXI_SIZEW	3
AXI_USERW	UMCTL2_AXI_USER_WIDTH_INT
BL16	0x8
BL32	0x10
BL8	0x4
CID_WIDTH	((UMCTL2_CID_WIDTH!=0)?UMCTL2_CID_WIDTH:1)
DDRCTL_1DDRC_2DFI	(((DDRCTL_LPDDR == 1) && (MEMC_DRAM_DATA_WIDTH == 32)) ? 1 : 0)
DDRCTL_1DDRC_4DFI	(((DDRCTL_LPDDR == 1) && (MEMC_DRAM_DATA_WIDTH == 64)) ? 1 : 0)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
DDRCTL_APB4_EN	(DDRCTL_CHB_MPAM_EN == 1 || DDRCTL_CHB_TZ_EN == 1 || DDRCTL_APB5_EN == 1 || DDRCTL_SECURE == 1)
DDRCTL_APB5_EN	(DDRCTL_CHB_RME_EN == 1)
DDRCTL_ARB_OR_CHB_OR_HIF_SBR_EN	(UMCTL2_INCL_ARB_OR_CHB == 1 || DDRCTL_HIF_SBR_EN==1)
DDRCTL_ARB_OR_CHB_OR_HIF_SBR_EN_1	(DDRCTL_ARB_OR_CHB_OR_HIF_SBR_EN == 1 ? 1 : 0)
DDRCTL_BURST_LENGTH_X2	((MEMC_BURST_LENGTH == 32) && (DDRCTL_LPDDR == 1)) ? 1 : 0
DDRCTL_CHB_CHIF_EN	(DDRCTL_CHB_VERSION >= 5) && (DDRCTL_INCL_CHB==1)
DDRCTL_CHB_HIF_CRDT_CNT_WIDTH	(MEMC_NO_OF_MAX_ENTRY > 256 ? 10 : ((MEMC_NO_OF_MAX_ENTRY > 128) ? 9 : (MEMC_NO_OF_MAX_ENTRY > 64 ? 8 : 7)))
DDRCTL_CHB_SAR_BW	(THEREIS_SAR==1) ? (DDRCTL_CHB_ADRW - UMCTL2_SAR_MIN_ADDRW) : 1
DDRCTL_CHB_SAR_REG_BW	(DDRCTL_CHB_SAR_BW==1) ? 2 : DDRCTL_CHB_SAR_BW
DDRCTL_CHB_SAR_SW	(THEREIS_SAR==1) ? 8 : 1
DDRCTL_CLK_GATE_TE	(DDRCTL_CLK_GATE_TE_EN==1)
DDRCTL_CLK_GATE_TE_OR_ARB	((DDRCTL_CLK_GATE_TE==1) || (DDRCTL_CLK_GATE_ARB==1))
DDRCTL_DCH1_RDATARAM_OPT	(DDRCTL_DDR_DCH_HBW==1 && UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==1)
DDRCTL_DDR	((DDRCTL_PRODUCT_NAME == 1 || DDRCTL_PRODUCT_NAME == 3 || DDRCTL_PRODUCT_NAME == 5 || DDRCTL_PRODUCT_NAME == 6 || DDRCTL_PRODUCT_NAME == 7 || DDRCTL_PRODUCT_NAME == 8) || (DDRCTL_PRODUCT_NAME == 9) || (DDRCTL_PRODUCT_NAME == 10) || (DDRCTL_PRODUCT_NAME == 11) || (DDRCTL_PRODUCT_NAME == 12) ? 1 :0)
DDRCTL_DDR4	(DDRCTL_DDR==1 && MEMC_DDR5_ONLY==0)
DDRCTL_DDR4_OR_LPDDR	(DDRCTL_DDR4==1 || DDRCTL_LPDDR==1)
DDRCTL_DDR4_OR_LPDDR__OR__UMCTL2_REF_ZQ_IO	((DDRCTL_DDR4_OR_LPDDR==1) || (UMCTL2_REF_ZQ_IO==1))
DDRCTL_DDR5CTL	((DDRCTL_PRODUCT_NAME==9) || (DDRCTL_PRODUCT_NAME==10) || (DDRCTL_PRODUCT_NAME==11) || (DDRCTL_PRODUCT_NAME==12) ? 1 : 0)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
DDRCTL_DDR_DRAM_DATA_WIDTH	((MEMC_DRAM_DATA_WIDTH % 16) ? (MEMC_DRAM_DATA_WIDTH-8) : MEMC_DRAM_DATA_WIDTH)
DDRCTL_DDR_DRAM_ECC_WIDTH	((MEMC_DRAM_DATA_WIDTH % 16) ? 8 : MEMC_DRAM_ECC_WIDTH)
DDRCTL_DDR_DUAL_CHANNEL	((DDRCTL_DDR==1) && (UMCTL2_DUAL_CHANNEL==1))
DDRCTL_DDR_DUAL_CHANNEL__OR__SINGLE_INST_DUALCH	(DDRCTL_DDR_DUAL_CHANNEL==1 || DDRCTL_SINGLE_INST_DUALCH==1)
DDRCTL_DDR_DUAL_CHANNEL__OR__SINGLE_INST_DUALCH_EN	(DDRCTL_DDR_DUAL_CHANNEL__OR__SINGLE_INST_DUALCH==1)
DDRCTL_DDR_DUAL_DFI_DATA	((DDRCTL_DDR_PHY_DUAL_DFI_DATA==1) && (DDRCTL_DDR_DUAL_CHANNEL==1))
DDRCTL_DDR_EN	(DDRCTL_DDR)
DDRCTL_DDR_OR_MEMC_LPDDR4	(MEMC_DDR5==1 || DDRCTL_LPDDR==1) ? 1 : 0
DDRCTL_DFI0_CS_WIDTH	(((MEMC_NUM_RANKS << UMCTL2_SHARED_AC_EN) > 4) ? 4 : (MEMC_NUM_RANKS << UMCTL2_SHARED_AC_EN))
DDRCTL_DFI_CTRLMSG	(DDRCTL_LPDDR==1 && !(UMCTL2_HWFFC_EN==1 && DDRCTL_PPT2==1))
DDRCTL_DFI_DATA_WIDTH	(DDRCTL_DDR == 1) ? ((((DDRCTL_DDR_DRAM_DATA_WIDTH >> DDRCTL_DDR_DCH_HBW) + DDRCTL_DDR_DRAM_ECC_WIDTH) << (DDRCTL_DDR_DUAL_CHANNEL__OR__SINGLE_INST_DUALCH_EN + 1))>>(DDRCTL_DDR_PHY_DUAL_DFI_DATA)) : ((MEMC_DRAM_TOTAL_DATA_WIDTH*2) / UMCTL2_NUM_DFI)
DDRCTL_DFI_SB_WDT_OR_MEMC_DDR5	((MEMC_DDR5==1) || (DDRCTL_DFI_SB_WDT==1))
DDRCTL_EAPAR_EN	0
DDRCTL_EAPAR_EN_1	(DDRCTL_EAPAR_EN==1)
DDRCTL_ENHANCED_WCK	((DDRCTL_LPDDR==1) && (MEMC_NUM_RANKS>1))
DDRCTL_EXTRA_CLK_APB	(DDRCTL_EXTRA_CLK_APB_EN==1)
DDRCTL_EXT_RAS_LOG_EN	0
DDRCTL_FREQUENCY_BITS	((UMCTL2_FREQUENCY_NUM <= 2) ? 1 : (UMCTL2_FREQUENCY_NUM <= 4) ? 2 : (UMCTL2_FREQUENCY_NUM <= 8) ? 3 : 4)
DDRCTL_HET_CAM	0
DDRCTL_HIF_KBD_WIDTH	(MEMC_DFI_DATA_WIDTH/DDRCTL_NUM_BITS_PER_KBD)
DDRCTL_HIF_SBR_EN	(UMCTL2_SBR_EN==1&& DDRCTL_SYS_INTF==0)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
DDRCTL_HIF_SBR_EN_1	(DDRCTL_HIF_SBR_EN == 1 ? 1 : 0)
DDRCTL_HWFFC_EXT	(((UMCTL2_HWFFC_EN==1) && (UMCTL2_FREQUENCY_NUM>4)) ? 1 : 0)
DDRCTL_HWFFC_EXT_AND_LPDDR5X	(((DDRCTL_HWFFC_EXT==1) && (MEMC_LPDDR5X==1)) ? 1 : 0)
DDRCTL_INCL_CHB	DDRCTL_SYS_INTF == 2
DDRCTL_INST_DFI0_CS_WIDTH	(DDRCTL_SINGLE_INST_DUALCH == 1 ? MEMC_NUM_RANKS : DDRCTL_DFI0_CS_WIDTH)
DDRCTL_INST_DFI_DATAEN_WIDTH	(DDRCTL_INST_DFI_DATA_WIDTH / 16)
DDRCTL_INST_DFI_DATA_WIDTH	(DDRCTL_SINGLE_INST_DUALCH == 1) ? (MEMC_DRAM_TOTAL_DATA_WIDTH*2) : (DDRCTL_DFI_DATA_WIDTH)
DDRCTL_INST_DFI_MASK_WIDTH	(DDRCTL_INST_DFI_DATA_WIDTH / 8)
DDRCTL_KBD_ECC_BYP_EN	0
DDRCTL_KBD_ECC_EN	((DDRCTL_CHB_POIS_EN==1) && (DDRCTL_KBD_ECC_BYP_EN==0))
DDRCTL_KBD_SBECC_EN	((DDRCTL_KBD_ECC_EN==1) || (DDRCTL_KBD_ECC_BYP_EN==1))
DDRCTL_KBD_SBECC_EN_1	(DDRCTL_KBD_SBECC_EN==1)
DDRCTL_LLC	((DDRCTL_PRODUCT_NAME==8) ? 1 : 0)
DDRCTL_LPDDR	((DDRCTL_PRODUCT_NAME == 0 || DDRCTL_PRODUCT_NAME == 2 || DDRCTL_PRODUCT_NAME == 4 || DDRCTL_PRODUCT_NAME == 13 || DDRCTL_PRODUCT_NAME == 14 || DDRCTL_PRODUCT_NAME == 15) ? 1 :0)
DDRCTL_LPDDR5_PPR_OR_DDRCTL_DDR4_PPR	(((DDRCTL_LPDDR5_PPR == 1) || (DDRCTL_DDR4_PPR == 1)))
DDRCTL_LPDDR_OR_DDR4_PINS	(DDRCTL_LPDDR | DDRCTL_DDR4_PINS)
DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA	(DDRCTL_LPDDR | DDRCTL_DDR_DUAL_DFI_DATA)
DDRCTL_LPDDR_RFM	((DDRCTL_LPDDR == 1 && DDRCTL_HW_RFM_CTRL == 1) ? 1 : 0)
DDRCTL_LPDDR_RFMSBC_EN	(DDRCTL_LPDDR_RFMSBC)
DDRCTL_LUT_ADDRMAP_CS_WIN_BITS	5
DDRCTL_MRWBUF_DATA_WIDTH	22
DDRCTL_MRWBUF_DEPTH	(UMCTL2_FREQUENCY_NUM * DDRCTL_MRWBUF_NUM_PER_FREQ)
DDRCTL_MRWBUF_DEPTH_LOG2	[function_of: DDRCTL_MRWBUF_DEPTH]
DDRCTL_MRWBUF_NUM_PER_FREQ	64
DDRCTL_OCSAP_EN_1	(DDRCTL_OCSAP_EN == 1 ? 1 : 0)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
DDRCTL_PPT2	((DDRCTL_LPDDR==1) && (MEMC_FREQ_RATIO==4))
DDRCTL_SAR_REG_BW	(DDRCTL_INCL_CHB) ? DDRCTL_CHB_SAR_REG_BW : UMCTL2_AXI_SAR_REG_BW
DDRCTL_SAR_SW	(DDRCTL_INCL_CHB) ? DDRCTL_CHB_SAR_SW : UMCTL2_AXI_SAR_SW
DDRCTL_SECURE	((DDRCTL_PRODUCT_NAME==11) || (DDRCTL_PRODUCT_NAME==12) ? 1 : 0)
DDRCTL_UMCTL5	1
DDRCTL_VER_NUMBER_VAL	0x3136302a
DDRCTL_VER_TYPE_VAL	0x6c633030
DFI_LP_WAKEUP_PD_WIDTH	5
FBW	0x0
HBW	0x1
HIF_RQOS_TW	UMCTL2_XPI_RQOS_TW
HPR	0x1
HWFFC_MRWBUF_ADDR_WIDTH	(DDRCTL_MRWBUF_DEPTH_LOG2-DDRCTL_FREQUENCY_BITS)
HWFFC_MRWBUF_SELECT_WIDTH	DDRCTL_FREQUENCY_BITS
HWFFC_MRWBUF_WDATA_WIDTH	DDRCTL_MRWBUF_DATA_WIDTH
LPDDR45_DQSOSC	((DDRCTL_LPDDR==1) && (MEMC_FREQ_RATIO==4))
LPDDR45_DQSOSC_EN	(LPDDR45_DQSOSC)
LPDDR54_DQOSC_EN_OR_MEMC_DDR5	((LPDDR45_DQSOSC) || (MEMC_DDR5==1))
LPR	0x0
MEMC_ACT_BYPASS	MEMC_BYPASS
MEMC_ADDR_ERR_EN	1
MEMC_BANK_BITS	(DDRCTL_DDR == 1 ? 2 : 3)
MEMC_BG_BANK_BITS	(DDRCTL_LPDDR == 1 || MEMC_DDR4_BG_BITS2_INTERNAL_TESTING == 1 ? 4 : 5)
MEMC_BG_BITS	(DDRCTL_LPDDR == 1 || MEMC_DDR4_BG_BITS2_INTERNAL_TESTING == 1 ? 2 : 3)
MEMC_BURST_LENGTH_32	(MEMC_BURST_LENGTH == 32) ? 1 : 0
MEMC_BYPASS	0
MEMC_DDR4_BG_BITS2_INTERNAL_TESTING	((DDRCTL_DDR == 1 && MEMC_BURST_LENGTH == 8) ? 1 : 0)
MEMC_DDR4_EN	(DDRCTL_DDR)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
MEMC_DDR5	(((DDRCTL_DDR==1)&& (MEMC_BURST_LENGTH==16)&& (MEMC_ENH_RDWR_SWITCH==1)) ? 1 : 0)
MEMC_DDR5_ONLY	(((DDRCTL_LLC==1)||(DDRCTL_DDR5CTL==1)) ? 1 : 0)
MEMC_DFI_ADDR_WIDTH	(DDRCTL_LPDDR_OR_DDR_DUAL_DFI_DATA == 1) ? 14 : (DDRCTL_DDR==1 && DDRCTL_DDR4_PINS==1) ? 18 : 14
MEMC_DFI_ADDR_WIDTH_P0	(DDRCTL_LPDDR == 1) ? 14 : (DDRCTL_DDR == 1) ? MEMC_DFI_ADDR_WIDTH : MEMC_DFI_ADDR_WIDTH
MEMC_DFI_DATA_WIDTH	(MEMC_FREQ_RATIO == 2) ? MEMC_DRAM_DATA_WIDTH*4 : MEMC_DRAM_DATA_WIDTH*8
MEMC_DFI_ECC_WIDTH	(MEMC_FREQ_RATIO == 2 ? MEMC_DRAM_ECC_WIDTH * 4 : MEMC_DRAM_ECC_WIDTH * 8)
MEMC_DRAM_DATA_WIDTH_64_OR_32__OR__MEMC_INLINE_ECC	(MEMC_DRAM_DATA_WIDTH==64 || MEMC_DRAM_DATA_WIDTH==32 || MEMC_INLINE_ECC_EN==1) ? 1 : 0
MEMC_DRAM_DATA_WIDTH_64_OR_MEMC_INLINE_ECC	(MEMC_DRAM_DATA_WIDTH==64 || MEMC_INLINE_ECC_EN==1) ? 1 : 0
MEMC_DRAM_ECC_WIDTH	(MEMC_SIDEBAND_ECC_EN==1 ? 8 : 0)
MEMC_DRAM_NBYTES	(MEMC_DRAM_DATA_WIDTH/8)
MEMC_DRAM_NBYTES_LG2	[function_of: MEMC_DRAM_NBYTES]
MEMC_DRAM_TOTAL_DATA_WIDTH	MEMC_DRAM_DATA_WIDTH + MEMC_DRAM_ECC_WIDTH+0
MEMC_ECC	(MEMC_ECC_SUPPORT > 0)
MEMC_ECCAP	((MEMC_INLINE_ECC == 1 && DDRCTL_LPDDR == 1) ? 1 : 0)
MEMC_ENH_CAM_PTR	1
MEMC_ENH_RDWR_SWITCH	(MEMC_ENH_CAM_PTR+0)
MEMC_FREQ_RATIO	(DDRCTL_LLC==1 ? 2 : 4)
MEMC_HIF_ADDR_WIDTH	(UMCTL2_LRANK_BITS + UMCTL2_DATA_CHANNEL_INTERLEAVE_EN + (MEMC_DDR4_BG_BITS2_INTERNAL_TESTING == 1 ? 33 : (DDRCTL_DDR == 1) ? 34 : (DDRCTL_LPDDR == 1) ? 32 : MEMC_HIF_MIN_ADDR_WIDTH))
MEMC_HIF_ADDR_WIDTH_MAX	(UMCTL2_DATA_CHANNEL_INTERLEAVE_EN==1 && UMCTL2_NUM_LRANKS_TOTAL==64) ? 41 : 40
MEMC_HIF_CMD_WDATA_MASK_FULL_EN	((SNPS_RSVDPARAM_518==1 && DDRCTL_LPDDR==1) || MEMC_INLINE_ECC_EN==1) ? 1 : 0
MEMC_HIF_CREDIT_BITS	(MEMC_INLINE_ECC_EN==1) ? 2 : 1
MEMC_HIF_MIN_ADDR_WIDTH	32

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
MEMC_INLINE_ECC	MEMC_INLINE_ECC_EN
MEMC_INLINE_ECC_EN	(MEMC_INLINE_ECC+0)
MEMC_LPDDR4_OR_UMCTL2_CID_EN	(DDRCTL_LPDDR==1 || UMCTL2_CID_EN==1) ? 1 : 0
MEMC_LPDDR5X	(((DDRCTL_PRODUCT_NAME==13) || (DDRCTL_PRODUCT_NAME==14) || (DDRCTL_PRODUCT_NAME==15)) ? 1 : 0)
MEMC_MAX_INLINE_ECC_PER_BURST	((MEMC_DRAM_DATA_WIDTH * MEMC_BURST_LENGTH)/64)
MEMC_MAX_INLINE_ECC_PER_BURST_BITS	((MEMC_MAX_INLINE_ECC_PER_BURST == 2) ? 1 : ((MEMC_MAX_INLINE_ECC_PER_BURST == 4) ? 2 : ((MEMC_MAX_INLINE_ECC_PER_BURST == 8) ? 3 : ((MEMC_MAX_INLINE_ECC_PER_BURST == 16) ? 4 : 5))))
MEMC_MRR_DATA_TOTAL_DATA_WIDTH	(DDRCTL_DDR == 1 ? MEMC_DFI_TOTAL_DATA_WIDTH : MEMC_DRAM_TOTAL_DATA_WIDTH)
MEMC_NO_OF_MAX_ENTRY	(MEMC_NO_OF_WR_ENTRY >= MEMC_NO_OF_RD_ENTRY) ? MEMC_NO_OF_WR_ENTRY : MEMC_NO_OF_RD_ENTRY
MEMC_NUM_CLKS	(DDRCTL_DDR == 1 ? 4 : 1)
MEMC_NUM_RANKS_GT_1	(MEMC_NUM_RANKS > 1) ? 1 : 0
MEMC_OPT_TIMING	1
MEMC_OPT_WDATARAM	(DDRCTL_DDR_DCH_HBW == 1 ? 1 : 0)
MEMC_PAGE_BITS	(DDRCTL_DDR_EN == 1) ? 18 : 18
MEMC_QBUS_SUPPORT	(((MEMC_DRAM_DATA_WIDTH%32==0) ||(MEMC_DRAM_DATA_WIDTH==40) ||(MEMC_DRAM_DATA_WIDTH==72)) && (DDRCTL_PBW_MODE_SUPPORT==0))
MEMC_RANKBANK_BITS	UMCTL2_LRANK_BITS + MEMC_BG_BANK_BITS
MEMC_RANK_BITS	((MEMC_NUM_RANKS == 1) ? 0 : ((MEMC_NUM_RANKS == 2) ? 1 : 2))
MEMC_RD_BYPASS	MEMC_BYPASS
MEMC_RDCMD_ENTRY_BITS	(MEMC_NO_OF_RD_ENTRY > 128 ? 8 : (MEMC_NO_OF_RD_ENTRY > 64 ? 7 : (MEMC_NO_OF_RD_ENTRY == 64 ? 6 : (MEMC_NO_OF_RD_ENTRY == 32 ? 5 : 4))))
MEMC_RDWR_SWITCH_POL_SEL	0
MEMC_SIDEBAND_ECC	MEMC_SIDEBAND_ECC_EN
MEMC_SIDEBAND_ECC_EN	(MEMC_SIDEBAND_ECC+0)
MEMC_WRCMD_ENTRY_BITS	(MEMC_NO_OF_WR_ENTRY > 256 ? 9 : (MEMC_NO_OF_WR_ENTRY > 128 ? 8 :

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
	(MEMC_NO_OF_WR_ENTRY > 64 ? 7 : (MEMC_NO_OF_WR_ENTRY == 64 ? 6 : (MEMC_NO_OF_WR_ENTRY == 32 ? 5 : 4)))))
MEMC_WRDATA_4_CYCLES	(MEMC_WRDATA_CYCLES == 4) ? 1 : 0
MEMC_WRDATA_8_CYCLES	0
MEMC_WRDATA_CYCLES	(MEMC_BURST_LENGTH/(MEMC_FREQ_RATIO*2))
NPORTS	UMCTL2_A_NPORTS
OCPAR_ADDR_PARITY_WIDTH	UMCTL2_OCPAR_ADDR_PARITY_W
QBW	0x2
SELFREF_TYPE_WIDTH	((DDRCTL_DDR_EN==1)?(MEMC_NUM_RANKS*2):2)
SNPS_RSVDPARAM_518	0
SNPS_RSVDPARAM_655	0
SNPS_RSVDPARAM_657	(DDRCTL_LPDDR)
SNPS_RSVDPARAM_666	(DDRCTL_LPDDR)
TARGET_FREQUENCY_WIDTH	DDRCTL_FREQUENCY_BITS
THEREIS_AXI4_PORT	((UMCTL2_INCL_ARB == 1) && ((UMCTL2_A_TYPE_0 == 3 || (UMCTL2_A_TYPE_1 == 3 && (UMCTL2_A_NPORTS > 1)) || (UMCTL2_A_TYPE_2 == 3 && (UMCTL2_A_NPORTS > 2)) || (UMCTL2_A_TYPE_3 == 3 && (UMCTL2_A_NPORTS > 3)) || (UMCTL2_A_TYPE_4 == 3 && (UMCTL2_A_NPORTS > 4)) || (UMCTL2_A_TYPE_5 == 3 && (UMCTL2_A_NPORTS > 5)) || (UMCTL2_A_TYPE_6 == 3 && (UMCTL2_A_NPORTS > 6)) || (UMCTL2_A_TYPE_7 == 3 && (UMCTL2_A_NPORTS > 7)) || (UMCTL2_A_TYPE_8 == 3 && (UMCTL2_A_NPORTS > 8)) || (UMCTL2_A_TYPE_9 == 3 && (UMCTL2_A_NPORTS > 9)) || (UMCTL2_A_TYPE_10 == 3 && (UMCTL2_A_NPORTS > 10)) || (UMCTL2_A_TYPE_11 == 3 && (UMCTL2_A_NPORTS > 11)) || (UMCTL2_A_TYPE_12 == 3 && (UMCTL2_A_NPORTS > 12)) || (UMCTL2_A_TYPE_13 == 3 && (UMCTL2_A_NPORTS > 13)) || (UMCTL2_A_TYPE_14 == 3 && (UMCTL2_A_NPORTS > 14)) || (UMCTL2_A_TYPE_15 == 3 && (UMCTL2_A_NPORTS > 15))))) ? 1 : 0
THEREIS_AXI_PORT	((UMCTL2_INCL_ARB == 1) && (((UMCTL2_A_TYPE_0 == 1 || UMCTL2_A_TYPE_0 == 3) || ((UMCTL2_A_TYPE_1 == 1 || UMCTL2_A_TYPE_1 == 3) && (UMCTL2_A_NPORTS > 1)) || ((UMCTL2_A_TYPE_2 == 1 || UMCTL2_A_TYPE_2 == 3) && (UMCTL2_A_NPORTS > 2)) || ((UMCTL2_A_TYPE_3 == 1 || UMCTL2_A_TYPE_3 == 3) && (UMCTL2_A_NPORTS > 3)) || ((UMCTL2_A_TYPE_4 == 1 || UMCTL2_A_TYPE_4 == 3) && (UMCTL2_A_NPORTS > 4)) ||

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
	((UMCTL2_A_TYPE_5 == 1 || UMCTL2_A_TYPE_5 == 3) && (UMCTL2_A_NPORTS > 5)) || ((UMCTL2_A_TYPE_6 == 1 || UMCTL2_A_TYPE_6 == 3) && (UMCTL2_A_NPORTS > 6)) || ((UMCTL2_A_TYPE_7 == 1 || UMCTL2_A_TYPE_7 == 3) && (UMCTL2_A_NPORTS > 7)) || ((UMCTL2_A_TYPE_8 == 1 || UMCTL2_A_TYPE_8 == 3) && (UMCTL2_A_NPORTS > 8)) || ((UMCTL2_A_TYPE_9 == 1 || UMCTL2_A_TYPE_9 == 3) && (UMCTL2_A_NPORTS > 9)) || ((UMCTL2_A_TYPE_10 == 1 || UMCTL2_A_TYPE_10 == 3) && (UMCTL2_A_NPORTS > 10)) || ((UMCTL2_A_TYPE_11 == 1 || UMCTL2_A_TYPE_11 == 3) && (UMCTL2_A_NPORTS > 11)) || ((UMCTL2_A_TYPE_12 == 1 || UMCTL2_A_TYPE_12 == 3) && (UMCTL2_A_NPORTS > 12)) || ((UMCTL2_A_TYPE_13 == 1 || UMCTL2_A_TYPE_13 == 3) && (UMCTL2_A_NPORTS > 13)) || ((UMCTL2_A_TYPE_14 == 1 || UMCTL2_A_TYPE_14 == 3) && (UMCTL2_A_NPORTS > 14)) || ((UMCTL2_A_TYPE_15 == 1 || UMCTL2_A_TYPE_15 == 3) &&
THEREIS_AXI_PORT ...(cont.)	(UMCTL2_A_NPORTS > 15))))) ? 1 : 0
THEREIS_PORT_DSIZE	((UMCTL2_INCL_ARB == 1) && ((UMCTL2_PORT_DSIZE_0 == 1 || (UMCTL2_PORT_DSIZE_1 == 1 && (UMCTL2_A_NPORTS > 1)) || (UMCTL2_PORT_DSIZE_2 == 1 && (UMCTL2_A_NPORTS > 2)) || (UMCTL2_PORT_DSIZE_3 == 1 && (UMCTL2_A_NPORTS > 3)) || (UMCTL2_PORT_DSIZE_4 == 1 && (UMCTL2_A_NPORTS > 4)) || (UMCTL2_PORT_DSIZE_5 == 1 && (UMCTL2_A_NPORTS > 5)) || (UMCTL2_PORT_DSIZE_6 == 1 && (UMCTL2_A_NPORTS > 6)) || (UMCTL2_PORT_DSIZE_7 == 1 && (UMCTL2_A_NPORTS > 7)) || (UMCTL2_PORT_DSIZE_8 == 1 && (UMCTL2_A_NPORTS > 8)) || (UMCTL2_PORT_DSIZE_9 == 1 && (UMCTL2_A_NPORTS > 9)) || (UMCTL2_PORT_DSIZE_10 == 1 && (UMCTL2_A_NPORTS > 10)) || (UMCTL2_PORT_DSIZE_11 == 1 && (UMCTL2_A_NPORTS > 11)) || (UMCTL2_PORT_DSIZE_12 == 1 && (UMCTL2_A_NPORTS > 12)) || (UMCTL2_PORT_DSIZE_13 == 1 && (UMCTL2_A_NPORTS > 13)) || (UMCTL2_PORT_DSIZE_14 == 1 && (UMCTL2_A_NPORTS > 14)) || (UMCTL2_PORT_DSIZE_15 == 1 && (UMCTL2_A_NPORTS > 15))))) ? 1 : 0

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
THEREIS_PORT_USIZE	((UMCTL2_INCL_ARB == 1) && ((UMCTL2_PORT_USIZE_0 == 1 || (UMCTL2_PORT_USIZE_1 == 1 && (UMCTL2_A_NPORTS > 1)) || (UMCTL2_PORT_USIZE_2 == 1 && (UMCTL2_A_NPORTS > 2)) || (UMCTL2_PORT_USIZE_3 == 1 && (UMCTL2_A_NPORTS > 3)) || (UMCTL2_PORT_USIZE_4 == 1 && (UMCTL2_A_NPORTS > 4)) || (UMCTL2_PORT_USIZE_5 == 1 && (UMCTL2_A_NPORTS > 5)) || (UMCTL2_PORT_USIZE_6 == 1 && (UMCTL2_A_NPORTS > 6)) || (UMCTL2_PORT_USIZE_7 == 1 && (UMCTL2_A_NPORTS > 7)) || (UMCTL2_PORT_USIZE_8 == 1 && (UMCTL2_A_NPORTS > 8)) || (UMCTL2_PORT_USIZE_9 == 1 && (UMCTL2_A_NPORTS > 9)) || (UMCTL2_PORT_USIZE_10 == 1 && (UMCTL2_A_NPORTS > 10)) || (UMCTL2_PORT_USIZE_11 == 1 && (UMCTL2_A_NPORTS > 11)) || (UMCTL2_PORT_USIZE_12 == 1 && (UMCTL2_A_NPORTS > 12)) || (UMCTL2_PORT_USIZE_13 == 1 && (UMCTL2_A_NPORTS > 13)) || (UMCTL2_PORT_USIZE_14 == 1 && (UMCTL2_A_NPORTS > 14)) || (UMCTL2_PORT_USIZE_15 == 1 && (UMCTL2_A_NPORTS > 15))))) ? 1 : 0
THEREIS_SAR	(UMCTL2_A_NSAR > 0) ? 1 : 0
THEREIS_USE2RAQ	(UMCTL2_TOT_USE2RAQ > 0) ? 1 : 0
tMRW	0x1
tMRW_L	0x2
tVRCG_DISABLE	0x4
tVRCG_ENABLE	0x5
UMCTL2_A_AXI	(THEREIS_AXI_PORT == 1) ? 1 : 0
UMCTL2_A_AXI_0	((UMCTL2_A_NPORTS >= (0+1)) && (UMCTL2_A_TYPE_0 == 1 || UMCTL2_A_TYPE_0 == 3) && (UMCTL2_INCL_ARB == 1)) ? 1 : 0
UMCTL2_A_DW	(MEMC_FREQ_RATIO == 4) ? (8*MEMC_DRAM_DATA_WIDTH) : ((MEMC_FREQ_RATIO == 2) ? (4*MEMC_DRAM_DATA_WIDTH) : (2*MEMC_DRAM_DATA_WIDTH))
UMCTL2_A_ID_MAPW	UMCTL2_A_IDW
UMCTL2_AP_ANY_ASYNC	(UMCTL2_USE_SCANMODE == 1)?1:0

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_APB_AW	24
UMCTL2_APB_DW	32
UMCTL2_A_SAR_0	(UMCTL2_A_NSAR >= (0+1)) ? 1 : 0
UMCTL2_AXI_ADDRW	((UMCTL2_A_ADDRW < UMCTL2_MIN_ADDRW) ? UMCTL2_MIN_ADDRW : UMCTL2_A_ADDRW)
UMCTL2_AXI_REGION_WIDTH	4
UMCTL2_AXI_SAR_BW	(THEREIS_SAR==1) ? (UMCTL2_A_ADDRW - UMCTL2_SAR_MIN_ADDRW) : 1
UMCTL2_AXI_SAR_REG_BW	(UMCTL2_AXI_SAR_BW==1) ? 2 : UMCTL2_AXI_SAR_BW
UMCTL2_AXI_SAR_SW	(THEREIS_SAR==1) ? 8 : 1
UMCTL2_AXI_USER_WIDTH_INT	(UMCTL2_AXI_USER_WIDTH > 0) ? UMCTL2_AXI_USER_WIDTH : 1
UMCTL2_CID_EN	(UMCTL2_CID_WIDTH>0)
UMCTL2_CMD_LEN_BITS	(MEMC_BURST_LENGTH != 8) ? 2 : 1
UMCTL2_DATA_CHANNEL_INTERLEAVE_EN_1	((UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 1) ? 1 : 0)
UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_0	((UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 1) && (UMCTL2_A_DW*2==UMCTL2_PORT_DW_0)) ? 1 : 0
UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_ANY_0	(((UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_0 == 1) || (UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_HBW_0 == 1) || (UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_QBW_0==1)) && (UMCTL2_A_AXI_0==1)) ? 1 : 0
UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_HBW_0	((UMCTL2_DATA_CHANNEL_INTERLEAVE_EN == 1) && (UMCTL2_A_DW==UMCTL2_PORT_DW_0) && (DDRCTL_PBW_MODE_SUPPORT!=2)) ? 1 : 0
UMCTL2_DATA_CHANNEL_INTERLEAVE_NS_QBW_0	0
UMCTL2_DATARAM_PAR_DW	(MEMC_DFI_DATA_WIDTH)/8
UMCTL2_DATARAM_PAR_DW_DCH1	(DDRCTL_DCH1_RDATARAM_OPT == 0) ? UMCTL2_DATARAM_PAR_DW : (UMCTL2_DATARAM_PAR_DW/2)
UMCTL2_DATARAM_PAR_DW_LG2	[function_of: UMCTL2_DATARAM_PAR_DW]
UMCTL2_DDR4_MRAM_EN	0
UMCTL2_DFI_MASK_PER_NIBBLE	0
UMCTL2_DUAL_DATA_CHANNEL	((UMCTL2_NUM_DATA_CHANNEL == 2) ? 1 : 0)
UMCTL2_DUAL_HIF_1	(UMCTL2_DUAL_HIF == 1) ? 1 : 0
UMCTL2_ECC_TEST_MODE_EN	(UMCTL2_INCL_ARB_OR_CHB == 0 && MEMC_SIDEBAND_ECC_EN==1) ? 1 : 0
UMCTL2_INCL_ARB	DDRCTL_SYS_INTF == 1

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_INCL_ARB_OR_CHB	DDRCTL_SYS_INTF != 0
UMCTL2_INT_NPORTS	(UMCTL2_A_NPORTS + UMCTL2_TOT_USE2RAQ + UMCTL2_SBR_EN)
UMCTL2_LPDDR4_DUAL_CHANNEL	((DDRCTL_LPDDR==1) && (UMCTL2_DUAL_CHANNEL==1))
UMCTL2_LRANK_BITS	((UMCTL2_NUM_LRANKS_TOTAL == 1) ? 0 : (UMCTL2_NUM_LRANKS_TOTAL == 2) ? 1 : (UMCTL2_NUM_LRANKS_TOTAL == 4) ? 2 : (UMCTL2_NUM_LRANKS_TOTAL == 8) ? 3 : (UMCTL2_NUM_LRANKS_TOTAL == 16) ? 4 : (UMCTL2_NUM_LRANKS_TOTAL == 32) ? 5 : 6)
UMCTL2_MAX_XPI_PORT_DW	[function_of: UMCTL2_A_NPORTS]
UMCTL2_MAX_XPI_PORT_DW_GTEQ_512	(UMCTL2_MAX_XPI_PORT_DW >= 512 ? 1 : 0)
UMCTL2_MIN_ADDRW	(MEMC_HIF_ADDR_WIDTH+MEMC_DRAM_NBYTES_LG2)
UMCTL2_NUM_DATA_CHANNEL	((UMCTL2_DUAL_CHANNEL == 1) ? 2 : 1)
UMCTL2_OCCAP_DDRC_INTERNAL_TESTING	0
UMCTL2_OCCAP_EN_1	(UMCTL2_OCCAP_EN == 1 ? 1 : 0)
UMCTL2_OCECC_EN_1	(UMCTL2_OCECC_EN == 1 ? 1 : 0)
UMCTL2_OCPAR_ADDR_LOG_HIGH_WIDTH	((UMCTL2_AXI_ADDRW > UMCTL2_OCPAR_ADDR_LOG_LOW_WIDTH) ? (UMCTL2_AXI_ADDRW - UMCTL2_OCPAR_ADDR_LOG_LOW_WIDTH) : 1)
UMCTL2_OCPAR_ADDR_LOG_LOW_WIDTH	32
UMCTL2_OCPAR_ADDR_PARITY_W	((UMCTL2_OCPAR_ADDR_PARITY_WIDTH == 0) ? 1 : [function_of:])
UMCTL2_OCPAR_EN_1	(UMCTL2_OCPAR_EN == 1 ? 1 : 0)
UMCTL2_OCPAR_OR_OCECC_EN_1	((UMCTL2_OCPAR_EN == 1) || (UMCTL2_OCECC_EN == 1))
UMCTL2_OCPAR_WDATA_OUT_ERR_WIDTH	(MEMC_INLINE_ECC_EN+1)
UMCTL2_PARTIAL_WR	(MEMC_BURST_LENGTH==8 && MEMC_FREQ_RATIO==4) ? 0 : 1
UMCTL2_PORT_CH0_0	(UMCTL2_NUM_VIR_CH_0 > 0 && UMCTL2_STATIC_VIR_CH_0 == 1) ? 1 : 0
UMCTL2_PORT_DSIZE_0	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_0!=0 && ((UMCTL2_PORT_DW_0>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_0>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_1	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_1!=0 &&

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
	((UMCTL2_PORT_DW_1>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_1>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_10	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_10!=0 && ((UMCTL2_PORT_DW_10>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_10>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_11	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_11!=0 && ((UMCTL2_PORT_DW_11>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_11>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_12	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_12!=0 && ((UMCTL2_PORT_DW_12>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_12>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_13	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_13!=0 && ((UMCTL2_PORT_DW_13>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_13>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_14	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_14!=0 && ((UMCTL2_PORT_DW_14>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_14>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_15	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_15!=0 && ((UMCTL2_PORT_DW_15>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_15>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_2	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_2!=0 && ((UMCTL2_PORT_DW_2>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_2>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_PORT_DSIZE_3	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_3!=0 && ((UMCTL2_PORT_DW_3>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_3>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_4	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_4!=0 && ((UMCTL2_PORT_DW_4>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_4>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_5	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_5!=0 && ((UMCTL2_PORT_DW_5>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_5>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_6	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_6!=0 && ((UMCTL2_PORT_DW_6>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_6>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_7	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_7!=0 && ((UMCTL2_PORT_DW_7>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_7>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_8	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_8!=0 && ((UMCTL2_PORT_DW_8>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_8>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_DSIZE_9	(UMCTL2_INCL_ARB== 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_9!=0 && ((UMCTL2_PORT_DW_9>UMCTL2_A_DW) || (DDRCTL_UMCTL5==1 && (UMCTL2_PORT_DW_9>(UMCTL2_A_DW/4))))) ? 1 : 0) : 5)
UMCTL2_PORT_EN_RESET_VALUE	0
UMCTL2_PORT_USIZE_0	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_0!=0 && UMCTL2_PORT_DW_0<UMCTL2_A_DW) ? 1 : 0) : 5)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_PORT_USIZE_1	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_1!=0 && UMCTL2_PORT_DW_1<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_10	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_10!=0 && UMCTL2_PORT_DW_10<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_11	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_11!=0 && UMCTL2_PORT_DW_11<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_12	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_12!=0 && UMCTL2_PORT_DW_12<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_13	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_13!=0 && UMCTL2_PORT_DW_13<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_14	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_14!=0 && UMCTL2_PORT_DW_14<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_15	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_15!=0 && UMCTL2_PORT_DW_15<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_2	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_2!=0 && UMCTL2_PORT_DW_2<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_3	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_3!=0 && UMCTL2_PORT_DW_3<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_4	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_4!=0 && UMCTL2_PORT_DW_4<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_5	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_5!=0 && UMCTL2_PORT_DW_5<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_6	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_6!=0 && UMCTL2_PORT_DW_6<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_7	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_7!=0 && UMCTL2_PORT_DW_7<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_8	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_8!=0 && UMCTL2_PORT_DW_8<UMCTL2_A_DW) ? 1 : 0) : 5)
UMCTL2_PORT_USIZE_9	(UMCTL2_INCL_ARB == 1 ? ((UMCTL2_INCL_ARB==1 && UMCTL2_A_TYPE_9!=0 && UMCTL2_PORT_DW_9<UMCTL2_A_DW) ? 1 : 0) : 5)

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_REF_ZQ_IO	0
UMCTL2_REGPAR_EN_1	(UMCTL2_REGPAR_EN == 1 ? 1 : 0)
UMCTL2_REG_SCRUB_INTERVALW	13
UMCTL2_RESET_WIDTH	1
UMCTL2_SAR_MIN_ADDRW	(UMCTL2_SARMINSIZE + 27)
UMCTL2_SBR_EN_1	(UMCTL2_SBR_EN == 1 ? 1 : 0)
UMCTL2_SHARED_AC_EN	(SNPS_RSVDPARAM_655)
UMCTL2_TOKENW	(MEMC_NO_OF_MAX_ENTRY > 256 ? 9 : (MEMC_NO_OF_MAX_ENTRY > 128 ? 8 : (MEMC_NO_OF_MAX_ENTRY > 64 ? 7 : (MEMC_NO_OF_MAX_ENTRY == 64 ? 6 : (MEMC_NO_OF_MAX_ENTRY == 32 ? 5 : 4)))))
UMCTL2_TOT_USE2RAQ	(UMCTL2_XPI_USE2RAQ_0 + UMCTL2_XPI_USE2RAQ_1 + UMCTL2_XPI_USE2RAQ_2 + UMCTL2_XPI_USE2RAQ_3 + UMCTL2_XPI_USE2RAQ_4 + UMCTL2_XPI_USE2RAQ_5 + UMCTL2_XPI_USE2RAQ_6 + UMCTL2_XPI_USE2RAQ_7 + UMCTL2_XPI_USE2RAQ_8 + UMCTL2_XPI_USE2RAQ_9 + UMCTL2_XPI_USE2RAQ_10 + UMCTL2_XPI_USE2RAQ_11 + UMCTL2_XPI_USE2RAQ_12 + UMCTL2_XPI_USE2RAQ_13 + UMCTL2_XPI_USE2RAQ_14 + UMCTL2_XPI_USE2RAQ_15)
UMCTL2_USE_SCANMODE	[function_of: UMCTL2_A_NPORTS UMCTL2_P_ASYNC_EN]
UMCTL2_VPR_EN	(UMCTL2_VPRW_EN == 1 ? 1 : 0)
UMCTL2_VPR_EN_VAL	(UMCTL2_VPR_EN)
UMCTL2_VPW_EN	(UMCTL2_VPRW_EN == 1 ? 1 : 0)
UMCTL2_WDATARAM_PAR_DW	(UMCTL2_OCECC_EN == 1) ? 5*(UMCTL2_WDATARAM_DW)/8 : (UMCTL2_WDATARAM_DW)/8
UMCTL2_WDATARAM_PAR_DW_EXT	(UMCTL2_OCECC_EN == 1) ? 5*(UMCTL2_WDATARAM_DW)/8 : (DDRCTL_OCSAP_EN == 1) ? (UMCTL2_WDATARAM_DW)/4 : (UMCTL2_WDATARAM_DW)/8
UMCTL2_XPI_RQOS_MLW	4
UMCTL2_XPI_RQOS_RW	2

Table A-1 Internal Parameters (continued)

Parameter Name	Equals To
UMCTL2_XPI_RQOS_TW	(UMCTL2_XPI_VPT_EN==1 || (UMCTL2_INCL_ARB==0 && UMCTL2_VPRW_EN==1)) ? 11 : 1
UMCTL2_XPI_USE_RMW	(((MEMC_ECC_SUPPORT>0 || DDRCTL_DDR==1 || DDRCTL_LPDDR==1) && MEMC_USE_RMW==1 && UMCTL2_INCL_ARB==1) ? 1 : 0)
UMCTL2_XPI_VPR_EN	(UMCTL2_INCL_ARB==1 && UMCTL2_VPR_EN==1) ? 1 : 0
UMCTL2_XPI_VPT_EN	(UMCTL2_XPI_VPR_EN==1 || UMCTL2_XPI_VPW_EN==1) ? 1 : 0
UMCTL2_XPI_VPW_EN	(UMCTL2_INCL_ARB==1 && UMCTL2_VPW_EN==1) ? 1 : 0
UMCTL2_XPI_WQOS_MLW	4
UMCTL2_XPI_WQOS_RW	2
UMCTL2_XPI_WQOS_TW	(UMCTL2_XPI_VPT_EN==1 || (UMCTL2_INCL_ARB==0 && UMCTL2_VPRW_EN==1)) ? 11 : 1
VPR	0x2
VPW	0x4
WR	0x3
WRDATA_CYCLES	MEMC_WRDATA_CYCLES