cādence®

SD 6.0 UHS-I CQ / eMMC 5.1 Host Controller IP

for

SD devices up to 6.1

SDIO devices up to 4.1

and eMMC devices up to 5.1

with SD/eMMC interface

Part Number: IP6061

IP Rev: R602- Doc Rev: 1.01

Integration Manual

2021-11-19

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders.

Restricted Permission: This document is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this document, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this document may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. This document contains the proprietary and confidential information of Cadence or its licensors, and is supplied subject to, and may be used only in accordance with, a written agreement between Cadence and its customer.

Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this document subject to the following conditions:

1. This document may not be modified in any way.
2. Any authorized copy of this document or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
3. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE AND DOES NOT REPRESENT A COMMITMENT ON THE PART OF CADENCE. EXCEPT AS MAY BE EXPLICITLY SET FORTH IN A WRITTEN AGREEMENT BETWEEN CADENCE AND ITS CUSTOMER, CADENCE DOES NOT MAKE, AND EXPRESSLY DISCLAIMS, ANY REPRESENTATIONS OR WARRANTIES AS TO THE COMPLETENESS, ACCURACY OR USEFULNESS OF THE INFORMATION CONTAINED IN THIS DOCUMENT. CADENCE DOES NOT WARRANT THAT USE OF SUCH INFORMATION WILL NOT INFRINGE ANY THIRD PARTY RIGHTS, AND CADENCE DISCLAIMS ALL IMPLIED WARRANTIES, INCLUDING MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. CADENCE DOES NOT ASSUME ANY LIABILITY FOR DAMAGES OR COSTS OF ANY KIND THAT MAY RESULT FROM USE OF SUCH INFORMATION. CADENCE CUSTOMER HAS COMPLETE CONTROL AND FINAL DECISION-MAKING AUTHORITY OVER ALL ASPECTS OF THE DEVELOPMENT, MANUFACTURE, SALE AND USE OF CUSTOMER'S PRODUCT, INCLUDING, BUT NOT LIMITED TO, ALL DECISIONS WITH REGARD TO DESIGN, PRODUCTION, TESTING, ASSEMBLY, QUALIFICATION, CERTIFICATION, INTEGRATION OF CADENCE PRODUCTS, INSTRUCTIONS FOR USE, LABELING AND DISTRIBUTION, AND CADENCE EXPRESSLY DISAVOWS ANY RESPONSIBILITY WITH REGARD TO ANY SUCH DECISIONS REGARDING CUSTOMER'S PRODUCT.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227- 14 and DFAR252.227-7013 et seq. or its successor.

Table of Contents

List of Tables

List of Figures

About this Document

This Integration Guide describes the interface and operational details for integration of the SD 6.0 UHS-I CQ / eMMC 5.1 Host Controller IP into a target design. The intended audience for this document is design engineers.

This document is organized as follows:

References and Related Documents

This guide references the following documents:

Table 1. References and Related Documents

Reference	Version/Description
SD Specifications - Part A2 SD Host Controller Standard Specification	version 6.00, 2017-12-12, SD Card Association [1]
SD Specifications - Part 1 Physical Layer Specification	version 6.10, 2018-03-18, SD Card Association
SD Specifications - Part E1 SDIO Specification	version 4.10, 2012-02-20, SD Card Association
Embedded Multi-Media Card (eMMC) Electrical Standard	version 5.1, July 2014, JEDEC
SD/eMMC Host Controller — User Guide	version 2.0, January 2019, Cadence
Combo DLL PHY IP — User Guide	version 1.12, January 2019, Cadence
SD/eMMC PHY IP — Register list	version 1.0, January 2019, Cadence

[1] Title page indicates that this controller support device compatible up to 6.00. However, it does not support optional feature — UHS-II/UHS-III Interface.

Acronyms and Abbreviations

The following acronyms and abbreviations (2) are used in this guide:

Table 2. Acronyms and Abbreviations

Term	Definition
SD	Secure Digital card
SDSC	Standard Capacity SD card
SDHC	High Capacity SD card
SDXC	eXtended Capacity SD card
SDUC	Ultra Capacity SD card
SDIO	Secure Digital Input/Output card
MMC	MultiMediaCard
eMMC	Embedded MultiMediaCard
FIFO	First In First Out memory
SDMA	Simple Direct Memory Access
ADMA	Advanced Direct Memory Access
DMA	Direct Memory Access
CRC	Cyclic Redundancy Check
UHS-I	Ultra High Speed Interface Phase I
UHS-II	Ultra High Speed Interface Phase II

Terminology

The following terminologies (3) are used in this guide:

Table 3. Terminology

Term	Definition
Data Transfer Terminology	
CPU	This transfer method uses direct access to the internal buffer through register interface. The buffer is mapped into address space as SRS08. The SRS08 works as a queue to internal buffer. The DMA engines in such transaction are disabled.
SDMA	Simple DMA — The (simple/single-operation) DMA algorithm introduced and defined in SD Host Controller Standard Specification Version 1.00
ADMA	Advanced DMA — The (advanced) DMA algorithm introduced and defined in SD Host Controller Specification Version 2.00 that provides the data transfers between system memory and the SD card without interruption of CPU operation. There are two types of ADMA: ADMA1 and ADMA2. Wherever the term 'ADMA' is used in this document, it applies to ADMA2 modes.
ADMA1	Advanced DMA mode 1 — The DMA algorithms defined in SD Host Controller Specification Version 2.00 — Appendix C. The ADMA1 can support transfer of data only if buffer is aligned to 4kB boundary in system memory. Since the SD Host specifications version 3.00 (and later) denotes ADMA1 mode as obsolete, therefore it is not supported by this version of SD Host Controller.
ADMA2	Advanced DMA mode 2 — The DMA algorithms defined as recommended ADMA algorithm in SD Host Controller Specification Version 2.00. The ADMA2 can support data transfer of any location and any size (removes the 4KB aligning restriction of the ADMA1 mode). The ADMA2 can operate in 32-bit or 64-bit addressing modes.
DMA	Wherever the term DMA is used in this document, it applies to both, SDMA and ADMA2 modes.

Term	Definition
SPRAM	Single-Port RAM — The internal FIFO module requires this memory type for data buffering.
Register Access Mode Terminology	
RO	Read-Only register. Write operation to this register is ignored. The reset does not alter the value.
ROC	Read-Only register. Content of this register is initialized to zero at the reset. Write operation is ignored.
RW	Read-Write register. It can be either set (’1’) or cleared (’0’) by software to the desired state.
RW1C	Read-Only register. This register is set to ’1’ by hardware on particular events. Writing ’1’ clears the register. Writing ’0’ has no effect.
RWAC	Read-Write, automatic clear register. When writing ’1’ to RWAC, the host is requested to perform given operation. When the requested operation is completed, this register is automatically cleared. Writing ’0’ to RWAC bits has no effect.
HwInit	Hardware Initialized register. It is read-only and a desired values is defined (hardcoded) in RTL. Write operation is ignored.
WO	Write-Only register. This is used to force the error status register setting. Each WO-type bit has a corresponding error status bit. Reading these bits returns 0.
P	The content of the register is write-protected by the SD Host Controller logic when a Command Inhibit (DAT) is active (set to 1) in the SRS09 register.
Text Formatting Conventions	
italics	Pin names are in italics inside the text. For example, *sdmclk*.

1. Introduction

1.1 Overview

1.1.1 Purpose of Document

This document contains the Integration guide for SD/eMMC Host Controller design.

The document provides the core architecture description, register set description and sub-modules specification.

1.2 Overview of the Controller IP

Figure 1 is a basic overview of system containing the Host Controller IP, showing the typical requirements to connect to an external SD/eMMC device and operate the software stacks.

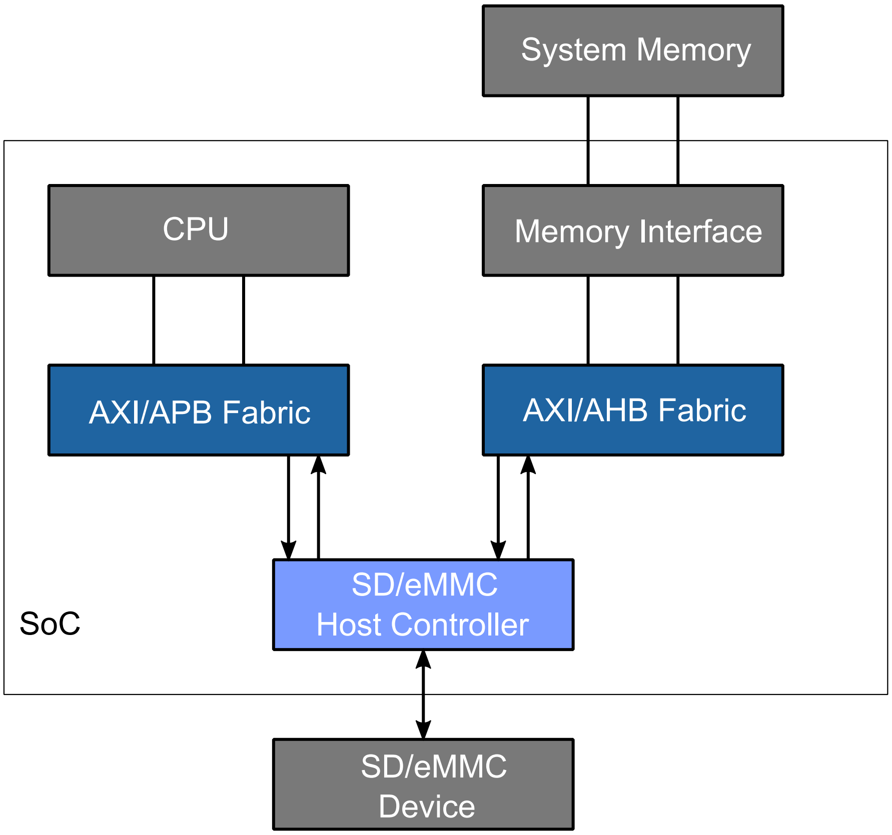

Figure 1. Example System Level Block Diagram

2. Design Integration

This chapter provides the information for integrating the Controller IP into your SoC design.

2.1 Delivery directories

Table 4 lists the package list and short description of derivelables. Please refer to provided RELEASE_TREE and RELEASE_NOTES files in the base folder of the package for further information on contents and usage.

Table 4. Delivery File Details

Directory	Subdirectory/Files	Description
dft		N/A[1]1
doc		All relevant IP documentation
func_ver	gatesim	N/A[1]
	sanity	Sanity Testbench
	hvm	N/A[1]
	soma	N/A[1]
	sva	N/A[1]
	sdf	N/A[1]
hdl	hdl_src	Unencrypted synthesizable design source files
	behav_src	N/A[1]
	behav_enc	N/A[1]
	hdl_enc	N/A[1]
fpga		N/A[1]
models	ipxact	Register abstraction models in IP-XACT format
	rdl	N/A[1]
pwr_intent	cpf	N/A[1]
	upf	N/A[1]
synth	constraints	Functional and scan mode constraint files
	logs	Log files of trial synthesis run
	reports	Analysis reports based on provided constraints
	technology	Technology-specific setup files
	scripts	Support scripts for synthesis run and analysis
software		Settings calculation script
hdl_qc		N/A[1]
sta	constraints	N/A[1]
	logs	N/A[1]
	reports	N/A[1]
	technology	N/A[1]
	scripts	N/A[1]

[1] Directory not applicable for this Soft IP

2.1.1 Installation

Typically, the IP is shipped in a single compressed tarball. The following description details how to install the model in a Linux or Unix environment.

To install the host, execute the following steps:

Copy the delivery pack file to your local directory:

```
cp <tarball_name>.tar.gz ./
```

Unzip compressed archive; the <tarball_name>.tar will be in the local directory:

```
gzip -d <tarball_name>.tar.gz
```

Untar the archive you will have the <tarball_name> directory, which contains all deliverables:

```
tar -xf <tarball_name>.tar
```

At this point, the core is ready to use.

2.2 Design Configuration

User gets configured version of controller according to addendum. No additional configuration of design is needed.

2.3 Interface Integration

The slave interface is provided to support a register access. The slave interface is equipped in module handling AXI4-Lite or APB signaling. The master interface is provided to support a DMA access. The master interface is equipped in modules handling AXI3 or AHB-Lite signaling. The slave and master interfaces are selected upon the SD Host Controller (top level) integration. Input ports of unused interface have to be tied to 0. Output ports of unused interface should be left unconnected. Additionally, to select type of the master interface, master_if port has to be tied to 0 (AXI) or 1 (AHB-Lite). The Interface to PHY is APB Interface for PHY configuration, and DFI interface for data transfer. For detailed description of used PHY Interface, please refer to SDHC User Guide.

2.3.1 Slave Interface Configuration

The host controller has two slave interfaces — AXI and APB. Only one interface can be used. The second interface is unused which means inputs are tied to 0 and the outputs are ignored.

2.3.2 Master Interface Configuration

The host controller has two master interfaces — AXI and AHB-Lite. Only one interface can be used. The second interface is unused which means inputs are tied to 0 and the outputs are ignored. The interface type is selected by assigning the master_if to 0 for AXI or to 1 for AHB-Lite.

2.3.3 PHY APB Interface Integration

The PHY has dedicated APB Interface to access PHY internal configuration and setting registers. From integration perspective, the PHY APB slave interface shall be connected to the Host Controller APB Master Interface.

2.4 Integrating DFT

The Cadence SD Host Controller IP is fully scanable. No specific features is required as wrote in Section 4..

2.5 Integrating Technology-Specific Cells

Cadence reuse cells for synthesis are delivered but must be replaced by dedicated technology cells. Replacement must be done in the following way:

- Replace content of existing file but keep the module name and interface
- Optionally keep configurable parameters

Table 5 lists modules that must be replaced by dedicated technology cells:

Table 5. Cadence Reuse Cells for Synthesis

Location	Description
cdns_sdhc/hdl/hdl_src/<prefix>_datasync_v1.v	Synchronization flops cell Used configuration: • Number of flops = 2 • Asynchronous reset

2.6 Integrating RAMs

The SD/eMMC Host Controller requires four external SPRAMs which function and interface is described in Host Controller User Guide. All SPRAMs are identical and depends of the FIFODEPTH parameter. When the parameter equals 6, each SPRAM is 64x64-bits (512 bytes). When the parameter equals 8 (default), each SPRAM is 256x64-bits (2048 bytes). The parameter must not be set to anything except values described above.

Table 6. Memory requirements

Data Width	Address Depth	Data Buffer Size	SPRAM Size	Total Memory Size
64-bit	64	512 bytes	512 bytes	2k bytes
64-bit	256	2048 bytes	2048 bytes	8k bytes

The delivery package includes SD/eMMC Host Controller and the Combo PHY. Figure 2 illustrates what is provided, and requires user integration. The figure ignores system elements and focuses on the memory requirement, PHY, and backend interface.

The integrated level consist of synthesizable modules. User adapts the *HIC* modules by porting them into the target technology (PHY User Guide describes details).

The user level shows what is provided with simulation environment in the cdns_sdhc/func_ver/sanity/chip/cdns_sdhc_chip_io.v, cdns_sdhc/func_ver/sanity/chip/cdns_sdhc_chip_mem.v, cdns_sdhc/hdl/hdl_src/cdns_sdhc_top.v files. Those files are an example solely used for verification purpose but which can give high level view on this topic.

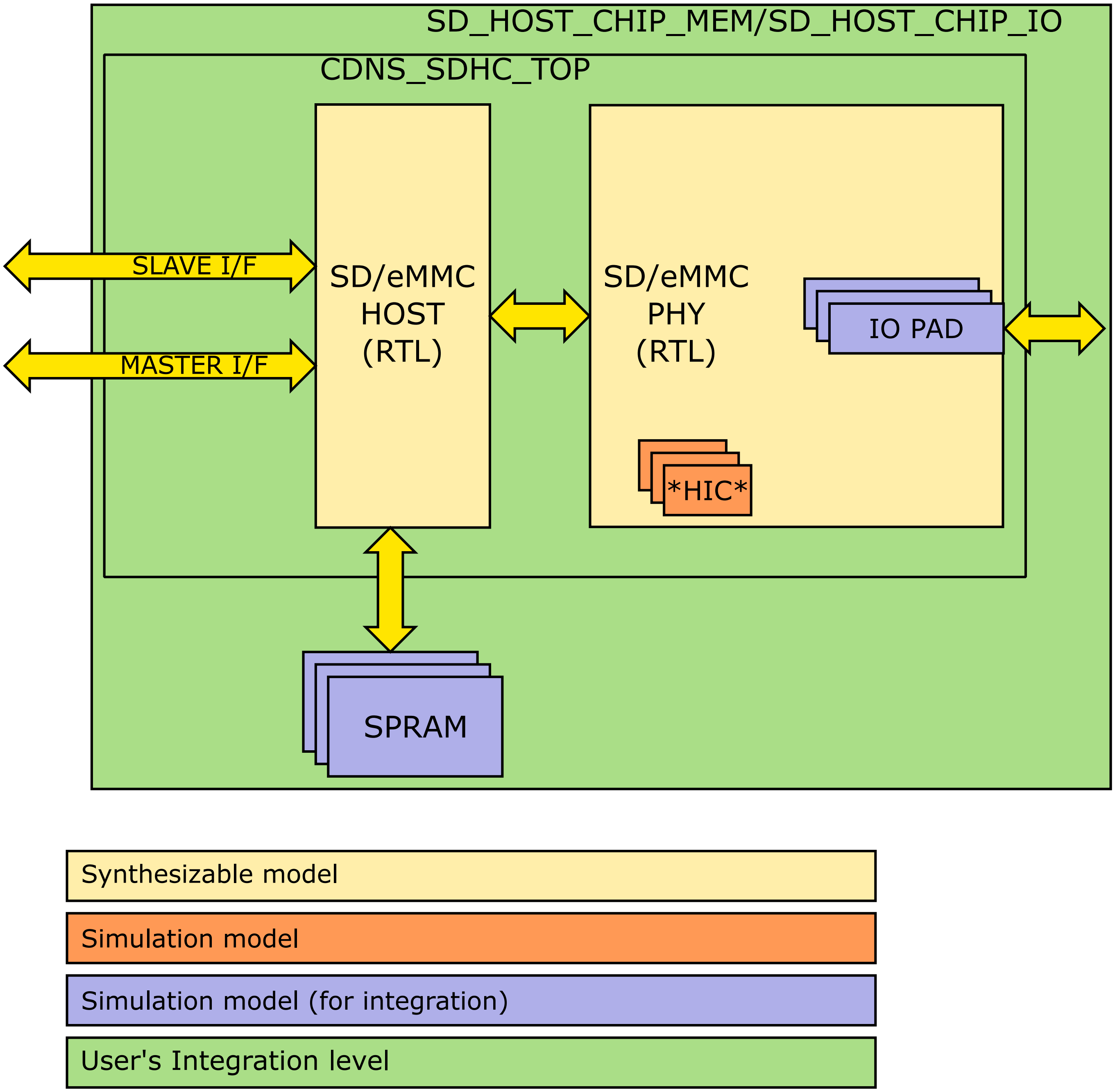

Figure 2. Integration Levels

Note:

- SD/eMMC HOST (RTL) — cdns_sdhc/hdl/hdl_src/top/cdns_sdhc.v
- SD/eMMC PHY (RTL) — cdns_combo_dll_phy/hdl/hdl_src/cdns_combo_dll_phy_top.v
- SD/eMMC PHY (FPGA RTL - optional) — cdns_combo_dll_phy/fpga/<target_name>/cdns_combo_dll_phy_top.v
- CDNS_SDHC_TOP — user level to integrate Host and PHY — cdns_sdhc/hdl/hdl_src/cdns_sdhc_top.v
- SD_HOST_CHIP_MEM/SD_HOST_CHIP_IO — user level to integrate CDNS_SDHC_TOP, SPRAMs.

2.7 Integrating with System Clocking and Reset Scheme

2.7.1 Clock Integration

Clock inputs are described in table 7.

Table 7. Clock Inputs

Clock	Min freq.	Max freq.	Description
s_pclk	20MHz	400MHz*	When the system APB master is connected to the SD/eMMC Host Controller APB slave interface, this input is supplied from the APB clock. The minimum and maximum frequencies are not specified by the SD standard, and those are defined as a verification assumption. The APB clock frequency must be defined within range from 20MHz to 400MHz. If the system AXI master is connected to the AXI slave interface and the APB slave interface is remained unconnected, this input is supplied from the same source clock as the clk.
clk	20MHz	400MHz*	This clock input must be supplied from the AXI slave interface clock or the AHB slave interface clock (user makes a decision which one is to be used). In case the system AXI master is connected to the AXI slave interface, the AXI master interface and the AXI/AHB iternface works on the common clock. The minimum and maximum frequencies are not specified by the SD standard, and those are defined as a verification assumption. The AXI/AHB clock frequency must be defined within range from 20MHz to 400MHz.
sdmclk	200MHz	200MHz**	This is the SD Master clock. It supplies the Card Interface Unit/-Logic in the SD and eMMC mode. The clock frequency is fixed and equal to 200MHz.
sdphy_reg_pclk	20MHz	400MHz*	This is a clock signal utilized by the APB interface connection between Host Controller and Combo PHY. The clock frequency must be defined within range from 20MHz to 400MHz, and the frequency equals. If the system AXI master is connected to the AXI slave interface and the APB slave interface is remained unconnected, this input is supplied from the same source clock as the clk.

* — Reference maximum frequency is based on TSMC 16nm technology and the actual achievable maximum frequency may vary per the specified process/library and margin requirements. For example, at TSMC 55nm the maximum is achievable system clock frequency is 200MHz. The maximum achievable system clock frequency may be reduced further at geometries above TSMC 55nm.

** — The card side clock requires a fixed 200MHz clock. This card side clock has smaller logic paths than the system clock (*clk*) and timing can safely be met with TSMC 16nm and TSMC 55nm. Careful consideration however should be taken at geometries above TSMC 55nm to ensure the 200MHz timing requirement can be met.

Signal sd_dfi_webar, which is connected to PHY is working as clock for SD Interface. Detailed description how to drive clock is decribed in SD Host Controller Specification ver.6.00 in section 3.2 SD Clock Control.

2.7.2 Reset Integration

Asynchronous Hardware Reset The SD/eMMC Host Controller is asynchronously reset core. The asynchronous resets are active low. The core has separate hardware reset inputs for each clock domain. The resets can be asserted at any time and are to be de-asserted on the rising edge of related clock (table 8). In order to reset the host controller, all resets are to be activated and all active resets period have to overlap before the resets are de-asserted. Minimum time of overlapping is not defined and depend on the target technology. The time is to be sufficient to reset controller logic.

Table 8. Hardware resets inputs

Reset name	Related clock domain
s_presetn	s_pclk
rstclk_n	clk
rstsdmclk_n	sdmclk
sdphy_reg_presetn	sdphy_reg_pclk

Software Reset

The SD/eMMC Host Controller can be reset by software in several ways depends on the selected mode. Software reset can be started at any time by setting one of the following bits:

- HRS00.SWR (Software Reset) resets all internal logic. This reset is common for the SD Host Controller and operates similarly to the hardware reset. Refer to the HRS00.SWR register description for details.
- SRS11.SRFA (Software Reset For All) resets all internal logic for a given slot. Please refer to the SRS11.SRFA register description for details.
- SRS11.SRCMD (Software Reset For CMD) resets the part of the design responsible for command generation and response checking for a given slot. Please refer to the SRS11.SRCMD register description for details.
- SRS11.SRDAT (Software Reset For DAT) resets the part of the design responsible for data transfers for a given slot. Please refer to the SRS11.SRDAT register description for details.

2.8 Integrating with System Low-Power Scheme

There are no low power techniques used in Controller IP.

2.9 Verification Features

There are no simulation support features.

2.10 Diagnostic Features

The register CDNS_SDHC HRS32 enables read current state of most FSMs in SD Host Controller. Details are provided in SD Host Controller User Guide.

2.11 Compiling the Design

See section "Environment usage" section in the SD Host Controller IP User Guide.

2.11.1 Tool Chain

Software tools used in the designs and verification process.

Table 9. Tool Chain

Tool	**Version**
Cadence Xcelium	21.08.001
Cadence VIPCAT	11.30.053
Tool	**Version**

Although we took all precautions to write the RTL code and the test environment in accordance with the HDL languages standards (Verilog), we cannot guarantee the user will get the same results as presented in our materials if using other tools, or other versions of tools, than those listed in the table above.

3. Synthesis

This chapter covers the example of Cadence Genus synthesis scripts (including netlist and result files) and constraints that are provided in the delivery. User can base on the scripts and constraints to meet the specific needs of SoC.

Two use cases are considered for this IP:

- The RTL code of the IP can be integrated and synthesized with target SoC directly.
- The RTL code of the IP can be synthesized as standalone netlist and integrated in target SoC as a pre-mapped component.

Provided scripts allow to generate netlist that is functionally equivalent to RTL code and can be implemented in customer flow.

3.1 Directory/Files

File	Description
synth/constraints/cdns_sdhc.func.sdc	SDC Synthesis constraints
synth/scripts/genus_synth.tcl	main script
synth/scripts/dft_setup.tcl	DFT insertion script
synth/scripts/dft_insert_scan.tcl	DFT insertion script
synth/scripts/mmmc.tcl	multi-mode-multi-corner settings
synth/scripts/set_tcl_vars.tcl	variables settings
synth/scripts/setup_dirs.tcl	variables settings
synth/scripts/project.tcl	variables settings
synth/scripts/Makefile	Makefile
synth/technology/tech_lib_setup.tcl	library settings
synth/technology/tech_lib_example.tcl	library settings template

3.2 Synthesis flow

The IP can be synthesized with scripts available in delivery. To synthesize the IP:

1. Ensure Genus executable is visible in the environment and license is configured.
2. Open and review library settings (synth/technology/tech_lib_setup.tcl). This file is example library setup.
3. Review the library settings template file (synth/technology/tech_lib_example.tcl). You can use this file to create your own setup. When done, just replace existing tech_lib_setup.tcl with new one.
4. Go to subdirectory `synth/scripts` and run ’`make`’
5. Review logfiles in synth/reports and synth/logs. Output data will be generated to `synth/data`.

3.3 Clocking Constraints

In Host Controller all clocks are asynchronous vs each other, so each one is placed in separate clock group. No clock gating is implemented in the RTL. There are no special requirements for Scan mode.

3.4 I/O Constraints

Generic I/O constraints for ports are applied in SDC to define default setup/hold on I/O paths. These constraints are safe margin for synthesizing the IP as standalone part. Clock assignments are described in User Guide.

3.5 Timing Modes

Not applicable for the Host Controller IP.

3.6 Power Constraints

Power constraints does not apply to the Host Controller IP.

3.7 Preserving Key Parts of the Design

It is recommended that all hand-instantiated modules (i.e.) sync flop modules from technology library, are preserved for synthesis, so they cannot be subsequently replaced by the tool with standard cells.

3.8 Latches

There are no latches in the Host Controller IP.

4. Design for Test

No specific DFT feature is required.

5. Performance, Power and Area

The Host Controller achieves the maximum throughput defined by the SD Physical Layer Specification Version 6.10 (with no support for UHS-II) and by JEDEC eMMC 5.1 (supporting highest speed modes HS400).The Host Controller together with SD/eMMC PHY supports the speed modes of SD/eMMC that are listed in the table 10.

5.1 Performance

Table 10. Performance

Group	Speed Mode	Data Rate	I/f Width	Freq. [MHz][1]	Transfer [MBps][2]
SD	Default Speed	Single	1,4	25	12.5
	High Speed	Single	1,4	50	25
SD UHS-I	SDR12	Single	1,4	25	12
	SDR25	Single	1,4	50	25
	SDR50	Single	1,4	100	50
	SDR104	Single	1,4	200	100
	DDR50	Dual	1,4	50	50
eMMC 5.10	Backward Compatible Mode	Single	1,4,8	25	25
	High Speed SDR	Single	4,8	50	50
	High Speed DDR	Dual	4,8	50	100
	HS200	Single	4,8	200	200
	HS400	Dual	8	200	400
	HS400 Enhanced Strobe	Dual	8	200	400

Advanced DMA uses a Scatter-Gather operation to provide efficient data transfers in a system with fragmented memory, and permit execution of transfers at a high rate without increasing overhead for the system processor.

[1] Maximum SD/eMMC (backend) interface clock frequency
[2] Maximum theoretical throughput assuming highest interface width

5.2 Power and Area

The table 11 presetns details about power and area estimations. All data is based on trial Synthesis/PnR flow.

Table 11. Power and Area

Process Information	
Foundry Process	TSMC16FFC/FFPLUS
Power Consumption	
IDLE: Leakage (mW)[1]	0.003
IDLE: Dynamic (mW)[1]	5.48
SDR104: Leakage (mW)[1]	0.003
SDR104: Dynamic (mW)[1]	5.84
Area	
Total Area (um2)[2]	30230.6
Placement density (%)[2]	76.38
Total Gatecount (NAND2)[2]	146k

[2] Power peak values, calculated at SDC frequencies for typical (TYP) PVT corner.

[2] Area values are calculated including clock gating insertion and DFT scan insertion logic.

Change history

Table 12. Change history

Revision	Date	Description
1.0	2019-06-28	IP6061 R602 released
Revision	**Date**	**Description**