SIEMENS

Axelera LPDDR Subsystem Verification Testplan

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Revision History

Revision	Author	Date	Reviewer	Review Date	Approver	Approval Date
1.0	Siemens	17-Oct-24	Axelera	08-Nov-2024	Axelera	08-Nov-2024

Revision	Description of Change
1.0	First Baseline post review and approval from Axelera taken on 12th Nov 2024.

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1 Introduction

1.1 Document Scope

This Document provides information regarding the Verification Plan of the LPDDR Subsystem. It lists all the different testcases planned as part of Verification for the LPDDR Subsystem. For each test case it provides a brief description, covering intent of the test and targeted functionality along with Combinations which are planned to be covered by verification. It also lists Reference Information pointers for better understanding.

Note: The test cases defined in Section 2, provide a brief overview of what is planned to be targeted for the verification of the associated functionality. However, the detailed Verification methodology in terms of concept of Stimulus definition, Checkers and Scoreboard approach is defined in the "Axelera LPDDR Subsystem Verification Specification" Document.

1.2 References Used

Table 1: List of References

Sr. No.	Name of Document	Version	Owner
1	Axelera_Europa_LPDDR5X_Subsystem_Databook	0.6	Axelera
2	Axelera_Europa_LPDDR5X_Subsystem_Reference_Manual	0.7	Axelera
3	LPDDR5X/5/4X Memory Controller Databook	1.60a	Synopsys, Inc
4	LPDDR5X/5/4X Memory Controller Reference Manual	1.60a	Synopsys, Inc
5	LPDDR5X/5/4X PHY Utility Block (PUB) Databook	2.30a	Synopsys, Inc
6	Axelera LPDDR Subsystem Verification Specification		Siemens

2 Verification Testplan

2.1 Initialization and Configuration Testing

2.1.1 Initialization Test

Description:

This testcase verifies that the Subsystem performs completes initialization steps per the LPDDR Protocol to Initialize the SDRAM and updates STAT.operating_mode as normal after initializing the DDR controller and PHY.
Note: Table 14-1 of Controller Databook and Section 6.4.1 of PHY Pub Databook are confirmed as steps required to verify the correct initialization here.

Combinations to be Covered:

- Cover combination of INITTMG0.skip_dram_init=0,01,11.
- Cover the DDRCTRL reset core_ddrc_rstn application
- Cover the HardIP(Reset_async) and warm reset (Reset) of phy application
- Cover logic '0' and '1' for DFIMISC.dfi_init_start, DFISTAT.dfi_init_complete for PHY Initialization.
- Cover the STAT.operating_mode as Normal Mode(value 1).
- Cover below values for MSTR0.burst_rdwr and MSTR0.data_bus_width:
  MSTR0.burst_rdwr as BL16
  MSTR0.data_bus_width as 00 (FBW) and 01 (HBW).
- Cover below logic values:
  MSTR0.active_ranks = 01, 11

Reference Information:

Axelera_Europa_LPDDR5x_Subsystem_databook.pdf Section 3.5
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section 14.1

2.1.2 APB Address Decoding Test

Description:

This testcase verifies that the Subsystem APB decoder differentiates DDR PHY and Controller accesses based on bits 25:22 of the APB Address.

Combinations to be Covered:

- Cover read and write of different DDR Controller Registers by setting APB Address bit 25 to logic '0'
- Cover read and write of different PHY Registers by setting APB Address bit [25 :22] as 'b1000 and other address bits to ensure one access in each region of PHY Address Space.
- Cover application of APB Reset, presetn

Reference Information:

Axelera_Europa_LPDDR5x_Subsystem_databook.pdf Section 3.8

2.1.3 Mode Register Write/Read Testing

Description:

This test case verifies that the Subsystem is performing Mode register write and reads through APB Configuration registers MRCTL0, MRCTL1, MRSTAT.

Combinations to be Covered:

Cover different combinations between following configurations:
- Different data on MRCTRL0.mr_addr, MRCTRL0.mr_rank, MRCTRL1.mr_data(in case of write only) for MRR/MRW.
- logic '0' and '1' values on MRCTRL0.mr_type, MRCTRL0.mrr_done_clr and MRSTAT.mrr_done
- Configured MR Values by MRW on INITMR*
- Response of MRR command on MRRDATA0 and MRRDATA1.
- perf_op_is_load_mode as logic '0' and '1'
- Non zero values on hif_mrr_data with hif_mrr_data_valid as logic '1'
- Cover perf_precharge_for_other to logic 1 when Pre-charged Issued due to MRW.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:10.1

2.1.4 DDRCTL Data Bus Inversion Test

Description:
This test case verifies that the Subsystem is performing Data Bus Inversion as configured through APB Configuration register DBICTL and DFIMISC.

Combinations to be Covered:
Cover different combinations of DBICTL.rd_dbi_en, DBICTL.wr_dbi_en, DBICTL.dm_en with logic '0' and '1' value of DFIMISC.phy_dbi_mode and data values with less than and more than 4 logic '1' in the data byte.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:10.2

2.2 Traffic flow and Address Translation Testing

2.2.1 AXI Input Traffic Handling

Description:

This testcase verifies that the Subsystem performs correct conversion of incoming AXI Read and Write Transactions of different sizes and addresses before sending on the DDR SDRAM Interface.

Combinations to be Covered:

Cover AXI Read and Write Transactions on the AXI Interface with the following attributes:
- Cover different values for burst type (FIXED, INCR and WRAP)
- Cover different Burst Size less than AXI data width
- Cover different Burst Length values.
- Cover different Burst Address values with different regions with addresses aligned and unaligned to Burst Boundaries.
- Cover different values on QOS
- Cover Unsupported Region, Checksum, Flow Control, Burst Transfer Error (Incomplete Bursts), Transfer Size Violation and Addressing Errors (Invalid and Unaligned Addresses)

Cover the different values of following performance logging signals
- perf_bank[2:0]
- perf_bg[1:0]
- perf_dfi_rd_data_cycles
- perf_dfi_wr_data_cycles
- perf_hif_rd
- perf_hif_rd_or_wr
- perf_hif_wr
- perf_op_is_cas
- perf_rank
- perf_hif_rmw

Cover application of AXI Reset, aresetn_0

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:3.1, 3.3
Axelera_Europa_LPDDR5X_Subsystem_Reference_Manual.pdf Section 1.26

2.2.2 Address Translation Test

Description:

This testcase verifies that Subsystem performs correct address translation of incoming AXI Read and Write Transactions by considering the recommendations mentioned in Section-6.4 of DWC_ddrctl_lpddr54_lpddr5x_databook.pdf before sending them on the DDR SDRAM Interface and support Bank Hashing Feature. It also verifies that the Subsystem is mapping Address according to selected bank architecture based on the programming of APB Configuration Registers DRAMSET1TMG24 , ADDRMAP3, ADDRMAP4, ADDRMAP5, ADDRMAP6 and that it generates SLVERR in response to invalid addresses if configured as a Non-Binary Device Density in ADDRMAP12.

Combinations to be Covered:

- Cover different ranges of AXI Read and Write transactions with addresses resulting in access to:
  - Each rank, bank and bank group.
  - Different ranges of row and column addresses on each page.
- Cover different valid values for non-reserved bits of ADDRMAPx (x=0 to 12) as defined in DWC_ddrctl_lpddr54_lpddr5x_reference.pdf to select the HIF address bits used as bits for rank, bank, bank group, row and column addresses.
- Cover ADDRMAP12.bank_hash_en as logic '0' and '1'
- Cover DRAMSET1TMG24.bank_org = 0 (BG Mode) and 2 (16B Mode)
- Cover following configuration for Address map Recommendations (As per Section-6.4):
  ADDRMAP6.addrmap_col_b3 = 0
  ADDRMAP6.addrmap_col_b4 = 0
  ADDRMAP4.addrmap_bg_b0 = 2

- Cover below cases for Non-binary Subsystem Densities:
  Cover all eight combinations of ADDRMAP12.nonbinary_Subsystem_density and AXI Reads and Writes resulting in Address Error for each of these density Configurations.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:6.2, 6.3, 6.4, 6.5, 6.7

2.2.3 LPDDR5 WCK Clocking Test

Description:
This test case verifies that the Subsystem is managing WCK by DDRCTL as programmed using APB Configuration Registers DFITMG4, DFITMG5, TMGCFG, MSTR4 and issues CAS-WS_RD, CAS-WS_WR, CAS-WS_FS, CAS-WS_OFF and CAS-WCK_SUSPEND commands as required.

Combinations to be Covered:
- Cover different timing values of DFITMG[4|5].dfi_twck_*.
- TMGCFG.frequency_ratio as logic '1'
- Cover logic '0' and '1' value on MSTR4.wck_on, MSTR4.ws_off_en, MSTR4.wck_suspend_en in different combinations
- Cover following performance logging signals as logic '0' and '1'
  perf_op_is_cas_wck_sus
  perf_op_is_cas_ws
  perf_op_is_cas_ws_off

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:12.3

2.2.4 Page Match Feature

Description:
This test case verifies that the Subsystem Locks on read and write ports when consecutive transactions to same page are observed and page match enable is for the port is set to logic '1' unless it needs to release lock due to credit unavailable, another high priority request or timeout out ports.

Combinations to be Covered:

Cover different combinations of following registers with associated values:
- logic '1' and '0' values for following registers:
  PCFGW.wr_port_pagematch_en
  PCFGR.rd_port_pagematch_en
- Different values of the PCCFG.pagematch_limit register
- Consecutive AXI Reads and Writes with addresses on same and different page
- Timeouts on other ports
- Read/Write credit unavailability

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 3.1.2.7

2.2.5 Throughput Test

Description:
This testcase verifies the throughput of the Subsystem by generating the maximum traffic over the AXI port by sending multiple reads and writes with different address values and QOS.

Combinations to be Covered:
Cover following traffic scenarios:
1. Back to back AXI Reads and Writes with similar QOS with Maximum Burst Length and Size on different addresses
2. Back to back AXI Reads and Writes with different QOS with Maximum Burst Length and Size on different addresses
3. Following Configurations:
  - Minimum timing for Latency Values in Mode Register and APB Configuration registers for timings between commands.
  - Maximum timing for all periodic maintenance timers (Example Refresh, ZCal)
  - DRAMSET1TMG24.bank_org = 0 (BG Mode) to support maximum speed

Reference Information:
NA

2.2.6 Transaction Poisoning Test

Description:
This testcase verifies how the Subsystem Handles the Poisoned Transactions on AXI Subordinate Interface

Combinations to be Covered:
Cover different combinations of below registers with associated values:
- logic '1' and '0' on Sideband Signals arpoison and awpoison on AXI for Poisoned transaction for AXI reads and writes.
2. Cover logic '0' and '1' value on POISONCFG.rd_poison_slverr_en, POISONCFG.rd_poison_intr_en, POISONCFG.rd_poison_intr_clr, POISONCFG.wr_poison_slverr_en, POISONCFG.wr_poison_intr_en, POISONCFG.wr_poison_intr_clr.
3. POISONSTAT.wr_poison_intr_0 and POISONSTAT.rd_poison_intr_0 as logic '1' and '0'

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:3.1.1.10

2.2.7 Async Performance Counter Test

Description:

This testcase verifies that the Subsystem updates each instance of performance counter output on o_cntrl_cnt_value based on i_count_inc and i_ctrl_cnt_en and checks the reset value to 0 based on flush input.

Combinations to be Covered:

- Cover both logic value 1 and 0 of register values which control i_cntr_en and i_ctrl_cnt_flush
- Cover incrementing non-reset values on o_cntrl_cnt_value
- Cover the transition of o_cntrl_cnt_value from non-reset to reset value with i_ctrl_cnt_flush input

Reference Information:

2.3 Command Scheduling

2.3.1 Page Policy Test

Description:

This test case verifies that the Subsystem is supporting Page Policy feature as programmed through APB Configuration Registers SCHED0, SCHEDTMG0.

Combinations to be Covered:

- Cover both logic '1' and '0' value of SCHED0.pageclose with zero and different non-zero values of SCHEDTMG0.pageclose_timer
- Cover the last Read/Write with auto-precharge command when SCHED0.pageclose is set to ’1’ and SCHEDTMG0.pageclose_timer=0
- Cover precharge command when SCHED0.pageclose is set to ’1’ and SCHEDTMG0.pageclose_timer>0.
- Consecutive AXI Reads and Writes to same and different page addresses

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:7.2

2.3.2 Write to Read Switching

Description:

This testcase verifies that switching the direction of read or write and prepare the page of the bank for it by sending back to back write and read in different order.

Combinations to be Covered:

Cover different combinations of following registers and associated values:

- PCFGQOS0.rqos_map_level[1|2] and PCFGQOS0.rqos_map_region[0|1|2] as different valid values
- PCFGWQOS0.wqos_map_level[1|2] and PCFGWQOS0.wqos_map_region[0|1|2] as different valid values
- Different timeout values on registers PCFGQOS1_n.qos_map_timeoutb, PCFGQOS1_n.rqos_map_timeoutr, PCFGWQOS1_n.wqos_map_timeout1 and PCFGWQOS1_n.wqos_map_timeout2
- rd_act_idle_gap and wr_act_idle_gap to 0 and non zero values
- Different values on SCHED4.wr_page_exp_cycles, SCHED4.rd_page_exp_cycles
- Different values on SCHED3.wrcam_highthresh, SCHED3.wrcam_lowthresh
- Cover AXI Reads and Writes with QOS values resulting in Low/Variable/High/Normal Reads/Writes

Cover the performance logging signals with different values:

- perf_op_is_activate
- perf_op_is_rd
- perf_op_is_rd_activate
- perf_op_is_rd_or_wr
- perf_war_hazard,
- perf_visible_window_limit_reached_wr,
- perf_visible_window_limit_reached_rd,
- perf_rdwr_transitions,
- perf_raw_hazard,
- perf_precharge_for_rdwr,
- perf_op_is_wr
- perf_hpr_xact_when_critical

- perf_hpr_req_with_nocredit
- perf_lpr_xact_when_critical
- perf_lpr_xact_when_nocredit
- hpr_credit_cnt
- lpr_credit_cnt
- wr_credit_cnt

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:7.3

2.3.3 Address Collision Handling and Write Combine Test

Description:
This testcase verifies that how Subsystem handles the back to back writes with same address depending on the write combine enable and disable(TODO how to enable/disable write combine).

Combinations to be Covered:
Cover AXI Reads and Writes in following scenarios:
- New read colliding with queued read
- New write colliding with queued write with logic '0' and logic '1' values of OPCTRL0.dis_wc and write ecc enable and disable
- New write colliding with queued Read
- New read colliding with queued write
- New read colliding with both read and write
- New write colliding with both read and write with logic '0' and logic '1' values of OPCTRL0.dis_wc and write ecc enable and disable
- New RMW colliding with queued write

Cover logic '0' and '1' on signals perf_write_combine, perf_write_combine_noecc and perf_write_combine and perf_write_combine_wrecc, perf_waw_hazard, perf_wr_xact_when_critical.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:7.4, 7.5

2.3.4 DDRC Read/Write internal Port Priorities

Description:
This testcase verifies the port priorities through port aging counters based on port priority registers PCFGR.rd_port_priority and PCFGW.wr_port_priority.
Also verifies the maksing the port read/write address channel from requesting to the PA depending on parmask/pawmask.
Also exercise CAM depth for both Read and Write.
Also verifies the RMW and datamask with aligned and unaligned bursts.

Combinations to be Covered:
- Cover the different values of :

PCFGR.rd_port_priority, PCFGW.wr_port_priority and supporting fields of PCFGR register.
SCHED0.lpr_num_entries (for covering credit mechanism)
SCHED0.hpr_num_entries

- Cover RMW with unaligned bursts when DBICTL.dm_en=0
- Cover data lengths on AXI resulting in full and partial reads and writes (Odd and even number of bytes of length) with DBICTL.dm_en=1
- Cover AXI Reads and Writes with QOS values resulting in Low/Variable/High/Normal Reads/Writes
- Cover signals parmask pawmask as logic '0' and '1'

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:3.1.2, 3.3.3

2.4 Refresh Control and Management

2.4.1 Refresh Using Direct Software Request of Refresh Command Test

Description:

This test verifies that the Subsystem gets refresh request from software and sends Refresh Command to SRAM based on auto-refresh feature is enabled or disabled.
It also verifies that OPCTRLSTAT.rank*_refresh_busy is asserted when refresh command reached to buffer size as per the table 9-1 of Controller Databook.

Combinations to be Covered:

- Cover different combinations of following configurations with logic '1' value of RFSHCTL0.dis_auto_refresh and toggle in RFSHCTL0.refresh_update_level:
- OPREFCTRL0.rank[0|1]_refresh to logic '1'
- OPCTRLSTAT.rank[0|1]_refresh_busy as logic '0' and '1'
- RFSHMOD0.per_bank_refresh as logic '1' and more than 65 refresh commands from APB consecutively
- RFSHMOD0.per_bank_refresh as logic '0' and more than 9 refresh commands from APB consecutively
- perf_op_is_crit_ref as logic '0' and '1'
- perf_op_is_refresh as logic '0' and '1'

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.1.2

2.4.2 Per Bank Refresh Using Auto-Refresh Feature Test

Description:

This test verifies the time interval between the Per bank refresh commands sent by LPDDR Subsystem depending on the configuration set on RFSHSET1MG[0|1|2] and RFSHMOD0 while using Auto Refresh Feature of the Controller. It also verifies that the Subsystem issues Speculative refresh based on RFSHSET1TMG0.refresh_to_x1_x32.

Combinations to be Covered:

Cover different combinations of following configurations with logic '0' value of RFSHCTL0.dis_auto_refresh and RFSHMOD0.per_bank_refresh as logic '1' and toggle in RFSHCTL0.refresh_update_level:
- RFSHMOD0.auto_refab_en as logic '0' and '1'
- RFSHMOD0.per_bank_refresh_opt_en as logic '0' and '1'
- RFSHSET1TMG0.refresh_to_x1_sel as logic '0' and '1'
- RFSHSET1TMG0.t_refi_x1_sel as logic '0' and '1'
- RFSHMOD0.refresh_burst as zero and different non-zero values.
- RFSHSET1TMG1.t_rfc_min and RFSHSET1TMG2.t_pbr2pbr as different valid values
- RFSHSET1TMG0.refresh_to_x1_x32 and RFSHSET1TMG0.t_refi_x1_x32 as different valid values
- perf_op_is_spec_ref as logic '1'

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.1.3

2.4.3 All Bank Refresh Using Auto-Refresh Feature Test

Description:

This test verifies the time interval between the All bank refresh commands sent by LPDDR Subsystem depending on the configuration set on RFSHSET1MG[1|3] and RFSHMOD0 while using Auto Refresh Feature of the Controller. It also verifies that the Subsystem issues Speculative refresh based on RFSHSET1TMG0.refresh_to_ab_x32.

Combinations to be Covered:
Cover different combinations of following configurations with logic '0' value of RFSHCTL0.dis_auto_refresh and RFSHMOD0.per_bank_refresh as logic '0' and toggle in RFSHCTL0.refresh_update_level:
- RFSHSET1TMG1.t_rfc_min_ab as different valid values
- RFSHSET1TMG3.refresh_to_ab_x32 as different valid values
- RFSHMOD0.refresh_burst as zero and different non-zero values.
- perf_op_is_spec_ref as logic '1'

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.1.3

2.4.4 Automatic Temperature Derating Test

Description:
This test case verifies that the Subsystem is supporting Automatic Temperature Derating feature through APB Configuration Registers DERATECTL0, DERATEINT, DERATECTL5.

Combinations to be Covered:
Cover different combinations of following registers and associated values:
- DERATECTL0.derate_enable as logic '0' and '1'
- DERATECTL6.derate_mr4_tuf_dis as logic '0' and '1'
- different possible values of DERATEINT.mr4_read_interval
- DERATECTL5.derate_temp_limit_intr_en, DERATECTL5.derate_temp_limit_intr_clr and DERATECTL5.derate_temp_limit_intr_force as logic '0' and '1'
- DERATESTAT0.derate_temp_limit_intr as logic '0' and '1'
- '01', '10' value for derate_temp_limit_intr_fault interrupt.
- DERATEVAL0 timings as different valid values and not equal to non-derated timing values
- MR4[4:0] as different configuration values and MR4[7] as logic '0' and '1'

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.1.4

2.4.5 Refresh Management test

Description:
This test case to verify the RFM feature is enabled by setting RFMMOD0.rfm_en if supported by the SDRAM Based on the Programmed MR Values.

Combinations to be Covered:
Cover the below values of registers:
- RFMMOD0.rfm_en as logic '1' and '0'
- RFMMOD0.rfmsbc as logic '1' and '0'

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.2

2.5 Periodic Memory and Phy Maintenance

2.5.1 ZQ Calibration Test

Description:

This testcase verifies that the LPDDR Subsystem issues ZQCal latch command automatically at regular interval or direct from software request, depending on configuration of ZQCTL0.dis_auto_zq bit. It also verifies the zq_calib_short_busy sets during ZQ initiate

Combinations to be Covered:

Cover different combinations of following configurations:
- ZQCTL0.dis_auto_zq as logic '0' and '1'
- ZQCTL1.zq_reset as logic '0' and '1'
- ZQSTAT.zq_reset_busy as logic '0' and '1'
- ZQSET1TMG0.t_zq_short_nop, ZQSET1TMG1.t_zq_reset_nop and ZQSET1TMG2.t_zq_stop as different values
- ZQSET1TMG1.t_zq_short_interval_x1024 as different values
- ZQCTL2. dis_srx_zqcl as logic '0' and '1' with SR-Powerdown exit
- Cover perf_precharge_for_other, perf_op_is_zqstart, perf_op_is_zqlatch to logic 1 when Pre-charged Issued due to ZQ Calib.

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.3

2.5.2 MRR Snooping Test

Description:

This testcase verifies LPDDR Subsystem schedules the MPC command and MRR commands periodically.

Combinations to be Covered:

Cover different combinations of following configurations:
- DQSOSCRUNTIME timing fields as different valid values
- DQSOSCCTL0.dqsosc_interval as different valid values
- DQSOSCCTL0.dqsosc_enable as logic '0' and '1'
- perf_op_is_dqsosc_mpc as logic '0' and '1'
- perf_op_is_dqsosc_mrr as logic '0' and '1'

- Cover perf_precharge_for_other, perf_op_is_tcr_mr to logic 1 when Pre-charged Issued due to MRR.

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 9.4

2.6 Low Power and Power Saving Features

2.6.1 Pre-charge Power down Test

Description:

This test case verifies that the Subsystem is issuing command to enter and exit Precharge Power down mode for power saving as programmed through APB Configuration Registers PWRCTL and PWRTMG.

Combinations to be Covered:

Cover different combinations of following registers with associated values:
- PWRCTL.powerdown_en as logic '0' and '1'
- DFILPCFG0.dfi_lp_en_pd as logic '0' and '1'
- Different timing values for PWRTMG.powerdown_to_x32 and DFILPTMG0.dfi_lp_wakeup_pd
- An idle period without any AXI Transactions for less or greater than the configured Power Down Timing
- Self Refresh Entry and AXI Transactions during Power Down State
- perf_op_is_enter_powerdown as logic '0' and '1' for each rank

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.2.2

2.6.2 Self Refresh Test

Description:

This test case verifies that the Subsystem is moving to Self-Refresh mode for power saving through APB Configuration Registers PWRCTL and DFIPHYMSTR.

Combinations to be Covered:

Cover different combinations of following registers with associated values:
- PWRCTL.selfref_en as logic '0' and '1'
- PWRCTL.selfref_sw as logic '0' and '1'
- PWRCTL.stay_in_selfref as logic '0' and '1'
- DFILPCFG0.dfi_lp_en_sr as logic '0' and '1'
- Different timing values for PWRTMG.selfref_to_x32 timing and DFILPTMG0.dfi_lp_wakeup_sr
- No pending reads or writes for the period PWRTMG.selfref_to_x32 timing
- HWLPCTL.hw_lp_en=1 and csysreq_ddrc/csysack_ddrc with cactive_in_ddrc=0 and 1 simultaneously with no pending reads/writes and with new Read/Write request.
- Different values of STAT.selfref_type register (stat_ddrc_reg_selfref_type)
- STAT.selfref_state as valid values 'h0, 'h1, 'h2, 'h3
- perf_op_is_enter_selfref and perf_selfref_mode as logic '0' and '1' for each rank
- Cover perf_precharge_for_other as logic 1 when Pre-charged Issued due to Refresh command.

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.2.3, 11.4.2

2.6.3 Deep Sleep Mode Test

Description:

This test case verifies that the Subsystem is moving to Deep-Sleep mode for power saving through APB Configuration Registers PWRCTL.

Combinations to be Covered:
Cover different combinations of following registers with associated values:
- PWRCTL.dsm_en as logic '0' and '1'
- DFILPCFG0.dfi_lp_en_dsm as logic '0' and '1'
- Different timing values for DFILPTMG0.dfi_lp_wakeup_sr
- Cover different combinations of below register signals with PWRCTL.dsm_en=1:
  PWRCTL.selfref_sw as logic '0' and '1'
  PWRCTL.selfref_en as logic '0' and '1'
  HWLPCTL.hw_lp_en as logic '0' and '1'
- When PWRCTL.dsm_en=1, cover logic '0' and '1' value on DFIPHYMSTR.dfi_phymstr_en.
- STAT.selfref_state as valid values 'h0, 'h4
- perf_op_is_enter_dsm as logic '0' and '1'
- Cover different combinations of below register fields for dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup:
  DFILPTMG0.dfi_lp_wakeup_dsm
  DFILPTMG0.dfi_lp_wakeup_sr
  DFILPTMG0.dfi_lp_wakeup_pd
  DFILPTMG1.dfi_lp_wakeup_data
- Cover different combinations of DFILPTMG1.dfi_tlp_resp for dfi_lp_ctrl_req and dfi_lp_data_req.
- Cover logic '1' and '0' value on DFIERRINTRPTCFG.dfi_error_intr_force, DFIERRINTRPTCFG.dfi_error_intr_clr and DFIERRINTRPTCFG.dfi_error_intr_en, DFIERRORSTAT.dfi_error_intr.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.2.4

2.6.4 Hardware Fast Frequency Change (HWFFC) Test

Description:
This test case verifies that the Subsystem is supporting clock frequency change without Software intervention through APB Configuration Register HWFFCCTL.

Combinations to be Covered:
- Cover different combinations on HWFFCCTL.hwffc_mode, HWFFCCTL.hwffc_en and ZQCTL2.dis_srx_zqcl_hwffc
- Cover different values of HWFFC_MRWBUF_CTRL_0 register fields for MRW Buffer Write/Read.
- Cover logic '0' and '1' value of below signals when csysreq_ddrc=0 and csysmode_ddrc=1:
  csysdiscamdrain_ddrc
  csysfsp_ddrc
  csysack_ddrc
  cactive_ddrc

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.6

2.6.5 LPDDR5 masked write Test

Description:
This test case verifies that the Subsystem is masks write data received on DQ inputs through APB Configuration Register DFIMISC and DBICTL.

Combinations to be Covered:
- Cover both logic values '1' and '0' on DFIMISC.IP_optimized_write.
- Cover different combinations of below signals with DFIMISC.IP_optimized_write=1:
  DBICTL.wr_dbi_en=1
  DBICTL.dm_en=1
  DFIMISC.phy_dbi_mode=0

Cover below performance logging signals-
- perf_op_is_mwr

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.7

2.6.6 Fast Frequency Change Test

Description:
This test case verifies that the Subsystem supports Fast Frequency Change, using up to four sets of timing registers and by following the sequence steps mentioned in DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section- 11.4.1.3

Combinations to be Covered:
- Cover below values for APB Write on MSTR2.target_frequency:
  0 - Frequency 0/Normal
  1 - Frequency 1/FREQ1
  2 - Frequency 2/FREQ2
  3 - Frequency 3/FREQ3
- Cover different values for APB Read on DFIMISC.dfi_frequency.
- Cover different values of Timing Registers for different frequency sets.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.5, 14.4.1.3

2.6.7 DFI DRAM CLK DISABLE Test

Description:
This test case verifies that the Subsystem is disabling DFI DRAM CLK for power saving through APB Configuration Registers PWRCTL in specific operating modes.

Combinations to be Covered:
- Cover Different timing values of following registers in Deep Sleep mode, Self-Refresh Power down mode, Power-Down mode and Normal Mode with PWRCTL.en_dfi_dram_clk_disable=1:
  - DFITMG0.dfi_t_ctrl_delay
  - DRAMSET1TMG5.t_cksre
  - DFITMG1.dfi_t_dram_clk_disable
  - DFITMG1.dfi_t_dram_clk_enable
  - DRAMSET1TMG5.t_cksrx
- Cover logic '0' -> '1' and '1' -> '0' transition on Bump Signals BP_CK0_T, BP_CK0_C, BP_CK1_T and BP_CK1_C.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:11.2.5
dwc_lpddr5x_phy_pub_databook_latest.pdf Section: 4.1

2.6.8 Self Refresh through PHY Master Test

Description:
This test case verifies that the Subsystem is moving to Self-Refresh mode because of DFI PHY MASTER INTERFACE through APB Configuration Registers DFIPHYMSTR, PPTTrainSetup_pX, MasUpdGoodCtr, MasUpdFailCtr, BlockDfiInterface and DfiMode.

Combinations to be Covered:
Cover following when DFIPHYMSTR.dfi_phymstr_en is logic '1', PWRCTL.selfref_en as logic '0' and PWRCTL.selfref_sw = 0:
- STAT.selfref_state from logic '0' -> '1' and '1' -> '0'
- APB Configuration register: STAT as following transitions:
  - IDLE → SR → IDLE
  - SRPD → SR → SRPD
- different values on PPTTrainSetup_pX.PhyMstrMaxReqToAck, PPTTrainSetup_pX.PhyMstrTrainInterval, MasUpdGoodCtr and MasUpdFailCtr.

Cover logic '0' and '1' value on BlockDfiInterface.BlockDfiInterfaceEn, DfiMode.Dfi0Enable and DfiMode.Dfi1Enable.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section: 4.1.11.2
dwc_lpddr5x_phy_pub_databook_latest.pdf Section: 10.9

2.7 Error Correction and RAS

2.7.1 Link ECC Test

Description:

This test case verifies that the Subsystem is supporting Link ECC feature as programmed through APB Configuration Registers LNKECCCTL0, LNKECCINDEX, LNKECCERRCNT0, LNKECCPOISONCTL0.

Combinations to be Covered:

Cover different combinations of following registers and associated values with AXI Write and DDR Read Response Data with correct and incorrect link ECC:

- LNKECCCTL0.wr/rd_link_ecc_enable as logic '0' and '1'
- LNKECCINDEX, LNKECCERRCNT0 as different values
- LNKECCERRSTAT.rd_link_ecc_corr_err_int and LNKECCERRSTAT.rd_link_ecc_uncorr_err_int as logic '0' and '1'
- LNKECCCTL1 fields as logic '0' and '1'
- LNKECCPOISONCTL0 fields as different values to inject Link ECC Errors
- LNKECCPOISONSTAT.linkecc_poison_complete as logic '0' and '1'
- SLVERR response for Read Transactions with Link ECC Error
- ECCCSYN0 and ECCUSYN0 as correctable and uncorrectable data patterns
- dis_regs_ecc_syndrome as logic '0' and '1'
- logic '0' and '1' for rd_linkecc_corr_err_intr, rd_linkecc_uncorr_err_intr and '01', '10' value for rd_linkecc_corr_err_intr_fault, rd_linkecc_uncorr_err_intr_fault interrupt.

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:12.4

2.7.2 LPDDR5 Post Package Repair Test

Description:

This test case verifies that the Subsystem supports a method of Fail Row address repair, PPR(Post Package Repair) through APB Configuration Registers.

Note : Perform PPR Sequence described in Table 12-7 of DWC_ddrctl_lpddr54_lpddr5x_databook.pdf to verify this test and PPR Feature

Combinations to be Covered:

Cover different combination of register values:

- MRCTRL0.ppr_en, MRCTRL0.mr_wr, MRCTRL0.ppr_pgmpst_en and MRCTRL0.ppr_done as logic '0' and '1'

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:12.5

2.7.3 Inline ECC Test

Description:

This test case verifies that the Subsystem is supporting Inline ECC feature through APB Configuration Registers ECCCFG0, ECCCFG1.

Combinations to be Covered:

Cover below different combinations in different ranges of data:

- Cover all four logical combinations of ECCCFG0.ecc_region_map_granu.

- Cover different ranges of ECCCFG0.ecc_region_map
- Cover both logic values '1' and '0' for ECCCFG0.ecc_region_remap_en and ECCCFG0.ecc_region_map_other
- Cover both logic values '1' and '0' for ECCCFG1.ecc_region_parity_lock and ECCCFG1.ecc_region_waste_lock
- Cover both logic values '1' and '0' for ECCCFG0.ecc_ap_en, ECCCFG1.med_ecc_en and ECCCFG1.ecc_ap_mode
- Cover SLVERR response while driving transactions accessing locked regions over AXI
- Cover different wrecc_credit_cnt values
- Cover different values on dbg_dfi_ie_cmd_type
- Cover logic '0' and '1' for ecc_ap_err_intr, ecc_corrected_err_intr, ecc_uncorrected_err_intr and '01', '10' value for ecc_ap_err_intr_fault, ecc_corrected_err_intr_fault, ecc_uncorrected_err_intr_fault interrupt, perf_ie_blk_hazard.

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:13.1

2.7.4 Scrubber Status Test

Description:
This test case verifies that the Subsystem supports scrubber commands for Inline ECC through APB Configuration Registers SBRCTL, SBRSTART1, SBRSTART0, SBRRANGE0, SBRRANGE1, SBRSTART0DCH1, SBRSTART1DCH1, SBRRANGE0DCH1, SBRRANGE1DCH1.

Combinations to be Covered:
- Cover default values of SBR logic on sbr_resetn = 0.
- Cover different values of SBRCTL.scrub_interval such as below:
  SBRCTL.scrub_interval = 0
  SBRCTL.scrub_interval = PWRTMG.powerdown_to_x32
  SBRCTL.scrub_interval = PWRTMG.selfref_to_x32
  SBRCTL.scrub_interval = different values other than PWRTMG.selfref_to_x32 and PWRTMG.powerdown_to_x32.
- Cover logic '0' and '1' value of SBRCTL.scrub_en.
- Cover different values of following register fields: SBRSTART1.sbr_address_start_mask_1, SBRSTART0.sbr_address_start_mask_0, SBRRANGE0.sbr_address_range_mask_0, SBRRANGE1.sbr_address_range_mask_1.
- Cover Non-zero values of SBRCTL.scrub_interval when SBRSTAT.scrub_busy =1 and SBRSTAT.scrub_done = 0.
- Cover below combinations when SBRCTL.scrub_interval = 0:
  For read, SBRSTAT.scrub_busy =1 and SBRSTAT.scrub_done = 1
  For write, SBRSTAT.scrub_busy =0 and SBRSTAT.scrub_done = 1
- Cover logic '1' and '0' value of SBRCTL.scrub_during_lowpower during below situations:
  PWRCTL.powerdown_en=1
  PWRCTL.selfref_en=1
  PWRCTL.selfref_sw=1

Reference Information:
DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:13.2

2.8 DFI Updates

2.8.1 DFI Updates Mode Test

Description:

This test case verifies that the controller and PHY perform regular DFI updates as per the different configurations.

Combinations to be Covered:

- Cover logic '1' and '0' value for DFIUPD0.dis_auto_ctrlupd when DDRCTL is idle.
- Cover logic '1' and '0' value for OPCTRLCMD.ctrlupd
- Cover logic '1' and '0' value for OPCTRLSTAT.ctrlupd_busy
- Cover logic '1' and '0' value for DFIUPD0.dfi_phyupd_en.
- Cover different values for DFITMG0.dfi_t_ctrl_delay.
- Cover different configurations of DFIUPDTMG[0|1|2|3].

Note: Configure DFI Constraints while testing.

Reference Information:

DWC_ddrctl_lpddr54_lpddr5x_databook.pdf Section:4.2, 4.3