



Synopsys Controller IP

LPDDR5X/5/4X Memory Controller

User Guide

Product Codes

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Revision History

The following table provides a summary of changes made to this user guide.

Version	Date	Description
1.60a-lca00	May 2024	Updated: <ul style="list-style-type: none">■ Document specific version to controller version■ Figure 1-1 on page 15■ “Clocks, Resets, and Clocking Scheme” on page 84

Version	Date	Description
2.30a	April 2024	<p>Added:</p> <ul style="list-style-type: none"> ■ “Technology Cell Binding” activity in “Performing Synthesis” on page 47 ■ Added table “DFT Interface Signals” in section “Inserting Design for Test” on page 62 ■ “Duplicated Parity Bit for Register Bit of Type R/W1C and R/W1S” on page 103 ■ Appendix D, “DDRCTL Implementation Guide” for DDR54, DDR5, and DDR5LL <p>Updated:</p> <ul style="list-style-type: none"> ■ “Reference Documentation” on page 10 ■ Section “Inserting Design for Test” on page 62 ■ Section “Clocks, Resets, and Clocking Scheme” on page 84 ■ “Asynchronous FIFO Glitch Free MUX Replacement” on page 90 ■ Section “Workspace Directory Structure Overview” on page 97 ■ Structure of the document to abide with document outline guidelines: <ul style="list-style-type: none"> □ Re-organized and renamed chapters and sections □ Removed section “STAR on the Web (SotW)” as it is present in the release notes □ Removed section “Installing and Setting Up DWC_ddrctl” as it is present in the installation guide □ Added Chapter 3, “Running Design Checks” and moved sections “Running Spyglass”, “Running VC SpyGlass”, and “Running VCS XPROP Analyzer” from Chapter 2, “Configuring the Controller” and section “Running Low Power Static Verification” from Chapter 5, “Performing Synthesis and Post-Synthesis Activities” to this chapter □ Renamed appendix “CDC Methodology” to “Clock-Domain-Crossing (CDC) Synchronizers” <p>Note: Changed instances of DesignWare Cores to Synopsys IP to align with corporate naming conventions.</p>
2.20a	December 2023	Updated section “DDR Controller Product Codes”
2.10a	November 2023	Updated section “Performing Synthesis and Post-Synthesis Activities”
2.00a	April 2023	Updated section “Files Related to Synthesis Flow”
1.00a	December 2022	Initial version of the general user guide for all controller types



In some instances, documentation-only updates occur. The Synopsys IP product <https://www.synopsys.com/designware-ip.html> has the latest information.

Preface

This user guide describes the Synopsys LPDDR5X/5/4X Memory Controller. The controller, combined with Synopsys LPDDR5X/5/4X PHY, is a complete memory interface solution for DDR memory subsystems. The LPDDR5X/5/4X Memory Controller (also referred to as DDRCTL) is delivered as configurable Verilog source and is compatible with various EDA environments.

This section contains the following topics:

- “[Product Codes](#)” on page [9](#)
- “[User Guide Organization](#)” on page [9](#)
- “[Web Resources](#)” on page [10](#)
- “[Reference Documentation](#)” on page [10](#)
- “[Synopsys Statement on Inclusivity and Diversity](#)” on page [10](#)
- “[Customer Support](#)” on page [11](#)

Product Codes

[Table 1](#) lists the product codes and product names for the Synopsys DDR Memory Controller.

Table 1 DDR Controller Product Codes

Product Code	Product Name
H507-0	dwc_lpddr5x_controller
H508-0	dwc_lpddr5x_controller_afp

User Guide Organization

The chapters of this user guide are organized as follows:

- Chapter 1, “[Design Flow](#)” introduces you to the coreConsultant tool, and describes the design flow of the DDRCTL.
- Chapter 2, “[Configuring the Controller](#)” describes how to configure the DDRCTL using coreConsultant tool, generate reports and views. It also describes how to run Spyglass Link and CDC.
- Chapter 3, “[Running Design Checks](#)” provides information about running design checks.

- Chapter 4, “[Running Simulations](#)” describes the provided Packaged Verification Environment (PVE) Testbench, and how to use it to verify the DDRCTL using coreConsultant and from command line.
- Chapter 5, “[Performing Synthesis and Post-Synthesis Activities](#)” describes the synthesis flow for the DDRCTL. It also shows you how to run formal verification, use the coreConsultant tool to insert DFT, run automatic test pattern generation (ATPG), and perform static timing analysis (STA)
- Chapter 6, “[Integrating the Controller](#)” describes instantiating and integrating the DDRCTL Memory Controller into a design, and in particular how to integrate it with a Synopsys DDR PHY.
- Appendix A, “[Clock-Domain-Crossing \(CDC\) Synchronizers](#)” provides detailed information about the Clock Domain Crossing (CDC) strategy used in DDRCTL.
- Appendix B, “[Additional coreConsultant Information](#)” provides additional information about the coreConsultant.
- Appendix C, “[OCCAP Synthesis Constraints](#)” provides information on special requirements for the duplicate modules used in On Chip Command and Address Path Protection (OCCAP) feature

Web Resources

For more information, check the following Synopsys online resources:

- Synopsys IP product information: <https://www.synopsys.com/designware-ip.html>
- Your custom Synopsys IP page: <https://www.synopsys.com/dw/mydesignware.php>
- Documentation through SolvNetPlus: <https://solvnetplus.synopsys.com> (Synopsys password required)
- Synopsys Common Licensing (SCL): <https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing.html>

Reference Documentation

This document assumes familiarity with the basic terminology and concepts outlined in:

- AMBA Specification, Rev. 2.0
<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ihi0011a/index.html>
- AMBA 3 AXI Specification
<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ihi0011a/index.html>
- *Synopsys Controller IP DDR Memory Controller Databook*
- *Synopsys Controller IP DDR Memory Controller Reference Manual*



Note You need to have the ARM account to access these documents.

Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation.

as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

Customer Support

To obtain support for your product, prepare the required files and contact the support center using one of the methods described:

- Prepare the following debug information, if applicable:
 - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:
 - **File > Build Debug Tar-file**
 - For simulation issues outside of coreConsultant or coreAssembler:
 - Create a waveform file (such as VPD, VCD, or FSDB).
 - Identify the hierarchy path to the Design Under Test (DUT).
 - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- For the fastest response, enter a case through SolvNetPlus:
 - a. <https://solvnetplus.synopsys.com>



Note SolvNetPlus does not support Internet Explorer.

- b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).
 - c. Complete the mandatory fields that are marked with an asterisk and click **Save**.
Make sure to include the following:
 - **Product L1:** DesignWare Cores
 - **Product L2:** Memory - Controller
 - d. After creating the case, attach any debug files you created.
For more information about general usage information, refer to the following article in SolvNetPlus:
<https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources>
- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
 - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
 - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.
 - Attach any debug files you created.

- Or, telephone your local support center:
 - North America:
Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
 - All other countries:
<https://www.synopsys.com/support/global-support-centers.html>

Design Flow

This chapter provides an overview of the Synopsys coreConsultant tool. It also discusses the design flow of the LPDDR5X/5/4X Memory Controller.

The topics in this chapter are as follows:

- “[coreConsultant Overview](#)” on page [14](#)
- “[Design Flow](#)” on page [15](#)

1.1 coreConsultant Overview

The Synopsys coreConsultant tool allows you to configure, simulate, synthesize, and export the DDR controller to your design flow. The final output from the coreConsultant design flow is a set of RTL files (the configured RTL) and scripts to allow you to run various tools within your own design flow. The coreConsultant features and tasks include:

- A graphical user interface (GUI) to guide you through design flow activities

You can also perform all activities through a command line interface. For details, see the *coreConsultant User Guide* (see “[Help Information](#)” on page [95](#) in [Appendix B, “Additional coreConsultant Information”](#)), and Help menu in coreConsultant.

- Interactive parameter selection

The coreConsultant tool checks for consistent settings and automatically derives any dependent parameters from your choices.

- Synthesis, verification, and test vector script generation

- Testbench simulation and synthesis configuration consistent with your parameter choices

- Docbook files documenting your final configured design

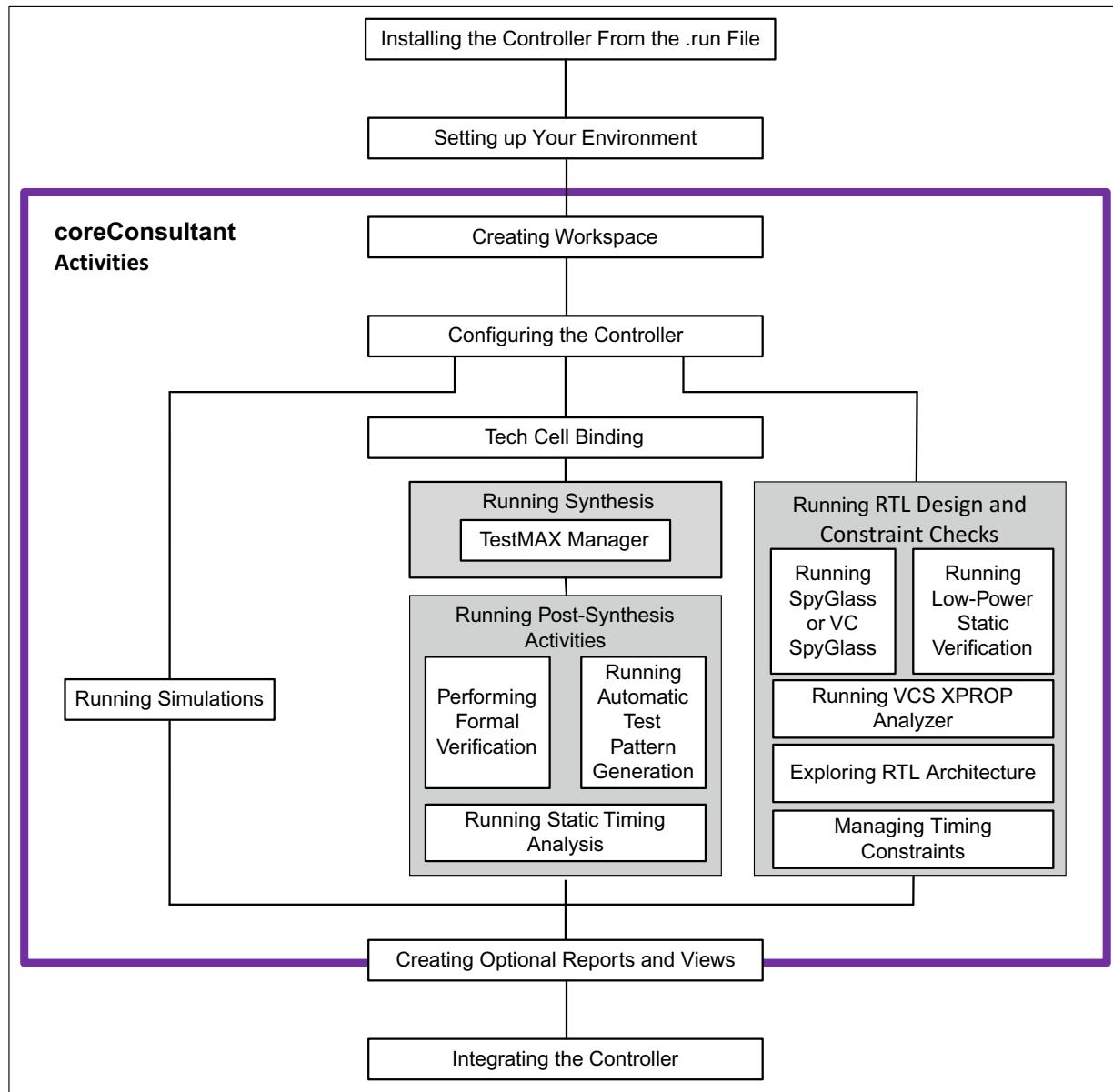
This user guide gives a more detailed information on how to configure your controller and generate RTL files, as well as running synthesis and simulation.

1.2 Design Flow

[Figure 1-1](#) gives the design flow for DDRCTL. The coreConsultant GUI guides you through the controller design flow in your workspace. A workspace is a local Unix directory structure containing your configured copy of the DDRCTL (see “[Creating the Workspace](#)” on page 19).

Most coreConsultant activities are optional and do not need to be completed before exporting the configured RTL to your chip design flow.

Figure 1-1 Design Flow



The following are the links to corresponding sections of the user guide:

- “[Setting Up Your Environment](#)” on page 18
- “[Creating the Workspace](#)” on page 19

- “Configuring the Controller” on page 17
- “Running Spyglass” on page 28
- “Important Simulation Files” on page 40
- “Synthesizing the Controller” on page 46
- “Running Automatic Test Pattern Generation (ATPG)” on page 64
- “Performing Formal Verification” on page 60
- “Running Simulations” on page 37
- “Running Static Timing Analysis” on page 66
- “Creating Optional Reports and Views” on page 24
- “Integrating the Controller” on page 71

2

Configuring the Controller

This chapter provides an overview of the step-by-step process to configure, synthesize, simulate, and export the DDR controller using the Synopsys coreConsultant tool.

The final output from the coreConsultant design flow is a set of RTL files comprising of the configured controller or an optimized gate-level netlist for custom configuration in your target technology. The output also includes scripts that allow you to run various tools stand alone within your own custom design flow. This chapter also describes how to export the controller into your chip development environment.

The topics in this chapter are as follows:

- “[Prerequisites for Configuring the Controller](#)” on page [18](#)
- “[Creating the Workspace](#)” on page [19](#)
- “[Configuring the Controller](#)” on page [21](#)
- “[Creating Optional Reports and Views](#)” on page [24](#)



Note When you are using more than one Synopsys IP, coreAssembler is recommended. The coreAssembler tool includes all of the features of coreConsultant but allows you to configure, automatically inter-connect, synthesize, and export a subsystem as opposed to a single component. For more information, see the coreAssembler documents mentioned in “[Help Information](#)” on page [95](#).

2.1 Prerequisites for Configuring the Controller

This section describes how to set up your environment and create a workspace so that you can start configuring the controller.



Note For information about the overview and architecture of the controller, see the databook.

2.1.1 Setting Up Your Environment

Before you install the DDRCTL, you must set the following environment variables:

1. Set the DESIGNWARE_HOME environment variable to your installation directory:

```
% setenv DESIGNWARE_HOME <path to c_ddrctl/DWC_ddrctl_Installation_Base_Directory>
```
2. Set either the SNPSLMD_LICENSE_FILE or the LM_LICENSE_FILE variable, if you have not already done so:

```
% setenv SNPSLMD_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
```

or

```
% setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file|port@host>
```
3. Include \$DESIGNWARE_HOME/bin in your PATH environment variable.

\$DESIGNWARE_HOME/bin is required in your PATH environment variable as it contains scripts that are necessary when using your Synopsys IP components.

For more information about setting up your environment, see the “Setting License File Environment Variable” and “Checking License Requirements” sections in the *LPDDR5X/5/4X Memory Controller Installation Guide*.



Attention

Do not proceed unless you have completed all of these steps.

2.2 Creating the Workspace

Use coreConsultant to create a workspace – your working version of the controller with a particular configuration in which you connect, configure, simulate, and synthesize your implementation of the subsystem. You can create several workspaces to experiment with different design alternatives.

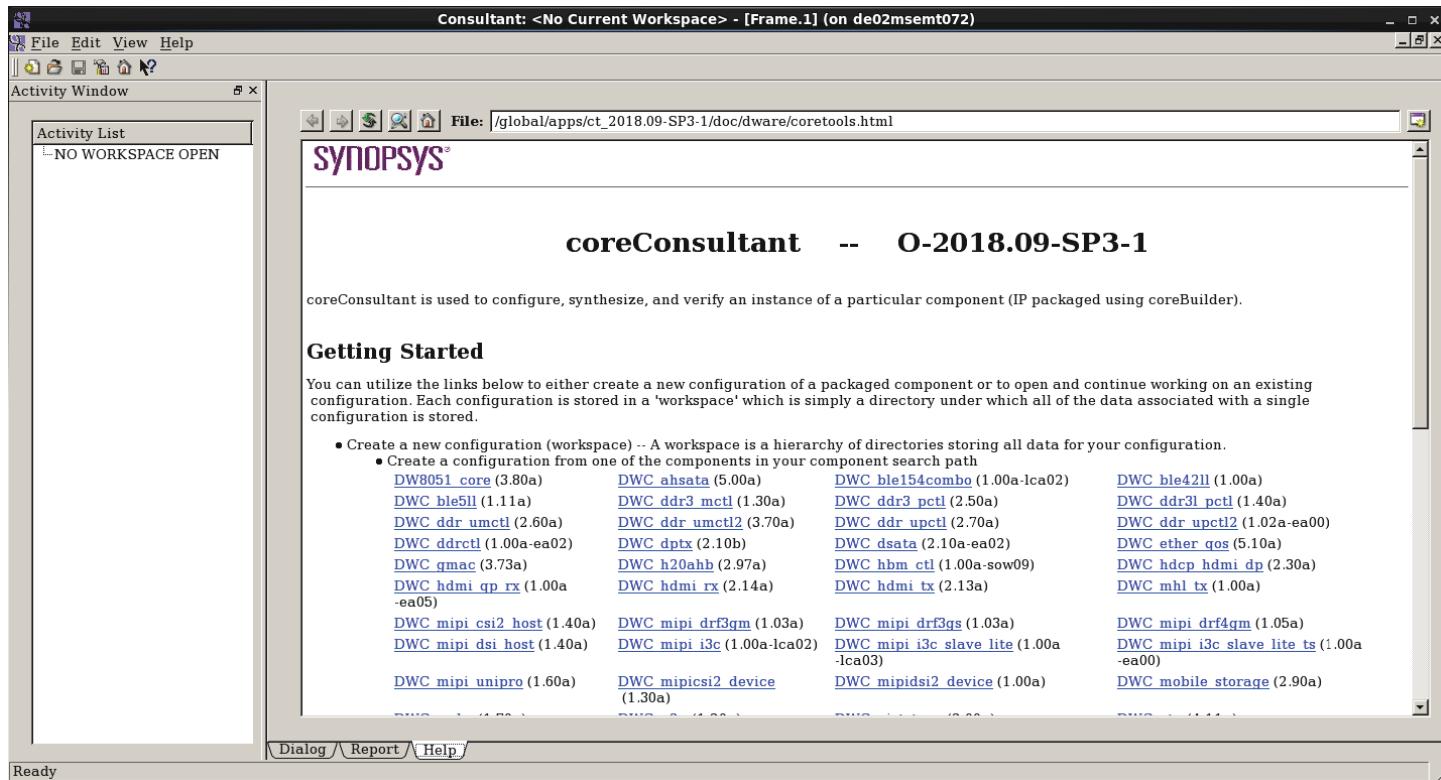
To create a workspace, follow these steps:

1. In a UNIX shell, navigate to a directory where you plan to locate your component workspace.
2. Start the coreConsultant GUI:

```
% coreConsultant &
```

[Figure 2-1](#) shows an example of the coreConsultant Welcome Page.

Figure 2-1 coreConsultant Welcome Page



3. Create a workspace.

From the Welcome page ([Figure 2-1](#)), click on the name of the IP controller that you wish to configure.



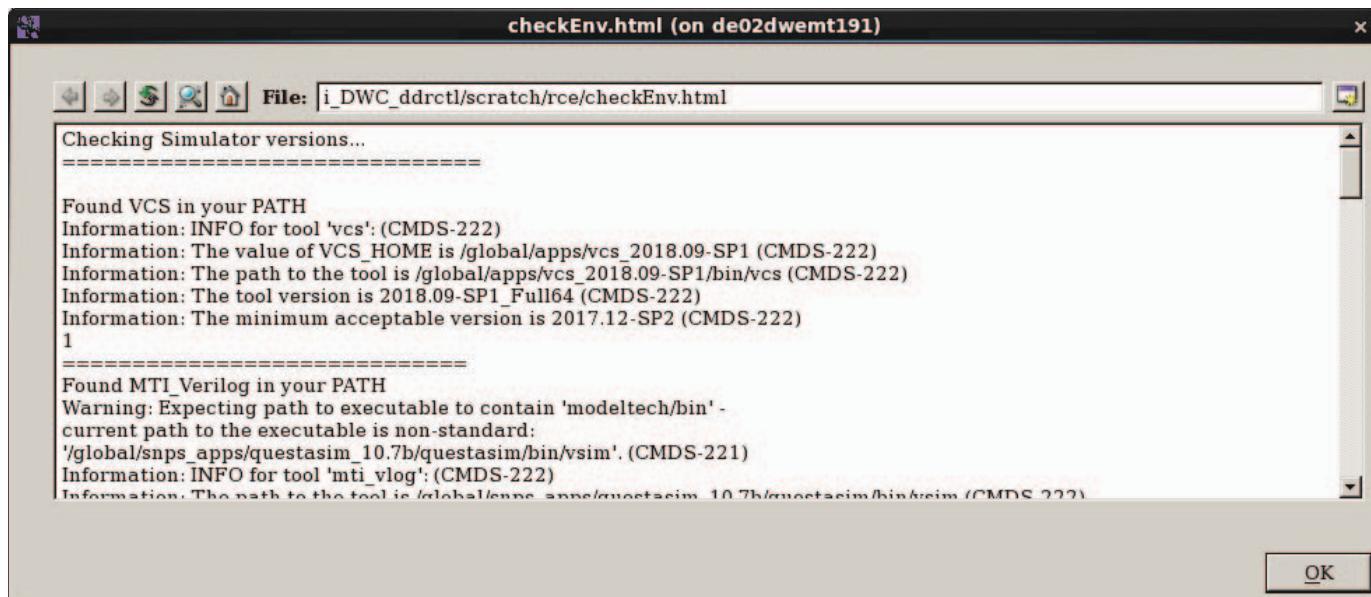
Here is a common problem that can occur:

- The DDR controller is not visible in the welcome page.

This issue is caused by not setting the \$DESIGNWARE_HOME environment variable (or by not setting it to your IP installation directory) in the shell from which coreConsultant was started. For information about setting \$DESIGNWARE_HOME correctly, refer to the LPDDR5X/5/4X Memory Controller Installation Guide.

4. Validate your installation and environment by selecting Help->Check Environment from the menu bar.
A report window shows the results (a sample is shown in [Figure 2-2](#)).

Figure 2-2 Sample Results of the Check Environment Activity

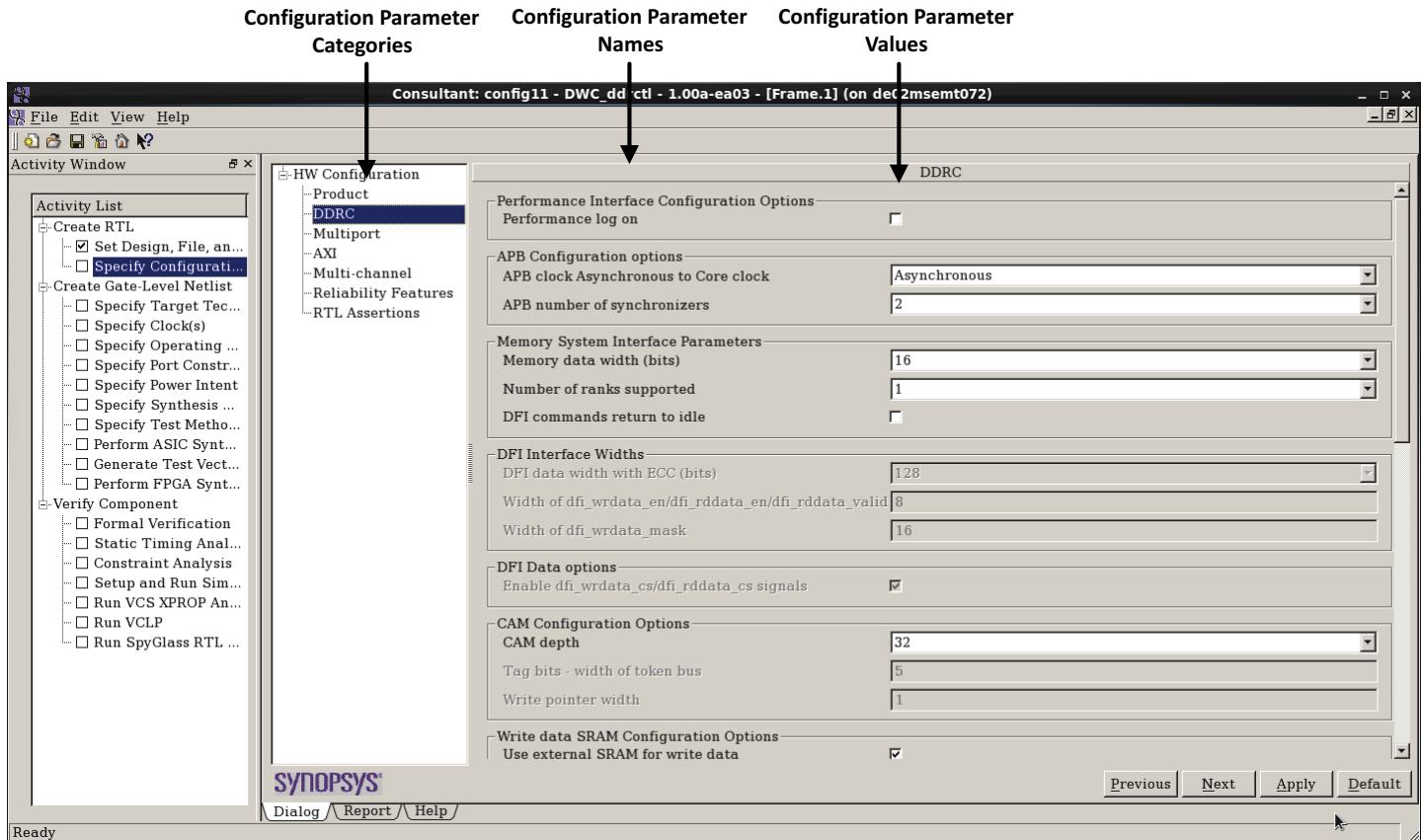


- ❑ Correct any reported errors by modifying your Unix environment setup or through the **Edit > Tool Installation Roots** menu.
- ❑ An error occurs if your \$DESIGNWARE_HOME environment variable is not set correctly. Failure to set up the \$DESIGNWARE_HOME environment variable properly before invoking coreConsultant could result in errors and unexpected IP behavior.
- ❑ To correct the \$DESIGNWARE_HOME environment variable, quit coreConsultant.
- ❑ For information about setting \$DESIGNWARE_HOME correctly, refer to the LPDDR5X/5/4X Memory Controller Installation Guide.

2.3 Configuring the Controller

After you have created a workspace, configure the controller and create the RTL using the activities under **Specify Configuration** section in coreConsultant (illustrated in the following figures).

Figure 2-3 Screenshot of coreConsultant GUI dialog to configure the IP



Complete the following steps to generate the RTL:

1. Set Design and File Prefix

The Set Design Prefix activity is already checked. This setting is used so that each design in your component has a unique name. The setting is needed only when you have two or more versions of the controller. This only changes module names; parameter names are preserved, regardless of this setting.



For the remaining steps in this chapter, we recommend to apply the default values so that the directions and description mentioned in this chapter coincide with your display. After you have used DWC_ddrctl in coreConsultant, you can then go back through these steps and change values to see how they affect the design.

Only pre-verified configurations are supported.

2. Specify Configuration

This is used to enable or disable features, to select the protocols to support, to choose the correct data width, CAM depth, and so on. Built-in checks will ensure that you choose settings that are consistent with each other.

You can access the information about each parameter by right-clicking on the parameter label and selecting **What's This?** or by selecting the **Help** tab.

3. Generate RTL

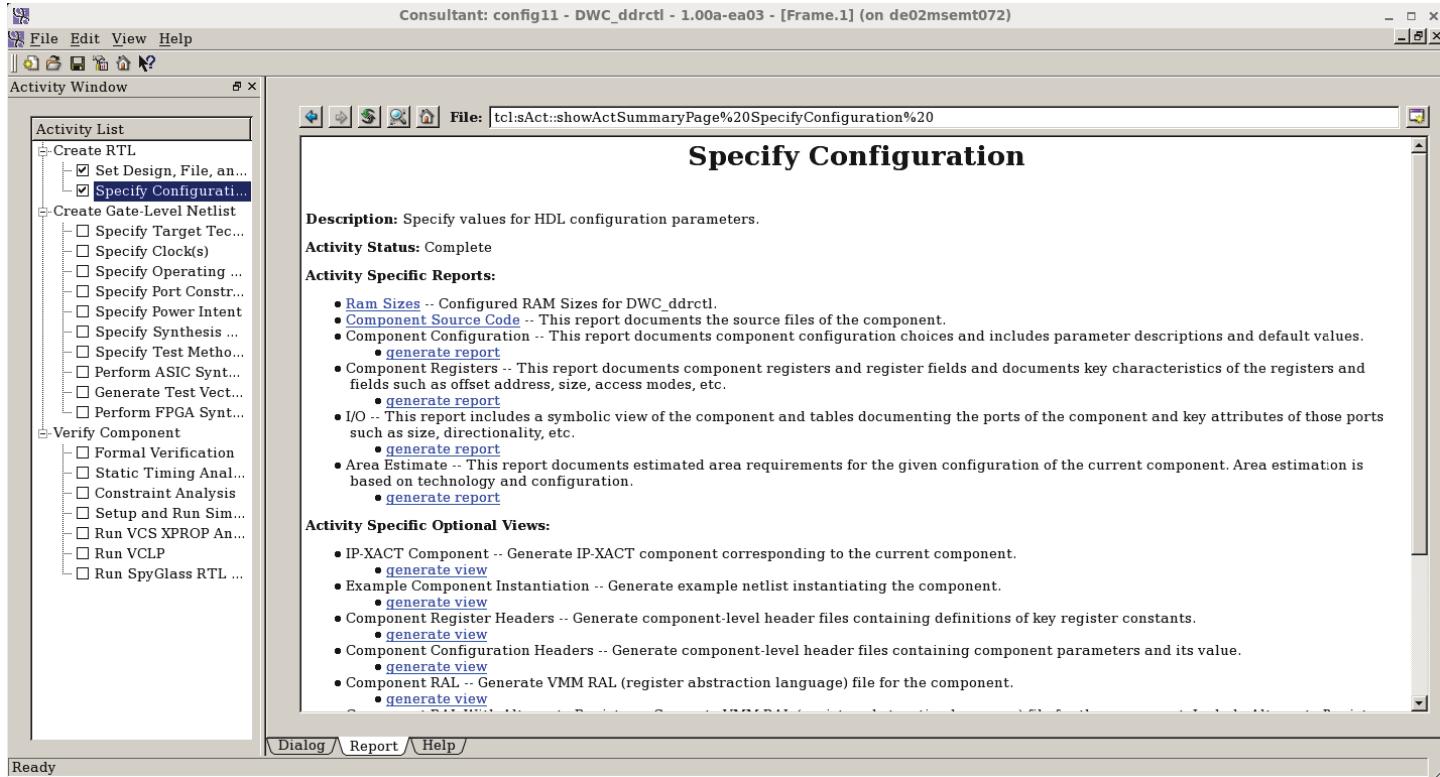
Click **Apply** to generate configured RTL code for the controller with the default values. The coreConsultant tool then checks your parameter values and generates configured RTL code in the <workspace>/src/ directory.

You can return to the Configuration activity to re-configure the controller (create new RTL) at any time. If you do so, you must complete any downstream activities again.

4. View Reports and Generate Optional Views/Reports

After you have configured the controller, coreConsultant generates several configuration reports. You can access these by clicking the **Report tab** under the **Specify Configuration** activity (see [Figure 2-4](#)).

Figure 2-4 Configuration Reports



Additionally, you can generate **Activity Specific Reports** and **Activity Specific Optional Views**. For more information, see [“Creating Optional Reports and Views”](#) on page 24. For example, to generate an IP-XACT component of the controller, click the generate view link as indicated in [Figure 2-4](#).

5. Create a Batch Script

In case you delete or overwrite your current workspace, you can create a batch script to recreate your exact configuration at a later stage. Choose the **File > Write Batch Script** menu item and enter a name for the file. This step is recommended as a batch script helps Synopsys Customer Support troubleshoot

problems you may encounter with your controller. For more information, see “[Creating a Batch Script](#)” on page [94](#).



Hint Some common problems that can occur in the **Specify Configuration** activity:

- Encrypted source code gets generated. Typically this problem is caused by not providing a Project ID when installing the DWC_ddrctl controller. You must re-install the DWC_ddrctl using the Project ID number.
 - The coreConsultant tool reports an error that it can not write certain files. Check the available storage. You may have too little storage on your server.
-



Note At this point, you can also:

- Generate a gate-level netlist (“[Synthesizing the Controller](#)” on page [46](#))
 - Verify the controller (“[Running Simulations](#)” on page [37](#))
-

2.4 Creating Optional Reports and Views

After configuring the controller, you can generate several configuration reports. The coreConsultant tool displays a list of activity-specific views you can optionally generate. You can access this list by clicking the **Report** tab, shown in [Figure 2-4](#) on page [22](#), in the **Specify Configuration** activity.



Attention Some of the activity-specific report creation may not be fully functional with your controller. For assistance, contact Synopsys Customer Support.

2.4.1 Activity-Specific Reports and Views

You can generate reports that document the I/O signals, parameters, and register descriptions.

[Table 2-1](#) describes the activity-specific optional reports.

Table 2-1 Activity-Specific Reports

Report	File Names (in <workspace>/report)	Description
Component Configuration	ComponentConfiguration.html ComponentConfiguration.xml	Documents component configuration choices and includes parameter descriptions and default values
Component Registers	ComponentRegisters.html ComponentRegisters.xml	Documents component registers and register fields; documents key characteristics of the registers and fields such as offset address, size, and access mode
I/O	IO.html IO.xml	Includes a symbolic view of the component and tables documenting the ports of the component and key attributes of those ports such as size, direction

You can also generate other reports and views such as area estimates, IP-XACT (to use IP-XACT XML format), component level header files, example component instantiation, and RAL files. These reports can be viewed through the coreConsultant Reports tab, and they are saved in the <workspace>/export directory. [Table 2-2](#) describes the activity-specific optional views.

Table 2-2 Activity-Specific Optional Views

Optional Views	File Name (in <workspace>/export)	Description
IP-XACT Component	DWC_ddrctl.xml	Generates IP-XACT component corresponding to the current component.
Example Component Instantiation	DWC_ddrctl_inst.v	Generates an example netlist that instantiates the component.
Component Register Headers	./headers/*	Generates component-level header files containing definitions of key register constants.



- To automatically generate these reports or views, select appropriate check boxes in the **File > Generate Reports or File > Generate Optional Views** dialog box.
- You can modify the schema version for IP-XACT output files by changing user's preferences as follows:
Edit -> Preferences -> IP-XACT -> Schema version for IP-XACT output files

2.4.2 Format of Activity-Specific Reports

The reports are generated in XML using the DocBook schema (an open source XML-based language). These reports are subsequently rendered in HTML applying an XSLT style sheet.

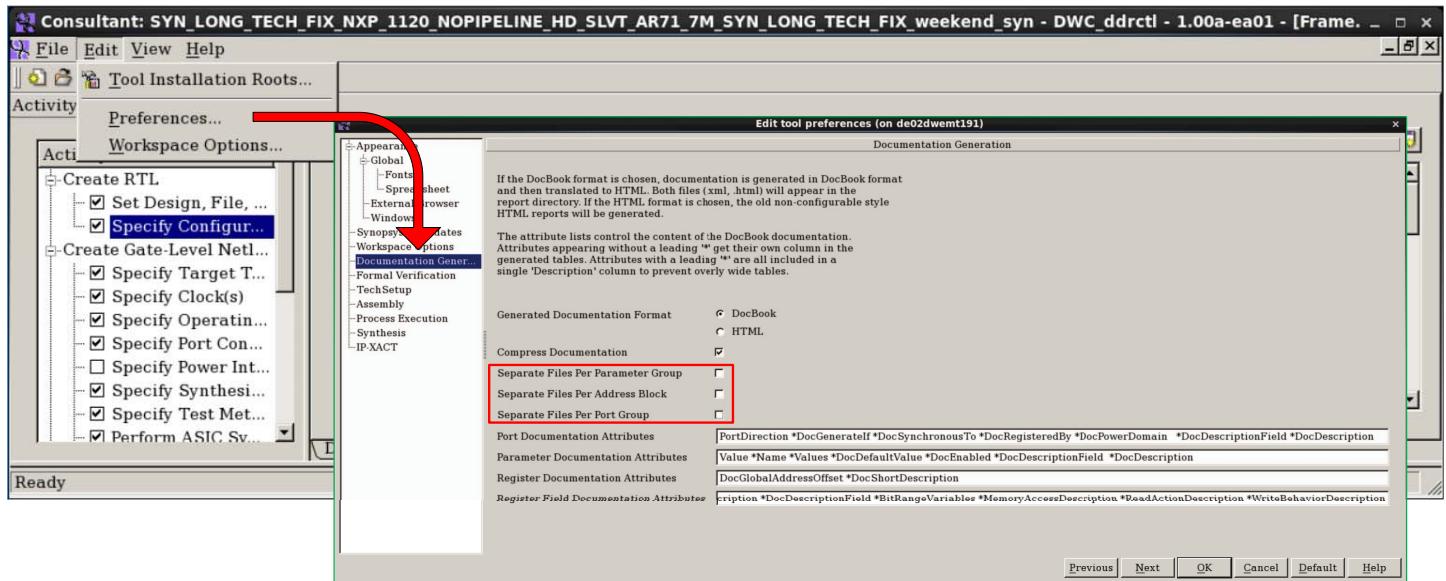
2.4.3 Setting Preferences for Report Generation

It is possible to generate reports as a single file or multiple files based on specific groups of signals and registers. To generate reports contained in a single file for easier navigation, set the preference as follows:

1. In the coreConsultant GUI, click **Edit > Preferences**.
2. In the **Edit tool preferences** window, select **Documentation Generation**.
3. Uncheck the “Separate Files Per ...” check boxes, as shown in [Figure 2-5](#).

You have to do this only once because these settings are saved in your `~/.synopsys_rt_prefs.tcl` file. You must do this before you create the reports. If you have previously created reports with old settings, delete the workspace and start again.

Figure 2-5 Separate Files Options



2.4.4 Generating Activity-Specific Reports

To generate the required report, click the respective **generate report**. For example, to generate component registers-related reports, click the one highlighted in [Figure 2-5](#).

2.4.5 Accessing Reports

To view the report, click **Reload Page** after clicking **generate report** as shown in [Figure 2-6](#).

Figure 2-6 Viewing Reports



You can also access these report files from the <your workspace>/report directory. The content of this directory is similar to that shown in [Figure 2-7](#).

Figure 2-7 Contents of the Report Directory

Name	Type
ComponentConfiguration.html	HTML Document
ComponentConfiguration.xml	XML Document
ComponentRegisters.html	HTML Document
ComponentRegisters.xml	XML Document
IO.html	HTML Document
IO.xml	XML Document

2.4.6 Generating and Accessing Activity-Specific Views

To generate the required view, click the respective **generate view** in the **Report** tab.

Access the generated views from the <your workspace>/export directory.

3

Running Design Checks

This chapter provides information about running design checks.

The topics in this chapter are as follows:

- “[Running Spyglass](#)” on page [28](#)
- “[Running VC SpyGlass](#)” on page [31](#)
- “[Running Low Power Static Verification](#)” on page [33](#)
- “[Running VCS XPROP Analyzer](#)” on page [35](#)

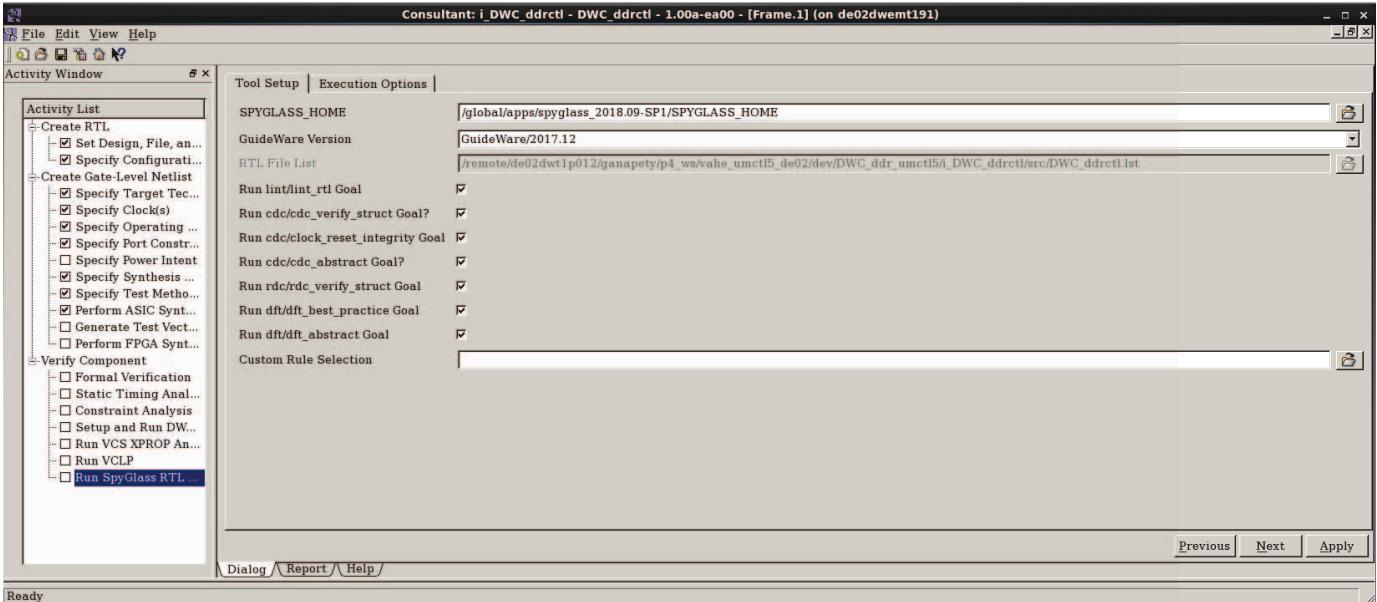
3.1 Running Spyglass

The Spyglass flow in coreConsultant runs Guideware rules for block/RTL handoff. Within the block/RTL handoff, only lint/lint_rtl and cdc/cdc_verify_struct goals are run.lc

Complete the following steps to run Spyglass Lint and CDC.

1. Select either Lint, CDC, or both run goals as shown in [Figure 3-1](#). By default, both Lint and CDC are enabled.

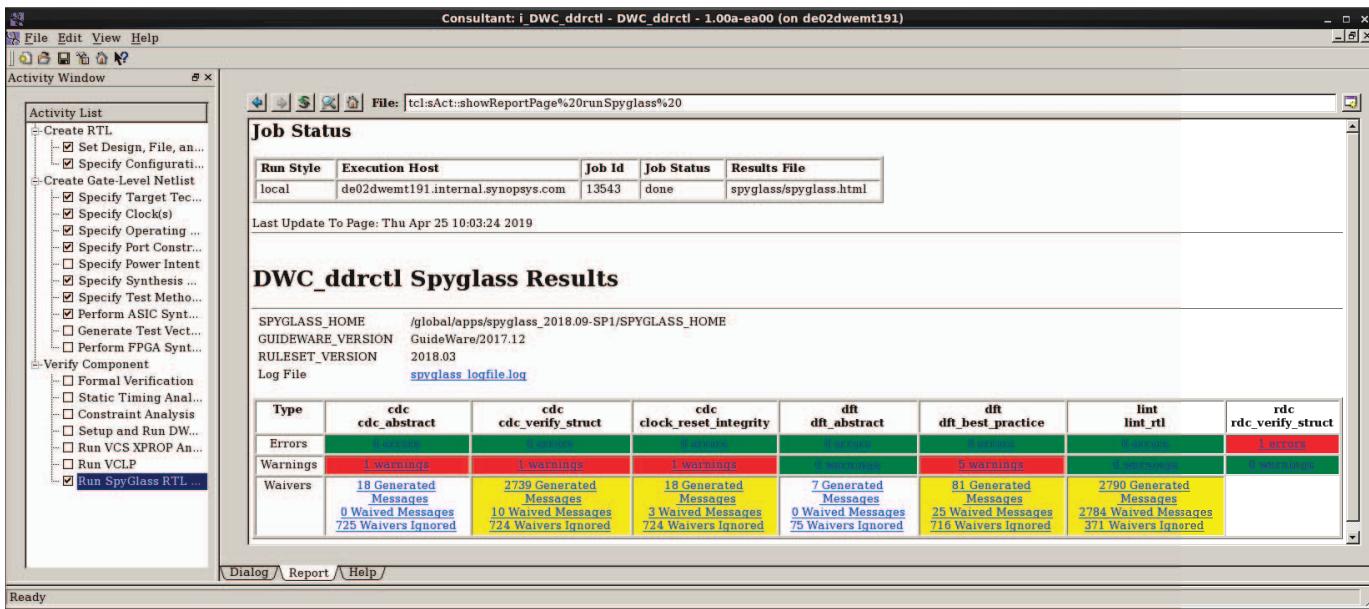
Figure 3-1 Spyglass Options in coreConsultant



2. Click **Apply** to run Spyglass.

When the Lint and/or CDC is run, the results are available in the **Report** tab. Any error is displayed with a red colored cell and any warning is displayed in a yellow colored cell as shown in [Figure 3-2](#).

Figure 3-2 Spyglass Results



3.1.1 Errors and Warnings

You may encounter errors or warnings when you run Spyglass using the coreConsultant flow because of the large number of possible configurations. For all Spyglass-related issues, open a support case to Synopsys.

Inspect the following files when the Spyglass Lint run fails with a warning:

<configured_workspace>/spyglass/work/core/consolidated_reports/<design_prefix>DWC_ddrctl_lint_1 int_rtl/moresimple_sevclass.rpt file

3.1.2 Lint

The coreConsultant tool uses the waiver files listed in [Table 3-1](#) for Spyglass Lint.

Table 3-1 Waiver Files for Spyglass Lint

File Name	Description
<configured_workspace>/spyglass/spyglass_engineering_council_waivers.tcl	These are DWC_ddrctl design specific rule waivers. There are two sections in this waiver file. The first portion is Lint waivers. The second portion is CDC waivers. The reason for each of the waivers are included as comments in the file.
<configured_workspace>/spyglass/spyglass_engineering_council_waivers.tcl	These are rules which Synopsys waives for its IPs.

3.1.3 CDC

To understand the Spyglass CDC constraints, you must understand the reset and clock logic used in DWC_ddrctl.

For more information, see:

- The Clock And Reset Requirements section in the Product Overview chapter of the LPDDR5X/5/4X Memory Controller Databook.

3.1.3.1 CDC Files

The coreConsultant tool uses the files listed in [Table 3-2](#) for Spyglass CDC.

Table 3-2 Waiver Files for Spyglass CDC

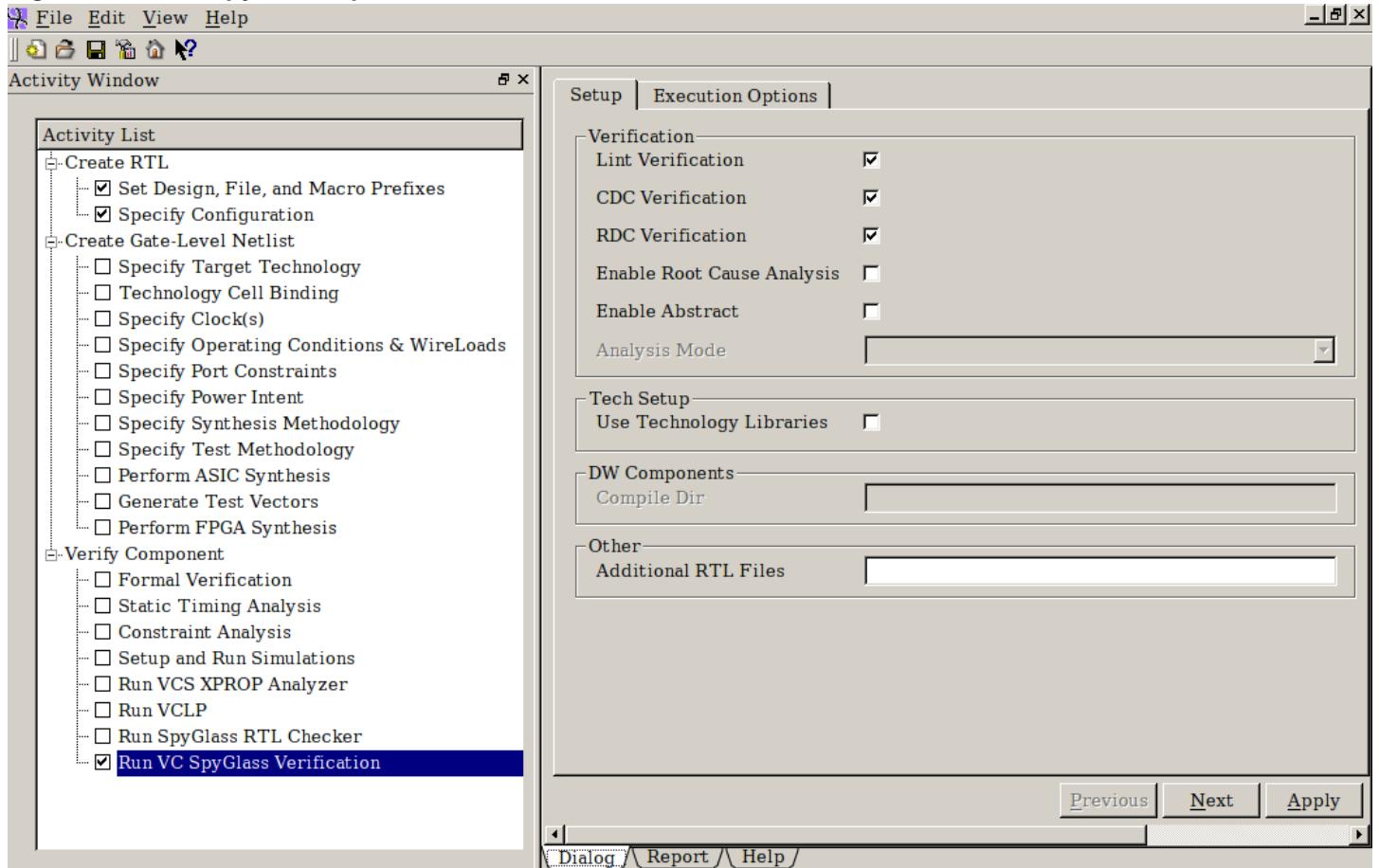
File Name	Description
<configured_workspace>/spyglass/manual.sgdc	These are the constraints pertaining to a given mode.
<configured_workspace>/spyglass/ports.sgdc	These are the list of I/O signals and their respective clocks.
<configured_workspace>/spyglass/spyglass_design_specific_waivers.swl	<p>These are DWC_ddrctl design specific rule waivers. The following sections are present in this waiver file:</p> <ul style="list-style-type: none"> ■ Lint waivers ■ CDC waivers <p>The reasons for each waiver are included as comments in the file.</p>
<configured_workspace>/spyglass/spyglass_engineering_council_waivers.tcl	These are rules which Synopsys waives for its IPs.

3.2 Running VC SpyGlass

The VC SpyGlass flow in coreConsultant runs Lint, CDC, and RDC verifications. Follow these steps to run VC SpyGlass Lint, CDC, and RDC verification.

1. Select all the required verification options (that is, Lint, CDC or RDC).

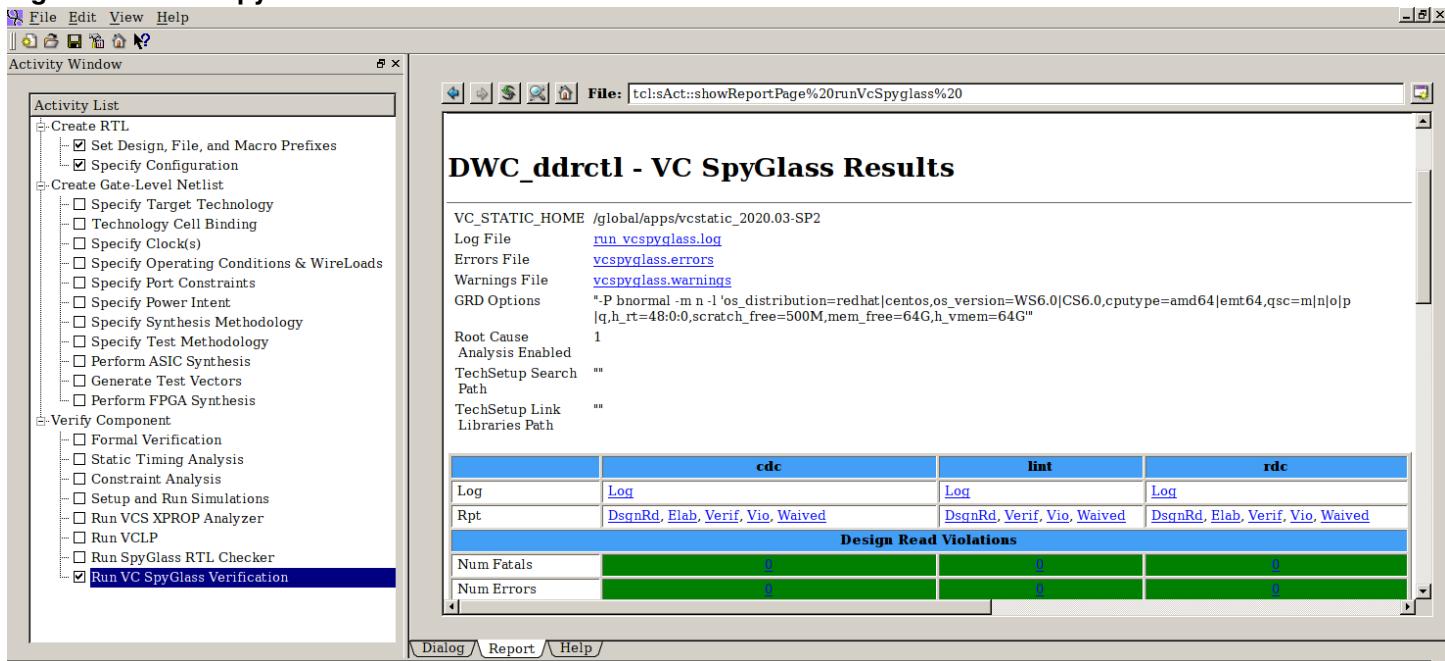
Figure 3-3 VC SpyGlass Options in coreConsultant



2. Click Apply to run the selected verification goal.



Note 'Enable Root Cause Analysis', 'Enable Abstract', 'Use Technology Libraries', and 'Additional RTL Files' options in VC SpyGlass Verification section are not fully tested in the coreConsultant environment.

Figure 3-4 VC SpyGlass Results

3.2.1 Errors and Warnings

Inspect the following files when the VC SpyGlass run fails with an error/warning.

Lint: <configured_workspace>/vcspyglass/lint/verification.violated.rpt

CDC: <configured_workspace>/vcspyglass/cdc/verification.violated.rpt

RDC: <configured_workspace>/vcspyglass/rdc/verification.violated.rpt

3.2.2 Waivers and Constraints Used

The following waiver and constraint files are used by VC SpyGlass for running the verification.

Waivers:

- vcspyglass/constraints/waivers.tcl

Constraints:

- vcspyglass/engineering_council/vcspyglass_bcm_constraints.tcl
- vcspyglass/constraints/DWC_ddrctl.sdc
- vcspyglass/constraints/resets.tcl
- vcspyglass/constraints/constraints.tcl

3.3 Running Low Power Static Verification

Low power static verification can be performed using Synopsys VC Low Power (VC LP) tool. You can run VC LP in the coreConsultant GUI (see [Figure 3-5](#)).

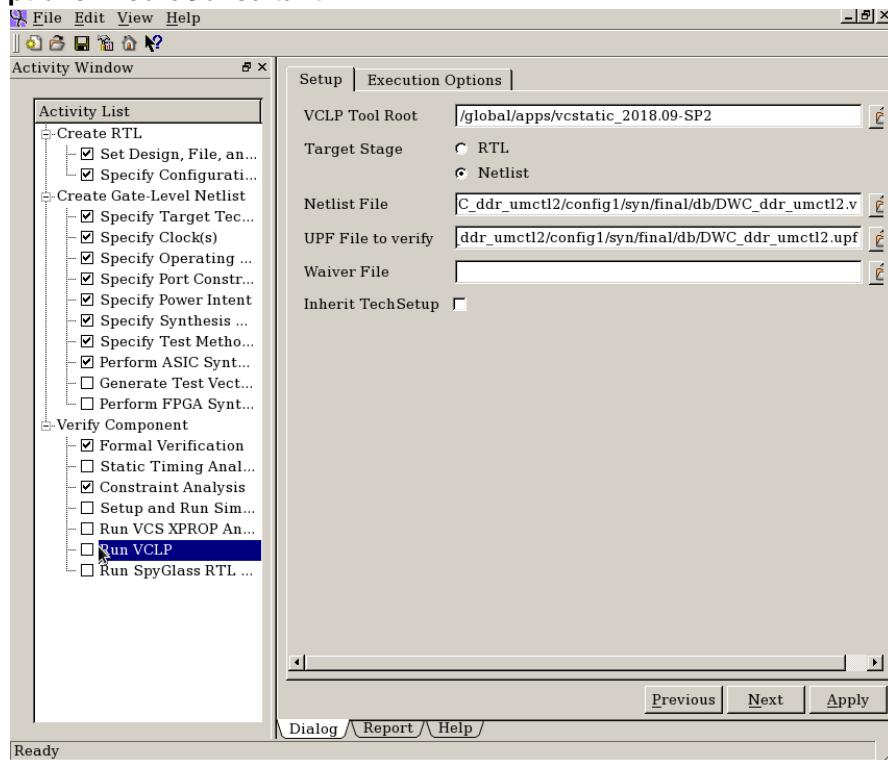
The VC LP flow in coreConsultant runs the following Low Power Checks either on the RTL or netlist:

- Power Intent Consistency Checks
- Signal Corruption Checks
- Structural Checks
- Power and Ground (PG)
- Checks and Functional Checks

For details on each of the checks, refer to the VC Low Power User Guide, which is available at the following location:

https://solvnet.synopsys.com/dow_retrieve/latest/ni/vc_static.html

Figure 3-5 VC LP Options in coreConsultant



To run VC LP, complete the following steps:

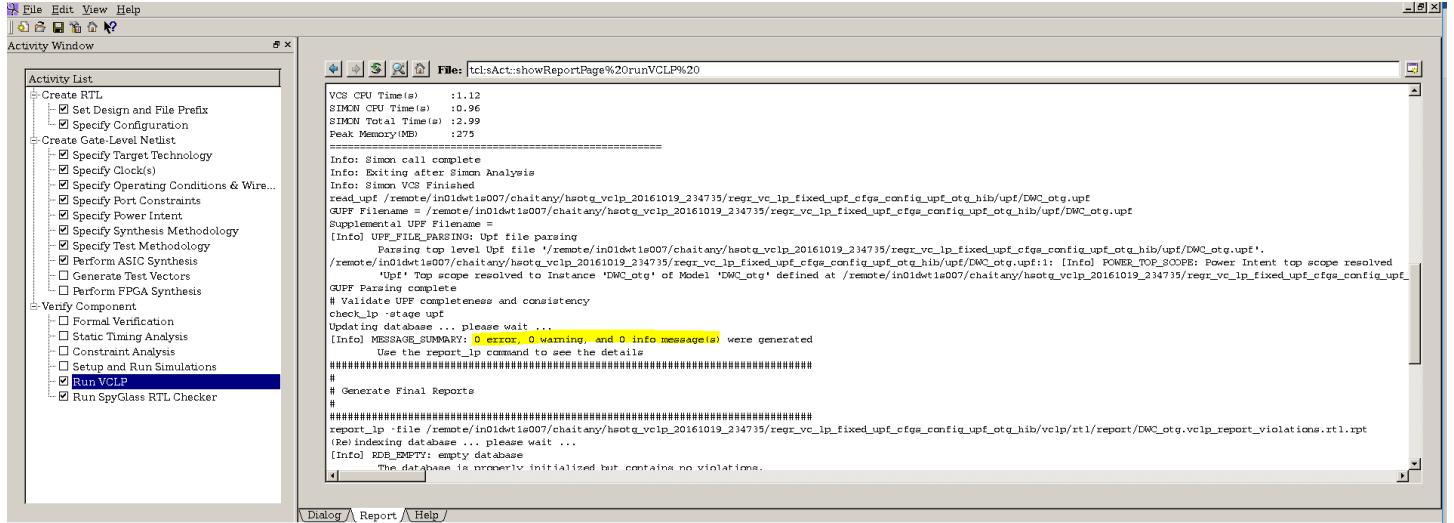
1. Select Verify Component> Run VCLP activity.
2. In the Setup tab, complete the following fields:
 - ❑ VCLP Tool Root: Specify the complete path for the VC LP tool.
 - ❑ Target Stage: Select either RTL or Netlist stage.
 - For RTL stage, specify the location of the *.upf file.

- For Netlist stage, specify the location of the netlist and the upf prime file (UPF output of Design Compiler).

3. Click Apply.

On completion, the results are available in the Report tab. Go to the report summary, and check for any errors/warnings as shown in [Figure 3-6](#). For debugging the warnings/errors, refer to the *VC Low Power User Guide*.

Figure 3-6 VC LP – Sample Report Summary



The screenshot shows the Synopsys Visual Compiler Low Power (VC LP) software interface. The window title is "File: tclsAct:showReportPage%20runVCLP%20". The left sidebar lists various design steps under "Activity List", with "Run VCLP" selected. The main pane displays a command-line log of the simulation process. Key log entries include:

```

VCS CPU Time(s) : 1.12
SIMON CPU Time(s) : 0.96
SIMON Total Time(s) : 2.99
Peak Memory(MB) : 275
=====
Info: Simon call complete
Info: Exiting after Simon Analysis
Info: Simon VCS Finished
read_upf /remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_otg_hib/upf/DWC_otg.upf
UPF Filename = /remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_otg_hib/upf/DWC_otg.upf
Supplemental UPF Filename =
[Info] UPF_FILE_PARSING: Upf file parsing
    Parsing top level Upf file '/remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_otg_hib/upf/DWC_otg.upf'.
    /remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_otg_hib/upf/DWC_otg.upf:1: [Info] POWER_TOP_SCOPE: Power Intent top scope resolved
        'Upf' Top scope resolved to Instance 'DWC_otg' of Model 'DWC_otg' defined at /remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_
        UPF Parsing complete
# Validate UPF completeness and consistency
check_lp_status.gpt
Updating database ... please wait ...
[Info] MESSAGE SUMMARY: 0 error, 0 warning, and 0 info message(s) were generated
    Use the report_lp command to see the details
=====
#
# Generate Final Reports
#
=====
report_lp -file /remote/in0ldwt1s007/chaityany/hspotq_vcclp_20161019_234735/regr_vc_lp_fixed_upf_ctqg_config_upf_otg_hib/vclp/r1/report/DWC_otg.vclp_report_violations.r1.rpt
(Re)indexing database ... please wait ...
[Info] IDE_EMPTY: empty database
    The database is currently initialized but contains no violations.

```

3.4 Running VCS XPROP Analyzer

After generating the RTL in the Specify Configuration activity, you can run the Xprop feature of the VCS simulator in the coreConsultant environment to check for the instrumentation capabilities of Xprop on the generated RTL. The RTL is analyzed with relevant VCS switches. You can check the resulting log file to ensure the RTL is 100% instrumented. For more details on VCS Xprop, see the VCS documentation.

Running VCS Xprop Analyzer

You must configure the controller (see “[Configuring the Controller](#)” on page 21) before starting this task. To run the VCS Xprop analyzer on your controller, complete the following steps in the Run VCS Xprop Analyzer activity (see Figure 2-15).

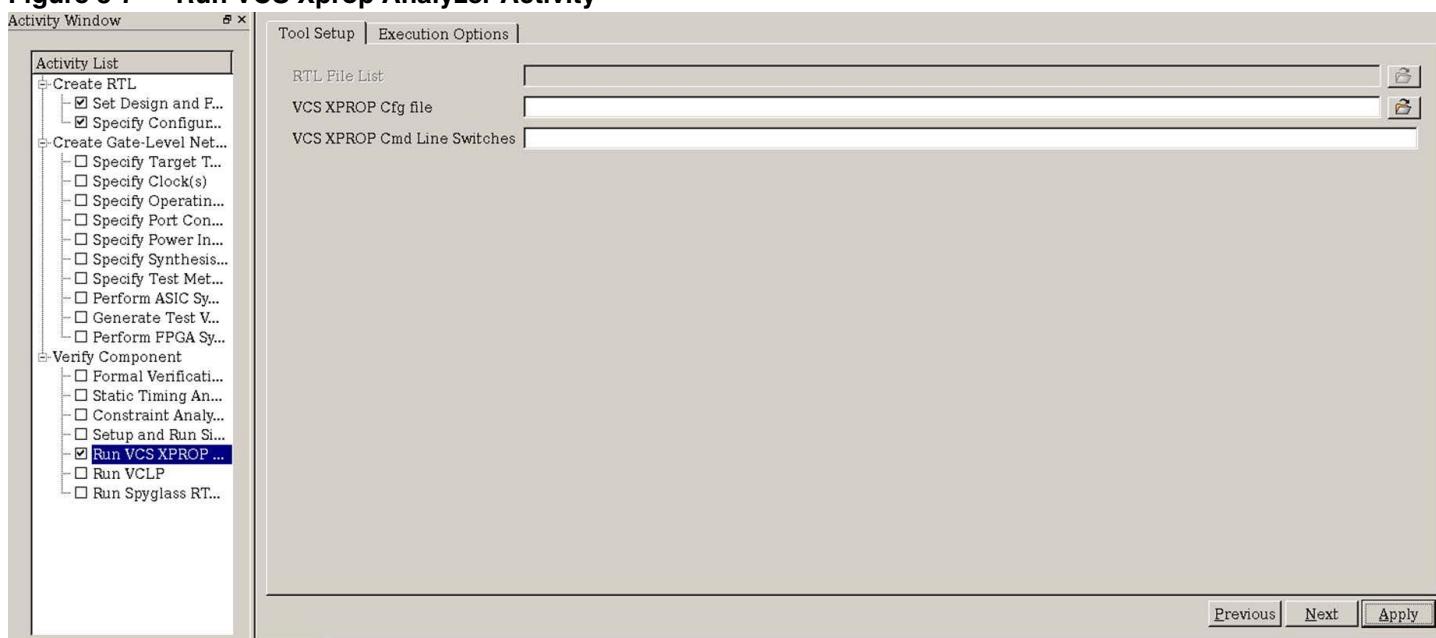
- **Specify Command Line Switches**

The following command line switches can be passed to VCS. By default, you do not need to specify any argument; you can leave these fields blank.

- **VCS Xprop Cfg File:** Specify the full path of the xprop config file that you want to pass to VCS as `-xprop=<CfgFile>`.
By default, you do not need to specify any file; you can leave this field blank.
- **VCS Xprop Cmd Line Switches:** You can also specify any additional switches that you want to pass to the VCS command line when running the VCS executable. By default, you do not need to specify any additional switches; you can leave this field blank.

- Click **Apply** to run the VCS Xprop Analyzer activity.

Figure 3-7 Run VCS Xprop Analyzer Activity



Checking VCS Xprop Analyzer Results

- Click the **Report** tab.
- Click the **Run VCS Xprop Analyzer Summary** link.

In the opened spreadsheet, the **Instrumentation** row should show 100%. If it is not 100%, then additional information will be provided for the non-instrumented statements.

4

Running Simulations

This chapter provides information about the UVM-based Packaged Verification Environment (PVE) Testbench that is provided with the DDR Controller IP. The PVE provides a starting point for understanding how to use Synopsys Verification IP (VIP) and the configured DDR controller together in your DDRCTL verification environment.

This chapter discusses the following topics:

- “[PVE Testbench](#)” on page 38
- “[Running the Simulation from coreConsultant](#)” on page 40
- “[Running the Simulation from Unix Command Line](#)” on page 42
- “[CINIT/SINIT Software](#)” on page 43

4.1 PVE Testbench

The PVE is a testbench written using UVM 1.2 base classes, making use of latest best in class verification IP to provide a scalable test vehicle for DDR products from Synopsys. It is an environment that simulates both Synopsys DDR Controllers and DDR PHYs together in a memory subsystem using Synopsys SVT memory models and other verification IPs. The PVE makes use of C-reference code for both controller and PHY initialization.



Note Third-party simulators and third-party memory models are not supported.

4.1.1 PVE Testbench Details

The information in this section is a summary; more detail is provided in HTML reference pages which are auto-extracted from PVE source code at the following location: <ws>/doc/html/pve.

4.1.2 PVE Testbench Files

Table 4-1 provides the locations and short descriptions for PVE Testbench files.



Note The sim directory is not fully populated until applying the Simulate Activity.

Table 4-1 PVE Testbench Files Locations and Descriptions

Directory	Description
sim/testbench	Top-level test-bench directory
sim/testbench/module	All test-bench Verilog modules including the PVE top-level wrapper file ddr_uvm_pve_tb_top.sv)
sim/testbench/tests	All UVM test-cases
sim/testbench/env	UVM top-level environment files
sim/testbench/macros	All test environment compile macro
sim/sw_utilities/cinit	Controller Initialization C files
sim/sw_utilities/phy	PHY initialization C files

4.1.3 List of PVE Tests

The test suite provided with the PVE is for demonstration purposes only. The controller IP is fully verified internally by Synopsys R&D teams. The tests provided are just a subset to help you in understanding certain features and as a guide for integration.

The list of tests can be found in HTML pages packaged with the controller IP.

4.1.4 PVE Test Case Details

Test case details can be found in HTML pages packaged with the controller (<ws>/doc/html/pve).

4.2 Running the Simulation from coreConsultant

To run the PVE in the coreConsultant GUI, select the *Verify Component/Setup and Run DWC_ddrctl Simulation*.

4.2.1 Running the Simulation

You can select the PHY type, memory model, and bus width, tests in the ‘Testbench’ options panel. Click Apply to start simulation jobs. A SIMV executable is compiled for each protocol; each test runs in a separate test directory. The directory name will be suffixed by the protocol in operation automatically.

4.2.2 Test Cases

Test case details can be found in HTML reference pages packaged with the controller.

4.2.3 Important Simulation Files

The log files produced by simulation are post-processed by runtest (PERL script) and a pass/fail status is determined. Some important files in the test directory are as follows:

Table 4-2 Important Simulation Files

Filenames	Description
compile.log	VCS compilation log file
test.log	VCS Simulation log file
dwc_ddrctl_cinit.log	CINIT debug log file
phyinit.log	PHYINIT output log file
test.error	If the test fails this will contain the first error
test.startsim	The main invocation script to begin the simulation
test.simcommand	VCS compile options
test.plusarg	VCS simulation runtime arguments, check this files for optional debug switches. For example +VIP_ENABLE_APB_TRACING=1 will enable APB log file containing CINIT and PHYINIT programming commands

4.2.4 Checking Simulation Status and Results

To check simulation status and results, click the Report tab; coreConsultant displays a dialog that indicates:

- Your selected Run Style (local, lsf, grd, or remote)
- The full path to the HTML file that contains your simulation results
- The name of the host on which the simulation is running
- The process ID (Job Id) of the simulation
- The status of the simulation job (running or done)

The Results dialog also enables you to kill the simulation (Kill Job) and to refresh the status display in the results dialog (refresh status).

The Results information includes:

- Simulation execution messages
- A pass or fail result

The runtest.html file in workspace/sim includes all of the results of the simulations. When multiple different tests are selected, this file contains the concatenated results of all these simulations (tests). Individually, each test's unique output can be found in the workspace/sim/test_testname/test.log file. The runtest.html file, presents the information in the following categories:

- Verification Activity Log: A log of the simulation activity
- Testbench Preparation: A list of runtest options that were executed during the simulation
- Simulation Execution: Provides the output of each simulation (test); this information is also saved to test.log in workspace/sim/test_testname
- Simulation Results: Includes the time the simulation completed, the path to test.log, how many errors were encountered and the overall result of each simulation

The workspace/sim/test_testname directory includes the various log files that are unique to a given test/simulation. The following output files are included at this level:

- test.log: Output of the testbench and includes specifics about the simulators used, transaction monitor and self checker messages, including error messages
- test.result: Summary report indicating whether the test PASSED or FAILED and when it failed, details about the failure (such as timestamp, expected response, actual response)
- uvm_ddr_pve_tb_top.fsdb or uvm_ddr_pve_tb_top.vpd: Waveform dump file when enabled through the simulation options
- dwc_ddrctl_cinit.log.gz: is a log file in which CINIT debug messages are printed along its execution
- dwc_ddrctl_apb.log.gz: The register settings logged in this file can be used as a guide to how to program the DDRCTL and PUB registers. While the registers are correct for the selected configuration and speed grade, they are not guaranteed to give optimum utilization and latency performance. To achieve optimum performance requires an analysis of the configuration and traffic patterns.



Note dwc_ddrctl_apb.log is created by a custom callback added to the APB VIP monitor.

4.3 Running the Simulation from Unix Command Line

To run PVE test cases from the Linux command line, the workspace must be fully populated first. This means that the RTL and testbench files are written out to a workspace ready for simulation. This can be done using the GUI or by running a coreConsultant batch file. You can prevent any simulations from running in the GUI by setting "DryRun=1" simulate activity parameter.

When the workspace directory is populated with a configured design, each test can be run from the command line by using the following simple steps:

```
% cd <path_to_cC_workspace>/sim/<test_name>  
% ./test.startsim -recompile -fsdb
```



Note Your environment must be configured correctly in order for these commands to be successful.

4.4 CINIT/SINIT Software

The Synopsys DDR/LPDDR CINIT is a software packaged designed for generation of initialization sequence for the DDR/LPDDR controllers based on the selected configuration.

For details about using the CINIT/SINIT software, see “Synopsys Controller IP DDR/LPDDR CINIT User Guide”.

Performing Synthesis and Post-Synthesis Activities

This chapter discusses the following topics:

- “[Synthesizing the Controller](#)” on page [46](#)
- “[Performing Formal Verification](#)” on page [60](#)
- “[Inserting Design for Test](#)” on page [62](#)
- “[Running Automatic Test Pattern Generation \(ATPG\)](#)” on page [64](#)
- “[Running Static Timing Analysis](#)” on page [66](#)

5.1 Synthesizing the Controller

The coreConsultant tool is your interface to Synopsys synthesis tools for ASIC synthesis of the controller. If you want to access the synthesis scripts for exporting to your chip database, then refer to “[Exporting Controller to Your Chip Design Database](#)” on page [72](#).

During the **Create Gate-Level Netlist** activity in coreConsultant, you can also perform Physical Synthesis, and Design For Test. Instructions for these tasks are provided in this section.

The topics in this section are as follows:

- “[Performing Synthesis](#)” on page [47](#)
- “[Checking Synthesis Results](#)” on page [57](#)
- “[Running Synthesis from a Unix Shell](#)” on page [58](#)
- “[Troubleshooting: Common Problems in this Step](#)” on page [58](#)



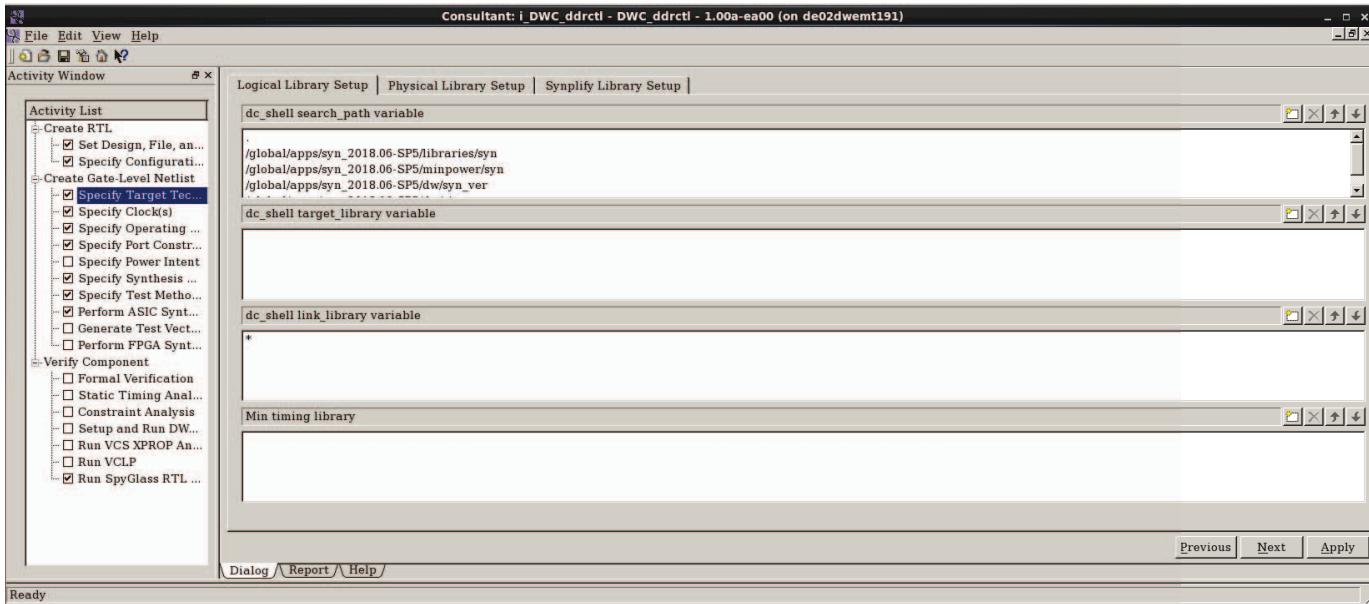
Hint Before you begin the **Create Gate-Level Netlist** activity, check that you have the latest tool versions installed and your environment variables set up correctly as detailed in the LPDDR5X/5/4X Memory Controller Installation Guide.

To check your tools, click the **Help > Check Environment** menu item. Correct any reported errors by modifying your Unix environment setup or through the **Edit > Tool Installation Roots** menu.

5.1.1 Performing Synthesis

Configure the controller (see “[Configuring the Controller](#)” on page 17) before starting this task. To synthesize your controller and create a gate-level netlist, select the **Create Gate-Level Netlist** activity as shown in [Figure 5-1](#).

Figure 5-1 Create Gate-Level Netlist Activity



1. Specify Target Technology

When you click on **Create Gate-Level Netlist**, the first step in this activity is **Specify Target Technology**. A target library must be specified, otherwise, errors occur in coreConsultant.

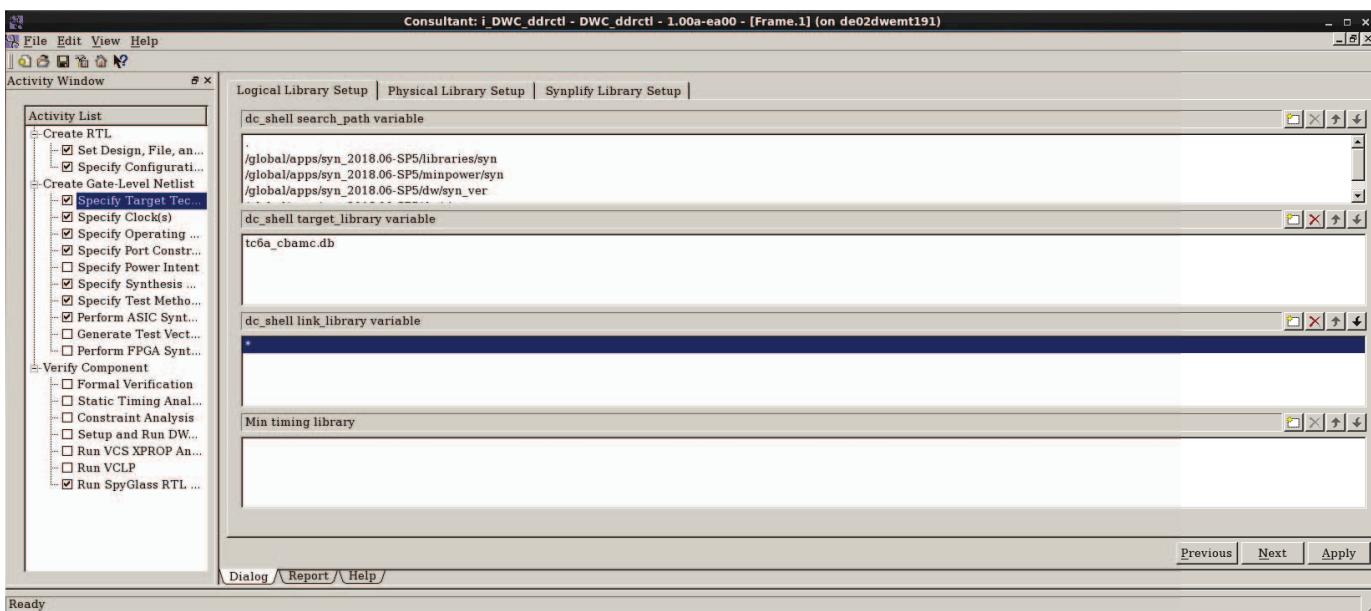
- **ASIC Synthesis**

For ASIC synthesis, use a target technology of .18 microns or less. To add variables and libraries to the dialog fields, click the folder icon (as shown in [Figure 5-2](#) on page 48) and use the navigation tool. The default values for the search_path and link_library do not normally need to be changed.



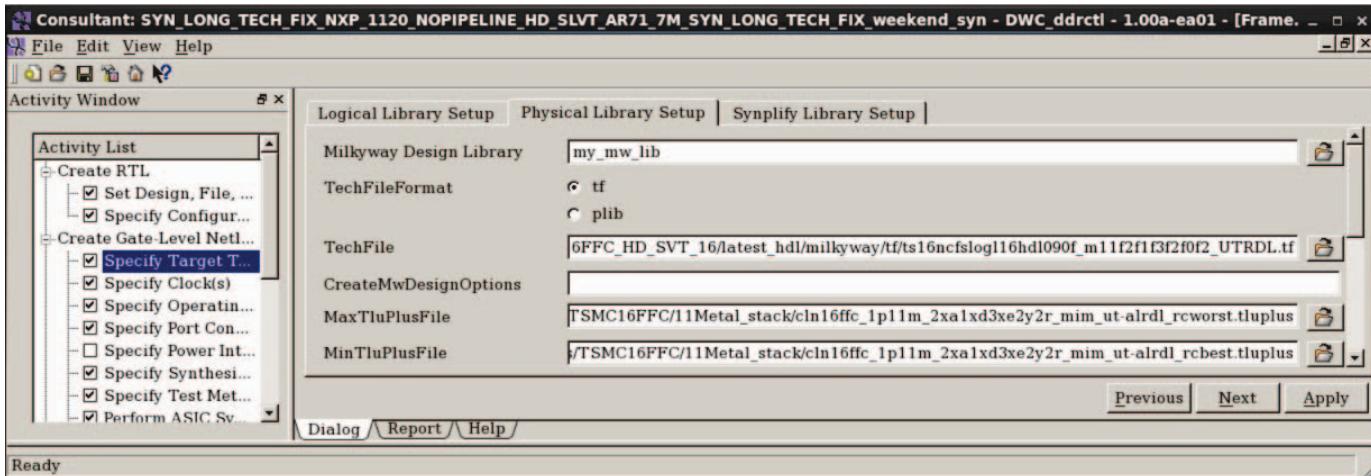
link_library should always contain '*' and all the specified files.

If you intend to use the Fusion_Compiler_Reference_Methodology as Strategy in the "Perform ASIC Synthesis" step, libraries that are compatible with FC need to be specified in this step. Otherwise, the option to select Fusion_Compiler_Reference_Methodology will not be available.

Figure 5-2 Specify Target Technology – Logical Library Setup

■ Physical Synthesis

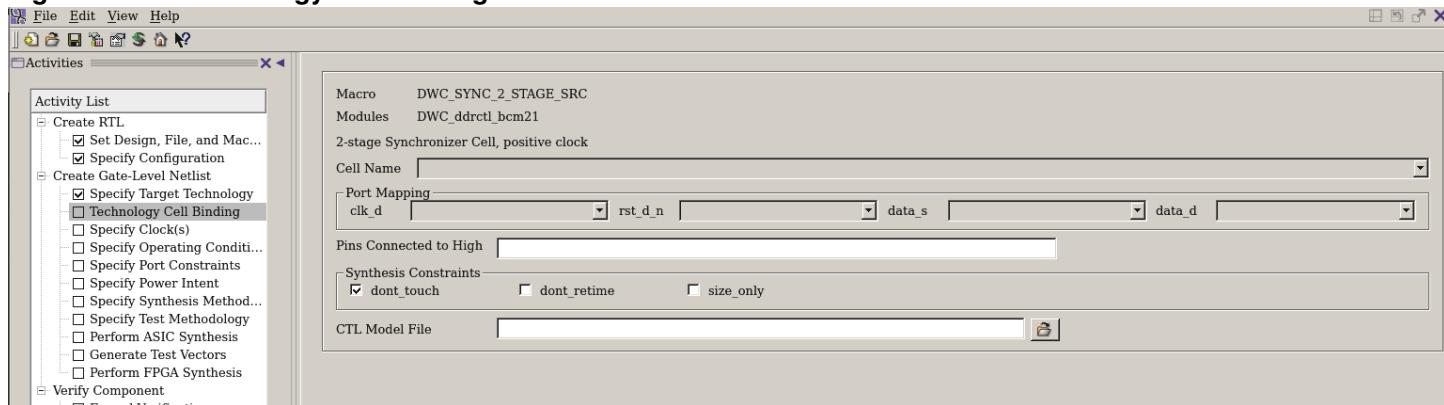
If you are running Physical Synthesis, then you must specify the physical library under the **Physical Library Setup** tab (Figure 5-3). You specify a Milkyway Reference Library and Milkyway Technology File when you enable Physical Synthesis during the Specify Target Technology activity. This may be .tf or .plib file. You may also provide optional files (TLUPlus), which allow the tools to model Deep Submicron effects with greater accuracy.

Figure 5-3 Specify Target Technology – Physical Library Setup

2. Technology Cell Binding

Certain modules in the RTL can be mapped to technology cells. This allows users to instantiate their selected technology library cells directly in the BCM source files.

The modules that can be mapped are identified in the “Technology Cell Binding” activity in coreConsultant, where it is possible to specify the technology library cell that will be used to replace the synchronizer module.

Figure 5-4 Technology Cell Binding

Design parameter synchronizer depths from 2 to 4 are supported and the replacement will use the optimal combination of the configured technology library stage-cells.

This activity will update the source code of the relevant modules to define the required macros that enable the instantiation of the selected technology cells.

Technology library instance pins not listed in the Port Mapping that need to be connected to a pull-up must be listed in “Pins Connected to High”, as otherwise synthesis will automatically connect them to a pull-down. For example, Preset active-low pins.

CTL Test Model must be provided for proper scan insertion of the technology synchronizer cells.



Note Only synchronization cells equivalent to the synchronizer depth design parameters will be available. A design parameter set to depth 4 requires a depth-3 synchronizer and a depth-1 synchronizer.

3. Specify Clock(s)

In **Create Gate-Level Netlist -> Specify Clock(s)** activity, the default Cycle Time for the input clocks is provided in [Table 5-1](#). These times match the DWC_ddrctl default clock-rate configuration (400 MHz).

Table 5-1 Default Cycle Time for DWC_ddrctl

Clock	Cycle Time
core_ddrc_core_clk	2.5

- ❑ Design for Test (DFT)

These clocks are also selected as ‘Test Clock’.

- ❑ ASIC/Physical

The default values for other clock-related synthesis attributes provide acceptable synthesis results in most libraries.

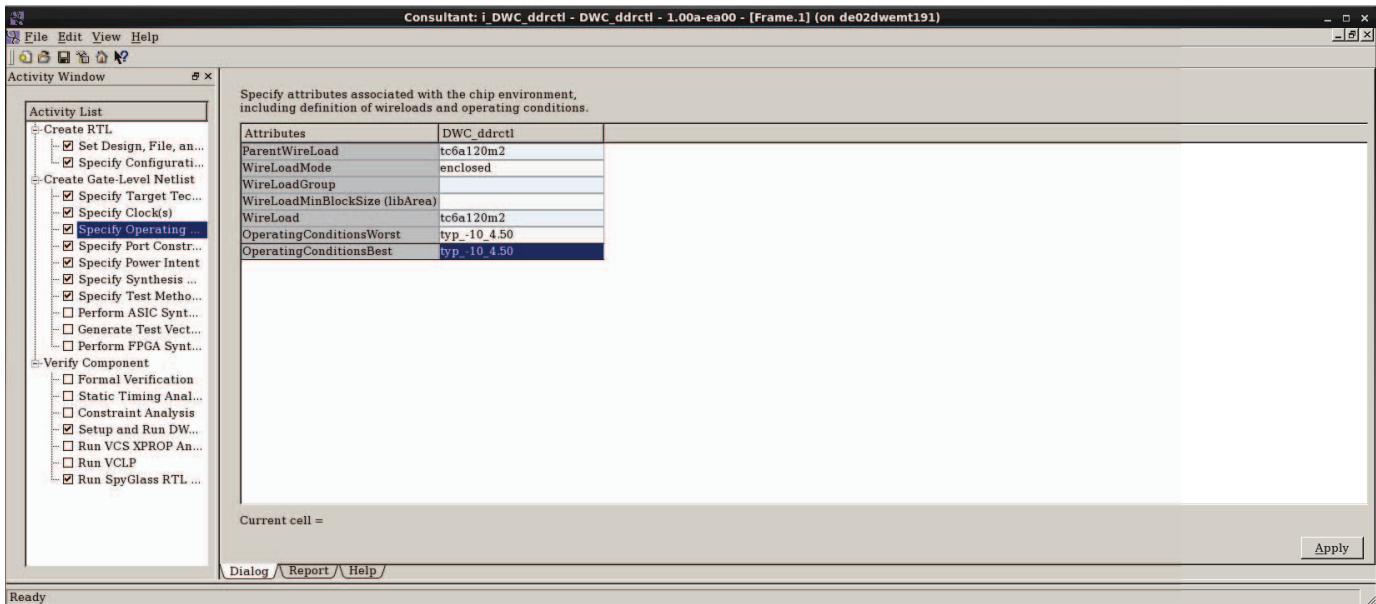


Note In configurations, when you set different Cycle Time values to the DDR4 and DDR5 clocks, an auxiliary TCL script is called in order to generate correct updated constraints. For more information, see “[Method 2: Use write_sdc Command](#)” on page [73](#).

4. Specify Operating Conditions and Wire Loads

- Select **Create Gate-Level Netlist -> Specify Operating Conditions and Wire Loads** activity.
- Set the various “WireLoad” attributes, unless you run the Physical Synthesis.
For detailed help on any of the options, right-click and select **Help on this Row**.
- Click **Apply** and look at the report, which gives the operating conditions and wireload information.

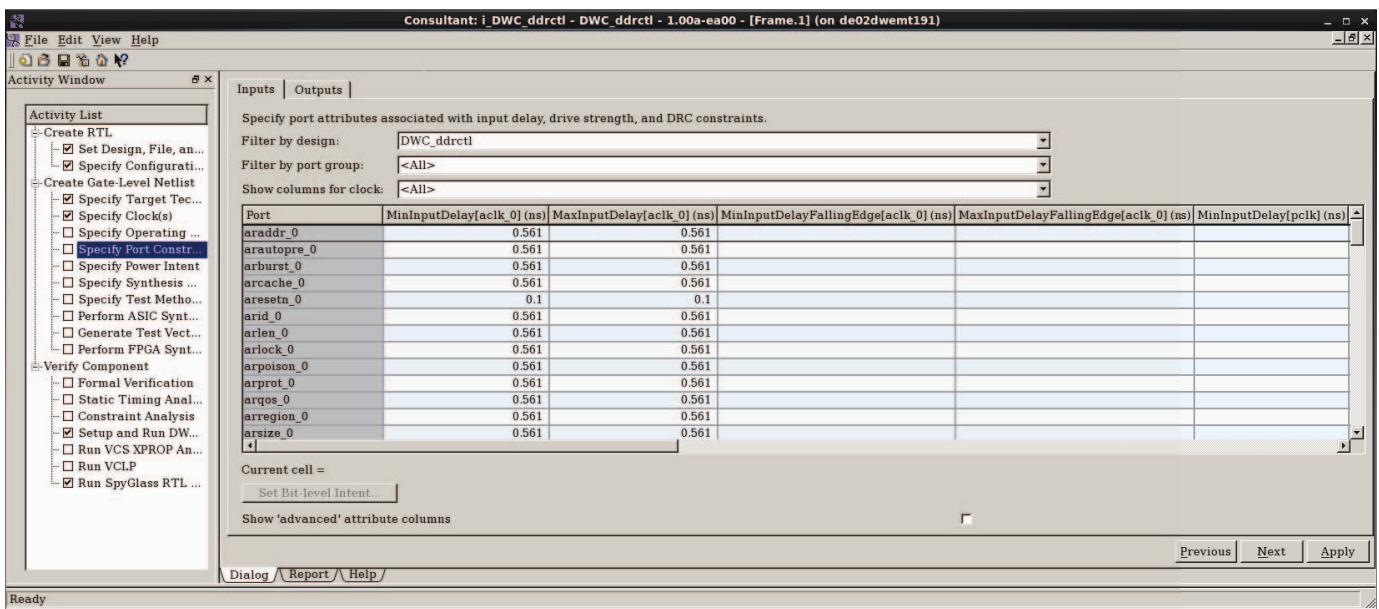
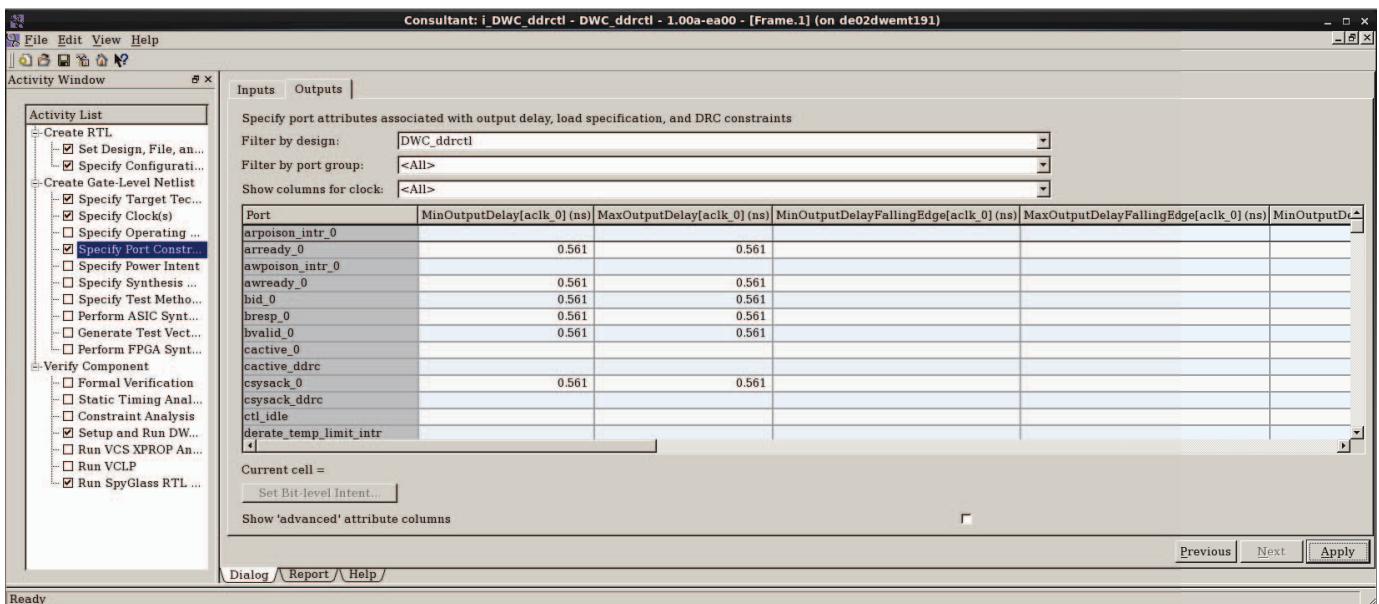
Figure 5-5 Specify Operating Conditions and Wireloads Window



5. Specify Port Constraints

In **Create Gate-Level Netlist -> Specify Port Constraints** task, port input and output delay constraints are specified relative to a virtual clock (`clk_ideal`), which has the same `CycleTime` as the real clocks specified in [Table 5-1](#) on page [49](#).

The default input and output delay constraint values are specified in nanoseconds and are configuration-dependent. The default set of these synthesis attributes provide acceptable synthesis results in most libraries.

Figure 5-6 Specify Port Constraints - Input Delay**Figure 5-7 Specify Port Constraints - Output Delay**

6. Specify Synthesis Methodology

❑ ASIC

In **Create Gate-Level Netlist -> Specify Synthesis Methodology** activity, review the synthesis strategy attributes. These attributes are set by the controller developer and can be optionally modified by you. The default setting of these attributes provide acceptable synthesis results in most libraries.

- Physical Synthesis

If you are running Physical Synthesis, then click on the **Physical Synthesis** tab (Figure 5-13 on page 56) and enter information in the related fields. The physical synthesis flow uses the Synopsys DC-Topographical engine, which is part of Design Compiler (dc_shell).

Figure 5-8 Specify Synthesis Methodology - Common Synthesis Strategy Attributes

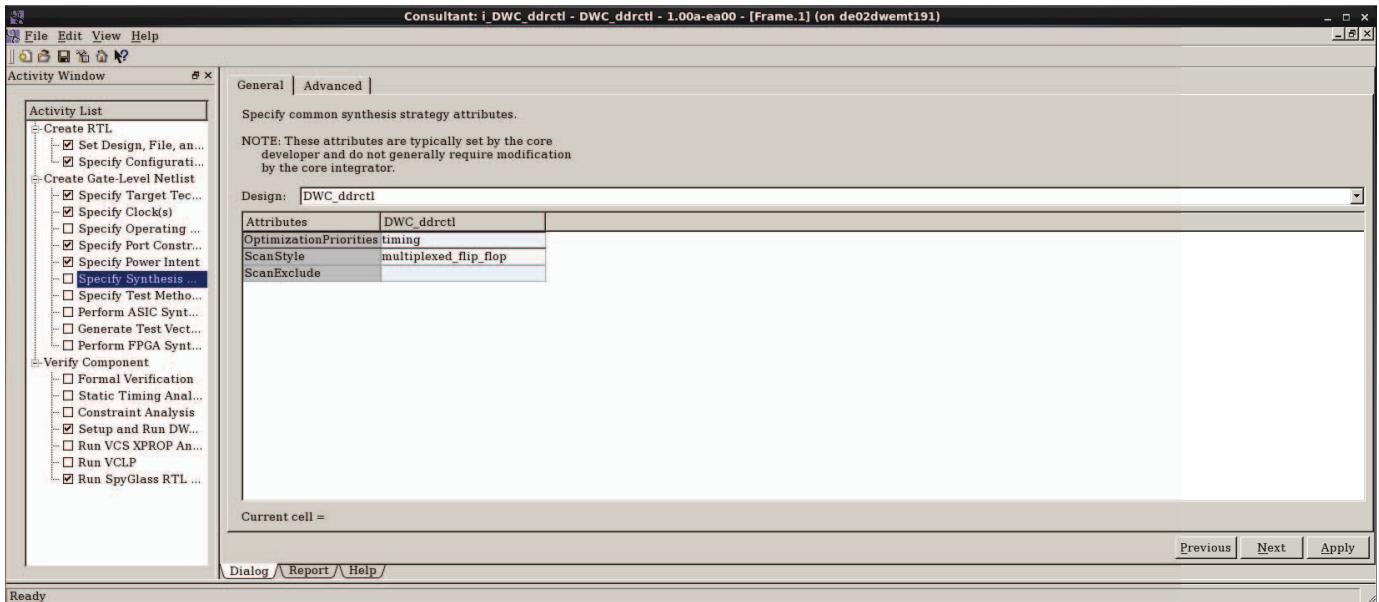
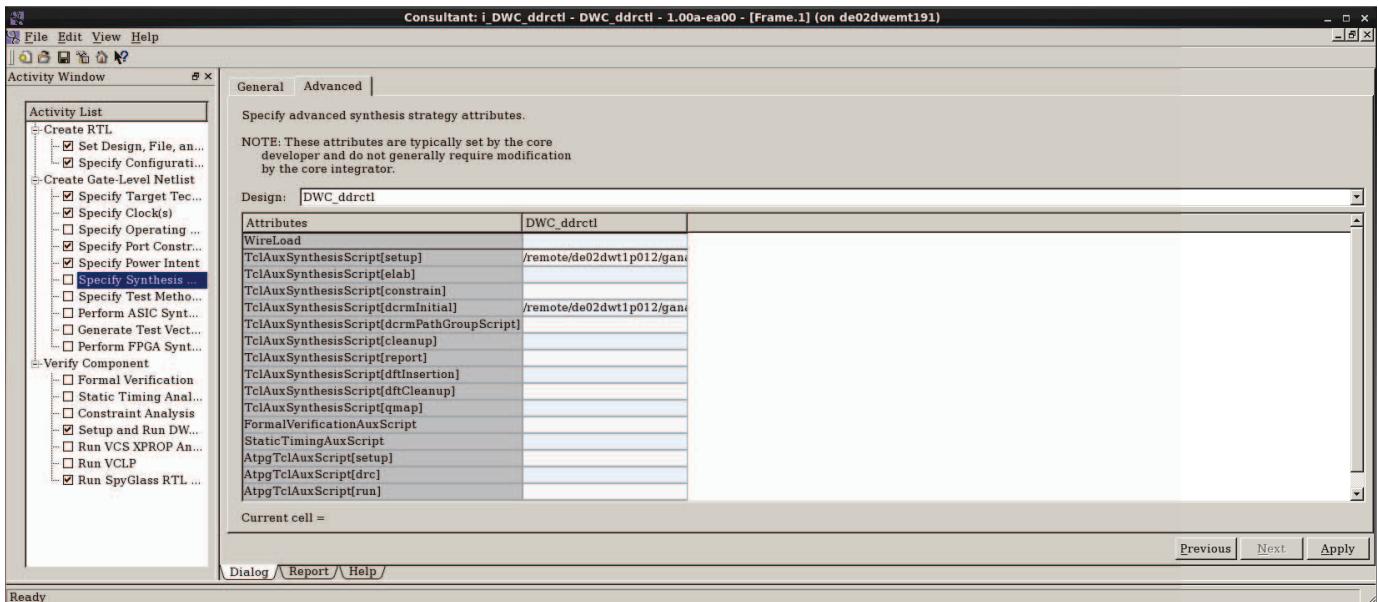


Figure 5-9 Specify Synthesis Methodology - Advanced Synthesis Strategy Attributes



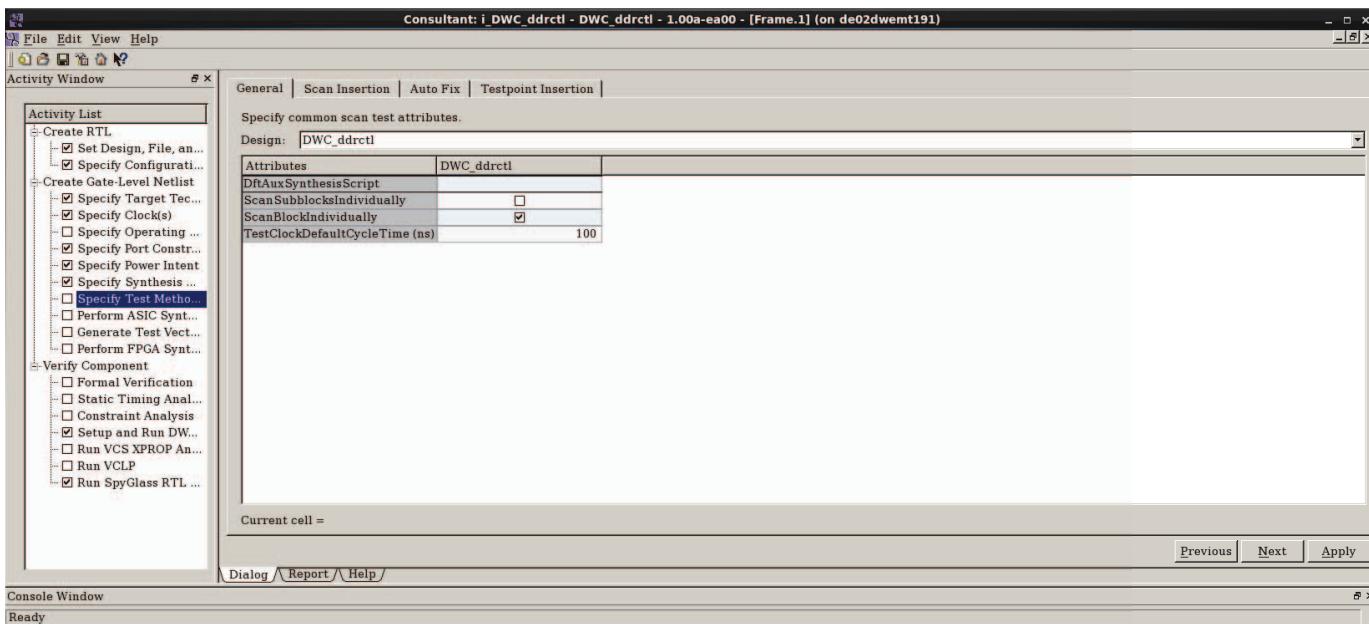
7. Specify Test Methodology

In **Create Gate-Level Netlist -> Specify Test Methodology** activity, these attributes are set by the controller developer and can be optionally modified by you.

Design for Test

Modify options according to your chip's DFT scheme. For more information on any of these options, right-click and select **Help on this Row**.

Figure 5-10 Specify Test Methodology



8. Synthesize

The next step in the **Create Gate-Level Netlist** is to Perform ASIC Synthesis.

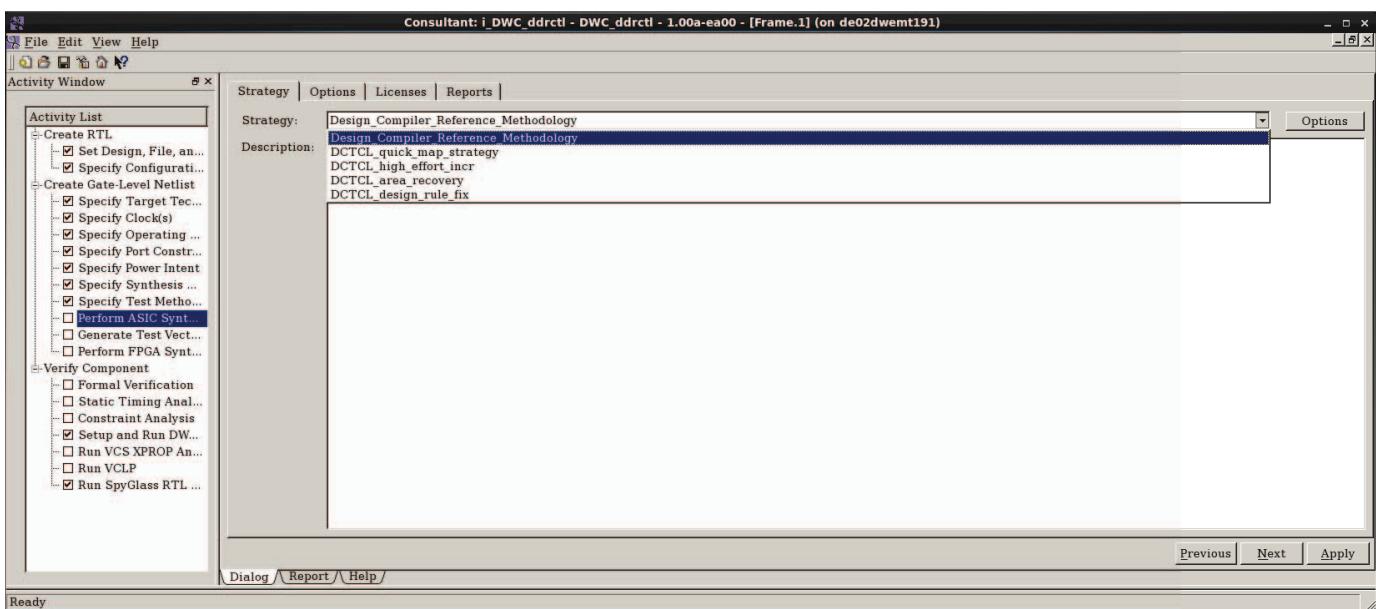
- ❑ ASIC Synthesis

In the **Perform ASIC Synthesis activity -> Strategy** tab, you can select the synthesis strategy/flow as shown in [Figure 5-11](#). The default flow is “Design Compiler Reference Methodology”. A detailed explanation of each strategy is provided in the GUI.

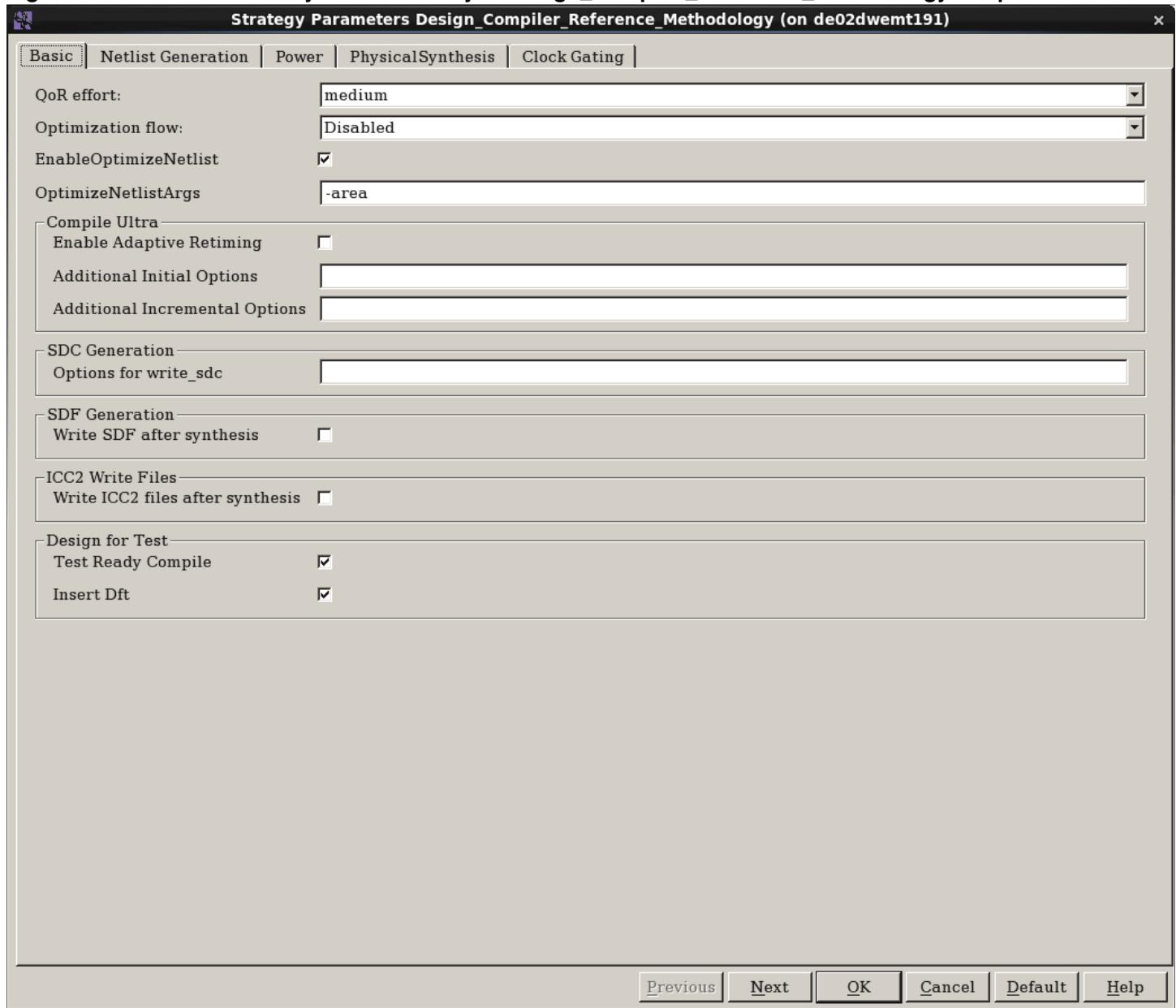


Hint Another strategy that is of interest is the DCTCL_one_pass_compile_ultra, which uses a simple TCL script based on the Synopsys Design Compiler Reference Methodology at <https://solnnet.synopsys.com/retrieve/021023.html>. This synthesis strategy is quicker and does not generate intermediate stages. Therefore, it is much easier to trace the steps in the flow.

When you select a strategy, you can click on the **Options** button next to the selected strategy drop-down list (highlighted in [Figure 5-11](#)) to specify other options for that particular strategy. For instance, [Figure 5-11](#) provides the options for the DCTCL_opto_strategy.

Figure 5-11 Perform ASIC Synthesis Activity -> Strategy Tab

For more information, right-click on any text field in the dialog box or refer to the coreConsultant User Guide (also see “[Help Information](#)” on page [95](#)).

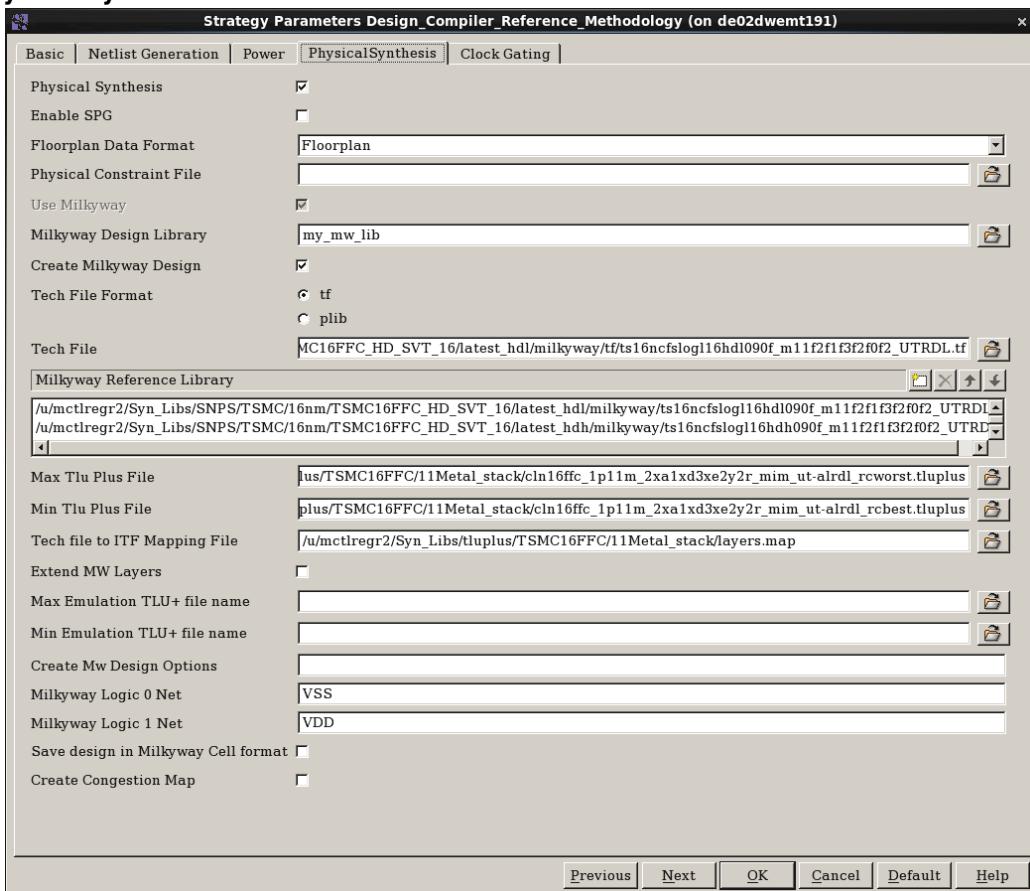
Figure 5-12 Perform ASIC Synthesis Activity -> Design_Compiler_Reference_Methodology -> Options Button

Note The 'Generate Test Vectors Activity' fails if, 'Insert Dft' option is not selected.

□ Physical Synthesis

- i. In the **Create Gate-Level Netlist -> Perform ASIC Synthesis** activity, select a strategy from the drop-down box or accept the default value (Design_Compiler_Reference_Methodology).
 - ii. Click the Options button and then select the **Physical Synthesis** tab (see [Figure 5-13](#) on page 56).
 - iii. Select **Physical Synthesis** check box and enter information in the related fields.
- Setting this parameter causes the physical synthesis placement engine to be used during optimization. Net loads and delays are estimated during placement. This flow may be used with either a physical library in the .ddc format or Milkyway reference library. Note that no placement data is saved with the ddc or Milkyway database.
- iv. Click **OK**.

Figure 5-13 Perform ASIC Synthesis Activity -> Design_Compiler_Reference_Methodology -> Options Button -> Physical Synthesis Tab

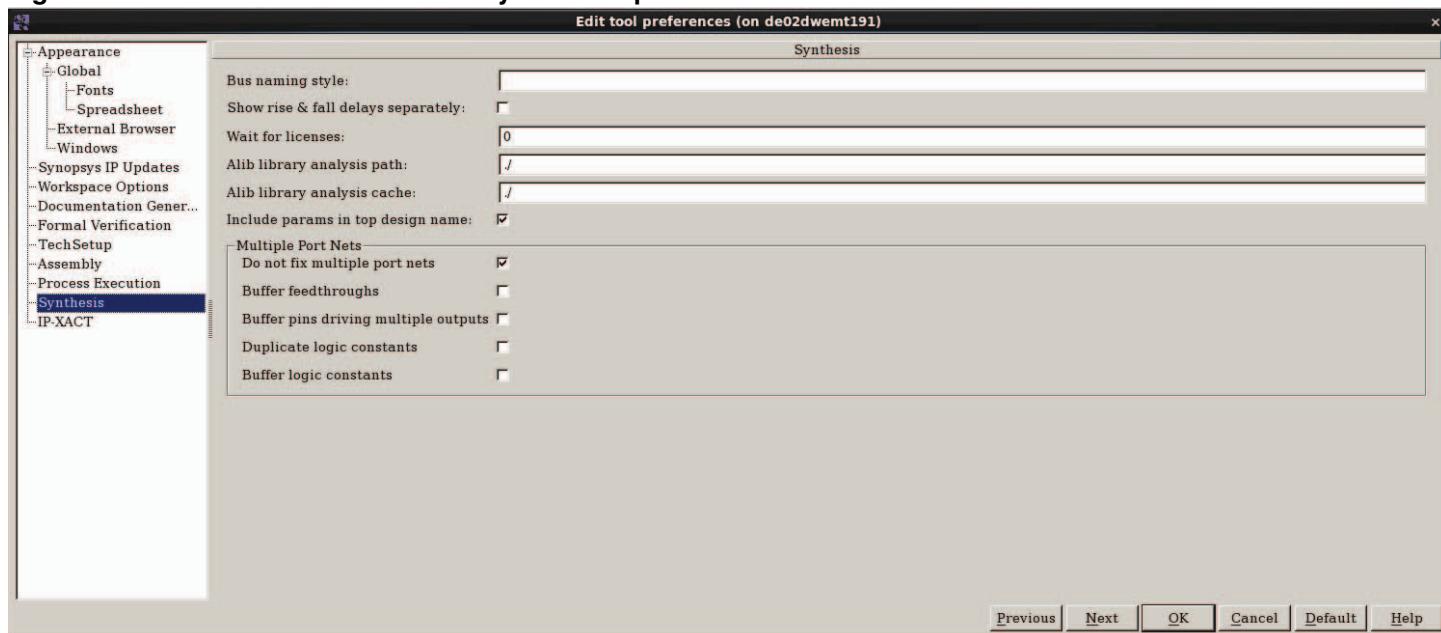


5.1.2 Setting Additional Synthesis Options

You can access more synthesis options in the Edit Tool Preferences dialog box accessed from the coreConsultant Edit Menu.

To set these additional options:

- Select **Edit -> Preferences**. The Edit Tool Preference dialog box is displayed.
- Click on **Synthesis** to display the list of options, as shown in [Figure 5-14](#) on page 57.

Figure 5-14 Edit Tool Preferences – Synthesis Options

5.1.3 Checking Synthesis Results

After you have run synthesis, you can check the results by clicking the **Report** tab. All the synthesis results and log files are created under your <workspace>/syn directory. The final symbolic link points to the current synthesis stage directory. The final log file is written to <workspace>/syn/run.log.

Except in the case of the DCTCL_one_pass_compile_ultra strategy, your final netlist and report directories (initial, incr1, or incr2) depend on the QoR effort that you chose for your synthesis (default is Medium) or whether you chose to insert DFT:

- Low effort – initial
- Medium effort – incr1
- High effort – incr2

The QoR effort is selected through the **Perform ASIC Synthesis -> Options¹ -> Basic** tab. There are also options here to:

- Generate reports for all stages
- Generate netlist for all stages

The synthesis process runs in stages or steps, which are normally initial, incr1, or incr2, depending on the value of the QoR Effort synthesis strategy parameter.



- In the <workspace>/syn directory, run.scr, Makefile, and final are symbolic links to the current synthesis stage files.
- These links are also used and set to different locations during ATPG and Formal Verification.

1. BUTTON as circled in [Figure 5-11](#) on page 54 and not TAB.

[Table 5-2](#) shows the other files that are generated after synthesis.

Table 5-2 Synthesis Output Files

Synthesis Type	Files	Purpose
ASIC	./syn/final/db/DWC_ddrctl.ddc	Synopsys database files (gate level) that can be read into dc_shell for further synthesis, if desired.
	./syn/final/db/DWC_ddrctl.v	Gate-level netlist that is mapped to technology libraries that you specify.
	./syn/final/report/*.*	Synthesis report files.
Physical	./syn/final/db/DWC_ddrctl.ddc	Synopsys database files (gate level) that can be read into dc_shell for further synthesis, if desired.
DFT	./syn/dft/*.*	Results of DFT insertion.

5.1.4 Running Synthesis from a Unix Shell

To run ASIC, FPGA, or Physical synthesis from Unix shell (before running from coreConsultant):

1. Complete all the setup steps as outlined in “[Synthesizing the Controller](#)” on page 46.
2. Select **Perform ASIC Synthesis -> Options -> Execution Options -> Generate scripts only?**
3. Click **Apply**.
4. Enter the following commands:

```
% cd <workspace>/syn
% run.scr
```

To run synthesis again from a Unix shell (after having run it from coreConsultant), enter the following commands:

```
% cd <workspace>/syn
% run.scr
```



Caution

- In the <workspace>/syn directory, run.scr, Makefile, and final are symbolic links to the current synthesis stage files.
- These links are also used/set to different locations during ATPG, Static Timing Analysis and Formal Verification. Therefore, ensure they are pointing to the correct location if you are attempting to run Synthesis from the Unix shell AFTER having just run ATPG, Static Timing Analysis or Formal Verification.

5.1.5 Troubleshooting: Common Problems in this Step

- coreConsultant cannot invoke the synthesis tool after a crash. The activity has detected the presence of a synthesis “guard” file from the previous run.

Usually this indicates that a synthesis run is in progress in this workspace. The guard file is removed when the synthesis run is completed. This activity cannot continue since files written by this activity can adversely affect the outcome of the synthesis run. Check the Console Pane for any messages which called out for the guard file name.

- A user-defined strategy file does not exist.
Go the Console Pane and scroll to the message complaining about the file. Create that file.
- Specified cell name could not be found in the loaded technology libraries.
Review the technology and link libraries being used and select a cell that exists within one of the libraries.
- BCM constraint script does not officially support post-synthesis tools. The recommended flow loads the constraints after elaboration, dumps SDC after compile, and loads the SDC into post-synthesis tools.

5.2 Performing Formal Verification



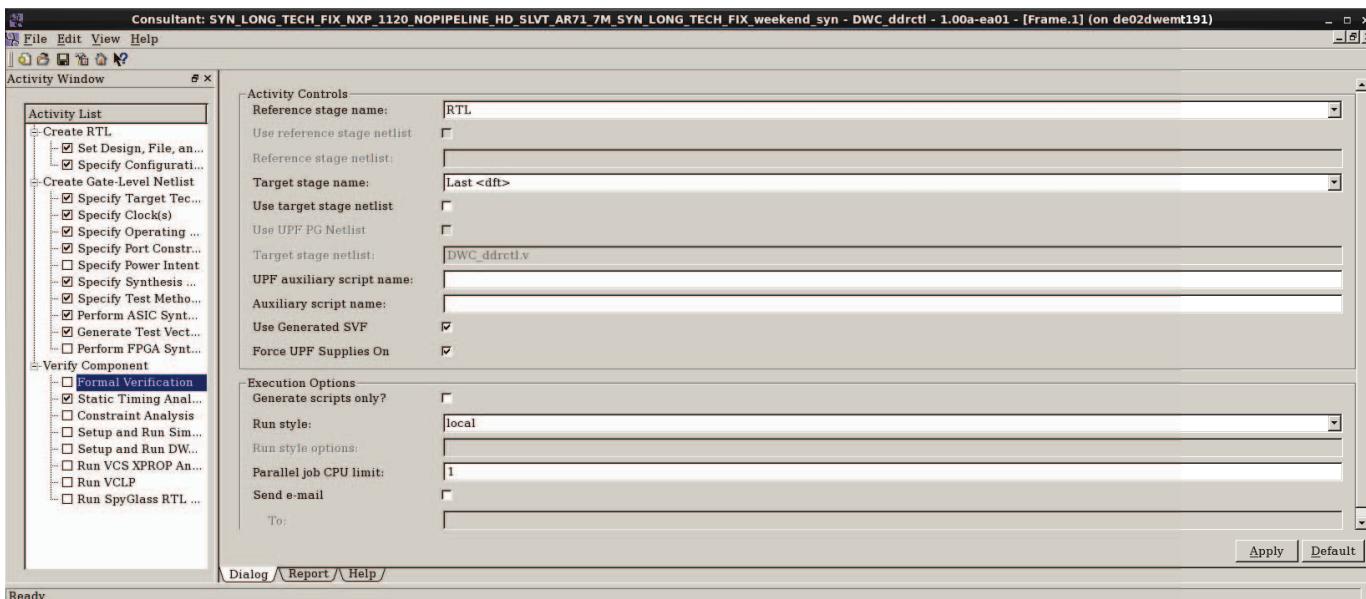
Attention Formal Verification (also referred to as formal equivalence checking) is an activity which takes the output of synthesis as input. Synthesis must be completed before a meaningful set up can exist in the Formality window.

The **Verify Component -> Formal Verification** activity in coreConsultant uses Synopsys Formality (fm_shell) to check two designs for functional equivalence. You can check the gate-level design from a selected phase of a previously executed synthesis strategy against either the RTL version of the design or the gate-level design from another stage of synthesis.

To perform formal verification:

1. Choose the **Verify Component -> Formal Verification** activity. The following dialog box is displayed.

Figure 5-15 Verify Component -> Formal Verification Activity



2. Complete the following fields:

- **Reference stage name:** RTL
- **Target stage name:** Select last synthesis stage from the pull-down menu.
- **Use Generated SVF:** Enabled

3. Click **Apply**.



Hint For more information about diagnosing and fixing failing points, see Formality User Guide. If you need to work with Formality directly to diagnose failing points, you can load the saved session file (workspace/syn/stage/final/db/Design.fss) directly into Formality.

5.2.1 Checking Formal Verification Results

The Formality results are saved in the <workspace>/syn/<Output stage> directory. The file <workspace>/syn/<Target stage name>.tcl may be inspected to help you understand the Formal Verification flow.

5.2.2 Running Formality from a Unix Shell

To run Formality from a Unix shell (before running it from coreConsultant), you must first complete all the setup steps as outlined previously, select **Formal Verification -> Execution Options -> Generate scripts only?** and then click **Apply**. Then enter the following commands:

```
% cd <workspace>/syn  
% <*>_fm.scr
```



Note The exact name of this script depends on the name of the 'last' executed stage of synthesis.

To re-run Formality from a Unix shell (after having run it from coreConsultant), enter the following commands:

```
% cd <workspace>/syn  
% <*>_fm.scr
```



Caution

- In the <workspace>/syn directory, run.scr is a symbolic link to the current Formal Verification run file.
- This link is also used/set to different during Synthesis, Static Timing Analysis and ATPG. Therefore, ensure it is pointing to the correct location if you are attempting to run Formal Verification from the Unix shell AFTER having just run ATPG, Static Timing Analysis or Synthesis.

5.3 Inserting Design for Test

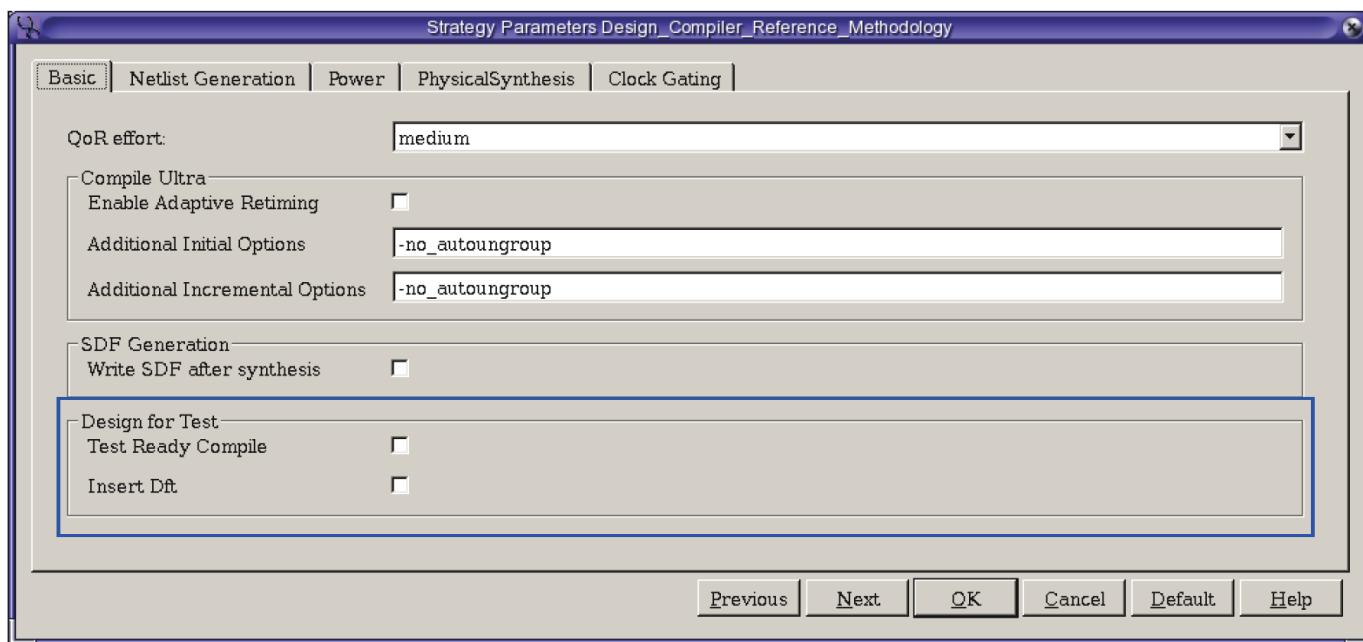
This section shows you how to use the coreConsultant tool to insert DFT during synthesis of the DDRCTL. This activity is not applicable to FPGA implementations.

You perform Design For Test (DFT) insertion during synthesis.

To insert DFT, perform the following steps:

- Check that the controller input clocks are selected as “Test Clock” in the “Specify Clocks” window. This is normally selected by default. See “Specify Clocks”.
- In the “Specify Test Methodology” window, modify the options according to your chip DFT scheme. For detailed help on any of the options, right-click and select “Help on this Row”.
- DFT insertion is controlled in the “Design For Test” tab that is displayed by clicking the “Options” button (NOT the Options tab) in the “Synthesis” window. You must select one of these two options:
 - “Test Ready Compile”: Design Compiler uses scan flops in synthesis, but it does not insert and route the chains. The scan option is added to the initial compile call.
 - “Insert Dft”: Design Compiler completes DFT insertion, that is, it performs synthesis with scan flops and scan chain insertion.

Figure 5-16 Design For Test Tab



The DFT results are saved in the *workspace/syn/dft/* directory.

The DFT insertion adds the interface signals of the controller.

Table 5-3 DFT Interface Signals

Signal	Purpose
test_mode	The purpose of this input signal is to switch between normal mode and test mode. Test points set for internal signals that cannot be controlled or observed in normal mode are enabled in test mode. When a test point is activated, ATPG test coverage is improved by making internal signals externally controllable or observable.
test_se	The purpose of this input signal is to enable the scan paths. When scan path is enabled, data shift operation across F/Fs is possible.
test_si	The purpose of this input signal is to input data for scan shift. Shift data is input externally using this signal before the scan test is executed. When the test_se signal is enabled, shift data can be input to this signal.
test_so	The purpose of this output signal is to output data for scan shifting. Shift data is output externally using this signal after the scan test is executed. When the test_se signal is enabled, shift data can be output from this signal.

5.4 Running Automatic Test Pattern Generation (ATPG)

This section shows you how to run automatic test pattern generation (ATPG) on the DDR controller using Synopsys TetraMax tool.

5.4.1 Running ATPG using TetraMax

ATPG is performed using TetraMax.

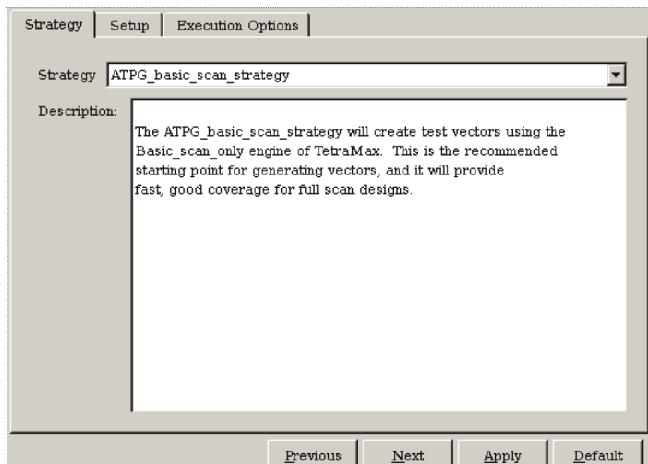


- ATPG is an activity which takes the output of synthesis as input.
- Synthesis must be completed before a meaningful setup can exist in the ATPG window.

After you have synthesized the controller with the Insert Dft option, complete the following procedure:

1. Select **Create Gate-Level Netlist -> Generate Test Vectors** activity. The following dialog box (see [Figure 5-17](#)) is displayed.

Figure 5-17 Create Gate-Level Netlist -> Generate Test Vectors Activity



2. Select the Setup tab and complete the following fields.

- **Input stage:** Specify the last synthesis stage from the pull-down menu.
- **Output stage:** Set to any name that you want to use identify the output files that are created in your workspace directory. For example, atpg.
- **Test Libraries:** Specify the library Verilog file names.

These are the Verilog simulation models for the target libraries used during synthesis. They provide the description of the logical functionality of all the cells in the standard cell library. They are needed for the ATPG tool to comprehend the logic function implemented by each standard cell instantiated.

- **Test Pattern Format:** Specify your test format.

3. Click **Apply** when you have finished specifying your options.

5.4.1.1 Checking ATPG Output Files

The ATPG results are saved in the <workspace>/syn/<Output stage> directory.

The following files in <workspace>/syn/<Output stage> may be inspected to help you understand the ATPG flow.

- script/DWC_ddrctl.tcl
- Makefile

5.4.1.2 Running ATPG from the Unix shell

To run ATPG from a Unix shell (before running it from coreConsultant), you must first complete all the setup steps as outlined previously and then select **Generate Test Vectors -> Execution Options -> Generate scripts only?** before clicking **Apply**. Then enter the following commands:

```
% cd <workspace>/syn  
% run.scr
```

To re-run ATPG from a Unix shell (after having run it from coreConsultant), enter the following commands:

```
% cd <workspace>/syn  
% run.scr
```



Caution

- In the <workspace>/syn directory, run.scr, Makefile, and final are symbolic links to the ATPG input stage files, which are identified by the label <'Output stage'>
- These links are also used/set to different locations during Synthesis and Formal Verification. Therefore, ensure they are pointing to the correct location if you are attempting to run ATPG from the Unix shell AFTER having just run Synthesis or Formal Verification.

For more information about running ATPG, see coreConsultant User Guide (also see “[Help Information](#)” on page [95](#)).

You have to do this only once because these settings are saved in your ~/.synopsys_rt_prefs.tcl file. You must do this before you create the reports. If you have previously created reports with old settings, delete the workspace and start again.

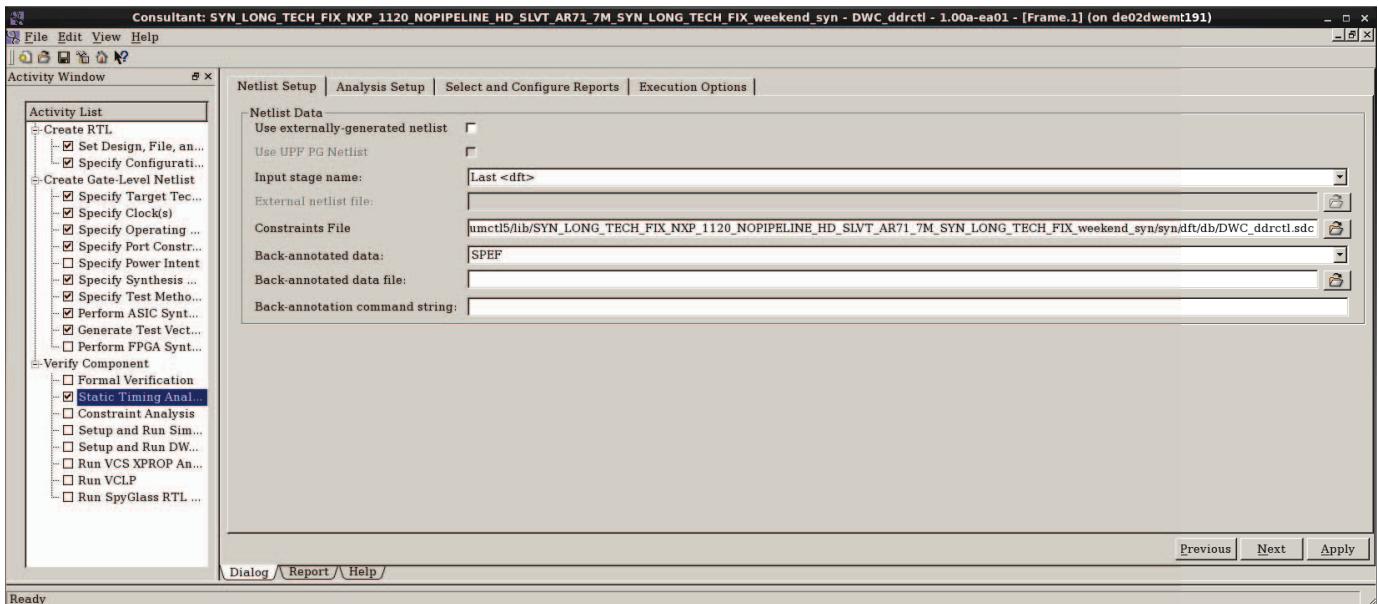
5.5 Running Static Timing Analysis

The **Verify Component -> Static Timing Analysis** activity allows you to run PrimeTime static timing analysis, using constraints generated from coreConsultant. This can be run either on the netlist generated from synthesis, or on an externally generated netlist (for example, from a layout tool). An externally generated SPEF or SDF file can also be read in for back-annotation.

5.5.1 Performing Static Timing Analysis

You must have completed the **Create Gate-Level Netlist** activity (see “[Synthesizing the Controller](#)” on page [46](#)), or have an externally generated netlist available before starting this task. To perform STA on your controller, select the **Static Timing Analysis** activity as shown in [Figure 5-1](#) on page [47](#).

Figure 5-18 Static Timing Analysis Activity-Netlist Setup Tab



1. Netlist Setup

The first step is to specify what netlist and back-annotated data you wish to use as inputs to the Static Timing Analysis (STA) activity.

- **Netlist**

If you choose to use a netlist from the **Create Gate-Level Netlist** activity, you should choose to use the netlist generated from any of the synthesis stages used during that activity. For more information on the synthesis stages, see “[Checking Synthesis Results](#)” on page [57](#).

If you choose to use an external netlist, specify its location in the **External netlist** file field.

- **Constraints**

You can specify what constraints to use. By default, this is populated with the constraints generated from the final synthesis stage from the **Create Gate-Level Netlist** activity, and you will not normally need to change this.

- **Back-annotated data**

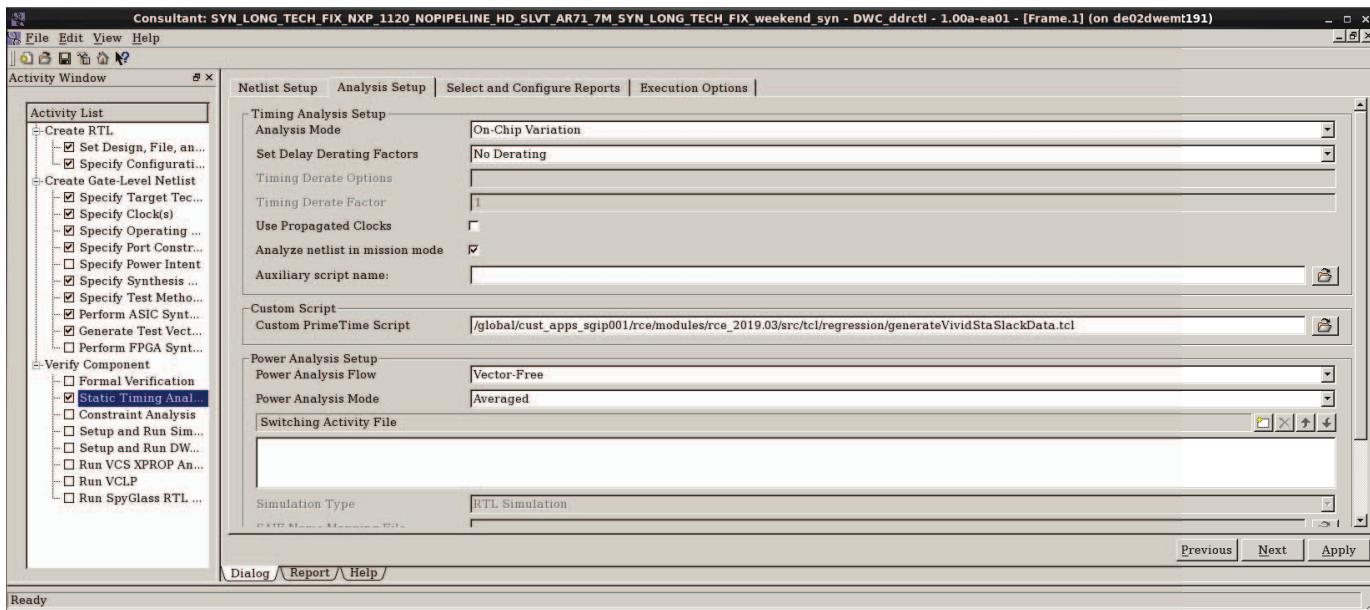
You can choose to use SPEF or SDF annotation, or to run STA without annotation, if none is available. If you choose to annotate, you should specify the SPEF or SDF file in the **Back- annotated data**

file. If you need to provide options to the read_spef or read_sdf command, they can be entered in the **Back-annotation command string**.

2. Analysis Setup

Click on the **Analysis Setup** tab (Figure 5-19), which allows you to select various STA setup options.

Figure 5-19 Static Timing Analysis Activity: Analysis Setup Tab



□ Timing Analysis Setup

Here you can choose whether to run in on-chip variation (OCV) or best-case/worst-case mode, and whether to include derating or not. There is also an option to use propagated clocks. For more information, right-click on the individual options and select **What's This?**.

□ Custom Script

There is an option to select a **Custom Prime Time Script**, which runs at the end of the PrimeTime run (after all reports have been generated).

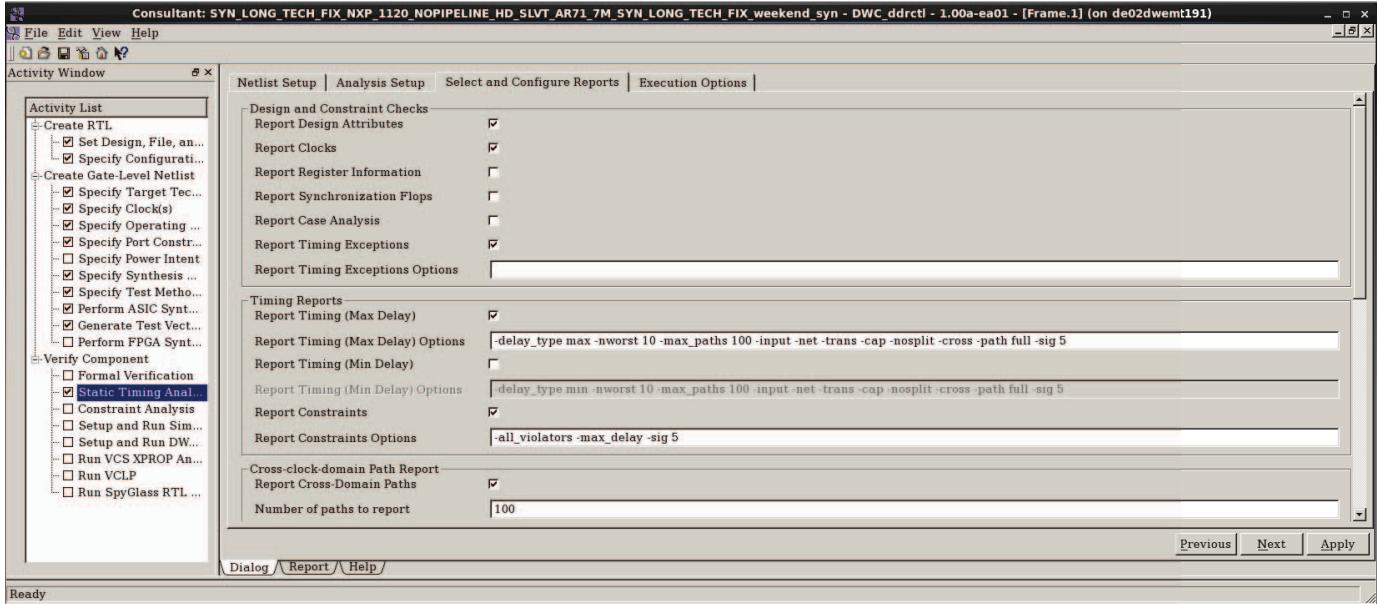
□ Power Analysis Setup

You can also use PrimeTime to generate power estimates. These can either be vector-free (not based on any external switching information), or based on an SAIF or simulation dump file. Fields are provided to specify the switching activity file, to map names between RTL and gates, and to specify what parts (hierarchical path, and simulation time) of the simulation dump file should be used for the power calculations. For more information, right-click on the individual options and select **What's This?**.

3. Select and Configure Reports

In this tab (see [Figure 5-20](#)), you can choose what reports you would like PrimeTime to produce.

Figure 5-20 Static Timing Analysis Activity: Select and Configure Reports Tab



- ❑ Design and Constraint Checks

You can choose whether to generate reports on design attributes, clocks, case analysis and timing exceptions. For timing exceptions, you can specify options to be appended to the PrimeTime report_exceptions command.

- ❑ Timing Reports

You can choose to generate max_delay, min_delay and constraints reports. In each case, options can be added to the appropriate PrimeTime command.

- ❑ Cross-clock-domain Path Reports

For detailed information, see "[Clock-Domain-Crossing \(CDC\) Synchronizers](#)" on page [83](#)

- ❑ Clock Reports

You can choose to generate clock_timing, min_pulse_width and clock_gating_check reports, and provide options for the last two.

- ❑ Power Analysis

This section performs power analysis using PrimeTime-PX. For more information, right-click on the individual options and select **What's This?**.

4. Execution Options

You can choose relevant options in the **Execution Options** tab. As with other coreConsultant activities, you can choose whether to generate the scripts only without running them, or the method of running them.

When you have chosen all relevant options for your Static Timing Analysis run, click **Apply**.

5.5.2 Checking STA Results

After you have run STA, you can check the results by clicking the **Report** tab. The location of all STA results and reports can be seen from the **Report** tab, and is typically in <workspace>/syn/incr1/report/sta. Links to all reports are also provided in the **Report** tab.

After you have run synthesis, you can check the results by clicking the **Report** tab. All the synthesis results and log files are created under your <workspace>/syn directory. The `final` symbolic link points to the current synthesis stage directory. The final log file is written to <workspace>/syn/run.log.

5.5.3 Running STA from Unix Shell

To run Static Timing Analysis from a Unix shell (before running it from coreConsultant):

1. Complete all the setup steps as outlined in “[Performing Static Timing Analysis](#)” on page [66](#).
2. Select **Static Timing Analysis-> Execution Options -> Generate scripts only?**
3. Click **Apply**.
4. Enter the following commands:

```
% cd <workspace>/syn  
% run.scr
```

To run STA again from a Unix shell (after having run it from coreConsultant), enter the following commands:

```
% cd <workspace>/syn  
% run.scr
```



Caution

- In the <workspace>/syn directory, `run.scr`, `Makefile`, and `final` are symbolic links to the current synthesis stage or STA files.
- These links are also used/set to different locations during Synthesis, ATPG and Formal Verification. Therefore, ensure they are pointing to the correct location if you are attempting to run STA from the Unix shell AFTER having just run Synthesis, ATPG or Formal Verification.

6

Integrating the Controller

This chapter contains the following sections:

- “[Exporting Controller to Your Chip Design Database](#)” on page [72](#)
- “[Integrating Controller with PHY](#)” on page [75](#)
- “[Integrating Host Interface \(HIF\)](#)” on page [78](#)
- “[Integrating External RAM](#)” on page [81](#)

6.1 Exporting Controller to Your Chip Design Database

At a certain point you may want to transfer (export) a configured controller into your own custom design flow. The coreConsultant tool has a number of features to accomplish this task. This section shows you how to access the relevant files, scripts, and information for your configured controller. You can then transfer these to your chip design database.

The topics in this section are as follows:

- “[Instantiating Your Controller](#)” on page [72](#)
- “[Exporting RTL Code](#)” on page [72](#)
- “[Synthesizing to a Device Outside of coreConsultant](#)” on page [72](#)
- “[Exporting Views and Reports](#)” on page [74](#)
- “[Simulating Outside coreConsultant](#)” on page [74](#)

6.1.1 Instantiating Your Controller

After you have configured your controller, you can generate an example Component Instantiation.

To instantiate the controller, follow these steps:

1. Select the **Report** tab in the **Specify Configuration** activity.
2. Click the **generate view** link.

The controller instantiation is now available in `export/DWC_ddrctl_inst.v`.

6.1.2 Exporting RTL Code

There is an `export` directory in your workspace. The coreConsultant tool populates this directory with various links and files for export use. After you have configured the controller, the files in [Table 6-1](#) are created in the `<workspace>/export` directory.

Table 6-1 Files (of interest) Created in export Directory After Specify Configuration Activity

File Name	Description
<code><workspace>/export/src/</code>	Configured source code
<code><workspace>/export/dwc_ddrctl.lst</code>	List of source files in proper analysis order

6.1.3 Synthesizing to a Device Outside of coreConsultant

If you want to map and synthesize the controller to a device using the Synopsys synthesis tools within coreConsultant, then follow the process as outlined in “[Synthesizing the Controller](#)” on page [46](#). Otherwise, you must export the synthesis scripts from coreConsultant as outlined here so that you can synthesize the controller in your own design flow. This section shows you how to access the relevant synthesis scripts and information for your configured controller. You can then transfer these to your chip design database.

To get a detailed description of how to integrate the IP at chip level, enter the following command in the coreConsultant command line:

```
coreConsultant> man Synthesis_API
```

The following pop-up window is displayed.

Figure 6-1 Synthesis_API Pop-Up Window

There are two methods used to export the synthesis scripts. If you have access to Synopsys Design Compiler, then you can use either method. If you not have access to Synopsys Design Compiler, then you must use the `write_sdc` method.

6.1.3.1 Method 1: Access Synopsys Design Compiler Scripts

To access Design Compiler scripts:

1. First complete all the set-up steps in “[Synthesizing the Controller](#)” on page 46.
2. Before clicking **Apply** to complete the **Create Gate-Level Netlist** activity, select the **Synthesize -> Options tab -> Execution Options -> Generate scripts only?** parameter.

[Table 6-2](#) lists files that are relevant to the synthesis flow.

Table 6-2 Files Related to Synthesis Flow

Synthesis Type	File	Description
ASIC	constrain/script/DWC_ddrctl.tcl	Primary constraints
	run.scr	Runs synthesis
	Makefile	Creates synthesis scripts

6.1.3.2 Method 2: Use `write_sdc` Command

Use the `write_sdc` command to write out a script in a Synopsys Design Constraints (SDC) format. The SDC files are TCL scripts that use a subset of the commands supported by PrimeTime and Design Compiler. This file generation process does not require a Design Compiler license.



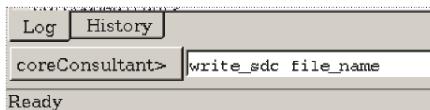
If a technology library is not loaded in the **Specify Target Technology -> dc_shell target_library variable** (or Synplicity Library Setup in the case of an FPGA), then the generated SDC file contains constraints relative to a generic technology library. You need to modify these constraints to match your target library cell names.

Invoke the following command from the coreConsultant command line:

```
coreConsultant> write_sdc [-force] [-version 2.1] file_name
```

If you use the `-force` option to force the writing of the SDC file even if the Specify Target Technology activity (or Synplicity Library Setup in the case of FPGA) is not complete. The `-version` option must be used when writing out the SDC file without completing the Specify Target Technology activity. It will specify the SDC version to be used.

Figure 6-2 write_sdc Command



6.1.4 Exporting Views and Reports

As part of the export process, you may want to generate documentation for your configured controller to be used as part of the documentation for an entire chip. The report and view generation process is based on DocBook instead of HTML. This allows documentation for I/O definitions, parameter definitions, and memory maps to be generated in HTML, RTF, and MIF formats from the DocBook source.

For more information, see “[Creating Optional Reports and Views](#)” on page 24. All reports can be accessed in the `<workspace>/report` directory. The optional views are located in the `<workspace>/export` directory.

6.1.5 Simulating Outside coreConsultant

When simulating the PHY and the Controller outside coreConsultant (user simulation environment), ensure that the interrelated SDRAM, Controller and PHY registers (for example, SDRAM timing parameters, SDRAM mode registers, and so on) are programmed to be in sync. For example, if you adapt the `apb.log` (controller register settings) from coreConsultant environment, then the PHY CSRs as well as your DRAM model settings must also be configured likewise. Otherwise, it is most likely the simulation may fail due to errors in timing/MR parameter mismatch.

6.2 Integrating Controller with PHY

The following sections detail how the DDR controller can be integrated with the Synopsys LPDDR5X/5/4X PHY, using the testbench options available in the “Testbench Options” tab of “Setup and Run Simulations” in coreConsultant.

This section contains the following sub-sections, which follow the structure of the coreConsultant options.

- “[PHY Type](#)” on page [75](#)
- “[PHY Simulation Model](#)” on page [75](#)
- “[Imported PHY Location](#)” on page [75](#)
- “[Imported C code location](#)” on page [76](#)

6.2.1 PHY Type

This parameter selects the PHY type to be used in the simulation. Options are:

- Synopsys DDR5/4 PHY
- Synopsys DDR5/4 PHY_V2
- Synopsys LPDDR5/4/4X PHY
- Synopsys LPDDR5X/5/4X PHY

6.2.2 PHY Simulation Model

The DDR controller allows you to simulate with different options for the PHY model used. The model is selected in coreConsultant (Setup and Run Simulations -> Testbench Options -> PHY Simulation Models). The options are as follows:

- Included (encrypted) Synopsys PHY model. This option simulates with the pre-installed (encrypted) versions of the Synopsys PHY model.
- Imported Synopsys PHY model. This option provides you the ability to simulate with a PHY model you import yourself. The intention here is to enable you to import a new version of your Synopsys PHY, and continue to simulate it with your existing DDRCTL core. This is not guaranteed to be possible with all new PHY versions.

6.2.3 Imported PHY Location

This option is only relevant if the “Imported Synopsys DWC DDR PHY model” option is chosen, otherwise, it is ignored.

This option must be set to point to the root directory (for example, Synopsys dwc_lpddr5x_phy_tsmc5ff12) of the installation of the Synopsys DDR PHY release. coreConsultant then searches the standard PHY directory structure to find the relevant simulation models for the PHY.



Note The imported PHY must correspond to the PHY type selected during the “Setup and Run Simulations” activity.

If the Imported PHY option is chosen, a top-level PHY wrapper module called dwc_ddrphy_top must be included in the above directories. This PHY wrapper is instantiated in the provided ddr_chip module (in

<workspace>/sim/testbench/tb/ddr_chip.v), and its ports must match that instantiation. All other Verilog modules required for the PHY must also be included in the above directories.

6.2.4 Imported C code location

This option is only relevant if the “Imported Synopsys DWC DDR PHY model” option is chosen, otherwise, this option is ignored.

For running simulations it is necessary to use C code to initialize the PHY. This option should point to the location of the C code, which is then read in and executed by the simulation. This should point to the phyinit directory of the PHY being simulated. For example,

<<PHY_installation_path>>/latest/phyinit/Latest/software/ path.

6.2.5 Imported Firmware Location

This option is relevant only if the “Imported Synopsys DWC DDR PHY model” option is chosen, otherwise, this option is ignored. For running simulations it is necessary to use firmware when the PHY is performing training/SDRAM initialization. This option must point to the location of the firmware files, which is then read in and executed by the simulation. This should point to the firmware directory of the PHY being simulated. For example, <<PHY_installation_path>>/Latest/firmware/Latest path.

6.2.6 PHY Parameters that can be Controlled from coreConsultant

When using simulating with a PHY in the DDRCTL environment, the PHY is automatically configured by coreConsultant. Some of this configuration is performed based on the configuration of the LPDDR5X/5/4X Memory Controller (for example, to ensure matching data widths between the LPDDR5X/5/4X Memory Controller and PHY), while other configuration is performed under the control of Testbench Options presented in the coreConsultant GUI.

Tables 6-3 to 6-5 list the PHY parameters that are configured to match the DDRCTL Memory Controller configuration.

For more information on all these Synopsys PHY parameters, see the appropriate PHY databook.

Table 6-3 List of Macros in PHY VDEFINES file modified / checked by coreConsultant for Synopsys DDR54 PHY

Description	VDEFINES Macro	Equivalent DDRCTL Testbench/Configuration Parameter
ACX4 Instance	DWC_DDRPHY_NUM_ANIBS	ANIBS
Number of bytes	DWC_DDRPHY_NUM_DBYTES	MEMC_DRAM_DATA_WIDTH/8
Enable 2 nd DFI Channel	DWC_DDRPHY_DFI1_EXISTS	DFI1_EXISTS
Specifies number of DfiClk pipeline stages added to all dfi_rrdata* signals	DWC_DDRPHY_PIPE_DFI_RD	pipe_dfi_rd
Specifies number of DfiClk pipeline stages added to all dfi_wrdata* signals	DWC_DDRPHY_PIPE_DFI_WR	pipe_dfi_wr

Description	VDEFINES Macro	Equivalent DDRCTL Testbench/Configuration Parameter
Specifies number of DfiClk pipeline stages added to all other dfi* signals, and to most dwc_ddrphy* signals	DWC_DDRPHY_PIPE_DFI_MISC	pipe_dfi_misc

Table 6-4 List of Macros in PHY VDEFINES file modified / checked by coreConsultant for Synopsys LPDDR5/4X PHY

Description	VDEFINES macro	Equivalent DDRCTL Testbench/Configuration Parameter
Number of channels	DWC_DDRPHY_NUM_CHANNELS_<n>	DFI1_EXISTS
Number of bytes per channels	DWC_DDRPHY_DBYTES_PER_CHANNEL_<n>	MEMC_DRAM_DATA_WIDTH/8 - divide value by 2 if DFI1_EXISTS=1
Number of Ranks	DWC_DDRPHY_NUM_RANKS_<n>	MEMC_NUM_RANKS
DMI/DBI support enabled	DWC_DDRPHY_DBYTE_DMI_ENABLED	Always enabled
LPDDR5 support enabled	DWC_DDRPHY_LPDDR5_ENABLED	Always enabled

Table 6-5 List of Macros in PHY VDEFINES file modified / checked by coreConsultant for Synopsys LPDDR5/5X/4X PHY

Description	VDEFINES macro	Equivalent DDRCTL Testbench/Configuration Parameter
Number of channels	DWC_LPDDR5XPHY_NUM_CHANNELS_n	DFI1_EXISTS
Number of bytes per channels	DWC_LPDDR5XPHY_NUM_DBYTES_PER_CHANNEL_n	MEMC_DRAM_DATA_WIDTH/8 - divide value by 2 if DFI1_EXISTS=1
Number of Ranks	DWC_LPDDR5XPHY_NUM_RANKS_n	MEMC_NUM_RANKS
DMI/DBI support enabled	DWC_LPDDR5XPHY_DBYTE_DMI_ENABLED	Always enabled
LPDDR5 support enabled	DWC_LPDDR5XPHY_LPDDR5_ENABLED	Always enabled

6.3 Integrating Host Interface (HIF)

The HIF on DWC_ddrctl is the command and data interface. Typically, you need to bridge this interface to an AXI or other system bus. This section provides guidelines for this. For more information about this interface, see the following sections of LPDDR5X/5/4X Memory Controller Databook:

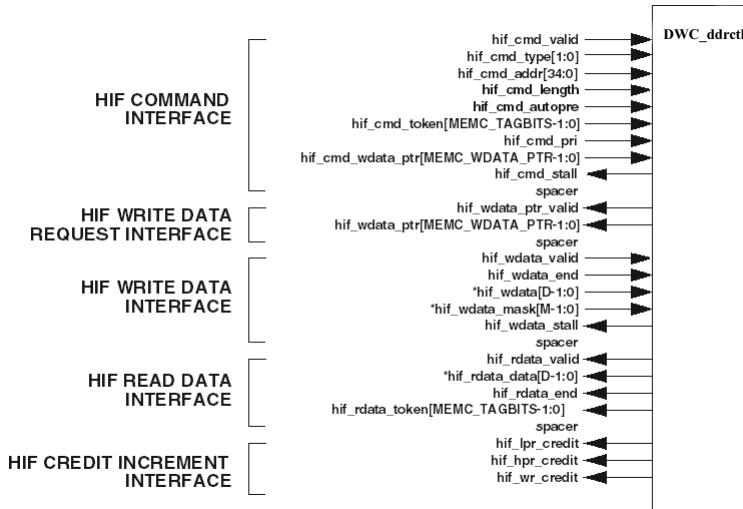
- Credit Requests
- Common Response
- Signals

The SoC core is required to maintain three credit counters - one each for the following queues:

- Low priority read
- High priority read
- Write command

A counter is decremented each time a command is sent to the DWC_ddrctl, and incremented each time a hif_*_credit signal from the DWC_ddrctl is asserted. For a read-modify-write (RMW) command, the low priority read and the write credit counters should both be decremented. These counters allow the SoC core to track the number of spaces available in the command queues. If a command queue is full (in other words, the credit counter is full), the SoC core must not send a command to that queue.

Figure 6-3 HIF Interface



The width of the data and mask signals depends on the configuration of the DDRCTL. For 1:1 mode configurations (MEMC_FREQ_RATIO=1), D=MEMC_DRAM_DATA_WIDTH*2. For 1:2 mode configurations (MEMC_FREQ_RATIO=2), D=MEMC_DRAM_DATA_WIDTH*4. In both cases, M=D/8.

6.3.1 HIF Command Interface

The HIF command interface consists of nine signals as shown in [Figure 6-3](#). These are summarized here:

- hif_cmd_valid qualifies all the command interface signals. The remaining command interface signals are ignored if this signal is de-asserted. The hif_cmd_valid signal must be asserted for one cycle for each command sent to the DWC_ddrctl (assuming that hif_cmd_stall is de-asserted).
- hif_cmd_type determines whether a write (00), read (01), or read-modify-write (RMW) (10) is sent.
- hif_cmd_addr is the word address (not the byte address).

- `hif_cmd_length` (for reads only) determines whether the read burst is of normal length (0) or partial length (in other words, half the normal length) (1).
- `hif_cmd_pri` (for reads only) determines whether the read is low priority (0) or high priority (1).
- `hif_cmd_autopre` determines whether the command should be issued to memory without (0) or with (1) an auto precharge. This can improve the efficiency in cases where it is known that the following command will or will not be a page hit.
- `hif_cmd_token` (for reads only) is a token for the command being sent. This must be generated by the SoC core and is returned from the DWC_ddrctl with the read data, so that out-of-order reads can be matched with their commands. The SoC core must keep track of which tokens are pending read responses, and must ensure that the token sent with each command does not match any pending token.
- `hif_cmd_wdata_ptr` (for writes and RMW only) is a pointer to the SoC core's own buffers, which is returned by the DWC_ddrctl when it is requesting the write data for this command. This field is not strictly required, as the write data is always requested by the DWC_ddrctl in the same order that the commands were sent.

6.3.2 HIF Write Data Request Interface

The write data request interface consists of two output signals from the DWC_ddrctl controller and is used to request that the SoC core sends the write data associated with a write or RMW command that has already been sent:

- `hif_wdata_ptr_valid` indicates that the `hif_wdata_ptr` signal is valid. If `hif_wdata_ptr_valid` is de-asserted, then `hif_wdata_ptr` should be ignored.
- `hif_wdata_ptr` is a pointer to the SoC core's own buffers, which matches the previously sent pointer by the SoC core as `hif_cmd_wdata_ptr`. It indicates the write command for which the DWC_ddrctl requires write data.

6.3.3 HIF Write Data Interface

The HIF write data interface conveys the write data from the SoC core to the DWC_ddrctl, and consists of five signals:

- `hif_wdata_valid` qualifies the other write data interface signals. If `hif_wdata_valid` is de-asserted, the other write data interface signals are ignored. It should be asserted for all cycles of the write data being sent to the DWC_ddrctl.
- `hif_wdata_end` indicates that the last cycle of data for the current transaction is sent. It should be asserted on the last cycle of data, and de-asserted on the other cycles.
- `hif_wdata` is the write data for the transaction.
- `hif_wdata_mask` is the byte mask for the transaction.
- `hif_wdata_stall` indicates that no write data can be accepted. If this is asserted, all other write data interface signals are ignored by the DWC_ddrctl.

6.3.4 HIF Read Data Interface

The HIF read data interface provides read data from the DWC_ddrctl to the SoC core. It consists of the following four signals:

- `hif_rdata_valid` qualifies the other read data interface signals. If this is de-asserted, all other read data interface signals should be ignored. It is asserted for all cycles in which the read data is valid.

- hif_rdata_data is the read data being returned from the DWC_ddrctl
- hif_rdata_end indicates that the current cycle is the last cycle of valid data for the current transaction.
- hif_rdata_token is a token which matches the hif_cmd_token that has been sent to the DWC_ddrctl with the command, and allows the SoC core to identify the command with which this read data is associated.

6.3.5 HIF Credit Increment Interface

The DWC_ddrctl indicates to the SoC core each time a command from one of the three command queues is scheduled to the SDRAM. This means that the SoC core should increment its credit count for that queue. The interface consists of one signal for each of the queues:

- hif_lpr_credit indicates that a low priority read command has been scheduled.
- hif_hpr_credit indicates that a high priority read command has been scheduled.
- hif_wr_credit indicates that a write command has been scheduled.

6.4 Integrating External RAM

The external RAM depth and width values depend on the values of other configured hardware parameters. It is not possible to configure these values during controller configuration. For the functions based on which the external RAM depth and width are calculated, see External RAM Interface Widths (information only) parameters in the HW/Multiport Parameters section of the “Parameter Descriptions” chapter in the LPDDR5X/5/4X Memory Controller Databook.

The exact configured values of the external RAM depth and width for your configuration can be obtained through the coreConsultant tool. See the generated DWC_ddrctl_cc_constants.v file after the controller configuration. You can also generate the ComponentConfiguration.html that provides these values. For information about generating reports, see “[Creating Optional Reports and Views](#)” on page [24](#).

For an understanding of the signals used and the related timing diagrams, see the “Write Data” and “Read Reorder Buffer” sections in the “System Interfaces” chapter of the Synopsys Controller IP LPDDR5X/5/4X Memory Controller Databook.

After you configure the controller in the coreConsultant tool, a report that gives the configured memory sizes and depths is available by clicking the Report tab under the Specify Configuration activity as shown in [Figure 2-4](#) on page [22](#). These can be used as input to a memory generator to produce the necessary memories that would be used in the Memory SubSystem. This report is also available in the text form at: <workspace>/export/mem.txt

A

Clock-Domain-Crossing (CDC) Synchronizers

This appendix provides a detailed information about the Clock Domain Crossing (CDC) strategy used in DDR controller. In addition, see “[Running Spyglass](#)” on page [28](#).

This appendix discusses the following topics:

- “[Clocks, Resets, and Clocking Scheme](#)” on page [84](#)
- “[Synchronizers Used in DDR Controller](#)” on page [85](#)
- “[Synthesis Constraints](#)” on page [87](#)
- “[Synchronization Method](#)” on page [89](#)
- “[CDC Constraints and Report](#)” on page [92](#)

A.1 Clocks, Resets, and Clocking Scheme

See the following sections:

- “Clock and Reset Requirements” section in the LPDDR5X/5/4X Memory Controller Databook.
- Clocks and Resets Signals in the Signal Descriptions chapter of the LPDDR5X/5/4X Memory Controller Reference Manual.

The figure “Simplified Relationship Between Clocks and Resets for Register Initialization” in the Programming chapter of the LPDDR5X/5/4X Memory Controller Databook illustrates the DDR controller clocking domain.

Main boundaries are:

- `pclk - aclk_n/core_ddrc_core_clk`: Crossing for configuration registers coming from the APB and used in the main logic, or for status/interrupt signals coming from the main logic and written to a status register. Crossing is done inside the APB device. Different methods for different type of registers are used. See “[Synchronization Method](#)” on page [89](#) for details. Whenever crossing is not necessary, no synchronizer is instantiated and value is simply passed through.
- `aclk_n - core_ddrc_core_clk`: Crossing between port n and the main logic. This is done inside the XPI block, primarily to transfer read/write command information and write data from the input port to the main logic and read data and read/write responses from the main logic to the output. Crossing is done through dual port FIFOs, see “[Data Bus Signals](#)” on page [90](#) for details. If crossing is not necessary, a single clock dual-port FIFO is used instead. See “[Asynchronous FIFO Glitch Free MUX Replacement](#)” on page [90](#) for details.
- `chi_clk_n - core_ddrc_core_clk`: Crossing between port n and the main logic. This is done inside the CHB block, primarily to transfer RXREQ Channel Command information and RXDAT Channel Write Data from the input ports to the downstream logic. This crossing allows transfer of Read data on TXDAT Channel and Read/Write responses on the TXRESP Channel responses from the main logic to the output ports. Crossing is done through dual port FIFOs, see “[Data Bus Signals](#)” on page [90](#) for details. If crossing is not necessary, a single clock dual-port FIFO is used instead. See “[Asynchronous FIFO Glitch Free MUX Replacement](#)” on page [90](#) for details.

A.2 Synchronizers Used in DDR Controller

A synchronizer is instantiated for every signal, register or data-bus crossing between different clock domains, with the exception of APB static and quasi-dynamic registers. For details, see “[APB Static Registers](#)” on page [89](#).

DDRCTL uses proven blocks, called Basic Core Modules (BCMs), to implement CDC. It uses a library of design-specific CDC parts that are mapped to the standard DesignWare library parts in <http://www.synopsys.com/dw/buildingblock.php> as follows:

Table A-1 DDRCTL to DesignWare Library Part Mapping

DDRCTL Part Name	DesignWare Library Part Name	Type of Synchronizer
AXI Interface Crossing		
DWC_ddrctl_bcm21.v	DW_sync	Single Clock Data Bus Synchronizer
APB Interface Crossing		
DWC_ddrctl_bcm25.v	DW_data_sync (x2 DW_sync plus flipflop)	Data Bus Synchronizer with Acknowledge
DWC_ddrctl_bcm23.v	DW_pulseack_sync	Pulse Synchronizer with Acknowledge
AXI Clock Domain Crossing		
DWC_ddrctl_bcm02.v	DW_mux_any	Universal Multiplexer
DWC_ddrctl_bcm05.v	DW_fifoctl_if	Submodule of DWbb_bcm07
DWC_ddrctl_bcm06.v	DW_fifoctl_s1_df	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DWC_ddrctl_bcm07.v	DW_fifoctl_s2_sf	Synchronous (Dual-Clock) FIFO Controller with Static Flags
DWC_ddrctl_bcm50.v		Memory read data multiplexer
DWC_ddrctl_bcm56.v		Memory array, used together with DWC_ddrctl_bcm50.v
DWC_ddrctl_bcm57.v	DW_ram_r_w_s_dff	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop Based)
DWC_ddrctl_bcm58.sv		Dual clock two port RAM with re-timing registers (Flip-Flop Based)
DWC_ddrctl_bcm65.v	DW_fifo_s1_sf	Synchronous (Single Clock) FIFO with Static Flags
DWC_ddrctl_bcm66_wae.sv	DW_fifo_s2_sf	Synchronous (Dual-Clock) FIFO with Static Flags with output ports for write address and write enable
Automotive Crossing		
DWC_ddrctl_bcm65_atv.v		Automotive version of DWC_ddrctl_bcm65.v

DDRCTL Part Name	DesignWare Library Part Name	Type of Synchronizer
DWC_ddrctl_bcm66_wae_atv.sv	DW_fifo_s2_sf	Synchronous (Dual-Clock) FIFO with Static Flags for Automotive IP with output ports for write address and write enable
DWC_ddrctl_bcm05_atv.v		Automotive version of DWC_ddrctl_bcm05.v
DWC_ddrctl_bcm06_atv.v		Automotive version of DWC_ddrctl_bcm06.v
DWC_ddrctl_bcm07_atv.v		Automotive version of DWC_ddrctl_bcm07.v
DWC_ddrctl_bcm21_atv.v		Automotive version of DWC_ddrctl_bcm21.v
DWC_ddrctl_bcm95_i.v		Triple Module Replication (TMR) Register used for Automotive support

A.3 Synthesis Constraints

The synthesis constraints applied to the design obey to a specific CDC Methodology, adding timing exceptions which override the default flop-to-flop timing paths that are defined for each individual clock domain. The set_max_delay constraint overrides the setup timing checks into the destination flip-flop while the set_min_delay constraint overrides the hold timing checks into the destination flip-flop. The "-ignore_clock_latency" switch in the set_max_delay/set_min_delay constraints is required in order to remove the clock tree latency from the timing calculations.

Note that set_false_path constraint has higher priority than set_max_delay/set_min_delay constraints, therefore these must not be used to constraint the same paths, otherwise set_max_delay/set_min_delay constraints will be ignored.

The CDC Methodology obeys to the following rules:

1. Global constraints are applied between asynchronous clocks. Every path between two different clock domains is constrained with a maximum delay (set_max_delay) equal to 150% of the destination clock period.

This ensures that the qualified data is always ready when the qualifier arrives. This constraint may be too strict in some cases (previous constraint always considers the worst case, that is when using a double register synchronizer).

If you encounter any difficulties meeting timing at the clock boundaries, the constraint can be relaxed by setting the maximum delay to (number of synchronizer stages - 0.5) * destination clock periods for qualified data signals.

These global constraints will be overridden if any specific path constraints are applied.

2. Use "-allow_paths" switch with set_clock_groups

The set_clock_groups constraint can be used to provide clock group information required in Signal Integrity analysis during P&R only if switch "-allow_paths" is included, otherwise set_max_delay / set_min_delay constraints will be ignored.

3. Define set_max_delay of 1 source clock period and set_min_delay of 0 constraints for Gray-coded signals

A "set_max_delay -ignore_clock_latency" constraint equivalent to 1 period (or less) of the source clock domain shall be applied in all Gray-coded signals reaching the first synchronization flip-flops in the destination clock domain. A "set_min_delay -ignore_clock_latency" constraint with value 0 shall be applied to the same paths. These constraints will ensure that only valid Gray codes will be sampled in the destination clock domain.

4. Define set_max_delay of (Number of Sync stages-0.5) x destination clock period and set_min_delay of 0 constraints for Qualifier-based Data Bus signals

A "set_max_delay -ignore_clock_latency" constraint equivalent to (Number of Sync stages - 0.5) x period (or less) of the destination clock domain shall be applied in Qualifier-based Data Bus signals reaching the first synchronization flip-flops in the destination clock domain. A "set_min_delay -ignore_clock_latency" constraint with value 0 shall be applied to the same paths. These constraints will ensure that the Data Bus signals are stable when sampled in the destination clock domain.

5. Define set_max_delay of 1 destination clock period and set_min_delay of 0 constraints for all CDC crossings (excluding Gray-coded and Qualifier-based Data Bus signals)

A "set_max_delay -ignore_clock_latency" constraint equivalent to 1 period (or less) of the destination clock domain shall be applied in all CDC crossings (excluding Gray-coded and Qualifier-based Data Bus signals) reaching the first synchronization flip-flops in the destination clock domain. A "set_min_delay -ignore_clock_latency" constraint with value 0 shall be applied to the same paths. These

constraints limit the separation between the flip-flops connecting the source and destination clock domains, therefore maintaining the assumptions for a safe CDC implementation.

6. Define "set_false_path -through" constraint for quasi-static signals at the output of the Bus Delay components

Since quasi-static signals are not required to meet timing, the "set_false_path -through" constraint will remove the timing checks on those paths. The "set_false_path -through" constraint shall be applied to the output pin of Bus Delay components (DWC_ddrctl_umctl2_bcm36_nhs).

A script runs an exhaustive search for the CDC cells instantiated through the design and applies the necessary constraints automatically.

In some configurations, synthesizer might be able to simplify the logic at the FIFO output. Doing so, it may get rid of some of the AND gates which protect against glitch propagation in the destination domain when the FIFO is empty.

To avoid unwanted optimization at the FIFO outputs, it is required to use the set_size_only constraint applied to the leaf cells of all the FIFO qualifiers. This allows the respective AND gates to be resized while preserving the AND gate functionality.

The following synthesis constraint applies the size_only attribute to the leaf cells of all U_AND_2TO1_SIN instances:

- ```
foreach_in_collection cell [get_cells -hierarchical U_AND_2TO1_SIN*] {set_size_only -all_instances [get_cells [get_object_name $cell]/*]}
```

Both the CDC methodology and "set\_size\_only" constraints are applied during the synthesis constrain phase, by automatically writing these constraints into the design constraints file, which can be found in <path\_to\_cC\_workspace>/syn/constrain/script/DWC\_ddrctl.tcl.

## A.4 Synchronization Method

The DDRCTL uses different types of synchronizers depending on type of signal to be crossed.

All synchronizers internally implement missampling models for verification purposes. These models are set to introduce missampling errors randomly from 0 to 1 clock cycle. Models can be enabled by defining the macro DW\_MODEL\_MISSAMPLES.

### A.4.1 APB Static Registers

No synchronization is done in this case.

Registers defined as static must not be reprogrammed outside reset. Their value in pc1k is simply sampled directly in the destination domains (core\_ddrc\_core\_clk/ac1k domains) without synchronizing circuits.

Registers defined as quasi dynamic are crossed the same way (that is, without synchronizers), but they can be changed outside reset, for details, see “Quasi Dynamic Registers” in the LPDDR5X/5/4X Memory Controller Databook.

The naming convention used in the APB device logic makes it easy to identify these registers. Their instances are denoted by the prefix "cfgs\_ff" within the apb\_slvif module.

### A.4.2 Dynamic Single Bit Signals

For single bit signals that are assured to keep their value for at least a guaranteed number of destination clock cycles, a standard multiple register synchronizer is used. Depth of synchronizer can be programmed to 2, 3 or 4, depending on the needs.

Such signals can be easily identified in the logic. In a CDC report generated by a CDC checking tool (Spyglass CDC/Meridian CDC), destination points which contain instance of bcm21, are signals synchronized using this method. For details about how to generate a report with Spyglass, see “[CDC Constraints and Report](#)” on page [92](#).

For the list of APB registers that fall into this category, see “Dynamic Registers”.

**Figure A-1 Standard Double Register Synchronizer**



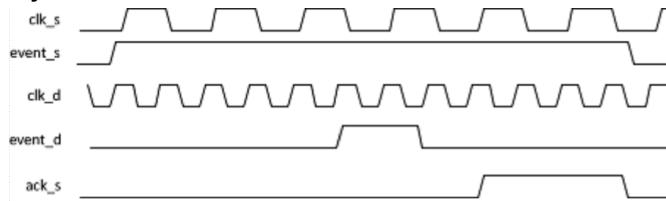
### A.4.3 Pulse Signals

Pulses are synchronized through a dual clock pulse synchronizer.

This is the case for one-to-set/one-to-clear type registers in the APB logic. These registers can be easily identified in a CDC report as a destination point whenever there is an instance of bcm23.

[Figure A-2](#) shows the synchronizer behavior: event\_s is crossed to a single clock signal event\_d in the destination domain. Acknowledge is then sent back to the source domain and at this stage input can be cleared.

**Figure A-2 Dual Clock Pulse Synchronizer**

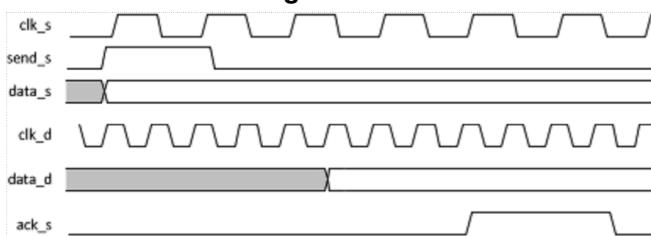


#### A.4.4 Data Bus Signals

Data bus signals such as multi bit dynamic configuration registers are crossed through a data bus synchronizer with acknowledge. A one clock cycle signal on the source domain indicates the end of the transfer.

Such signals can be identified in a CDC report as destination point whenever there is an instance of bcm25.

**Figure A-3 Data Bus Synchronizer with Acknowledge**



Data buses that are required to stream are synchronized through FIFOs, which internally implement a dual-clock FIFO synchronizer, which can be recognized when an instance of bcm07 is seen in the destination point. This is the case for data, address and response paths inside the XPI.

Every FIFO is equipped with empty/full signals for handshake purposes.

#### A.4.5 Asynchronous FIFO Glitch Free MUX Replacement

The asynchronous FIFOs (DWC\_ddrctl1\_bcm66\*.sv) used in the memory controller uses a module DWC\_ddrctl1\_bcm58 to implement the memory array. There is a MUX inside this module which is implemented using an array of DWC\_ddrctl1\_bcm00\_nand instances.

The NAND functionality is implemented inside the DWC\_ddrctl1\_bcm00\_nand block as:

```

`ifdef DWC_NAND_SRC
`DWC_NAND_SRC
`else
 assign zn = ~(a&b);
`endif

```

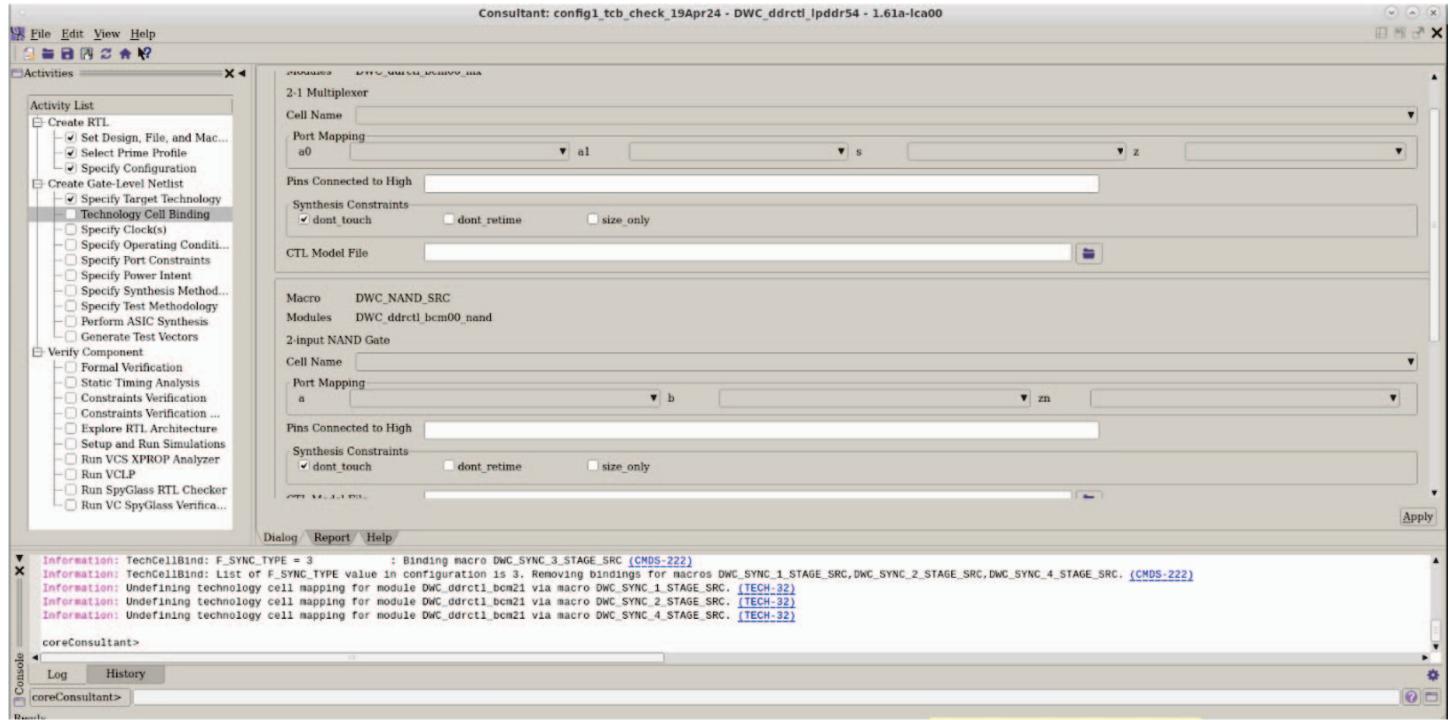
You must define the macro DWC\_NAND\_SRC to use the NAND technology cell and map the inputs and outputs to a, b, and zn. You must define set\_size\_only SDC constraint on the NAND technology cells to

prevent optimization of the logic by synthesis tools. This is important to prevent glitch propagation through the CDC logic inside the asynchronous FIFO.



Technology Cell Binding activity in coreConsultant can be used to replace DWC\_NAND\_SRC with the technology cell and apply dont\_touch/dont\_retime/size\_only synthesis constraint.

**Figure A-4 CoreConsultant Technology Cell Binding Window**



## A.5 CDC Constraints and Report

You can use the coreConsultant tool to generate a report of the clock domain crossing paths. This is useful when compiling a list of registers where timing checks can be ignored in gate-level simulations. For more information, see “[Running Spyglass](#)” on page [28](#). To generate the CDC report only `cdc/cdc_verify_struct` Goal is needed.

Spyglass CDC constraints for your specific configuration are provided with the coreConsultant tool. After configuring the controller, execute the Spyglass flow as explained in the section “[Running Spyglass](#)” on page [28](#). You can find the CDC constraints and waiver files in your workspace as documented in [Table 3-2](#) on page [30](#).

Two main reports are generated in directory

`<workspace>/spyglass/work/core/<top_name>/cdc/cdc_verify_struct/spyglass_reports/clock-reset/`

- `Ar_sync01.csv`: Spreadsheet containing all the reset synchronizers
- `Ac_sync01.csv`: Spreadsheet containing register crossings for scalar signals within the IP with source and destination point
- `Ac_sync02.csv`: Spreadsheet containing register crossings for vector signals within the IP with source and destination point

Each line of the `Ar_sync01` spreadsheet refers to a specific reset, information provided are:

- RESET: Reset signal source path
- PINTYPE: Reset type (clear / set)
- INSTANCE: Destination register
- CLOCK: Destination clock
- SYNCHRONIZER: path to the reset synchronizer

Each line of `Ac_sync02` spreadsheet refers to a specific register which is synchronized between a source and a destination clock. Information provided are:

- SOURCE: Start point
- SOURCE CLOCK: Clock start point
- DEST: End point
- DEST CLOCK: Clock end point
- METHOD: Synchronization method (synchronizer cell name)
- CSV FILE: Spreadsheet for the specific crossing

More information about each crossing can be found in the csv file linked in `Ac_sync02.csv`.

# B

## Additional coreConsultant Information

---

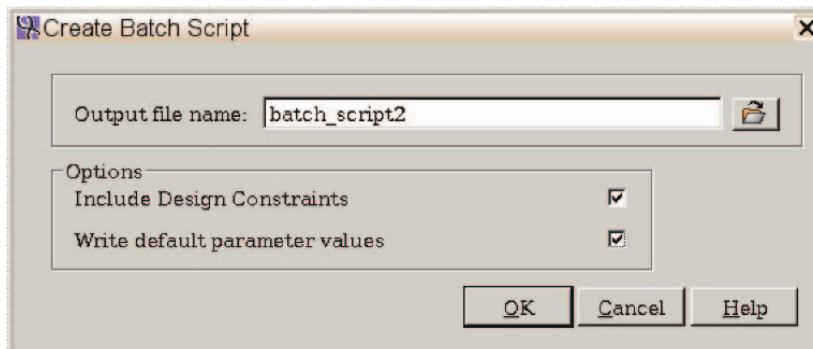
The topics in this appendix are as follows:

- “[Creating a Batch Script](#)” on page [94](#)
- “[Help Information](#)” on page [95](#)
- “[Workspace Directory Structure Overview](#)” on page [97](#)
- “[Dumping Debug Information when Problems Occur](#)” on page [98](#)

## B.1 Creating a Batch Script

Batch mode allows you to execute a series of coreConsultant commands from a batch file. To create a batch file, choose the **File > Write Batch Script** menu item and enter a name for the file (shown in [Figure B-1](#)).

**Figure B-1 Create Batch Script**



You can review and edit the batch file by looking at the file in an ASCII editor.

- By default, the ‘parameter configuration’ section of the batch script only specifies those parameters whose values have been changed by you from their default values.
- If you have not modified any of the default information in the Synthesis section, it is possible to remove the very verbose synthesis intent commands from the batch script.
- Depending on how you plan to use the batch script (see next paragraph), you may be able to remove all the initial statements from the batch script that deal with creating the workspace. You can prefer to create a batch script that is only used to set configuration parameters and to control all other activities manually.

You can use the batch script to reproduce the workspace using any of the following methods:

- To run in non-GUI batch mode:

```
% coreConsultant -shell -f <batch_file_name>
```

- To run in GUI mode:

```
% coreConsultant
```

If your batch script does not have any commands for creating a workspace, then you must create a workspace first. For more information on creating a workspace, see “[Creating the Workspace](#)” on page [19](#).

- Source the batch file from the coreConsultant command line:

```
source <batch_file_name>
```

Your source the batch file before, or after, you have created a workspace, depending on whether the script includes commands to create the workspace.

## B.2 Help Information

Several types of online help are available through coreConsultant:

- coreConsultant User Guide and Command Reference

These are available through the Help menu (see [Figure B-2](#)) and are also available at <cc\_tool\_root>/.../doc/dware where <cc\_tool\_root> is the path to your coreConsultant executable as returned by typing the following command in a Unix shell:

```
% which coreConsultant
```

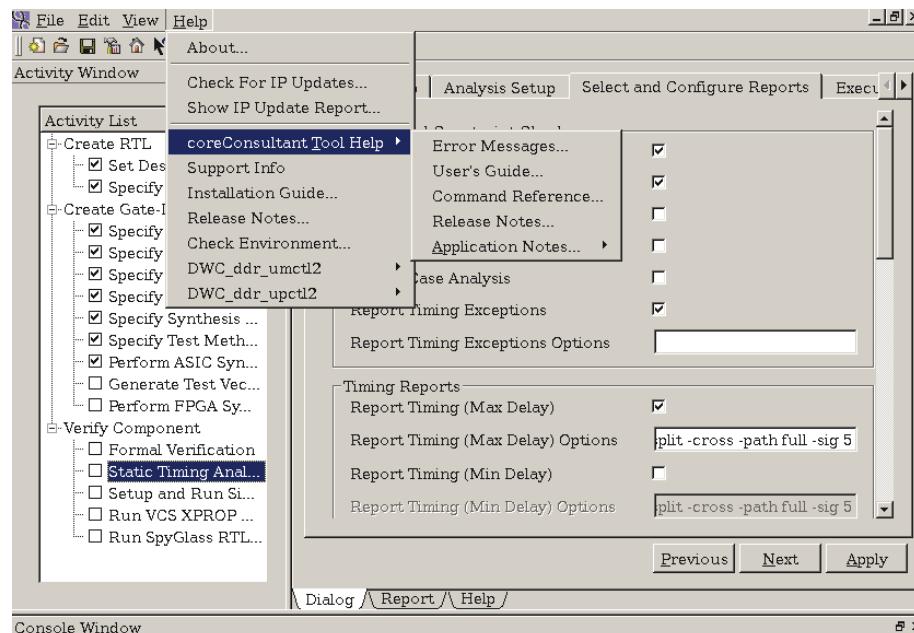
- "What's This?" Quick Help**

When you position your mouse pointer over a GUI item and right-click, coreConsultant displays a menu with the **What's This?** option. Clicking **What's This?** displays a brief help message for the selected item. **What's This?** can also be accessed by left-clicking the Question Pointer on the toolbar and then left-clicking on a GUI item.

- The Toolbar Help Menu**

Click the toolbar Help button to show a list of help topics. When you click a topic, the corresponding help information appears. [Figure B-2](#) shows the Help pull-down with the available manuals for both the DDR controller and the coreConsultant tool.

**Figure B-2 coreConsultant Help Menu Pull-down Showing DDR Controller and coreConsultant Manuals**



- Activity View Help Tab**

The Activity View pane features a **Help** tab that displays a detailed, context-specific help page, with additional links to the online command reference and other appropriate references.

## ■ Help on coreConsultant Commands

The Synopsys coreTools Online Command Reference Index is available through the Help menu. It contains a collection of man pages for all coreConsultant commands, attributes, variables, and item types.

You can also access coreConsultant command help by entering one of the following commands at the coreConsultant prompt in the Console pane:

```
coreConsultant> help [cmd] [-verbose]
coreConsultant> cmd -help
coreConsultant> man [cmd]
```

## B.3 Workspace Directory Structure Overview

For standard coreConsultant workspace directory structure, see the “coreKits and Workspaces” section in the *CoreConsultant User Guide*.

## B.4 Dumping Debug Information when Problems Occur

The menu entry, **File > Build Debug Tar-file**, is used to capture debug information for the Synopsys Support Center. This menu item creates the file <working\_dir>/debug.tar.gz.

This debug file includes:

- Batch script for recreating the workspace
- Output from the existing debug\_info command
- Synthesis and simulation log files (if available)
- Results of an environment check (if available)

# C

## OCCAP Synthesis Constraints

If you are using the OCCAP feature (see “On Chip Command and Address Path Protection (OCCAP)” in the LPDDR5X/5/4X Memory Controller Databook), special care is needed with respect to synthesizer setup for the following:

- Duplicated modules (see ‘Duplication with Comparison’ section in the LPDDR5X/5/4X Memory Controller Databook.)
- Automotive FIFO controllers (see ‘Automotive FIFO Controllers’ section of the LPDDR5X/5/4X Memory Controller Databook).
- Triple Module Replication (TMR) of specific registers (See ‘Triple Module Replication (TMR) of Registers’ section in the LPDDR5X/5/4X Memory Controller Databook).

Synthesizer might be able to “simplify” the logic of these features which use redundant logic for protection. For example, the duplicated modules may be incorrectly simplified by combining some of the registers in one instance of the module with the other instance of same module.

The topics in this appendix are as follows:

- “[Duplicated Modules](#)” on page [100](#)
- “[Automotive FIFO Controllers](#)” on page [101](#)
- “[Triple Module Replication \(TMR\) of Specific Registers](#)” on page [102](#)
- “[Duplicated Parity Bit for Register Bit of Type R/W1C and R/W1S](#)” on page [103](#)

## C.1 Duplicated Modules

To avoid unwanted optimization on this logic, it is recommended to use the "set hierCells" attribute for the cells of the duplicated modules. An example of this is as follows:

- set hierCells [get\_cells -quiet -hierarchical { \*ddrc\_ctrl\_inst\* \*mr\_inst\* \*rd\_inst\* \*RP\_inst\* \*WP\_inst\* \*WS\_inst\* \*AU\_inst\* }]
- if {[sizeof\_collection \$hierCells]} { set\_ungroup \$hierCells false}



**Note** If synthesis runs in cC environment, the above constraints are part of the coreTools customizations that are automatically done. Otherwise, you must ensure that these constraints are part of your SDC.

## C.2 Automotive FIFO Controllers

To avoid unwanted optimization on this logic, it is recommended to use the “set size\_only” attribute for the cells of the triplicated registers/modules.

For all configurations, DWC\_ddrctl\_bcm95\_i is used and its internal register has a unique name when triplicated: “dw\_so\_reg”. Hence, an example for this is as follows:

- `foreach_in_collection cell [get_cells -hierarchical *dw_so_reg*] {set_size_only -all_instances [get_cells [get_object_name $cell]]}`

Furthermore, when using Asynchronous AXI ports, the DWC\_ddrctl\_bcm21\_atv is used inside the DWC\_ddrctl\_bcm05\_atv (synchronous (Dual Clock) FIFO controller). Hence, it is recommended to use the following:

- `set_size_only -all_instances [get_cells -hierarchical *sample_meta*]`
- `set_size_only -all_instances [get_cells -hierarchical *sample_sync*]`

### C.3 Triple Module Replication (TMR) of Specific Registers

To avoid unwanted optimization on this logic, it is recommended to use the “set size\_only” attribute for the cells of the triplicated registers inside the DWC\_ddrctl\_bcm95\_i module:

- `foreach_in_collection cell [get_cells -hierarchical *dw_so_reg*] {set_size_only -all_instances [get_cells [get_object_name $cell]]}]`



This is already covered by the Automotive FIFO controller synthesis requirements.

## C.4 Duplicated Parity Bit for Register Bit of Type R/W1C and R/W1S

To avoid unwanted optimization of duplicated register parity bit of type R/W1C and R/W1S, it is recommended to use the “set\_size\_only” attribute for the register parity bit:

- ```
foreach_in_collection cell [get_cells -hierarchical *ff_regb*_parity*] {  
    set_size_only -all_instances [get_cells [get_object_name $cell]]  
}
```