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**Axelera LPDDR Subsystem Verification Testplan**

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# **Revision History**

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# **Introduction**

## **Document Scope**

This Document provides information regarding the Verification Plan of the LPDDR Subsystem. It lists all the different testcases planned as part of Verification for the LPDDR Subsystem. For each test case it provides a brief description, covering intent of the test and targeted functionality along with Combinations which are planned to be covered by verification. It also lists Reference Information pointers for better understanding.

**Note:** The test cases defined in Section 2, provide a brief overview of what is planned to be targeted for the verification of the associated functionality. However, the detailed Verification methodology in terms of concept of Stimulus definition, Checkers and Scoreboard approach is defined in the “Axelera LPDDR Subsystem Verification Specification” Document.

## **References Used**

Table : List of References

|  |  |  |  |
| --- | --- | --- | --- |
| **Sr. No.** | **Name of Document** | **Version** | **Owner** |
| 1 | Axelera\_Europa\_LPDDR5X\_Subsystem\_Databook | 0.6 | Axelera |
| 2 | Axelera\_Europa\_LPDDR5X\_Subsystem\_Reference\_Manual | 0.7 | Axelera |
| 3 | LPDDR5X/5/4X Memory Controller Databook | 1.60a | Synopsys, Inc |
| 4 | LPDDR5X/5/4X Memory Controller Reference Manual | 1.60a | Synopsys, Inc |
| 5 | LPDDR5X/5/4X PHY Utility Block (PUB) Databook | 2.30a | Synopsys, Inc |
| 6 | Axelera LPDDR Subsystem Verification Specification |  | Siemens |

# **Verification Testplan**

## **Initialization and Configuration Testing**

### **Initialization Test**

**Description:**

This testcase verifies that the Subsystem performs completes initialization steps per the LPDDR Protocol to Initialize the SDRAM and updates STAT.operating\_mode as normal after initializing the DDR controller and PHY.

Note: Table 14-1 of Controller Databook and Section 6.4.1 of PHY Pub Databook are confirmed as steps required to verify the correct initialization here.

**Combinations to be Covered:**

- Cover combination of INITTMG0.skip\_dram\_init=0,01,11.

- Cover the DDRCTRL reset core\_ddrc\_rstn application

- Cover the HardIP(Reset\_async) and warm reset (Reset) of phy application

- Cover logic '0' and '1' for DFIMISC.dfi\_init\_start, DFISTAT.dfi\_init\_complete for PHY Initialization.

- Cover the STAT.operating\_mode as Normal Mode(value 1).

- Cover below values for MSTR0.burst\_rdwr and MSTR0.data\_bus\_width:

MSTR0.burst\_rdwr as BL16

MSTR0.data\_bus\_width as 00 (FBW) and 01 (HBW).

- Cover below logic values:

MSTR0.active\_ranks = 01, 11

**Reference Information:**

Axelera\_Europa\_LPDDR5x\_Subsystem\_databook.pdf Section 3.5

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section 14.1

### **APB Address Decoding Test**

**Description:**

This testcase verifies that the Subsystem APB decoder differentiates DDR PHY and Controller accesses based on bits 25:22 of the APB Address.

**Combinations to be Covered:**

- Cover read and write of different DDR Controller Registers by setting APB Address bit 25 to logic '0'

- Cover read and write of different PHY Registers by setting APB Address bit [25 :22] as 'b1000 and other address bits to ensure one access in each region of PHY Address Space.

- Cover application of APB Reset, presetn

**Reference Information:**

Axelera\_Europa\_LPDDR5x\_Subsystem\_databook.pdf Section 3.8

### **Mode Register Write/Read Testing**

**Description:**

This test case verifies that the Subsystem is performing Mode register write and reads through APB Configuration registers MRCTL0, MRCTL1, MRSTAT.

**Combinations to be Covered:**

Cover different combinations between following configurations:

- Different data on MRCTRL0.mr\_addr, MRCTRL0.mr\_rank, MRCTRL1.mr\_data(in case of write only) for MRR/MRW.

- logic '0' and '1' values on MRCTRL0.mr\_type, MRCTRL0.mrr\_done\_clr and MRSTAT.mrr\_done

- Configured MR Values by MRW on INITMR\*

- Response of MRR command on MRRDATA0 and MRRDATA1.

- perf\_op\_is\_load\_mode as logic '0' and '1'

- Non zero values on hif\_mrr\_data with hif\_mrr\_data\_valid as logic '1'

- Cover perf\_precharge\_for\_other to logic 1 when Pre-charged Issued due to MRW.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:10.1

### **DDRCTL Data Bus Inversion Test**

**Description:**

This test case verifies that the Subsystem is performing Data Bus Inversion as configured through APB Configuration register DBICTL and DFIMISC.

**Combinations to be Covered:**

Cover different combinations of DBICTL.rd\_dbi\_en, DBICTL.wr\_dbi\_en, DBICTL.dm\_en with logic '0' and '1' value of DFIMISC.phy\_dbi\_mode and data values with less than and more than 4 logic '1' in the data byte.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:10.2

## **Traffic flow and Address Translation Testing**

### **AXI Input Traffic Handling**

**Description:**

This testcase verifies that the Subsystem performs correct conversion of incoming AXI Read and Write Transactions of different sizes and addresses before sending on the DDR SDRAM Interface.

**Combinations to be Covered:**

Cover AXI Read and Write Transactions on the AXI Interface with the following attributes:

- Cover different values for burst type (FIXED, INCR and WRAP)

- Cover different Burst Size less than AXI data width

- Cover different Burst Length values.

- Cover different Burst Address values with different regions with addresses aligned and unaligned to Burst Boundaries.

- Cover different values on QOS

- Cover Unsupported Region, Checksum, Flow Control, Burst Transfer Error (Incomplete Bursts), Transfer Size Violation and Addressing Errors (Invalid and Unaligned Addresses)

Cover the different values of following performance logging signals

- perf\_bank[2:0]

- perf\_bg[1:0]

- perf\_dfi\_rd\_data\_cycles

- perf\_dfi\_wr\_data\_cycles

- perf\_hif\_rd

- perf\_hif\_rd\_or\_wr

- perf\_hif\_wr

- perf\_op\_is\_cas

- perf\_rank

- perf\_hif\_rmw

Cover application of AXI Reset, aresetn\_0

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:3.1, 3.3

Axelera\_Europa\_LPDDR5X\_Subsystem\_Reference\_Manual.pdf Section 1.26

### **Address Translation Test**

**Description:**

This testcase verifies that Subsystem performs correct address translation of incoming AXI Read and Write Transactions by considering the recommendations mentioned in Section-6.4 of DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf before sending them on the DDR SDRAM Interface and support Bank Hashing Feature. It also verifies that the Subsystem is mapping Address according to selected bank architecture based on the programming of APB Configuration Registers DRAMSET1TMG24 , ADDRMAP3, ADDRMAP4, ADDRMAP5, ADDRMAP6 and that it generates SLVERR in response to invalid addresses if configured as a Non-Binary Device Density in ADDRMAP12.

**Combinations to be Covered:**

- Cover different ranges of AXI Read and Write transactions with addresses resulting in access to:

- Each rank, bank and bank group.

- Different ranges of row and column addresses on each page.

- Cover different valid values for non-reserved bits of ADDRMAPx (x=0 to 12) as defined in DWC\_ddrctl\_lpddr54\_lpddr5x\_reference.pdf to select the HIF address bits used as bits for rank, bank, bank group, row and column addresses.

- Cover ADDRMAP12.bank\_hash\_en as logic '0' and '1'

- Cover DRAMSET1TMG24.bank\_org = 0 (BG Mode) and 2 (16B Mode)

- Cover following configuration for Address map Recommendations (As per Section-6.4):

ADDRMAP6.addrmap\_col\_b3 = 0

ADDRMAP6.addrmap\_col\_b4 = 0

ADDRMAP4.addrmap\_bg\_b0 = 2

- Cover below cases for Non-binary Subsystem Densities:

Cover all eight combinations of ADDRMAP12.nonbinary\_Subsystem\_density and AXI Reads and Writes resulting in Address Error for each of these density Configurations.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:6.2, 6.3, 6.4, 6.5, 6.7

### **LPDDR5 WCK Clocking Test**

**Description:**

This test case verifies that the Subsystem is managing WCK by DDRCTL as programmed using APB Configuration Registers DFITMG4, DFITMG5, TMGCFG, MSTR4 and issues CAS-WS\_RD, CAS-WS\_WR, CAS-WS\_FS, CAS-WS\_OFF and CAS-WCK\_SUSPEND commands as required.

**Combinations to be Covered:**

- Cover different timing values of DFITMG[4|5].dfi\_twck\_\*.

- TMGCFG.frequency\_ratio as logic '1'

- Cover logic '0' and '1' value on MSTR4.wck\_on, MSTR4.ws\_off\_en, MSTR4.wck\_suspend\_en in different combinations

- Cover following performance logging signals as logic '0' and '1'

perf\_op\_is\_cas\_wck\_sus

perf\_op\_is\_cas\_ws

perf\_op\_is\_cas\_ws\_off

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:12.3

### **Page Match Feature**

**Description:**

This test case verifies that the Subsystem Locks on read and write ports when consecutive transactions to same page are observed and page match enable is for the port is set to logic '1' unless it needs to release lock due to credit unavailable, another high priority request or timeout out ports.

**Combinations to be Covered:**

Cover different combinations of following registers with associated values:

- logic '1' and '0' values for following registers:

PCFGW.wr\_port\_pagematch\_en

PCFGR.rd\_port\_pagematch\_en

- Different values of the PCCFG.pagematch\_limit register

- Consecutive AXI Reads and Writes with addresses on same and different page

- Timeouts on other ports

- Read/Write credit unavailability

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 3.1.2.7

### **Throughput Test**

**Description:**

This testcase verifies the throughput of the Subsystem by generating the maximum traffic over the AXI port by sending multiple reads and writes with different address values and QOS.

**Combinations to be Covered:**

Cover following traffic scenarios:

1. Back to back AXI Reads and Writes with similar QOS with Maximum Burst Length and Size on different addresses

2. Back to back AXI Reads and Writes with different QOS with Maximum Burst Length and Size on different addresses

3. Following Configurations:

- Minimum timing for Latency Values in Mode Register and APB Configuration registers for timings between commands.

- Maximum timing for all periodic maintenance timers (Example Refresh, ZCal)

- DRAMSET1TMG24.bank\_org = 0 (BG Mode) to support maximum speed

**Reference Information:**

NA

### **Transaction Poisoning Test**

**Description:**

This testcase verifies how the Subsystem Handles the Poisoned Transactions on AXI Subordinate Interface

**Combinations to be Covered:**

Cover different combinations of below registers with associated values:

- logic '1' and '0' on Sideband Signals arpoison and awpoison on AXI for Poisoned transaction for AXI reads and writes.

2. Cover logic '0' and '1' value on POISONCFG.rd\_poison\_slverr\_en, POISONCFG.rd\_poison\_intr\_en, POISONCFG.rd\_poison\_intr\_clr, POISONCFG.wr\_poison\_slverr\_en, POISONCFG.wr\_poison\_intr\_en, POISONCFG.wr\_poison\_intr\_clr.

3. POISONSTAT.wr\_poison\_intr\_0 and POISONSTAT.rd\_poison\_intr\_0 as logic '1' and '0'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:3.1.1.10

### **Async Performance Counter Test**

**Description:**

This testcase verifies that the Subsystem updates each instance of performance counter output on o\_cntrl\_cnt\_value based on i\_count\_inc and i\_ctrl\_cnt\_en and checks the reset value to 0 based on flush input.

**Combinations to be Covered:**

- Cover both logic value 1 and 0 of register values which control i\_cntr\_en and i\_ctrl\_cnt\_flush

- Cover incrementing non-reset values on o\_cntrl\_cnt\_value

- Cover the transition of o\_cntrl\_cnt\_value from non-reset to reset value with i\_ctrl\_cnt\_flush input

**Reference Information:**

## **Command Scheduling**

### **Page Policy Test**

**Description:**

This test case verifies that the Subsystem is supporting Page Policy feature as programmed through APB Configuration Registers SCHED0, SCHEDTMG0.

**Combinations to be Covered:**

- Cover both logic '1' and '0' value of SCHED0.pageclose with zero and different non-zero values of SCHEDTMG0.pageclose\_timer

- Cover the last Read/Write with auto-precharge command when SCHED0.pageclose is set to ’1’ and SCHEDTMG0.pageclose\_timer=0

- Cover precharge command when SCHED0.pageclose is set to ’1’ and SCHEDTMG0.pageclose\_timer>0.

- Consecutive AXI Reads and Writes to same and different page addresses

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:7.2

### **Write to Read Switching**

**Description:**

This testcase verifies that switching the direction of read or write and prepare the page of the bank for it by sending back to back write and read in different order.

**Combinations to be Covered:**

Cover different combinations of following registers and associated values:

- PCFGQOS0.rqos\_map\_level[1|2] and PCFGQOS0.rqos\_map\_region[0|1|2] as different valid values

- PCFGWQOS0.wqos\_map\_level[1|2] and PCFGWQOS0.wqos\_map\_region[0|1|2] as different valid values

- Different timeout values on registers PCFGQOS1\_n.qos\_map\_timeoutb, PCFGQOS1\_n.rqos\_map\_timeoutr,

PCFGWQOS1\_n.wqos\_map\_timeout1 and PCFGWQOS1\_n.wqos\_map\_timeout2

- rd\_act\_idle\_gap and wr\_act\_idle\_gap to 0 and non zero values

- Different values on SCHED4.wr\_page\_exp\_cycles, SCHED4.rd\_page\_exp\_cycles

- Different values on SCHED3.wrcam\_highthresh, SCHED3.wrcam\_lowthresh

- Cover AXI Reads and Writes with QOS values resulting in Low/Variable/High/Normal Reads/Writes

Cover the performance logging signals with different values:

- perf\_op\_is\_activate

- perf\_op\_is\_rd

- perf\_op\_is\_rd\_activate

- perf\_op\_is\_rd\_or\_wr

- perf\_war\_hazard,

- perf\_visible\_window\_limit\_reached\_wr,

- perf\_visible\_window\_limit\_reached\_rd,

- perf\_rdwr\_transitions,

- perf\_raw\_hazard,

- perf\_precharge\_for\_rdwr,

- perf\_op\_is\_wr

- perf\_hpr\_xact\_when\_critical

- perf\_hpr\_req\_with\_nocredit

- perf\_lpr\_xact\_when\_critical

- perf\_lpr\_xact\_when\_nocredit

- hpr\_credit\_cnt

- lpr\_credit\_cnt

- wr\_credit\_cnt

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:7.3

### **Address Collision Handling and Write Combine Test**

**Description:**

This testcase verifies that how Subsystem handles the back to back writes with same address depending on the write combine enable and disable(TODO how to enable/disable write combine).

**Combinations to be Covered:**

Cover AXI Reads and Writes in following scenarios:

- New read colliding with queued read

- New write colliding with queued write with logic '0' and logic '1' values of OPCTRL0.dis\_wc and write ecc enable and disable

- New write colliding with queued Read

- New read colliding with queued write

- New read colliding with both read and write

- New write colliding with both read and write with logic '0' and logic '1' values of OPCTRL0.dis\_wc and write ecc enable and disable

- New RMW colliding with queued write

Cover logic '0' and '1' on signals perf\_write\_combine, perf\_write\_combine\_noecc and perf\_write\_combine and perf\_write\_combine\_wrecc, perf\_waw\_hazard, perf\_wr\_xact\_when\_critical.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:7.4, 7.5

### **DDRC Read/Write internal Port Priorities**

**Description:**

This testcase verifies the port priorities through port aging counters based on port priority registers PCFGR.rd\_port\_priority and PCFGW.wr\_port\_priority.

Also verifies the maksing the port read/write address channel from requesting to the PA depending on parmask/pawmask.

Also exercise CAM depth for both Read and Write.

Also verifies the RMW and datamask with aligned and unaligned bursts.

**Combinations to be Covered:**

- Cover the different values of :

PCFGR.rd\_port\_priority, PCFGW.wr\_port\_priority and supporting fields of PCFGR register.

SCHED0.lpr\_num\_entries (for covering credit mechanism)

SCHED0.hpr\_num\_entries

- Cover RMW with unaligned bursts when DBICTL.dm\_en=0

- Cover data lengths on AXI resulting in full and partial reads and writes (Odd and even number of bytes of length) with DBICTL.dm\_en=1

- Cover AXI Reads and Writes with QOS values resulting in Low/Variable/High/Normal Reads/Writes

- Cover signals parmask pawmask as logic '0' and '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:3.1.2, 3.3.3

## **Refresh Control and Management**

### **Refresh Using Direct Software Request of Refresh Command Test**

**Description:**

This test verifies that the Subsystem gets refresh request from software and sends Refresh Command to SRAM based on auto-refresh feature is enabled or disabled.

It also verifies that OPCTRLSTAT.rank\*\_refresh\_busy is asserted when refresh command reached to buffer size as per the table 9-1 of Controller Databook.

**Combinations to be Covered:**

- Cover different combinations of following configurations with logic '1' value of RFSHCTL0.dis\_auto\_refresh and toggle in RFSHCTL0.refresh\_update\_level:

- OPREFCTRL0.rank[0|1]\_refresh to logic '1'

- OPCTRLSTAT.rank[0|1]\_refresh\_busy as logic '0' and '1'

- RFSHMOD0.per\_bank\_refresh as logic '1' and more than 65 refresh commands from APB consecutively

- RFSHMOD0.per\_bank\_refresh as logic '0' and more than 9 refresh commands from APB consecutively

- perf\_op\_is\_crit\_ref as logic '0' and '1'

- perf\_op\_is\_refresh as logic '0' and '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.1.2

### **Per Bank Refresh Using Auto-Refresh Feature Test**

**Description:**

This test verifies the time interval between the Per bank refresh commands sent by LPDDR Subsystem depending on the configuration set on RFSHSET1MG[0|1|2] and RFSHMOD0 while using Auto Refresh Feature of the Controller. It also verifies that the Subsystem issues Speculative refresh based on RFSHSET1TMG0.refresh\_to\_x1\_x32.

**Combinations to be Covered:**

Cover different combinations of following configurations with logic '0' value of RFSHCTL0.dis\_auto\_refresh and RFSHMOD0.per\_bank\_refresh as logic '1' and toggle in RFSHCTL0.refresh\_update\_level:

- RFSHMOD0.auto\_refab\_en as logic '0' and '1'

- RFSHMOD0.per\_bank\_refresh\_opt\_en as logic '0' and '1'

- RFSHSET1TMG0.refresh\_to\_x1\_sel as logic '0' and '1'

- RFSHSET1TMG0.t\_refi\_x1\_sel as logic '0' and '1'

- RFSHMOD0.refresh\_burst as zero and different non-zero values.

- RFSHSET1TMG1.t\_rfc\_min and RFSHSET1TMG2.t\_pbr2pbr as different valid values

- RFSHSET1TMG0.refresh\_to\_x1\_x32 and RFSHSET1TMG0.t\_refi\_x1\_x32 as different valid values

- perf\_op\_is\_spec\_ref as logic '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.1.3

### **All Bank Refresh Using Auto-Refresh Feature Test**

**Description:**

This test verifies the time interval between the All bank refresh commands sent by LPDDR Subsystem depending on the configuration set on RFSHSET1MG[1|3] and RFSHMOD0 while using Auto Refresh Feature of the Controller. It also verifies that the Subsystem issues Speculative refresh based on RFSHSET1TMG0.refresh\_to\_ab\_x32.

**Combinations to be Covered:**

Cover different combinations of following configurations with logic '0' value of RFSHCTL0.dis\_auto\_refresh and RFSHMOD0.per\_bank\_refresh as logic '0' and toggle in RFSHCTL0.refresh\_update\_level:

- RFSHSET1TMG1.t\_rfc\_min\_ab as different valid values

- RFSHSET1TMG3.refresh\_to\_ab\_x32 as different valid values

- RFSHMOD0.refresh\_burst as zero and different non-zero values.

- perf\_op\_is\_spec\_ref as logic '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.1.3

### **Automatic Temperature Derating Test**

**Description:**

This test case verifies that the Subsystem is supporting Automatic Temperature Derating feature through APB Configuration Registers DERATECTL0, DERATEINT, DERATECTL5.

**Combinations to be Covered:**

Cover different combinations of following registers and associated values:

- DERATECTL0.derate\_enable as logic '0' and '1'

- DERATECTL6.derate\_mr4\_tuf\_dis as logic '0' and '1'

- different possible values of DERATEINT.mr4\_read\_interval

- DERATECTL5.derate\_temp\_limit\_intr\_en, DERATECTL5.derate\_temp\_limit\_intr\_clr and DERATECTL5.derate\_temp\_limit\_intr\_force as logic '0' and '1'

- DERATESTAT0.derate\_temp\_limit\_intr as logic '0' and '1'

- '01', '10' value for derate\_temp\_limit\_intr\_fault interrupt.

- DERATEVAL0 timings as different valid values and not equal to non-derated timing values

- MR4[4:0] as different configuration values and MR4[7] as logic '0' and '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.1.4

### **Refresh Management test**

**Description:**

This test case to verify the RFM feature is enabled by setting RFMMOD0.rfm\_en if supported by the SDRAM Based on the Programmed MR Values.

**Combinations to be Covered:**

Cover the below values of registers:

- RFMMOD0.rfm\_en as logic '1' and '0'

- RFMMOD0.rfmsbc as logic '1' and '0'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.2

## **Periodic Memory and Phy Maintenance**

### **ZQ Calibration Test**

**Description:**

This testcase verifies that the LPDDR Subsystem issues ZQCal latch command automatically at regular interval or direct from software request, depending on configuration of ZQCTL0.dis\_auto\_zq bit. It also verifies the zq\_calib\_short\_busy sets during ZQ initiate

**Combinations to be Covered:**

Cover different combinations of following configurations:

- ZQCTL0.dis\_auto\_zq as logic '0' and '1'

- ZQCTL1.zq\_reset as logic '0' and '1'

- ZQSTAT.zq\_reset\_busy as logic '0' and '1'

- ZQSET1TMG0.t\_zq\_short\_nop, ZQSET1TMG1.t\_zq\_reset\_nop and ZQSET1TMG2.t\_zq\_stop as different values

- ZQSET1TMG1.t\_zq\_short\_interval\_x1024 as different values

- ZQCTL2. dis\_srx\_zqcl as logic '0' and '1' with SR-Powerdown exit

- Cover perf\_precharge\_for\_other, perf\_op\_is\_zqstart, perf\_op\_is\_zqlatch to logic 1 when Pre-charged Issued due to ZQ Calib.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.3

### **MRR Snooping Test**

**Description:**

This testcase verifies LPDDR Subsystem schedules the MPC command and MRR commands periodically.

**Combinations to be Covered:**

Cover different combinations of following configurations:

- DQSOSCRUNTIME timing fields as different valid values

- DQSOSCCTL0.dqsosc\_interval as different valid values

- DQSOSCCTL0.dqsosc\_enable as logic '0' and '1'

- perf\_op\_is\_dqsosc\_mpc as logic '0' and '1'

- perf\_op\_is\_dqsosc\_mrr as logic '0' and '1'

- Cover perf\_precharge\_for\_other, perf\_op\_is\_tcr\_mr to logic 1 when Pre-charged Issued due to MRR.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 9.4

## **Low Power and Power Saving Features**

### **Pre-charge Power down Test**

**Description:**

This test case verifies that the Subsystem is issuing command to enter and exit Precharge Power down mode for power saving as programmed through APB Configuration Registers PWRCTL and PWRTMG.

**Combinations to be Covered:**

Cover different combinations of following registers with associated values:

- PWRCTL.powerdown\_en as logic '0' and '1'

- DFILPCFG0.dfi\_lp\_en\_pd as logic '0' and '1'

- Different timing values for PWRTMG.powerdown\_to\_x32 and DFILPTMG0.dfi\_lp\_wakeup\_pd

- An idle period without any AXI Transactions for less or greater than the configured Power Down Timing

- Self Refresh Entry and AXI Transactions during Power Down State

- perf\_op\_is\_enter\_powerdown as logic '0' and '1' for each rank

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.2.2

### **Self Refresh Test**

**Description:**

This test case verifies that the Subsystem is moving to Self-Refresh mode for power saving through APB Configuration Registers PWRCTL and DFIPHYMSTR.

**Combinations to be Covered:**

Cover different combinations of following registers with associated values:

- PWRCTL.selfref\_en as logic '0' and '1'

- PWRCTL.selfref\_sw as logic '0' and '1'

- PWRCTL.stay\_in\_selfref as logic '0' and '1'

- DFILPCFG0.dfi\_lp\_en\_sr as logic '0' and '1'

- Different timing values for PWRTMG.selfref\_to\_x32 timing and DFILPTMG0.dfi\_lp\_wakeup\_sr

- No pending reads or writes for the period PWRTMG.selfref\_to\_x32 timing

- HWLPCTL.hw\_lp\_en=1 and csysreq\_ddrc/csysack\_ddrc with cactive\_in\_ddrc=0 and 1 simultaneously with no pending reads/writes and with new Read/Write request.

- Different values of STAT.selfref\_type register (stat\_ddrc\_reg\_selfref\_type)

- STAT.selfref\_state as valid values 'h0, 'h1, 'h2, 'h3

- perf\_op\_is\_enter\_selfref and perf\_selfref\_mode as logic '0' and '1' for each rank

- Cover perf\_precharge\_for\_other as logic 1 when Pre-charged Issued due to Refresh command.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.2.3, 11.4.2

### **Deep Sleep Mode Test**

**Description:**

This test case verifies that the Subsystem is moving to Deep-Sleep mode for power saving through APB Configuration Registers PWRCTL.

**Combinations to be Covered:**

Cover different combinations of following registers with associated values:

- PWRCTL.dsm\_en as logic '0' and '1'

- DFILPCFG0.dfi\_lp\_en\_dsm as logic '0' and '1'

- Different timing values for DFILPTMG0.dfi\_lp\_wakeup\_sr

- Cover different combinations of below register signals with PWRCTL.dsm\_en=1:

PWRCTL.selfref\_sw as logic '0' and '1'

PWRCTL.selfref\_en as logic '0' and '1'

HWLPCTL.hw\_lp\_en as logic '0' and '1'

- When PWRCTL.dsm\_en=1, cover logic '0' and '1' value on DFIPHYMSTR.dfi\_phymstr\_en.

- STAT.selfref\_state as valid values 'h0, 'h4

- perf\_op\_is\_enter\_dsm as logic '0' and '1'

- Cover different combinations of below register fields for dfi\_lp\_ctrl\_wakeup and dfi\_lp\_data\_wakeup:

DFILPTMG0.dfi\_lp\_wakeup\_dsm

DFILPTMG0.dfi\_lp\_wakeup\_sr

DFILPTMG0.dfi\_lp\_wakeup\_pd

DFILPTMG1.dfi\_lp\_wakeup\_data

- Cover different combinations of DFILPTMG1.dfi\_tlp\_resp for dfi\_lp\_ctrl\_req and dfi\_lp\_data\_req.

- Cover logic '1' and '0' value on DFIERRINTRPTCFG.dfi\_error\_intr\_force, DFIERRINTRPTCFG.dfi\_error\_intr\_clr and DFIERRINTRPTCFG.dfi\_error\_intr\_en, DFIERRORSTAT.dfi\_error\_intr.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.2.4

### **Hardware Fast Frequency Change (HWFFC) Test**

**Description:**

This test case verifies that the Subsystem is supporting clock frequency change without Software intervention through APB Configuration Register HWFFCCTL.

**Combinations to be Covered:**

- Cover different combinations on HWFFCCTL.hwffc\_mode, HWFFCCTL.hwffc\_en and ZQCTL2.dis\_srx\_zqcl\_hwffc

- Cover different values of HWFFC\_MRWBUF\_CTRL\_0 register fields for MRW Buffer Write/Read.

- Cover logic '0' and '1' value of below signals when csysreq\_ddrc=0 and

csysmode\_ddrc=1:

csysdiscamdrain\_ddrc

csysfsp\_ddrc

csysack\_ddrc

cactive\_ddrc

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.6

### **LPDDR5 masked write Test**

**Description:**

This test case verifies that the Subsystem is masks write data received on DQ inputs through APB Configuration Register DFIMISC and DBICTL.

**Combinations to be Covered:**

- Cover both logic values '1' and '0' on DFIMISC.IP\_optimized\_write.

- Cover different combinations of below signals with DFIMISC.IP\_optimized\_write=1:

DBICTL.wr\_dbi\_en=1

DBICTL.dm\_en=1

DFIMISC.phy\_dbi\_mode=0

Cover below performance logging signals-

- perf\_op\_is\_mwr

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.7

### **Fast Frequency Change Test**

**Description:**

This test case verifies that the Subsystem supports Fast Frequency Change, using up to four sets of timing registers and by following the sequence steps mentioned in DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section- 11.4.1.3

**Combinations to be Covered:**

- Cover below values for APB Write on MSTR2.target\_frequency:

0 - Frequency 0/Normal

1 - Frequency 1/FREQ1

2 - Frequency 2/FREQ2

3 - Frequency 3/FREQ3

- Cover different values for APB Read on DFIMISC.dfi\_frequency.

- Cover different values of Timing Registers for different frequency sets.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.5, 14.4.1.3

### **DFI DRAM CLK DISABLE Test**

**Description:**

This test case verifies that the Subsystem is disabling DFI DRAM CLK for power saving through APB Configuration Registers PWRCTL in specific operating modes.

**Combinations to be Covered:**

- Cover Different timing values of following registers in Deep Sleep mode, Self-Refresh Power down mode, Power-Down mode and Normal Mode with PWRCTL.en\_dfi\_dram\_clk\_disable=1:

- DFITMG0.dfi\_t\_ctrl\_delay

- DRAMSET1TMG5.t\_cksre

- DFITMG1.dfi\_t\_dram\_clk\_disable

- DFITMG1.dfi\_t\_dram\_clk\_enable

- DRAMSET1TMG5.t\_cksrx

- Cover logic '0' -> '1' and '1' -> '0' transition on Bump Signals BP\_CK0\_T, BP\_CK0\_C, BP\_CK1\_T and BP\_CK1\_C.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:11.2.5

dwc\_lpddr5x\_phy\_pub\_databook\_latest.pdf Section: 4.1

### **Self Refresh through PHY Master Test**

**Description:**

This test case verifies that the Subsystem is moving to Self-Refresh mode because of DFI PHY MASTER INTERFACE through APB Configuration Registers DFIPHYMSTR, PPTTrainSetup\_pX, MasUpdGoodCtr, MasUpdFailCtr, BlockDfiInterface and DfiMode.

**Combinations to be Covered:**

Cover following when DFIPHYMSTR.dfi\_phymstr\_en is logic '1', PWRCTL.selfref\_en as logic '0' and PWRCTL.selfref\_sw = 0:

- STAT.selfref\_state from logic '0' -> '1' and '1' -> '0'

- APB Configuration register: STAT as following transitions:

- IDLE → SR → IDLE

- SRPD → SR → SRPD

- different values on PPTTrainSetup\_pX.PhyMstrMaxReqToAck, PPTTrainSetup\_pX.PhyMstrTrainInterval, MasUpdGoodCtr and MasUpdFailCtr.

Cover logic '0' and '1' value on BlockDfiInterface.BlockDfiInterfaceEn, DfiMode.Dfi0Enable and DfiMode.Dfi1Enable.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section: 4.1.11.2

dwc\_lpddr5x\_phy\_pub\_databook\_latest.pdf Section: 10.9

## **Error Correction and RAS**

### **Link ECC Test**

**Description:**

This test case verifies that the Subsystem is supporting Link ECC feature as programmed through APB Configuration Registers LNKECCCTL0, LNKECCINDEX, LNKECCERRCNT0, LNKECCPOISONCTL0.

**Combinations to be Covered:**

Cover different combinations of following registers and associated values with AXI Write and DDR Read Response Data with correct and incorrect link ECC:

- LNKECCCTL0.wr/rd\_link\_ecc\_enable as logic '0' and '1'

- LNKECCINDEX, LNKECCERRCNT0 as different values

- LNKECCERRSTAT.rd\_link\_ecc\_corr\_err\_int and LNKECCERRSTAT.rd\_link\_ecc\_uncorr\_err\_int as logic '0' and '1'

- LNKECCCTL1 fields as logic '0' and '1'

- LNKECCPOISONCTL0 fields as different values to inject Link ECC Errors

- LNKECCPOISONSTAT.linkecc\_poison\_complete as logic '0' and '1'

- SLVERR response for Read Transactions with Link ECC Error

- ECCCSYN0 and ECCUSYN0 as correctable and uncorrectable data patterns

- dis\_regs\_ecc\_syndrome as logic '0' and '1'

- logic '0' and '1' for rd\_linkecc\_corr\_err\_intr, rd\_linkecc\_uncorr\_err\_intr and '01', '10' value for rd\_linkecc\_corr\_err\_intr\_fault, rd\_linkecc\_uncorr\_err\_intr\_fault interrupt.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:12.4

### **LPDDR5 Post Package Repair Test**

**Description:**

This test case verifies that the Subsystem supports a method of Fail Row address repair, PPR(Post Package Repair) through APB Configuration Registers.

Note : Perform PPR Sequence described in Table 12-7 of DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf to verify this test and PPR Feature

**Combinations to be Covered:**

Cover different combination of register values:

- MRCTRL0.ppr\_en, MRCTRL0.mr\_wr, MRCTRL0.ppr\_pgmpst\_en and MRCTRL0.ppr\_done as logic '0' and '1'

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:12.5

### **Inline ECC Test**

**Description:**

This test case verifies that the Subsystem is supporting Inline ECC feature through APB Configuration Registers ECCCFG0, ECCCFG1.

**Combinations to be Covered:**

Cover below different combinations in different ranges of data:

- Cover all four logical combinations of ECCCFG0.ecc\_region\_map\_granu.

- Cover different ranges of ECCCFG0.ecc\_region\_map

- Cover both logic values '1' and '0' for ECCCFG0.ecc\_region\_remap\_en and ECCCFG0.ecc\_region\_map\_other

- Cover both logic values '1' and '0' for ECCCFG1.ecc\_region\_parity\_lock and ECCCFG1.ecc\_region\_waste\_lock

- Cover both logic values '1' and '0' for ECCCFG0.ecc\_ap\_en, ECCCFG1.med\_ecc\_en and ECCCFG1.ecc\_ap\_mode

- Cover SLVERR response while driving transactions accessing locked regions over AXI

- Cover different wrecc\_credit\_cnt values

- Cover different values on dbg\_dfi\_ie\_cmd\_type

- Cover logic '0' and '1' for ecc\_ap\_err\_intr, ecc\_corrected\_err\_intr, ecc\_uncorrected\_err\_intr and '01', '10' value for ecc\_ap\_err\_intr\_fault, ecc\_corrected\_err\_intr\_fault, ecc\_uncorrected\_err\_intr\_fault interrupt, perf\_ie\_blk\_hazard.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:13.1

### **Scrubber Status Test**

**Description:**

This test case verifies that the Subsystem supports scrubber commands for Inline ECC through APB Configuration Registers SBRCTL, SBRSTART1, SBRSTART0, SBRRANGE0, SBRRANGE1, SBRSTART0DCH1, SBRSTART1DCH1, SBRRANGE0DCH1, SBRRANGE1DCH1.

**Combinations to be Covered:**

- Cover default values of SBR logic on sbr\_resetn = 0.

- Cover different values of SBRCTL.scrub\_interval such as below:

SBRCTL.scrub\_interval = 0

SBRCTL.scrub\_interval = PWRTMG.powerdown\_to\_x32

SBRCTL.scrub\_interval = PWRTMG.selfref\_to\_x32

SBRCTL.scrub\_interval = different values other than PWRTMG.selfref\_to\_x32 and PWRTMG.powerdown\_to\_x32.

- Cover logic '0' and '1' value of SBRCTL.scrub\_en.

- Cover different values of following register fields: SBRSTART1.sbr\_address\_start\_mask\_1, SBRSTART0.sbr\_address\_start\_mask\_0, SBRRANGE0.sbr\_address\_range\_mask\_0, SBRRANGE1.sbr\_address\_range\_mask\_1.

- Cover Non-zero values of SBRCTL.scrub\_interval when SBRSTAT.scrub\_busy =1 and SBRSTAT.scrub\_done = 0.

- Cover below combinations when SBRCTL.scrub\_interval = 0:

For read, SBRSTAT.scrub\_busy =1 and SBRSTAT.scrub\_done = 1

For write, SBRSTAT.scrub\_busy =0 and SBRSTAT.scrub\_done = 1

- Cover logic '1' and '0' value of SBRCTL.scrub\_during\_lowpower during below situations:

PWRCTL.powerdown\_en=1

PWRCTL.selfref\_en=1

PWRCTL.selfref\_sw=1

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:13.2

## **DFI Updates**

### **DFI Updates Mode Test**

**Description:**

This test case verifies that the controller and PHY perform regular DFI updates as per the different configurations.

**Combinations to be Covered:**

- Cover logic '1' and '0' value for DFIUPD0.dis\_auto\_ctrlupd when DDRCTL is idle.

- Cover logic '1' and '0' value for OPCTRLCMD.ctrlupd

- Cover logic '1' and '0' value for OPCTRLSTAT.ctrlupd\_busy

- Cover logic '1' and '0' value for DFIUPD0.dfi\_phyupd\_en.

- Cover different values for DFITMG0.dfi\_t\_ctrl\_delay.

- Cover different configurations of DFIUPDTMG[0|1|2|3].

Note: Configure DFI Constraints while testing.

**Reference Information:**

DWC\_ddrctl\_lpddr54\_lpddr5x\_databook.pdf Section:4.2, 4.3