

SHAILAJA ALLAM

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**Profile Summary**

I am currently working as a student trainee with 5+ months of hands-on experience at **Maven Silicon Pvt. Ltd, Bangalore**

(Advanced VLSI frontend Design and Verification course) in domains like **Digital Design, Verilog, and System Verilog** )

Looking for an **entry-level position** in the Core Front-end domain **(RTL / ASIC Design, Design and Verification, FPGA & DFT)** where I can utilize my extensive knowledge about the subjects, gained during my Training and Professional Courses.

# Professional Training \_

## Maven Silicon Pvt Ltd, Bangalore (Advanced Design & Verification) Jan 2022 – Present

*[Digital Design, STA, Verilog, FPGA Design flow, CMOS Design, System Verilog]*

* ***Digital Design*** (Boolean Algebra / Combinational & Sequential Circuits / FSM Design / FIFOs & Memory / CDC, Clock Domain Crossing)
* ***FPGA Fundamentals*** (CLBs, LUTs, I/O Blocks / Design flow / RTL Schematics)
* ***STA*** (DTA / Timing paths / Path sensitization / False Paths / Timing Violations & Fixing Techniques)
* ***Verilog HDL*** (Data types / Operators / Continuous & Procedural Assignments / BA & NBA / Tasks & Functions / FSM Coding / Code Coverage / Stratified Event Queue)
* ***System Verilog HDVL*** (Data types / Interfaces & Clocking blocks / Inheritance / Object Oriented Programming / Polymorphism / Randomization / Threads / Functional Coverage / Assertions)

# Academic Qualifications\_ \_

## Siddhartha Institute of Engineering and Technology JNTU-H University August 2016 – July 2020

Bachelor of Technology in Electronics and communication Engineering **CGPA – 8.02**

## Vikas Junior College May 2016

Intermediate **Percentage – 96.3**

## Zilla Parishat High School May 2014

S.S.C **CGPA – 9.0**

# Front – End VLSI Skills \_ \_

* ***Programming Languages:*** Verilog HDL, System Verilog HVL
* ***Verification Technologies:*** System Verilog (Coverage + Assertions)
* ***IDEs:*** Vivado Design Suite, Modelsim, INTEL Quartus prime lite edition, Mentor Graphics Questasim, EDA Playground
* ***Operating Systems:*** Windows, Linux

**Front - End VLSI Projects**

## Router 1X3 – RTL Design and Verification

HDL: Verilog

EDA Tools: Modelsim, Quartus Prime and Questasim

Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Responsibilities:

* + Architected the block level structure for the design.
  + Implemented RTL using Verilog HDL.
  + Verified the RTL model using Verilog.
  + Generated functional and code coverage for the RTL verification sign-off.
  + Synthesized the design.

# BTech Thesis Projects \_

## An Intelligent IOT based security system for server rooms in industries

EDA Tool: Embedded C, MP lab

Microcontroller: PIC16F877A

Description: The main concept of this project is to provide security for server rooms with the help of reduce IOT technology ,Thus we can decrease the human power and increase efficiency, we will get an alert before any incident occurs.

Responsibilities:

* + Architected the block level structure for the design.
  + Design the layout of the PCB on diptrace.
  + Placed all the components on the PCB and solder it after etching and drilling.
  + Tested the functionality of the project using BLYNK application.

# Personality Traits

* + Critical Thinking
  + Team Player
  + Adaptability
  + Positive Approach

# Certifications & Extra – Curricular Activities \_ \_

* + I have participated in Hackathon program at Siddhartha institute of engineering and technology
  + I have participated in paper presentation at Nishitha college of engineering and technology
  + I have participated in Technical Quiz at JNTUH University
  + Best Student Award at Intermediate level
  + I have Participated and won prizes in Essay writing and sports competition in school level
  + I have Participated in science fair competition in school level

# Leisure Time Activities \_

* + - Cooking
    - Playing Chess
    - Travelling
    - Listening Songs

# Additional Information \_

* + - ***Date of Birth:*** March,05, 1999
    - ***Languages:*** English, Telugu

# Declaration \_ \_

I hereby declare that all the information contained in this resume is in accordance with facts or truths to my sense. I take full authority for the correctness of the written information

**City:** Mancherial

## Date: SHAILAJA ALLAM