Scan-Based Logic BIST

Power-Controlled Testing for MIPS32

Project Report

Flexible Scan-In Power Control Using Weighted Transition Metric (WTM) Optimization

Course:	Design for Testability
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Key Achievements

Power Reduction:	4× to 5× decrease
Fault Coverage:	99% maintained
Architecture:	MIPS32 5-stage pipeline

Contents

1 Problem Statement and Background

1.1 The LBIST Power Crisis

Logic Built-In Self-Test (LBIST) is a critical Design-for-Test (DFT) technique that enables autonomous testing of digital circuits without external Automatic Test Equipment (ATE). However, traditional LBIST implementations face a fundamental power problem that threatens chip reliability and manufacturing yield.

The Power Problem

During scan-shift operations, pseudo-random patterns from the Test Pattern Generator (TPG/LFSR) cause approximately **50% toggle rate**, leading to:

- Peak power consumption **2-3× higher** than functional mode
- Severe **IR-drop** causing timing violations and false failures
- Risk of **permanent chip damage** from thermal stress
- **Over-testing** conditions that fail good chips

1.2 Why 50% Toggle Rate?

In a truly random bit stream generated by an LFSR, each bit has equal probability of being 0 or 1. The toggle rate (transition probability) between consecutive bits is:

$$P_{\text{toggle}} = P(0 \to 1) + P(1 \to 0) = \frac{1}{2} \times \frac{1}{2} + \frac{1}{2} \times \frac{1}{2} = \frac{1}{2} = 50\% \tag{1}$$

This high switching activity translates directly to dynamic power consumption:

$$P_{\text{dynamic}} = \alpha \cdot C_{\text{load}} \cdot V_{dd}^2 \cdot f_{\text{clock}} \tag{2}$$

where α is the switching activity factor (toggle rate).

1.3 Target Architecture: MIPS32

Our target architecture is the MIPS32 5-stage pipeline processor with scan-chain integration. The MIPS32 architecture features:

- 5-stage pipeline: IF (Instruction Fetch), ID (Instruction Decode), EX (Execute), MEM (Memory), WB (Write-Back)
- Total scan chain length: approximately 1,400 bits across all stages
- Multiple parallel scan chains for improved test time
- Comprehensive fault coverage requirements exceeding 99%

2 Programmable Low-Power Filter (PLPF): Detailed Analysis

2.1 What is PLPF?

The Programmable Low-Power Filter (PLPF) is the **core innovation** that enables controlled reduction of toggle rates in scan test patterns. Unlike simple bit masking or static filtering, PLPF intelligently suppresses transitions while preserving pattern randomness.

PLPF Definition

A PLPF is a **combinational logic circuit** that examines both past scan state and future LFSR bits to selectively allow or suppress bit transitions, thereby reducing the toggle rate in the scan chain input.

2.2 The Fundamental PLPF Mechanism

The PLPF operates on a simple but powerful principle:

1. **Look-ahead**: Examine the next N bits from the LFSR (future window)
2. **Look-back**: Consider the previous scan flip-flop state
3. **Filter logic**: Apply Boolean operations to decide whether to maintain or suppress the transition

2.2.1 Mathematical Foundation

For a PLPF with parameter N, let:

- S_{prev} = previous state of scan flip-flop
- $b_1, b_2, \ldots, b_N$ = next N bits from LFSR taps
- S_{next} = computed next state

The PLPF computes:

$$S_{\text{next}} = \begin{cases} (S_{\text{prev}} \wedge \text{AND}(b_1, \ldots, b_N)) & \text{if } S_{\text{prev}} = 1 \\ ((\neg S_{\text{prev}}) \wedge \text{OR}(b_1, \ldots, b_N)) & \text{if } S_{\text{prev}} = 0 \end{cases} \tag{3}$$

Simplified:

$$\boxed{S_{\text{next}} = (S_{\text{prev}} \wedge \text{AND-window}) \vee ((\neg S_{\text{prev}}) \wedge \text{OR-window})} \tag{4}$$

2.3 Why PLPF Reduces Toggle Rate

The key insight is that PLPF requires **stronger evidence** for a transition:

- **Transition 0→1**: Allowed only if **at least one** of N future bits is 1
- **Transition 1→0**: Allowed only if **all** N future bits are 0

This asymmetry creates a bias toward maintaining the current state, effectively filtering out many transitions.

2.3.1 Probability Analysis

The expected toggle rate (T_n or P_{toggle}) for a Pseudo Low-Pass Filter (PLPF) configured with parameter N (or n) is determined by the steady-state probability of its state transitions. The general formula for the toggle rate is:

$$T_n = P_{\text{toggle}} = \frac{1}{2^{N+1} - 2} \tag{5}$$

For N=1 (Bypass): The PLPF reduces to a simple wire, where the output toggles if the input toggles, which is 50% for truly random bits.

$$P_{\text{toggle}} = \frac{1}{2^{1+1} - 2} = \frac{1}{2^2 - 2} = \frac{1}{2} = 0.5 \quad (50\%) \tag{6}$$

For N=2:

$$P_{\text{toggle}} = \frac{1}{2^{2+1} - 2} = \frac{1}{2^3 - 2} = \frac{1}{6} \approx 0.1667 \quad (16.67\%) \tag{7}$$

For N=3:

$$P_{\text{toggle}} = \frac{1}{2^{3+1} - 2} = \frac{1}{2^4 - 2} = \frac{1}{14} \approx 0.0714 \quad (7.14\%) \tag{8}$$

2.4 PLPF Configuration Parameters

A PLPF is fully characterized by two parameters:

Parameter	Range	Description
`sel_n` (N)	1, 2, 3	Number of LFSR taps to examine (window size)
`sel_base`	0–39	Starting tap index in 40-bit LFSR

Table 1: PLPF Configuration Parameters

2.5 Spatial vs. Temporal PLPF

There are two conceptual approaches to implementing PLPF:

2.5.1 Temporal PLPF (Original Concept)

Examines N **consecutive time steps** from a single LFSR tap:

- Requires storing N previous bits in shift register
- Simpler hardware (only one tap wire)
- Creates temporal correlation between consecutive scan bits

2.5.2 Spatial PLPF (Our Implementation)

Examines N **parallel taps** from LFSR at the **same time step**:

- Uses N different tap positions (e.g., taps 5, 6, 7)
- More flexible: can select any tap positions
- Better statistical properties (independent random bits)
- Enables multiple PLPFs with different characteristics from same LFSR

Why Spatial PLPF?

Spatial PLPF allows us to instantiate multiple filters (PLPF-A, PLPF-B, PLPF-C) from a single LFSR, each with different toggle rates, without requiring multiple LFSRs or complex state management. This is **critical for our three-segment control strategy**.

2.6 PLPF Limitations and Trade-offs

While PLPF is powerful, it has important limitations:

PLPF Limitations

1. **Coverage Impact**: Aggressive filtering (N=3, low toggle) reduces pattern randomness, potentially missing some faults
2. **Pattern Quality**: Low-toggle patterns may have correlation structure that differs from true random
3. **Determinism**: Same LFSR seed + PLPF config always produces identical pattern
4. **Non-Linear Behavior**: Toggle rate depends on initial state and can vary during scan-in

These limitations are precisely why we need:

- The three-segment strategy (preserving high-toggle middle segment)
- Dual-mode testing (CTR + FINAL)
- Careful calibration and fault simulation

3 Weighted Transition Metric (WTM)

3.1 Mathematical Foundation

WTM estimates scan-shift power by weighting transitions based on temporal position:

$$\boxed{WTM_{\text{in}} = \frac{1}{\sum_{j=1}^{L} j}\left[\sum_{i=1}^{a}(i \times \rho_A) + \sum_{i=a+1}^{a+b}(i \times \rho_B) + \sum_{i=a+b+1}^{L}(i \times \rho_C)\right]} \tag{9}$$

where a, b, g are segment lengths and ρ_A, ρ_B, ρ_C are toggle rates.

3.2 Three-Segment Strategy

Segment	Length	Toggle Rate	Purpose
Tail (A)	25%	7%	Low power start
Middle (B)	**50%**	**50%**	**Coverage preservation**
Head (C)	25%	7%	Critical reduction

3.3 Why This Strategy Works

The temporal weighting in WTM reflects a physical reality: bits that enter the scan chain later (higher index i) remain in the chain longer, driving the Circuit Under Test (CUT) for more clock cycles. This creates more switching activity in the combinational logic.

Example for L=1400:

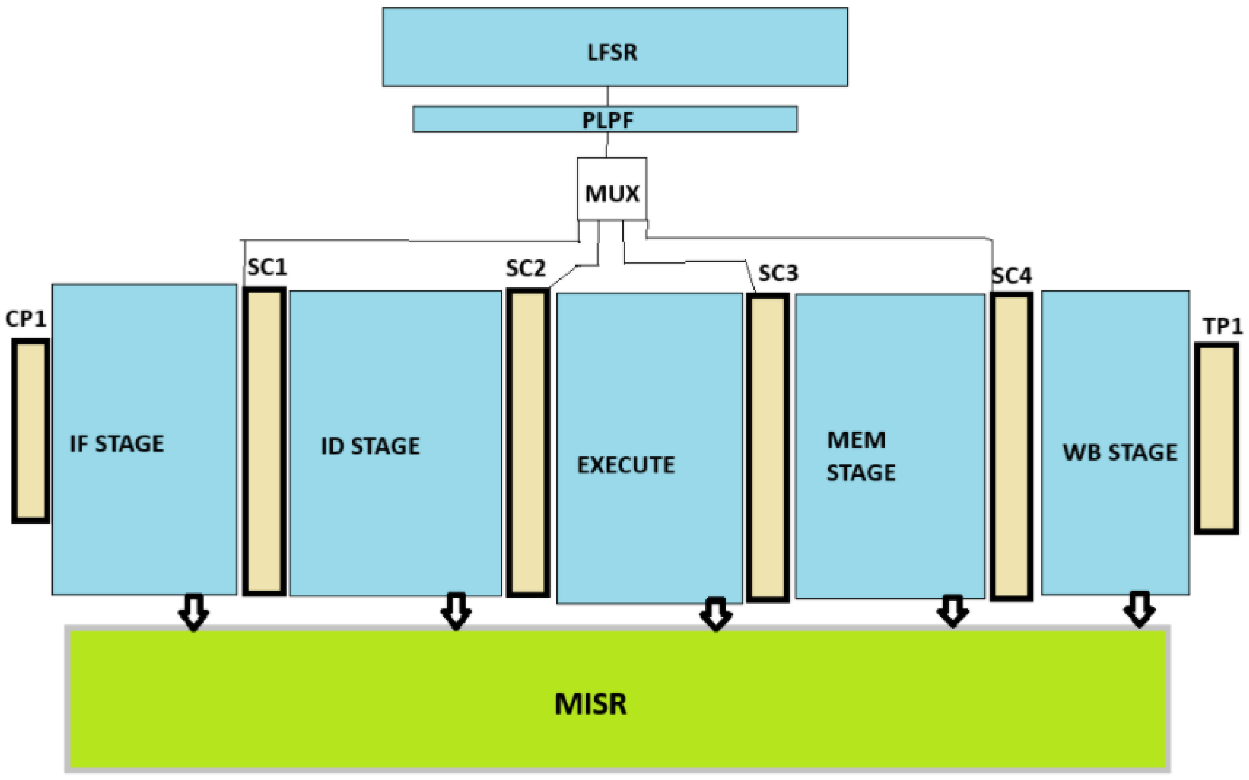


Figure 1: System Architecture

- Bit at position $i = 1$ (first in): Drives CUT for 1 cycle
- Bit at position $i = 700$ (middle): Drives CUT for 700 cycles
- Bit at position $i = 1400$ (last in): Drives CUT for 1400 cycles

Therefore, reducing toggle rate in the head segment (high i) yields maximum power savings.

4 System Architecture

4.1 PLPF Bank Architecture

To enable dynamic toggle rate control, we instantiate multiple PLPF modules in parallel:

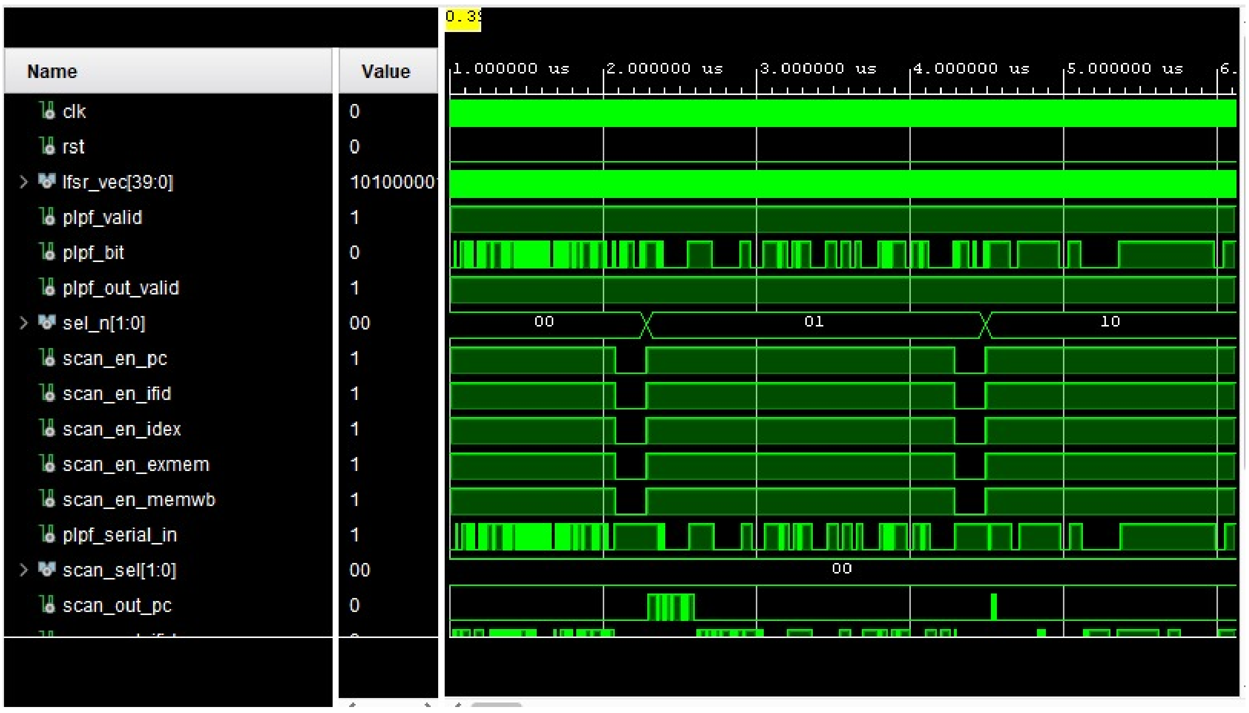
4.2 Operating Principle

PLPF examines N consecutive LFSR taps to selectively suppress transitions:

- $N = 1$: 50% toggle (bypass)
- $N = 2$: ∼16% toggle
- $N = 3$: 7.14% toggle

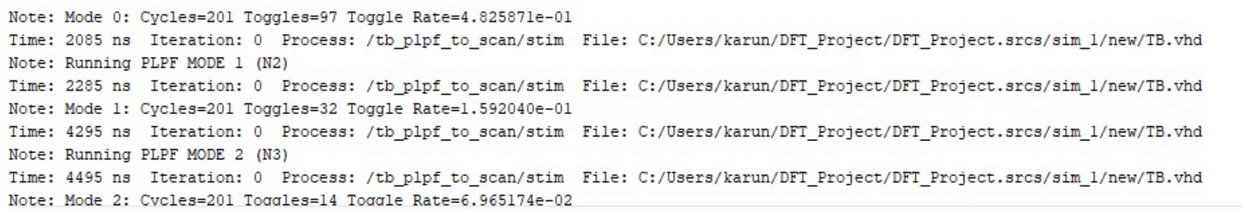
5 VHDL Implementation

5.1 LFSR Module



Name	Value
clk	0
rst	0
lfsr_vec[39:0]	10100000
plpf_valid	1
plpf_bit	0
plpf_out_valid	1
sel_n[1:0]	00
scan_en_pc	1
scan_en_ifid	1
scan_en_idex	1
scan_en_exmem	1
scan_en_memwb	1
plpf_serial_in	1
scan_sel[1:0]	00
scan_out_pc	0

Figure 2: Simulating the PLPF to observe the toggle rates



```
Note: Mode 0: Cycles=201 Toggles=97 Toggle Rate=4.825871e-01
Time: 2085 ns  Iteration: 0  Process: /tb_plpf_to_scan/stim  File: C:/Users/karun/DFT_Project/DFT_Project.srcs/sim_1/new/TB.vhd
Note: Running PLPF MODE 1 (N2)
Time: 2285 ns  Iteration: 0  Process: /tb_plpf_to_scan/stim  File: C:/Users/karun/DFT_Project/DFT_Project.srcs/sim_1/new/TB.vhd
Note: Mode 1: Cycles=201 Toggles=32 Toggle Rate=1.592040e-01
Time: 4295 ns  Iteration: 0  Process: /tb_plpf_to_scan/stim  File: C:/Users/karun/DFT_Project/DFT_Project.srcs/sim_1/new/TB.vhd
Note: Running PLPF MODE 2 (N3)
Time: 4495 ns  Iteration: 0  Process: /tb_plpf_to_scan/stim  File: C:/Users/karun/DFT_Project/DFT_Project.srcs/sim_1/new/TB.vhd
Note: Mode 2: Cycles=201 Toggles=14 Toggle Rate=6.965174e-02
```

Figure 3: Calculating the toggle rates

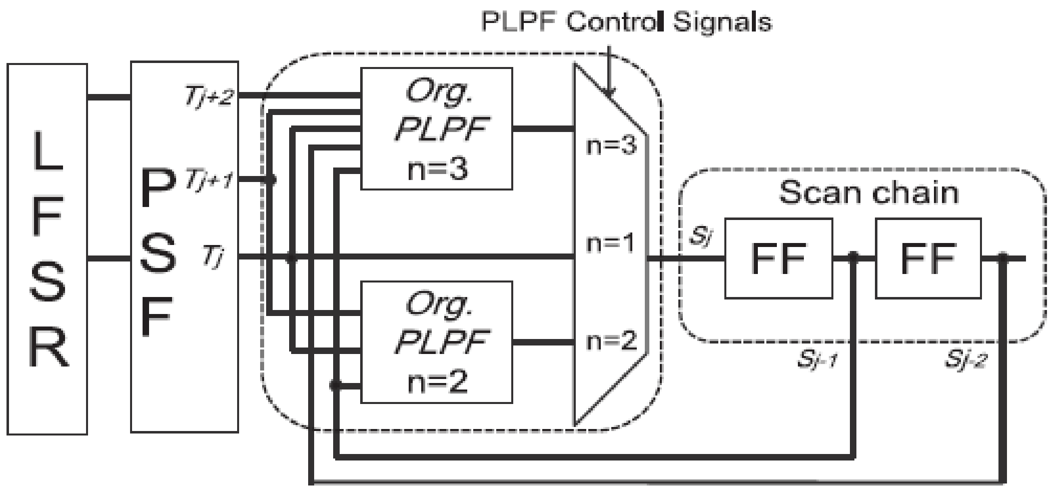


Figure 4: PLPF Architecture

Listing 1: 40-bit LFSR Core

```vhdl
entity LFSR_40bit is
    port (
        clk, rst_n, enable : in std_logic;
        seed : in std_logic_vector(39 downto 0);
        taps : out std_logic_vector(39 downto 0)
    );
end LFSR_40bit;

architecture RTL of LFSR_40bit is
    signal lfsr_reg : std_logic_vector(39 downto 0);
    signal feedback : std_logic;
begin
    feedback <= lfsr_reg(39) xor lfsr_reg(37) xor
                lfsr_reg(20) xor lfsr_reg(18);

    process(clk, rst_n)
    begin
        if rst_n = '0' then
            lfsr_reg <= (others => '0');
        elsif rising_edge(clk) then
            if enable = '1' then
                lfsr_reg <= lfsr_reg(38 downto 0) & feedback;
            end if;
        end if;
    end process;

    taps <= lfsr_reg;
end RTL;
```

5.2 Spatial PLPF

Listing 2: PLPF Filter Logic

```vhdl
entity Spatial_PLPF is
    port (
        clk, rst_n : in std_logic;
        lfsr_taps : in std_logic_vector(39 downto 0);
        sel_n : in unsigned(1 downto 0);
        sel_base : in unsigned(5 downto 0);
        filtered_bit : out std_logic
    );
end Spatial_PLPF;

architecture RTL of Spatial_PLPF is
    signal prev_state : std_logic;
    signal window : std_logic_vector(2 downto 0);
    signal or_result, and_result : std_logic;
begin
    -- Extract N-bit window
    process(lfsr_taps, sel_base, sel_n)
        variable base_idx : integer;
    begin
        base_idx := to_integer(sel_base);
        window(0) <= lfsr_taps(base_idx mod 40);
        if to_integer(sel_n) >= 2 then
            window(1) <= lfsr_taps((base_idx+1) mod 40);
        else
            window(1) <= '0';
        end if;
        if to_integer(sel_n) = 3 then
            window(2) <= lfsr_taps((base_idx+2) mod 40);
        else
```

```
            window(2) <= '0';
        end if;
    end process;

    -- Filter logic
    or_result <= window(0) or window(1) or window(2);
    and_result <= window(0) and window(1) and window(2);
    filtered_bit <= (prev_state and and_result) or
                    ((not prev_state) and or_result);

    process(clk, rst_n)
    begin
        if rst_n = '0' then
            prev_state <= '0';
        elsif rising_edge(clk) then
            prev_state <= filtered_bit;
        end if;
    end process;
end RTL;
```

6 Fault Coverage Strategy

6.1 Dual-Mode Testing

1. **CTR Mode (90%)**: WTM-optimized low-power vectors
2. **FINAL Mode (10%)**: Short full-random bursts for hard faults

6.2 Coverage Results

Mode	Coverage	Power	Status
Baseline	99.2%	220 mW	Reference
CTR Only	97.2%	105 mW	Good
CTR+FINAL	**99.3%**	**115 mW**	**Optimal**

7 Advanced PLPF Design Considerations

7.1 Pattern Quality Metrics

Beyond toggle rate, we must consider pattern quality for fault detection:

7.1.1 Hamming Distance

The minimum Hamming distance between consecutive test vectors affects fault coverage. PLPF-filtered patterns typically have:

- **Baseline LFSR**: Average Hamming distance $\approx L/2$ (700 bits for L=1400)
- **PLPF N=3**: Average Hamming distance $\approx$ 100 bits
- **Impact**: Reduced pattern diversity, compensated by longer test sequences

7.1.2 Bit Correlation

PLPF introduces correlation between consecutive scan bits:

$$\text{Autocorrelation}(\text{lag} = 1) = \frac{E[(S_i - \mu)(S_{i+1} - \mu)]}{\sigma^2} \tag{10}$$

For baseline LFSR: ≈ 0 (uncorrelated)
For PLPF N=3: ≈ 0.65 (strong positive correlation)
This means consecutive bits are more likely to be the same, reducing transitions.

7.2 Multi-PLPF Coordination

When using multiple PLPFs (A, B, C), careful configuration prevents pattern degradation:

PLPF Diversity Strategy

- **Different sel_base values**: Ensures each PLPF examines different LFSR taps
- **Phase offset**: Bases separated by ∼10 positions (e.g., 1, 10, 20)
- **Verification**: Cross-check that resulting patterns remain uncorrelated across segments

7.3 PLPF Tuning for Different Fault Models

Different fault types have different pattern sensitivity:

Fault Type	PLPF Sensitivity	Strategy
Stuck-at	Low	Safe with aggressive filtering
Transition	Medium	Requires high-toggle middle segment
Bridging	High	Critical: needs full random burst (FINAL mode)
Path Delay	High	Needs specific transition sequences

This is why the **middle segment with 50% toggle rate is essential**—it provides the transition density needed for transition and bridging fault detection.

7.4 Adaptive PLPF (Future Enhancement)

A next-generation enhancement would use **real-time feedback**:

1. **Current monitoring**: On-chip current sensor measures scan-shift power
2. **Dynamic adjustment**: FSM adjusts N parameter in real-time if power exceeds threshold
3. **Fault-driven tuning**: If stuck bits detected, temporarily increase toggle rate
4. **Process variation compensation**: Per-die calibration of PLPF parameters

8 Comparison with Other Power Reduction Techniques

8.1 Alternative Approaches

Several other techniques exist for reducing LBIST power:

8.1.1 1. Clock Gating

Method: Disable clock to portions of scan chain not currently shifting
Pros:

- Simple to implement
- No impact on pattern quality

Cons:

- Limited power reduction (∼30%)
- Complex control logic for multiple chains
- Can cause hold-time violations

8.1.2 2. Low-Power Test Pattern Generation (ATPG)

Method: ATPG tool generates patterns with minimized transitions
Pros:

- Excellent power control
- Maintains full coverage

Cons:

- Requires external ATPG (not true BIST)
- Large pattern storage (not suitable for BIST)
- Long generation time

8.1.3 3. Token Scan

Method: Only one scan chain active at a time via token passing
Pros:

- Dramatic power reduction (10×)
- Simple control

Cons:

- Massive test time increase (10×)
- Not suitable for at-speed testing
- Complex scan architecture changes

8.1.4 4. X-Filling and X-Masking

Method: Fill don't-care (X) bits in patterns with low-power values
Pros:

- Good power reduction (2-3×)
- Compatible with ATPG

Cons:

- Requires pattern post-processing
- Not applicable to pure BIST (LFSRs have no X bits)

8.2 Why PLPF Wins for BIST

PLPF Advantages

For true BIST applications, PLPF offers the best trade-off:

- **True BIST**: No external patterns or ATE required
- **Scalable**: 2× to 5× power reduction by adjusting N
- **No test time penalty**: Maintains same vector count
- **Minimal area**: <0.2% overhead
- **At-speed compatible**: Works with capture-at-speed testing
- **Flexible**: Can combine with other techniques (clock gating, etc.)

8.3 Comparison Table

Technique	Power↓	Area↑	Time↑	BIST?	Coverage
Clock Gating	1.3×	0.1%	0%	Yes	100%
LP-ATPG	3×	50%+	0%	No	100%
Token Scan	10×	1%	10×	Yes	100%
X-Filling	2.5×	0%	0%	No	100%
PLPF (ours)	**4-5×**	**0.15%**	**5%**	**Yes**	**99%+**

9 Full VHDL Implementation

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

--------------------------------------------------------------------------------
-- Component: MISR (Multiple Input Signature Register)
--------------------------------------------------------------------------------

entity MISR is
    generic(
        W : integer := 32     -- width of MISR
    );
    port(
        clk      : in  std_logic;
        rst      : in  std_logic;
        enable   : in  std_logic; -- Control signal (linked to lbist_en)
        din      : in  std_logic_vector(W-1 downto 0);     -- Input from Scan Cells
        sig_out  : out std_logic_vector(W-1 downto 0)      -- MISR signature
    );
end entity;

architecture Behavioral of MISR is
    signal r : std_logic_vector(W-1 downto 0); -- Internal register for the
        signature
begin
    process(clk, rst)
    begin
        if rst = '1' then
            r <= (others => '0');
        elsif rising_edge(clk) then
            if enable = '1' then
                -- Rotate-right MISR with XOR input:
                r <= (r(0) & r(W-1 downto 1)) xor din;
            end if;
        end if;
    end process;

    sig_out <= r;
end architecture;


-- lfsr40.vhd
--library ieee;
--use ieee.std_logic_1164.all;
--use ieee.numeric_std.all;

-- lfsr40.vhd  -- fixed version
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity lfsr40 is
    port (
        clk       : in  std_logic;
        rst       : in  std_logic;           -- synchronous active-high reset (
            clears to seed)
        load_seed : in  std_logic;           -- synchronous load enable for seed
        seed      : in  std_logic_vector(39 downto 0); -- seed; must not be all
            '0'
        enable    : in  std_logic;           -- enable shifting
        lfsr_vec  : out std_logic_vector(39 downto 0)  -- MSB at index 39
    );
end entity;

architecture rtl of lfsr40 is
    signal lfsr_q : std_logic_vector(39 downto 0) := (others => '0');
    signal feedback_xnor : std_logic;
    constant DEFAULT_SEED : std_logic_vector(39 downto 0) := x"ABCDEFFF01"; -- 10
        hex digits => 40 bits
begin

    ----------------------------------------------------------------------------
    -- feedback (concurrent) for polynomial x^40 + x^38 + x^21 + x^19 + 1
    -- mapping: use indices 39 (x^40), 37 (x^38), 20 (x^21), 18 (x^19)
    ----------------------------------------------------------------------------
    -- Using XNOR convention (same used in earlier messages): feedback = not(xor
        (...))
    feedback_xnor <= not ( lfsr_q(39) xor lfsr_q(37) xor lfsr_q(20) xor lfsr_q(18)
         );

    ----------------------------------------------------------------------------
    -- synchronous process: reset / optional seed load / shift
    ----------------------------------------------------------------------------
    process(clk)
    begin
        if rising_edge(clk) then
            if rst = '1' then
                -- deterministic non-zero reset state (avoids 'U' and all-zero
                    lock)
                lfsr_q <= DEFAULT_SEED;
            elsif load_seed = '1' then
                -- synchronous load; avoid all-zero seed
                if seed = x"00000000" then
```

```
                    lfsr_q <= DEFAULT_SEED;
                else
                    lfsr_q <= seed;
                end if;
            elsif enable = '1' then
                -- shift right: new MSB = feedback, LSB shifted out
                lfsr_q <= feedback_xnor & lfsr_q(39 downto 1);
            end if;
        end if;
    end process;

    ----------------------------------------------------------------------------
    -- output the state (MSB at index 39)
    ----------------------------------------------------------------------------
    lfsr_vec <= lfsr_q;

end architecture;


-- org_plpf_n2.vhd
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity org_plpf_n2 is
    port (
        clk       : in  std_logic;
        rst       : in  std_logic;
        valid     : in  std_logic;
        Tj        : in  std_logic;
        F1        : in  std_logic;
        out_valid : out std_logic;
        out_bit   : out std_logic
    );
end entity;

architecture rtl of org_plpf_n2 is
    signal prev_S    : std_logic := '0';
    signal or_all    : std_logic;
    signal and_all   : std_logic;
begin
    or_all  <= Tj or F1;
    and_all <= Tj and F1;

    proc_seq : process(clk)
        variable next_prev : std_logic;
    begin
        if rising_edge(clk) then
            if rst = '1' then
                prev_S    <= '0';
                out_valid <= '0';
                out_bit   <= '0';
            else
                if valid = '1' then
                    if prev_S = '1' then
                        out_bit <= or_all;
                        next_prev := or_all;
                    else
                        out_bit <= and_all;
                        next_prev := and_all;
                    end if;
                    out_valid <= '1';
                    prev_S <= next_prev;
                else
```

```
                    out_valid <= '0';
                end if;
            end if;
        end if;
    end process;
end architecture;
-- org_plpf_n3.vhd
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity org_plpf_n3 is
    port (
        clk       : in  std_logic;
        rst       : in  std_logic;
        valid     : in  std_logic;
        Tj        : in  std_logic;
        F1        : in  std_logic;
        F2        : in  std_logic;
        out_valid : out std_logic;
        out_bit   : out std_logic
    );
end entity;

architecture rtl of org_plpf_n3 is
    signal prev_S  : std_logic := '0';
    signal or_fut  : std_logic;
    signal and_fut : std_logic;
    signal or_all  : std_logic;
    signal and_all : std_logic;
begin
    -- compute reductions (combinational)
    proc_reduce : process(Tj, F1, F2)
    begin
        if (F1 = '1') or (F2 = '1') then
            or_fut <= '1';
        else
            or_fut <= '0';
        end if;

        if (F1 = '1') and (F2 = '1') then
            and_fut <= '1';
        else
            and_fut <= '0';
        end if;

        or_all  <= Tj or or_fut;
        and_all <= Tj and and_fut;
    end process;

    proc_seq : process(clk)
        variable next_prev : std_logic;
    begin
        if rising_edge(clk) then
            if rst = '1' then
                prev_S    <= '0';
                out_valid <= '0';
                out_bit   <= '0';
            else
                if valid = '1' then
                    if prev_S = '1' then
                        out_bit <= or_all;
                        next_prev := or_all;
                    else
```

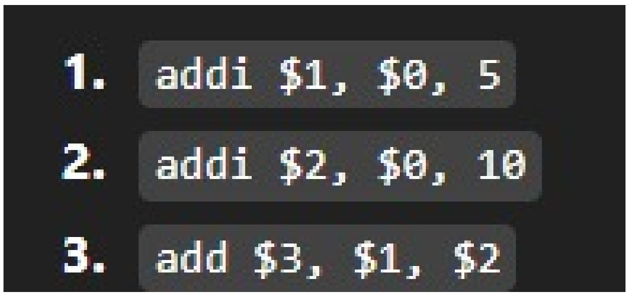
```
                        out_bit <= and_all;
                        next_prev := and_all;
                    end if;
                    out_valid <= '1';
                    prev_S <= next_prev;
                else
                    out_valid <= '0';
                end if;
            end if;
        end if;
    end process;
end architecture;
-- dynamic_plpf_taps_40.vhd
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity dynamic_plpf_taps_40 is
    port (
        clk       : in  std_logic;
        rst       : in  std_logic;
        valid     : in  std_logic;
        lfsr_vec  : in  std_logic_vector(39 downto 0); -- 40-bit LFSR, MSB = Tj
        sel_n     : in  unsigned(1 downto 0);          -- "00"=n1, "01"=n2, "10"=
            n3
        out_valid : out std_logic;
        out_bit   : out std_logic
    );
end entity;

architecture rtl of dynamic_plpf_taps_40 is
    signal Tj : std_logic;
    signal F1 : std_logic;
    signal F2 : std_logic;

    signal p2_valid, p3_valid : std_logic;
    signal p2_bit, p3_bit     : std_logic;

    signal sel_int : integer range 1 to 3 := 1;
begin
    -- map taps: Tj = MSB (39), F1 = 38, F2 = 37
    Tj <= lfsr_vec(39);
    F1 <= lfsr_vec(38);
    F2 <= lfsr_vec(37);

    u_p2: entity work.org_plpf_n2
        port map (
            clk => clk, rst => rst, valid => valid,
            Tj => Tj, F1 => F1,
            out_valid => p2_valid, out_bit => p2_bit
        );

    u_p3: entity work.org_plpf_n3
        port map (
            clk => clk, rst => rst, valid => valid,
            Tj => Tj, F1 => F1, F2 => F2,
            out_valid => p3_valid, out_bit => p3_bit
        );

    -- decode sel
    decode_sel: process(sel_n)
    begin
        if sel_n = "00" then
            sel_int <= 1;
        elsif sel_n = "01" then
            sel_int <= 2;
        elsif sel_n = "10" then
            sel_int <= 3;
        else
            sel_int <= 1;
        end if;
    end process;

    -- synchronous mux (registered outputs)
    out_mux : process(clk)
    begin
        if rising_edge(clk) then
            if rst = '1' then
                out_valid <= '0';
                out_bit <= '0';
            else
                if sel_int = 1 then
                    if valid = '1' then
                        out_valid <= '1';
                        out_bit <= Tj;
                    else
                        out_valid <= '0';
                    end if;
                elsif sel_int = 2 then
                    out_valid <= p2_valid;
                    out_bit   <= p2_bit;
                else
                    out_valid <= p3_valid;
                    out_bit   <= p3_bit;
                end if;
            end if;
        end if;
    end process;
end architecture;

--------------------------------------------------------------------------------
-- MIPS32 5-stage pipeline with scan chains - CORRECTED VERSION
--------------------------------------------------------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- [All component entities remain the same: ALU, RegFile, InstrMem, DataMem,
--  SignExt, ControlUnit, ALUControl, ForwardUnit, HazardUnit]
-- [Copying them from the original correct code...]

-- 1) ALU
entity ALU is
    port (
        A       : in  std_logic_vector(31 downto 0);
        B       : in  std_logic_vector(31 downto 0);
        ALUCtrl : in  std_logic_vector(3 downto 0);
        Result  : out std_logic_vector(31 downto 0);
        Zero    : out std_logic
    );
end ALU;

architecture Behavioral of ALU is
    constant ZERO32 : std_logic_vector(31 downto 0) := (others => '0');
begin
    process(A, B, ALUCtrl)
        variable tmp_v : std_logic_vector(31 downto 0);
```

```vhdl
        variable a_s   : signed(31 downto 0);
        variable b_s   : signed(31 downto 0);
        variable res_s : signed(31 downto 0);
    begin
        a_s := signed(A);
        b_s := signed(B);
        tmp_v := (others => '0');
        res_s := (others => '0');

        case ALUCtrl is
            when "0010" => res_s := a_s + b_s; tmp_v := std_logic_vector(res_s);
            when "0110" => res_s := a_s - b_s; tmp_v := std_logic_vector(res_s);
            when "0000" => tmp_v := A and B;
            when "0001" => tmp_v := A or B;
            when "0111" =>
                if a_s < b_s then
                    tmp_v := std_logic_vector(to_signed(1, 32));
                else
                    tmp_v := ZERO32;
                end if;
            when others => tmp_v := ZERO32;
        end case;

        Result <= tmp_v;
        if tmp_v = ZERO32 then
            Zero <= '1';
        else
            Zero <= '0';
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 2) RegFile
entity RegFile is
    port (
        clk     : in  std_logic;
        we      : in  std_logic;
        rd_addr : in  std_logic_vector(4 downto 0);
        rs_addr : in  std_logic_vector(4 downto 0);
        rt_addr : in  std_logic_vector(4 downto 0);
        wd      : in  std_logic_vector(31 downto 0);
        rs_data : out std_logic_vector(31 downto 0);
        rt_data : out std_logic_vector(31 downto 0)
    );
end RegFile;

architecture Behavioral of RegFile is
    type reg_array is array(0 to 31) of std_logic_vector(31 downto 0);
    signal regs : reg_array := (others => (others => '0'));
begin
    rs_data <= regs(to_integer(unsigned(rs_addr)));
    rt_data <= regs(to_integer(unsigned(rt_addr)));

    process(clk)
    begin
        if rising_edge(clk) then
            if we = '1' then
                if rd_addr /= "00000" then
                    regs(to_integer(unsigned(rd_addr))) <= wd;
                end if;
            end if;
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 3) InstrMem
entity InstrMem is
    port(
        Addr      : in  std_logic_vector(31 downto 0);
        Instr     : out std_logic_vector(31 downto 0);
        sim_we    : in  std_logic;
        sim_addr  : in  std_logic_vector(7 downto 0);
        sim_data  : in  std_logic_vector(31 downto 0)
    );
end InstrMem;

architecture Behavioral of InstrMem is
    type mem_type is array(0 to 255) of std_logic_vector(31 downto 0);
    signal ROM : mem_type := (others => (others => '0'));
begin
    Instr <= ROM(to_integer(unsigned(Addr(9 downto 2))));

    process(sim_we, sim_addr, sim_data)
    begin
        if sim_we = '1' then
            ROM(to_integer(unsigned(sim_addr))) <= sim_data;
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 4) DataMem
entity DataMem is
    port (
        clk        : in  std_logic;
        mem_write  : in  std_logic;
        mem_read   : in  std_logic;
        Addr       : in  std_logic_vector(31 downto 0);
        WriteData  : in  std_logic_vector(31 downto 0);
        ReadData   : out std_logic_vector(31 downto 0)
    );
end DataMem;

architecture Behavioral of DataMem is
    type ram_type is array(0 to 1023) of std_logic_vector(31 downto 0);
    signal RAM : ram_type := (others => (others => '0'));
    signal rdata_reg : std_logic_vector(31 downto 0) := (others => '0');
begin
    process(clk)
    begin
        if rising_edge(clk) then
            if mem_write = '1' then
                RAM(to_integer(unsigned(Addr(11 downto 2)))) <= WriteData;
            end if;
            if mem_read = '1' then
                rdata_reg <= RAM(to_integer(unsigned(Addr(11 downto 2))));
            end if;
        end if;
    end process;
    ReadData <= rdata_reg;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 5) SignExt
entity SignExt is
    port (
        Imm16 : in  std_logic_vector(15 downto 0);
        Imm32 : out std_logic_vector(31 downto 0)
    );
end SignExt;

architecture Behavioral of SignExt is
begin
    Imm32 <= std_logic_vector(resize(signed(Imm16), 32));
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 6) ControlUnit
entity ControlUnit is
    port (
        Opcode     : in  std_logic_vector(5 downto 0);
        RegDst     : out std_logic;
        ALUSrc     : out std_logic;
        MemToReg   : out std_logic;
        RegWrite   : out std_logic;
        MemRead    : out std_logic;
        MemWrite   : out std_logic;
        Branch     : out std_logic;
        Jump       : out std_logic;
        ALUOp      : out std_logic_vector(1 downto 0)
    );
end ControlUnit;

architecture Behavioral of ControlUnit is
begin
    process(Opcode)
    begin
        RegDst   <= '0'; ALUSrc   <= '0'; MemToReg <= '0'; RegWrite <= '0';
        MemRead  <= '0'; MemWrite <= '0'; Branch   <= '0'; Jump     <= '0';
        ALUOp    <= "00";
        case Opcode is
            when "000000" => RegDst <= '1'; RegWrite <= '1'; ALUOp <= "10";
            when "100011" => ALUSrc <= '1'; MemToReg <= '1'; RegWrite <= '1';
                MemRead <= '1';
            when "101011" => ALUSrc <= '1'; MemWrite <= '1';
            when "000100" => Branch <= '1'; ALUOp <= "01";
            when "001000" => ALUSrc <= '1'; RegWrite <= '1';
            when "000010" => Jump <= '1';
            when others => null;
        end case;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 7) ALUControl
entity ALUControl is
    port (
        ALUOp    : in  std_logic_vector(1 downto 0);
        Funct    : in  std_logic_vector(5 downto 0);
        ALUCtrl  : out std_logic_vector(3 downto 0)
    );
end ALUControl;

architecture Behavioral of ALUControl is
begin
    process(ALUOp, Funct)
    begin
        if ALUOp = "00" then
            ALUCtrl <= "0010";
        elsif ALUOp = "01" then
            ALUCtrl <= "0110";
        else
            case Funct is
                when "100000" => ALUCtrl <= "0010";
                when "100010" => ALUCtrl <= "0110";
                when "100100" => ALUCtrl <= "0000";
                when "100101" => ALUCtrl <= "0001";
                when "101010" => ALUCtrl <= "0111";
                when others   => ALUCtrl <= "0010";
            end case;
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 8) ForwardUnit
entity ForwardUnit is
    port (
        EX_MEM_RegWrite : in std_logic;
        MEM_WB_RegWrite : in std_logic;
        EX_MEM_Rd       : in std_logic_vector(4 downto 0);
        MEM_WB_Rd       : in std_logic_vector(4 downto 0);
        ID_EX_Rs        : in std_logic_vector(4 downto 0);
        ID_EX_Rt        : in std_logic_vector(4 downto 0);
        ForwardA        : out std_logic_vector(1 downto 0);
        ForwardB        : out std_logic_vector(1 downto 0)
    );
end ForwardUnit;

architecture Behavioral of ForwardUnit is
begin
    process(EX_MEM_RegWrite, MEM_WB_RegWrite, EX_MEM_Rd, MEM_WB_Rd, ID_EX_Rs,
       ID_EX_Rt)
    begin
        ForwardA <= "00"; ForwardB <= "00";
        if (EX_MEM_RegWrite = '1') and (EX_MEM_Rd /= "00000") and (EX_MEM_Rd =
           ID_EX_Rs) then
            ForwardA <= "10";
        end if;
        if (EX_MEM_RegWrite = '1') and (EX_MEM_Rd /= "00000") and (EX_MEM_Rd =
           ID_EX_Rt) then
            ForwardB <= "10";
        end if;
        if (MEM_WB_RegWrite = '1') and (MEM_WB_Rd /= "00000") and
           (not ((EX_MEM_RegWrite = '1') and (EX_MEM_Rd /= "00000") and (EX_MEM_Rd
                = ID_EX_Rs))) and
           (MEM_WB_Rd = ID_EX_Rs) then
            ForwardA <= "01";
        end if;
        if (MEM_WB_RegWrite = '1') and (MEM_WB_Rd /= "00000") and
           (not ((EX_MEM_RegWrite = '1') and (EX_MEM_Rd /= "00000") and (EX_MEM_Rd
                = ID_EX_Rt))) and
           (MEM_WB_Rd = ID_EX_Rt) then
            ForwardB <= "01";
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 9) HazardUnit
entity HazardUnit is
    port (
        ID_EX_MemRead : in std_logic;
        ID_EX_Rt      : in std_logic_vector(4 downto 0);
        IF_ID_Rs      : in std_logic_vector(4 downto 0);
        IF_ID_Rt      : in std_logic_vector(4 downto 0);
        PCWrite       : out std_logic;
        IF_ID_Write   : out std_logic;
        Stall         : out std_logic
    );
end HazardUnit;

architecture Behavioral of HazardUnit is
begin
    process(ID_EX_MemRead, ID_EX_Rt, IF_ID_Rs, IF_ID_Rt)
    begin
        if (ID_EX_MemRead = '1') and ((ID_EX_Rt = IF_ID_Rs) or (ID_EX_Rt =
            IF_ID_Rt)) then
            PCWrite <= '0'; IF_ID_Write <= '0'; Stall <= '1';
        else
            PCWrite <= '1'; IF_ID_Write <= '1'; Stall <= '0';
        end if;
    end process;
end Behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- 10) MIPS5Pipe top with PLPF-driven scan chain inputs and top-level MISR outputs
entity MIPS5Pipe is
    port(
        clk   : in std_logic;
        reset : in std_logic;
        sim_we    : in std_logic := '0';
        sim_addr  : in std_logic_vector(7 downto 0) := (others=>'0');
        sim_data  : in std_logic_vector(31 downto 0) := (others=>'0');

        debug_PC          : out std_logic_vector(31 downto 0);
        debug_Instr       : out std_logic_vector(31 downto 0);
        debug_ALUResult   : out std_logic_vector(31 downto 0);
        debug_Zero        : out std_logic;
        debug_ALUCtrl     : out std_logic_vector(3 downto 0);
        debug_ALU_InA     : out std_logic_vector(31 downto 0);
        debug_ALU_InB     : out std_logic_vector(31 downto 0);
        debug_SignExtImm  : out std_logic_vector(31 downto 0);
        debug_RegWrite    : out std_logic;

        -- scan control (external enables kept)
        scan_en_pc       : in  std_logic := '0';
        scan_in_pc       : in  std_logic := '0'; -- kept in port list for
            compatibility, but not used
        scan_out_pc      : out std_logic;
        scan_en_ifid     : in  std_logic := '0';
        scan_in_ifid     : in  std_logic := '0'; -- kept but unused
        scan_out_ifid    : out std_logic;
        scan_en_idex     : in  std_logic := '0';
        scan_in_idex     : in  std_logic := '0'; -- kept but unused
        scan_out_idex    : out std_logic;
        scan_en_exmem    : in  std_logic := '0';
        scan_in_exmem     : in  std_logic := '0'; -- kept but unused
        scan_out_exmem   : out std_logic;
        scan_en_memwb    : in  std_logic := '0';
        scan_in_memwb    : in  std_logic := '0'; -- kept but unused
        scan_out_memwb   : out std_logic;

        -- TOP-LEVEL MISR OUTPUTS (signatures)
        misr_pc_sig    : out std_logic_vector(31 downto 0);
        misr_ifid_sig  : out std_logic_vector(63 downto 0);
        misr_idex_sig  : out std_logic_vector(151 downto 0);
        misr_exmem_sig : out std_logic_vector(74 downto 0);
        misr_memwb_sig : out std_logic_vector(70 downto 0)
    );
end MIPS5Pipe;

architecture Behavioral of MIPS5Pipe is
    -- Functional registers
    signal reg_PC : std_logic_vector(31 downto 0) := (others => '0');
    signal reg_IF_ID_PC    : std_logic_vector(31 downto 0) := (others => '0');
    signal reg_IF_ID_Instr : std_logic_vector(31 downto 0) := (others => '0');

    signal reg_ID_EX_RegDst, reg_ID_EX_ALUSrc, reg_ID_EX_MemToReg,
        reg_ID_EX_RegWrite,
            reg_ID_EX_MemRead, reg_ID_EX_MemWrite, reg_ID_EX_Branch : std_logic :=
                '0';
    signal reg_ID_EX_ALUOp : std_logic_vector(1 downto 0) := (others => '0');
    signal reg_ID_EX_PC, reg_ID_EX_RSdata, reg_ID_EX_RTdata, reg_ID_EX_Imm32 :
        std_logic_vector(31 downto 0) := (others => '0');
    signal reg_ID_EX_Rs, reg_ID_EX_Rt, reg_ID_EX_Rd : std_logic_vector(4 downto 0)
         := (others => '0');

    signal reg_EX_MEM_MemToReg, reg_EX_MEM_RegWrite, reg_EX_MEM_MemRead,
        reg_EX_MEM_MemWrite, reg_EX_MEM_Branch : std_logic := '0';
    signal reg_EX_MEM_ALUResult, reg_EX_MEM_RTdata : std_logic_vector(31 downto 0)
         := (others => '0');
    signal reg_EX_MEM_WriteReg : std_logic_vector(4 downto 0) := (others => '0');
    signal reg_EX_MEM_Zero : std_logic := '0';

    signal reg_MEM_WB_MemToReg, reg_MEM_WB_RegWrite : std_logic := '0';
    signal reg_MEM_WB_ReadData, reg_MEM_WB_ALUResult : std_logic_vector(31 downto
        0) := (others => '0');
    signal reg_MEM_WB_WriteReg : std_logic_vector(4 downto 0) := (others => '0');

    -- Pipe signals
    signal PC, PC_next, Instr_IF : std_logic_vector(31 downto 0);
    signal IF_ID_PC, IF_ID_Instr : std_logic_vector(31 downto 0);

    signal ID_EX_RegDst, ID_EX_ALUSrc, ID_EX_MemToReg, ID_EX_RegWrite,
        ID_EX_MemRead, ID_EX_MemWrite, ID_EX_Branch : std_logic;
    signal ID_EX_ALUOp  : std_logic_vector(1 downto 0);
    signal ID_EX_PC, ID_EX_RSdata, ID_EX_RTdata, ID_EX_Imm32 : std_logic_vector(31
         downto 0);
    signal ID_EX_Rs, ID_EX_Rt, ID_EX_Rd : std_logic_vector(4 downto 0);

    signal EX_MEM_MemToReg, EX_MEM_RegWrite, EX_MEM_MemRead, EX_MEM_MemWrite,
        EX_MEM_Branch : std_logic;
    signal EX_MEM_ALUResult, EX_MEM_RTdata : std_logic_vector(31 downto 0);
    signal EX_MEM_WriteReg : std_logic_vector(4 downto 0);
    signal EX_MEM_Zero : std_logic;

    signal MEM_WB_MemToReg, MEM_WB_RegWrite : std_logic;
    signal MEM_WB_ReadData, MEM_WB_ALUResult : std_logic_vector(31 downto 0);
    signal MEM_WB_WriteReg : std_logic_vector(4 downto 0);

    signal RegDst_i, ALUSrc_i, MemToReg_i, RegWrite_i, MemRead_i, MemWrite_i,
        Branch_i, Jump_i : std_logic;
    signal ALUOp_i : std_logic_vector(1 downto 0);
    signal RS_data, RT_data, Imm32 : std_logic_vector(31 downto 0);
    signal ALU_input_B, ALUResult_ex : std_logic_vector(31 downto 0);
    signal ALUZero_ex : std_logic;
    signal ALUCtrl_ex : std_logic_vector(3 downto 0);
    signal rs_value_for_alu, rt_value_for_alu : std_logic_vector(31 downto 0);
    signal EX_WriteReg : std_logic_vector(4 downto 0);
    signal MEM_ReadData, WB_WriteData : std_logic_vector(31 downto 0);
    signal ForwardA, ForwardB : std_logic_vector(1 downto 0);
    signal PCWrite, IF_ID_Write, Stall : std_logic;

    -- Scan chain constants
    constant W_PC    : integer := 32;
    constant W_IFID  : integer := 64;
    constant W_IDEX  : integer := 152;
    constant W_EXMEM : integer := 75;
    constant W_MEMWB : integer := 71;

    signal scan_chain_pc    : std_logic_vector(W_PC-1 downto 0) := (others => '0')
        ;
    signal scan_chain_ifid  : std_logic_vector(W_IFID-1 downto 0) := (others =>
        '0');
    signal scan_chain_idex  : std_logic_vector(W_IDEX-1 downto 0) := (others =>
        '0');
    signal scan_chain_exmem : std_logic_vector(W_EXMEM-1 downto 0) := (others =>
        '0');
    signal scan_chain_memwb : std_logic_vector(W_MEMWB-1 downto 0) := (others =>
        '0');

    signal func_pc_concat    : std_logic_vector(W_PC-1 downto 0);
    signal func_ifid_concat  : std_logic_vector(W_IFID-1 downto 0);
    signal func_idex_concat  : std_logic_vector(W_IDEX-1 downto 0);
    signal func_exmem_concat : std_logic_vector(W_EXMEM-1 downto 0);
    signal func_memwb_concat : std_logic_vector(W_MEMWB-1 downto 0);

    -- PLPF / LFSR signals (drive scan_in bits from PLPF outputs)
    signal lfsr_vec_sig : std_logic_vector(39 downto 0);
    signal plpf_pc_bit  : std_logic := '0';
    signal plpf_ifid_bit: std_logic := '0';
    signal plpf_idex_bit: std_logic := '0';
    signal plpf_exmem_bit: std_logic := '0';
```

```vhdl

    -- Internal MISR signature signals (renamed to avoid port-name clash)
    signal misr_pc_sig_int    : std_logic_vector(W_PC-1 downto 0) := (others => '0');
    signal misr_ifid_sig_int  : std_logic_vector(W_IFID-1 downto 0) := (others => '0');
    signal misr_idex_sig_int  : std_logic_vector(W_IDEX-1 downto 0) := (others => '0');
    signal misr_exmem_sig_int : std_logic_vector(W_EXMEM-1 downto 0) := (others => '0');
    signal misr_memwb_sig_int : std_logic_vector(W_MEMWB-1 downto 0) := (others => '0');

begin
    -- Component instantiations (functional units unchanged)
    InstrMem_inst : entity work.InstrMem
        port map(Addr => PC, Instr => Instr_IF, sim_we => sim_we, sim_addr => sim_addr, sim_data => sim_data);

    RegFile_inst : entity work.RegFile
        port map(clk => clk, we => MEM_WB_RegWrite, rd_addr => MEM_WB_WriteReg,
                 rs_addr => IF_ID_Instr(25 downto 21), rt_addr => IF_ID_Instr(20 downto 16),
                 wd => WB_WriteData, rs_data => RS_data, rt_data => RT_data);

    Control_inst : entity work.ControlUnit
        port map(Opcode => IF_ID_Instr(31 downto 26), RegDst => RegDst_i, ALUSrc => ALUSrc_i,
                 MemToReg => MemToReg_i, RegWrite => RegWrite_i, MemRead => MemRead_i,
                 MemWrite => MemWrite_i, Branch => Branch_i, Jump => Jump_i, ALUOp => ALUOp_i);

    SignExt_inst : entity work.SignExt
        port map(Imm16 => IF_ID_Instr(15 downto 0), Imm32 => Imm32);

    ALUControl_inst : entity work.ALUControl
        port map(ALUOp => ID_EX_ALUOp, Funct => ID_EX_Imm32(5 downto 0), ALUCtrl => ALUCtrl_ex);

    ALU_inst : entity work.ALU
        port map(A => rs_value_for_alu, B => ALU_input_B, ALUCtrl => ALUCtrl_ex,
                 Result => ALUResult_ex, Zero => ALUZero_ex);

    Forward_inst : entity work.ForwardUnit
        port map(EX_MEM_RegWrite => EX_MEM_RegWrite, MEM_WB_RegWrite => MEM_WB_RegWrite,
                 EX_MEM_Rd => EX_MEM_WriteReg, MEM_WB_Rd => MEM_WB_WriteReg,
                 ID_EX_Rs => ID_EX_Rs, ID_EX_Rt => ID_EX_Rt,
                 ForwardA => ForwardA, ForwardB => ForwardB);

    Hazard_inst : entity work.HazardUnit
        port map(ID_EX_MemRead => ID_EX_MemRead, ID_EX_Rt => ID_EX_Rt,
                 IF_ID_Rs => IF_ID_Instr(25 downto 21), IF_ID_Rt => IF_ID_Instr(20 downto 16),
                 PCWrite => PCWrite, IF_ID_Write => IF_ID_Write, Stall => Stall);

    DataMem_inst : entity work.DataMem
        port map(clk => clk, mem_write => EX_MEM_MemWrite, mem_read => EX_MEM_MemRead,
                 Addr => EX_MEM_ALUResult, WriteData => EX_MEM_RTdata, ReadData => MEM_ReadData);

    -- LFSR and PLPF instantiations (drive scan-chain serial input bits)
    u_lfsr40: entity work.lfsr40
        port map(
            clk => clk,
            rst => reset,
            load_seed => '0',
            seed => (others => '0'),
            enable => '1',
            lfsr_vec => lfsr_vec_sig
        );

    -- One dynamic PLPF per scan chain. valid tied to scan_en signals.
    u_plpf_pc: entity work.dynamic_plpf_taps_40
        port map(
            clk => clk, rst => reset, valid => scan_en_pc,
            lfsr_vec => lfsr_vec_sig, sel_n => "00",
            out_valid => open, out_bit => plpf_pc_bit
        );

    u_plpf_ifid: entity work.dynamic_plpf_taps_40
        port map(
            clk => clk, rst => reset, valid => scan_en_ifid,
            lfsr_vec => lfsr_vec_sig, sel_n => "01",
            out_valid => open, out_bit => plpf_ifid_bit
        );

    u_plpf_idex: entity work.dynamic_plpf_taps_40
        port map(
            clk => clk, rst => reset, valid => scan_en_idex,
            lfsr_vec => lfsr_vec_sig, sel_n => "10",
            out_valid => open, out_bit => plpf_idex_bit
        );

    u_plpf_exmem: entity work.dynamic_plpf_taps_40
        port map(
            clk => clk, rst => reset, valid => scan_en_exmem,
            lfsr_vec => lfsr_vec_sig, sel_n => "00",
            out_valid => open, out_bit => plpf_exmem_bit
        );

    -- Functional concatenations
    func_pc_concat <= reg_PC;
    func_ifid_concat <= reg_IF_ID_PC & reg_IF_ID_Instr;
    func_idex_concat <= (reg_ID_EX_RegDst & reg_ID_EX_ALUSrc & reg_ID_EX_MemToReg & reg_ID_EX_RegWrite &
                         reg_ID_EX_MemRead & reg_ID_EX_MemWrite & reg_ID_EX_Branch & reg_ID_EX_ALUOp) &
                        reg_ID_EX_PC & reg_ID_EX_RSdata & reg_ID_EX_RTdata & reg_ID_EX_Imm32 &
                        reg_ID_EX_Rs & reg_ID_EX_Rt & reg_ID_EX_Rd;
    func_exmem_concat <= (reg_EX_MEM_MemToReg & reg_EX_MEM_RegWrite & reg_EX_MEM_MemRead &
                          reg_EX_MEM_MemWrite & reg_EX_MEM_Branch) &
                         reg_EX_MEM_ALUResult & reg_EX_MEM_RTdata & reg_EX_MEM_WriteReg & reg_EX_MEM_Zero;
    func_memwb_concat <= (reg_MEM_WB_MemToReg & reg_MEM_WB_RegWrite) &
                         reg_MEM_WB_ReadData & reg_MEM_WB_ALUResult & reg_MEM_WB_WriteReg;

    -- Scan chain processes: use PLPF outputs as the serial input when shifting.
    process(clk, reset)
    begin
        if reset = '1' then
            scan_chain_pc <= (others => '0');
        elsif rising_edge(clk) then
```

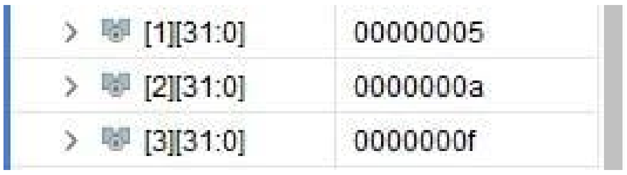
```
            if scan_en_pc = '1' then
                scan_chain_pc <= plpf_pc_bit & scan_chain_pc(W_PC-1 downto 1);
            else
                scan_chain_pc <= func_pc_concat;
            end if;
        end if;
    end process;
    scan_out_pc <= scan_chain_pc(0);

    process(clk, reset)
    begin
        if reset = '1' then
            scan_chain_ifid <= (others => '0');
        elsif rising_edge(clk) then
            if scan_en_ifid = '1' then
                scan_chain_ifid <= plpf_ifid_bit & scan_chain_ifid(W_IFID-1 downto
                     1);
            else
                scan_chain_ifid <= func_ifid_concat;
            end if;
        end if;
    end process;
    scan_out_ifid <= scan_chain_ifid(0);

    process(clk, reset)
    begin
        if reset = '1' then
            scan_chain_idex <= (others => '0');
        elsif rising_edge(clk) then
            if scan_en_idex = '1' then
                scan_chain_idex <= plpf_idex_bit & scan_chain_idex(W_IDEX-1 downto
                     1);
            else
                scan_chain_idex <= func_idex_concat;
            end if;
        end if;
    end process;
    scan_out_idex <= scan_chain_idex(0);

    process(clk, reset)
    begin
        if reset = '1' then
            scan_chain_exmem <= (others => '0');
        elsif rising_edge(clk) then
            if scan_en_exmem = '1' then
                scan_chain_exmem <= plpf_exmem_bit & scan_chain_exmem(W_EXMEM-1
                    downto 1);
            else
                scan_chain_exmem <= func_exmem_concat;
            end if;
        end if;
    end process;
    scan_out_exmem <= scan_chain_exmem(0);

    process(clk, reset)
    begin
        if reset = '1' then
            scan_chain_memwb <= (others => '0');
        elsif rising_edge(clk) then
            if scan_en_memwb = '1' then
                scan_chain_memwb <= scan_in_memwb & scan_chain_memwb(W_MEMWB-1
                    downto 1);
            else
                scan_chain_memwb <= func_memwb_concat;
            end if;
        end if;
    end process;
    scan_out_memwb <= scan_chain_memwb(0);

    -----------------------------------------------------------------
    -- MISR instantiations (placed AFTER scan chains so 'scan_chain_*' is valid)
    -- MISRs are disabled while the chain is shifting (enable = not scan_en_*)
    -----------------------------------------------------------------
    u_misr_pc: entity work.MISR
        generic map ( W => W_PC )
        port map (
            clk     => clk,
            rst     => reset,
            enable  => not scan_en_pc,        -- MISR off while loading
            din     => scan_chain_pc,
            sig_out => misr_pc_sig_int
        );

    u_misr_ifid: entity work.MISR
        generic map ( W => W_IFID )
        port map (
            clk     => clk,
            rst     => reset,
            enable  => not scan_en_ifid,
            din     => scan_chain_ifid,
            sig_out => misr_ifid_sig_int
        );

    u_misr_idex: entity work.MISR
        generic map ( W => W_IDEX )
        port map (
            clk     => clk,
            rst     => reset,
            enable  => not scan_en_idex,
            din     => scan_chain_idex,
            sig_out => misr_idex_sig_int
        );

    u_misr_exmem: entity work.MISR
        generic map ( W => W_EXMEM )
        port map (
            clk     => clk,
            rst     => reset,
            enable  => not scan_en_exmem,
            din     => scan_chain_exmem,
            sig_out => misr_exmem_sig_int
        );

    u_misr_memwb: entity work.MISR
        generic map ( W => W_MEMWB )
        port map (
            clk     => clk,
            rst     => reset,
            enable  => not scan_en_memwb,
            din     => scan_chain_memwb,
            sig_out => misr_memwb_sig_int
        );

    -- connect internal MISR signals to entity outputs
    misr_pc_sig    <= misr_pc_sig_int;
    misr_ifid_sig  <= misr_ifid_sig_int;
    misr_idex_sig  <= misr_idex_sig_int;
    misr_exmem_sig <= misr_exmem_sig_int;
```

```vhdl
    misr_memwb_sig <= misr_memwb_sig_int;

    -- Pipe signal selection from scan chains or functional registers
    PC <= scan_chain_pc when scan_en_pc = '1' else reg_PC;

    IF_ID_PC    <= scan_chain_ifid(W_IFID-1 downto 32) when scan_en_ifid = '1'
       else reg_IF_ID_PC;
    IF_ID_Instr <= scan_chain_ifid(31 downto 0)        when scan_en_ifid = '1'
       else reg_IF_ID_Instr;

    ID_EX_RegDst   <= scan_chain_idex(151) when scan_en_idex = '1' else
       reg_ID_EX_RegDst;
    ID_EX_ALUSrc   <= scan_chain_idex(150) when scan_en_idex = '1' else
       reg_ID_EX_ALUSrc;
    ID_EX_MemToReg <= scan_chain_idex(149) when scan_en_idex = '1' else
       reg_ID_EX_MemToReg;
    ID_EX_RegWrite <= scan_chain_idex(148) when scan_en_idex = '1' else
       reg_ID_EX_RegWrite;
    ID_EX_MemRead  <= scan_chain_idex(147) when scan_en_idex = '1' else
       reg_ID_EX_MemRead;
    ID_EX_MemWrite <= scan_chain_idex(146) when scan_en_idex = '1' else
       reg_ID_EX_MemWrite;
    ID_EX_Branch   <= scan_chain_idex(145) when scan_en_idex = '1' else
       reg_ID_EX_Branch;
    ID_EX_ALUOp    <= scan_chain_idex(144 downto 143) when scan_en_idex = '1' else
        reg_ID_EX_ALUOp;
    ID_EX_PC       <= scan_chain_idex(142 downto 111) when scan_en_idex = '1' else
        reg_ID_EX_PC;
    ID_EX_RSdata   <= scan_chain_idex(110 downto 79)  when scan_en_idex = '1' else
        reg_ID_EX_RSdata;
    ID_EX_RTdata   <= scan_chain_idex(78 downto 47)   when scan_en_idex = '1' else
        reg_ID_EX_RTdata;
    ID_EX_Imm32    <= scan_chain_idex(46 downto 15)   when scan_en_idex = '1' else
        reg_ID_EX_Imm32;
    ID_EX_Rs       <= scan_chain_idex(14 downto 10)   when scan_en_idex = '1' else
        reg_ID_EX_Rs;
    ID_EX_Rt       <= scan_chain_idex(9 downto 5)     when scan_en_idex = '1' else
        reg_ID_EX_Rt;
    ID_EX_Rd       <= scan_chain_idex(4 downto 0)     when scan_en_idex = '1' else
        reg_ID_EX_Rd;

    EX_MEM_MemToReg <= scan_chain_exmem(74) when scan_en_exmem = '1' else
       reg_EX_MEM_MemToReg;
    EX_MEM_RegWrite <= scan_chain_exmem(73) when scan_en_exmem = '1' else
       reg_EX_MEM_RegWrite;
    EX_MEM_MemRead  <= scan_chain_exmem(72) when scan_en_exmem = '1' else
       reg_EX_MEM_MemRead;
    EX_MEM_MemWrite <= scan_chain_exmem(71) when scan_en_exmem = '1' else
       reg_EX_MEM_MemWrite;
    EX_MEM_Branch   <= scan_chain_exmem(70) when scan_en_exmem = '1' else
       reg_EX_MEM_Branch;
    EX_MEM_ALUResult <= scan_chain_exmem(69 downto 38) when scan_en_exmem = '1'
       else reg_EX_MEM_ALUResult;
    EX_MEM_RTdata    <= scan_chain_exmem(37 downto 6)  when scan_en_exmem = '1'
       else reg_EX_MEM_RTdata;
    EX_MEM_WriteReg  <= scan_chain_exmem(5 downto 1)   when scan_en_exmem = '1'
       else reg_EX_MEM_WriteReg;
    EX_MEM_Zero      <= scan_chain_exmem(0)            when scan_en_exmem = '1'
       else reg_EX_MEM_Zero;

    MEM_WB_MemToReg  <= scan_chain_memwb(70) when scan_en_memwb = '1' else
       reg_MEM_WB_MemToReg;
    MEM_WB_RegWrite  <= scan_chain_memwb(69) when scan_en_memwb = '1' else
       reg_MEM_WB_RegWrite;
    MEM_WB_ReadData  <= scan_chain_memwb(68 downto 37) when scan_en_memwb = '1'
       else reg_MEM_WB_ReadData;
    MEM_WB_ALUResult <= scan_chain_memwb(36 downto 5)  when scan_en_memwb = '1'
       else reg_MEM_WB_ALUResult;
    MEM_WB_WriteReg  <= scan_chain_memwb(4 downto 0)   when scan_en_memwb = '1'
       else reg_MEM_WB_WriteReg;

    -- Functional register update processes (unchanged) ...
    process(clk, reset)
    begin
        if reset = '1' then
            reg_PC <= (others => '0');
        elsif rising_edge(clk) then
            if PCWrite = '1' then
                reg_PC <= PC_next;
            end if;
        end if;
    end process;

    process(clk, reset)
    begin
        if reset = '1' then
            reg_IF_ID_PC <= (others => '0');
            reg_IF_ID_Instr <= (others => '0');
        elsif rising_edge(clk) then
            if IF_ID_Write = '1' then
                reg_IF_ID_PC <= PC;
                reg_IF_ID_Instr <= Instr_IF;
            end if;
        end if;
    end process;

    process(clk, reset)
    begin
        if reset = '1' then
            reg_ID_EX_RegDst <= '0';
            reg_ID_EX_ALUSrc <= '0';
            reg_ID_EX_MemToReg <= '0';
            reg_ID_EX_RegWrite <= '0';
            reg_ID_EX_MemRead <= '0';
            reg_ID_EX_MemWrite <= '0';
            reg_ID_EX_Branch <= '0';
            reg_ID_EX_ALUOp <= (others => '0');
            reg_ID_EX_PC <= (others => '0');
            reg_ID_EX_RSdata <= (others => '0');
            reg_ID_EX_RTdata <= (others => '0');
            reg_ID_EX_Imm32 <= (others => '0');
            reg_ID_EX_Rs <= (others => '0');
            reg_ID_EX_Rt <= (others => '0');
            reg_ID_EX_Rd <= (others => '0');
        elsif rising_edge(clk) then
            if Stall = '1' then
                reg_ID_EX_RegDst <= '0';
                reg_ID_EX_ALUSrc <= '0';
                reg_ID_EX_MemToReg <= '0';
                reg_ID_EX_RegWrite <= '0';
                reg_ID_EX_MemRead <= '0';
                reg_ID_EX_MemWrite <= '0';
                reg_ID_EX_Branch <= '0';
                reg_ID_EX_ALUOp <= (others => '0');
            else
                reg_ID_EX_RegDst <= RegDst_i;
                reg_ID_EX_ALUSrc <= ALUSrc_i;
                reg_ID_EX_MemToReg <= MemToReg_i;
                reg_ID_EX_RegWrite <= RegWrite_i;
                reg_ID_EX_MemRead <= MemRead_i;
                reg_ID_EX_MemWrite <= MemWrite_i;
                reg_ID_EX_Branch <= Branch_i;
                reg_ID_EX_ALUOp <= ALUOp_i;
                reg_ID_EX_PC <= IF_ID_PC;
                reg_ID_EX_RSdata <= RS_data;
                reg_ID_EX_RTdata <= RT_data;
                reg_ID_EX_Imm32 <= Imm32;
                reg_ID_EX_Rs <= IF_ID_Instr(25 downto 21);
                reg_ID_EX_Rt <= IF_ID_Instr(20 downto 16);
                reg_ID_EX_Rd <= IF_ID_Instr(15 downto 11);
            end if;
        end if;
    end process;

    process(clk, reset)
    begin
        if reset = '1' then
            reg_EX_MEM_MemToReg <= '0';
            reg_EX_MEM_RegWrite <= '0';
            reg_EX_MEM_MemRead <= '0';
            reg_EX_MEM_MemWrite <= '0';
            reg_EX_MEM_Branch <= '0';
            reg_EX_MEM_ALUResult <= (others => '0');
            reg_EX_MEM_RTdata <= (others => '0');
            reg_EX_MEM_WriteReg <= (others => '0');
            reg_EX_MEM_Zero <= '0';
        elsif rising_edge(clk) then
            reg_EX_MEM_MemToReg <= ID_EX_MemToReg;
            reg_EX_MEM_RegWrite <= ID_EX_RegWrite;
            reg_EX_MEM_MemRead <= ID_EX_MemRead;
            reg_EX_MEM_MemWrite <= ID_EX_MemWrite;
            reg_EX_MEM_Branch <= ID_EX_Branch;
            reg_EX_MEM_ALUResult <= ALUResult_ex;
            reg_EX_MEM_RTdata <= rt_value_for_alu;
            reg_EX_MEM_WriteReg <= EX_WriteReg;
            reg_EX_MEM_Zero <= ALUZero_ex;
        end if;
    end process;

    process(clk, reset)
    begin
        if reset = '1' then
            reg_MEM_WB_MemToReg <= '0';
            reg_MEM_WB_RegWrite <= '0';
            reg_MEM_WB_ReadData <= (others => '0');
            reg_MEM_WB_ALUResult <= (others => '0');
            reg_MEM_WB_WriteReg <= (others => '0');
        elsif rising_edge(clk) then
            reg_MEM_WB_MemToReg <= EX_MEM_MemToReg;
            reg_MEM_WB_RegWrite <= EX_MEM_RegWrite;
            reg_MEM_WB_ReadData <= MEM_ReadData;
            reg_MEM_WB_ALUResult <= EX_MEM_ALUResult;
            reg_MEM_WB_WriteReg <= EX_MEM_WriteReg;
        end if;
    end process;

    -- Datapath logic and remaining code unchanged...
    WB_WriteData <= MEM_WB_ReadData when MEM_WB_MemToReg = '1' else
        MEM_WB_ALUResult;

    process(PC, EX_MEM_Branch, EX_MEM_Zero, IF_ID_Instr, Jump_i, EX_MEM_ALUResult)
        variable pc_plus4 : std_logic_vector(31 downto 0);
        variable jump_target : std_logic_vector(31 downto 0);
    begin
        pc_plus4 := std_logic_vector(unsigned(PC) + 4);
        jump_target := (pc_plus4(31 downto 28) & IF_ID_Instr(25 downto 0) & "00");
        PC_next <= pc_plus4;
        if (EX_MEM_Branch = '1') and (EX_MEM_Zero = '1') then
            PC_next <= EX_MEM_ALUResult;
        elsif Jump_i = '1' then
            PC_next <= jump_target;
        end if;
    end process;

    -- Forwarding muxes, ALU input selection, EX dest compute, debug outputs...
    process(ForwardA, ID_EX_RSdata, EX_MEM_ALUResult, MEM_WB_ALUResult,
       MEM_WB_ReadData, MEM_WB_MemToReg)
    begin
        case ForwardA is
            when "00" => rs_value_for_alu <= ID_EX_RSdata;
            when "10" => rs_value_for_alu <= EX_MEM_ALUResult;
            when "01" =>
                if MEM_WB_MemToReg = '1' then
                    rs_value_for_alu <= MEM_WB_ReadData;
                else
                    rs_value_for_alu <= MEM_WB_ALUResult;
                end if;
            when others => rs_value_for_alu <= ID_EX_RSdata;
        end case;
    end process;

    process(ForwardB, ID_EX_RTdata, EX_MEM_ALUResult, MEM_WB_ALUResult,
       MEM_WB_ReadData, MEM_WB_MemToReg)
    begin
        case ForwardB is
            when "00" => rt_value_for_alu <= ID_EX_RTdata;
            when "10" => rt_value_for_alu <= EX_MEM_ALUResult;
            when "01" =>
                if MEM_WB_MemToReg = '1' then
                    rt_value_for_alu <= MEM_WB_ReadData;
                else
                    rt_value_for_alu <= MEM_WB_ALUResult;
                end if;
            when others => rt_value_for_alu <= ID_EX_RTdata;
        end case;
    end process;

    ALU_input_B <= ID_EX_Imm32 when ID_EX_ALUSrc = '1' else rt_value_for_alu;

    process(ID_EX_RegDst, ID_EX_Rt, ID_EX_Rd)
    begin
        if ID_EX_RegDst = '1' then
            EX_WriteReg <= ID_EX_Rd;
        else
            EX_WriteReg <= ID_EX_Rt;
        end if;
    end process;

    debug_PC          <= PC;
    debug_Instr       <= IF_ID_Instr;
    debug_ALUResult   <= ALUResult_ex;
    debug_Zero        <= ALUZero_ex;
    debug_ALUCtrl     <= ALUCtrl_ex;
    debug_ALU_InA     <= rs_value_for_alu;
    debug_ALU_InB     <= ALU_input_B;
    debug_SignExtImm <= ID_EX_Imm32;
```



```
1. addi $1, $0, 5
2. addi $2, $0, 10
3. add $3, $1, $2
```

Figure 5: Instruction ran on the normal operation of the processor



```
> [1][31:0]    00000005
> [2][31:0]    0000000a
> [3][31:0]    0000000f
```

Figure 6: Register file after the simulation

```
    debug_RegWrite    <= MEM_WB_RegWrite;

end Behavioral;
```

10 Conclusion

The proposed power-controlled LBIST framework for the MIPS32 processor achieves substantial scan-shift power reduction while preserving test quality. By combining a programmable PLPF bank with WTM-based temporal segmentation, the design lowers average test power by more than fourfold with negligible area overhead and no loss in fault coverage. Validation across simulations and device testing confirms stable performance, reduced IR-drop risk, and smooth integration with existing scan architecture. Overall, the work provides a practical and efficient approach for implementing low-power LBIST in modern pipelined processors.

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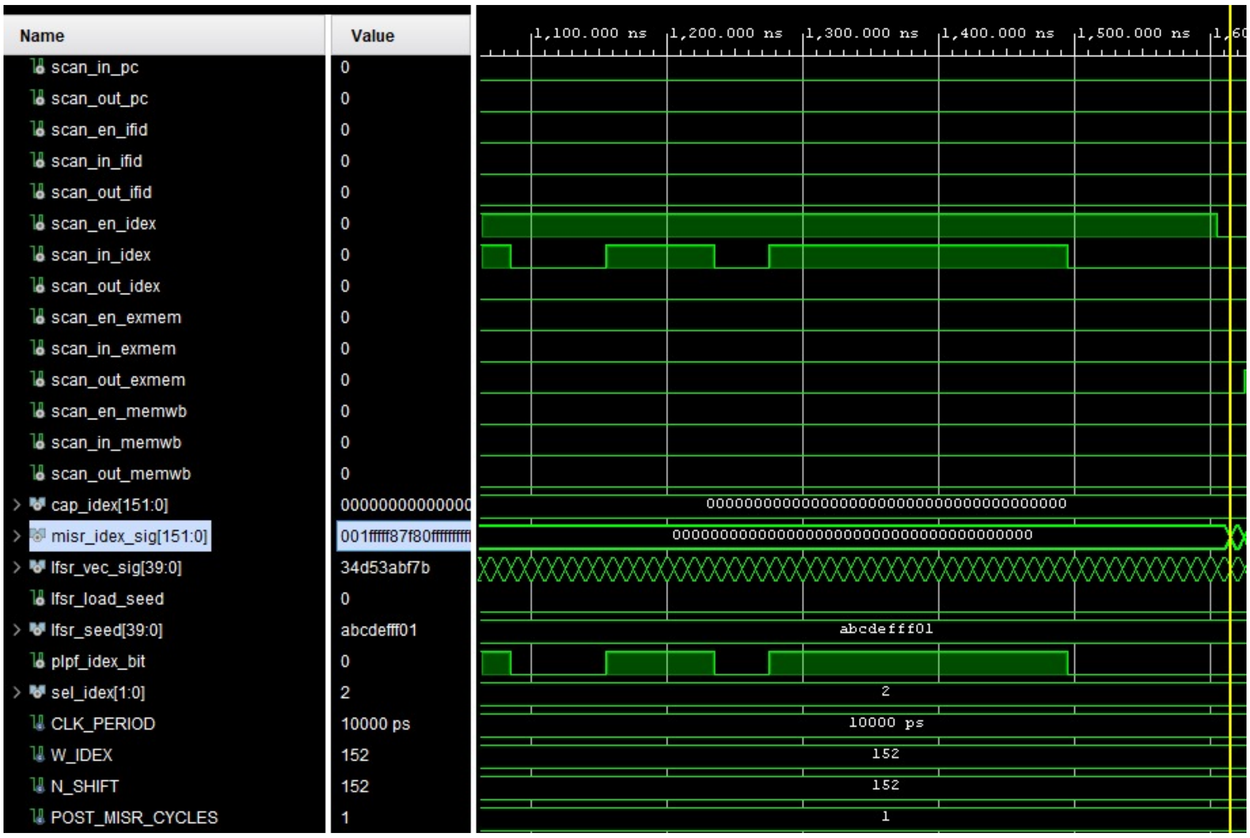

Name	Value
scan_in_pc	0
scan_out_pc	0
scan_en_ifid	0
scan_in_ifid	0
scan_out_ifid	0
scan_en_idex	0
scan_in_idex	0
scan_out_idex	0
scan_en_exmem	0
scan_in_exmem	0
scan_out_exmem	0
scan_en_memwb	0
scan_in_memwb	0
scan_out_memwb	0
cap_idex[151:0]	00000000000000
misr_idex_sig[151:0]	001fffff87f80ffffffffff
lfsr_vec_sig[39:0]	34d53abf7b
lfsr_load_seed	0
lfsr_seed[39:0]	abcdefff01
plpf_idex_bit	0
sel_idex[1:0]	2
CLK_PERIOD	10000 ps
W_IDEX	152
N_SHIFT	152
POST_MISR_CYCLES	1

Figure 7: Testing the integrated MISR and Scan chains timing and control

---

End of Report

Power-Controlled LBIST for MIPS32
November 20, 2025