1. FULL WAVE RECTIFIER WITH & WITHOUT FILTERS

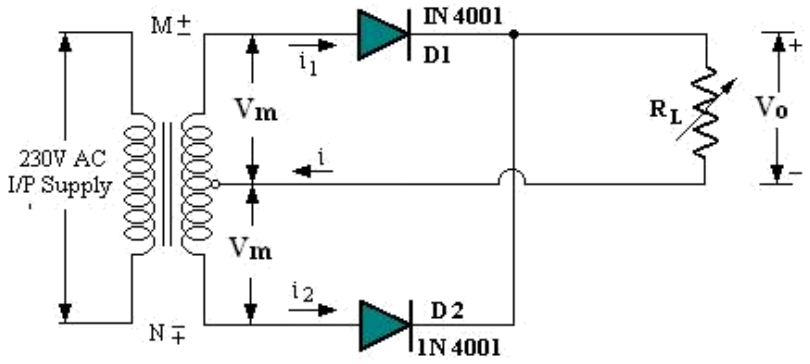
AIM: To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave rectifier center tapped circuit with and without Capacitor filter.

APPARATUS:

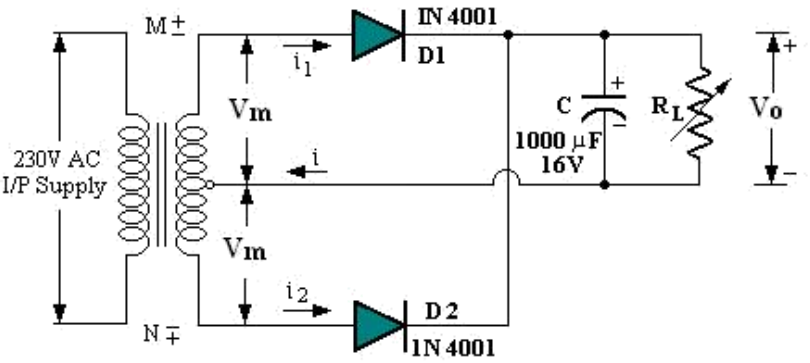
S.No	Name	Range / Value	Quantity
1	Transformer	230V / 9-0-9V	1
2	Diode	1N4001	2
3	Capacitors	1000µF/16V, 470µf/25V	1
4	Decade Resistance Box	-	1
5	Multimeter	-	1
6	Bread Board and connecting wires	-	1
7	Dual Trace CRO	20MHz	1

CIRCUIT DIAGRAMS:

WITHOUT FILTER AND WITH FILTER:



Full-wave Rectifier without filter



Full-wave Rectifier with capacitor filter

THEORY:

A **Rectifier** is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as **rectification**. Physically, rectifiers take a number of forms, including vacuum tube diodes, mercury-arc valves, copper and selenium oxide rectifiers, semiconductor diodes, silicon-controlled rectifiers and other silicon-based semiconductor switches. Because of the alternating nature of the input AC sine wave, the process of rectification alone produces a DC current that, though unidirectional, consists of pulses of current.

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased. The diode D1 conducts and current flows through load resistor RL. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor RL in the same direction. There is a continuous current flow through the load resistor RL, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

PROCEDURE:

WITHOUT FILTER:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance (DRB) and note down no load voltage Vdc ($V_{\text{no load}}$)
6. Connect load resistance at 1KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
7. Calculate ripple factor $= \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of Regulation, $\% = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{no load}}} \times 100\%$

WITH CAPACITOR FILTER:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

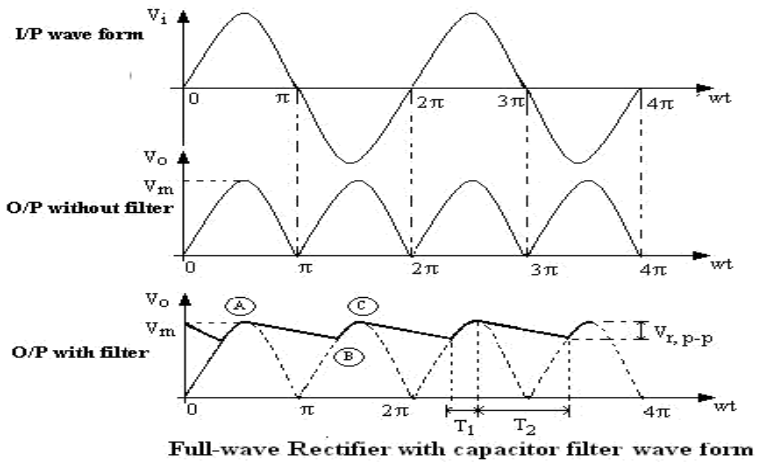
FULL WAVE RECTIFIER WITHOUT CAPACITOR

S.No	R(KΩ)	V_{dc}FL	V**ac**	Γ=V**ac/V$_{dc}$**
1	1	9.65	4.49	0.4652
2	2	9.58	4.47	0.4665
3	3	9.58	4.47	0.4665
4	4	9.59	4.48	0.4671
5	5	9.63	4.50	0.4672
6	6	9.63	4.49	0.4662
7	7	9.65	4.51	0.4663
8	8	9.64	4.51	0.4678
9	9	9.65	4.51	0.4673
10	10	9.64	4.51	0.4678

FULL WAVE RECTIFIER WITH CAPACITOR

S.No	R(KΩ)	V_{dc}FL	V**ac**	Γ=V**ac/V$_{dc}$**
1	1	15.26	0.01	0.000655
2	2	15.22	0.01	0.000634
3	3	15.26	0.01	0.000655
4	4	15.27	0.01	0.000655
5	5	15.26	0.01	0.0006557
6	6	15.25	0.01	0.000658
7	7	15.19	0.01	0.000659
8	8	15.17	0.01	0.0006587
9	9	15.17	0.01	0.000658
10	10	15.19	0.01	0.0006587

WAVE SHAPES:



Full-wave Rectifier with capacitor filter wave form

RESULT: Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full-wave rectifier with and without filter.

WITHOUT FILTER:

Ripple Factor :
Regulation :

WITH CAPACITOR FILTER:

Ripple Factor :
Regulation :

PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

VIVA QUESTIONS:

1. What is a full wave rectifier?
2. How Diode acts as a rectifier?
3. What is the significance of PIV requirement of Diode in full-wave rectifier?
4. Compare capacitor filter with an inductor filter?
5. Draw the o/p wave form without filter? Draw the O/P? What is wave form with filter?
6. What is meant by ripple factor? For a good filter whether ripple factor should be high or low? What happens to the ripple factor if we insert the filter?
7. What is meant by regulation? Why regulation is poor in the case of inductor filter?
8. What is meant by time constant?
9. What happens to the o/p wave form if we increase the capacitor value? What happens if we increase the capacitor value?
10. What is the theoretical maximum value of ripple factor for a full wave rectifier?

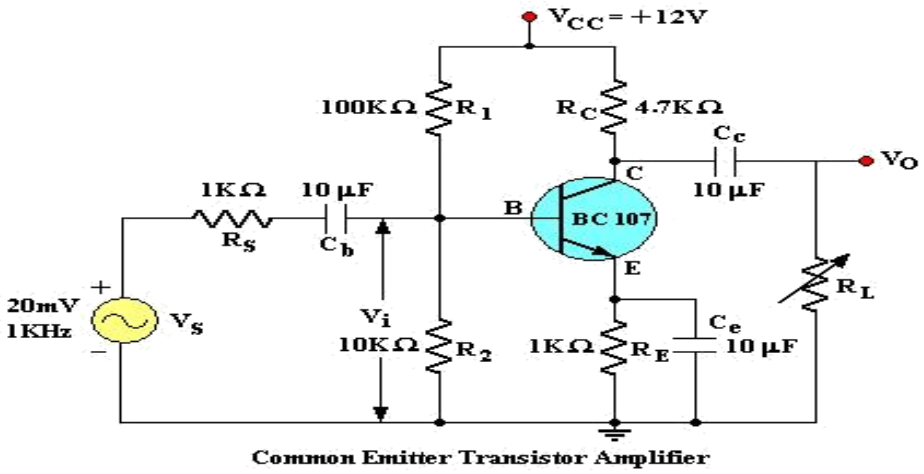
2. COMMON EMITTER AMPLIFIER CHARACTERISTICS

AIM: To Find the frequency response of a Common Emitter Transistor Amplifier and to find the Bandwidth from the Response, Voltage gain, Input Resistance, output resistance.

APPARATUS:

S.No	Name	Range / Value	Quantity
1	Regulated D.C Power supply	0–30 Volts	1
2	Transistor	BC107	1
3	Resistors	1KΩ	2
4	Resistors	100kΩ,10KΩ, 4.7KΩ.	Each 1
5	Capacitors	10µf	3
6	Potentio Meter	--	1
7	Signal Generator	(0 – 1MHz)	1
8	Dual Trace CRO	20MHz	1
9	Bread Board and connecting wires	--	1 Set

CIRCUIT DIAGRAM:-



Common Emitter Transistor Amplifier

THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

PROCEDURE:

1. Connect the circuit as per the Fig.1.,Apply Vcc of 12 Volts DC.

2. Apply I/P Voltage of 20mV at 1KHz from the Signal Generator and observe the O/P on CRO.
3. Vary the frequency from 50 Hz to 1MHz in appropriate steps and note down the corresponding O/P Voltage Vo in a tabular form .
4. Calculate the Voltage Gain Av = Vo/Vs and note down in the tabular form.
5. Plot the frequency (f) Vs Gain (Av) on a Semi-log Graph sheet
6. Draw a horizontal line at 0.707 times Av and note down the cut off points and the Bandwidth is given by B.W = $f_2 - f_1$.

INPUT RESISTANCE RI:

1. Apply I/P Voltage of 20mV at 1KHz from the Signal Generator and observe voltage Vi across R2 on CRO.
2. Without Disturbing the setup note Vi.
3. find Ii = (Vs – Vi) / Rs and Ri= Vi / Ii Ohms.

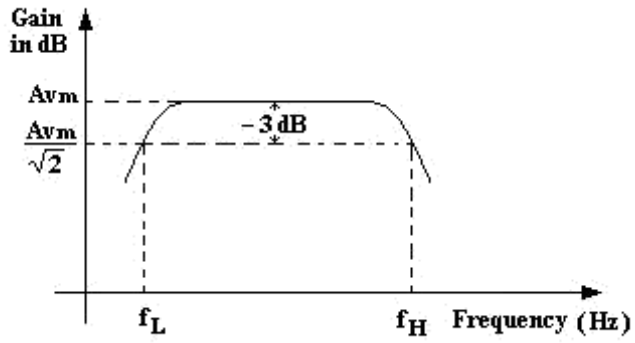
OUTPUT RESISTANCE (R_O):

1. Apply I/P Voltage of 50mV at 1KHz from the Signal Generator and observe the o/p on CRO
2. Connect a Potentio meter across the O/P terminals and without disturbing Vs adjust the potentiometer such that o/p falls to $V_0/2$
3. The Resistance of the potentiometer is equal to Ro.

TABULAR FORMS:

S.No	Frequency (Hz)	O/P Voltage, Vo (V)	Voltage Gain Av =Vo/Vi	Av in dB= 20 log (Av)
1	10	**1.2**	**0.1**	**2**
2	100	**2.2**	**0.83**	**10.75**
3	700	**2.4**	**0.2**	**13.97**
4	1K	**2.4**	**0.2**	**13.97**
5	10K	**2.4**	**0.2**	**13.97**
6	100K	**2**	**0.167**	**10.54**
7	500K	**0.8**	**0.067**	**5.47**
8	1M	**0.4**	**0.033**	**1.45**

MODEL GRAPH:



RESULT:

BandWidth	B.W	$= f_2 - f_1 =$	Hz
Voltage Gain	Av	=	
Input Resistance	Ri	=	ohms
Output Resistance	Ro	=	ohms

PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start
3. All the contacts must be intact

VIVA QUESTIONS:

1. What is an Amplifier?
2. How many types of an Amplifiers?
3. What is meant Band width, Lower cut-off and Upper cut-off frequency?
4. How much phase shift for CE Amplifier?
5. What are the applications?
6. Draw the Equivalent circuit for low frequencies

3.COMMON BASE AMPLIFIER CHARACTERISTICS

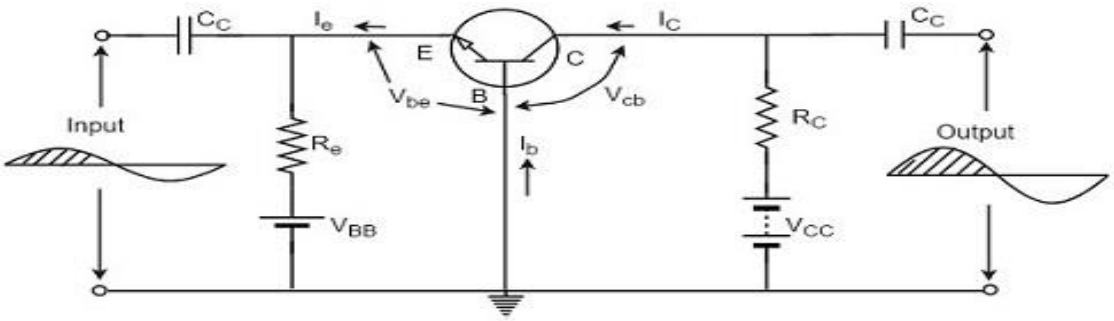
AIM: -

1. Plot the frequency response of a BJT amplifier in common base configuration.
2. Calculate gain.
3. Calculate bandwidth.

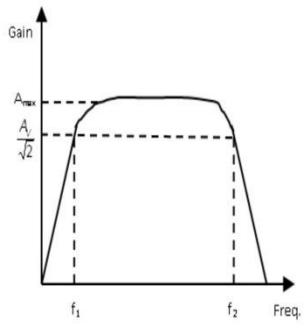
COMPONENTS & EQUIPMENTS REQUIRED: -

S.No	Device	Range/Rating	Qty
1.	(a) DC supply voltage (b) BJT (c) Capacitors (d) Resistors	12V BC10710 10μF 50Ω,10kΩ, 20kΩ	1 1 3 1
2.	Signal generator	0-1MHz	1
3.	CRO	0Hz-20MHz	1
4.	Connecting wires		

CIRCUIT DIAGRAM:



MODEL WAVEFORMS



PROCEDURE: -

1. Connect the circuit diagram as shown in figure for common base amplifier.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV, vary the input signal frequency from 0 to 1MHz in steps as shown in tabular column and note the corresponding output voltages.
4. Find Voltage Gain.
5. Draw a semi log graph for Gain in dB Vs Frequency.

PRECAUTIONS:

1. Avoid loose connections give proper input voltage

TABULAR COLUMN

Frequency (in Hz)	Output Voltage (Vo)	Gain Av=Vo/Vi	Gain(in dB) =20log10(Vo/Vi)
20			
50			
100			
1k			
10k			
100k			
200,500K			
1M			

RESULT: -

Frequency response of BJT in CB mode amplifier is plotted.

Gain = _____dB (maximum).

Bandwidth= fH--fL = _____Hz.

4. COMMON SOURCE AMPLIFIER CHARACTERISTICS

AIM:

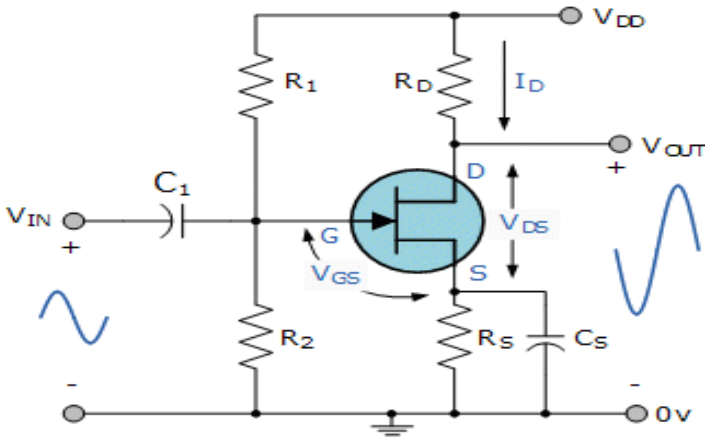
To conduct an experiment on a given JFET and obtain

1) Drain characteristics
2) Transfer Characteristics.
3) To find r_d, g_m, and μ from the characteristics.

APPARATUS:

S.No	Name	Range / Value	Quantity
1	Dual Regulated D.C Power supply	(0–30 Volts)	1
2	JFET	BFW 10 or 11	1
3	D.C Ammeter	(0 – 20mA)	1
4	D.C Voltmeters	(0 – 2V), (0 – 20V)	Each 1
5	Bread Board and connecting wires	--	1 Set

CIRCUIT DIAGRAM:-



THEORY:

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics.

PROCEDURE:

1. Connect the circuit as per the Fig.1,Apply Vdd of 12 Volts DC.
2. Apply I/P Voltage of 20mV at 1KHz from the Signal Generator and observe the O/P on CRO.
3. Vary the frequency from 50 Hz to 1MHz in appropriate steps and note down the corresponding O/P Voltage Vo in a tabular form .
4. Calculate the Voltage Gain Av = Vo/Vs and note down in the tabular form.
5. Plot the frequency (f) Vs Gain (Av) on a Semi-log Graph sheet
6. Draw a horizontal line at 0.707 times Av and note down the cut off points and the Bandwidth is given by B.W = $f_2 - f_1$.

Frequency (in Hz)	Output Voltage (Vo)	Gain Av=Vo/Vi	Gain(in dB) =20log10(Vo/Vi)
20			
50			
100			
1k			
10k			
100k			
200,500K			
1M			

PRECAUTIONS:

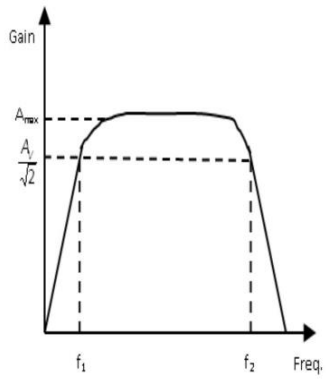
1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before starting the experiment.
3. All the contacts must be intact.
4. For a good JFET I_D will be $\geq$ 11.0 mA at V_{GS} = 0.0 volts if not change the JFET.

RESULT: The characteristics of common source JFET is Verified.

VIVA QUESTIONS:

1. What are the advantages of JFET over BJT?
2. Why input resistance in FET amplifier is more than the BJT amplifier?
3. What is a uni-polar device?
4. What is pinch off voltage?
5. What are various FETs?
6. What is Enhancement mode and Depletion mode?
7. Draw the Equivalent circuit of JFET for low frequencies?
8. Write the mathematical equation for g_m in terms of g_{mo}?
9. Write equation of FET I_D in terms of V_{GS} and V_p?

MODEL WAVEFORMS



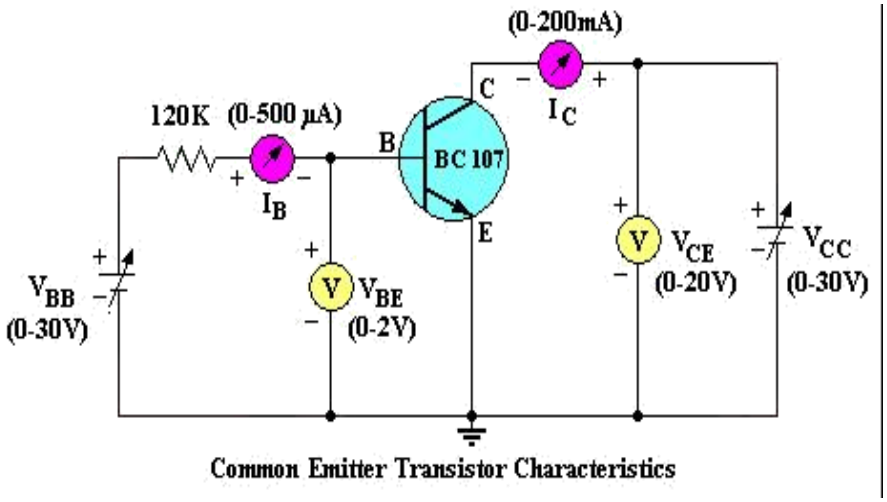
5. MEASUREMENT OF H-PARAMETERS OF TRANSISTOR IN CB,CE,CC CONFIGURATIONS

AIM: To plot the Input and Output characteristics of a transistor connected in Common Emitter Configuration and to find the h – parameters from the characteristics.

APPARATUS:

S.No	Name	Range / Value	Quantity
1	Dual Regulated D.C Power supply	0–30 Volts	1
2	Transistor	BC107	1
3	Resistors	120K□	1
4	DC Ammeters	(0-200□A), (0-200mA)	Each 1 No
5	DC Voltmeters	(0-2V), (0-20V)	Each 1 No
6	Bread Board and connecting wires	-	1 Set

CIRCUIT DIAGRAM:-



Common Emitter Transistor Characteristics

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE . Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B.$$

The transistor always operates in the active region. I.e. the collector current IC increases with V_{CE} very slowly. For low values of the V_{CE} the I_C increases rapidly with a small increase in V_{CE} .The transistor is said to be working in saturation region.

Output resistance is the ratio of change of collector emitter voltage ΔV_{CE} , to change in collector current ΔI_C with constant I_B. Output resistance or Output Impedance

$h_{oe} = \Delta V_{CE} / \Delta I_C$ at IB constant.

Input Impedance $h_{ie} = \Delta V_{BE} / \Delta I_B$ at V_{CE} constant.

Output impedance $h_{oe} = \Delta V_{CE} / \Delta I_C$ at I_B constant.

Reverse Transfer Voltage Gain $h_{re} = \Delta V_{BE} / \Delta V_{CE}$ at I_B constant.

Forward Transfer Current Gain $h_{fe} = \Delta I_C / \Delta I_B$ at constant V_{CE}.

PROCEDURE:

TO FIND THE H – PARAMETERS:

Calculation of h_{ie}:

Mark two points on the Input characteristics for constant V_{CE}. Let the coordinates of these two points be (V_{BE1}, I_{B1}) and (V_{BE2}, I_{B2}).

$$h_{ie} = \frac{VBE2 - VBE1}{I_{B2} - IB1};$$

Calculation of h_{re}:

Draw a horizontal line at some constant I_B value on the Input characteristics. Find VCE2, VCE1, VBE2, VBE1

$$h_{rb} = \frac{VBE2 - VBE1}{VCB2 - VCB1};$$

Calculation of h_{fe}:

Draw a vertical line on the out put characteristics at some constant V_{CE} value. Find

Ic2, Ic1 and IB2, IB1 .

$$h_{fe} = \frac{IC - 2\ I_{C1}}{IB - 2\ I_{B1}};$$

Calculation of h_{oe}:

On the Output characteristics for a constant value of I_B mark two points with coordinates (V_{CE2} , I_{C2}) and (V_{CE1} , I_{C1}) .

$$h_{ob} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}};$$

RESULTS:

h parameters are calculated in CE amplifier.

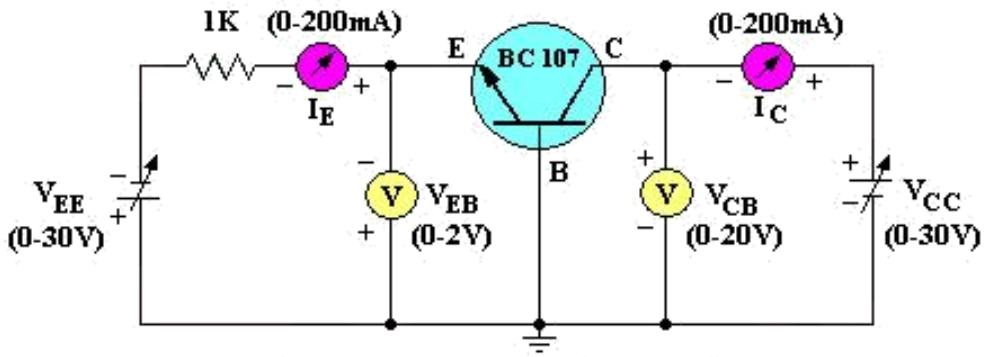
h_{ie}= --------- ohms. h_{re}= ----------

h_{oe}= -------- mhos. h_{fe} = ----------

VIVA QUESTIONS:

1. What is the range of β for the transistor?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. What is the relation between α and β
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration

CIRCUIT DIAGRAMS:



Common Base Transistor Characteristics

THEORY:

A transistor is a three terminal active device. T he terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, IE is +ve, IC is –ve and IB is –ve. So,

$$V_{EB}=f1\ (V_{CB},I_E)\ \text{and}$$

$$I_C=f2\ (V_{CB},I_B)$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases.The current amplification factor of CB configuration is given by,

$$A= \Delta I_C/ \Delta I_E$$

Output resistance is the ratio of change of collector emitter voltage ΔV_{CE} , to change in collector current ΔI_C with constant I_B.

Output resistance or Output impedance $h_{oe} = \Delta V_{CE} / \Delta I_C$ at I_B constant.
Input Impedance $h_{ie} = \Delta V_{BE} / \Delta I_E$ at V_{CB} constant.
Output impedance $h_{oe} = \Delta V_{CB} / \Delta I_C$ at I_E constant.
Reverse Transfer Voltage Gain $h_{re} = \Delta V_{BE} / \Delta V_{CB}$ at I_B constant.
Forward Transfer Current Gain $h_{fe} = \Delta I_C / \Delta I_E$ at constant V

PROCEDURE:

TO FIND THE H – PARAMETERS:

Calculation of h_{ib}:

Mark two points on the Input characteristics for constant V_{CB}. Let the coordinates of these two points be (V_{EB1}, I_{E1}) and (V_{EB2}, I_{E2}).

$$h_{ib} = \frac{VEB2 - VEB1}{IE2 - IE1}$$

Calculation of h_{rb}:

Draw a horizontal line at some constant I_E value on the input characteristics. Find VCB2, VCB1, VEB2, VEB1

$$h_{rb} = \frac{VEB2 - VEB1}{VCB2 - VCB1}$$

Calculation of h_{fb}:

Draw a vertical line on the Output characteristics at some constant V_{CB} value. Find Ic2, Ic1 and IE2, IE1 .

$$h_{fb} = \frac{I_{C2} - I_{C1}}{I_{E2} - I_{E1}}$$

Calculation of h_{ob}:

On the Output characteristics for a constant value of I_E mark two points with coordinates (V_{CB2} , I_{C2}) and (V_{CB1} , I_{C1}) .

$$h_{ob} = \frac{I_{C2} - I_{C1}}{V_{CB2} - V_{CB1}}$$

RESULTS:

h parameters are calculated in CB amplifier.

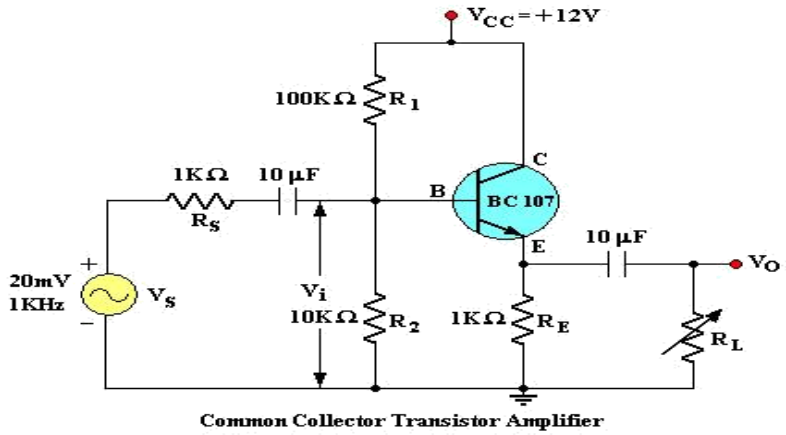
h_{ib}= --------- ohms. h_{rb}= ----------

h_{ob}= -------- mhos. h_{fb} = ----------

VIVA QUESTIONS:

1. What is the range of α for the transistor?
2. Draw the input and output characteristics of the transistor in CB configuration?
3. Identify various regions in output characteristics?
4. What is the relation between α and β?
5. What are the applications of CB configuration?
6. What are the input and output impedances of CB configuration?
7. Define α(alpha)?
8. What is EARLY effect?
9. Draw diagram of CB configuration for PNP transistor?
10. What is the power gain of CB configuration?

CIRCUIT DIAGRAM:-



Common Collector Transistor Amplifier

THEORY:

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation.

This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower.

PROCEDURE:

TO FIND THE H – PARAMETERS:

Calculation of h_{ic}:

$$h_{ic=(Vbc/ib)}$$

Calculation of h_{re}:

$$h_{re=(Vbc/Vec)}$$

Calculation of h_{fe}:

$$h_{fe} = \frac{I e}{Ib};$$

Calculation of h_{oe}:

$$h_{ob} = \frac{Ie}{---};$$

V_{ec}

RESULTS:

h parameters are calculated in CC amplifier.

h_{ic}= --------- ohms. h_{re}= ----------

h_{ob}= -------- mhos. H_{fe} = ----------

6. INPUT AND OUTPUT CHARACTERISTICS OF FET IN CS CONFIGURATION

AIM:

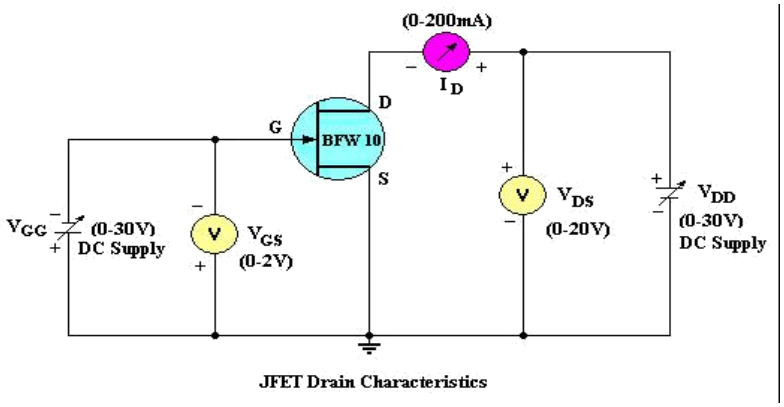
To conduct an experiment on a given JFET and obtain

1. Drain characteristics
2. Transfer Characteristics.
3. To find r_d, g_m, and μ from the characteristics.

APPARATUS:

S.No	Name	Range / Value	Quantity
1	Dual Regulated D.C Power supply	(0–30 Volts)	1
2	JFET	BFW 10 or 11	1
3	D.C Ammeter	(0 – 20mA)	1
4	D.C Voltmeters	(0 – 2V), (0 – 20V)	Each 1
5	Bread Board and connecting wires	--	1 Set

CIRCUIT DIAGRAM:-



JFET Drain Characteristics

THEORY:

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics.

PROCEDURE:

DRAIN CHARACTERISTICS:

1. Connect the circuit as per the Fig. 1 and start with V_{GG} and V_{DD} keeping at zero volts.
2. Keep V_{GG} such that V_{GS} = 0 volts, Now vary V_{DD} such that V_{DS} Varies in steps of 1 volt up to 10 volts. And Note down the corresponding Drain current I_D
3. Repeat the above experiment with V_{GS} = -1V and -2V and tabulate the readings.
4. Draw a graph V_{DS} Vs I_D against V_{GS} as parameter on graph.
5. From the above graph calculate r_d and note down the corresponding diode current against the voltage in the tabular form.
6. Draw the graph between voltages across the Diode Vs Current through the diode in the first quadrant as shown in fig.

TRANSFER CHARACTERISTICS:

1. Set V_{GG} and V_{DD} at zero volts .keep V_{DS} = 1Volt.
2. Vary V_{GG} such that V_{GS} varies in steps of 0.5 volts. Note down the corresponding Drain current I_D, until I_D = 0mA and Tabulate the readings.
3. Repeat the above experiment for V_{DS} = 3.0 Volts and 5.0 Volts and tabulate the readings.
4. Draw graph between V_{GS} Vs I_D with V_{DS} as parameter.
5. From the graph find g_m.
6. Now $\mu = g_m \times r_d$.

TABULAR FORM:

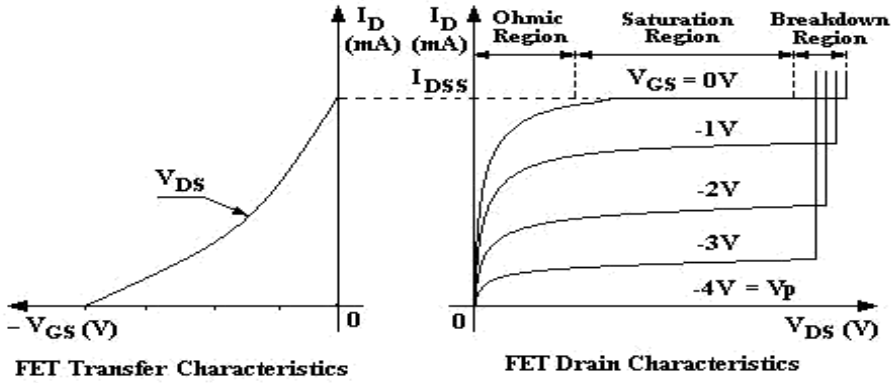
DRAIN CHARACTERISTICS:

S.No	V_{DS} (V)	V_{GS} = 0 volts I_D (mA)	V_{GS} = -1V I_D (mA)	V_{GS} = -2V I_D (mA)
1	0.0			
2	0.5			
3	1.0			
4	1.5			
5	2.0			
6	2.5			
7	3.0			
8	3.5			

TRANSFER CHARACTERISTICS:

S.No	V_{GS} (V)	V_{DS} = 1.0V I_D (mA)	V_{DS} = 3.0V I_D (mA)	V_{DS} = 5.0V I_D (mA)
1	0.0			
2	0.5			
3	1.0			
4	1.5			
5	2.0			

MODEL GRAPH:



CALCULATIONS:

CALCULATION OF r_d :

Construct a Triangle on one of the output characteristic for a particular V_{GS} in the active region and find ΔV_{DS} and ΔI_D

Now $\mathbf{r_d} = \Delta V_{DS} / \Delta I_D$ (V_{GS} = constant)

CALCULATION OF g_m :

Construct a Triangle on one of the Transfer characteristics for a particular V_{DS} find ΔV_{GS} and ΔI_D.

Now $\mathbf{g_m} = \Delta I_D / \Delta V_{GS}$ (V_{DS} = constant).

CALCULATION OF μ :

$\mu = g_m * r_d$.

RESULT: The characteristics of common source JFET is Verified.

PRECAUTIONS:

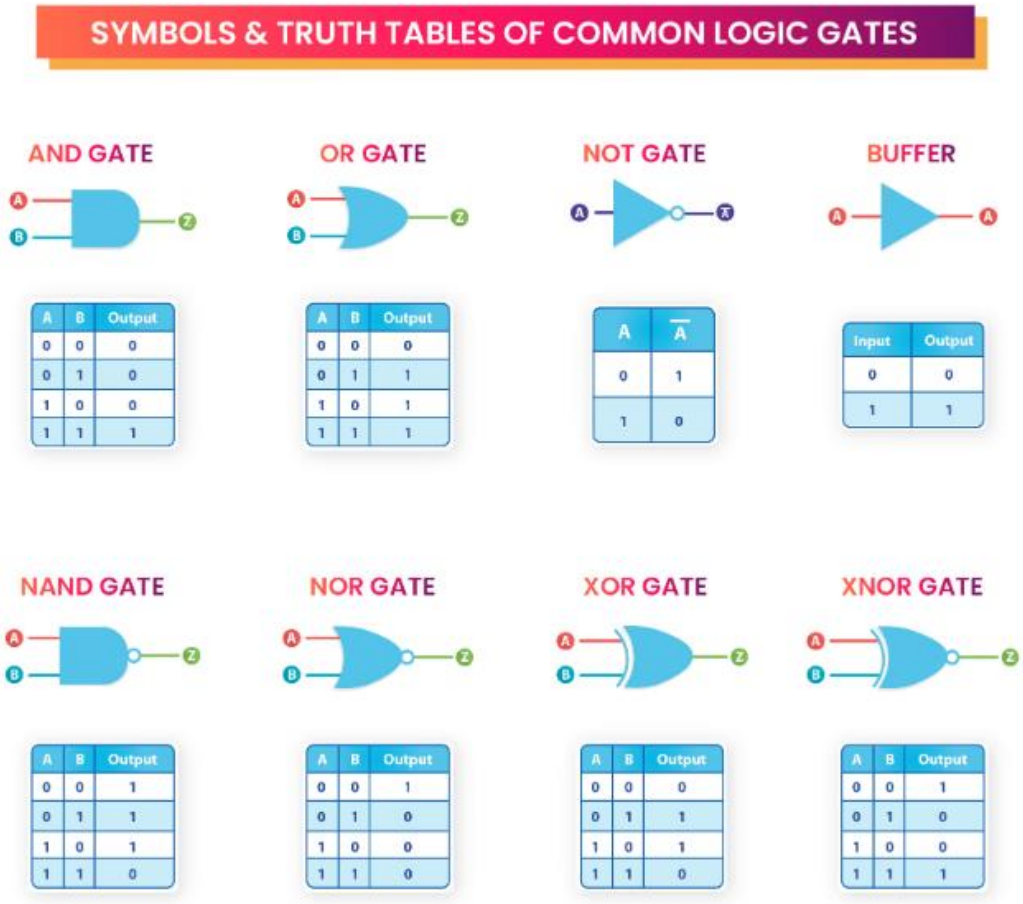
1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before starting the experiment.
3. All the contacts must be intact.
4. For a good JFET I_D will be $\geq$ 11.0 mA at V_{GS} = 0.0 volts if not change the JFET.

VIVA QUESTIONS:

1. What are the advantages of JFET over BJT?
2. Why input resistance in FET amplifier is more than the BJT amplifier?
3. What is a uni-polar device?
4. What is pinch off voltage?
5. What are various FETs?
6. What is Enhancement mode and Depletion mode?
7. Draw the Equivalent circuit of JFET for low frequencies?
8. Write the mathematical equation for g_m in terms of g_{mo}?
9. Write equation of FET I_D in terms of V_{GS} and V_p?

7.REALIZATION OF BOOLEAN EXPRESSIONS USING GATES

AIM: Realization of Boolean expressions by using logic gates.
Apparatus Required: IC 7420, Trainer kit, Connecting wires, patch cards.



IC No.	Specification
IC 7400	NAND Gate (2-input)
IC 7402	NOR Gate (2-input)
IC 7404	NOT Gate
IC 7408	AND Gate (2-input)
IC 7410	NAND Gate(3-input)
IC 7420	NAND Gate(4-input)
IC 7432	OR Gate (2-input)
IC 7486	EX-OR Gate (2-input)

PROCEDURE:

PART (A):

1. Supply connections are given at the corresponding pins of ICs.
2. Each IC is taken separately and the individual gates in each IC are tested by giving inputs and the truth tables are verified.
3. Same procedure is repeated for all ICs.

PART (B):

1. Connect the circuit as per the given expression
   I. $F=(x+y)^1+y$

   II. $F=(xy)^1+x$

   III. $F=(xy^1+x^1y)$

   IV. $F=(xy^1+x^1y)^1$

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins

RESULT:

The truth tables of individual gates are verified and the given Boolean expressions are realized by using gates.

SAMPLE QUESTIONS:

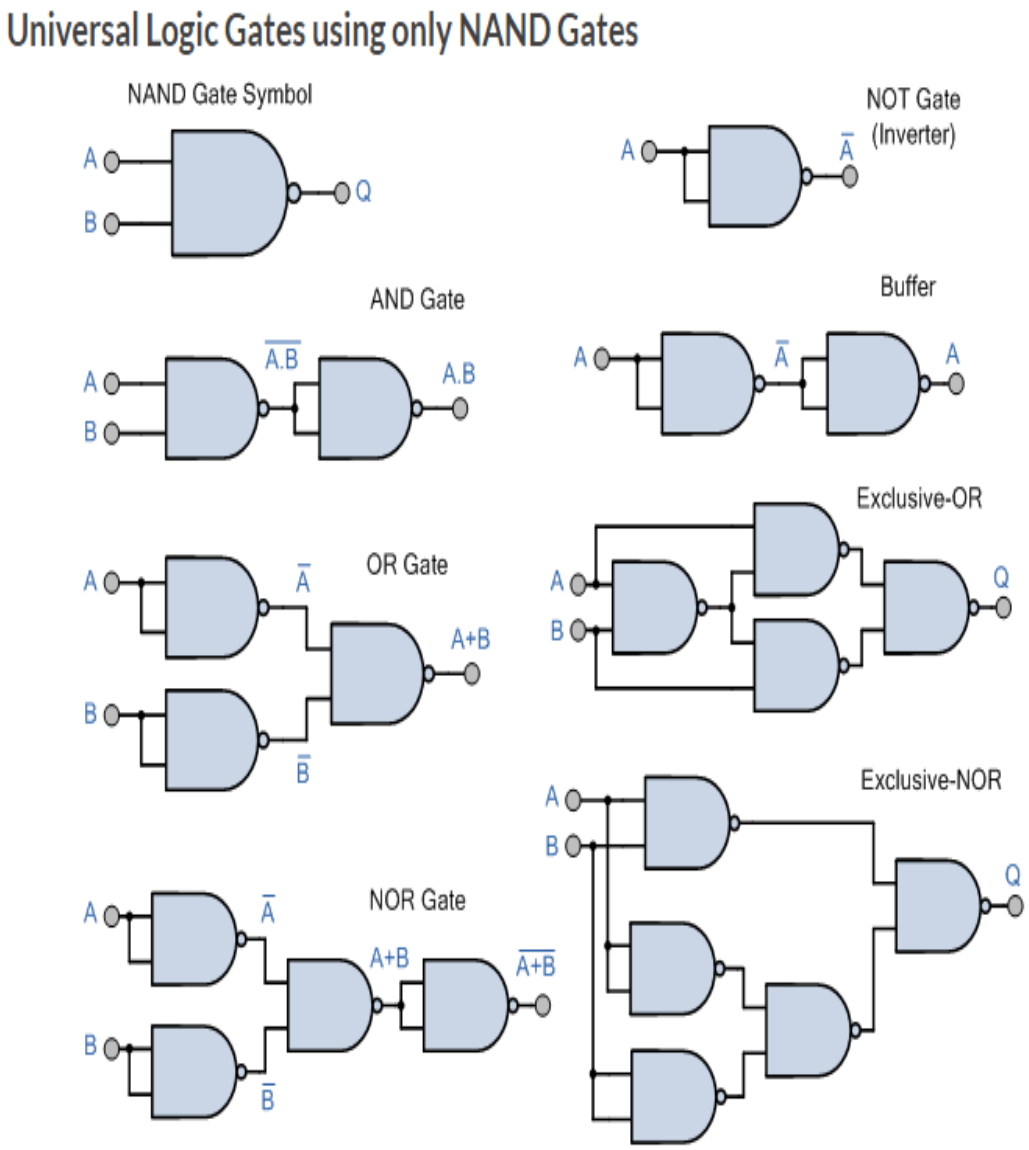
1. Which logic gate gives the ouput logic high when if any one of input is high.
2. Which logic gate gives the ouput logic 0 when if any one of input is high.
3. Which logic gate gives the ouput logic high when both the inputs given as same.

8.DESIGN AND REALIZATION OF LOGIC GATES USING UNIVERSAL GATES

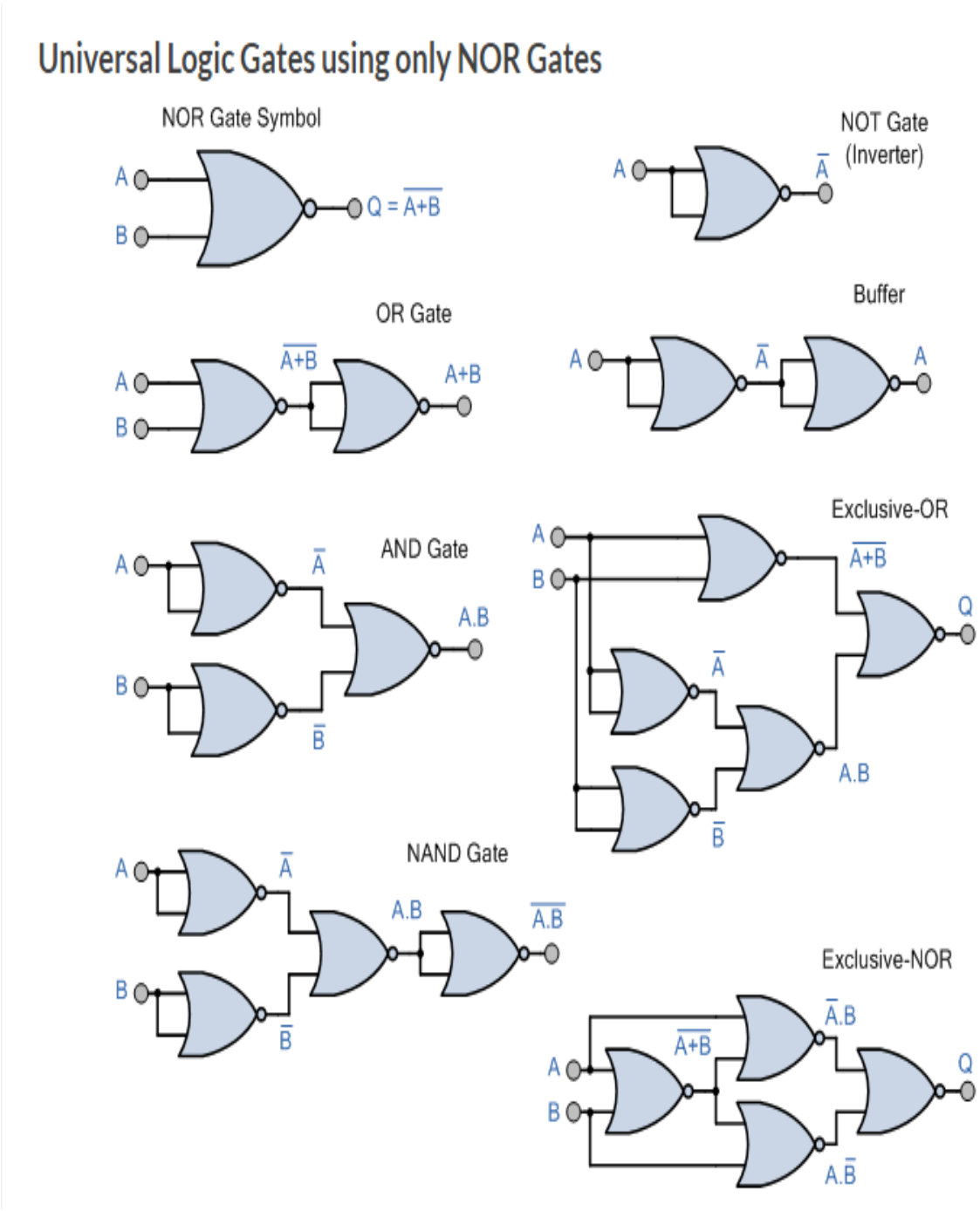
AIM: To verify NAND and NOR as universal gates

APPARATUS REQUIRED: IC 7420, Trainer kit, Connecting wires, patch cards.

REALIZATION OF LOGIC GATES OPERATIONS USING NAND GATES:



REALIZATION OF LOGIC GATES OPERATIONS USING NOR GATE:



PROCEDURE:

PART (A):

1. Supply connections are given at the corresponding pins of ICs.
2. Each IC is taken separately and the individual gates in each IC are tested by giving inputs and the truth tables are verified.
3. Same procedure is repeated for all ICs.

PART (B):

1. Supply connections are given at the corresponding pins of ICs.
2. For realization of individual gates using NAND gates alone, the connections are made as per the logic diagrams.
3. Inputs are given and the truth tables of individual gates are verified.
4. The same procedure is repeated for realization of individual gates using NOR gates.

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

RESULT:

The truth tables of individual gates are verified and their realizations using NAND gates alone and NOR gates alone have been verified.

SAMPLE QUESTIONS:

1. If one of the inputs of an EX-OR gate is *high,* its output will be--------
2. The number of rows in a truth table of 4 variables are----------.
3. A 3 input NOR gate is required to detect the simultaneous occurrence of all the inputs in the LOW state. Its output is----------(active low /active-high).
4. The minimum number of bits required to distinguish 108 distinct objects is--------.
5. What is the difference between a positive logic system and negative logic system?
6. What are universal gates? Why that name?
7. Minimum number of NAND gates necessary to realize EX-OR gate using NAND gates only is ------.
8. Minimum number of NOR gates necessary to realize EX-OR gate using NOR gates only is

9.GENERATION OF CLOCK USING NAND / NOR GATES

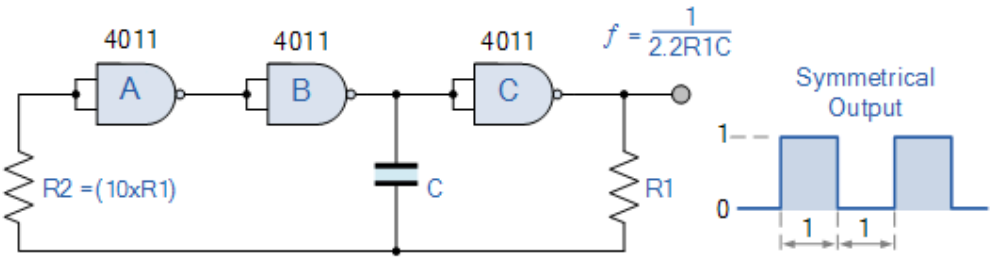
AIM: To Study and implement the generation of clock using NAND/NOR gates

APPARATUS:-

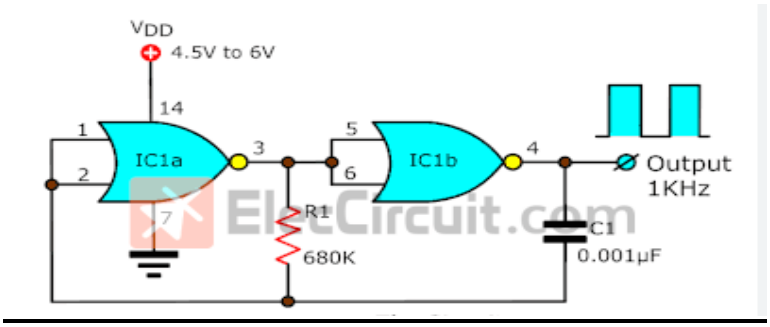
1) Trainer kit
2) Patch chords
3) CRO
4) Power supply

CIRCUIT DIAGRAM:-

GENERATION OF CLOCK USING NAND GATES:



GENERATION OF CLOCK USING NOR GATES



PROCEDURE:-

1) Connect the power chord to the mains power supply
2) Turn on the trainer kit you can observe the led indication on the kit.
3) Now connect the CRO probe in channel '1' to the NAND gate and connect the positive to the output of the circuit and negative to the ground.
4) Observe the waveform on the CRO and note down the waveform time period and amplitude of the signal.
5) Plot the graph for the above readings.

- The above steps repeated for the NOR gate also.

RESULT:

Hence, the generation of clock using NAND/NOR gates are studied and implemented.

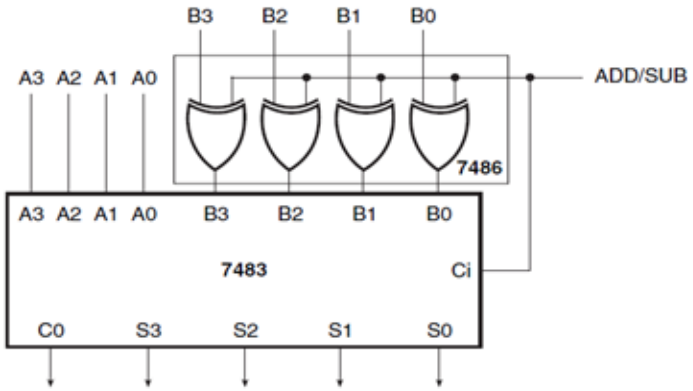
10. DESIGN A 4 – BIT ADDER / SUBTRACTOR

AIM: To study and implement the 4 bit Adder/Subtractor

APPARATUS:

1. Trainer kits
2. Patch cards
3. Power supply

CIRCUIT DIAGRAM:



Adder–subtractor circuit

THEORY

IC type 7483 is a 4-bit binary parallel adder. It has two 4-bit inputs. Each input consists of 4-bits.The input A consists of A4 , A3 , A2 and A1 whereas input B consists of B4 , B3 , B2 and B1. It Has four sum outputs consisting of S4 , S3 , S2 and S1. C0 is the input carry and C4 output carry.The Vcc is at pin 5 and GND is at pin 12.

PROCEDURE

1. Connect the Digital Logic Trainer to 220V AC power supply
2. Turn on the trainer and verify the voltage of the power supply using the multi-meter. It should be exactly +5V.
3. Insert the IC 74LS83 on the trainer's breadboard
4. Develop the circuit according to the figure
5. Connect , A3 , A2 ,A1and A0 of input A to logic switches and mark them carefully.
6. Connect B3 , B2 , B1 and B0 of input B to logic switches and mark them carefully.
7. Connect carry in to ground.
8. Connect S3 , S2 , S1 and S0 of output S to LEDs .
9. Connect Carry out to the other LED and marks all outputs.
10. Connect Vcc of all IC's to the +5V available in the trainer.
11. Connect GND of all IC's to the ground available in the trainer.
12. Now change the values of inputs A and B, and observe the output.

RESULT: Hence the 4bit adder/subtractor is implemented.

4 BIT ADDER

INPUTS								OUTPUT				
A3	A2	A1	A0	B3	B2	B1	B0	COUT	S3	S2	S1	S0

4 BIT SUBTRACTOR

INPUTS								OUTPUT				
A3	A2	A1	A0	B3	B2	B1	B0	BOUT	S3	S2	S1	S0

11. DESIGN AND REALIZATION A SYNCHRONOUS AND ASYNCHRONOUS COUNTER USING FLIP-FLOPS

AIM: Design and realization a synchronous and asynchronous counter using flip flops.

APPARATUS:

1. Trainer kits
2. Patch cards
3. Power supply

THEORY:

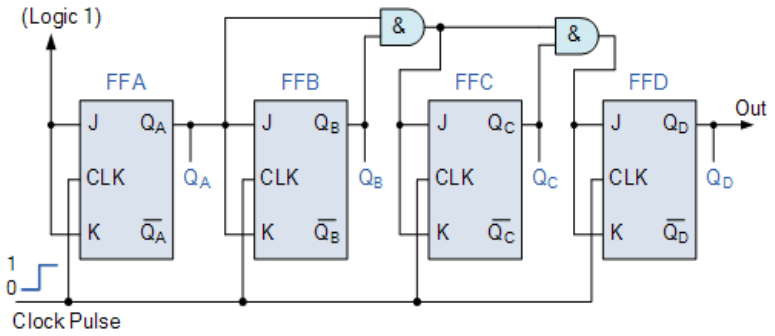
Synchronous and asynchronous counters are two primary types of digital counters, differing primarily in how their flip-flops are clocked. Synchronous counters use a common clock signal to trigger all flip-flops simultaneously, while asynchronous (or ripple) counters clock each flip-flop sequentially, with the output of one flip-flop triggering the next.

PROCEDURE:

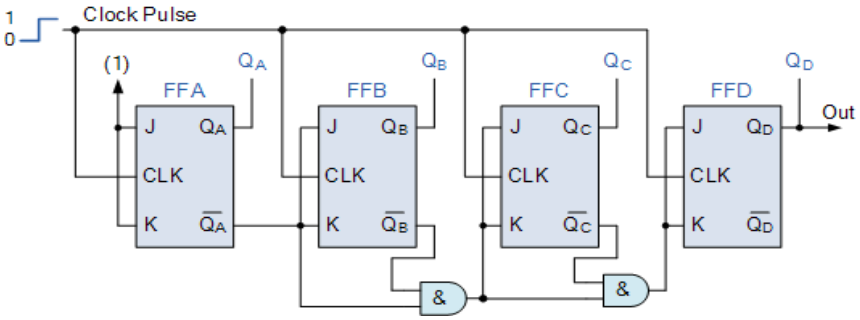
1. Power supply connections are made for the two separate 7476 ICs.
2. The preset and clear pins of all flip-flops are disabled by connecting to HIGH for normal operation of flip- flops and all JK inputs to 1(Vcc or HIGH)
3. All connections are made as per the circuit diagram. For UP counter operation (0000 to 1111), the Q output of LSB flip-flop (to which clock of 1 Hz is applied) is connected as clock input for next higher significant bit flip- flop and so on. For DOWN counter operation(1111 to 0000), the Q' outputs are connected as clock input for next significant flip-flops.
4. The Q outputs of all four flip- flops are connected to 4 output indicators for showing the count.
5. Apply clock input from pulser (press push button in the pulser and release it to produce a single pulse) and verify the count and also counter operation. You can also give clock input of low frequency from clock generator(about 1 Hz).

CIRCUIT DIAGRAM

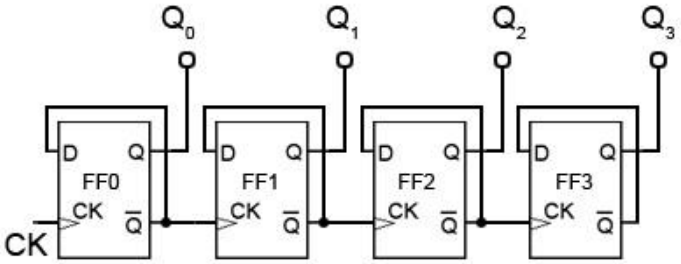
BINARY 4-BIT SYNCHRONOUS UP COUNTER:



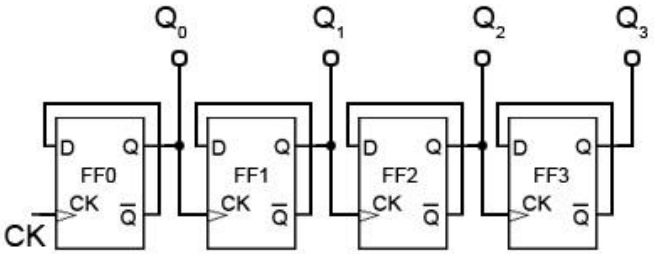
BINARY 4-BIT SYNCHRONOUS DOWN COUNTER:



BINARY 4-BIT ASYNCHRONOUS UP COUNTER:



BINARY 4-BIT SYNCHRONOUS DOWN COUNTER:



PRECAUTIONS:

1. No pins must be left open. If we are not using particular pins in that application, disable those pins.
2. Care has to be taken in identifying the LSB and MSBs.
2. Avoid loose connections and shorting of pins.

RESULT:

The 4- bit synchronous and Asynchronous UP/DOWN counters constructed and their operation is verified.

SYNCHRONOUS/ASYNCHRONOUS UP COUNTER

CK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

SYNCHRONOUS/ASYNCHRONOUS DOWN COUNTER

CLK	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

EXPERMENT 12
REALIZATION OF LOGIC GATES USING DTL,TTL,ECL,ETC.

AIM: Realization of logic gates using DTL,TTL,ECL,etc.

EQUIPMENTS: IC 7420, Trainer kit, Connecting wires, patch cards.

THEORY:

DTL (Diode-Transistor Logic), TTL (Transistor-Transistor Logic), and CMOS (Complementary Metal-Oxide Semiconductor) are different logic families used in digital circuits. DTL utilizes diodes and transistors, TTL relies solely on transistors in saturation mode, and CMOS uses complementary MOSFETs. DTL is faster than RTL but slower than TTL, while CMOS offers high speed and low power consumption.

CIRCUIT DIAGRAM:

- **The basic DTL Inverter/NOT gate**

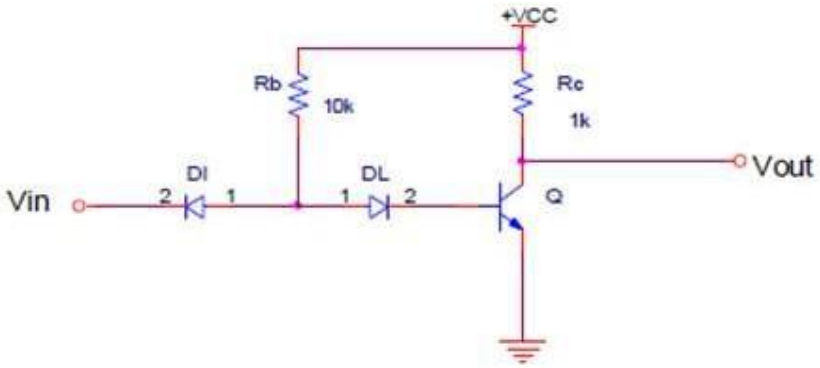


Figure 1: The DTL inverter

- **The NAND gate**

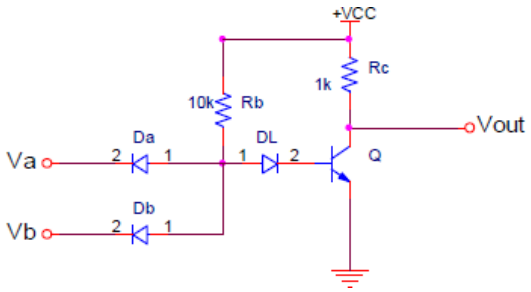


Fig 2:The DTL NAND GATE

❖ **The NOR gate**

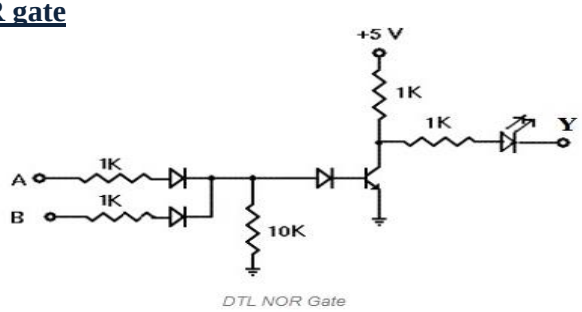


Fig 3:The DTL NOR GATE

❖ **The Basic TTL Inverter**

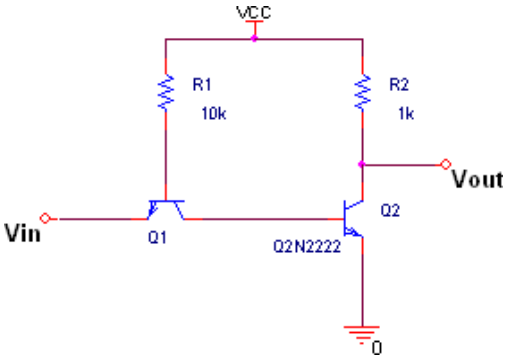


FIG.4 :THE TTL INVERTER

❖ **The TTL NAND Gate**

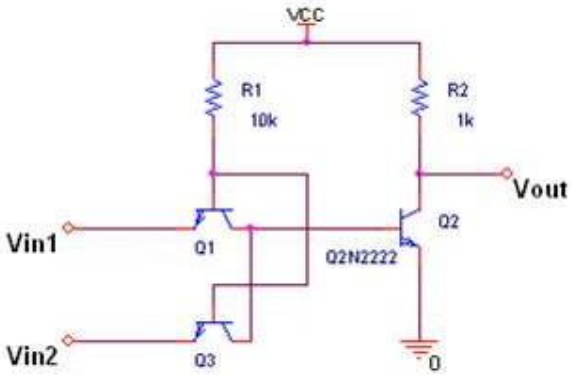


FIG 5: TWO INPUT TTL NAND GATE

❖ **The NOR Gate**

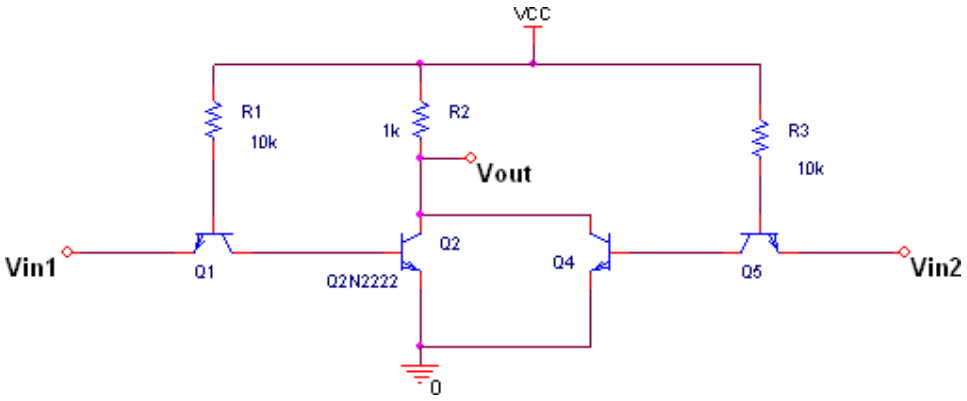


FIG 6:. TWO-INPUT TTL NOR GATE

❖ **THE ECL NOT/INVERTER GATE**

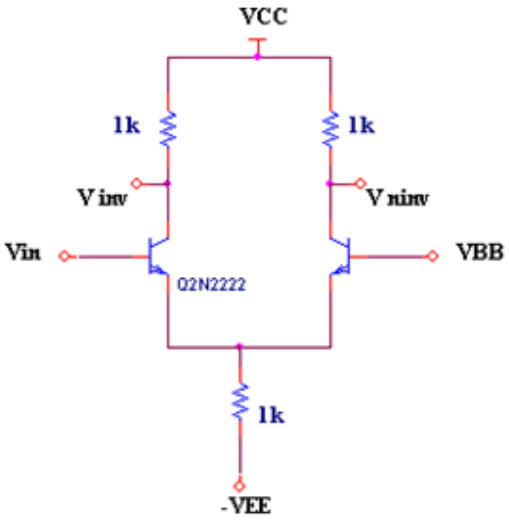


FIG 7: THE ECL NOT/INVERTER GATE

❖ **ECL NOR/OR Gate**

By adding additional input transistors with coupled collectors and coupled emitters to the ECL current switch, the inverting output becomes a NOR outputs and the non-inverting output becomes an OR output.

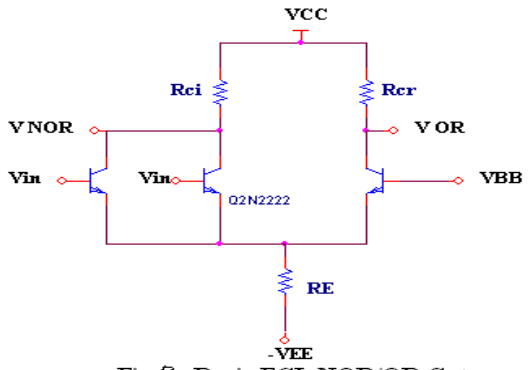
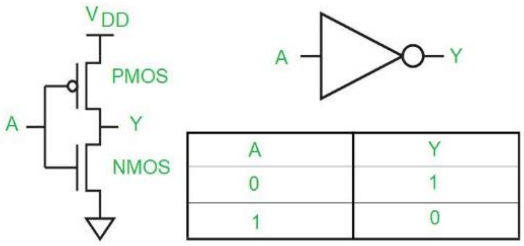
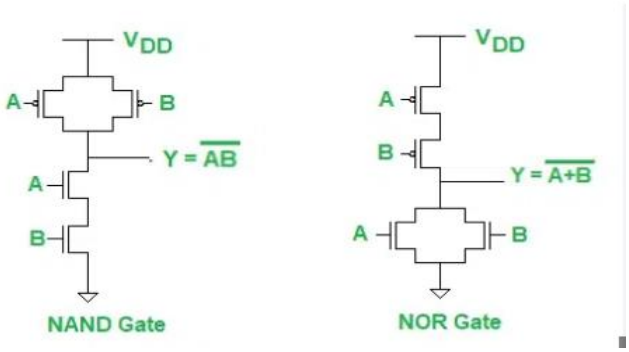


Fig 8 , Basic ECL NOR/OR Gate

CMOS NOT /INVERTER GATE



CMOS NAND /NOR GATES GATE



RESULT: Hence, Realized logic gates using DTL,TTL,ECL,etc

LEAD EXPERIMENTS

ZENER DIODE CHARACTERISTICS AND ZENER AS VOLTAGE REGULATOR

AIM: 1.To observe and draw the V-I characteristics and Regulation characteristics of a Zener diode.

2.To find the Zener Breakdown voltage in reverse biased condition.

APPARATUS:

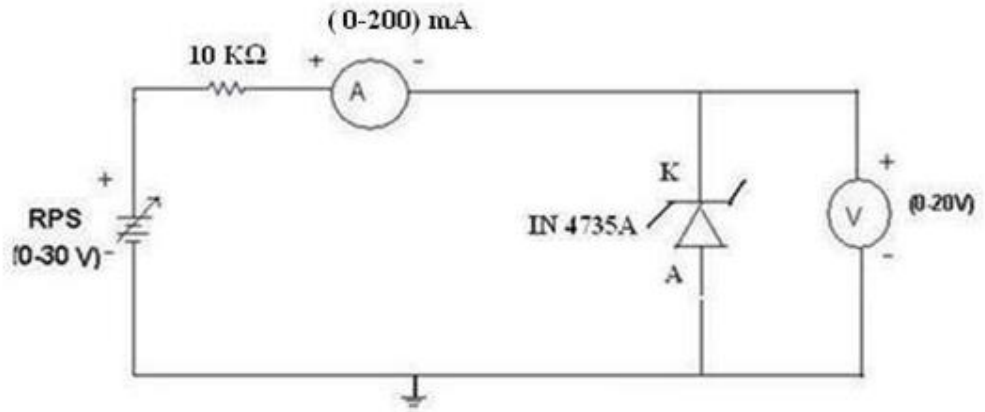
S.No	Name of the Apparatus	Range	Quantity
1	Zener Diode(IN 4735A)		1
2	Resistors	1KΩ, 10KΩ	1
3	Regulated Power Supply	(0-30)VDC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)VDC	1
7	Connecting Wires	As Required	

THEORY:

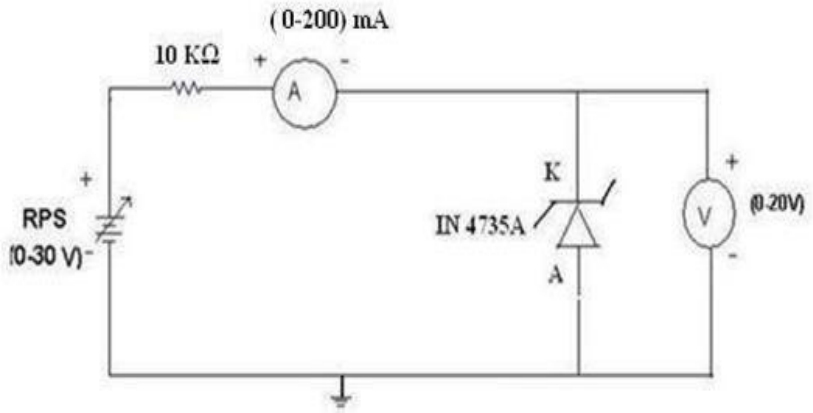
A zener diode is heavily doped p-n junction diode, specially made to operate in the breakdown region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Breakdown Voltage. High current through the diode can permanently damage the device To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it,i.e.it has very lowd ynamic resistance.It isused in voltage regulators

CIRCUIT DIAGRAM:

(i) V-I CHARACTERISTICS:



II) REGULATION CHARACTERISTICS



PROCEDURE:

(i) V-I CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The zener current(lz),and the zener voltage(Vz.)are observed and then noted in the tabular form.
4. A graph is plotted between zener current (Iz) on y-axis and zener voltage (Vz) on x-axis.

II) REGULATION CHARACTERISTICS

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased insteps.
3. The voltage across the diode(Vz.)remains almost constant although the current through the diode increases. This voltage serves as reference voltage.
4. The zener current(lz),and the zener voltage(Vz.)are observed and then noted in the tabular form.
5. Agraph is plot ted between zener current(Iz)on y-axis and zener voltage(Vz) on x-axis.

OBSERVATIONS:

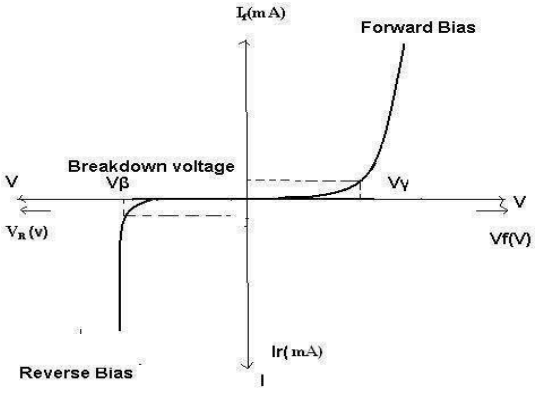
(i) V-I CHARACTERISTICS:

S.No	ZenerVoltage(VZ) (volts)	ZenerCurrent(IZ)(m A)

(ii) REGULATION CHARACTERISTICS:

S.No	ZenerVoltage(VZ) (volts)	ZenerCurrent(IZ)(m A)

V-I& REGULATIONCHARACTERISTICS



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the zener diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULT:

Hence, observed and drawn the V-I characteristics and Regulation characteristics of a Zener diode.&observed the Zener Breakdown voltage in reverse biased condition.

2. DESIGN & REALIZATION OF 8*1 MULTIPLEXER USING 4*1 MULTIPLEXER

AIM: To Design & Realization of 8*1 multiplexer using 4*1 multiplexer.

APPARATUS: IC 7420, Trainer kit, Connecting wires, patch cards

THEORY:

An 8:1 multiplexer (MUX) can be built using two 4:1 MUXs. The key is to use one 4:1 MUX for inputs 0-3 and the other for inputs 4-7. The selection lines (S1, S0) control which of these two 4:1 MUXs is active, effectively selecting one of the eight inputs.

BLOCK DIAGRAM:

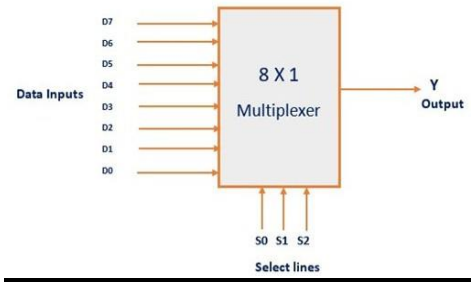


Fig :8*1 MUX block diagram

INPUTS			OUTPUTS
S0	***S1***	***S2***	***Y***
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Table: Truth Table of 8:1MUX

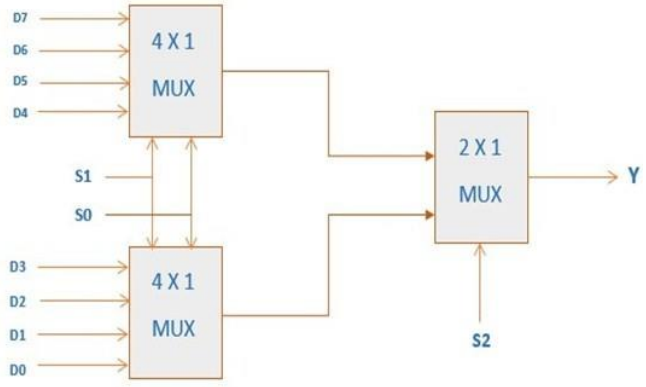


FIG: Realization of 8*1 multiplexer using 4*1 multiplexer

PROCEDURE:

1. Connect the power chord to the mains power supply
2. Turn on the trainer kit you can observe the led indication on the kit.
3. connect the circuit as per the given 58diagram
4. Observe the outputs on LED s and verify the truth table

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

RESULT:

Hence, Realized 8*1 multiplexer using 4*1 multiplexe

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