📘 **Day 15 Topic: Verilog codes for T Latch Using Cadence (Xcelium)**

🔹 What is a Latch?

A latch is the simplest form of a memory element in digital electronics.

- It can store 1 bit of data.
- It is level-sensitive → works as long as the Enable (or Clock) input is active.
- Unlike flip-flops (which are edge-triggered), latches are transparent when enabled.

T Latch (Toggle Latch) Description

A T latch (Toggle latch) is a type of sequential logic circuit. It is derived from the JK latch by connecting both the J and K inputs together and calling this single input T (Toggle input).

- T = 0 → No Change (latch holds its previous state)
- T = 1 → Output toggles (changes to the opposite of the present state)

That's why it is called a "toggle latch."

Inputs and Outputs

- Input:
    - T (Toggle input) – the main control input
    - Enable (CLK or Gate signal) – controls when the latch can change state
- Output:
    - Q (main output)
    - Q' (complement of Q)

Working

1. When Enable = 0 (Latch disabled):
    - The output Q does not change, it remembers the previous state (latched).

2. When Enable = 1 (Latch enabled):
    - If T = 0 → Q remains the same (no change).
    - If T = 1 → Q toggles (switches from 0 to 1 or from 1 to 0).

Truth Table

Enable	T	Next State (Q^{n+1})
0	X	Q^n (no change)
1	0	Q^n (no change)
1	1	$\bar{Q}^n$ (toggle)

Circuit

- It is usually built using JK latch with J = K = T.
- Can also be implemented using D latch, by connecting D = T ⊕ Q (XOR gate).

🔹 **1.1) Design Code**

t_latch.v

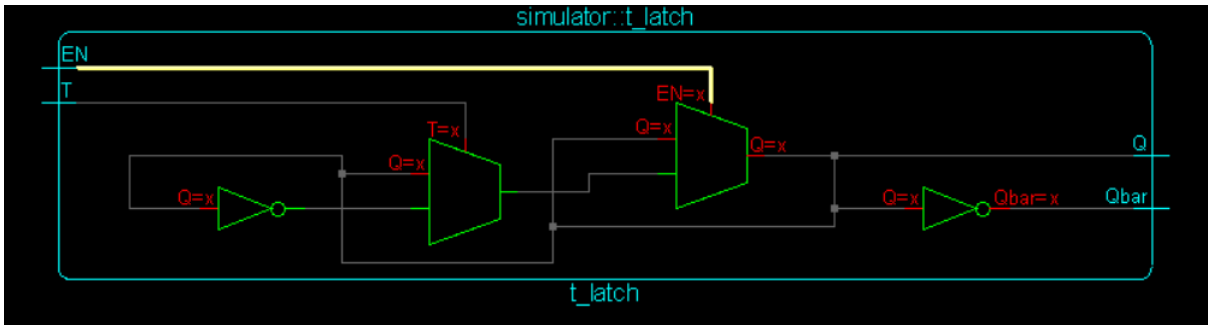
```
// T Latch (Level Sensitive)
module t_latch (
    input wire T, EN,
    output reg Q,
    output wire Qbar
);

    assign Qbar = ~Q;

    always @(*) begin
        if (EN) begin
            if (T)
                Q <= ~Q; // Toggle
            else
                Q <= Q;  // Hold
        end
        else
            Q <= Q;      // Hold
    end
endmodule
```

1.2) Test Bench Code

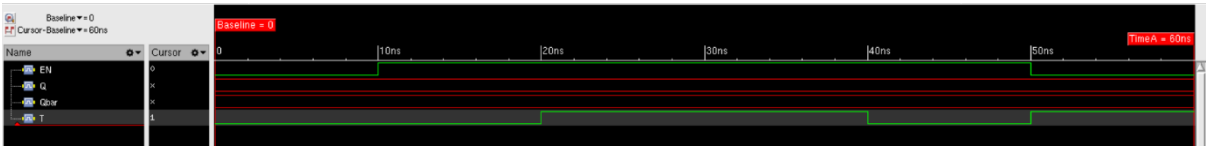
tb.v

```
module tb_t_latch;
    reg T, EN;
    wire Q, Qbar;

    // Instantiate T Latch
    t_latch uut (.T(T), .EN(EN), .Q(Q), .Qbar(Qbar));

    initial begin
        $monitor("T=%0t | EN=%b T=%b | Q=%b Qbar=%b", $time, EN, T, Q, Qbar);

        // Start with EN=0 (Latch disabled)
        EN=0; T=0; #10;

        // Enable latch and test
        EN=1; T=0; #10; // Hold
        EN=1; T=1; #10; // Toggle
        EN=1; T=1; #10; // Toggle again
        EN=1; T=0; #10; // Hold
        EN=0; T=1; #10; // Hold (EN=0)

        $finish;
    end
endmodule
```

1.3) Schematic



1.4) Wave Forms



Applications

- Counters: T latch is the basic building block of binary counters, since toggle operation is needed.
- Frequency Division: A chain of T latches can divide the clock frequency by 2, 4, 8, etc.
- State Machines: Used in sequential circuits where toggle functionality is required.