

Day 8 Topic: Verilog codes for 3-to-8 Decoder Using Cadence (Xcelium)

◆ What is a Decoder?

- A **decoder** is a combinational circuit.
- It takes **n inputs** and produces **2^n outputs**.
- Only **one output is active** (logic 1) at a time, depending on the input combination.
- Example: With 3 inputs → **8 outputs**.

◆ 3-to-8 Decoder

- Inputs: A, B, C (3 bits)
- Outputs: D0 to D7 (8 lines)

The decoder activates **exactly one output** corresponding to the binary value of (A,B,C).

◆ Truth Table (3 inputs → 8 outputs)

A B C Active Output

0 0 0 D0 = 1

0 0 1 D1 = 1

0 1 0 D2 = 1

0 1 1 D3 = 1

1 0 0 D4 = 1

1 0 1 D5 = 1

1 1 0 D6 = 1

1 1 1 D7 = 1

 At any given time, only **one line is HIGH**, rest are LOW.

◆ 1.1) Design Code

decoder_3_8.v

```
// 3-to-8 Decoder
module decoder3x8(
    input A, B, C,
    output D0, D1, D2, D3, D4, D5, D6, D7
);
    assign D0 = ~A & ~B & ~C;
    assign D1 = ~A & ~B & C;
    assign D2 = ~A & B & ~C;
    assign D3 = ~A & B & C;
    assign D4 = A & ~B & ~C;
    assign D5 = A & ~B & C;
    assign D6 = A & B & ~C;
    assign D7 = A & B & C;
endmodule
```

◆ 1.2) Test Bench Code

tb.v

```
module tb_decoder3x8;
    reg A, B, C;
    wire D0, D1, D2, D3, D4, D5, D6, D7;

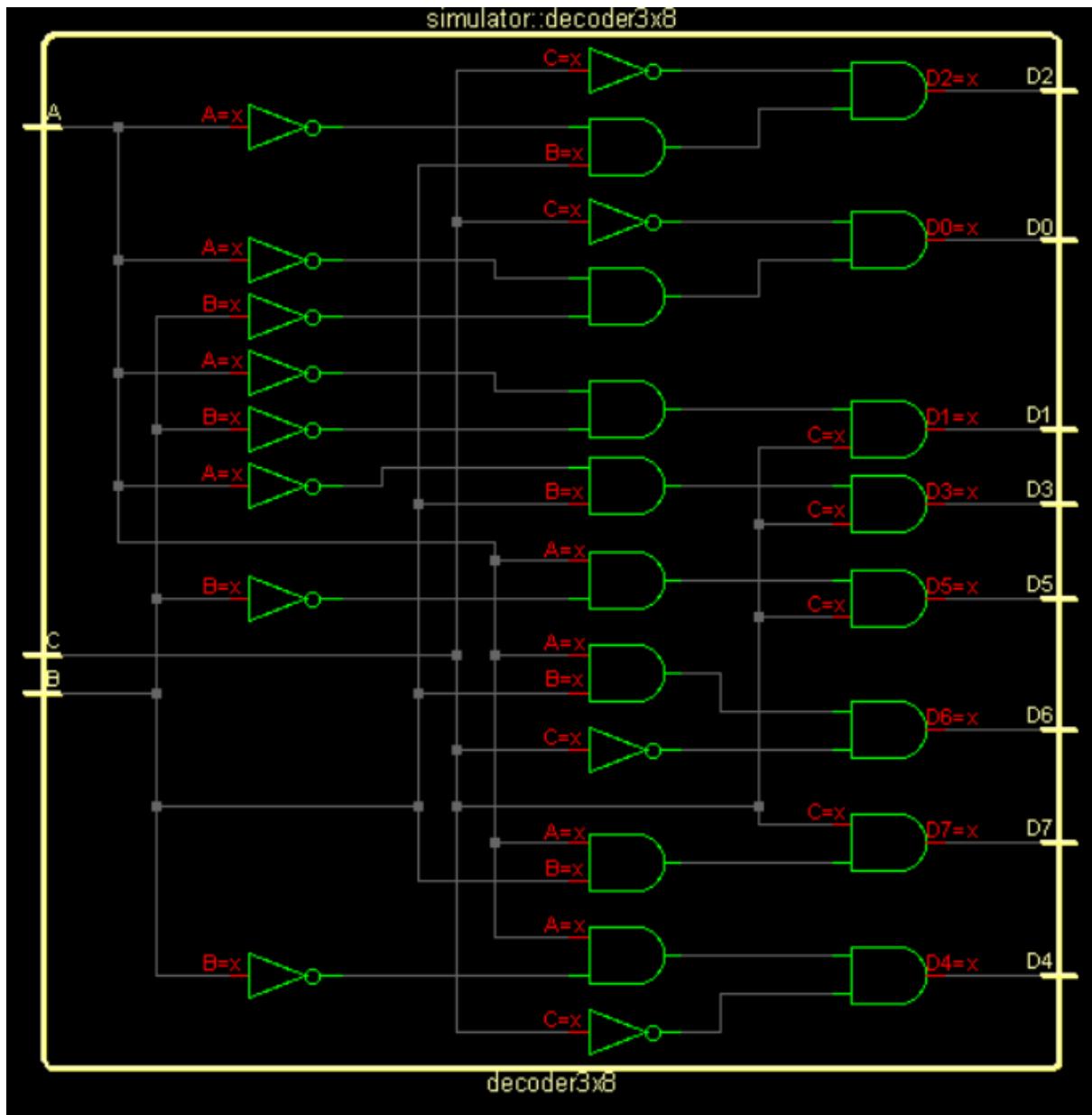
    // Instantiate DUT
    decoder3x8 uut (.A(A), .B(B), .C(C),
                      .D0(D0), .D1(D1), .D2(D2), .D3(D3),
                      .D4(D4), .D5(D5), .D6(D6), .D7(D7));

    initial begin
        $display("A B C | D0 D1 D2 D3 D4 D5 D6 D7");
        $display("-----");

        {A,B,C} = 3'b000; #10;
        {A,B,C} = 3'b001; #10;
        {A,B,C} = 3'b010; #10;
        {A,B,C} = 3'b011; #10;
        {A,B,C} = 3'b100; #10;
        {A,B,C} = 3'b101; #10;
        {A,B,C} = 3'b110; #10;
        {A,B,C} = 3'b111; #10;

        $stop;
    end
endmodule
```

◆ 1.3) Schematic



◆ 1.4) Wave Forms

