
Day 20 Topic: Verilog codes for T Flipflop Using Cadence (Xcelium)

◆ What is a Flip-Flop?

- A flip-flop is a small memory element in digital electronics.
 - It can store 1 bit of data: either 0 (LOW) or 1 (HIGH).
 - It is used in registers, counters, and memory circuits.
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T Flip-Flop Description

A T flip-flop (Toggle flip-flop) is a sequential circuit that changes (toggles) its output state every time the clock receives an active edge (rising or falling), only if the T input is HIGH (1).

If the T input is LOW (0), the flip-flop retains its previous state.

It is derived from the JK flip-flop by connecting J = K = T.

Inputs and Outputs

- Inputs:
 - T (Toggle input)
 - Clock (CLK) – edge-triggered signal
 - Outputs:
 - Q (main output)
 - Q' (complement output)
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Working

The operation of the T flip-flop depends on the clock edge and the value of T:

1. T = 0 → No change (the output remains the same as before the clock edge).
 2. T = 1 → Toggle (the output changes from 0 → 1 or 1 → 0 on every clock pulse).
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Truth Table (Edge-Triggered)

CLK Edge T Next State (Q^{n+1})

\uparrow / \downarrow 0 Q^n (no change)

\uparrow / \downarrow 1 \bar{Q}^n (toggle)

(\uparrow means rising-edge triggered, \downarrow means falling-edge triggered depending on design)

Circuit Implementation

- From JK Flip-Flop: Connect $J = K = T$.
 - From D Flip-Flop: Connect $D = T \oplus Q$ (XOR gate).
 - If $T = 1 \rightarrow D = \bar{Q} \rightarrow$ toggles.
 - If $T = 0 \rightarrow D = Q \rightarrow$ holds.
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Characteristic Equation

$$Q_{next} = T \oplus Q_{present}$$

→ "Next state equals T XOR present state."

◆ 1.1) Design Code

```
// T Flip-Flop
module t_ff (
    input wire T, CLK,
    output reg Q,
    output wire Qbar
);

    assign Qbar = ~Q;

    always @(posedge CLK) begin
        if (T)
            Q <= ~Q; // Toggle
        else
            Q <= Q; // Hold
    end
endmodule
```

◆ 1.2) Test Bench Code

```
tb.v

module tb_t_ff;
    reg T, CLK;
    wire Q, Qbar;

    // Instantiate T FF
    t_ff uut (.T(T), .CLK(CLK), .Q(Q), .Qbar(Qbar));

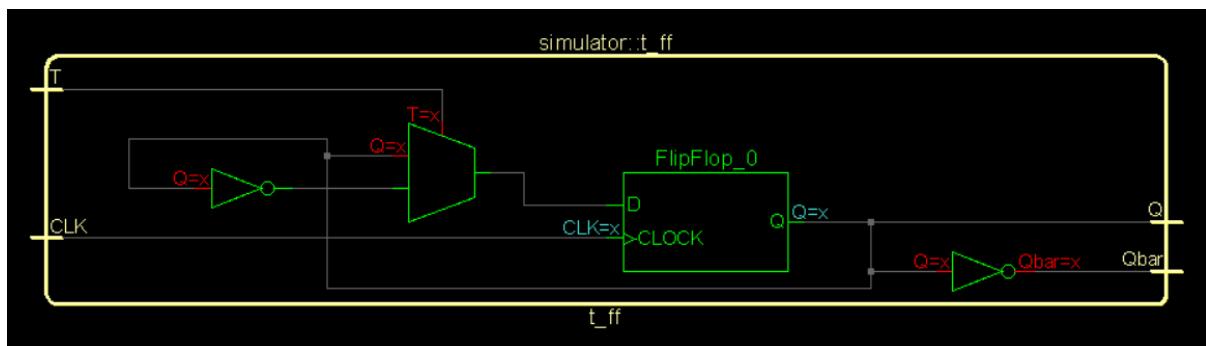
    // Clock generation: 10ns period
    initial begin
        CLK = 0;
        forever #5 CLK = ~CLK;
    end

    initial begin
        $monitor("T=%0t | CLK=%b T=%b | Q=%b Qbar=%b", $time, CLK, T, Q, Qbar);

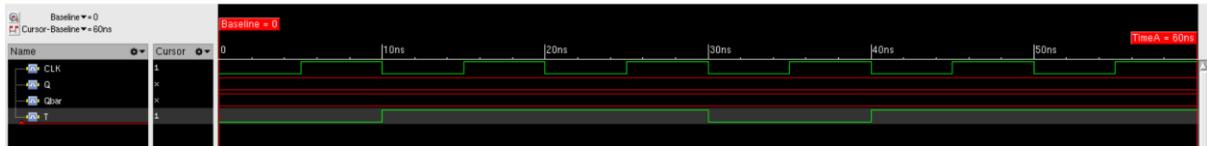
        // Initialize
        T=0; #10; // Hold
        T=1; #10; // Toggle
        T=1; #10; // Toggle again
        T=0; #10; // Hold
        T=1; #20; // Toggle twice more

        $finish;
    end
endmodule
```

◆ 1.3) Schematic



◆ 1.4) Wave Forms



Applications

1. Counters:

- The T flip-flop is the main building block for binary counters (asynchronous and synchronous).
- A single T flip-flop divides the clock frequency by 2.
- Multiple T flip-flops connected in series form frequency dividers.

2. Frequency Division:

- Used to divide frequency in clock generation circuits.

3. Toggle Circuits:

- Used where a simple ON/OFF alternation is needed.

4. Shift Registers and FSMs:

- Used for state toggling in sequential logic systems.