📘 **Day 29 Topic: Verilog codes for Synchronous Down Counter Using Cadence (Xcelium)**

Synchronous Down Counter

A Synchronous Down Counter is a counter in which all flip-flops are triggered by the same clock signal, and the counter counts downward in binary sequence (for example: 111 → 110 → 101 → ... → 000).

Since all flip-flops receive the clock pulse simultaneously, there is no ripple delay, and the operation is fast and synchronized.

Key Points

- All flip-flops share a common clock.
- The count decreases by one with each clock pulse.
- The next state of each flip-flop depends on the present states of the other flip-flops.
- Implemented using JK or T flip-flops.
- Faster and more accurate than asynchronous counters.

Example: 3-bit Synchronous Down Counter

Clock Pulses	Q2	Q1	Q0
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

- **1.1) Design Code**

syn_down_counter.v

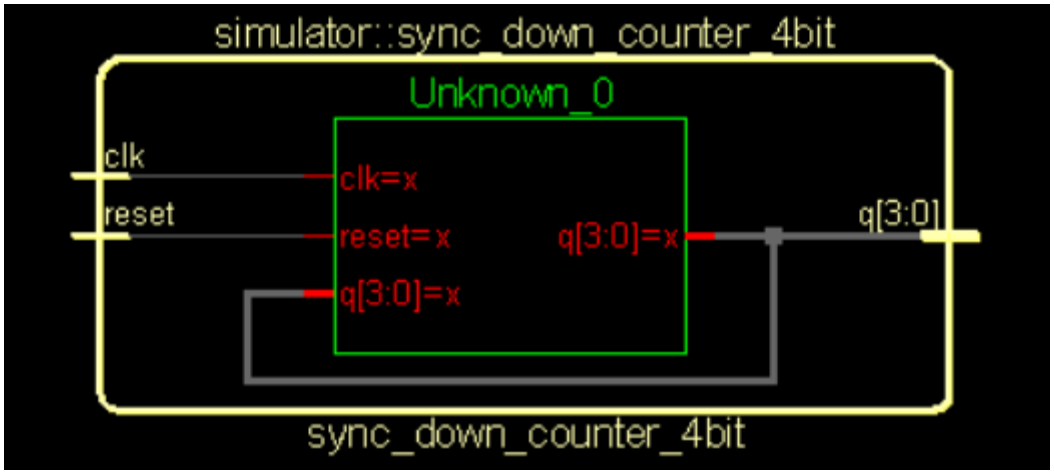
```
module sync_down_counter_4bit (
    input clk, reset,
    output reg [3:0] q
);
    always @(posedge clk or posedge reset) begin
        if (reset)
            q <= 4'b1111;
        else
            q <= q - 1'b1;
    end
endmodule
```

- **1.2) Test Bench Code**

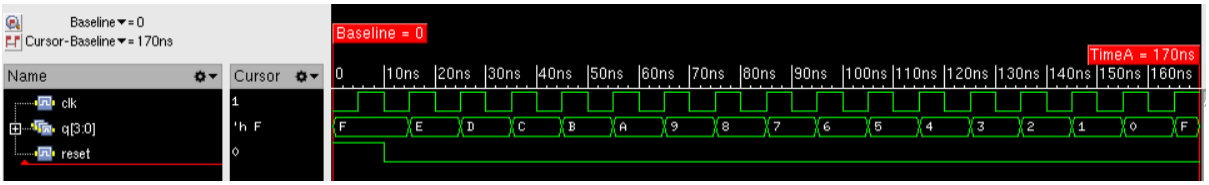
tb.v

```
module tb_sync_down_counter_4bit;
    reg clk, reset;
    wire [3:0] q;

    // Instantiate DUT
    sync_down_counter_4bit uut (.clk(clk), .reset(reset), .q(q));

    // Clock generation
    initial begin
        clk = 0;
        forever #5 clk = ~clk;   // 10ns clock period
    end

    // Stimulus
    initial begin
        reset = 1; #10;
        reset = 0;
        #160 $finish;
    end

    // Monitor outputs
    initial begin
        $monitor("Time=%0t | Q=%b", $time, q);
    end
endmodule
```

- **1.3) Schematic**



- **1.4) Wave Forms**



Applications

- **Digital clocks (for countdown timers)**
- **Sequence generators**
- **Reverse counting systems**
- **Frequency dividers**