

Day 3 Topic: Half Subtractor and Full Subtractor. in Verilog Using Cadence (Xcelium)

1 Half Subtractor

- Inputs: a, b
- Outputs: diff, borrow
- Equations:
 - $\text{diff} = a \wedge b$
 - $\text{borrow} = \sim a \wedge b$

◆ 1.1) Design Code

```
hs.v

module half_subtractor (
    input wire a, b,
    output wire diff, borrow
);
    assign diff = a ^ b;      // XOR for difference
    assign borrow = ~a & b;   // Borrow logic
endmodule
```

◆ 1.2) Test Bench Code

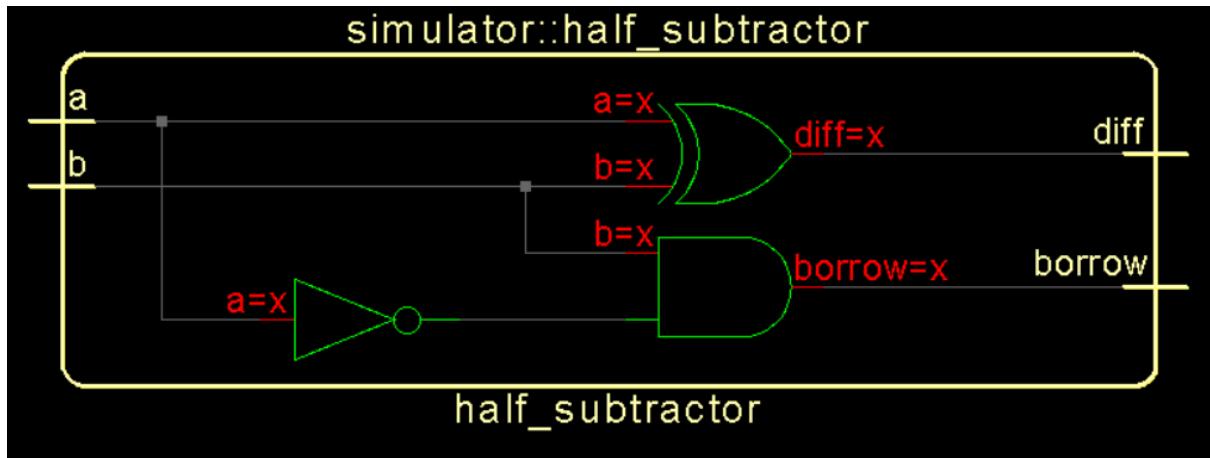
```
hs_tb.v

module half_subtractor_tb;
    reg a, b;
    wire diff, borrow;

    half_subtractor uut (a, b, diff, borrow);

    initial begin
        $display("a b | diff borrow");
        a=0; b=0; #10 $display("%b %b | %b %b", a,b,diff,borrow);
        a=0; b=1; #10 $display("%b %b | %b %b", a,b,diff,borrow);
        a=1; b=0; #10 $display("%b %b | %b %b", a,b,diff,borrow);
        a=1; b=1; #10 $display("%b %b | %b %b", a,b,diff,borrow);
        $finish;
    end
endmodule
```

◆ 1.3) Schematic



◆ 1.4) Wave Forms



2 Full Subtractor

- Inputs: a, b, bin (minuend, subtrahend, borrow-in)
- Outputs: diff, bout (difference, borrow-out)
- Equations:
 - $\text{diff} = a \wedge b \wedge \text{bin}$
 - $\text{bout} = (\neg a \wedge b) \mid ((\neg(a \wedge b)) \wedge \text{bin})$

◆ 2.1) Design Code

```

fs.v

module full_subtractor (
    input wire a, b, bin,
    output wire diff, bout
);
    assign diff = a ^ b ^ bin;           // XOR for difference
    assign bout = (~a & b) | (~(a ^ b) & bin); // Borrow out
endmodule

```

◆ 2.2) Test Bench Code

```

fs_tb.v

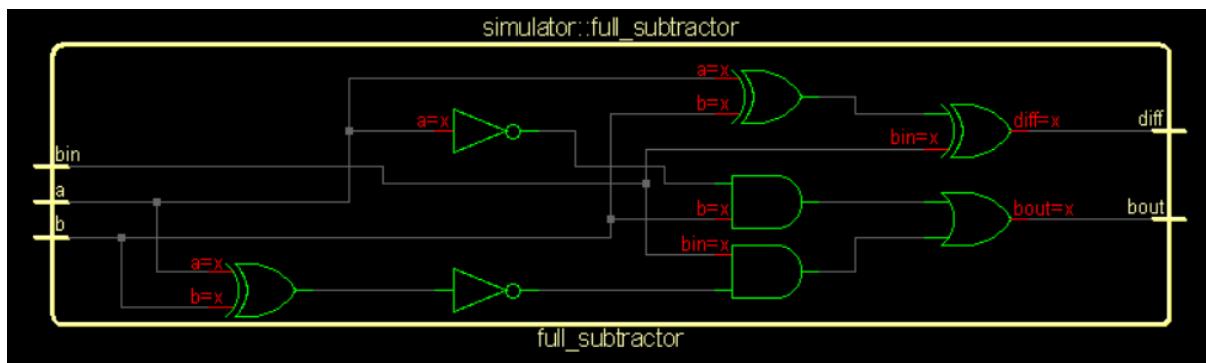
module full_subtractor_tb;
    reg a, b, bin;
    wire diff, bout;

    full_subtractor uut (a, b, bin, diff, bout);

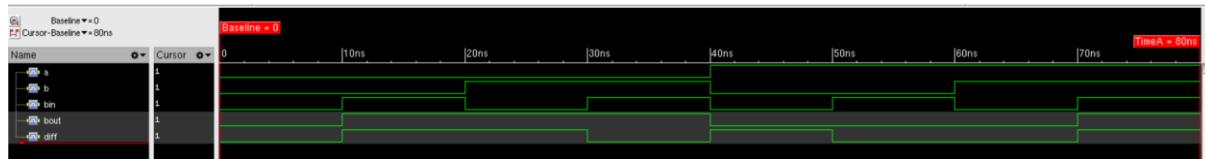
    initial begin
        $display("a b bin | diff bout");
        a=0; b=0; bin=0; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=0; b=0; bin=1; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=0; b=1; bin=0; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=0; b=1; bin=1; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=1; b=0; bin=0; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=1; b=0; bin=1; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=1; b=1; bin=0; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        a=1; b=1; bin=1; #10 $display("%b %b %b | %b %b", a,b,bin,diff,bout);
        $finish;
    end
endmodule

```

◆ 2.3) Schematic



◆ 2.4) Wave Forms



✓ Day 2 Summary:

- Implemented **Half Subtractor + Full Subtractor**.
- Wrote and explained **Verilog + Testbench** step by step.