👋 Hi, I'm Srilakshmi Jyothula

🎓 Final Year B.Tech Student | Aditya University, Surampalem

🔬 Passionate about VLSI | Design Verification | Digital Electronics

🚀 Trained in Verilog HDL, SystemVerilog, Protocols, STA

🏆 Project Topper in VLSI Domain – Technical Hub (Top 1 out of 123 teams)

🔧 Skills

- 🛠 Languages: C, Verilog, SystemVerilog, Assembly (8086, 8051)

- 📘 Tools: ModelSim, Vivado, Proteus, MASM, GTKWave

- 🧪 Verification: Testbenches, Assertions, Coverage

- 💡 Soft Skills: Teamwork, Planning, Time Management

📁 Projects

- 🔹 Low Power DSP using Approximate Circuits – http://sites.google.com/view/synthesissquad/home

- 🔹 Smart Blind Stick with Ultrasonic Sensor

- 🔹 Arduino-Based Radar Detection

🏅 Certifications

- Cadence Certifications (Digital IC, Verilog, SystemVerilog, STA)

- Digital Hardware with FPGA | Arduino | eSIM

📫 Let's Connect

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