Srinath PS

Lead Engineer

15 years of expertise in embedded firmware, infra-applications, and networking consistently demonstrating my proficiency as a strong technical leader. My track record encompasses leading and mentoring teams to success while spearheading the creation of innovative products across diverse domains.

PROFILE

- Extensive hands-on experience in system and firmware design, development, and debugging of multitasking embedded real-time systems.
- Design infrastructure applications/remote management solutions in multi chassis distributed systems like ISSU (In-Service Software Upgrade), HA (High Availability), Thermal & Power Management, FRU detection and management, Firmware upgrade Management, etc.
- Software design and development with proficiency at various levels of product development.
- Programming in Linux, ThreadX, vxWorks environment and Bare metal applications for different Hardware Architectures (ARM, PIC, PPC, x86).
- Exceptional troubleshooting and debugging skills, with a demonstrated track record of effectively resolving complex issues in customer-scaled environments, resulting in increased satisfaction and optimized performance.
- Experience leading collaborative efforts across geographies working closely with customers and vendors to drive requirements, debug issues, and implement effective solutions.
- Strong communication and analytical skills, adeptly handling multiple tasks while excelling in both independent and team-oriented environments.

EXPERIENCE

CISCO SYSTEMS, TECHNICAL LEAD ENGINEER, JULY 2019 – PRESENT

WESTERN DIGITAL, PRINCIPAL FIRMWARE ENGINEER, JUNE 2018 – JUNE 2019

HEWLETT PACKARD ENTERPRISE, SENIOR FIRMWARE SPECIALIST, FEBRUARY 2015 – JUNE 2018

JUNIPER NETWORKS, SOFTWARE ENGINEER(MTS3), SEPTEMBER 2012 – FEBRUARY 2015

ARICENT GROUP, SENIOR SOFTWARE ENGINEER, JULY 2009 – SEPTEMBER 2012

CONTACT

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EDUCATION

Bachelors, Electronics & Communication Engineering, 2009
Anna University, Chennai

SKILLS

Programming Languages: C, C++, Golang
Scripting: Python, Bash
Assembly Language: ARM
Operating Systems: ThreadX, Linux, VxWorks
Tool Chains: GCC, IAR Embedded Workbench, Green Hills
Target Platforms: ARM Cortex-M4, PIC32-MX
Communication Protocols: I2C, RS232, SPI, Ethernet, PCIe
Debugging: GDB, Oscilloscopes, I2C Analyzer, WireShark, IXIA, JTAG,
Standards & Protocols: Ethernet OAM, 802.1Q, STP, VLAN Stacking
Configuration Management: Perforce, SVN, CVS, GIT
Additional Technologies: Docker, Kubernetes, Kafka, MongoDB, Restful APIs

CISCO SYSTEMS, TECHNICAL LEAD ENGINEER,

Intersight – Firmware Upgrade Management:
Role: Technical Lead Engineer
Intersight is a SAAS cloud/on-prem platform designed to manage compute, storage, and networking infrastructure. As the technical lead engineer for the firmware upgrade management service, I oversaw the development of features allowing for the seamless management of firmware distributable installations, scheduled upgrades, firmware inventory, and upgrade recommendations across the infrastructure. Our goal was to orchestrate firmware installations end-to-end while minimizing user interactions.

Responsibilities and Impact:

- Designed and implemented an LRU (Least Recently Used) cache system within the firmware repository. This dynamic system automatically manages and cleanses firmware distributable from storage, optimizing resources based on usage and predefined storage thresholds. This innovation significantly reduced the need for manual intervention, streamlining the firmware distribution process.
- Successfully migrated Cisco software repository images to S3 storage, incorporating CDN support to improve accessibility and download speeds for customers. This strategic move led to a notable 50% reduction in firmware download times, greatly enhancing user experience and operational efficiency.
- Developed a single fabric interconnect upgrade feature, empowering customers to upgrade one interconnect independently when the other is offline due to hardware failure or network disconnection. This implementation ensures continuous operation and flexibility in firmware updates, departing from the traditional requirement to update fabric clusters in pairs.
- Implemented Lot9 and scrub workflows compliant with European data standards for storage cleaning. These workflows are automatically initiated upon server decommission or when RMA action is triggered by the user, ensuring adherence to regulatory requirements and optimal data management practices."

DDC (Disaggregated Distributed Chassis):
Role: Technical Lead Engineer

IOS XR on Whitebox hardware as a stand-alone router:
First phase of this project aimed at bringing up IOS XR which is built on Windriver Linux on a Standalone chassis and be able to host XR and Calvados VM's that run admin and routing applications. The vendor board was brought up till IOS XR in a week's time which brought in lots of accolades to the team followed up with the next phase of work.

IOS XR on Whitebox hardware as a DDC Multi-Chassis:
Second phase of this project aimed at bringing up IOS XR on a Distributed Chassis. The hardware architecture comprises of 4 different chassis from different vendors where each of these chassis responsible for various functionalities. My role was to drive the effort in bringing up all these boards with Windriver Linux and setup inter-connects between them to route traffic.

Migration of Windriver Linux to OpenEmbedded Linux:
This phase involved migrating from Windriver Linux (Kernel 3.x) to OpenEmbedded Linux(5.4x) that required upgrading the necessary drivers, packages and other utilities. Migrated init services to systemd services.

Responsibilities and Impact:

- Led architectural efforts for the hardware abstraction layer, facilitating the integration of kernel drivers for vendor hardware, as well as the deployment of administrative and routing applications.
- Collaborated with vendors and partner teams based in Taiwan and the US throughout various stages of product integration.
- Played a key role in enabling support for chassis FRU/power management using IPMI, seamlessly integrating it into the administrative plane.

- Architectured and developed diverse debuggability solutions for a cluster of 50 different chassis acting as a logical router.
- Spearheaded the standardization of firmware and software releases across three different vendors for various chassis.
- Engaged in the process of backporting kernel patches to address issues in drivers and the kernel.
- Collaborated closely with customers to address requirements, debug issues, and resolve them seamlessly during the stages of development, integration, and deployment.
- Received recognition from the customer for technical contributions, proficiency, and design expertise demonstrated throughout the development and deployment phases.
- Recognized for exceptional technical proficiency and steadfast dedication to fulfilling customer requirements, leading to elevated project success and satisfaction that has led to substantial business growth, with the product currently utilized by AT&T, generating a software business of $95M.

WESTERN DIGITAL, PRINICIPAL FIRMWARE ENGINEER

UFS Host Controller Infrastructure for HDD:
The hard disk drives with an integrated UFS NAND controller and NAND flash to cache the data writes prior writing to the disks or hold the data during power loss. My role as an Agile scrum master involved working closely with Agile Product Owners/Architects to understand the requirements, design and collaborate with team in implementation of the host controller interface driver.

Responsibilities and Impact:
- As a scrum master work along with team and product owner coordinating all scrum ceremonies including Sprint Planning, Retrospectives, Demos and Release planning.
- Bring-up the palladium FPGA for pre validation of the NAND controller.
- Work on the implementation of UFS controller in test driven methodology.

HEWLETT PACKARD ENTERPRISE, SENIOR FIRMWARE SPECIALIST

Chassis Controller Firmware:
The server chassis controller is responsible for performing power sequencing, management, cooling functionalities, power metering, calibration, regulation, zoning, FRU management etc. My role included performing bring up working closely with hardware team working on-site. And have worked on different functionalities like power capping, FRU management etc.

Pass through Switch Firmware:
The passthrough switch fits into the chassis and provides a direct one-to-one connect between each server in the enclosure and the external network device that provides non-switched, non-blocking path between the network and the server. My role involved porting of the firmware from a different hardware series to fit into the HPC series chassis doing a sole end-end bring up working closely with the hardware team.

Responsibilities and Impact:
- Involved in prototype/bring up of the new chassis controller/passthrough hardware based on ARM-Cortex M4 using ThreadX RTOS.
- Migrated bare metal services to ThreadX that's responsible for performing various chassis management functionalities.
- Migrated ThreadX kernel which enabled FPU in ARM reducing the CPU instruction cycle by more than 50% thereby improving the metering, capping responsiveness.
- Enabled DMA for ADC which resulted in much faster and improved power measurements and calibrations offloading the CPU.
- Designed and Implemented power capping/zoning functionality which caps the CPU power to set limits by throttling the CPU frequency.

- Implemented cooling management which monitors the thermal sensors that spread across the chassis and servers to drive the fans/water coolants to keep the chassis temperature under limits. Worked closely with thermal team to understand the requirements and test in lab.
- Designed and enabled firmware upgrade capability on the pass-through switch firmware which is managed by the chassis controller.
- Engaged closely with cross functional teams across geographic zones during the bring-up and feature development.
- Recognized by the team for proactive initiatives and innovative optimization solutions that notably improved the performance of the chassis controller.
- Engaged in sustaining older chassis controller, a bare metal firmware based on PIC32 MX.

JUNIPER NETWORKS, SOFTWARE ENGINEER(MTS3)

Responsibilities and Impact:

- Involved in development of Chassis management features which is responsible for managing various sub-component within a chassis (Fans, Line cards, PEM, Craft panel) and redundancy management.
- Have involved in development of interface management module which is responsible for managing and monitoring the line card interfaces, detecting optics and bring-up of the physical links.
- Involved in development of diagnostics tests for modular interface cards which includes PHY tests, clock tests, FPGA access/interrupt tests, RX LOS test, RX clock squelch tests, MAC tests, Packet path tests etc.
- Developed micro kernel drivers for BCM PHYs, temperature sensors, voltage monitors optics.
- Involved in development of ISSU infrastructure of modular interface cards for warm software update.
- Designed a new distributed diagnostics framework for JUNOS which eased the execution of diagnostics in stand-alone mode and run-time mode providing offline and online diagnostics capabilities.
- Engaged with JTAC closely provided support for debugging & fixing various field issues directly interacting with customers.

ARICENT GROUP, SOFTWARE ENGINEER(MTS3)

Responsibilities and Impact:

- CPE Test Head Generator – Provides generator/analyzer capability that help validate the Metro Ethernet network between the end points of customer Ethernet services.
    - Prototyped this functionality in Marvel Cheetah ASIC and Broadcom ASIC for Alcatel Switches
    - Implemented the feature and provided support for fixing issues reported from QA
- Ethernet OAM – Virtual UP MEP and 100ms Support – Enhanced Ethernet OAM to support 100ms interval from software and added Virtual UP MEP support as a requirement for ERP that can support OAM monitoring in a ring without burning out a physical port.
- TCAM Filter Reduction – Optimized the usage of TCAM entries occupied by Ethernet OAM in Marvell ASIC since it had a limitation to support maximum 128 entries. This helped scale the configurable MEPs in OAM for Alcatel switches.
- Service Assurance Agent – Provides Service Level Monitoring by measuring network delay and jitter at IP layer as well as MAC layer. Uses the ping, OAM packets and MAC packet to measure SLAs end-to-end.
    - Prototyped the functionality and show cased it to the customer.
    - Involved in requirement analysis, design and implementation of the functionality.
    - Added support for hardware timestamping of the SAA packets to get more accuracy on SLAs.
    - Involved in fixing various issue reported from the field and QA.

References upon request