Srinath PS

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PROFILE

- 13 years of overall embedded firmware/software architecture and development experience.
- Sound Knowledge and Experience in
  - System/Firmware Design, Development and Debugging for Multi Tasking Embedded Real-Time Systems.
  - Design Infrastructure Applications/Remote Management Solutions in Multi chassis Distributed Systems Chassis Management, ISSU (In-Service Software Upgrade), HA (High Availability), Thermal & Power Management, FRU Detection and Management, etc.
  - Software Design and Development with Proficiency at Various Levels of Product Development.
  - Programming in Linux, ThreadX, vxWorks Environment and Non-OS Bare Metal Applications For Different Hardware Architectures (ARM, PIC, PPC, x86).
  - Customer and Vendor Interactions Driving Solutions/Debugging.
  - Outstanding troubleshooting and debugging skills with proven track record.

EDUCATION

Bachelors, Electronics & Communication Engineering 2009
K.L.N College of Engineering
Anna University, Chennai

SKILLS

- Programming Languages : C, C++
- Scripting : Python, Shell
- Assembly Language : ARM
- Operating Systems : ThreadX, Linux, VxWorks,
- Tool Chains : GCC, IAR Embedded Workbench, Green Hills
- Target Platforms : ARM Cortex-M4, PIC32-MX
- Debugging : GDB, Oscilloscopes, I2C Analyzer, WireShark, IXIA, JTAG
- Standards & Protocols : Ethernet OAM, 802.1Q, STP, VLAN Stacking
- Communication Protocols : I2C, RS232, SPI, Ethernet
- Configuration Management : Perforce, SVN, CVS, GIT

WORK EXPERIENCE

Cisco Systems July 2019 – Present
Technical Leader | Bangalore, India

- Worked closely with System Architects to define requirements and design of XR disaggregated cluster for white box platforms.
- Bring up of Cisco XR NOS on Whitebox box ONIE based platform(s) and compute server.
- Uplifted the multi chassis Cisco XR NOS for white box cluster architecture support.
- Worked with white box vendors to drive hardware issues to closure and track the hardware/firmware deliverables.
- Prepare yocto recipes for vendor drivers in WindRiver Linux.
- Responsible for handling internal/customer issues reported across release cycles of the product.

Western Digital, June 2018 – June 2019
Principal Firmware Engineer | Bangalore, India

- Engage with System Architects to define high level requirements for UFS infrastructure support in HDD
- UFS v2.1 Host Controller Interface Infrastructure design & development for hybrid HDD product.
- Agile Scrum Master – Co-ordinate all Scrum ceremonies including Sprint Planning, Retrospectives, Demos and Release Planning.

Hewlett Packard Enterprise, February 2015 – June 2018
Senior Firmware Engineer | Bangalore, India

- Bring up of BMC satellite controller & Pass through switch firmware (Freescale K60, K64 - ARM Cortex M4) with ThreadX RTOS.
- Played key-role in designing & developing various power sequencing, management and cooling functionalities like Metering, Calibration, Regulation, Zoning, Fan Thermal Control, Power Supply Management, Server Power/FRU management etc.
- Architected mechanism to speed up ADC conversions for power measurement using PDB (Programmable Delay Blocks), DMA and hardware rework that substantially reduced the conversion duration by offloading the CPU.
- Designed block protocol mechanism over I2C for chassis controller communication with BMC.
- Provided support for handling customer specific enhancement & porting of various fixes in older generation chassis controllers based on PIC32MX.
- Enabled firmware upgrade support for pass through module.
- Engaged closely with cross-functional teams across Taiwan and Houston during bring-up and feature developments.
- Engaged in mentoring Interns and Junior Engineers.

Juniper Networks, September 2012 – February 2015
Software Engineer (MTS3) | Bangalore, India

- Chassis management module which is responsible for managing various sub-component within a chassis (Fans, Line cards, PEM, Craft panel) and redundancy management.
- Have involved in development of interface management module which is responsible for managing and monitoring the line card interfaces, detecting optics and bring-up of the links.
- Supported and qualified various optics for Juniper modular interface cards
- Developed diagnostics tests for modular interface cards which includes PHY tests, clock tests, FPGA access/interrupt tests, RX LOS test, RX clock squelch tests, MAC tests, Packet path tests etc.
- Developed micro kernel drivers for BCM PHYs, temperature sensors, voltage monitors optics.
- Proof of concept for new distributed diagnostics framework for JUNOS which eased the execution of diagnostics in stand-alone mode and run-time mode. This framework replicates the hardware schematics in the form of device graph which has a set of diagnostics test bound to it. This framework shall help in capturing the missing diagnostics and provides end to end validation of entire hardware.
- Involved in development of ISSU infrastructure for modular interface cards that handles software update without undergoing a cold reboot.
- Engaged with JTAC closely provided support for debugging & fixing various field issues directly interacting with customers.

Aricent Group, July 2009 – September 2012
Senior Software Engineer | Bangalore, India

- **CPE Test Head Generator** – Provides generator/analyzer capability that help validate the Metro Ethernet network between the end points of customer Ethernet services.
    - Prototyped this functionality in Marvel Cheetah ASIC and Broadcom ASIC for Alcatel Switches
    - Implemented the feature and provided support for fixing issues reported from QA

- **Ethernet OAM – Virtual UP MEP and 100ms Support** – Enhanced Ethernet OAM to support 100ms interval from software and added Virtual UP MEP support as a requirement for ERP that can support OAM monitoring in a ring without burning out a physical port.
- **TCAM Filter Reduction** – Optimized the usage of TCAM entries occupied by Ethernet OAM in Marvell ASIC since it had a limitation to support maximum 128 entries. This helped scale the configurable MEPs in OAM for Alcatel switches.
- **Service Assurance Agent** – Provides Service Level Monitoring by measuring network delay and jitter at IP layer as well as MAC layer. Uses the ping, OAM packets and MAC packet to measure SLAs end-to-end.
    - Prototyped the functionality and show cased it to the customer
    - Involved in requirement analysis, design and implementation of the functionality.
    - Added support for hardware timestamping of the SAA packets to get more accuracy on SLAs.
    - Developed management cloud for Alcatel Switches.
    - Involved in fixing various issue reported from the field and QA.