LDO Design

Project Name: Low-Dropout (LDO) Voltage Regulator Design

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Institution/Organization: Arizona State University

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Project Overview

Introduction:

This project consists of design, simulations, and analysis of low-dropout regulator (LDO). LDO utilizes an amplifier as the core circuit to regulate the output voltage. Low-Dropout (LDO) regulators are critical analog components used in voltage regulation to achieve efficient, stable, and precise power delivery across varying loads. This project explores the design and analysis of an LDO regulator using the CMOS TSMC 0.25µm process. The regulator was designed to meet stringent specifications, focusing on performance metrics such as power dissipation, gain, bandwidth, stability, and ripple voltage. This report delves into the design methodology, challenges faced, and results achieved for each component of the LDO regulator.

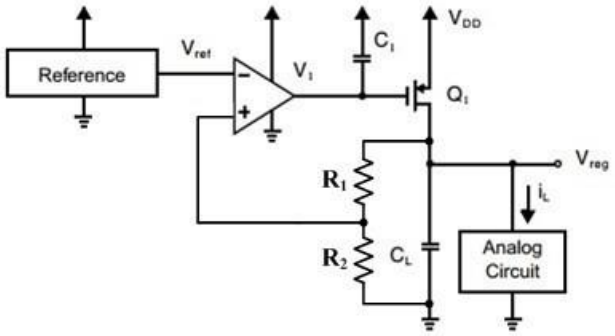

Fig. 1. Schematic of a low dropout regulator. The circuit utilizes a high gain amplifier together with a driver stage to supply the required current and a feedback network.

Problem Statement:

The objective of this project was to design an LDO regulator capable of delivering an output voltage of 1.6V from a supply voltage of 2.2V, load Current ranges reliably from 1mA to 50mA and maintain ripple voltage below 5% also by keeping power dissipation below 0.3mW and achieving a stable device with a phase margin greater than 60 degrees.

The design incorporated two major stages:

Driver Stage – Responsible for current sourcing and stability.

Amplifier Stage – Provides the required gain and bandwidth for proper regulation.

Requirements:

- Voltage supply 2.2V
- CMOS TSMC 0.25µm Process
- VREF = 1V
- Output capacitor = 50 pF
- Delivers 1 mA~50 mA current
- Output Regulated Voltage of 1.6V
- VRipple <5%
- PDC<0.3 mW

Design and Implementation

Driver Stage Design:

The driver stage is responsible to provide the required current to the load. The driver stage is designed such a way that the size of driver stage is estimated with respect to operation of this stage in saturation while providing the requested current range at the requested output voltage. The major object is to design the PMOS driver to deliver load currents ranging from 1mA to 50mA, while ensuring the transistor operates in saturation. The width of the PMOS driver was swept to identify an optimal configuration. The input capacitance of the PMOS transistor was calculated as 10pF, providing intrinsic compensation. Smaller width led to poor phase margins, falling below 60 degrees, causing instability. Larger width provided adequate current sourcing capability and improved stability. Input Capacitance is 10pF at width of 2.6m used for PMOS to do compensation in LDO Stage

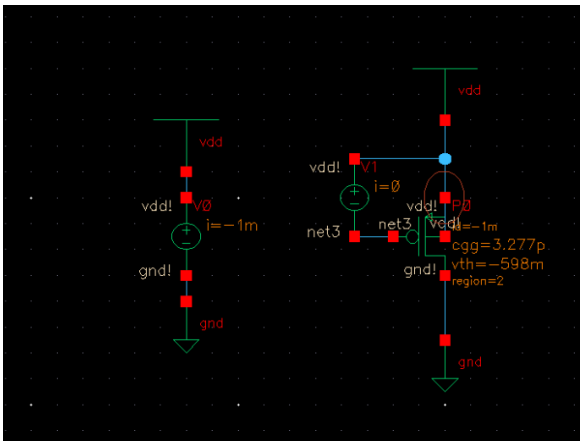

Fig. 2.1. MOSFET at saturation when driver current is at minimum

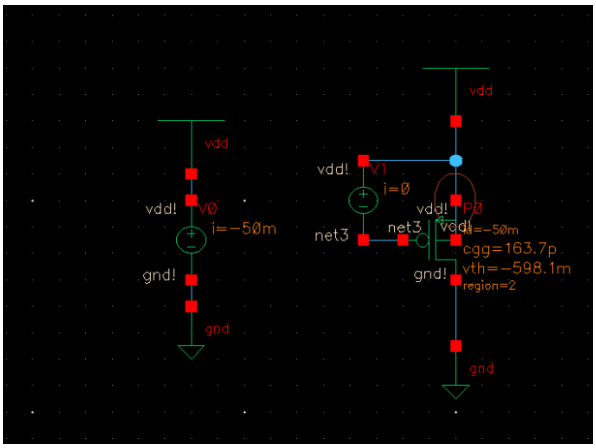

Fig. 2.2. MOSFET at saturation when driver current is at maximum

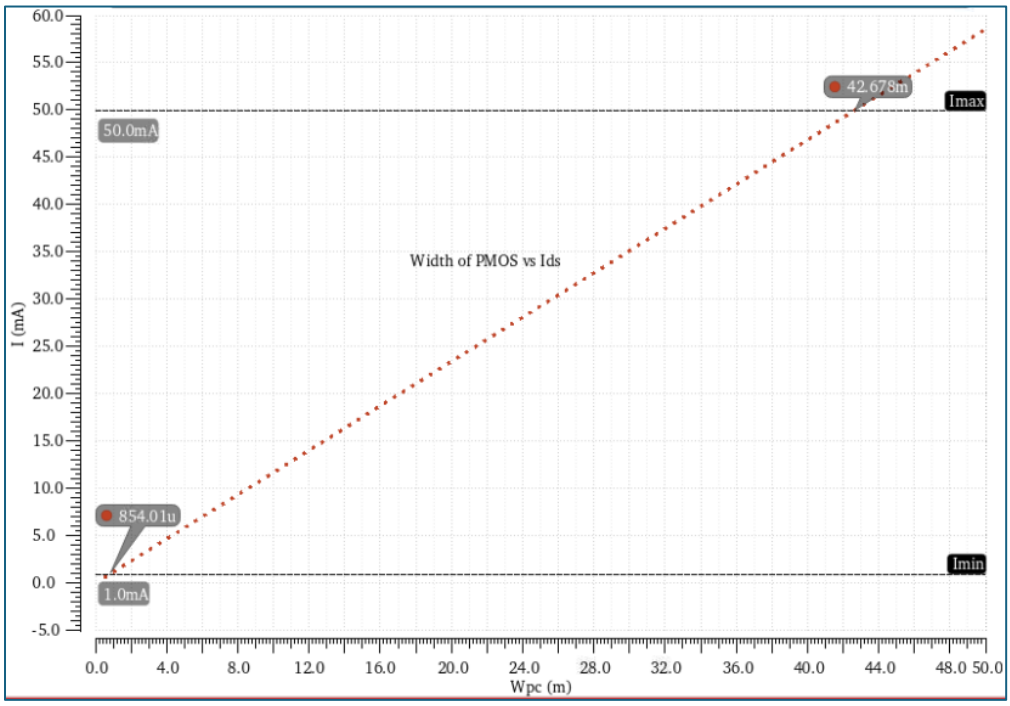

Fig. 3. Width of MOSFET vs Driver Current

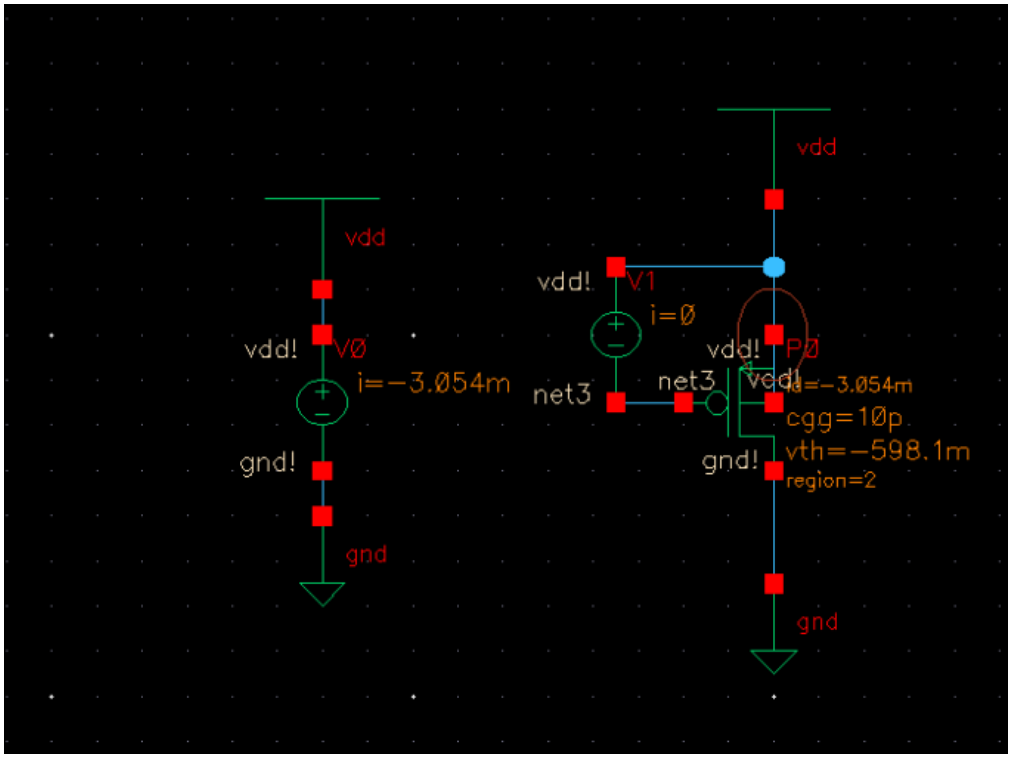

Fig. 4. Gate Capacitance of MOSFET was set at 10pF

Amplifier Stage Design:

This project consists of design, simulations, and analysis of low-dropout regulator (LDO). LDO utilizes an amplifier as the core circuit to regulate the output voltage. The amplifier stage was designed to provide high gain, bandwidth, and stability to the regulator while minimizing power dissipation. In the amplifier stage the NMOS sizing was chosen to provide high transconductance and PMOS sizing was chosen to provide high output impedance. This will help in providing high gain in amplifier stage. The size of amplifier was ensured to be low to keep power less than max power. Increasing the output impedance of PMOS may result in decrease in bandwidth, so sizing of PMOS length to be made sure that bandwidth lies at given range. Performed AC analysis plotting the Gain and Phase plot and ensured device is stable and matching all given requirements of Amplifier Stage and ensure all devices are in saturation.

Final Schematics:

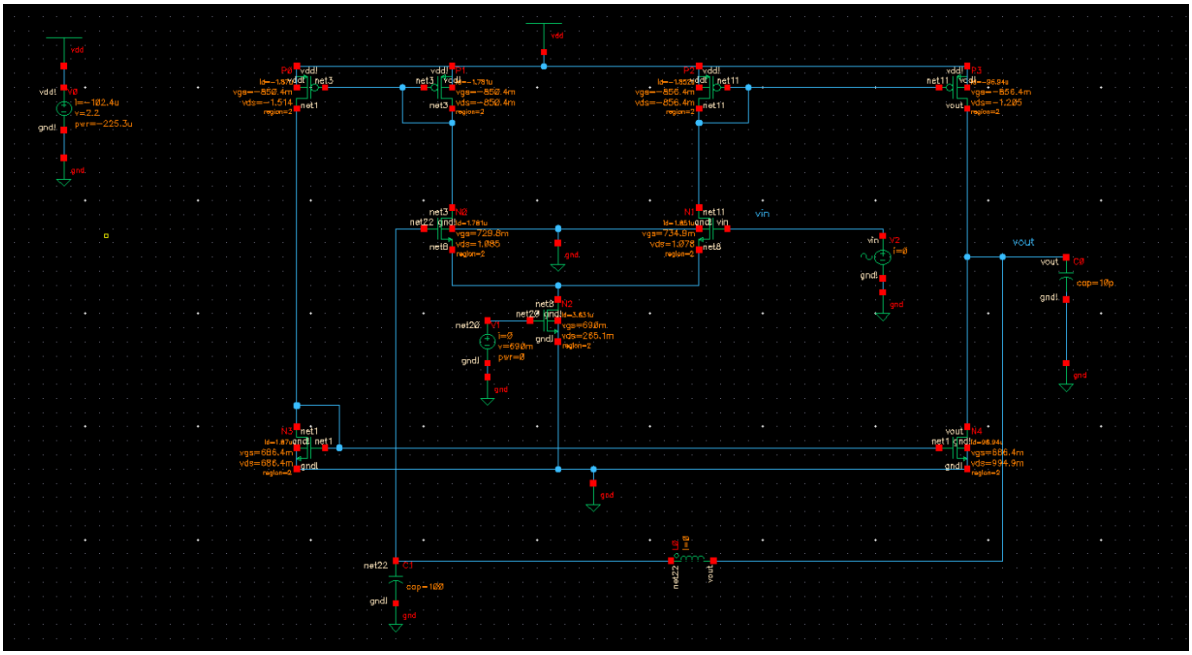

Fig. 5. Schematics of Amplifier Stage with all devices in saturation (region 2)

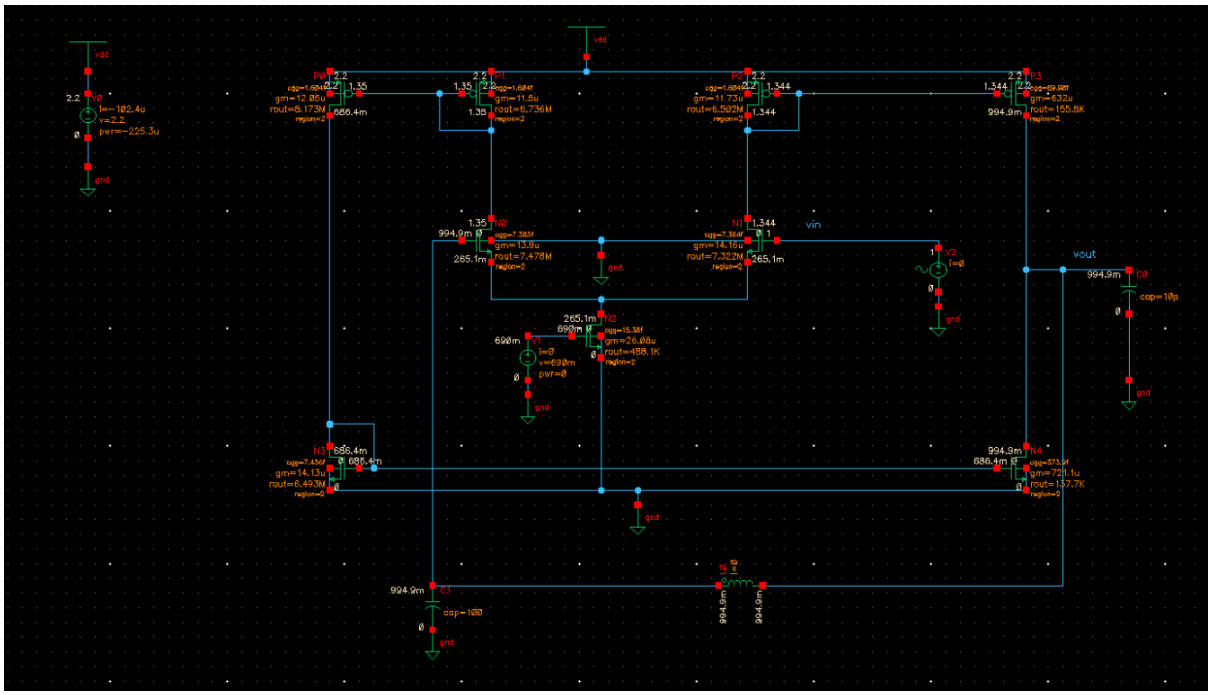

Fig. 6. Schematics of Amplifier Stage with gate capacitances, transconductance and output impedances

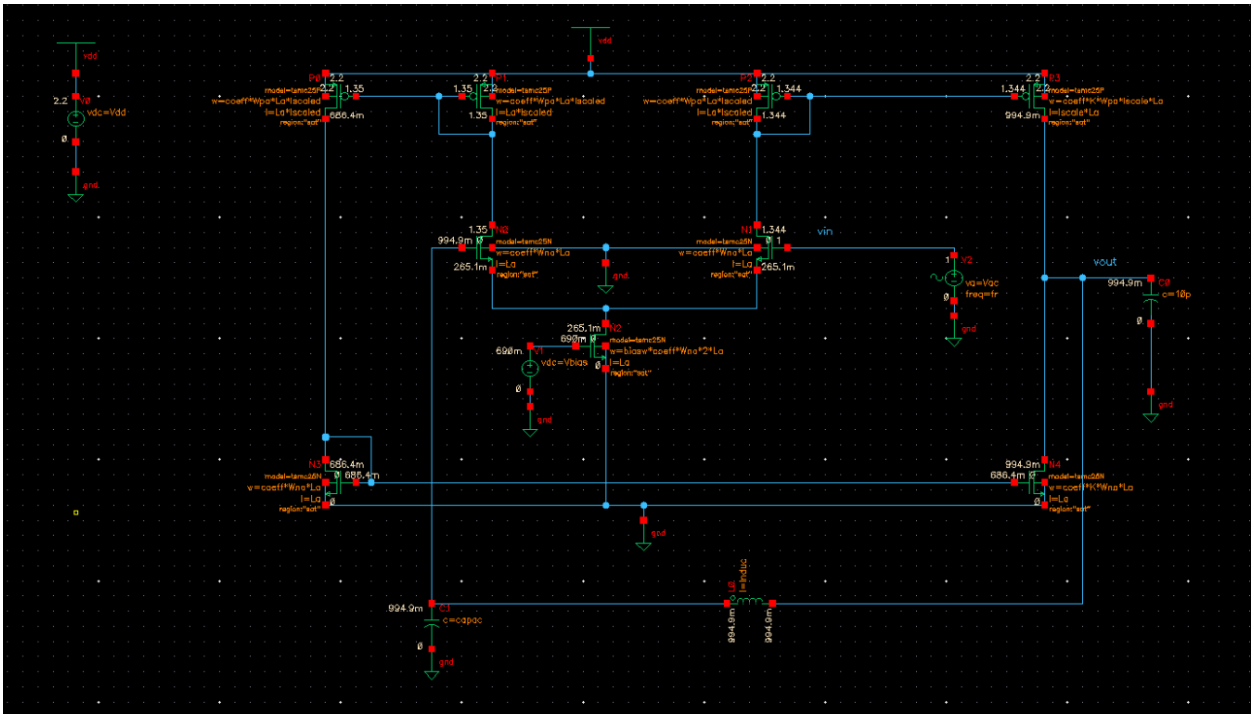

Fig. 7. Schematics of Amplifier Stage with width and length design variables of all devices

Observation and Results

Open-Loop Analysis:

Open-loop analysis was conducted to evaluate the regulator's performance without feedback. For open loop analysis, a combination of inductor and capacitor is used. Note that, inductor will present a high impedance (open), and the capacitor will introduce a low impedance (short) at our desired frequencies. The value of these components should be high enough to not affect the operation of the real circuit. The combination of the large inductor and the large capacitor is open at useful frequencies but creates feedback around DC to stabilize the biasing point of the amplifier. This is just for simulation purposes, and it is never used in real amplifier implementation.

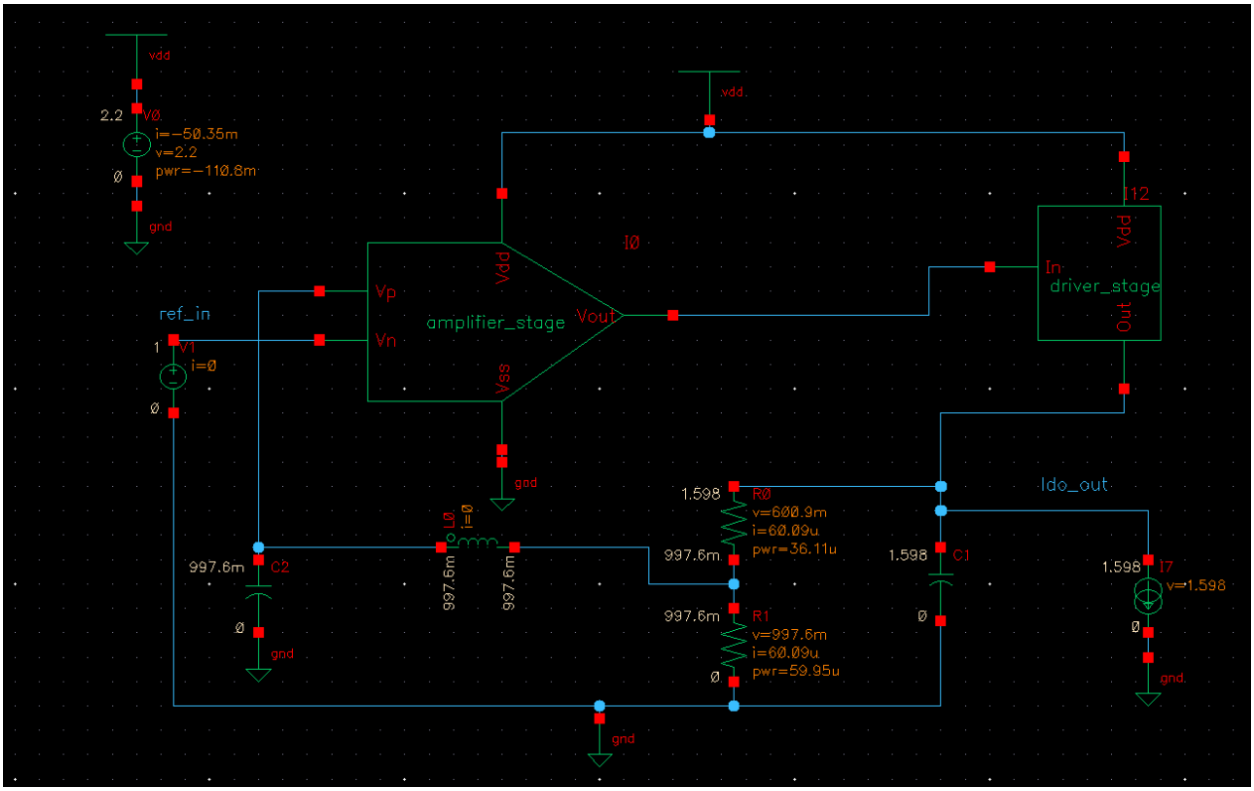

Fig. 8. Schematics of Final LDO in open loop

DC Analysis:

Operating points were simulated for load currents of 0.1mA, 1mA, 10mA, and 50mA. Observed steady-state output voltages within the desired range.

Currents	Vout	Vsg	Isd	Irl
100uA	1.632V	520mV	-161.364uA	61.3uA
1mA	1.626V	630mV	-1.06mA	61.12uA
10mA	1.616V	845mV	10.06mA	60.73uA
50mA	1.598	1.235V	-50.06mA	60.09uA

AC Analysis:

Frequency response plots revealed stable gain and bandwidth for varying capacitive loads.

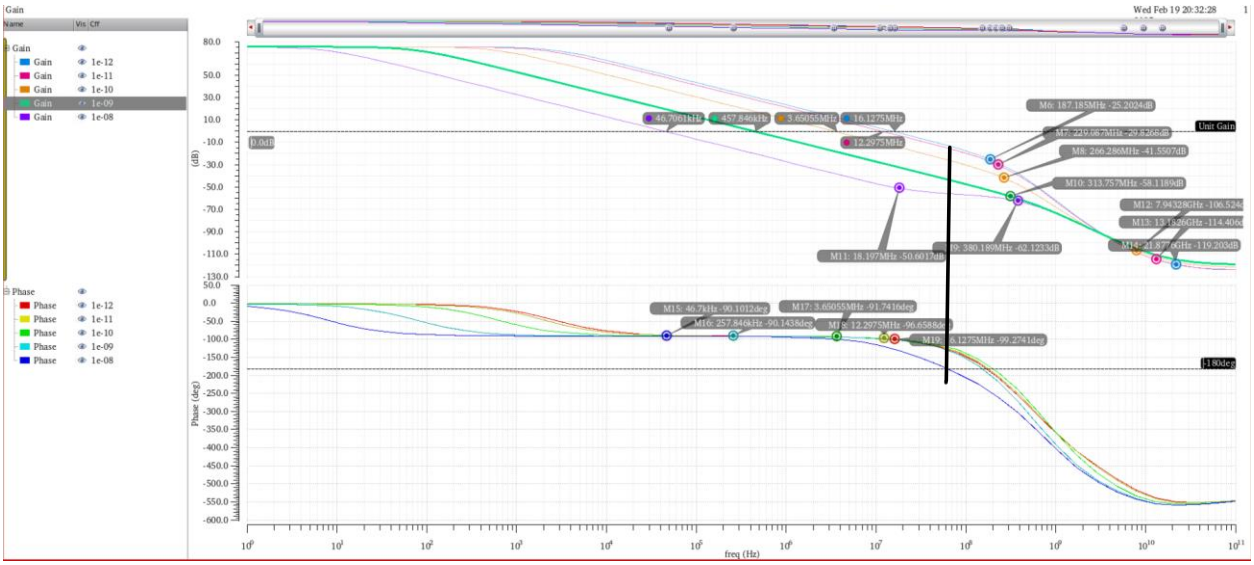

Fig. 9. AC Gain and Phase plot at amplifier stage for various capacitive loads

Gain = 78dB

Bandwidth = 207.3kHz

Phase Margin (due to phase shift) = 81 degrees

Closed-Loop Analysis:

The closed-loop analysis focused on transient response, line regulation, and stability under practical conditions.

Transient Response:

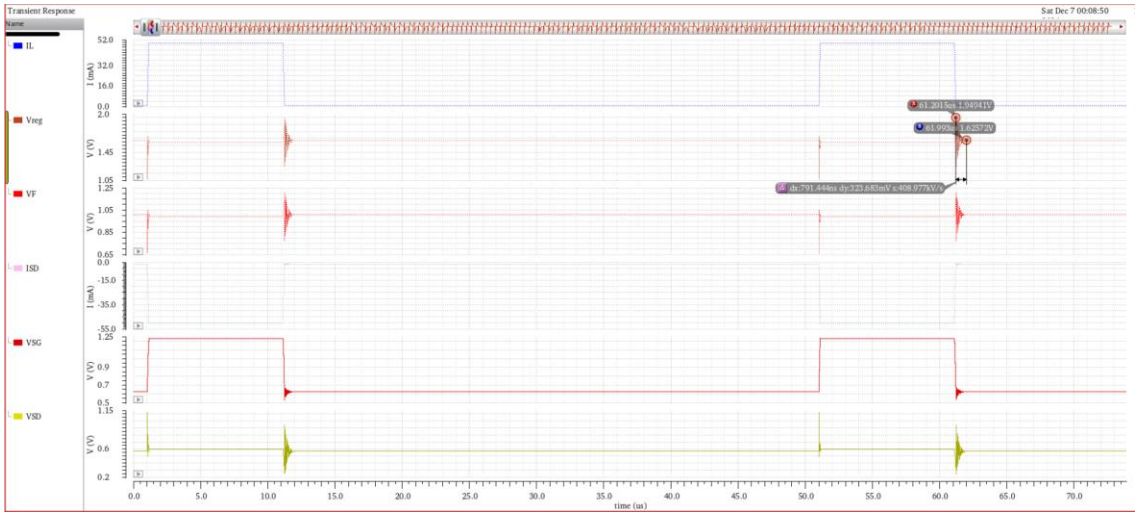

Fig. 10. Transient analysis of Load Current IL, Regulation Voltage Vreg, Feedback Voltage VF, Source Drain Current ISD, Source Gate Voltage Vsg and Source Drain Voltage Vsd

Step load tests simulated a current pulse (1mA to 50mA). Results included:

- Settling Time: 802ns.
- Ripple Voltage: 697mV (above the acceptable threshold).

Ripple voltage was influenced by unmodeled parasitic effects.

Line Regulation:

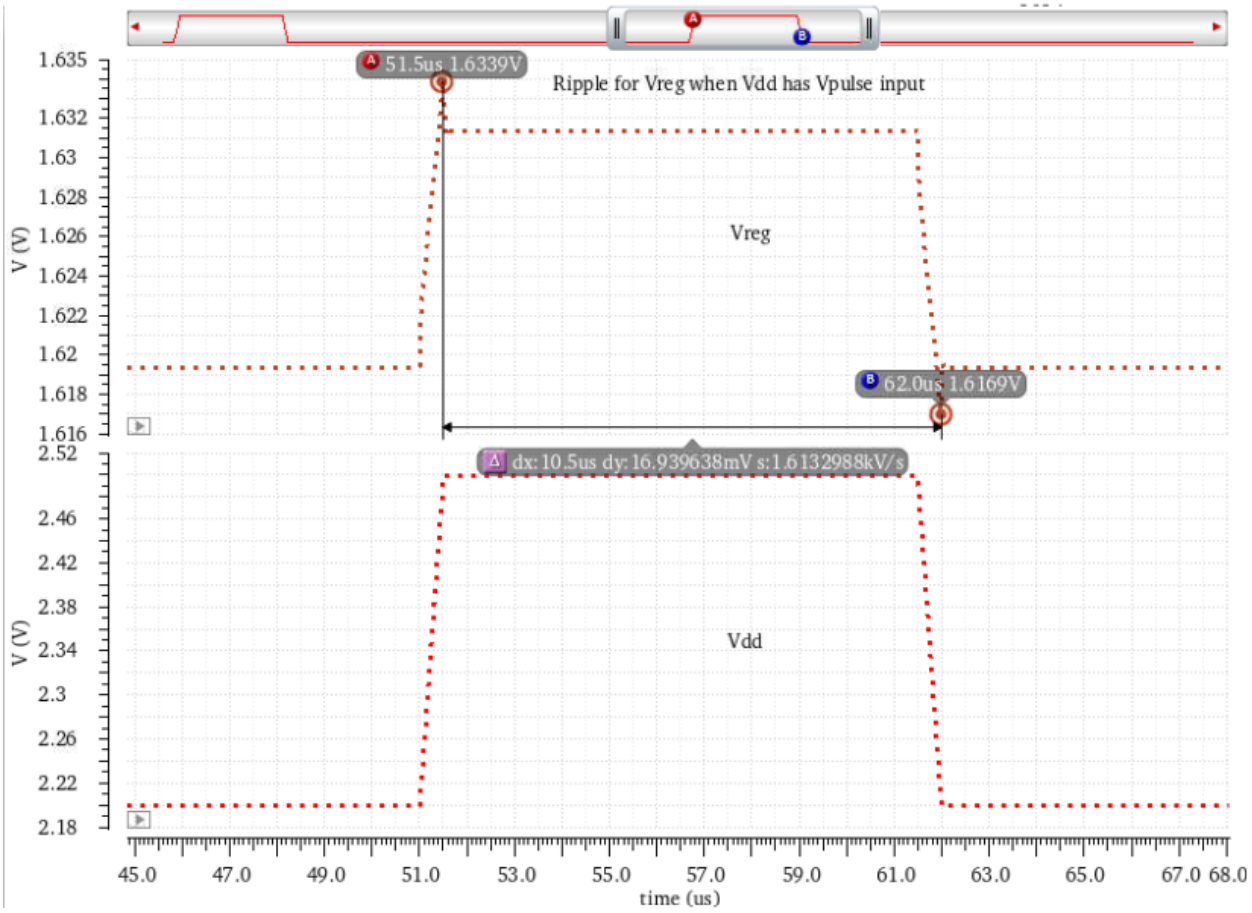

Fig. 11. Ripple when Vdd has pulse input from 2.2V to 2.5V

A voltage pulse (2.2V to 2.5V) was applied to the supply, revealing:

- Minimal transient voltage drop – 16.94mV.
- Rapid recovery times, ensuring reliable operation under varying supply conditions.

Learning Outcomes

This project underscored the complex trade-offs in analog circuit design, particularly for LDO regulators. The trade-off between power, gain, bandwidth, and stability necessitated a careful balance:

1. **Gain and Bandwidth Trade-off:** The relationship between transconductance, gain, and bandwidth highlighted the importance of transistor sizing. Increasing gain through higher NMOS transconductance improved regulation but added parasitic capacitance, reducing bandwidth. Optimization required iterative tuning of PMOS and NMOS sizing.
2. **Power and Stability Trade-off:** Achieving low power dissipation was accomplished by reducing the PMOS and NMOS sizes in the differential stage. This, however, introduced potential stability concerns due to decreased output resistance. Intrinsic compensation using the driver's gate capacitance (10pF) provided adequate phase margin without requiring external compensation capacitors.
3. **Ripple and Efficiency:** The ripple voltage exceeded specifications due to unaccounted parasitics. Future iterations should incorporate comprehensive parasitic modeling and optimized layout techniques to minimize ripples and improve overall efficiency.

The project demonstrated the critical importance of iterative design and simulation in meeting stringent design specifications for analog circuits.

Conclusion and Future Scope

Metric	Target	Achieved	Status
Power Dissipation	< 0.3mW	0.225mW	Met
Gain	≥ 40dB	78dB	Met
Bandwidth	> 200kHz	207.3kHz	Met
Phase Margin	> 60°	81°	Met
Ripple Voltage	< 5%	18%	Not Met
Settling Time	Minimal	802ns	Acceptable

This project successfully demonstrated the design of an LDO regulator that meets most performance metrics, including power efficiency, gain, bandwidth, and stability. Ripple voltage, however, remains an area for improvement. By optimizing transistor sizing and incorporating intrinsic compensation, the design achieved high stability without external capacitors.

1. **Ripple Voltage Reduction:** Include detailed parasitic extraction to better model ripple effects. Explore advanced compensation techniques.
2. **Robustness:** Conduct Monte Carlo simulations to assess performance under process, voltage, and temperature (PVT) variations.
3. **Power Efficiency:** Investigate subthreshold biasing techniques to further reduce power dissipation.

References

1. CMOS TSMC 0.25µm Process Design Rules.
2. EEE433/591 Final Project Guidelines by Dr. Saeed Zeinolabedinzadeh.
3. Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education.
4. Gray, P., Hurst, P., Lewis, S., & Meyer, R. (2001). *Analysis and Design of Analog Integrated Circuits*. Wiley.