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A Novel Wireless Interconnect Technology Using Impulse Radio for Interchip Communications

Yuanjin Zheng, *Member, IEEE*, Yueping Zhang, and Yan Tong, *Student Member, IEEE*

***Abstract*—This paper presents a novel wireless interconnect technology using impulse radio for interchip communications. The performance analysis of a binary phase-shift-keying (BPSK) impulse radio shows that a high data rate of 2.5 Gb/s with a low bit error rate $< 10^{-6}$ over an interchip wireless channel of length 20 cm can be achieved with the radiated power spectral density less than −41 dBm/MHz. The hardware design of the BPSK ultra-wideband (UWB) impulse radio realizes transmitter and receiver integrated circuits in 0.18-μm CMOS and antenna in a low-temperature cofired ceramic processes. Due to the current design and process limitations, the prototype impulse radio achieves a maximum data rate up to 200 Mb/s over the interchip wireless channel of length 20 cm with a total power consumption of 120 mW. The feasibility of using UWB impulse radio for Gb/s interchip wireless communication is addressed.**

***Index Terms*—CMOS, impulse radio, low-temperature cofired ceramic (LTCC), ultra-wideband (UWB), wireless interconnect.**

I. Introduction

With THE continued growth in the integration density of CMOS and clock frequency of ultra-large-scale integrated circuits, the wire interconnect technology is emerging as the major bottleneck to the improvement of integrated circuit (IC) technology. The semiconductor industry has sought to address this primary problem by increasing the thickness of the wires, using more exotic substrate materials with lower dielectric loss tangents, and employing more sophisticated input/output drivers at the transmitter and receiver. However, all of these potential solutions are costly, thereby making wireless interconnect technology an increasingly attractive alternative. A wireless interconnect technology uses a radio technology to provide communications between functions on a large integrated circuit chip (intrachip) as well as communications between functions on separate chips (interchip) located on a multichip module or on a motherboard, where distances are measured in a few to tens of centimeters and data rates are gigabits per second. The wireless interconnect technology has become possible due to the confluence of wireless communications algorithms with RF silicon processes. For example, Floyd *et al.* have demonstrated a wireless interconnect technology with integrated antennas, transmitters, and receivers in a 0.18-μm CMOS process for intrachip clock distribution at 15 GHz [1]. Zhang has evaluated the performance of a wireless interconnect technology for intrachip data transmission at 15 GHz [2]. Chang *et al.* have implemented a wireless interconnect technology for interchip communications using a capacitive coupling technique and Mizoguchi *et al.* using an inductive coupling mechanism [4]. The wireless interconnect technology is a very new approach, and much work remains to be done before becoming a viable candidate to replace global wires. Recently, the FCC has released an unlicensed 3.1–10.6-GHz frequency band for ultra-wideband (UWB)-related applications, where UWB transmission is defined as the occupied fraction bandwidth $>20\%$ or larger than 500 MHz of absolute bandwidth [5]. Since the UWB technique employs ultra-wide bandwidth and very low emission power density, it can be potentially used in low-cost, low-power, and short-range high-speed communication applications and is robust in the multipath environment and immune to the interferences [6]. In this paper, we propose a novel wireless interconnect technology that features the use of UWB impulse radio for interchip communications. The performance of impulse radio over an interchip wireless interconnect channel is analyzed in Section II. We present the hardware design and measured performance of UWB impulse radio in 0.18-μm CMOS technology in Section III. The experimental results are presented in Section IV and the conclusion is in Section V.

II. Performance Analysis of Impulse Radio Over Interchip Wireless Interconnect Channel

Fig. 1 illustrates the wireless interconnect technology within a multichip module that features the use of impulse radio. Conventionally, a processor chip interconnects with a memory chip in the multichip module using a peripheral component interconnect express (PCIe) circuit. The PCIe circuit is a recent industry standard in which a differential driver and a differential receiver reside on the processor chip, and a differential driver and a differential receiver reside on the memory chip. The differential driver on the processor chip is coupled to the differential receiver on the memory chip through a pair of wires. The differential driver on the memory chip is coupled to the differential receiver on the processor chip through another pair of wires. The pair of wires needs to support a high data rate of 2.5 Gb/s. The PCIe standard is intended to provide architecture that can extend into the future to accommodate the ever-increasing requirements for communication performance between chips [7]. The wireless interconnect technology employs an impulse radio to realize a wireless PCIe. Specifically, an impulse transmitter replaces a PCIe driver, an impulse receiver replaces

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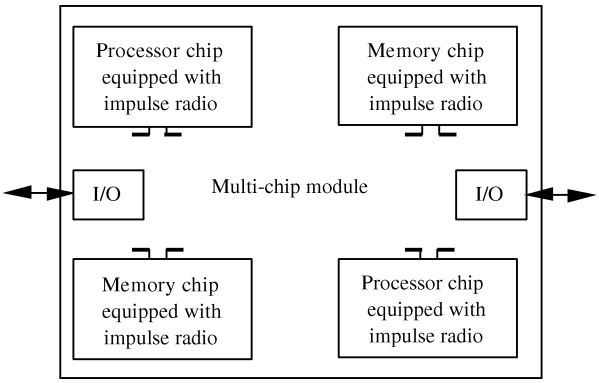


Fig. 1. Wireless interconnect using impulse radio for interchip communication.

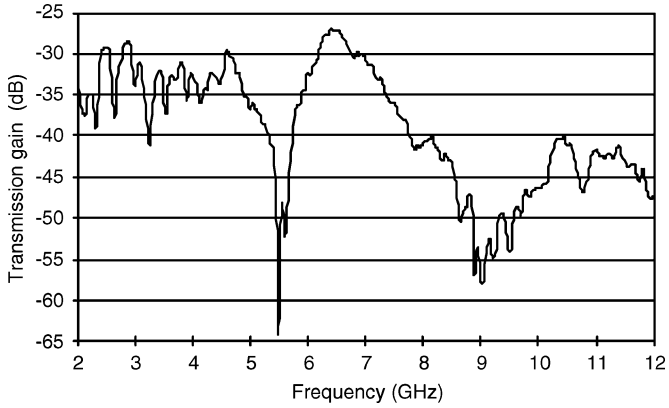


Fig. 2. Transmission gain versus frequency.

a PCIe receiver, and an antenna replaces a pair of wires. As compared with the conventional PCIe, the wireless interconnect technology has such advantages as scalability and reconfigurability. It can also be used at the system level to attain fault tolerance, because one can reconfigure the multichip module by software commands to debug and then to eliminate the fault chips via reconfiguration [8]. To fully exploit the capabilities of the wireless interconnect technology for interchip communications, the assessment of the theoretical performance of the impulse radio over an interchip wireless channel appears desirable. In this section, the performance of the binary phase-shift-keying (BPSK) impulse radio is evaluated over an interchip wireless channel of length 20 cm. The impulse radio operates with the radiated power spectral density < -41 dBm/MHz (or the average transmitted power less than -2.85 dBm) to meet the emission regulation over the UWB from 3.1 to 10.6 GHz [5].

The wirelesses interconnect technology operates on a unique interchip wireless channel. The transmission gain of the channel is defined using the S-parameter between a pair of antennas as

$$G_{\rm tr} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}. \tag{1}$$

$G_{\rm tr}$ is the ratio of the received power to the transmitted power when both antennas are conjugately matched. Fig. 2 shows the value of $G_{\rm tr}$ versus frequency at a separation distance of 20 cm for the on-package monopole antenna pair in a multichip module in free space. As seen from the figure, the transmission gain fluctuates with frequency because of the multipath propagation between the pair of antennas. The locations of the deep nulls depend on the structure and geometry of the multichip module. It is found that the average value of $G_{\rm tr}$ is -31 dB at 3.1 GHz and increases to -30 dB at 6.85 GHz but decreases to -44 dB at 10.6 GHz.

The interchip wireless channel can be regarded as a Rician fading channel. This treatment agrees with the measurements of the radio signal transmission from 2 to 12 GHz where the line-of-sight (LOS) path exists. In addition, the time-delay spread of the intrachip wireless channel is calculated to be negligible as compared with the data rate considered here, and the external interferences are insignificant as the module can be well shielded. Hence, over such a nondispersive Rician fading channel, the system performance depends on the signal-to-noise ratio (SNR). The thermal noise dominates the switching noise for interchip wireless communications. This is because most of the switching noise coupled to the antenna is common-mode in nature. The circuitry can be designed in differential structures to reject most of the common-mode noise [1]. Hence, the bit-error-rate (BER) performance of the BPSK impulse radio can be evaluated as

$$\text{BER} = P_e = \int_0^\infty P_e(X)p(X)dX \tag{2}$$

where $P_e(X)$ is the probability of error for the BPSK modulation at a specific value of SNR X, $X = \alpha^2 E_{rb}/(N_o + S_o)$, and $p(X)$ is the probability density function of X due to the fading channel. E_{rb}, N_o, and S_o are constants that represent the average energy per bit, the thermal noise power density, and the switching noise power density in a nonfading additive white Gaussian noise (AWGN) channel. The random variable α^2 is used to represent instantaneous power values of the fading channel, with respect to the nonfading $E_{rb}/(N_o+S_o)$ [2]. Using the complementary error function, $P_e(X)$ for the BPSK modulation is given as

$$P_e(X) = \frac{1}{2}\text{erfc}(\sqrt{X}). \tag{3}$$

For the intrachip wireless channel, the fading amplitude α has a Rician distribution, so the fading power α^2 and consequently X can be expressed as

$$p(X) = \frac{1+K}{\Gamma}\exp\left(-\frac{X(1+K)+K\Gamma}{\Gamma}\right) \times I_o\left(\sqrt{\frac{4(1+K)KX}{\Gamma}}\right) \tag{4}$$

where $\Gamma = \overline{\alpha}^2 E_{rb}/(N_o + S_o)$ is the average value of the SNR, K is the specular-to-random ratio of the Rician distribution, and $I_o(y)$ is the zeroth-order modified Bessel function of the first kind. Substituting (3) and (4) into (2) and solving the infinity

integration, we obtain the BER performance of the BPSK impulse radio. The average energy per bit $E_{\rm rb}$ is given by

$$E_{\rm rb}\,({\rm dBm}) = E_{\rm tb}\,({\rm dBm}) + G_{\rm tr}\,({\rm dB}) + G_r\,({\rm dB}) + G_m\,({\rm dB}) \tag{5}$$

where $E_{\rm tb}$ is the transmitted energy per bit, $G_{\rm tr}$ is the average value of the transmission gain between the transmit and receive antennas, G_r is the gain of the receiver, and G_m is an implementation margin. G_m is -15 dB, including -10 dB for the reduction of $G_{\rm tr}$ due to inevitable metal lines in between the transmit and receive antennas and -5 dB for other marginal loss. The thermal noise power spectral density N_o is given by

$$N_o = kT_oF = kT_o\left(\frac{T_{\rm ant}}{T_o} + F_r\right) \tag{6}$$

where k is the Boltzman constant, T_o is the reference temperature (typically taken as 290 K), $T_{\rm ant}$ is the antenna temperature (taken as 330 K due to hot chip environment), and F_r is the receiver noise figure. The switching noise power spectral density S_o is given by

$$S_o = \frac{\sum_i \sum_j \frac{\chi_{ij} A_{ij}^2}{2}}{B_W} \tag{7}$$

where χ_{ij} is the ith coupling factor from the jth switching noise source, A_{ij} is the amplitude of the ith harmonics from the jth switching noise source within the system bandwidth B_W. Considering a single dominant switching noise source, the measured switching noise was found to be 10 dB lower than the thermal noise [9]. In a multichip module, there is a large number of switching noise sources; they will increase the switching noise level. Nevertheless, the switching noise will not exceed the thermal noise because of its common-mode nature, which can be effectively suppressed with the balanced antenna and the differential receiver. In the following BER calculation, H indicates the switching noise being either 10 or 5 dB lower than the thermal noise.

Fig. 3 shows the BER performance of the BPSK impulse radio for the case of the ratio K of 10 dB and G_r of 15 dB. As shown, the BER performance degrades with data rate. Taking the worst case ($G_r = 15$ dB, $F_r = 15$ dB, and $H = 5$ dB) as an example, for the fixed 20-cm distance, it degrades from 10^{-8} at 1 Gb/s to 10^{-7} at 2.5 Gb/s. Thus, it is feasible to achieve a high data rate compatible to PCIe at 2.5 Gb/s with a low BER $< 10^{-6}$ over the entire module of size 20×20 cm^2.

III. Hardware Design of Impuse Radio in CMOS

Having understood that the interchip wireless channel can support the data rate as high as PCIe, we proceed to design impulse radio in a 0.18-μm CMOS process. The block diagram of the proposed UWB impulse-radio transceiver architecture is shown in Fig. 4. The building blocks of the UWB transmitter comprises a UWB Gaussian pulse generator, modulator, and

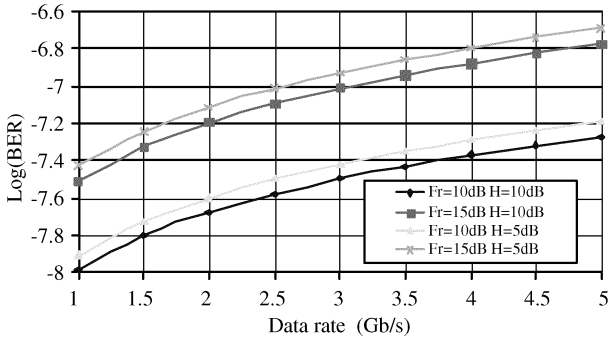


Fig. 3. BER versus data rate.

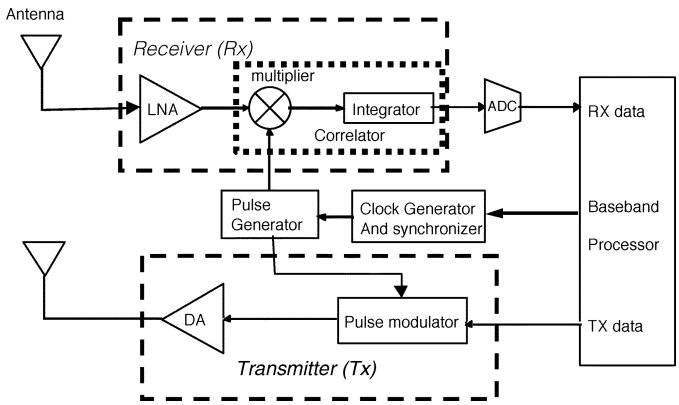


Fig. 4. Architecture of UWB wireless transceiver.

UWB driver amplifier (DA) [10]. The Gaussian pulse generator generates a UWB Gaussian pulse and the UWB pulse modulator modulates the pulse. The modulated UWB Gaussian pulse is then amplified by the UWB DA. Subsequently, the UWB antenna transmits the amplified pulse wirelessly. The receiver consists of a UWB low-noise amplifier (LNA), a correlator (including a multiplier and integrator), an analog-to-digital converter (ADC), and clock generation and synchronization circuits [11]. The UWB LNA is matched to the UWB antenna by means of a matching network. The purpose of the UWB LNA is to amplify the received pulses to a suitable level for signal processing as well as to provide enough gain so as to overcome noise in subsequent stages. The data is subsequently recovered by the correlator. The ADC is used to convert the analog demodulated signal into the digital signal. The digital baseband provides control for the clock generation, synchronization, and data processing.

A. Low-Temperature Cofired Ceramic (LTCC) Antenna

An impulse radio requires UWB antennas. The design of the UWB antenna in CMOS should be avoided because of the lossy nature of the CMOS substrate. Instead, the UWB antenna is designed on the package that carries the chip in LTCC. Fig. 5 shows the photograph of the on-package monopole antenna. The on-package antenna has a return loss lower than -10 dB from 3.1 to 10.6 GHz, indicating an acceptable matching to a 50-Ω source. The on-package monopole antenna was fabricated in the LTCC substrate with a dielectric constant of 5.9 and a thickness of 0.8 mm. The on-package monopole antenna is a linear silver structure that is 15-μm thick, 8-mm wide, and 15-mm long.

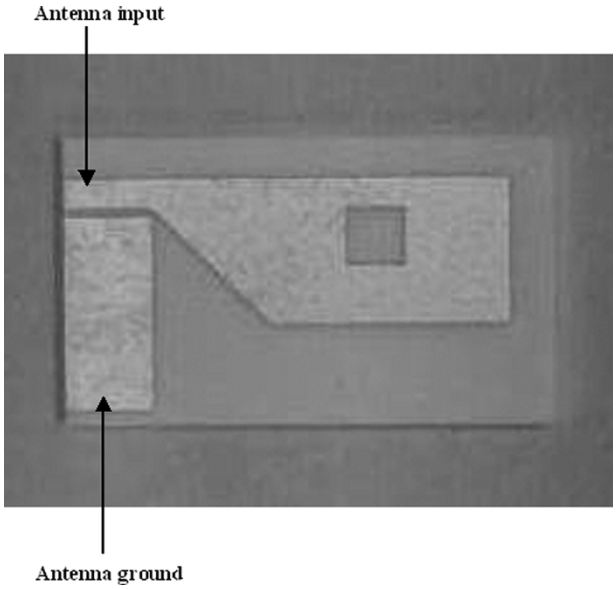


Fig. 5. UWB antenna in LTCC.

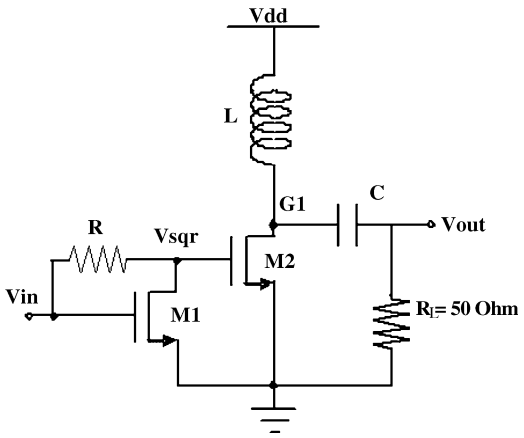


Fig. 6. UWB pulse generation circuit.

B. Pulse Generator and Modulator

The proposed monocycle pulse generation circuit implemented in CMOS process is shown in Fig. 6 [10]. The square circuit is composed of transistor M1 and resistor R. When M1 is biased in the saturation region, the drain voltage of M1 can be written as

$$V_{\rm sqr} = V_{\rm in} - R\frac{K}{2}(V_{\rm in} - V_{\rm th})^2. \tag{8}$$

If choosing

$$R = \frac{2}{KV_{\rm th}} \tag{9}$$

then (8) becomes

$$V_{\rm sqr} = -\frac{1}{V_{\rm th}}\left(V_{\rm in} - \frac{3V_{\rm th}}{2}\right)^2 + \frac{5V_{\rm th}}{4} \tag{10}$$

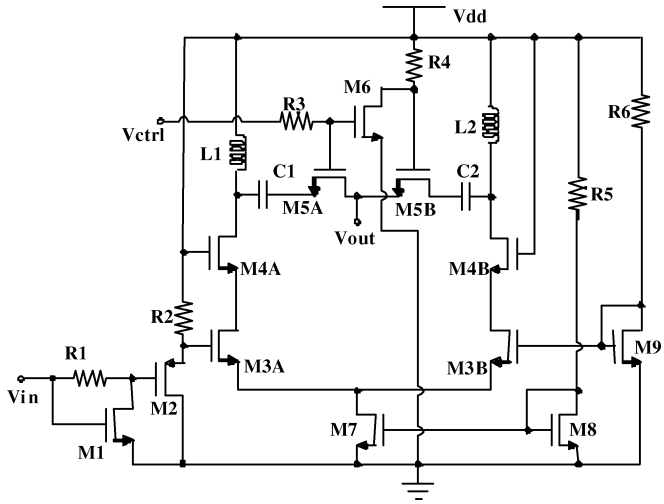


Fig. 7. Pulse modulation circuit.

where $V_{\rm th} < V_{\rm in} < 2V_{\rm th}$ should be satisfied to keep M1 in the saturation region. Thus, a two-quadrant voltage square circuit is implemented as indicated by (10).

NMOS transistor M2 is biased in the weak inversion region so that exponential I–V characteristics can be obtained as follows:

$$I_{\rm DS2} = \kappa_e e^{\frac{V_{GS2}}{\lambda}} = \kappa_e e^{\frac{V_{\rm sqr}}{\lambda}}. \tag{11}$$

Here, κ_e and λ are process-dependent parameters. Obviously, exponential I–V characteristics [see (11)] can also be realized with bipolar transistors. The second-order derivation circuit is implemented by an *RLC* network in Fig. 6. The trans-impedance of the *RLC* network in the s domain is

$$T(s) = \frac{V_{\rm out}(s)}{I_{\rm DS2}(s)} = \frac{sR_LL}{R_L + sL + \frac{1}{sC}}. \tag{12}$$

In RF integrated circuits, the values of on-chip inductors and metal–insulator–metal (MIM) capacitors are typically in the ranges of 1–10 nH and 0.3–6 pF, respectively. If taking the load resistance R_L as 50 Ω, the approximation of $R_L + sL \ll 1/sC$ is sufficiently accurate in the desired frequency range (1–5 GHz). Thus, (12) can be approximated to

$$V_{\rm out}(s) \approx R_LLCs^2I_{\rm DS2}(s). \tag{13}$$

Obviously, the output $V_{\rm out}$ is a second derivative of the drain current $I_{\rm DS2}$. Combining (10), (11), and (13) or cascading the three stages as shown in Fig. 6, a monocycle pulse generator is realized.

A pulse modulation circuit implemented in a CMOS technology is shown in Fig. 7. Two CMOS pulse generators are composed of R1, M1, M2, M3A-M3B, and M4A-M4B. Here, M3A and M4A work in the weak inversion region to provide an exponential current function. Cascoded transistors M4A and M4B are used to improve the inverse isolation. Current sources M7 and M8 are employed to provide high output impedance, so that the current in the left side of the modulator can be mirrored to

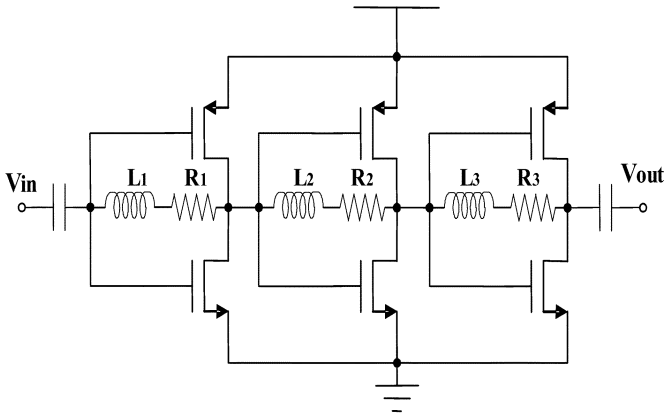


Fig. 8. Driver amplifier circuit.

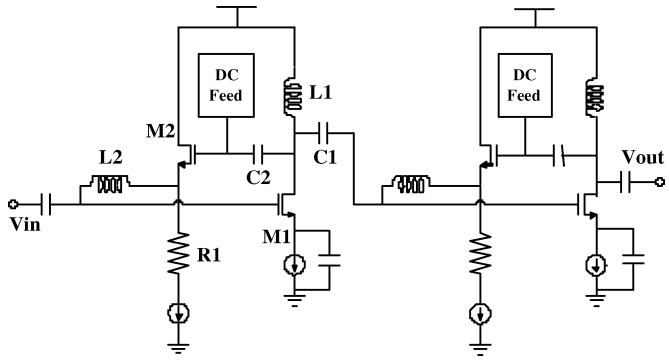
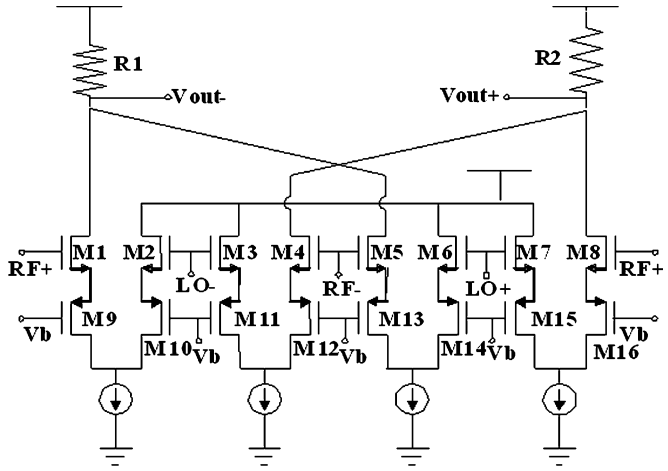
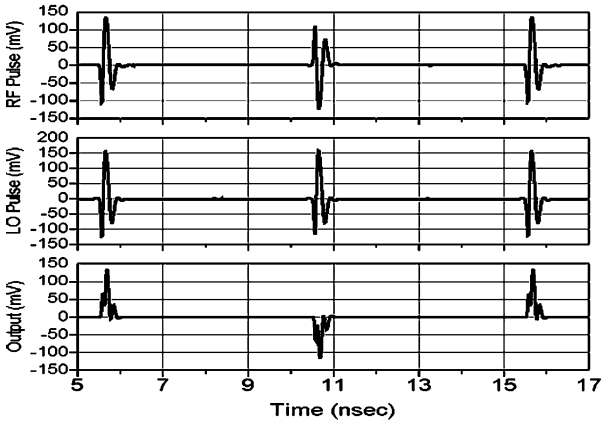


Fig. 9. LNA circuit.



(a)



(b)

Fig. 10. Multiplier. (a) Circuit schematic. (b) Simulation results of pulse multiplication.

the right side. As explained in [10], the second-order derivative current of Gaussian pulses with reverse polarities are formed at the output of the *LC* networks. M_{5A} and M_{5B} are used as two transmission gates and biased by complimentary control voltages. Thus, at one time only, one current can pass through the capacitor C_1 or C_2 and feeds the 50-Ω load to form a positive or negative monocycle pulse. The polarity of the output pulse is determined by the control voltage's level. The detailed simulation results of the pulse generator and modulator have been reported in [10].

C. Driver Amplifier

The design of the driver amplifier involves complex tradeoff between noise gain, matching, power consumption, and linearity. The schematic diagram of the proposed UWB DA is shown in Fig. 8. It consists of three cascade stages. Each stage is a shunt-feedback common-source amplifier with resistor and inductor feedback, where the pMOS–nMOS current reuse technique is employed to improve the gm and thus the gain without sacrificing the bandwidth [12].

D. LNA

A CMOS LNA design has been reported in [13]. It needs five inductors and occupies a large area. Fig. 9 shows a new design of a two-stage cascaded LNA, where each stage is essentially an inductor-peaking shunt-feedback amplifier. The feedback loop is formed by C2, M2, and L2 and used for bandwidth expansion. The source follower circuit consisting of M2 and R1 is used to provide dc bias for M1. Inductor L2 is used to provide the dc bias to M1 and isolate the ac signal path as well as for feedback peaking. *LC* loading L1 and C1 are tuned to boost the gain.

E. Multiplier

A symmetrical multiplier, as shown in Fig. 10(a), is employed to implement the square function. The multiplier core consists of transistors M1–M8 and R1 and R2 [14]. M9–M16 are cascaded to improve the port-to-port isolation for reducing the output dc offset. For noncoherent demodulation, the RF port is connected to the local oscillator (LO) port, and thus the multiplier can act as a squarer. When the external synchronization mechanism is available, the multiplier can be used as a correlator for coherent demodulation, where the transmission rate is expected to be much higher. This multiplier achieves 5-dB conversion gain and 1.75-GHz bandwidth. The simulated performance of a pulse multiplication is shown in Fig. 10(b). The first two signals are RF and LO input, respectively. The third signal is the output of the multiplier.

F. Integrator

In order to maintain a steady integration level in response to a pulse input and hold it for at least 5 ns (for a 100-Mb/s

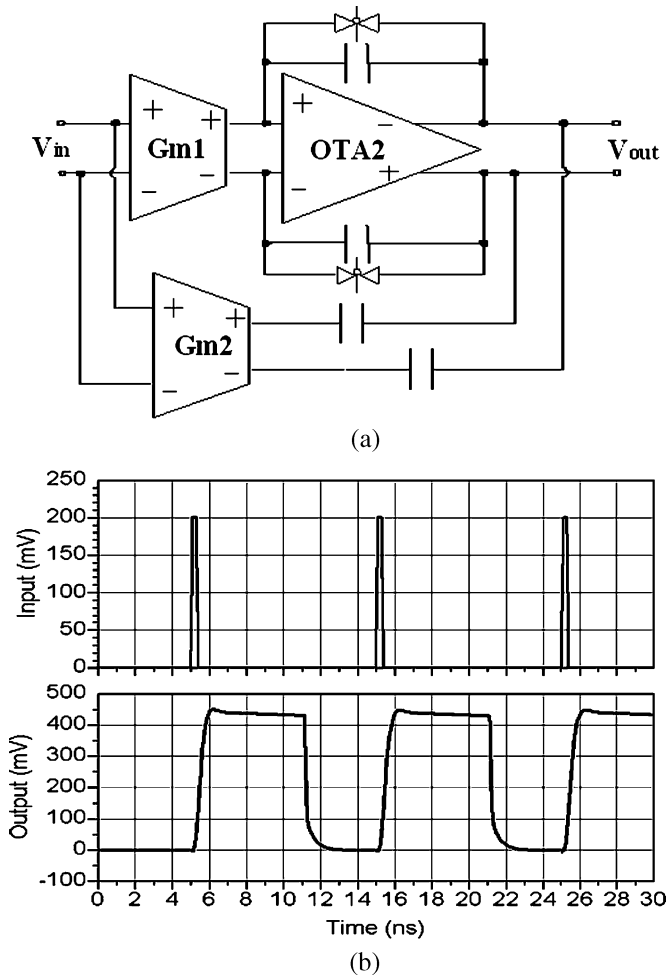


Fig. 11. Gm-C-OTA integrator. (a) Circuit schematic. (b) Transient response to a narrow pulse.

transmission rate) to facilitate the A/D conversion, the integrator should be made as lossless as possible. This implies a very low −3-dB frequency. On the other hand, the integration response time should be short so that the ADC would have enough time to perform conversion. This means that the integrator should have a high slew rate and fast settling behavior.

The block diagram of the implemented integrator is shown in Fig. 11(a). Due to the Miller effect, the parasitic capacitors' impact is reduced and the requirements for output impedance and output swing of transconductor are relaxed. By modeling the transconductor and the operational transconductance amplifier (OTA) as two separate first-order low-pass systems, we can obtain that the −3-dB bandwidth is $\omega_o = p_1 \approx 1/R^*_{\text{out\_gm}}C^*A_{\text{OTA}}$, and the overall dc gain is $A_{\text{DC}} = A^*_{\text{gm}}A_{\text{OTA}}$, where A_{gm}, A_{OTA}, and $R_{\text{out\_gm}}$ are the dc gain of the Gm cell, the dc gain of the OTA, and the output resistance of the Gm cell, respectively. The unity gain bandwidth (GBW) is $\omega_u \approx g_m/C$. It is clear that, for a given ω_u, a low −3-dB bandwidth is much easier to achieve in a Gm-C-OTA integrator than in a Gm-C integrator (the −3-dB bandwidth can be A_{OTA} times lower). To achieve high integration speed and short rising time of less than 1 ns, large output current is used

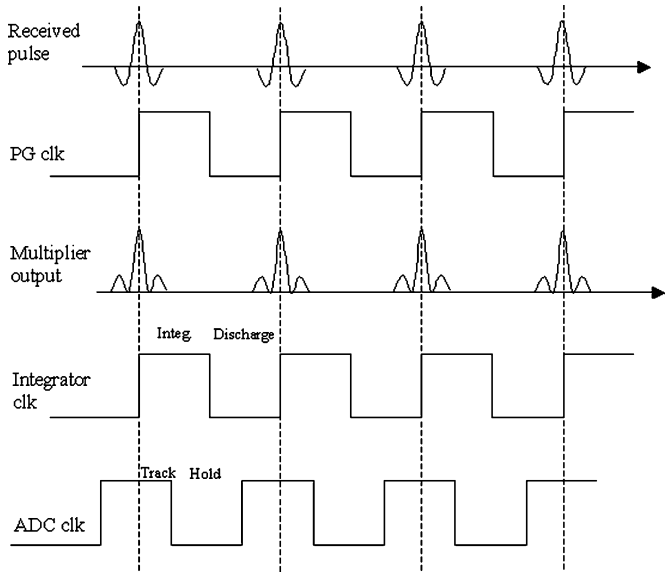


Fig. 12. Clock timing of the receiver.

to obtain a high slewing rate. Another parallel transconductor is used to create a feedforward path for compensating the high-frequency response and building the rapidly rising edge of the output signal [15].

To clear the previous integration value before the next period comes, the voltage of the output nodes and the interstage nodes are set to their corresponding dc voltage periodically by turning on switches implemented with CMOS transmission gates. The discharging time can be set to half of a period cycle. The clock for nMOS/pMOS transistors is provided by the clock generator. The transient circuit simulation result [see Fig. 11(b)] shows that the integrator has a fast response to a narrow pulse and long holding time. The integration rising time is around 1 ns, and the discharging edge is sharp and has no ringing. Due to the Gm-C-OTA structure, its frequency response has a reduced −3-dB bandwidth of 1 MHz and increased GBW of larger than 1 GHz, which result in large correlation gain and longer holding time of 10 ns with less than 3% charge error.

G. Clock Generator and ADC

An ADC employing full flash architecture and sampling rates up to 500 Msample/s can be employed after the integrator, and 4-b resolution is enough for baseband signal processing including synchronization and equalization.

Clocks for pulse generator, integrator, and ADC are provided outside the receiver chip. Two cascaded delayed locked loops (DLL) are used as a mutiphase clock generator and synchronizer, which provide delayed shifts of the clocks. It can work at clock rates from 100 to 500 MHz, and the clock has an output swing of 1 V, jitter of less than 30 ps, and duty cycle of ∼50%. The first DLL delays the clock by the minimal step of 1 ns (coarse delay), and the second DLL further delays the clock with a resolution of 0.1 ns (fine delay). By cascading two DLLs with proper logic control, the output clock can be shifted with a step of 0.1 ns within 10 ns. Coherent demodulation will take place

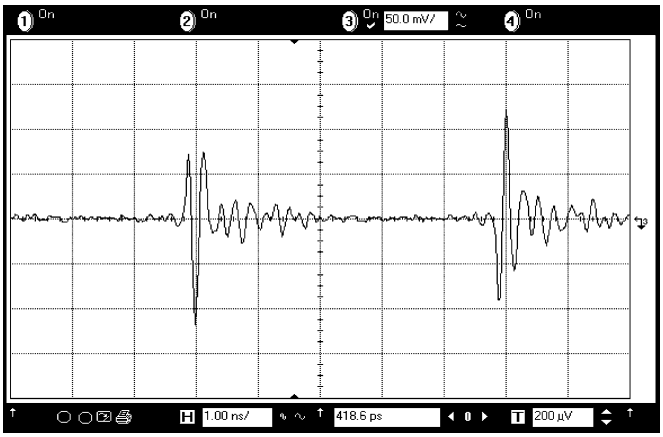


Fig. 13. Measured BPSK pulses.

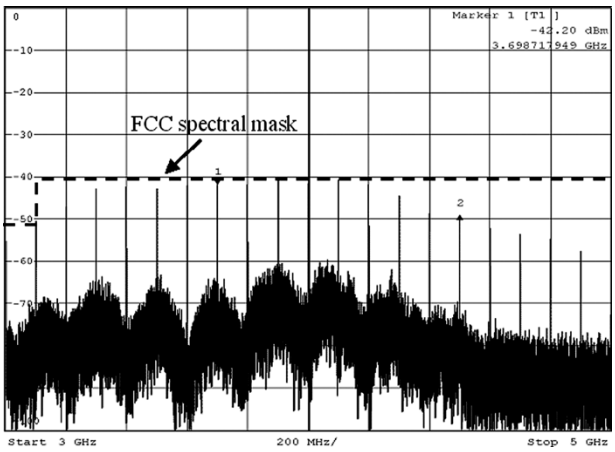


Fig. 14. Measured frequency spectrum of pulses.

once the DLL is locked to synchronize the local pulses (triggered by a shifted clock) with the received pulses.

Taking a 100-Mb/s transmission rate as an example, the clock timing for pulse generator, integrator, and ADC is shown in Fig. 12. In each period, once the clock rising edge for the pulse generator is synchronized with the received pulse, the multiplied pulse comes out and the integrator starts integrating. A half period of time is used for integration, and a half period of time is used for discharging. The tracking time of the ADC is about one quarter of period ahead of the discharging time, so that a stable sampling can be taken.

IV. Experimental Results

Typical measured BPSK-modulated pulses at the output of the transmitter are shown in Fig. 13. The Gaussian monocyle pulses are generated. Here, the pulse repetition rate (PRR) is 200 MHz. The pulse output swing is adjustable in 40 800 mV with a pulsewidth of less than 1 ns. A typical measured spectrum of the pulse sequence (PRR of 100 MHz) is shown in Fig. 14. The -10-dB bandwidth is observed from 3.1 of 4.4 GHz within the FCC spectrum mask.

In Fig. 15, It can be seen that the DA has a measured -3-dB bandwidth of 1.1 to 9.2 GHz, a power gain of 19–21 dB, and a low noise figure of 3.2–3.6 dB. The input referred third-order intermodulation point (IIP3) is -10 dBm measured at the central frequency of the passband (5.05 GHz), shown in Fig. 15(c). Here, the DA design covers the full band for future exploitation although, in this paper, the transceiver only works in the FCC low band (3.1–5 GHz). Shown in Fig. 16, the measured LNA has a power gain (S_{21}) of 18 dB with 0.5-dB passband ripple, input reflection coefficients (S_{11}) < -10 dB, noise figure of 4.0–4.6 dB, and -3-dB bandwidth around 2.5 GHz. Compared with that in [13], the much higher gain is obtained with the tradeoff of narrower bandwidth and is sufficient for UWB low-band applications. The measured integrator performance is shown in Fig. 17. It is quite close to the simulation result in the integration rising time (1 ns). The effective holding time is around 2 ns, and the discharge rate is slower than the simulated one. This may be due to the leakage current which is larger than the simulated results.

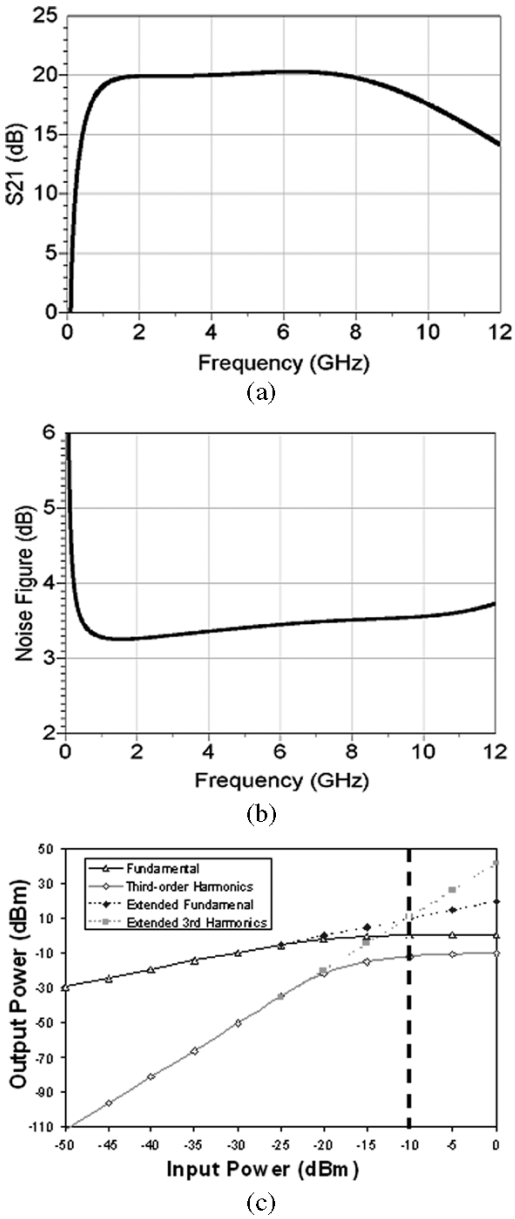


Fig. 15. Measured DA. (a) Gain. (b) Noise figure. (c) IIP3.

The feasibility of UWB impulse radio for interchip wireless communication is verified in this study. The microphotograph

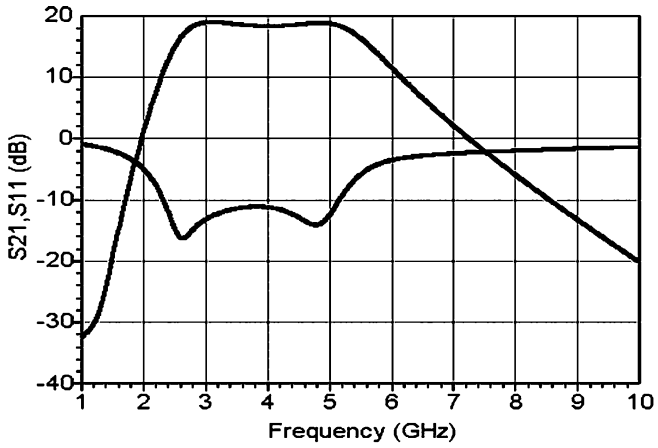


Fig. 16. Measured LNA. (a) Gain and reflection coefficients. (b) Noise figure.

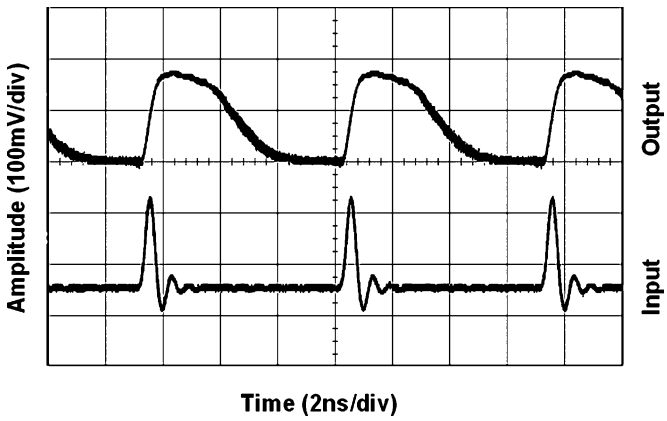


Fig. 17. Measured integrator performance.

of the impulse-radio transceiver chip is shown in Fig. 18, and the transceiver performance is summarized in Table I. The sensitivity here is defined as the weakest pulse signal level that can be detected and demodulated by the receiver. Although the tested maximum pulse transmission rate is 200 Mb/s, we believe the much higher data rate can be achieved if employing a much advanced submicrometer CMOS process and proper UWB circuit design. We are moving to 90-nm CMOS for the impulse-radio design, which make the Gb/s transmission data rate possible.

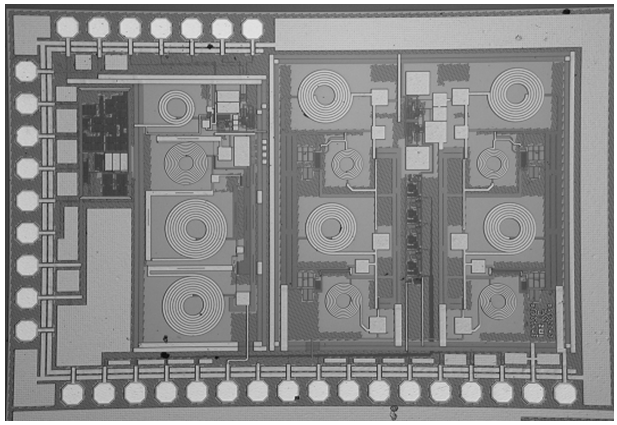


Fig. 18. Chip microphotograph.

TABLE I
SUMMARY OF TX AND RX PERFORMANCE

Receiver		Transmitter	
RX Noise Figure	7.5 dB	Transmitted PSD	-41.3 dBm/MHz (3.1-5GHz)
RX Gain ADC Power	80 dB	Pulse Width	< 1 ns
IIP3 at Max Gain	-12 dBm	TX Bandwidth (-10dB)	1.5 GHz
IIP3 at Reduced Gain	-2 dBm	TX Power Dissipation	21 mW
RX P-1 dB	-22 dBm	TX Rate	100-200 Mbps/s
Sensitivity	-78 dBm		
RX Power Dissipation	99 mW	Clock Generator Output swing	~30 mV
VGA Gain Range	-10 ~ 45 dB	**Overall**	
ADC Resolution	4 bits	Supply Vol.	1.8 V
ADC Sampling Rate	100-500 MSamples/s	Technology	0.18-μm CMOS
ADC Power	45 mW	TRX Die Size	2.32 mm ×1.75 mm

V. CONCLUSION

A novel wireless interconnect technology using UWB impulse radio was proposed for interchip communications. The BER performance of this wireless interconnect system was analyzed. A prototype of the impulse-radio transceiver ICs has been fabricated in a 0.18-μm CMOS process with an LTCC antenna. The measured prototype impulse radio achieved a data rate of 165 Mb/s over the interchip wireless channel of length 20 cm with a power consumption of TX 21 mW and RX 99 mW. An improved design in 90-nm CMOS process is now under development, and a much faster speed is expected.

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