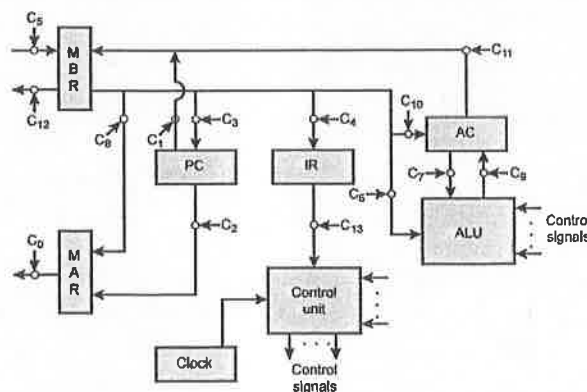
 VIT-AP UNIVERSITY	Final Assessment Test – Long Summer (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization & Architecture	
Set No: 2	Exam Type : Closed Book	School: SENSE
Date: 20-07-2024	Slot: C	Session: AN
Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice		
General Instructions if any: <ol style="list-style-type: none"> 1. "fx series" - non Programmable calculator are permitted: NO 2. Reference tables permitted : NO 		

Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. What are basic functions of a computer? Discuss with some real-life example. (10 M)
2. Discuss Moor's Law and its significance. (10 M)
3. Depict the restoring division Algorithm flowchart and perform binary operation to perform 9/3. (10 M)
4. Discuss IEEE 32-bit Floating point representation and present 123.55 in this format. (10 M)
5. Develop an 8086 Assembly Language Program (ALP) to find a number in an array of 50 numbers located at 3000H: 7000H. An optimum ALP is expected. (10 M)
6. Draw and discuss the flag register of 8086 microprocessor. (10 M)
7. What is pipelining in microprocessors and what are its hazards? (10 M)
8. (10 M)




For the IAS computer instructions, LOAD 350; SUB 300; derive the hardwire control unit using state table method. Use the above diagram to identify the control signals.

9. Draw the microprogrammed control unit. (10 M)
10. Discuss the memory hierarchy in computer. What is the need for this hierarchy? (10 M)
11. Perform the memory mapping between the Cache memory of 64 kB to the main memory of 8 GB using 4 way set associative method where the block or page or frame size is of 8 KB. (10 M)
12. A computer has the following memory capacity: Ram: 4 GB (10 M)

Cache: 8 kB

Block size: 32 Bytes

Perform the One-way Set Associative Mapping and discuss the searching process with suitable diagrams.


 VIT-AP UNIVERSITY	Final Assessment Test – Short Summer-II (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization and Architecture	
Set No: 2	Exam Type : Close Book	School: SENSE
Date: 20-07-2024	Slot: C	Session: FN
Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice		
General Instructions if any:		
1. "fx series" - non Programmable calculator are permitted: NO 2. Reference tables permitted: NO (if Yes, Please specify: NA)		

PART – A: Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

- Q1.** Explain how to represent the number -41.125 using the IEEE 32-bit floating-point format? (10M)
- Q2.** Perform -9 by 6 using Booth's Algorithm step by step? (10M)
- Q3.** Describe the different instruction sets used in the 8086 processor with examples for each to illustrate how they work? (10M)
- Q4.** Explain microprogrammed control unit. What are the limitations of microprogrammed control unit? (10M)
- Q5.** Describe the levels of memory hierarchy in terms of speed, size, and cost. Explain the role of primary memory in this context? (10M)
- Q6.** Define pipelining in computer architecture. Discuss its hazards with examples and outline its drawbacks and limitations? (10M)
- Q7.** Show how to represent the numbers -8 and +21 using 8-bit 2's Complement notation? (10M)
- Q8.** Perform the division of -7 by -2 using the restoring division algorithm with clear steps. (10M)
- Q9.** Discuss the various flags used in 8086 microprocessors, provide the examples to illustrate how each flag is set or cleared during program execution? (10M)
- Q10.** Describe IAS memory machine. (10M)
- Q11.** What do you mean by Interrupt Vector Table (IVT) in an 8086 microprocessor, What is vectored interrupt and non-vectored interrupt? (10M)
- Q12.** What is the key difference between 2nd and 3rd generations of computer, Describe Von-Neumann Computer architecture? (10M)

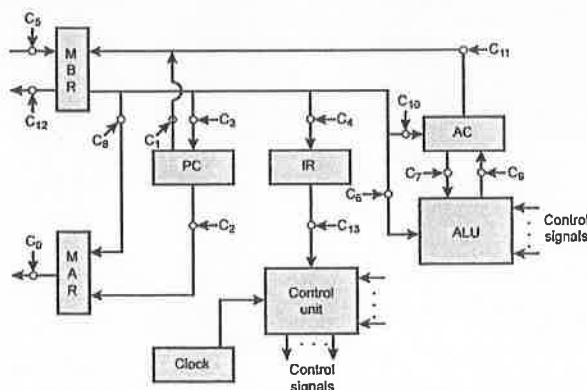
QP MAPPING

Q. No.	E/A/T	Module Number	Marks	BL	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped
Q1	E	1	10	2	1	1,2,3	1,2	1
Q2	A	2	10	3	2	1,2,3	1,2	1
Q3	T	3	10	3	3	1,2,3	1,2	1
Q4	E	4	10	2	4	1,2,3	1,2	1
Q5	A	5	10	2	5	1,2,3	1,2	1
Q6	T	6	10	3	6	1,2,3	1,2	1
Q7	E	1	10	3	1	1,2,3	1,2	1
Q8	A	2	10	2	2	1,2,3	1,2	1
Q9	T	3	10	2	3	1,2,3	1,2	1
Q10	E	1	10	3	1	1,2,3	1,2	1
Q11	A	5	10	3	5	1,2,3	1,2	1
Q12	T	1	10	2	1	1,2,3	1,2	1

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