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QUESTION PAPER

Name of the Examination: FAT (Fall 2023-2024)-FAT

Course Code: ECE2002 **Course Title:** COA

Slot: 01 **Date of Exam:** 01/12/2023 (AN)

Duration: 120 min **Total Marks: 60** (B_2)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

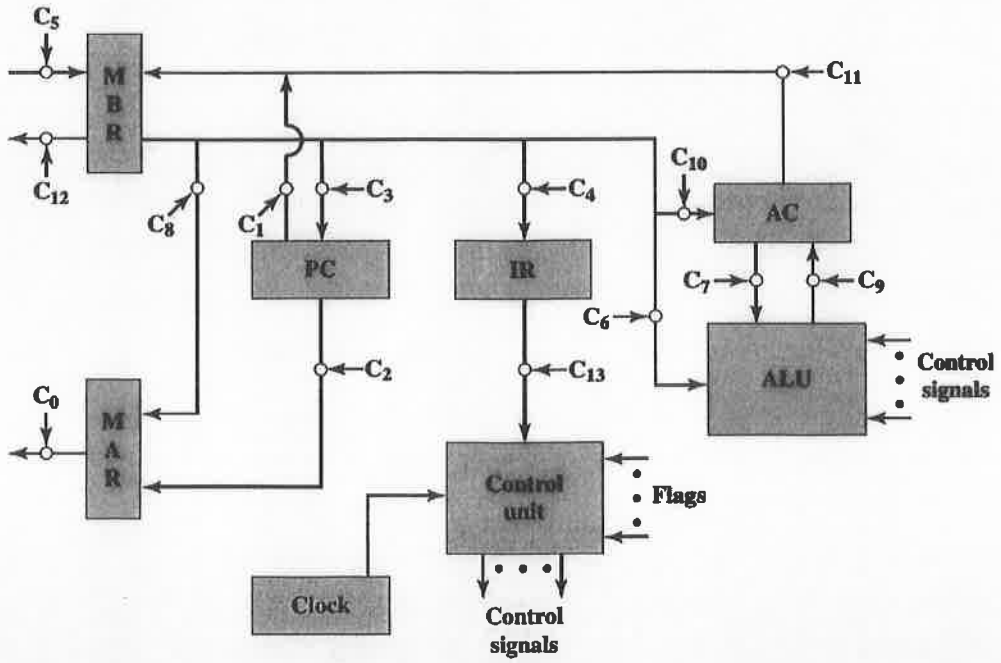
Q1. Demonstrate the multiplication approach using Booth's algorithm to multiply 09 by 08. **(12M)**

Q2. What is the micro-operation required for following instruction?

(a) STC
(b) MOV [R1], R2
(c) ADD R1, [BX] **(12M)**

Q.3. Referring to the figures below,

(a) Depict the control signals required for the fetch and execution cycle of ADD 200.
(b) Express the Boolean expression for each of the control signals.
(c) Implement the Boolean expressions for each of the control signals using a minimum number of gates. **(12M)**



Q4. An 8-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 24 bits. The size of the physical address space is 4 GB. Calculate the number of bits required for the SET field and TAG field. **(12M)**

Q5. A four-stage pipeline has stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to execute 1000 instructions on the pipeline will be? **(12M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1	1	2	12
Q2	3	3	1	2	1	12
Q3	4	4	1	3	1	12
Q4	5	5	2	4	3	12
Q5	6	6	2	3	3	12

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QUESTION PAPER

Name of the Examination: Fall 2023-24 Semester – FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 02 **Date of Exam:** 02/12/2023 (AN) (G1)

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Compute the product -5 × -7 using 4-bit twos complement notation based on Booth's algorithm? **(12M)**

Q2. Explain the concept of interrupts and the role of the Interrupt Vector Table (IVT) in managing interrupts in the context of 8086 microprocessor architecture. Provide examples of non-maskable and maskable interrupts? **(12M)**

Q3. A 5-stage pipelined processor has the stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any instruction. The execution stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. **(8 + 4 = 12M)**

a. How many clock cycles are required to execute the following sequence of instructions with pipelining? Prepare the pipeline diagram.

MUL R2, R10, R1

DIV R5, R3, R4

ADD R2, R5, R2

SUB R5, R2, R6

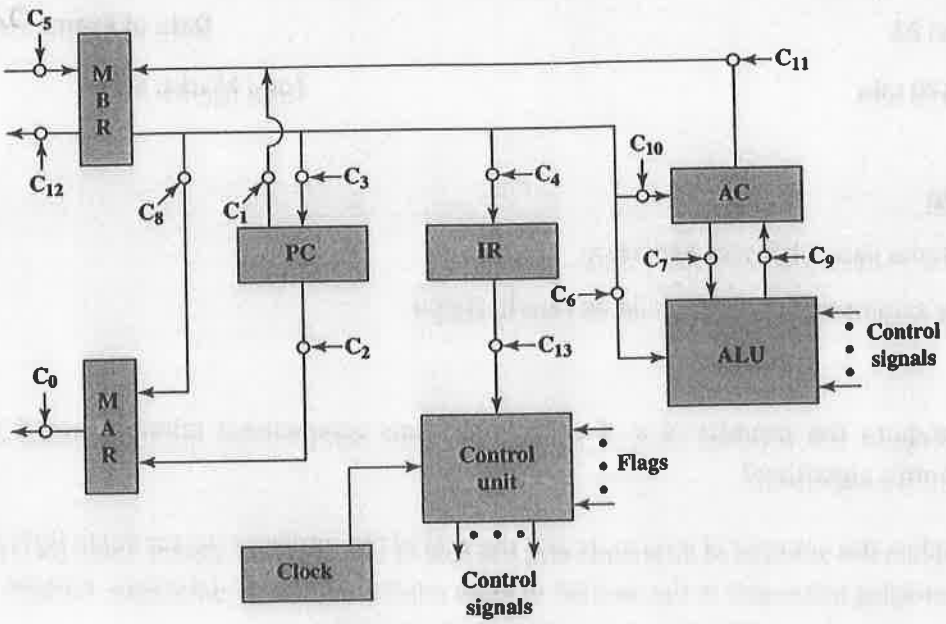
b. If the Microcontroller frequency is 2MHz, what is the operating frequency? Also calculate the number of clock cycles without pipelining.

Q4. List the sequence of micro-operations and corresponding active control signals of the following instructions in a tabular form for the processor shown in the below figure. **(3 + 3 + 3 = 12M)**

a) ADD R1, [5000H]
(Meaning: Add the contents of memory location 5000H with register R1)

b) MOV R1, [R2]
(Meaning: R1 register gets the data from memory location pointed by R2)

c) Jump if AC = 0



Q5. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. **(3 + 4 + 3 + 2 = 12M)**

a. How is a 16-bit memory address divided into set number, block number, and location number?

b. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

d. How many total bytes of memory can be stored in the cache?

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1, 2, 3	1	1	12
Q2	3	2	1, 2, 3	1	1	12
Q3	6	6	1, 2, 3	1	1	12
Q4	5	3	1, 2, 3	1	1	12
Q5	4	4	1, 2, 3	1	1	12

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Name of the Examination: Final Assessment Test (FAT)

Fall Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 06 **Date of exam:** 04/12/2023 (AN) (D2)

Duration: 120 mins **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform the -14/11 using restoring signed division algorithm. [12]

Q2. Explain the micro operations of the following instructions of 8086 and IAS computer [4+4+4]

a. MOV AX, BX
b. AND AX, [1000H]
c. STOR M(200)

Q3. The alphabet "B" of a keyboard is pressed which is connected to the INTR pin of an 8086 processor. Explain the steps associated to execute the interrupt requested through the keyboard. Write a program to initialize the keyboard interrupt in vector table with interrupt vector 52H. The ISR of the keyboard interrupt is stored in offset address 4032H in data segment with segment address 2000H. [12]

Q4. A processor has 64 GB of RAM and 2MB of cache memory. If the size of the cache block is 128 bytes, then explain the mapping structure using 32-way associative mapping with a suitable diagram. Besides, find the following parameters [12]

a. Number of searches
b. Number of blocks in a set
c. Number of blocks in the RAM
d. Number of sets in the RAM
e. Tag size
f. Memory address structure

Q5. Design a microcontroller instruction pipeline to execute a program which has 6 instructions. Each instruction has 4 pipeline stages in the following order – Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), and Register Write Back (WB). The fetch operation takes 1 clock cycle, decode operation takes 1 clock cycles, and register write back takes 2 cycles. The execution operation takes various clock cycles in each instruction whose values are (in the order of each instruction) 2, 5, 7, 6, 4, 2 clock cycles. [6+6]

a. With necessary diagrams, calculate the total number of clock cycles that will take to execute the program using pipeline. If the microcontroller is given a

clock with input clock frequency 1.5 GHz, what is the maximum clock frequency with which the microcontroller can operate?

b. If the instruction pipeline is flushed after every 2 instructions, calculate the total number of clock cycles taken.

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1,2,3	1,2	1	12
Q2	3	4,5	1,2,3,5	1,2	1	12
Q3	4	4	1,2,3,5	1,2	1	12
Q4	5	3	1,2,3,5	1,2	1	12
Q5	6	6	1,2,3,5	1,2	1	12

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QUESTION PAPER

Name of the Examination: FAT (FALL 2023-2024)

Course Code:	ECE2002	**Course Title:**	Computer Organization and Architecture
Set number:	08	**Date of exam:**	30/11/2023 (AN)(A2)
Duration:	120 mins	**Total Marks:**	60

Instructions:

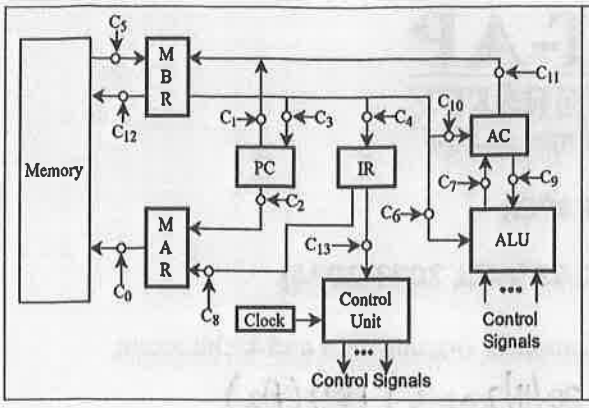
1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Consider the division of two signed numbers, -24 (dividend) and 5 (divisor), using the restoring algorithm. **[10]**

Q2. Give a detailed description about Interrupt Vectors. Draw a circuit diagram to show how a device with interrupt vector 45H can be connected on an 8088 microprocessor system. Using the Interrupt Vector Table shown below, determine the address of the ISR of a device with interrupt vector 45H **[15]**

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00000	3C	22	10	38	6F	13	2C	2A	33	22	21	67	EE	F1	32	25
00010	11	3C	32	88	90	16	44	32	14	30	42	58	30	36	34	66
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00100	4A	33	3C	4A	AA	1A	1B	A2	2A	33	3C	4A	AA	1A	3E	77
00110	C1	58	4E	C1	4F	11	66	F4	C5	58	4E	20	4F	11	F0	F4
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00250	00	10	10	20	3F	26	33	3C	20	26	20	C1	3F	10	28	32
00260	20	4E	00	10	50	88	22	38	10	5A	38	10	4C	55	14	54
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
003E0	3A	10	45	2F	4E	33	6F	90	3A	44	37	43	3A	54	54	7F
003F0	22	3C	80	01	3C	4F	4E	88	22	3C	50	21	49	3F	F4	65

Q3. In the following diagram and Table different control signals are given with respect to the different microinstructions occurred during different cycles. Find out the equations and gate level circuits for all the control signals generated during fetch and execution of LOAD 600 instruction. **[15]**



	Microoperations	Active control singals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← PC+1	C_5 , C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	$C_5 C_R$
	t_3: IR(Address) ← MBR(Address)	C_4
Interrupt :	t_1: MAR ← (PC)	C_1
	t_2: MAR ← Save-Address PC ← Routine-Address	
	t_3: Memory ← (MBR)	C_{12} , C_W

Q4 Given a Pentium processor with the following configuration **[10]**

Size of Main Memory	8GB
Size of Cache Memory	16KB
Size of Cache Block	128 Bytes

A Fully Associative mapping is employed. Explain the mapping technique with suitable diagrams. Then find the following

1. Tag Size
2. Number of Search's
3. Method of Searching

Q5 Design a microcontroller instruction pipeline to execute a program which has 6 instructions. **[10]**
Each instruction has 5 pipeline stages in the following order – Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), Memory Access (MEM) and Register Write Back (WB). The fetch operation takes 1 clock cycles, decode operation takes 1 clock cycles, memory access takes 2 cycles and register write back takes 1 cycle. The execution operation takes various clock cycles in each instruction whose values are (in the order of each instruction) 2, 3, 1, 3, 2, 1 clock cycles.

a) With necessary diagrams, calculate the total number of clock cycles that will take to execute the program in pipeline method. (8marks)
b) If the microcontroller is given a clock with input clock frequency 1.5 GHz, what is the maximum clock frequency with which the microcontroller can operate? (2marks)

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1,2	1, 2, 3			10
Q2	3	3	1, 2, 3			15
Q3	4	4	1, 2, 3, 5			15
Q4	5	5	1, 2, 3			10
Q5	6	6	1, 2, 3,5			10

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QUESTION PAPER

Name of the Examination: Fall 2023-24 Semester – FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 10 **Date of Exam:** 30/11/2023 (FN) (AN)

Duration: 120 mins **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Convert the following decimal number into 64-bit IEEE 754 format 62597.57719781 x 2^{-11}. Also convert the given binary number into decimal 1 10010101011 10101111011000000.....0.

(12M)

Q2. For a processor requiring 60 micro-operations for all the instructions, show how this will be implemented using Wilke's design with suitable diagrams. Show how the control signals are generated of any two instructions of your choosing. **(12M)**

Q3. Design the memory mapping between the Cache memory of 16KB to the main memory of 512KB using a 2-way set associative method where the block size is of 2KB. Consider each memory location is byte addressable. Assume the cache is having the below given values from the respective sets of main memory. For example, "S61 B3" represents Block 3 from Set 61 of the main memory. Now, let the CPU is trying to access the memory location 5612. Determine whether you will have a cache HIT or a MISS? **(12M)**

S57 B0
S1 B1
S8 B2
S44 B3
S0 B0
S37 B1
S29 B2
S61 B3

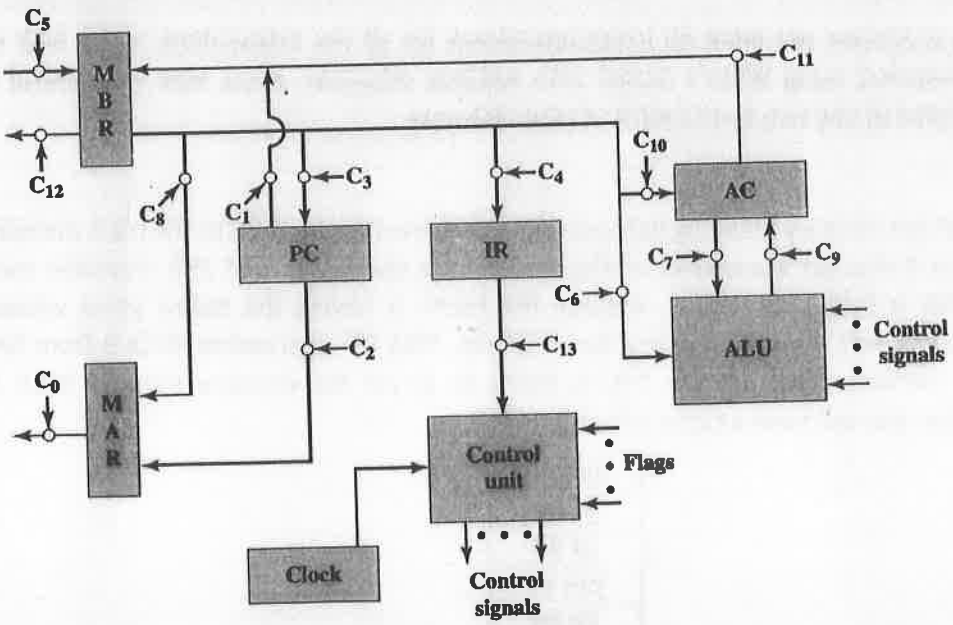
Q5. Explain how the 3-stage and 4-stage pipelined microprocessors work with the help of diagrams and derive the expressions for finding the time required for executing 'n' instructions? Identify the type of hazard that can result, if the following instructions are executed on a pipelined microprocessor and how they can be avoided? **(12M)**

SUB [5000H], AL

MOV BL, [5000H]

Q4. Explain the execution cycle of each of the following instructions in terms of micro-operations and their associated control signals: JMP 200 and CMP R1. JMP 200 will start executing from the address given in the instruction and CMP R1 will compare the registers R1 and AC and if both are equal the next two instructions are skipped. Design a control circuitry for all the control signals for both the instructions using minimum logic gates. **(12M)**

	Micro-operations	Active Control Signals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← (PC) + 1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5, C_R
	t_3: IR(Address) ← (MBR(Address))	C_4
Interrupt:	t_1: MBR ← (PC)	C_1
	t_2: MAR ← Save-address PC ← Routine-address	
	t_3: Memory ← (MBR)	C_{12}, C_W



QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1, 2, 3	1	1	12
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Q3	5	5	1, 2, 3	1	1	12
Q4	6	6	1, 2, 3, 5	1	1	12
Q5	4	4	1, 2, 3, 5	1	1	12