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QUESTION PAPER

Name of the Examination: CAT – 2 (Winter 2021-2022)

Course Code: ECE2002 | **Course Title: COA**

Slot: E2+TE2 | **Date of Exam: 22.04.2022**

Duration: 90 min | **Total Marks: 50**

Class ID: AP2021225000066

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform the division of 16 by 7 using non-restoring algorithm. Mention all the steps clearly. **(10M)**

Q2. Estimate and draw the lower order flag register that will be generated after the following program execution.

MOV AL, 78H

MOV BL, 67H

XOR AL, BL **(10M)**

Q3. Write a program to swap the lower and higher bytes of 10 data stored in the memory which starts from 2000H offset address in a segment where the starting address is 50000H. **(15M)**

Q4. Write a program to count the number of '0's and '1's in a 8 bit data which is stored in the memory location 3000H:1000H. The results should be stored in 3000H:2000H **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3	1	1	10
Q2	3	3	1,2,3	3	3	10
Q3	3	3	1,2,3	3	3	15
Q4	3	3	1,2,3	3	3	15

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QUESTION PAPER

Name of the Examination: CAT – 2 (Winter 2021-2022)

Course Code: ECE2002 | **Course Title: COA**

Slot: E1+TE1 | **Date of Exam: 22.04.2022**

Duration: 90 min | **Total Marks: 50**

Class ID: AP2021225000065

Instructions:

1. Assume data wherever necessary. Answer All
2. Any assumptions made should be clearly stated.

Q1. Perform the division of 16 by -7 using restoring algorithm. Mention all the steps clearly. **(10M)**

Q2. Estimate and draw the lower order flag register that will be generated after the following program execution.

MOV AX, 7890H

MOV BX, 6789H

SUB AX, BX **(10M)**

Q3. Write an efficient program without using string instructions to transfer a string of 16 data bytes from offset 0200H to 0300H in the data segment whose initial address is 70000H. **(15M)**

Q4. Write a program to get Factorial of 10 numbers stored from the starting location 4000H:1000H. The results should be stored in 4000H:2000H **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3	1	1	10
Q2	3	3	1,2,3	3	3	10
Q3	3	3	1,2,3	3	3	15
Q4	3	3	1,2,3	3	3	15

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QUESTION PAPER

Name of the Examination: CAT (Long Summer 2021-2022)

Course Code: ECE2002 **Course Title:** COA

Slot: B+TB+TBB **Date of Exam:** 02/07/2022

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Consider the floating-point number X = 32.50, Y = -15.25 Express X, Y in single precession IEEE 32-bit format. **(10M)**

Q2. Realize the following decimal numbers in sign magnitude and value box representation to store it in a register of 8-bits. (a) -28 (b) 87 (c) -102.

Comment on the differences shown by the two representations in the above question. **(10M)**

Q3. Discuss the required hardware, algorithm for Booth's Multiplication Algorithm. Compute the multiplication result of x and y using Booth's algorithm. Where x = 12 and y = 08 **(10M)**

Q4. Demonstrate the division approach using restoring algorithm to divide 30 by 5. **(10M)**

Q5. Write an assembly language program to calculate the result of the logical expression

$$X = (A \oplus B) + \bar{A}B$$

using 8086 microprocessors. where program starting address is 2000 and the numbers A and B are 8-bit number stored at memory location 3000 and 3001 and store result into 6000 memory address. **(10M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	1	1	1	1	1	10
Q3	4	2	2	2	2	10
Q4	4	2	2	2	2	10
Q5	5	3	2	2	2	10

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QUESTION PAPER

Name of the Examination: RE-CAT (FAST TRACK 2022-2023)

Course Code: ECE2002 **Course Title:** COA

Slot: C+TC+TCC **Date of Exam:** 27/08/2022

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. How floating-point addition is implemented. Consider the floating-point number X = 10.25, Y = -17.70. Compute X+Y and write its equivalent in IEEE 32 bit format **(10M)**

Q2. Realize the following decimal numbers in sign magnitude and 1's, 2's complement to store it in a register of 16-bits. (a) -72 (b) 87 (c) -50.

Comment on the differences shown by the two representations in the above question. **(10M)**

Q3. Discuss the required hardware for Booth's Multiplication Algorithm. Compute the multiplication result of x and y using Booth's algorithm. Where x = -14 and y = 07 **(10M)**

Q4. Demonstrate the division approach using the restoring algorithm to divide 16 by 3. **(10M)**

Q5. Write an assembly language program to evaluate the result of the logical expression

$$X = (A + B) * C + \frac{A}{B} * C$$

using 8086 microprocessors. the numbers A and B are 16-bit number stored at memory location 3000 and 3001 and store result into 6000 memory address. **(10M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	1	1	1	1	1	10
Q3	4	2	2	2	2	10
Q4	4	2	2	2	2	10
Q5	5	3	2	2	2	10

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QUESTION PAPER

Name of the Examination: RECAT – 2 (Winter 2021-2022)

Course Code: ECE2002 **Course Title: COA**

Slot: **Date of Exam:**

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform the division of 17 by -7 using restoring algorithm. Mention all the steps clearly. **(15M)**

Q2. Two floating points numbers are in the format $X = X_s \times B^{X_E}$ and $Y = Y_s \times B^{Y_E}$. Where

$X_s = 1100$ and $Y_s = 1110$

$X_E = 1011$ and $Y_E = 1001$

Show the operation $X \div Y$ and compute the result using Unsigned Binary Division Restoring Algorithm.

(10M)

Q3. List out the content of the affected register after execution following instructions. Assume other general purpose register content initially 0000H and memory locations [7890H] = 55H; [6789H] = 7BH, [8011h] = 99H.

```
MOV AX, 7890H
MOV BX, 6789H
SUB  AX, BX
ADD AL, BL
INC BL
XCHG DL, [8011h]
MOV CL, AL
MOV CH,DH
XOR DH, CL
MUL CL
```

(15M)

Q4. Compute the address of the operand's final memory address for where the content of different registers and memory locations are as follows:

Code Segment Register (**CS**) = 4000h; **IP** = 0305h; **BX** = 0702h; **DI** = 0202h;
Data Segment Register (**DS**) = 6000h; **DL**= 8Bh; **SI** = 0302h

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QUESTION PAPER

Name of the Examination: CAT (FALL 2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Slot: SB2+STB2 **Date of Exam: 01-11-2022**

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Draw and explain the internal hardware architecture of the 8086 microprocessor with a neat diagram. **(10M)**

Q2. Write a program to move the contents of the memory location 0500H to register BX and to CX. Add immediate byte 05H to the data residing in the memory location, whose address is computed using DS=2000H and offset=0600H. Store the result of the addition at 0700H. Assume that the data is located in the segment specified by the data segment register DS which contains 2000H. **(15M)**

Q3. Discuss in detail the architecture of the IAS computer. With a suitable diagram explain how the instructions are executed within this machine. **(10M)**

Q4. Carry out the calculation steps for the 4-bit binary division of positive numbers 1001/0100 (i.e., 9/4) using the non-restoring division algorithm. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1, 2, 3, 5	2	1	10
Q2	3	3	1, 2, 3, 5	2	1	15
Q3	1	1	1, 2, 3	2	1	10
Q4	2	2	1, 2, 3	2	1	15

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QUESTION PAPER

Name of the Examination: CAT (FALL 2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Slot: SB1+STB1 **Date of Exam: 01-11-2022**

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. What are the different buses used in the Microprocessor? Draw the single bus structure. **(10M)**

Q2. Draw the flow chart and demonstrate the division approach using the restoring algorithm to divide 11 by 3. **(15M)**

Q3. How to represent the signed integer numbers? Perform arithmetic operation in binary using sign-magnitude and 2's complement representation.

(i) (+34) + (-15)

(ii) (-34) – (-15) **(10M)**

Q4. What are the different addressing modes used in the 8086 microprocessor? Discuss each with a suitable example. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	2	1	2	2	1	15
Q3	2	2	3	2	3	10
Q4	3	2	4	2	3	15

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QUESTION PAPER

Name of the Examination: CAT (FALL 2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Slot: SC1+STC1 **Date of Exam: 02-11-2022**

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Define Computer architecture and computer organization. Justify whether a common instruction set supports different architecture. **(10M)**

Q2. Demonstrate the division approach using the restoring algorithm to divide 9 by 3. **(10M)**

Q3. What are the functions of the Execution unit and Bus Interface unit? Explain their utility by taking five instructions as an example. **(15M)**

Q4. Write a program for 8086 microprocessor to reverse the order of 10 numbers stored at 5000h using only stack and its related instructions. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1, 2, 3	2	1	10
Q2	2	2	1, 2, 3	2	1	10
Q3	3	3	1, 2, 3, 5	2	1	15
Q4	3	3	1, 2, 3, 5	2	1	15

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QUESTION PAPER

Name of the Examination: CAT – 2 (Winter 2021-2022)

Course Code: ECE2002 **Course Title:** COA

Slot: D1 **Date of Exam:** 21/04/2022

Duration: 90 min **Total Marks:** 50

Class ID: AP2021225000117

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform division of 14/5 and 14/-5 using restoring algorithm. Mention all the steps using proper Table. Also mention the difference between them

(15M)

Q2. Two floating points numbers are in the format $X = X_S \times B^{X_E}$ and $Y = Y_S \times B^{Y_E}$. Where

$X_S = 1111$ and $Y_S = 0110$

$X_E = 1111$ and $Y_E = 1001$

Show the operation $X \div Y$ and compute the result using Unsigned Binary Division Restoring Algorithm.

(10M)

Q3. For the following instructions, explain the computation of the final memory address of a physical memory location of the operands. Also mention the corresponding addressing mode.

The content of different registers and memory locations are as follows:

Code Segment Register (**CS**) = 4000h; **IP** = 0305h; **BX** = 0702h; **DI** = 0202h;

Data Segment Register (**DS**) = 6000h; **DL**= 8Bh; **SI** = 0302h

[**2004h**] = 0Ah; [**2005h**] = 1Ch; [**2006h**] = 20h; [**2006h**] = 2Dh; [**2007**] = 0Ah;

1) AND AL, [SI]
2) XCHG DL, 00A1h[BX][DI],
3) MOV DH, [BX+DI]
4) ADD BX, [2005h]
5) INC [BX][SI]

(10M)

Q4. Find out the content of the relevant registers and memory after the execution of each instruction of the following program in 8086 where memory locations have following contents

[7011h] = 22h; [7012h] = 33h; [7013h] = 44h; [7014h] = BBh;

MOV DX, 5004h

MOV AH, [7012h]

ADD DL, AL

SUB AH, 0Ch

XCHG DL, [7011h]

MOV CL, AL

MOV CH,DH

XOR DH, CL

INC DL

MUL CL

(15M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3	1	1	15
Q2	2	2	1,2,3	1	1	10
Q3	3	3	1,2,3	3	3	10
Q4	3	3	1,2,3	3	3	15

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QUESTION PAPER

Name of the Examination: CAT – 2 (Winter 2021-2022)

Course Code: ECE2002 **Course Title:** COA

Slot: E1+TE1 **Date of Exam:** 22/04/2022

Duration: 90 min **Total Marks:** 50

Class ID: AP2021225000079

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform division of 29/7 using non-restoring algorithm. Mention all the steps using a proper Table. **(15 M)**

Q2. Two floating points numbers are in the format $X = X_S \times B^{X_E}$ and $Y = Y_S \times B^{Y_E}$. Where

$X_S = 1011$ and $Y_S = 0111$

$X_E = 1101$ and $Y_E = 1100$

Show the operation $X \div Y$ and compute the result using Unsigned Binary Division Restoring Algorithm. **(10 M)**

Q3. Write a program using one address instructions, two address instructions and three address instructions for implementing equation $Y = (\frac{C}{D} + B) \times (A - C)$. Assume the necessary temporary registers and mention them too. **(10M)**

Q4. Find out the content of the relevant registers and memory after the execution of each instruction of the following program in 8086 microprocessor. Where memory locations have following contents: **(15M)**

[5001h] = 2Ah; [5002h] = 4Dh; [5003h] = 40h; [5004h] = 4Ch;

MOV BX, 5004h

MOV AX, [5003h]

ADD BH, AL

SUB AH, 0Ch

MOV CL, AL

XCHG CL, [5001h]

MOV DI, CL

XOR [5003], AL

INC BX

MUL CL

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3	1	1	15
Q2	2	2	1,2,3	1	1	10
Q3	3	3	1,2,3	3	3	10
Q4	3	3	1,2,3	3	3	15

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QUESTION PAPER

Name of the Examination: FAT (Winter 2021-2022)

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Slot: D1+TD1 **Date of Exam:** 26/05/2022

Duration: 120 min. **Total Marks:** 60

Instructions:

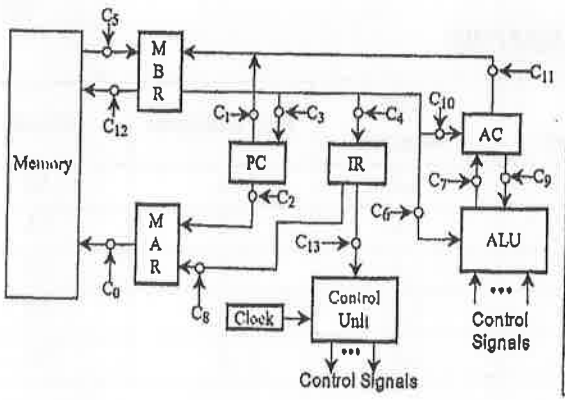
1. **Assume data wherever necessary.**

Q1. A patient's daily temperature is measured by a digital thermometer in a hospital for 14 days. The thermometer readings are stored in the memory starting from 2000H:60D0H of a computer with 8086-microprocessor. After 14 days, if the average temperature exceeds 101F, patient considered to be in serious category otherwise declared normal. Write an assembly language program for finding out if the patient is serious or normal. In case of serious condition, store FF in 2000H:60E0 otherwise store AA in same location.

(10 M)

Q2. In the following diagram and Table different control signals are given with respect to the different microinstructions occurred during different cycles. Find out the equations for the control signals C_2, C_5, C_4, C_8, C_{12}, C_w, and C_R, generated during the execution of different instructions and draw gate level circuits for each equation.

(15 M)



	Microoperations	Active control signals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← PC+1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5, C_R
	t_3: IR(Address) ← MBR(Address)	C_4
Interrupt:	t_1: MAR ← (PC)	C_2
	t_2: MAR ← Save-Address PC ← Routine-Address	C_8
	t_3: Memory ← (MBR)	C_{12}, C_w

Q3. In a digital machine C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11 control signals are needed for execution of a particular instruction. The sequence of signals is as follow:

T cycle	Control signals
T1	C1
T2	C2
T3	C3 if (p=0) or C4 if (p=1), p is an input signal/variable
T4	C5
T5	C6 if (v=0) or C7 if (v=1), v is an input signal/variable

T6	C8
T7	C9 if (v=0) or C10 if (v=1), v is an input signal/variable
T8	C11

Explain the design of the control unit for execution of the instruction using Flow chart/ Delay element method.

(10 M)

Q4. Assume an Intel processor has following memory configuration:

Size of main memory	8 GB
Size of cache memory	64 KB
Size of a cache block	128 Bytes

A cache mapping technique is used which provides exactly 8 searches to find a hit or miss. Explain the mapping technique using diagram. Find out the Tag size, number of searches, number of blocks in a set, number of sets in main memory, memory address structure and method of searching required for the mapping.

(15 M)

Q5. Discuss about 5-stage parallel pipeline architecture and how it provides temporal parallelism. Discuss the data hazard using w.r.t following example and indicate the instructions may cause data hazard in a 3-stages pipeline processor:

```
MOV AH, 20H
INC [60F0H]
JZ Lable1
MOV [60F0H], AH
ADD CL, DH
DEC [60A3H]
SUB DH, [60A3H]
Lable1: XOR AH, DH
MOV[2002H],AH
```

(10 M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1,2,3	1,2	1	10
Q2	4	4	1,2,3	1,2	1	15
Q3	4	4	1,2,3	1,2	1	10
Q4	5	5	1,2,3	1,2	1	15
Q5	6	6	1,2,3	1,2	1	10

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QUESTION PAPER

Name of the Examination: FAT (Winter 2021-2022)

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Slot: E1+TE1 **Date of Exam:** 27/05/2022

Duration: 120 min. **Total Marks:** 60

Instructions:

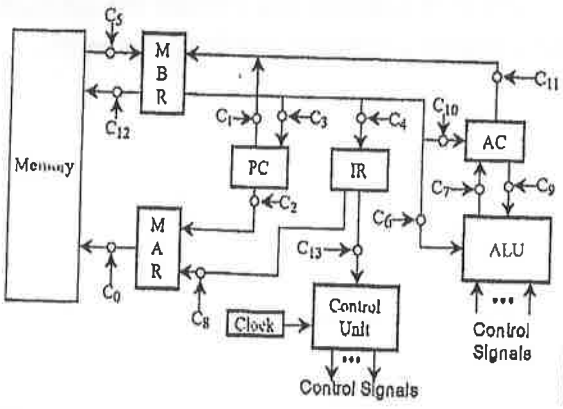
1. **Assume data wherever necessary**

Q1. Write a program to find the average score (runs/over) of a batter for 3 overs. The runs of the batter are stored at the memory locations starting from 2000H. The output score should be stored at the memory location 3000H. Assume suitable data wherever necessary and mention the same.

(10 M)

Q2. In the following diagram and Table different control signals are given with respect to the different microinstructions occurred during different cycles. Find out the equations and gate level circuits for all the control signals generated during fetch and execution of Store 400 instruction. Here, consider 400 as the address of the memory location.

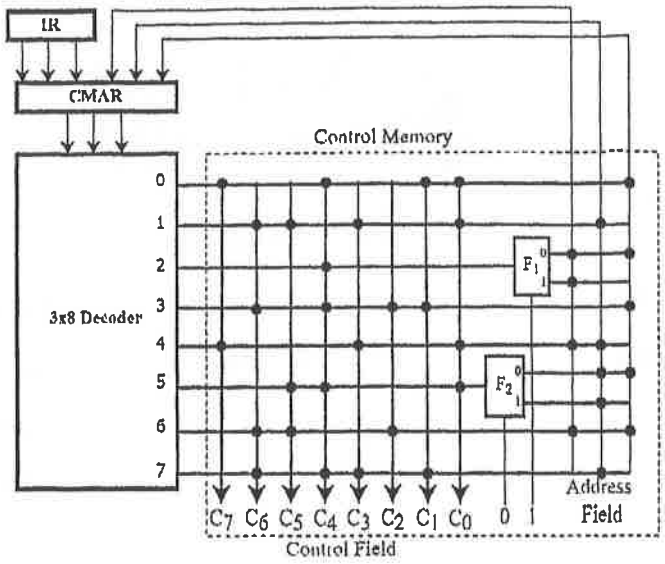
(15 M)



	Microoperations	Active control singals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← PC+1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5 C_R
	t_3: IR(Address) ← MBR(Address)	C_4
Interrupt :	t_1: MAR ← (PC)	C_1
	t_2: MAR ← Save-Address PC ← Routine-Address	
	t_3: Memory ← (MBR)	C_{12}, C_W

Q3. Discuss about control memory? In the following figure of microprogrammed control unit, find out the control signals of the first five micro instructions of an instruction. The first microinstruction address is 110 provided by IR register. The F_1 and F_2 are flag bits.

(10 M)



Q4. Assume an Intel processor has following memory configuration:

Size of main memory	8 GB
Size of cache memory	8 KB
Size of a cache block	64 Bytes

A cache mapping technique is used which provides exactly 4 searches to find a hit or miss. Explain the mapping technique using diagram. Find out the Tag size, number of searches, number of blocks in a set, number of sets in main memory, memory address structure and method of searching required for the mapping.

(15 M)

Q5. Discuss about spatial and temporal parallelism in a super-scalar pipeline architecture. Discuss the control hazard using w.r.t following example and indicate the instructions whose results may need to be flushed out from a 5 stages pipeline processor:

```
MOV AH, 20H
DEC AH
JZ Lable1
MOV DH, AH
ADD CL, DH
INC CL
SUB DL, CL
Lable1: XOR AH, DH
MOV[2002H],AH
```

(10 M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1,2,3	1,2	1	10
Q2	4	4	1,2,3	1,2	1	15
Q3	4	4	1,2,3	1,2	1	10
Q4	5	5	1,2,3	1,2	1	15
Q5	6	6	1,2,3	1,2	1	10

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QUESTION PAPER

Name of the Examination: FAT (FAST Track Fall 2022-2023)

Course Code: ECE2002 **Course Title:** COA

Slot: C+TC+TCC **Date of Exam:** 27-08-2022

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Convert the following 32-bit binary number to its decimal floating-point equivalent:

Sign	Exponent	Mantissa
1	10100010	11010000…..0

(10M)

Q2. Demonstrate the basic organization of a hardwired control unit and the generation of control signals using hardwired control. **(10M)**

Q.3 Clarify the importance of various memory units in a typical computer system. Demonstrate the set associative mapping technique in cache memory. **(10M)**

Q4. Demonstrate the hardware implementation for multiply 53 with -23 Using array multiplication method. **(10M)**

Q5. Demonstrate the I/O interface with block diagram and also show how data transfers can be controlled using handshaking techniques? **(10M)**

Q6. (a) Discuss instruction pipelining and various hazards that occurred during instruction Pipelining. **(7M)**

(b) Differentiate between RISC & CISC based microprocessors. **(3M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	2	10
Q2	2	2	1	2	1	10
Q3	3	3	1	3	1	10
Q4	4	4	2	4	3	10
Q5	5	5	2	3	3	10
Q6	6	5	2	3	2	10

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QUESTION PAPER

Name of the Examination: FAT (FAST TrACK 2021-2022)

Course Code: ECE2002 **Course Title:** COA

Slot: C+TC+TCC **Date of Exam:** 30/07/2022

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Demonstrate the hardware implementation of addition and subtraction of following signed numbers x = 12 and y= 21 and explain its operation. **(10M)**

Q2. Consider x = 1.0001 x 2^6, y = 0.111010 x 2^4. Represent x, y in IEEE 32 bit format. Compute (x + y) and write its equivalent in IEEE format. (10)

Q3. Discuss the flowchart of Booth's Algorithm for multiplication and compute the multiplication of (+15) * (-13) using Booth's Algorithm. **(10M)**

Q4. Demonstrate the division approach using a non-restoring algorithm to divide -17 by 4. **(10M)**

Q5. Write an 8086 program to convert gray numbers into binary. where 8-bit number stored at memory location 3000 and store result into 6000 memory address. **(10M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	1	1	1	1	1	10
Q3	4	2	2	2	2	10
Q4	4	2	2	2	2	10
Q5	5	3	2	2	2	10

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QUESTION PAPER

Name of the Examination: FAT (Long Summer 2021-2022)

Course Code: ECE2002 **Course Title:** COA

Slot: B+TB+TBB **Date of Exam:** 29/07/2022

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. How to represent the signed integer numbers? Perform arithmetic operation in binary using 1's and 2's complement representation

(i). (+42) + (-13)

(ii) (-42) – (-13) **(10M)**

Q2. Demonstrate and explain how control signals are generated using hardwired control. **(10M)**

Q.3 Explain a function of the memory management unit in a typical computer. Demonstrate Direct and Set associative map technique in cache memory. **(10M)**

Q4. Multiplicand B=10111, Multiplier A= 10011. Demonstrate the hardware implementation and algorithm for multiply operation **(10M)**

Q5. (a) What is the I/O interface? show how I/O devices can be interfaced with a block diagram

(b) How data transfers can be controlled using handshaking techniques? **(10M)**

Q6. What is instruction pipelining? Discuss the conflicts that occurred during instruction Pipelining? **(10M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	2	10
Q2	2	2	1	2	1	10
Q3	3	2	1	3	1	10
Q4	4	1	2	4	3	10
Q5	5	3	2	3	3	10
Q6	6	3	2	3	2	10