

# ECE-2002 Computer Organization and Architecture

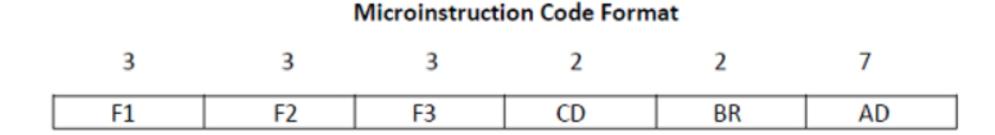
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## **Micro Program**

- >A program is a set of instructions. An instruction requires a set of micro-operations.
- ➤ Micro-operations are performed using control signals.
- ➤ Instead of generating the control signals by hardware, here, these control signals are generated using micro-instructions.
- > This means every instruction requires a set of micro-instructions
- > A set of micro-instructions are called micro-program.
- ➤ Microprograms for all instructions are stored in a small memory called control memory.
- > The control memory is present inside the processor.

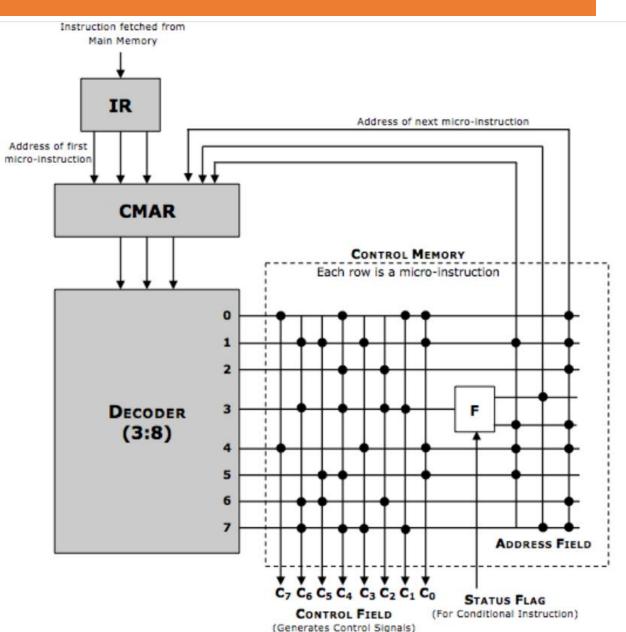
#### **Micro-Instructions**

> A microinstruction format includes 20 bits in total.

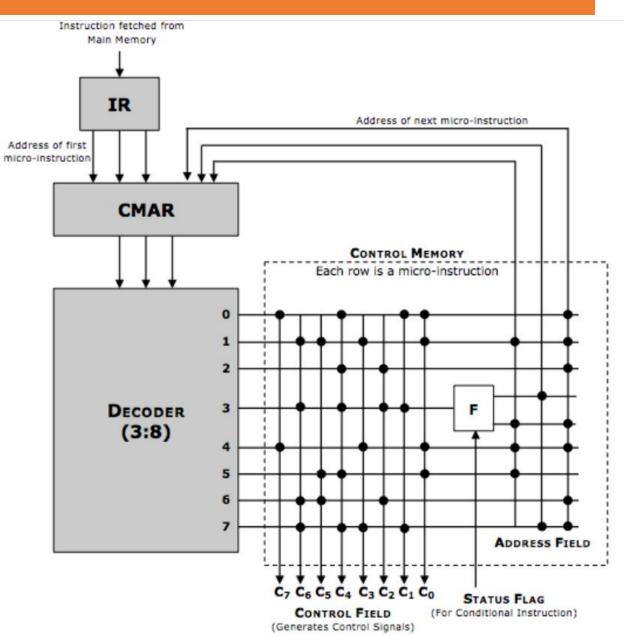


- ➤ F1, F2, F3 are the micro-operation fields. They determine micro-operations for the computer.
- >CD is the condition for branching. They choose the status bit conditions.
- >BR is the branch field. It determines the type of branch.
- > AD is the address field. It includes the address field whose length is 7 bits.
- \*Each microinstruction can have only three micro-operations, one from each field.

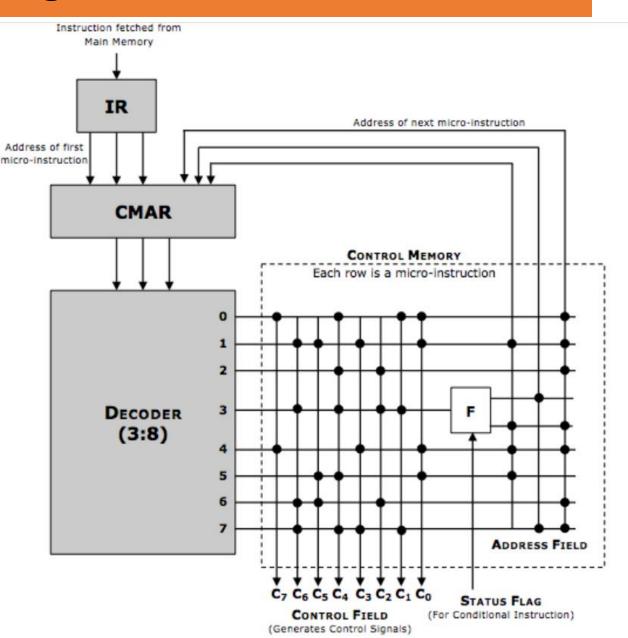
- Consider an instruction fetched from the main memory into the Instruction Register (IR).
- The processor uses opcode to identify the address of the first micro-instruction.
- That address is loaded into CMAR (Control Memory Address Register).
- CMAR passes the address to decoder.



- The decoder identifies the corresponding microinstruction from the control memory.
- ➤ A microinstruction has two fields: Control field and Address field.
- ➤ Control field: indicates the control signal to be generated.
- Address field: indicates the address of the next microinstruction
- ➤ This address is further loaded into CMAR to fetch the next instruction.

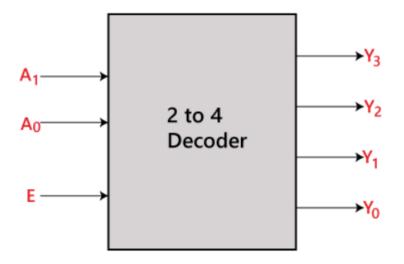


For a conditional microinstruction, there are two address fields, as the address of the next microinstruction depends on the condition (true or false).



#### Decoder

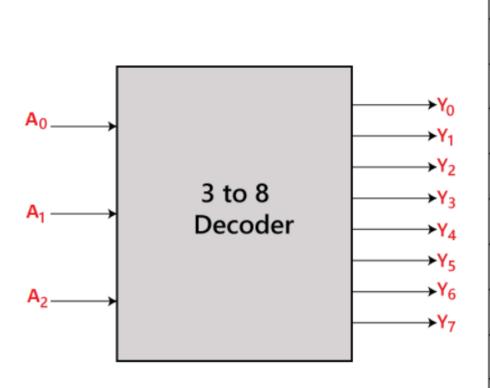
- Decoder: n binary inputs and 2<sup>n</sup> binary outputs
- In the 2 to 4 line decoder, there is a total of three inputs, i.e.,  $A_0$ , and  $A_1$  and E and four outputs, i.e.,  $Y_0$ ,  $Y_1$ ,  $Y_2$ , and  $Y_3$ . For each combination of inputs, when the enable 'E' is set to 1, one of these four outputs will be 1.



Enable	INP	UTS	OUTPUTS						
E	A <sub>1</sub>	A <sub>0</sub>	<b>Y</b> <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>			
0	Х	Х	0	0	0	0			
1	0	0	0	0	0	1			
1	0	1	0	0	1	0			
1	1	0	0	1	0	0			
1	1	1	1	0	0	0			

#### Decoder

• In a 3 to 8 line decoder, there is a total of eight outputs, i.e., Y0, Y1, Y2, Y3, Y4, Y5, Y6, and Y7 and three inputs, i.e., A0, A1, and A2.

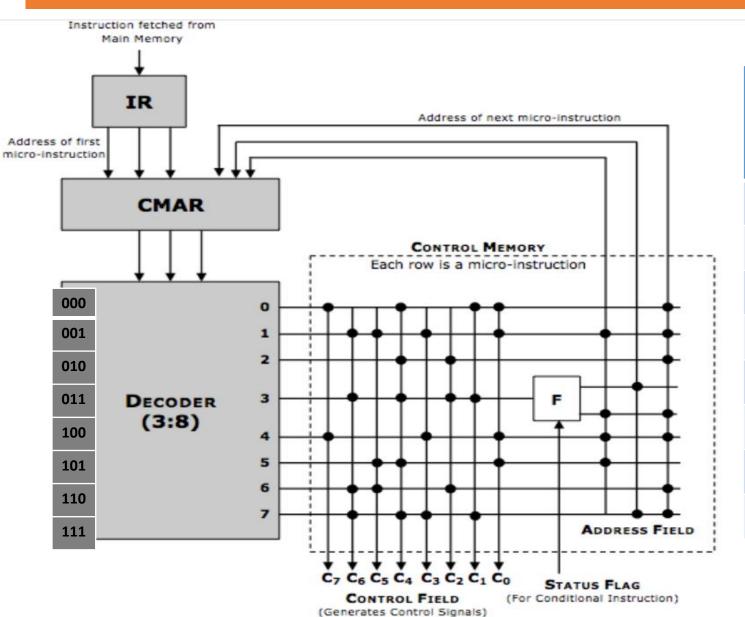


Enable	INPUTS				Outputs							
E	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	<b>Y</b> <sub>7</sub>	<b>Y</b> <sub>6</sub>	<b>Y</b> <sub>5</sub>	Y <sub>4</sub>	<b>Y</b> <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>	
0	х	х	х	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	1	
1	0	0	1	0	0	0	0	0	0	1	0	
1	0	1	0	0	0	0	0	0	1	0	0	
1	0	1	1	0	0	0	0	1	0	0	0	
1	1	0	0	0	0	0	1	0	0	0	0	
1	1	0	1	0	0	1	0	0	0	0	0	
1	1	1	0	0	1	0	0	0	0	0	0	
1	1	1	1	1	0	0	0	0	0	0	0	

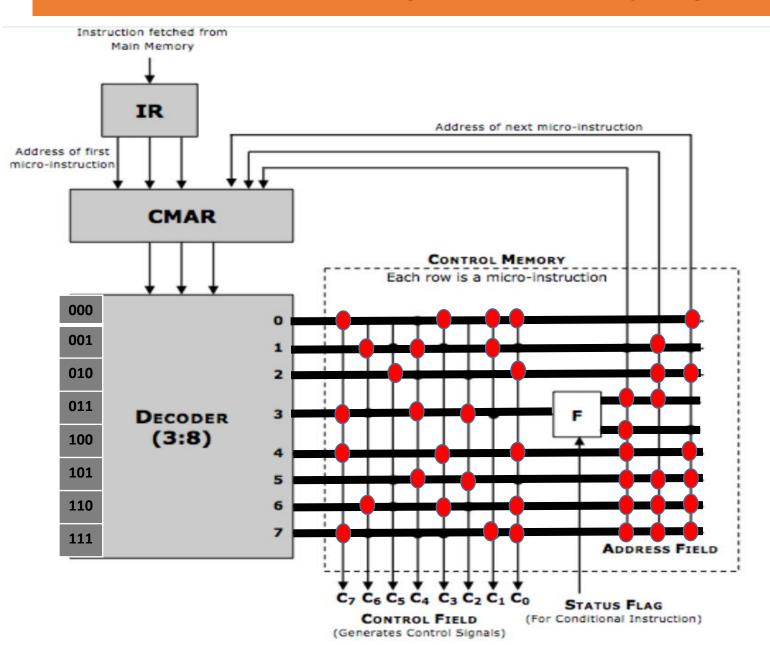
### Decoder

In the 4 to 16 line decoder, there is a total of 16 outputs, i.e., Y<sub>0</sub>, Y<sub>1</sub>, Y<sub>2</sub>,...., Y<sub>16</sub> and four inputs, i.e., A<sub>0</sub>, A1, A<sub>2</sub>, and A<sub>3</sub>.

	INPUTS									ου	TPU	TS							
<b>A</b> <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	Ao	Y <sub>15</sub>	Y <sub>14</sub>	Y <sub>13</sub>	Y <sub>12</sub>	Y <sub>11</sub>	Y <sub>10</sub>	<b>Y</b> 9	Y <sub>8</sub>	<b>Y</b> <sub>7</sub>	Y <sub>6</sub>	<b>Y</b> <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Yo
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



Address of current instruction	Control signal	Address of next instruction
000	C0, C1, C4, C7	001
001	C0, C3, C5, C6	101
010	C2, C4	001
011	C1, C2, C4, C6	010/101
100	C0, C3, C7	101
101	C0, C4, C5	100
110	C2, C5, C6	001
111	C1, C3, C4, C6	011



Address of current instruction	Control signal	Address of next instruction
000		
001		
010		
011		
100		
101		
110		
111		