VIT-AP UNIVERSITY

MODULE-VI

Pipeline Problems

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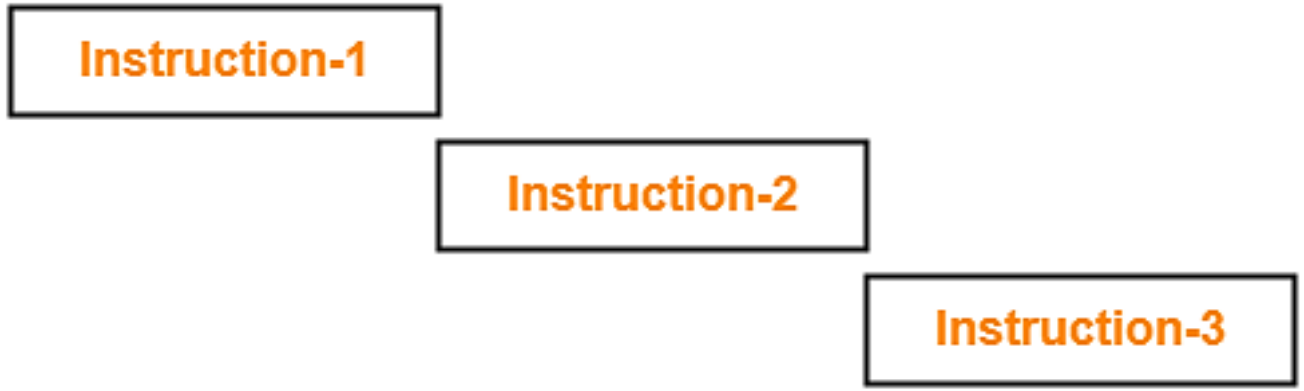
CONTENT

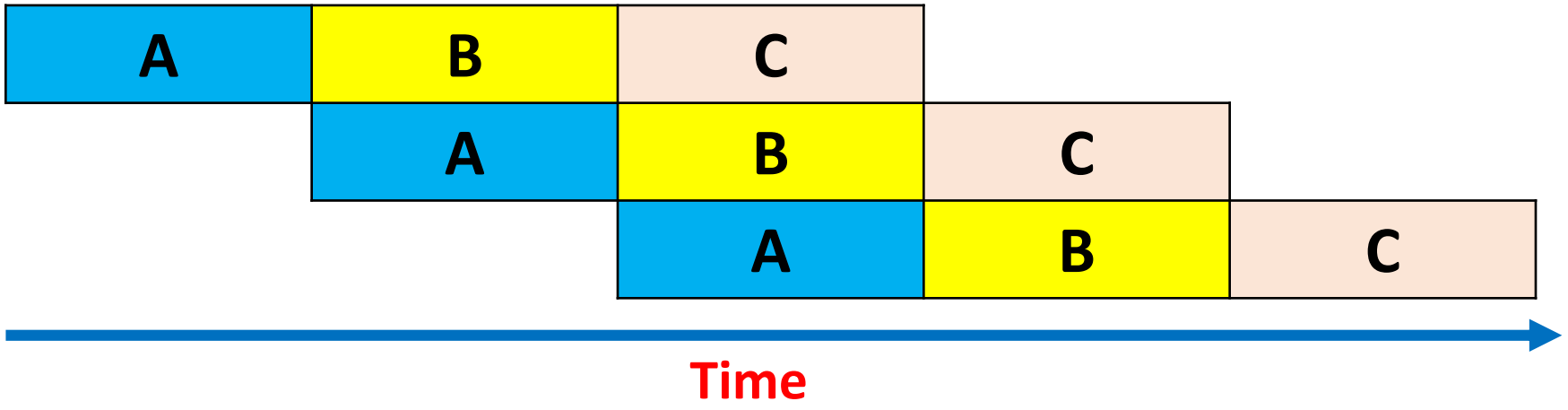
- ✓ **Problems on Pipeline**

PIPELINE

Non-pipeline



Pipeline



MODEL-1 : PIPELINE PROBLEM-1

Problem 1: Find the **number of clock cycles** required to execute 10 instructions with pipeline method and without pipeline method for the following instruction structure ?

I	F (2)	D (1)	E (1)

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

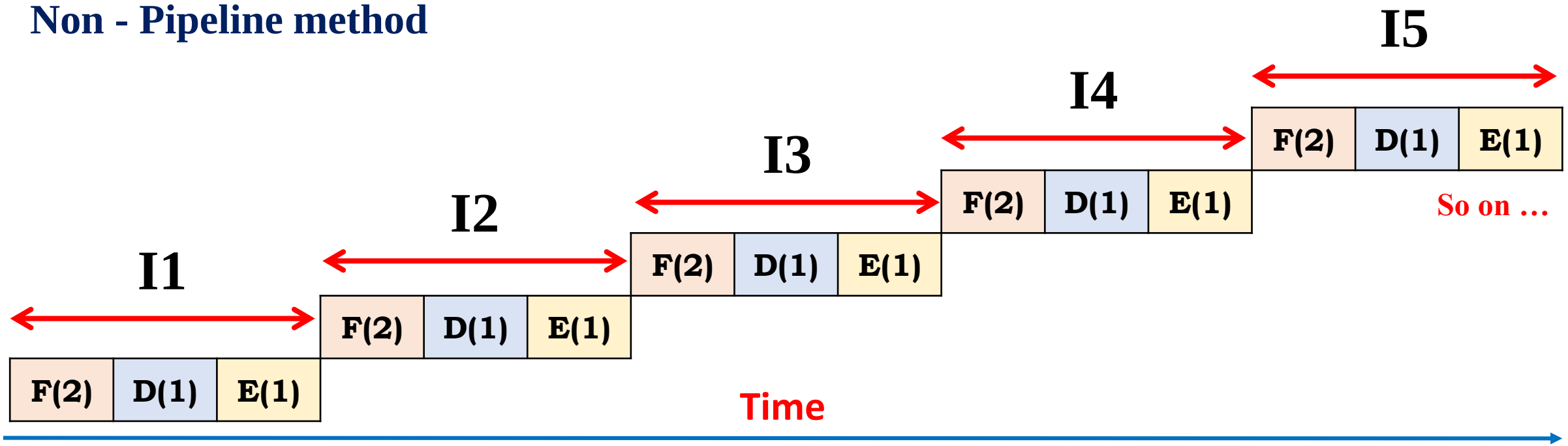
Fetch - 2 Clock cycle

Decoding - 1 Clock cycle

Execution - 1 Clock cycle

MODEL-1 : PIPELINE PROBLEM-1

Non - Pipeline method



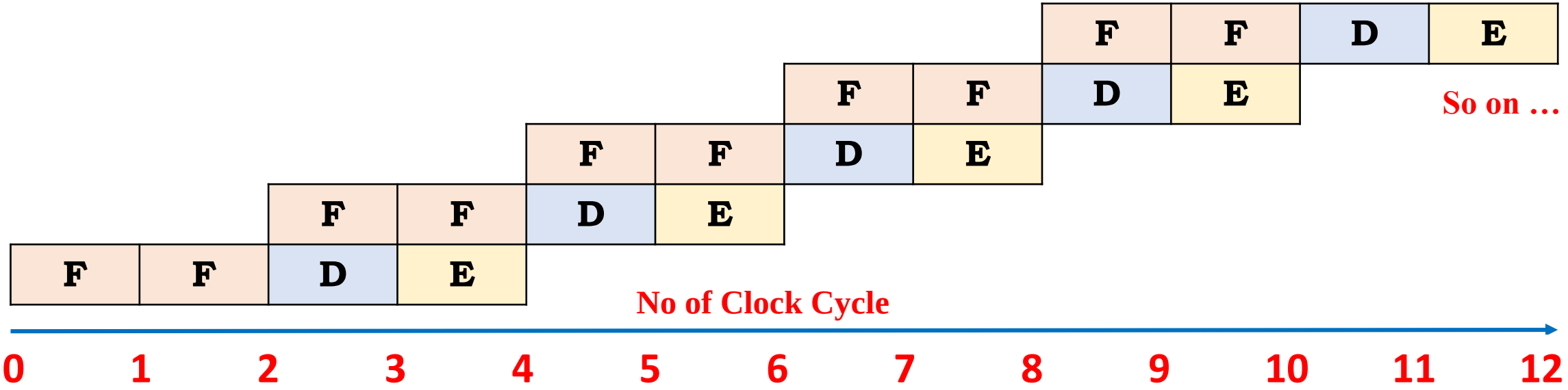
No of Clock Cycle required to execute 10 instructions is

= (No of instructions) x (Total no of required for single instruction)

= 10 x 4 = **40 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-1

Pipeline method



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 4 + ((10-1) x 2) = 4 + (9 x 2) = 4 + 18 = **22 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-2

Problem 2: Find the **number of clock cycles** required to execute 100 instructions with pipeline method and without pipeline method for the following instruction structure ?

I	F (2)	D (1)	E (3)

Fetch - 2 Clock cycle

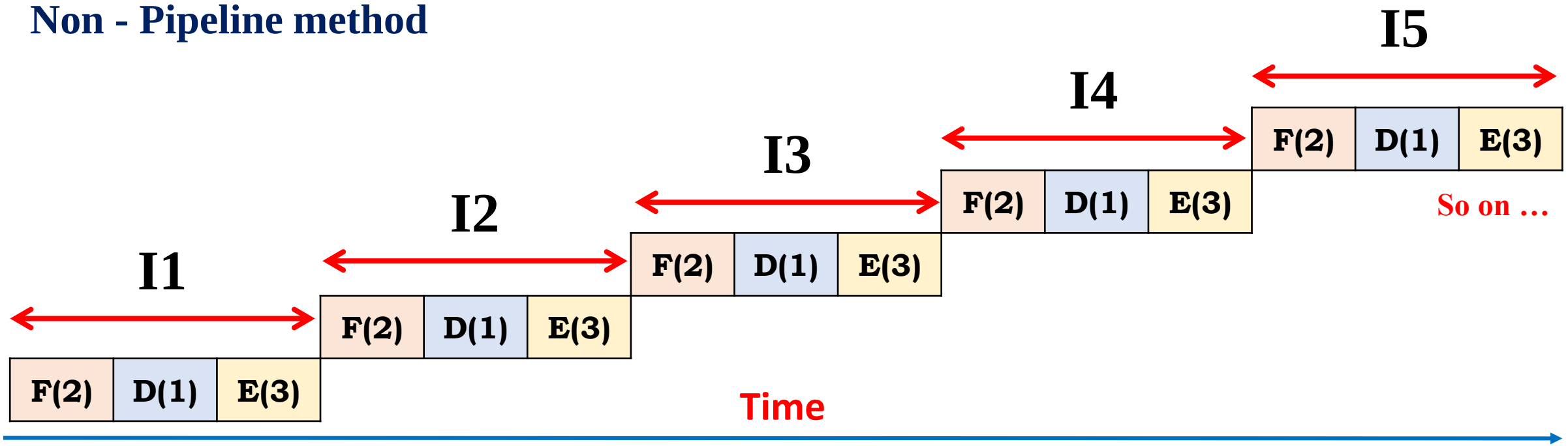
Decoding - 1 Clock cycle

Execution - 3 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM-2

Non - Pipeline method



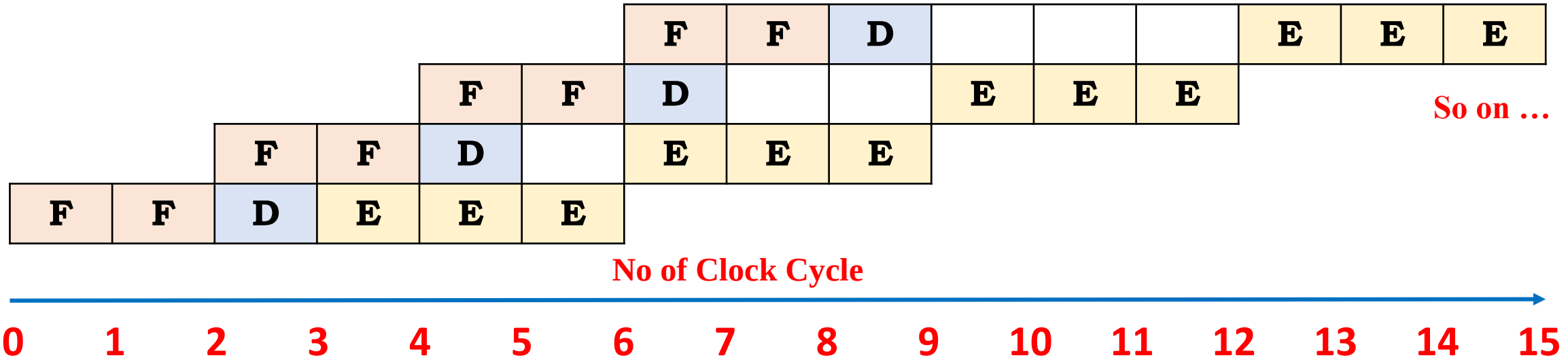
No of Clock Cycle required to execute 100 instructions is

= (No of instructions) x (Total no of cycles required for single instruction)

= 100 x 6 = **600 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-2

Pipeline method



No of Clock Cycle required to execute 100 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((100-1) x 3) = 6 + (99 x 3) = 6 + 297 = **303 Clock cycles**

MODEL-1 : PIPELINE PROBLEM ASSIGNMENT-1

Assignment - 1: Find the **number of clock cycles** required to execute 1000 instructions with pipeline method and without pipeline method for the following instruction structure ?

I	F (1)	D (2)	E (3)

Fetch - 1 Clock cycle

Decoding - 2 Clock cycle

Execution - 3 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM ASSIGNMENT-1

Assignment - 1: Find the **number of clock cycles** required to execute 1000 instructions with pipeline method and without pipeline method for the following instruction structure ?

I	F (1)	D (2)	E (3)

Fetch - 1 Clock cycle

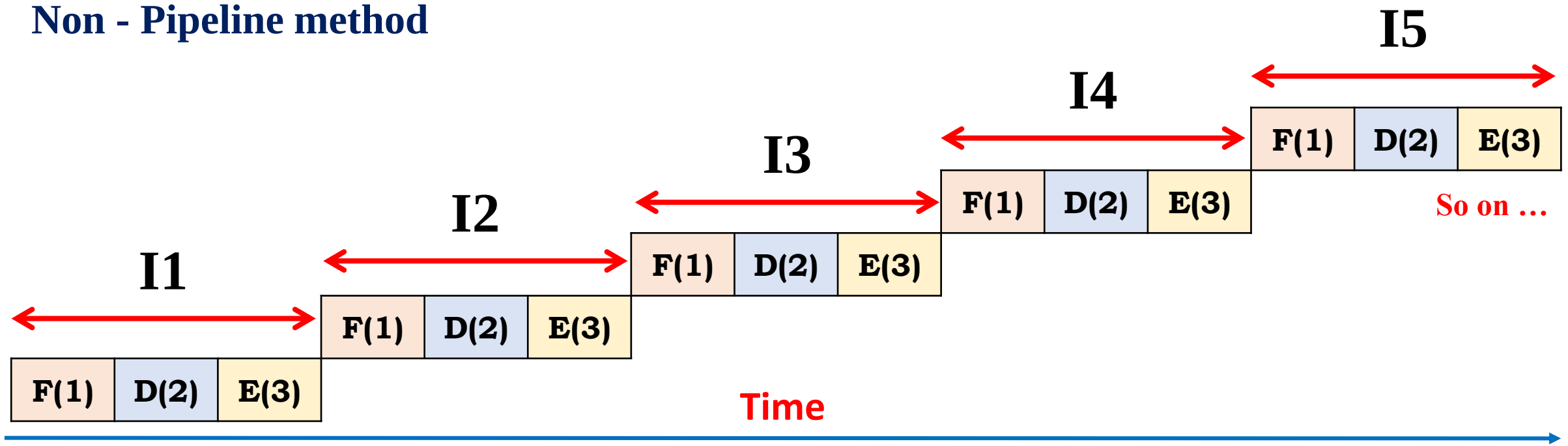
Decoding - 2 Clock cycle

Execution - 3 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM ASSIGNMENT-1

Non - Pipeline method



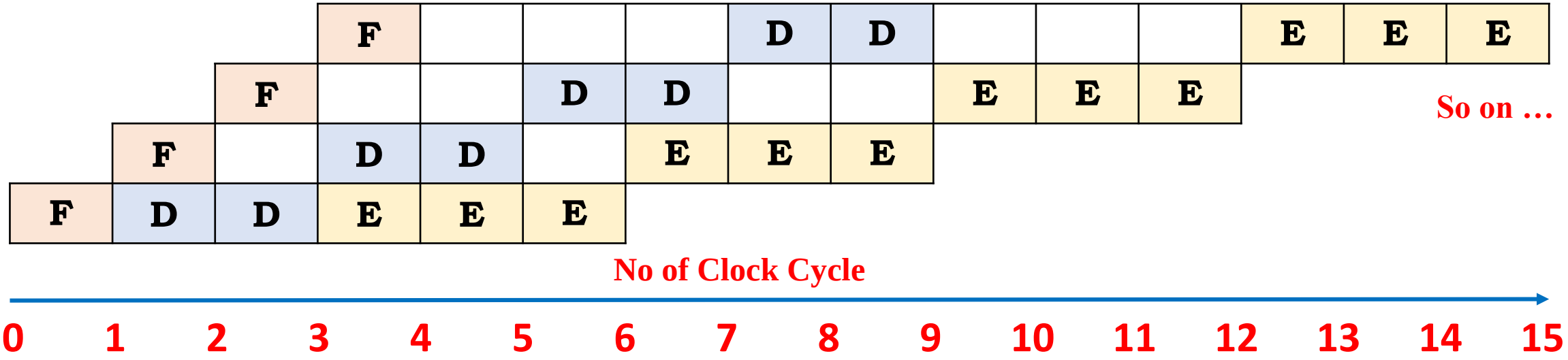
No of Clock Cycle required to execute 1000 instructions is

= (No of instructions) x (Total no of required for single instruction)

= 1000 x 6 = **6000 Clock cycles**

MODEL-1 : PIPELINE PROBLEM ASSIGNMENT-1

Pipeline method



No of Clock Cycle required to execute 100 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((1000-1) x 3) = 6 + (999 x 3) = 6 + 2997 = **3003 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-3

Problem 1: Find the **number of clock cycles** required to execute 1000 instructions with pipeline method and without pipeline method for the following instruction structure? **If microcontroller frequency is 1GHz then also find the max operating frequency**?

I	F (1)	D (1)	E (4)

Fetch - 1 Clock cycle

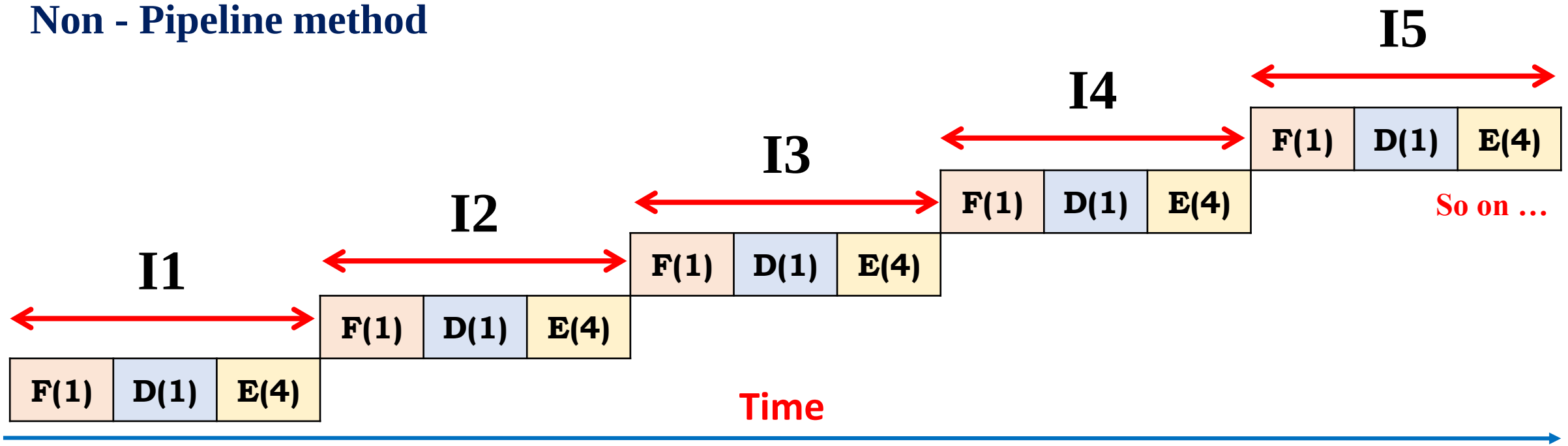
Decoding - 1 Clock cycle

Execution - 4 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM-3

Non - Pipeline method



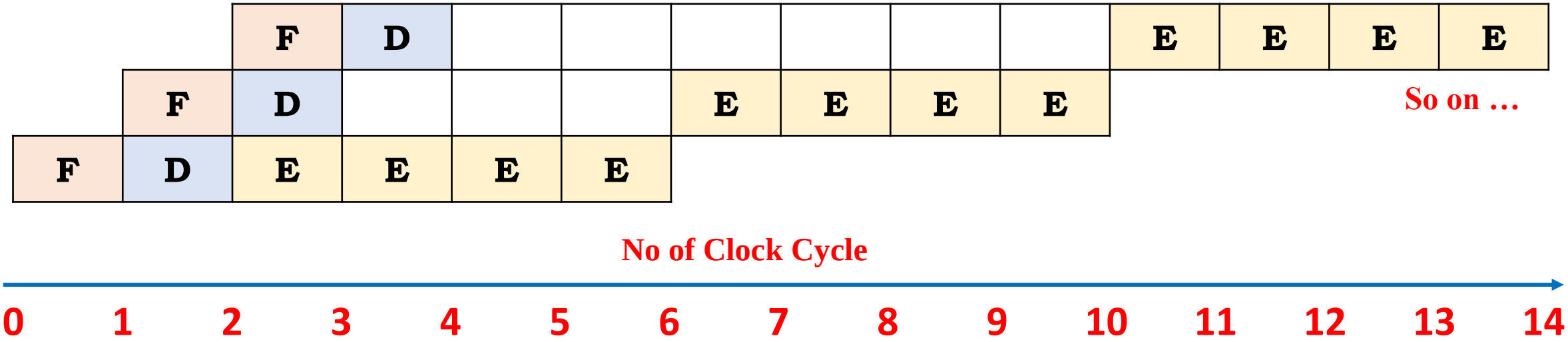
No of Clock Cycle required to execute 1000 instructions is

= (No of instructions) x (Total no of required for single instruction)

= 1000 x 6 = **6000 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-3

Pipeline method



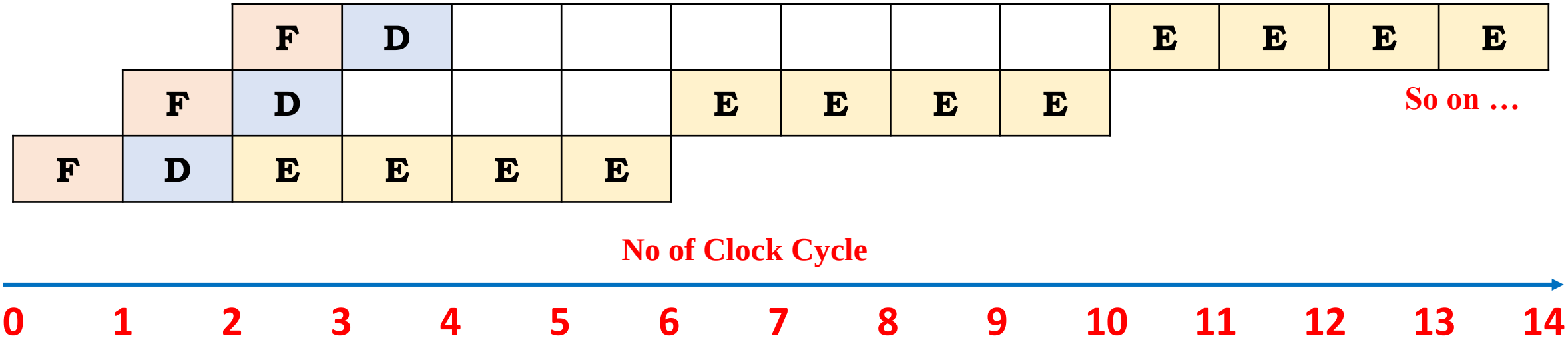
No of Clock Cycle required to execute 1000 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((1000-1) x 4) = 6 + (999 x 4) = 6 + 3996 = **4002 Clock cycles**

MODEL-1 : PIPELINE PROBLEM-3

Pipeline method



Maximum operating frequency is given by

$$f_{max.\ op} = \frac{f_{mc}}{\text{max. difference between two instructions}} = \frac{1\text{GHz}}{4} = 0.25\ \text{GHz}$$

MODEL-1 : PIPELINE PROBLEM-4

Problem 4: If microcontroller frequency is 1GHz then also find the max operating frequency?

I	F (2)	D (1)	E (1)

Fetch - 2 Clock cycle

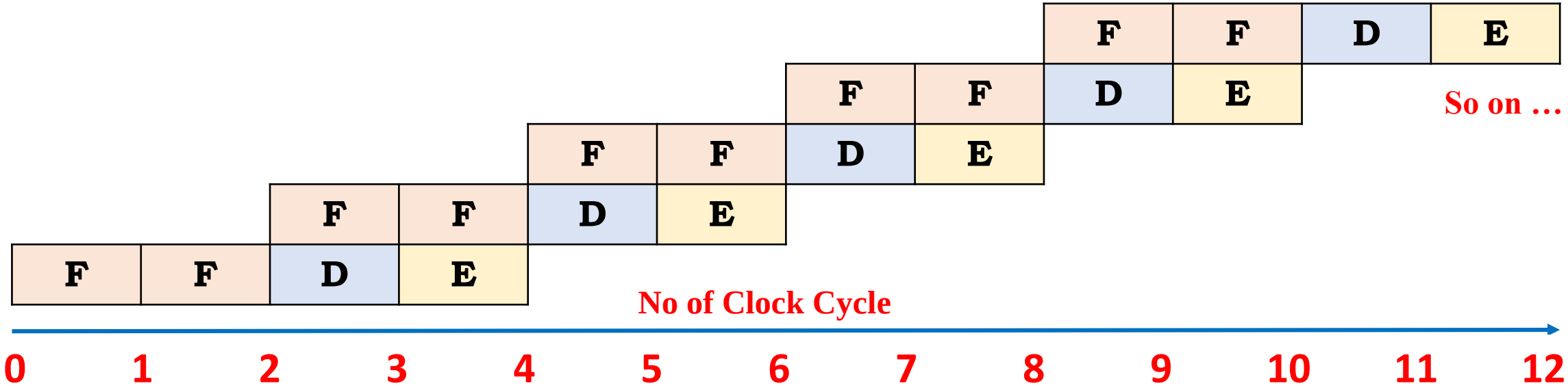
Decoding - 1 Clock cycle

Execution - 1 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM-4

Pipeline method



Maximum operating frequency is given by

$$f_{max.\ op} = \frac{f_{mc}}{\text{max. difference between two instructions}} = \frac{1\text{GHz}}{2} = 0.5\ \text{GHz}$$

MODEL-1 : PIPELINE PROBLEM-5

Problem 5: If microcontroller frequency is 1GHz then also find the max operating frequency ?

I	F (2)	D (1)	E (3)

Fetch - 2 Clock cycle

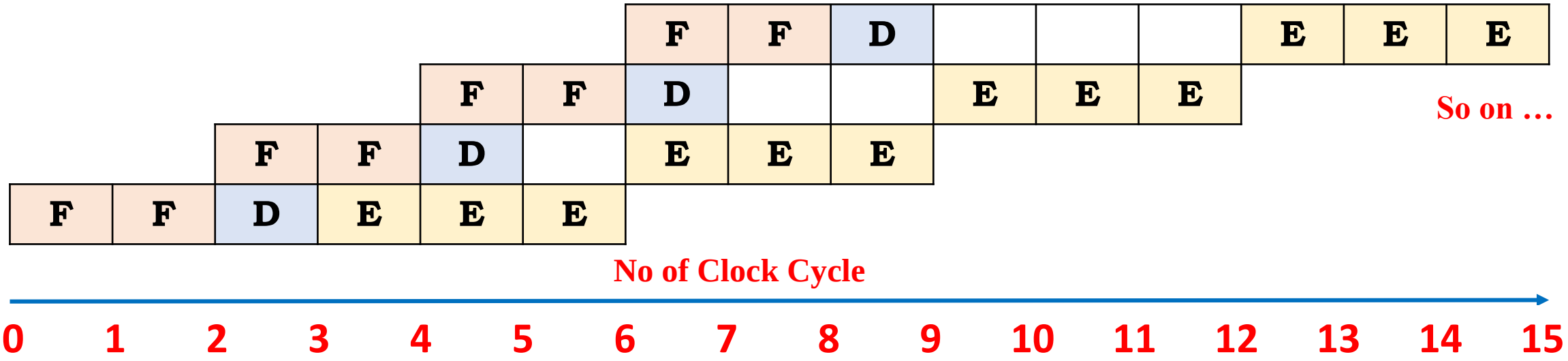
Decoding - 1 Clock cycle

Execution - 3 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-1 : PIPELINE PROBLEM-5

Pipeline method



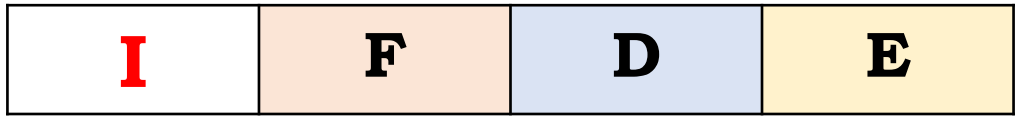
Maximum operating frequency is given by

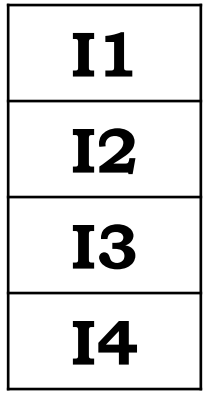
$$f_{max.\ op} = \frac{f_{mc}}{\text{max. difference between two instructions}} = \frac{1\text{GHz}}{3} = 0.33\ \text{GHz}$$

MODEL-2 PROBLEMS

MODEL-2 : PIPELINE PROBLEM-1

Problem 1: Find the **number of clock cycles** required to execute 4 instructions with pipeline method and without pipeline method for the following instruction structure? If microcontroller frequency is 1GHz then also find the max operating frequency?





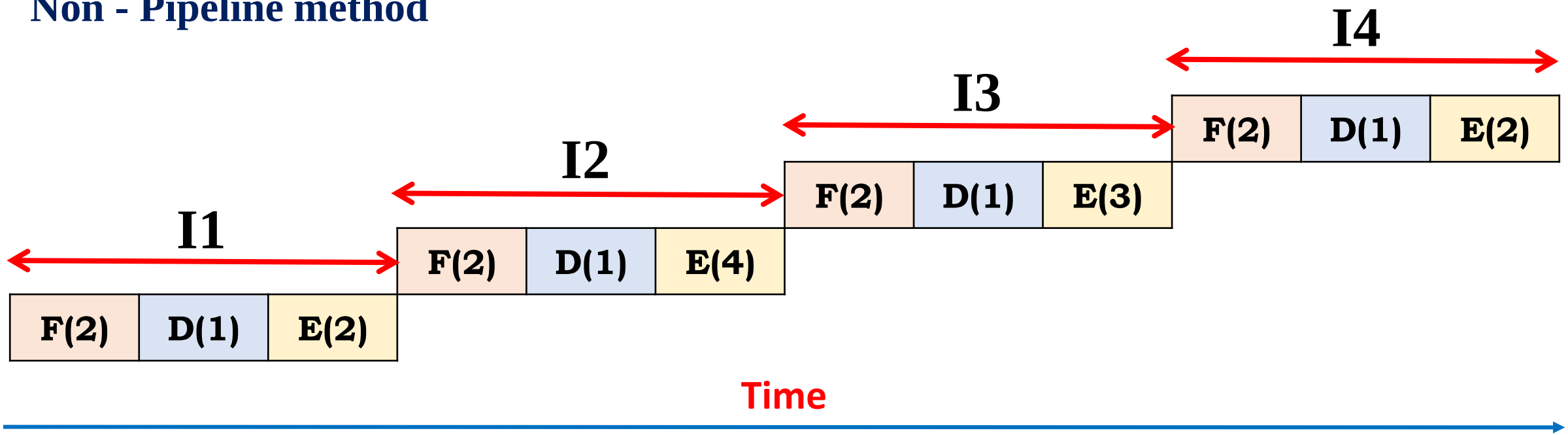
Fetch – 2 Clock cycle

Decoding – 1 Clock cycle

Execution – 2 (I1), 4 (I2), 3 (I3) and 2 (I4) Clock cycles

MODEL-2 : PIPELINE PROBLEM-1

Non - Pipeline method

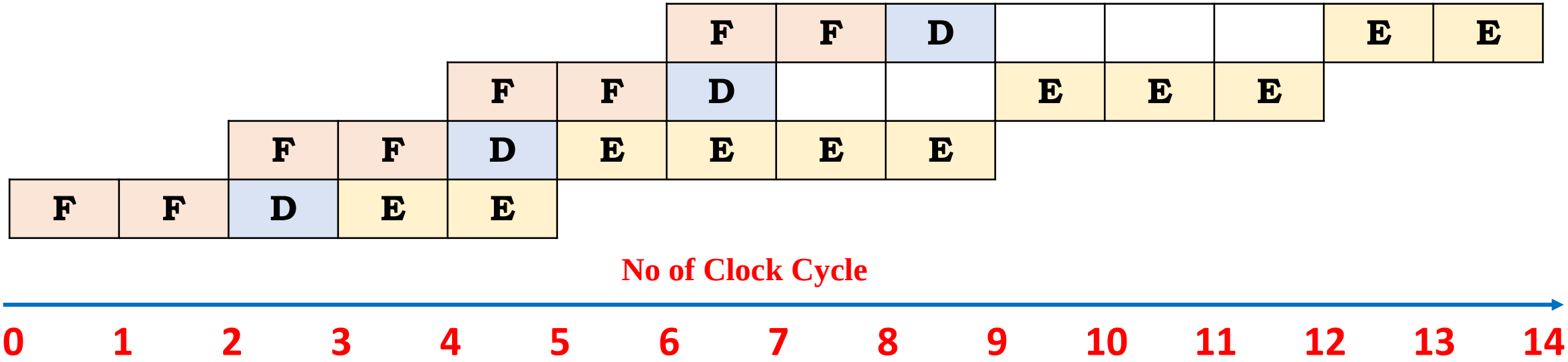


No of Clock Cycle required to execute 4 instructions is

= 5 + 7 + 6 + 5 = **23 Clock cycles**

MODEL-2 : PIPELINE PROBLEM-1

Pipeline method

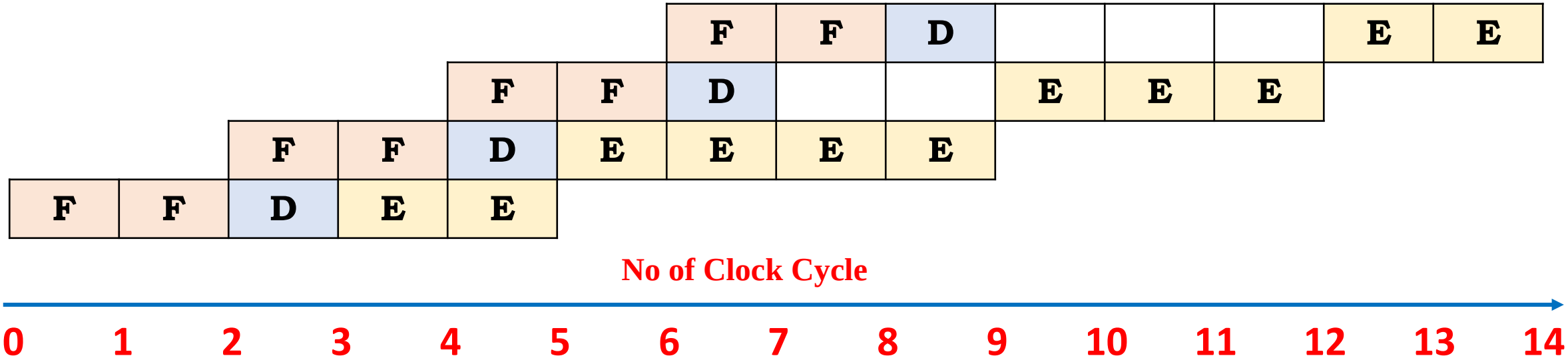


No of Clock Cycle required to execute 4 instructions is

= **14 Clock Cycles** (From diagram)

MODEL-2 : PIPELINE PROBLEM-1

Pipeline method

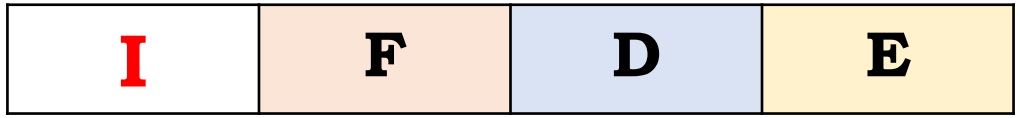


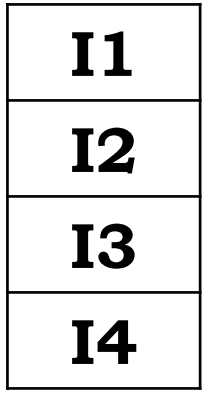
Maximum operating frequency is given by

$$f_{max.\ op} = \frac{f_{mc}}{\text{max. difference between two instructions}} = \frac{1\text{GHz}}{4} = 0.25\ \text{GHz}$$

MODEL-2 : PIPELINE PROBLEM-2

Problem 2: Find the **number of clock cycles** required to execute 4 instructions with pipeline method and without pipeline method for the following instruction structure? If microcontroller frequency is 1GHz then also find the max operating frequency?





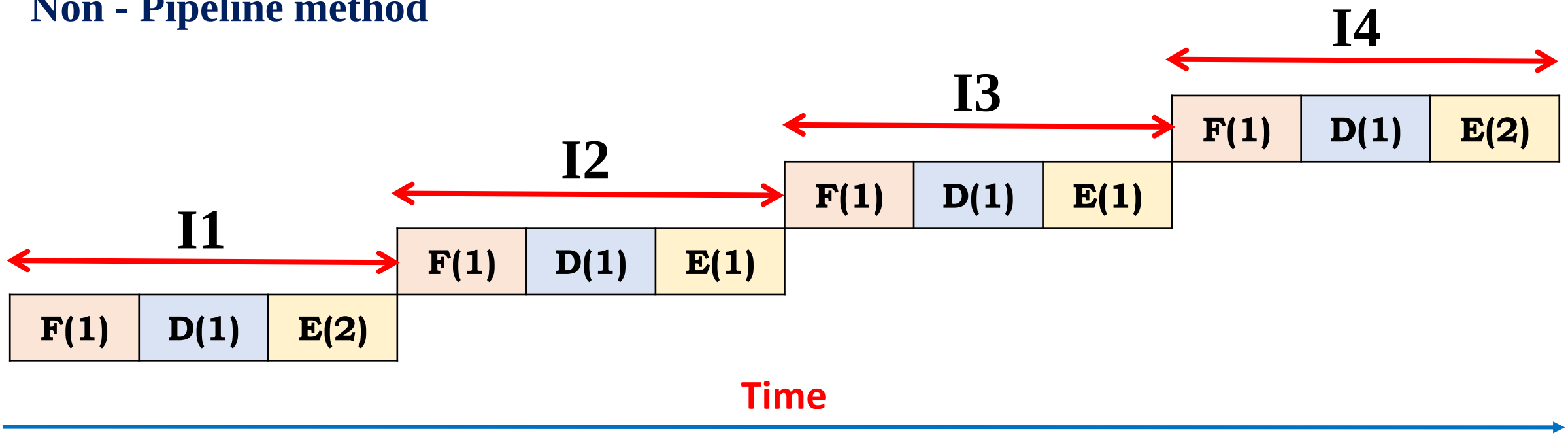
Fetch – 1 Clock cycle

Decoding – 1 Clock cycle

Execution – 2 (I1), 1 (I2), 1 (I3) and 2 (I4) Clock cycles

MODEL-2 : PIPELINE PROBLEM-2

Non - Pipeline method

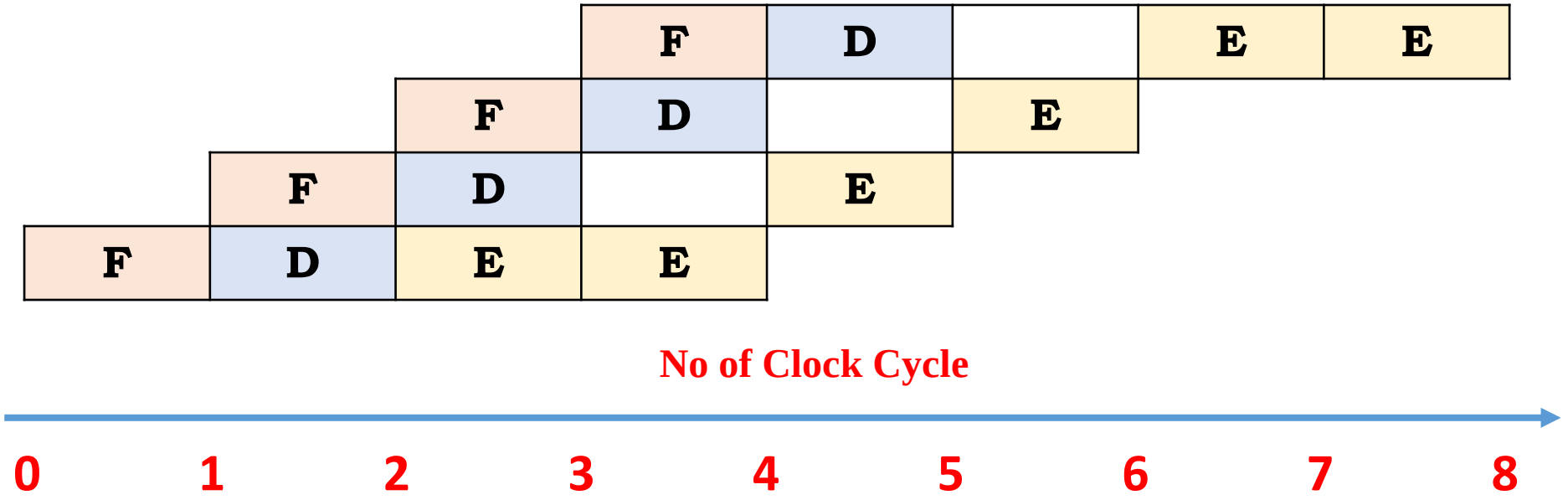


No of Clock Cycle required to execute 4 instructions is

= 4 + 3 + 3 + 4 = **14 Clock cycles**

MODEL-2 : PIPELINE PROBLEM-2

Pipeline method

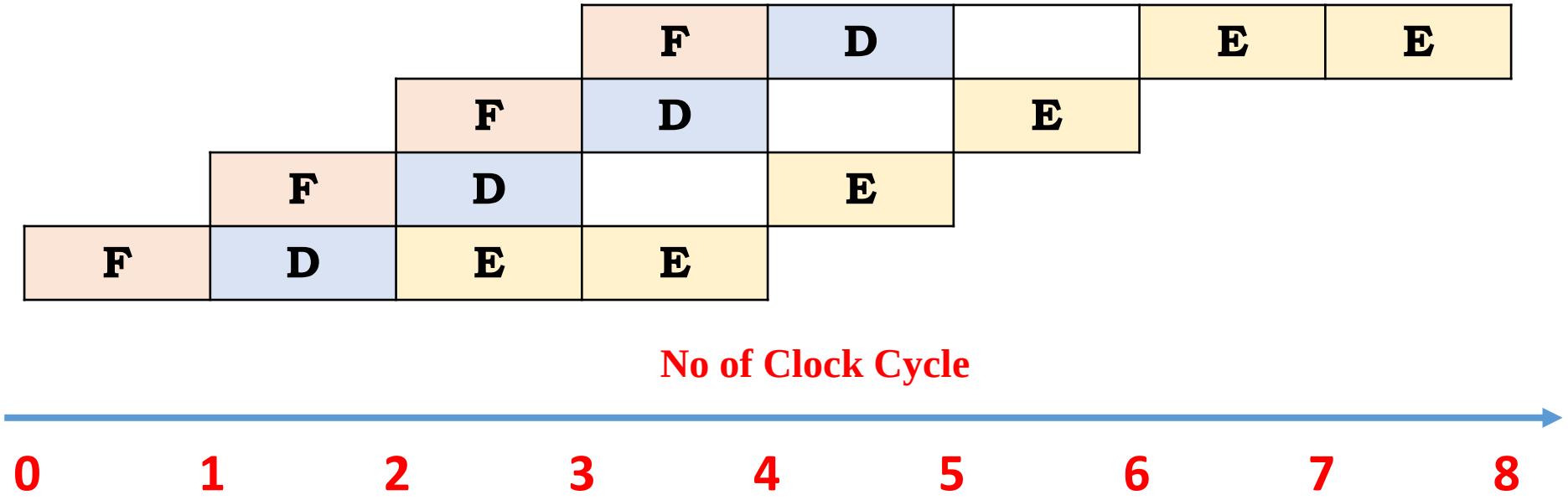


No of Clock Cycle required to execute 4 instructions is

= **8 Clock Cycles** (From diagram)

MODEL-2 : PIPELINE PROBLEM-2

Pipeline method

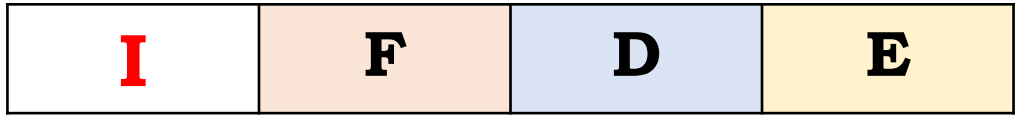


Maximum operating frequency is given by

$$f_{max.\ op} = \frac{f_{mc}}{\text{max. difference between two instructions}} = \frac{1\text{GHz}}{2} = 0.5\ \text{GHz}$$

MODEL-2 : PIPELINE PROBLEM ASSIGNMENT-1

Assignment - 1: Find the **number of clock cycles** required to execute 5 instructions with pipeline method and without pipeline method for the following instruction structure? If microcontroller frequency is 2 GHz then also find the max operating frequency?



I1
I2
I3
I4
I5

Fetch – 1 Clock cycle

Decoding – 1 Clock cycle

Execution – 3 (I1), 4 (I2), 2 (I3), 1 (I4) and 2 (I5) Clock cycles

MODEL-3 PROBLEMS

MODEL-3 : PIPELINE PROBLEM-1

Problem - 1: If the pipeline is flushed for every 3 instructions then find the number of clock cycles required to execute 9 instructions with pipeline method?

I	F (1)	D (1)	E (4)

Fetch - 1 Clock cycle

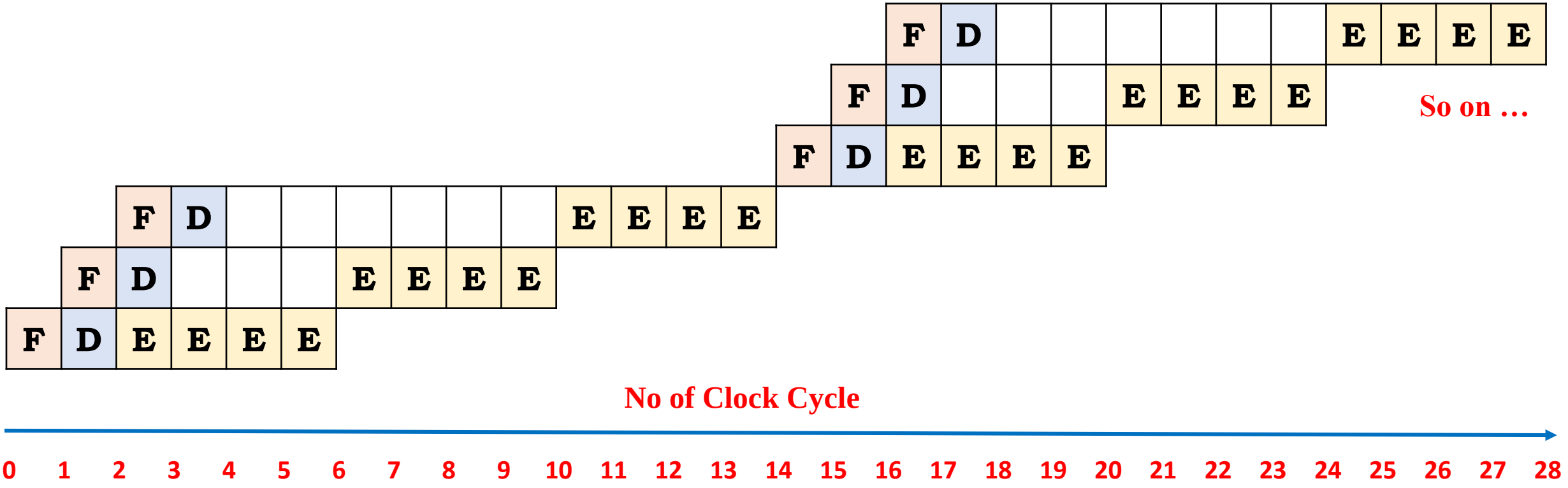
Decoding - 1 Clock cycle

Execution - 4 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9

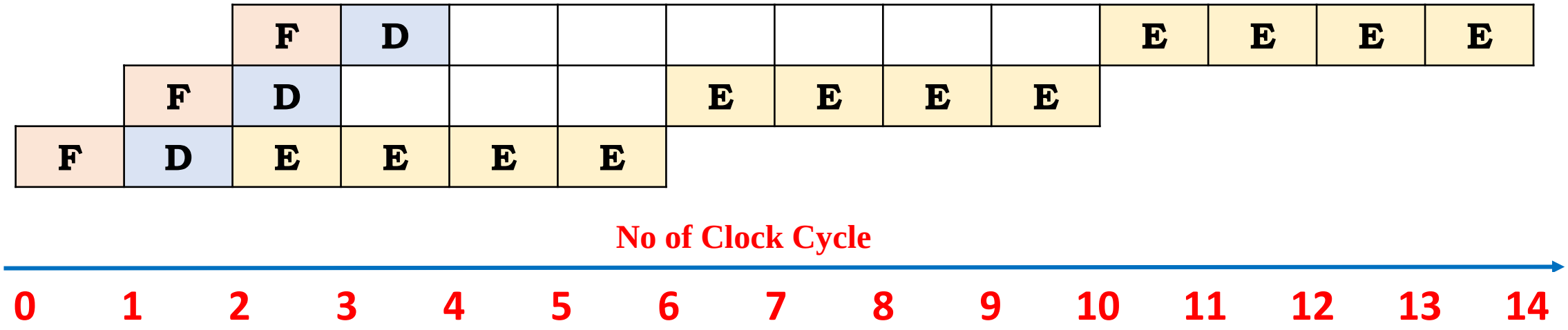
MODEL-3 : PIPELINE PROBLEM-1

Pipeline method



MODEL-3 : PIPELINE PROBLEM-1

Pipeline method



No of Clock Cycle required to execute 3 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((3-1) x 4) = 6 + (2 x 4) = 6 + 8 = **14 Clock cycles**

Total = 14 + 14 + 14 = 42 Clock cycles

MODEL-3 : PIPELINE PROBLEM-2

Problem - 2: If the pipeline is flushed for every 10 instructions then find the number of clock cycles required to execute 40 instructions with pipeline method?

I	F (1)	D (1)	E (4)

Fetch - 1 Clock cycle

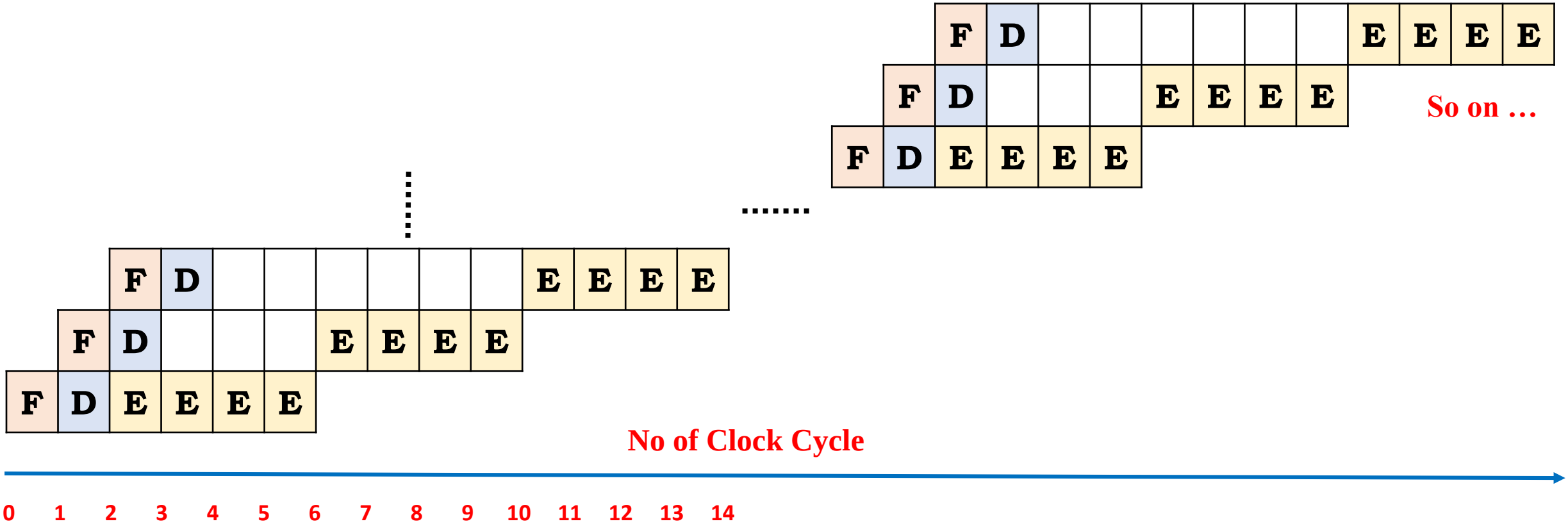
Decoding - 1 Clock cycle

Execution - 4 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

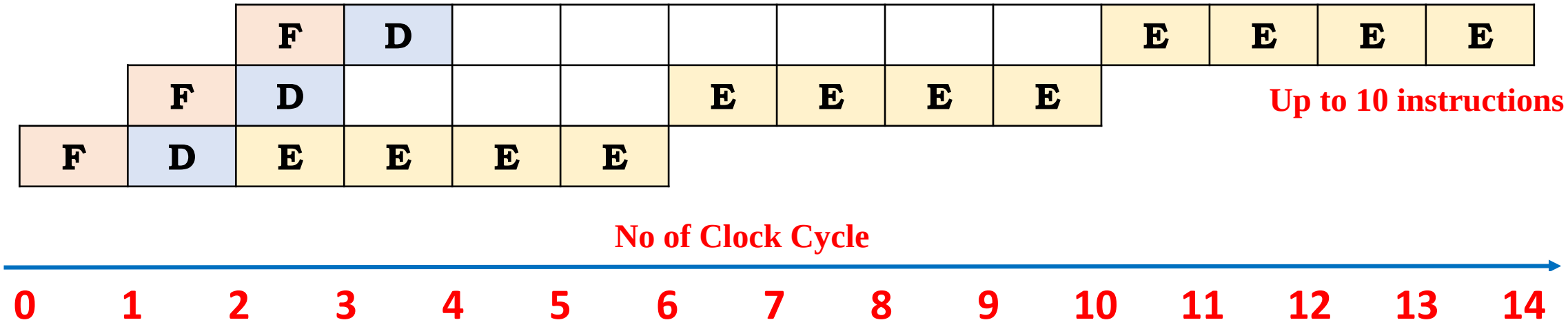
MODEL-3 : PIPELINE PROBLEM-2

Pipeline method



MODEL-3 : PIPELINE PROBLEM-2

Pipeline method



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((10-1) x 4) = 6 + (9 x 4) = 6 + 36 = **42 Clock cycles**

Total = 42 + 42 + 42 + 42 = 168 Clock cycles

MODEL-3 : PIPELINE PROBLEM-3

Problem - 3: If the pipeline is flushed for every 10 instructions then find the number of clock cycles required to execute 41 instructions with pipeline method?

I	F (1)	D (1)	E (4)

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

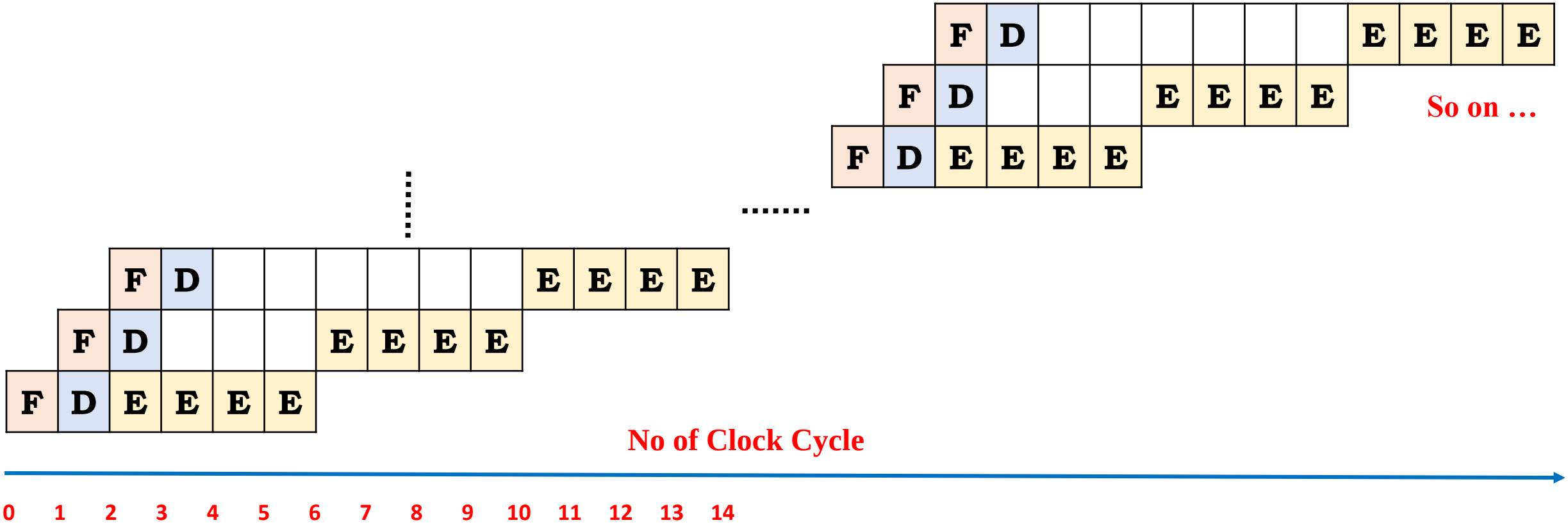
Fetch - 1 Clock cycle

Decoding - 1 Clock cycle

Execution - 4 Clock cycle

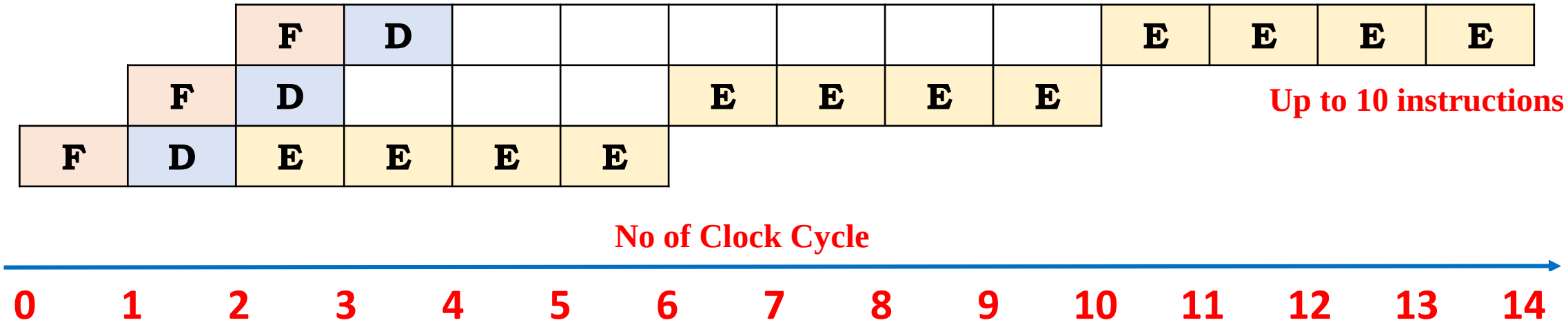
MODEL-3 : PIPELINE PROBLEM-3

Pipeline method



MODEL-3 : PIPELINE PROBLEM-3

Pipeline method



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((10-1) x 4) = 6 + (9 x 4) = 6 + 36 = **42 Clock cycles**

Total = 4 x 42 + 6 = 168 + 6 = 174 Clock cycles

MODEL-3 : PIPELINE PROBLEM-4

Problem - 4: If the pipeline is flushed for every 10 instructions then find the number of clock cycles required to execute 141 instructions with pipeline method?

I	F (2)	D (1)	E (3)

Fetch - 2 Clock cycle

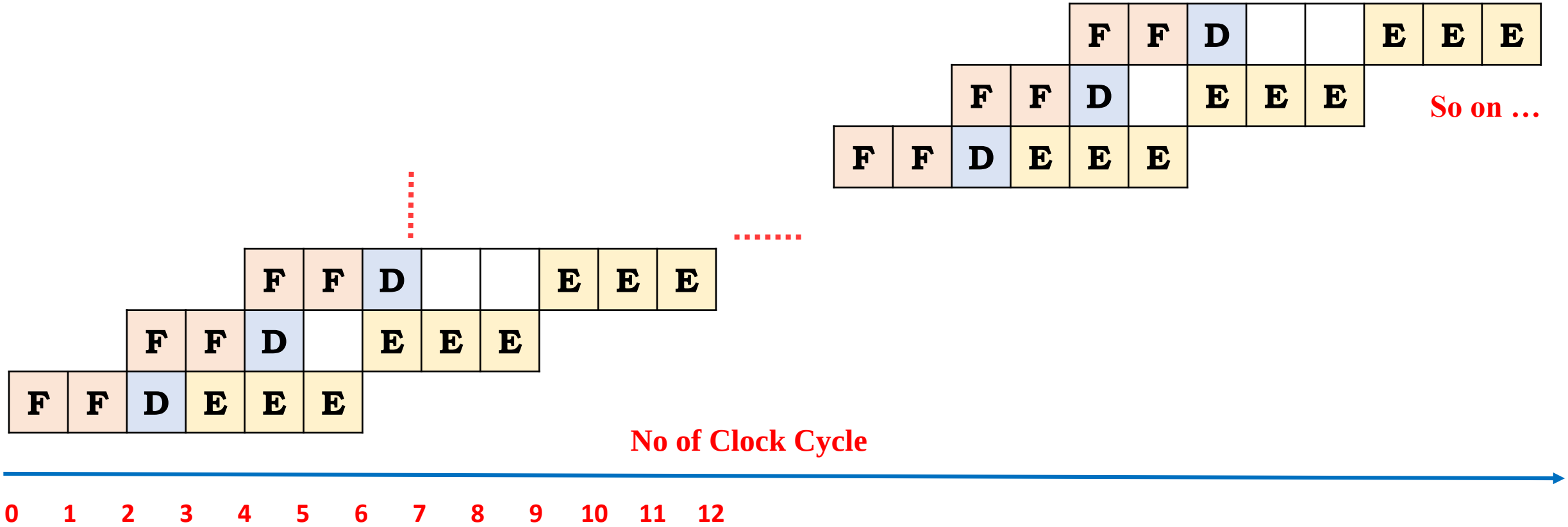
Decoding - 1 Clock cycle

Execution - 3 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

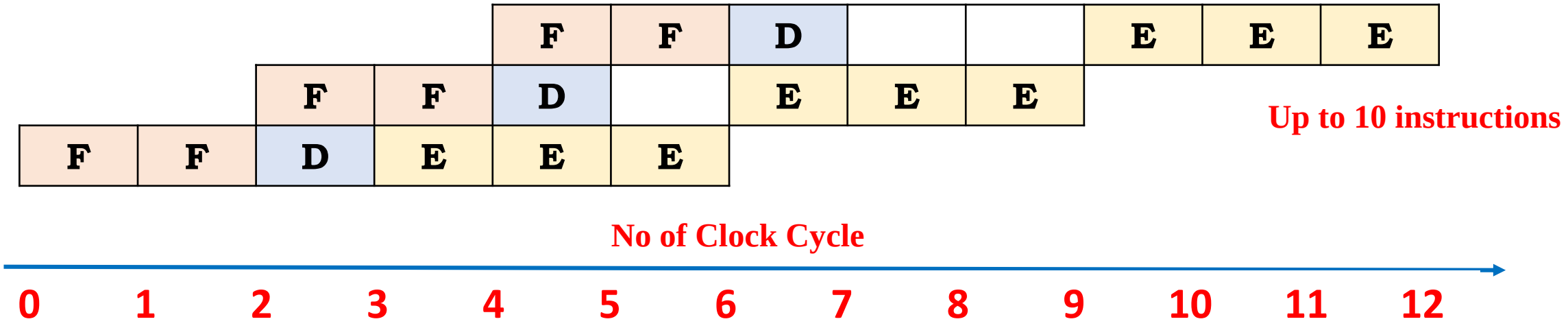
MODEL-3 : PIPELINE PROBLEM-4

Pipeline method



MODEL-3 : PIPELINE PROBLEM-4

Pipeline method



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((10-1) x 3) = 6 + (9 x 3) = 6 + 27 = **33 Clock cycles**

No of Clock Cycle required to execute 141 instructions = 14 x 33 + 6 = 462 + 6 = **468 Clock cycles**

MODEL-3 : PIPELINE PROBLEM ASSIGNMENT-1

Problem - 1: If the pipeline is flushed for every 15 instructions then find the number of clock cycles required to execute 1501 instructions with pipeline method?

I	F (2)	D (1)	E (4)

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

Fetch - 2 Clock cycle

Decoding - 1 Clock cycle

Execution - 4 Clock cycle

MODEL-4 PROBLEMS

MODEL-4 : PIPELINE PROBLEM-1

Problem 1: Find the **number of clock cycles** required to execute 10 instructions with pipeline method and without pipeline method for the following instruction structure?

Improve the pipeline structure.

I	F (1)	D (1)	E (4)

Fetch - 1 Clock cycle

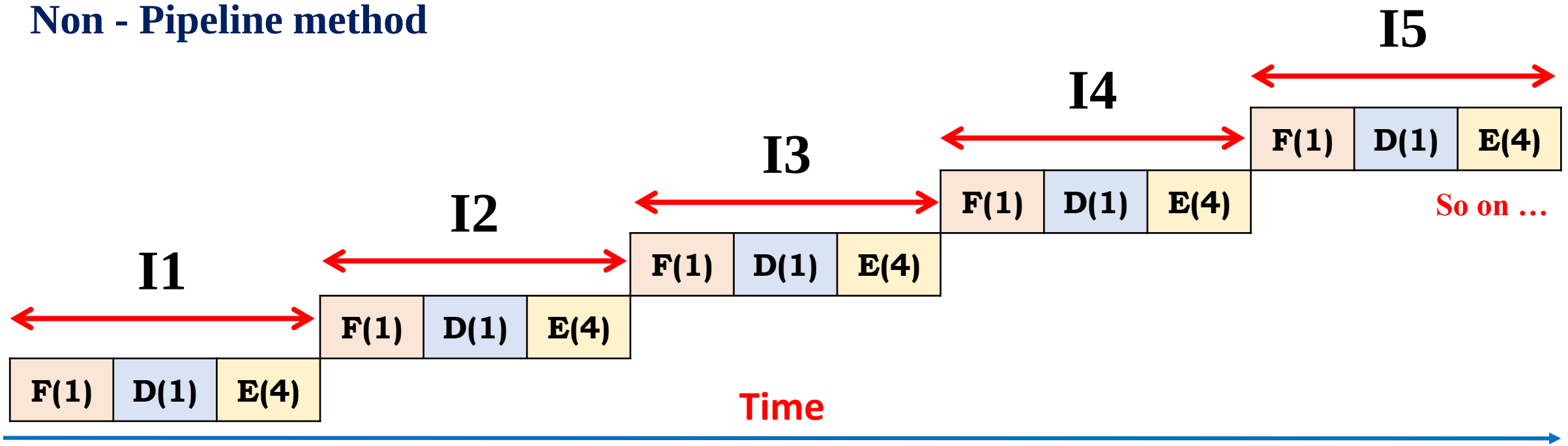
Decoding - 1 Clock cycle

Execution - 4 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-4 : PIPELINE PROBLEM-1

Non - Pipeline method



No of Clock Cycle required to execute 10 instructions is

= (No of instructions) x (Total no of required for single instruction)

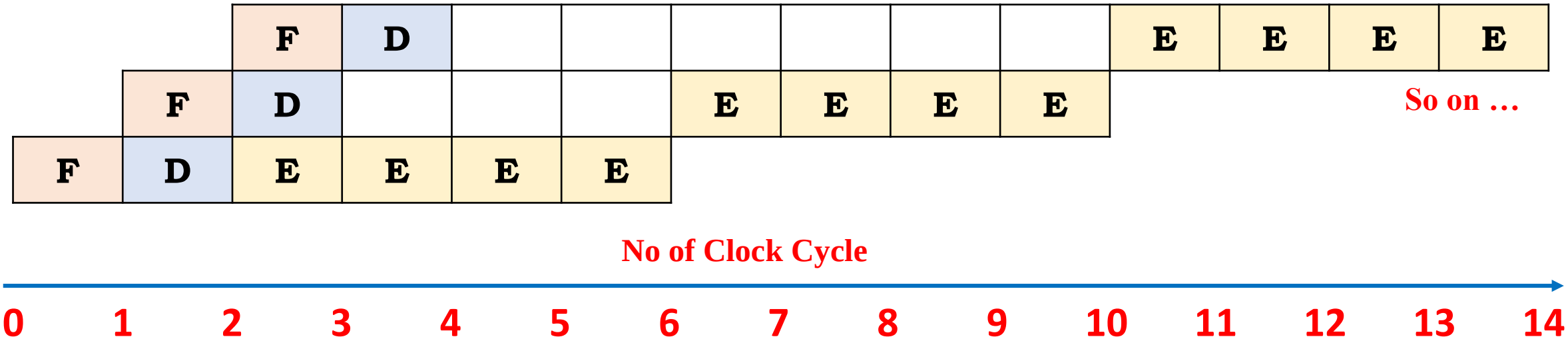
= 10 x 6 = **60 Clock cycles**

MODEL-4 : PIPELINE PROBLEM-1

Less efficient design of pipeline

Pipeline method

I	F (1)	D (1)	E (4)



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

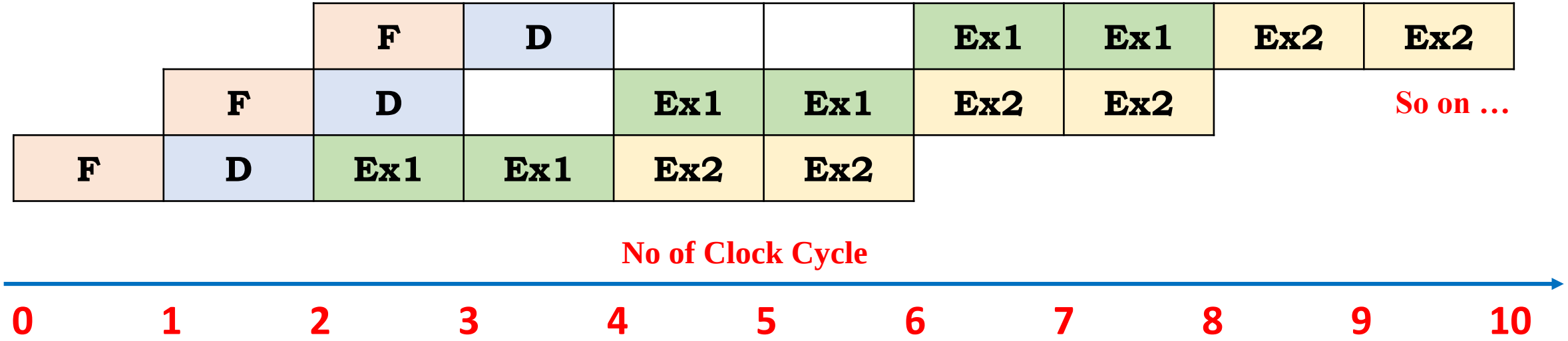
= 6 + ((10 - 1) x 4) = 6 + (9 x 4) = 6 + 36 = **42 Clock cycles**

MODEL-4 : PIPELINE PROBLEM-1

Pipeline method

I	F(1)	D(1)	Ex1 (2)	Ex2 (2)

More efficient design of pipeline: Break the execution in two parts of two cycle each



No of Clock Cycle required to execute 10 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 6 + ((10 - 1) x 2) = 6 + (9 x 2) = 6 + 18 = **24 Clock cycles**

MODEL-4 : PIPELINE PROBLEM-2

Problem 2: Find the **number of clock cycles** required to execute 100 instructions with pipeline method and without pipeline method for the following instruction structure?

Improve the pipeline structure.

I	F (2)	D (1)	E (6)

Fetch - 2 Clock cycle

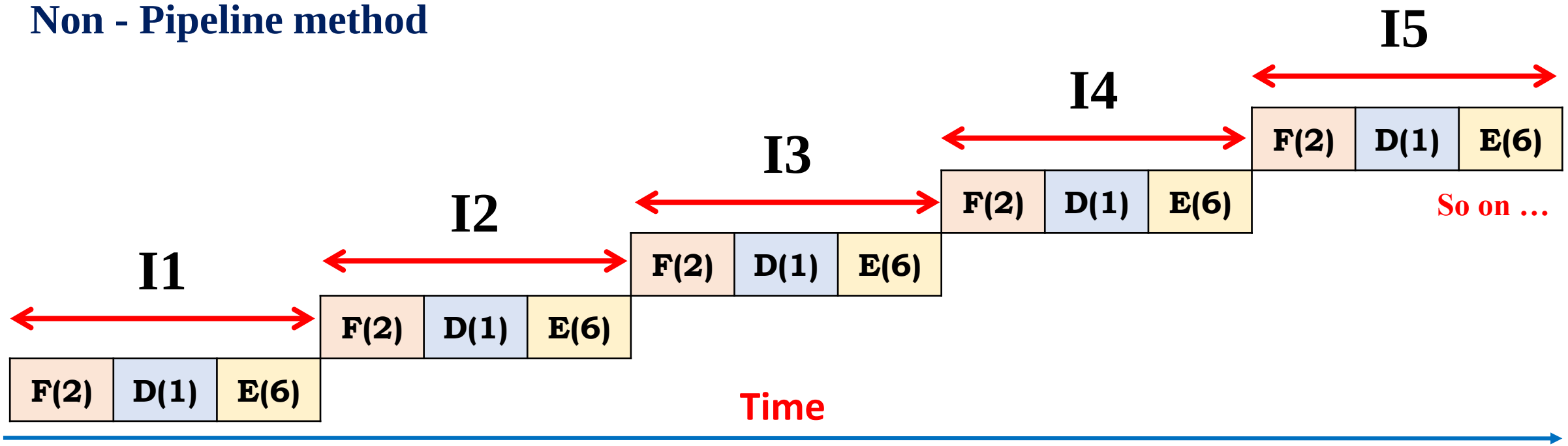
Decoding - 1 Clock cycle

Execution - 6 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-4 : PIPELINE PROBLEM-2

Non - Pipeline method



No of Clock Cycle required to execute 100 instructions is

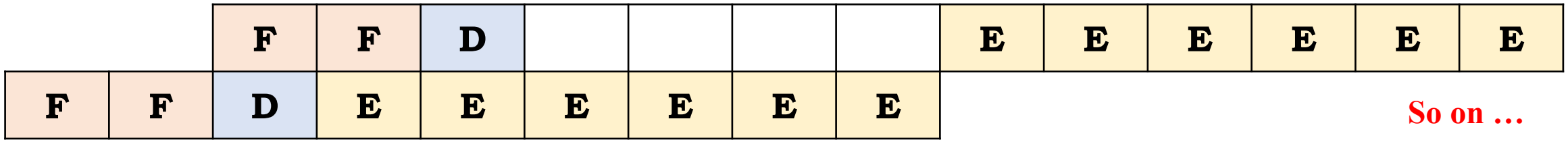
= (No of instructions) x (Total no of required for single instruction)

= 100 x 9 = **900 Clock cycles**

MODEL-4 : PIPELINE PROBLEM-2

Pipeline method

I	F (2)	D (1)	E (6)



No of Clock Cycle required to execute 100 instructions is

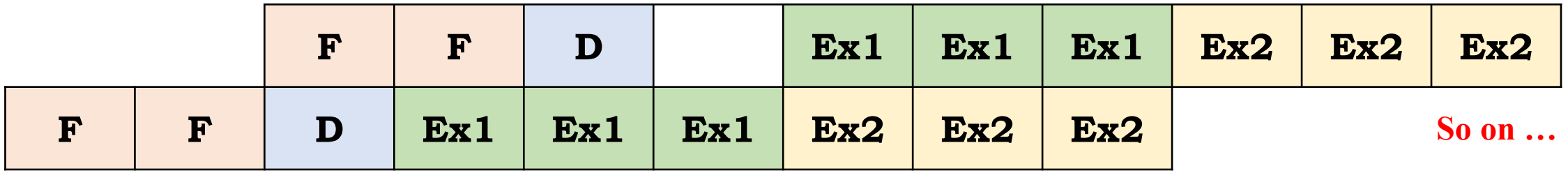
= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 9 + ((100 - 1) x 6) = 9 + (99 x 6) = 9 + 594 = **603 Clock cycles**

MODEL-4 : PIPELINE PROBLEM-2

Pipeline method

I	F(2)	D(1)	Ex1 (3)	Ex2 (3)



No of Clock Cycle

0 1 2 3 4 5 6 7 8 9 10 11 12

No of Clock Cycle required to execute 100 instructions is

= (No of clocks required for 1st instruction)+ ((no of instruction -1) x (difference between two instruction))

= 9 + ((100 - 1) x 3) = 9 + (99 x 3) = 9 + 297 = **306 Clock cycles**

MODEL-4 : PIPELINE PROBLEM ASSIGNMENT-1

Problem - 1: Find the **number of clock cycles** required to execute 5432 instructions with pipeline method and without pipeline method for the following instruction structure ? **Improve the pipeline structure**.

I	F (2)	D (1)	E (8)

Fetch - 2 Clock cycle

Decoding - 1 Clock cycle

Execution - 8 Clock cycle

I1
I2
I3
I4
I5
I6
I7
I8
I9
I10

MODEL-5 PROBLEMS

Problem-:

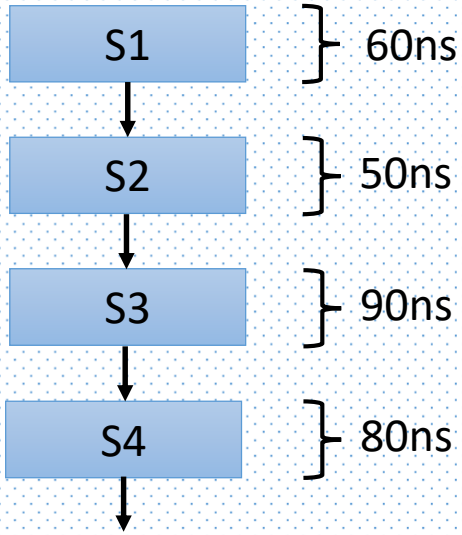
Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns.
Calculate-

1. Pipeline cycle time
2. Non-pipeline execution time
3. Speed up ratio
4. Pipeline time for 1000 instructions
5. Sequential time for 1000 instructions
6. Throughput

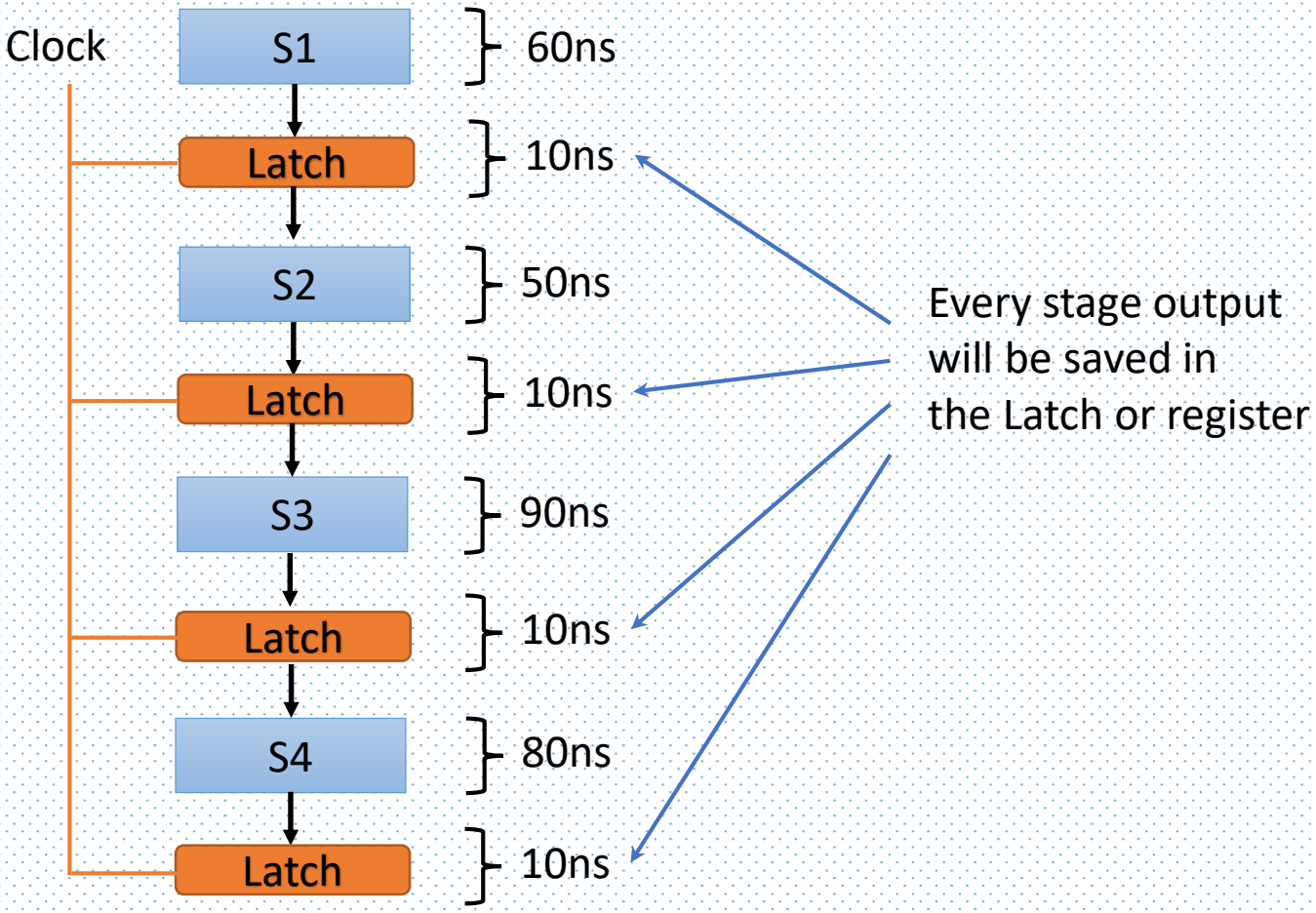
Solution:

Given-

- Four stage pipeline is used
- Delay of stages = 60, 50, 90 and 80 ns
- Latch delay or delay due to each register = 10 ns



Non-Pipelined Architecture



Pipelined Architecture

Note: In any stage of pipeline, the output of each stage will be moved to the next state after the 100 ns (max(60,50,90,80) + 10 ns)

Part-01: Pipeline Cycle Time-

Cycle time = Maximum delay due to any stage + Delay due to its register (Latch)
= Max { 60, 50, 90, 80 } + 10 ns
= 90 ns + 10 ns
= 100 ns

Part-02: Non-Pipeline Execution Time-

Non-pipeline execution time for one instruction = 60 ns + 50 ns + 90 ns + 80 ns
= 280 ns

Part-03: Speed Up Ratio-

Speed up = Non-pipeline execution time / Pipeline execution time
= 280 ns / Cycle time
= 280 ns / 100 ns
= 2.8

Part-04: Pipeline Time For 1000 Instructions-

Pipeline time for 1000 instructions

= Time taken for 1st instruction + Time taken for remaining 999 instructions

= 1 x 4 clock cycles + 999 x 1 clock cycle

= 4 x cycle time + 999 x cycle time

= 4 x 100 ns + 999 x 100 ns

= 400 ns + 99900 ns

= 100300 ns

Part-05: Sequential Time For 1000 Instructions-

Non-pipeline time for 1000 tasks

= 1000 x Time taken for one instruction

= 1000 x 280 ns

= 280000 ns

Part-06: Throughput-

Throughput for pipelined execution = Number of instructions executed per unit time

= 1000 instructions / 100300 ns


Thank You