Srinivasan Subramaniyan

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Objective

Obtain an Internship that will leverage my technical and research experience and strengthen my industry experience in Computer Engineering. My key areas of expertise include Computer architecture, GPU performance optimization, Embedded systems design and Hardware design techniques.

Experience

The Ohio State University **Jan 22 - May 22**
Graduate Teaching Assistant *Columbus, Ohio*

- Teaching Assistant for the course Introduction to Digital Logic (ECE 2060).
- Will help 350 students by clearing their doubts and hosting office hours.

The Ohio State University **Aug 21 - Present**
Research Assistant *Columbus, Ohio*

- Working as a Research Assistant at the Power-Aware Computer Systems Laboratory (PACS).
- Pursuing my PhD Dissertation under the supervision of Dr Xiaorui Wang.

Centre for Heterogeneous and Intelligent Processing System **Feb 21 - Aug 21**
Research Fellow *Bangalore, India*

- **Matrix Multiplication in FPGAs**: Designed kernels for Sparse matrix multiplication using Xilinx design tools.
- Achieved an energy efficient design which had less power consumption and high throughput.
- Research work is accepted to be published at VLSID 2022.

Computer Architecture and High Performance Computing Lab **Aug 19 - Dec 20**
Junior Research Fellow *Bangalore, India*

- **ECHO**: Error-correcting codes in high-performance communication systems through joint exploration of inference algorithms and parallel architectures.
- Funded by the Department of Science and Technology (DST), India and Fundação para a Ciência e Tecnologia (FCT) Portugal.
- Developed kernels for the Min-Max algorithm targeting Field Programmable Gate Arrays (FPGAs) for comparing various design parameters.
- Visiting Research Fellow with the Instituto de Telecomunicações in the Department of Electrical and Computer Engineering at the University of Coimbra Portugal from March 21 till June 30th.
- Published two papers in SIPS 2020 and FCCM 2020. Journal paper was accepted at the IEEE communications and surveys tutorials during this tenure.

Computer Architecture and High Performance Computing Lab **Aug 19 - Dec 20**
Internship *Bangalore, India*

- **Performance comparisions for DNN:** Worked on the Indo Swedish project "Towards Next Generation Embedded Systems: Utilizing Parallelism and Re-configurability".
- Funded by the Department of Science and Technology, India and Vinnova, Sweden.
- A division of workload across CPUs, GPUs and FPGAs was proposed to reduce the overall energy consumption.

National Institute of Technology Karnataka **Dec 17 - Jan 18**
Internship *Mangalore, India*

- SiGML application for creating gesture animations based on sign notations. Developed an android application for the same.

Education

The Ohio State University **Aug. 2021 – Present**
Doctor of Philosophy *Electrical and Computer Engineering* *Columbus, Ohio*

Amrita Vishwa Vidyapeetham **Aug.2015 – May 2019**
Bachelors of Technology *Electronics and Communication Engineering* *Kollam, India*

Relevant Coursework

- Computer Architecture
- Embedded Systems
- Hardware Design
- Digital Circuits
- Signals and Systems
- Internet of Things
- Applied Linear Algebra
- Computer Organisation

Conference Publications

1. Subramaniyan, S., Ferraz, O., Ashuthosh, M. R., Krishna, S., Wang, G., Cavallaro, J. R., ... Purnaprajna, M. (2020, October). Pushing the Limits of Energy Efficiency for Non-Binary LDPC Decoders on GPUs and FPGAs. In 2020 IEEE Workshop on Signal Processing Systems (SiPS) (pp. 1-6). IEEE.

2. Ferraz, O., Subramaniyan, S., Wang, G., Cavallaro, J. R., Falcao, G., Purnaprajna, M. (2020, May). Gbit/s Non-Binary LDPC Decoders: High-Throughput using High-Level Specifications. In 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) (pp. 226-226). IEEE.

3. K. Vanishree, A. George, S. Gunisetty, S. Subramanian, S. Kashyap R. and M. Purnaprajna, "CoIn: Accelerated CNN Co-Inference through data partitioning on heterogeneous devices," 2020 6th International Conference on Advanced Computing and Communication Systems (ICACCS), 2020, pp. 90-95, doi: 10.1109/ICACCS48705.2020.9074444.

Journal Publication

1. Ferraz, O., Subramaniyan, S., Chinthalaa, R., Andrade, J., Cavallaro, J. R., Nandy, S. K., ... Falcao, G. (2021). A Survey on High-Throughput Non-Binary LDPC Decoders: ASIC, FPGA and GPU Architectures. IEEE Communications Surveys Tutorials.

Technical Skills

Languages: Python, C++, Verilog
Framework: Pytorch, Keras
Tools: Xilinx Design tools, Matlab

Volunteer Experience/ Extracurricular

IEEE GSB **Fall 2021 – Present**
Volunteer *The Ohio State University*

- Helped conduct career fair at the Ohio State University .