Contact Information

805, 059 Dreese Laboratories, Columbus Ohio 43202 USA
+1-740-274-2814 subramaniyan.4@osu.edu Linkedin Github Google Scholar Personal webpage

Research Interest

GPU Architecture and Scheduling, Parallel Computing, Architectural Vulnerabilities in Accelerators, Deep Learning across accelerators.

Summary

Passionate and innovation-focused PhD. student, with three years of extensive research experience in Computer Engineering. My key areas of expertise are in Computer architecture, GPU Scheduling, and Parallel computing.

Education

The Ohio State University Jan 22- Present
- Qualified Ph.D. Student in the Electrical and Computer Engineering Department
- Minor in Computer Science and Engineering
- Advisor : Xiaorui Wang

Amrita Vishwa Vidyapeetham Aug 15 - May 19
- Bachelor in Electronics and Communication Engineering
- Undergraduate Thesis Advisor : Dr Madhura Purnaprajna

Research Experience

Power-Aware Computer Systems (PACS) Laboratory (Research Assistant) Jan 22 - Present
- Advisor : Xiaorui Wang
- GP-GPU Scheduling main research area for Ph.D. Dissertation

AMD Research (Research Intern) May 22- Aug 22
- Mentors : Bradford Beckmann and Pete Ehrett
- Worked on scheduling GP-GPU kernels for Graph applications.

Computer Architecture and High-Performance Lab (Research Fellow) Jan 19 - Aug 21
- Mentors : Dr Madhura Purnaprajna, Gabriel Falcao
- Visiting Research Fellow with the **Instituto de Telecommunications** in the Department of Electrical and Computer Engineering at the University of Coimbra Portugal from March 21 to June 30th

Conference Publications

1. Ashuthosh, M. R., Krishna, S., Sudarshan, V., Subramaniyan, S., Purnaprajna, M. (2022, February). MAPPARAT : A Resource Constrained FPGA-Based Accelerator for Sparse-Dense Matrix Multiplication. In 2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID) (pp. 102-107). IEEE Computer Society.
2. Subramaniyan, Srinivasan, Oscar Ferraz, M. R. Ashuthosh, Santosh Krishna, Guohui Wang, Joseph R. Cavallaro, Vitor Silva, Gabriel Falcao, and Madhura Purnaprajna. "Pushing the limits of energy efficiency for non-binary LDPC decoders on GPUs and FPGAs." In 2020 IEEE Workshop on Signal Processing Systems (SiPS), pp. 1-6. IEEE, 2020.
3. Ferraz, O., Subramaniyan, S., Wang, G., Cavallaro, J. R., Falcao, G., Purnaprajna, M. (2020, May). Gbit/s non-binary LDPC decoders : High-throughput using high-level specifications. In 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) (pp. 226-226). IEEE.

Journal Publications

1. Ferraz, Oscar, Srinivasan Subramaniyan, Ramesh Chinthalaa, JoÃ£o Andrade, Joseph R. Cavallaro, Soumitra K. Nandy, Vitor Silva, Xinmiao Zhang, Madhura Purnaprajna, and Gabriel Falcao. "A Survey on High-Throughput Non-Binary LDPC Decoders : ASIC, FPGA, and GPU Architectures." IEEE Communications Surveys Tutorials 24, no. 1 (2021) : 524-556.
2. Subramaniyan, Srinivasan, Oscar Ferraz, M. R. Ashuthosh, Santosh Krishna, Guohui Wang, Joseph R. Cavallaro, Vitor Silva, Gabriel Falcao, and Madhura Purnaprajna. "Enabling High-Level Design Strategies for High-Throughput and Low-power NB-LDPC Decoders." IEEE Design Test (2022).

Selected Recognition

- A.K. Choudhary Best Paper Award" at The 35th International Conference on VLSI Design and The 21st International Conference on Embedded Systems (VLSID 2022).
- Recipient of Amrita Scholarship during my undergraduate degree in Amrita Vishwa Vidyapeetham.

Research Projects

OptiALS : Scheduling the Alternate Least Squares Algorithm in GPUs

- Mentor : Pete Ehrett and Wang Xiaorui
- Performed experiment to understand the sensitivity of the ALS algorithm in the MI-100 GPUs
- Designed OptiALS which gives us the optimal solution for scheduling ALS algorithm in the GPU

Sparse Matrix Multiplication on FPGAs

- Mentor : Madhura Purnaprajna
- Designed kernels for Sparse matrix multiplication using Xilinx design tools.
- Achieved an energy-efficient design that had less power consumption and high throughput.

Design of High-Performance NB-LDPC Decoders

- Mentor : Madhura Purnaprajna
- Developed kernels for the Min-Max algorithm targeting Field Programmable Gate Arrays (FPGAs)
- Performed Design Space exploration for optimizing latency and resource utilization.
- Mentor : Madhura Purnaprajna

Performance Comparision for Deep Neural Networks in a cross accelerator System

- Mentor : Madhura Purnaprajna
- Performance measurements for different neural networks from the TANGO benchmark suite were performed.
- A division of workload among CPU, GPU, and FPGA was proposed.

Skills

Programming languages : C, C++, Python, Cuda, OpenMp, MPI, Verilog, hip, Shell.

Scientific Software : Matlab, Vitis Design tools, ROCM Stack, Android Studio, GP-GPU Sim.

Teaching Experience

- **The Ohio State University** Jan 22 - Present

  Supervised the course "Introduction to Digital Logic ECE 2060" for the fall and spring semesters. The class comprised 450 *Students from both the ECE and CSE Department. I was responsible for Grading the homework, Managing the TAs, and publishing the grades for students.*