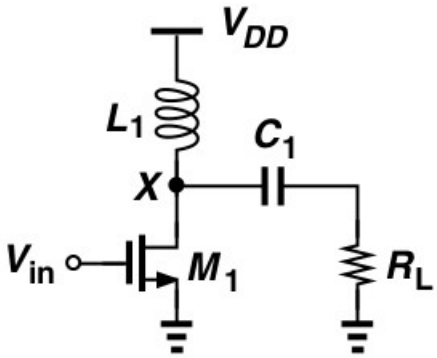
DESIGN PROCEDURE & CHALLENGES :

TOPOLOGY :



PROCEDURE :

We start with the above topology of " Common-Source Power Amplifier with Inductive Load"

- Given $R_L = 50\Omega$ and minimum P_{out} delivered is 10mW (10dBm), we calculate the minimum voltage swing at the node X and I_{rms} required.

  $P_{out} = Vs^2/2R_L$, => V_s (amplitude voltage swing at X) = 1V, which allows a $V_{d,sat}$ = 0.2 V.

  $P_{out} = I_{rms}^2 R_L$, => I_s (amplitude current swing at X) = 20mA, which allows I_{bias} = 20mA (to satisfy cut-off requirement). Since the voltage swing required at output is reasonable and within Vdd, we don't require any matching network to tune down the load resistance seen by the drain of transistor.

  Assuming the length of the MOSFET to be 120nm, we can proceed to compute W of the transistor. $I_{bias} = 0.5 * \mu_n C_{ox} W/L * V_{d,sat}^{2,}$ which gives W = 80um. The bias inductor L_bias is set to 4nH .

- For the assumed values of parameters the P_{out} is fairly satisfied. To improve Gain, we increase W and Ibias proportionately and tune L_bias to check on AM-PM deviation. We finally arrive at W = 120um, Ibias = 25mA, L_bias = 5nH

CHALLENGES :

- My phase deviation in AM-PM charectristic slightly exceeds the given specs, but I am unable to fix it anything better. Not sure about the reason.

Note : I'm not explicitly attaching hand calculations as I have mentioned clearly how to arrive at basic parameters in the first paragraph of design procedure.