# EE6320 Design Project 3: VCO Design – due 11:59pm Sunday 25/04/2021

In this project, you are asked to design a fully-differential LC-VCO that meets or exceeds the specifications given below. Use the IBM 130nm CMOS process parameters used by you earlier. Design the VCO for the following specs:

- $f_0$ = 3.8 to 4.2GHz (400 MHz tuning range)
- $V_{DD}$ = 1.2V
- Minimum VCO output single-ended amplitude = 1V
- Phase noise specification: -115dBc/Hz @ 1MHz offset and -140dBc/Hz @ 20MHz offset
- Maximum number of inductors = 2. In the case of a nmos-only or pmos-only VCO, the two sections of a symmetrical centre-tap inductor is considered as 1 inductor, with the centre tap connected to $V_{DD}$/ground. The second inductor can be used in various ways.
- Tuning should be done using a combination of MOS-transistor-based varactors for fine-tuning and a binary weighted switched-capacitor bank for coarse-tuning. The fine-tuning circuit should exhibit a nominal $K_{VCO}$ of 100MHz/V over the usable tuning range.
- There should be about 33% frequency overlap between fine tuning curves of adjacent coarse tuning bits.
- Minimise overall power consumption

Notes:

1. No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 15 at 4GHz. All capacitors can be assumed to be ideal.
2. Include and discuss your VCO design procedure and architecture choice in your report. Remember to include the $K_{VCO}$ plot as well as VCO transient simulation output to show startup behaviour.