Table 1: VCO Performance Summary Table
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	Design Metric	Performance	Specification
Output Amplitude	f_o = 3.8GHz	1.069 V	≥1V
	f_o = 4.0GHz	1.085 V	≥1V
	f_o = 4.2GHz	1.101 V	≥1V
Phase Noise [1MHz offset]	f_o = 3.8GHz	-116.89 dBc/Hz	≤−115dBc/Hz
	f_o = 4.0GHz	-117.32 dBc/Hz	≤−115dBc/Hz
	f_o = 4.2GHz	-117.41 dBc/Hz	≤−115dBc/Hz
Phase Noise [20MHz offset]	f_o = 3.8GHz	-145.39 dBc/Hz	≤−140dBc/Hz
	f_o = 4.0GHz	-145.26 dBc/Hz	≤−140dBc/Hz
	f_o = 4.2GHz	-145.88 dBc/Hz	≤−140dBc/Hz
Tuning Range	Total Tuning Range [Specify Range]	407 MHz	≥400MHz
	Number of bits in coarse-tuning	3 bits	
	Voltage range in fine-tuning	0.1V – 1.15V	
	Average K_{VCO}	100.7 MHz/V	≈ 100MHz/V
	% variation in K_{VCO}	6.55 % **	Minimal
Power [4.2GHz]	VCO average power consumption [Excluding Bias]	3.77 mW	
	Bias circuit power consumption	0.24 mW	
Other	Sum of all capacitances [in capacitor bank]	434 fF + 1uF*	
	Inductance used	4.04 nH	
	Simulator Used	Eldo	

Percentage Overlap between F_osc Vs V_cntrl curves : 55 % (Specification : 33 %)

* 1 uF capacitor used at tail to filter even harmonics (to reduce phase noise).

** % Variation calculated as average of all variations corresponding to each curve.