EE6320 Project 1: LNA Design – due Sunday 21/03/2021 (11:59pm)

In this project, you are asked to design a differential cascoded common source Low-Noise Amplifier (CS-LNA) for the specifications given below. The basic circuit topology should be that discussed in class. However, you can modify it with circuit techniques to improve its performance, as long as you support it with analytical and simulation results. Use the IBM 130nm CMOS process parameters supplied to you through the class website. Design for the following specs:

- Frequency of operation f_0 = 1.9 to 2.1GHz
- Differential R_{in} = 100Ω; S11 < -10dB between 1.9GHz to 2.1GHz. For all your simulations, you can place an ideal balun from ahdlLib library between single-ended input port with impedance of 50Ω and differential input of LNA.
- Voltage gain ≥ 20 dB over the complete band. Assume the LNA drives a load capacitance of 1pF differential. This will represent the mixer input capacitance as well as any tuning required for process variations in tank resonance frequency.
- NF ≤ 1.5dB.
- IIP_3 ≥ -10dBm {Use two tones separated by 1MHz; choose the extrapolation point carefully}
- Minimise power consumption (P_{diss}); V_{DD} = 1.2V

Note 1: No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 15 at 2GHz). All capacitors can be assumed to be ideal.

Note 2: If the gate inductor becomes too large (>7nH), its Q will limit your noise figure. For this project, assume that the gate inductor will be implemented using a high-Q off-chip inductor. Therefore, add a resistance in parallel with the gate inductor such that its Q = 50 at 2GHz.