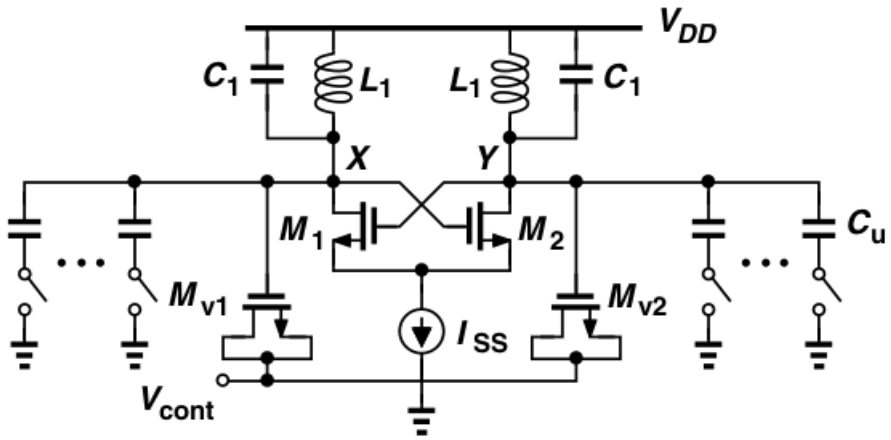
DESIGN PROCEDURE & CHALLENGES :

TOPOLOGY :



PROCEDURE :

We start with the above topology of " Voltage Controlled Fully-Differential Cross-Coupled LC Oscillator"

- Let us assume a single-ended load inductance of 2 nH (i.e., a differential load inductance of 2 nH) with a Q of about 15 at 4 Ghz (**Q = R/ωL**). Such values yield a single-ended parallel equivalent resistance of 754Ω, requiring a tail current of about 2.1 mA to yield a single-ended amplitude of output swing of **(2/π)*R_p* I_SS > 1 V.**
- To begin with, choose the value of CC NMOS transistor width to be 200um and length to 0.12um (infact set the length of all MOSFET at 0.12um). Vary the width of varactor to tune the oscillation frequency to meet the upper limit of the band requirements (4.2 Ghz, since later adding switch capacitors parallel will reduce the oscillation frequency).
- Check the oscillation frequency limits and tune L1 and C_var to set slope (K_vco) requirements. If the amplitude of the output reduces try balancing by increasing the I_bias.
- To enable the VCO to generate all frequencies in the range of 3.8 Ghz – 4.2 Ghz and a binary capacitor switch bank (switches can be implemented by biasing the switch transistors at 0V (open) and Vdd (closed)). Fine-tuning might be required at this stage as the capacitor bank might contribute to noise and affect oscillation frequency. Switch-Bank capacitors are chosen in the same order of C_var (started with 20fF and tuned for better overlap and range optimisation).
- After all this , it is found that the Noise specs aren't satisfactory (-98 dBc/Hz at 1 Mhz offset and -132 dbc/Hz at 20 Mhz offset). One possible reason could be the effect of 2ωo frequency noise at tail current source that gets translated to ωo after mixing with the oscillation signal. This is removed using a large capacitor (1uF) added parallel to the tail current source. With this modification we are able to meet the specs and have mentioned it in summary table.

- We once again fine tune parameters to see that K_vco, amplitude, overlap and noise conditions are satisfied.

CHALLENGES :

- One issue with the above modification is that the single-ended o/p signals are kind of clipped (distorted) of below the threshold voltage (which was not observed in the absence of tail capacitor).
- Initially using the same switch sizes for all the bits in the capacitance bank, resulted in uneven gaps between the bands, due to the same parasitic capacitance of the switches. Resizing the switch widths in the ratio of their respective capacitances, rectified this.

Note : I’m not explicitly attaching hand calculations as I have mentioned clearly how to arrive at basic parameters in the first paragraph of design procedure.