Project report on
Alarm Clock using FPGA

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1 Introduction

Field Programmable Gate Array (FPGA) has wide variety of uses. Using FPGA makes processing of a program faster by parallel processing.

While FPGAs can be used to solve any computational problem (like computers), and offer more flexibility in terms of the number of things you can do in parallel.

Alarm clock using FPGA is our point of interest here. Using alarm we can remind ourselves and here using FPGA we can get large number of operations on single FPGA.

We will fetch alarm code into a FPGA board. Using some external hardware we will give input to our system. FPGA will give signal after some time which we have given as input. Signal of output will be audio.

2 Block Diagram

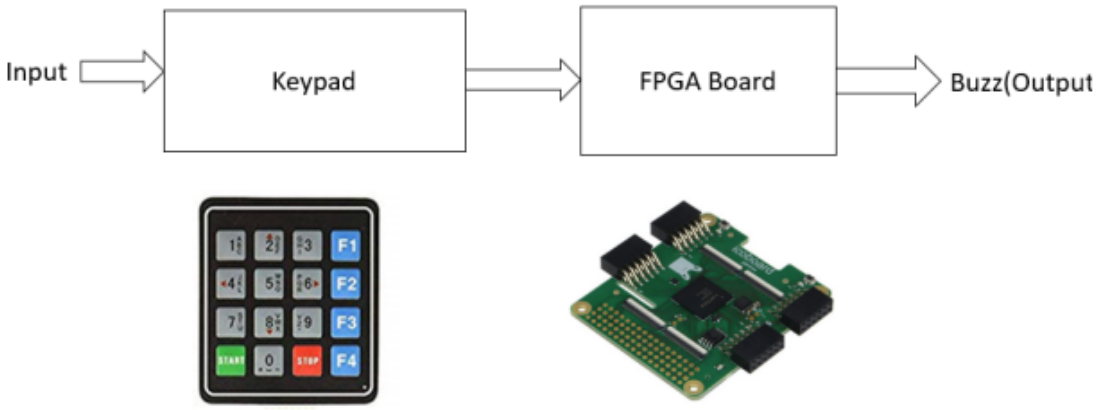

Figure 1: Block diagram

3 Flow Chart

Below Flow chart will explain clearly how this algorithm works on FPGA.

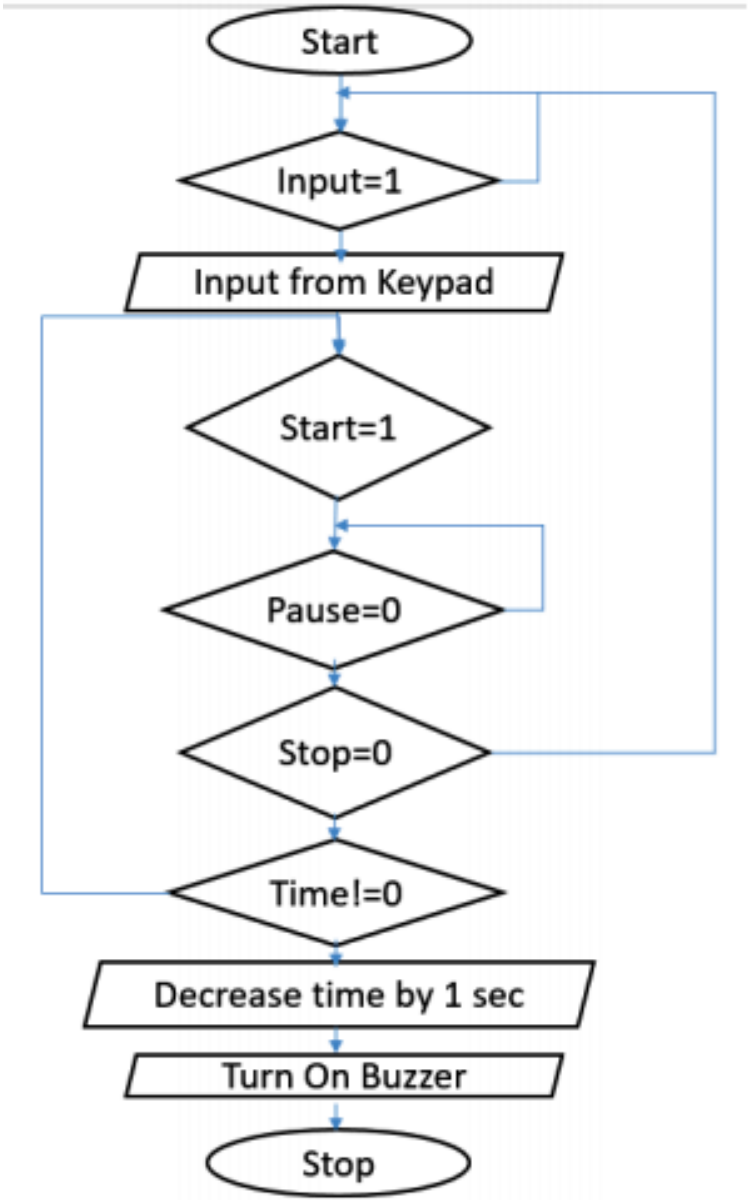

Figure 2: Flow chart

4 Working Process

Before starting we have to fetch the code into FPGA board. If the FPGA board is not in INPUT mode then it will go to starting again and will wait for INPUT mode to activate and on the other hand FPGA is in INPUT mode it will take 6 digit input (i.e. `hh mm ss`). Then FPGA will go into START mode and it will count down the time.

After the START mode if we give STOP mode it will again goes to starting if not after the prescribed time we will get output from the FPGA board to the output, after receiving a signal from the board buzzer will give some sort of audio signal to remind us that alarm time completed. After audio signal we stop or reset using STOP/RESET mode.

5 Result

On performing all these MODES of operations we will get output. Here output is audio signal(`buzzer`).