Project report on
Alarm Clock using FPGA

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Introduction

Field Programmable Gate Array (FPGA) has wide variety of uses. Using FPGA makes processing of a program faster by parallel processing.

Alarm clock using FPGA is our point of interest here. We will fetch alarm code into a FPGA board. Using some external hardware we will give input to our system. FPGA will give signal after some time which we have given as input. Signal of output will be audio.

Components required are FPGA Board, push buttons, Buzzer/LED, Connecting cables

Block diagram

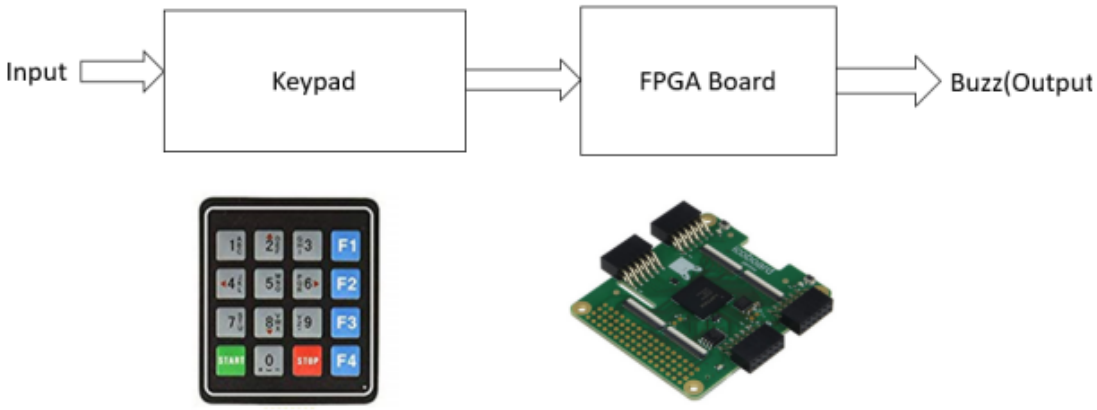

Figure 1: Block diagram

Flow Chart

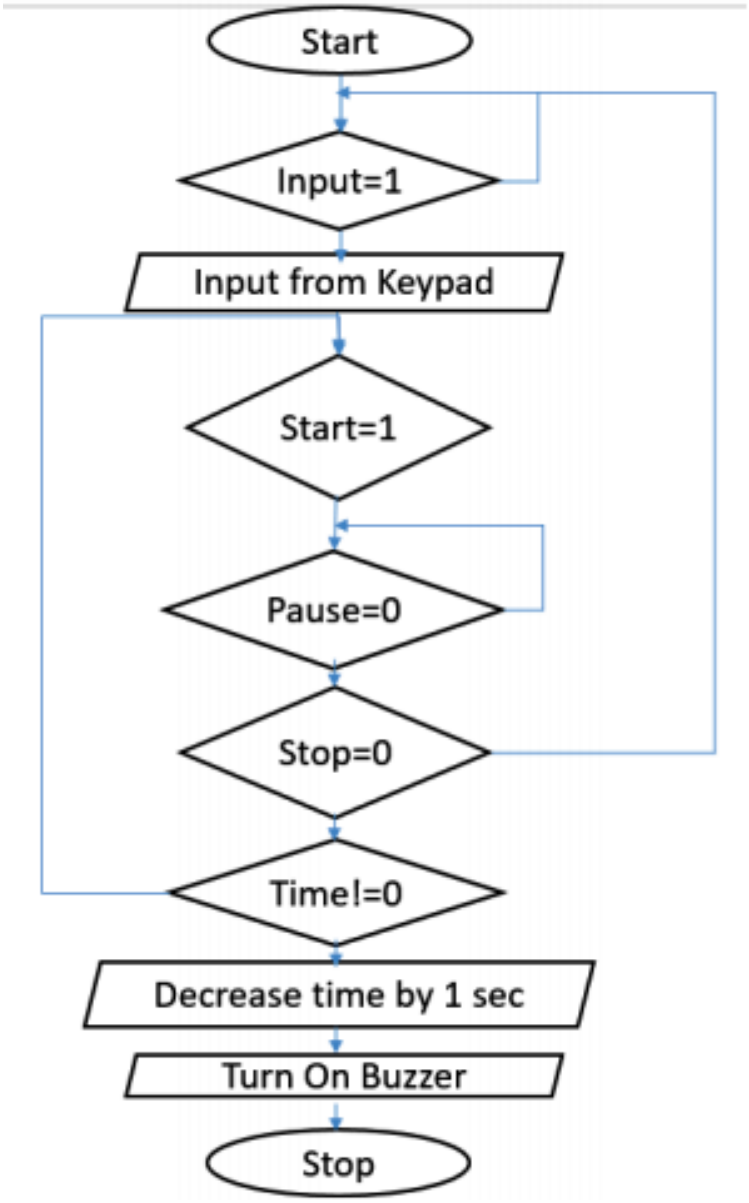

Figure 2: Flow chart

Working Process

We will first dump alarm code into FPGA board. If it is in INPUT mode it will take 6 digit input (i.e. `hh mm ss`). Then FPGA will go into START mode and it will count down the time. After the prescribed time we will get output from the FPGA board to the output, buzzer will give some audio signal to remind us that alarm time completed. After Buzzer it will go into STOP/RESET mode.

Result

On performing all these MODES of operations we will get output. Here output is audio signal(`buzzer`).