Design of Manchester Carry Chain Adder Using High Speed Domino Logic

ABSTRACT

Dynamic logic circuits are preferred over static logic circuits for their increased speed performance and lower power consumption. However, they are found prone to false evaluation while cascading multiple stages of dynamic logic circuits. To overcome this problem, the domino logic circuits were proposed by researchers.

Manchester Carry Chain Adder design is explored for use with domino logic and comparison of various domino logic topologies intended for improved noise immunity and reduced leakage current against the proposed structure have been carried out. In this project we will design wide fan-in gates and 8-bit Manchester Carry Chain Adder (MCC) based on various high speed domino logic circuit topologies using PSPICE (Personal Simulation Program for Integrated Circuits Emphasis) tool.

Design of 8-bit OR gate, using High Speed Domino (HSD) topology consumes lower power in comparison with Controlled-Current Comparison-based domino logic (C3D) topology. Furthermore, we will estimate that an 8-bit Manchester Carry Chain adder using HSD topology is faster than C3D topology and the leakage power consumption is also reduced .

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