1.

Given that the dynamic RAM refreshes 50 times in a millisecond and each refresh requires 120ns.

The total time the DRAM consumes in a millisecond for memory refresh is = 50 * 120 ns
= 6000 ns

This means that in one millisecond DRAM uses 6000 ns for memory refresh

Percentage of memory total operating time to be given for memory refresh = 6000ns / 1ms
= 6000ns / 1000000ns

= 0.0006

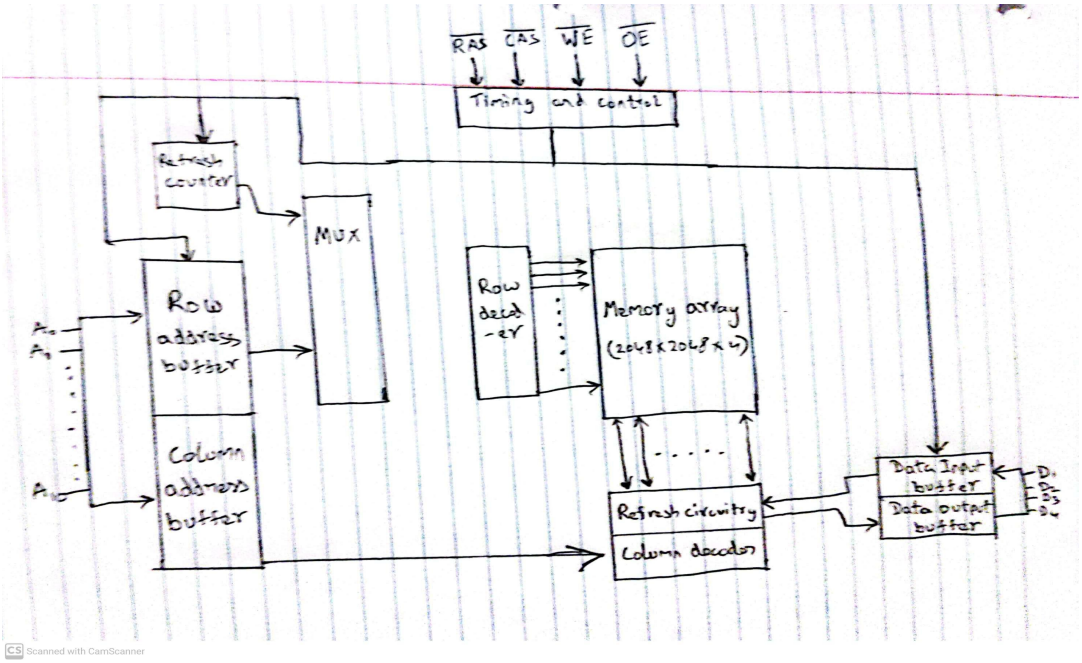
= **0.6%**

Since DRAM spends 0.6% of the time for refresh the rest 99.4% of the time is used for other operations like read and write.
The amount of time in 1ms DRAM uses for operations like read and write = 0.994 * 1ms
= 994000ns

No of memory cycles which can be completed in 994000ns = 994000/ 200 , since each memory cycle is 200 ns.

No of Memory cycles = 994000/200 = **4970 cycles**

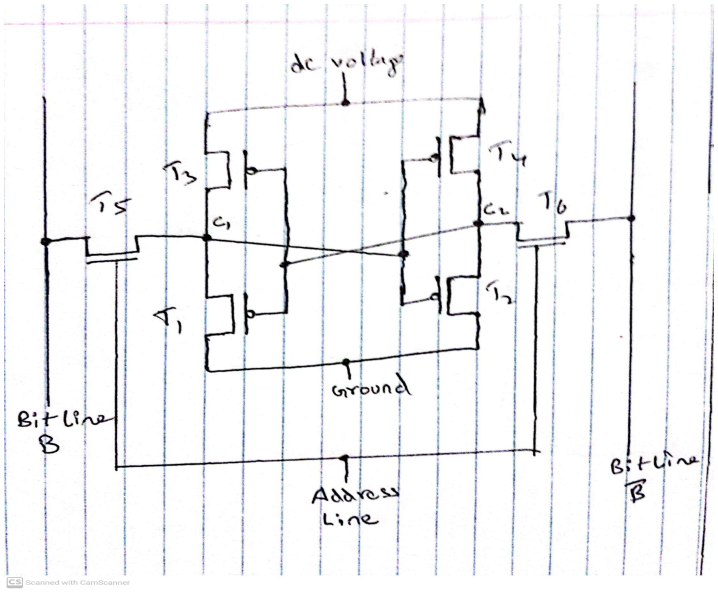
2.



The Figure above shows the organization of an 4M x 4 DRAM. For this RAM we can access 4 bits at a time, so we can actually read or write 4 bits at the same time in parallel. The Memory array consists of 4 square arrays each having a size of 2048 x 2048 elements as shown in the figure above. The elements of an array are connected by both horizontal and vertical lines, the horizontal line connects to the select terminal of each cell and vertical lines connect to the Data-In/Sense terminal of each cell.

Address lines contains the address of the word to be selected. Since we have 2048 rows in a memory array we need 11 address lines to store the address of the word. In general we require $\log_2 W$ address lines. The address lines are then fed to a row decoder and the row decoder finds the row containing the word. In our case row decoder takes 11 address lines as input and selects one of the 2048 rows. An additional 11 address lines select one of 2048 columns of 4 bits per column. Four data lines are used for the input and output of 4 bits to and from a data buffer. During write operation, the bit driver of each bit line is activated for a 1 or 0 according to the value of the corresponding data line. During read operation, the value of each bit line is passed through a sense amplifier and presented to the data lines. The row line selects which row of cells is used for reading or writing. Since only 4 bits can be accessed at a time we need multiple DRAM's connected to the memory controller to read or write a word of data to the bus.
We actually require 22 address lines 11 for rows and 11 for columns but we use only 11 address lines to save on pins. The 22 required address lines are passed through select logic external to the chip and multiplexed onto the 11 address lines. First, 11 address signals are passed to the chip to define the row address of the array, and then the other 11 address signals are presented for the column address. These signals are accompanied by row address select (RAS) and column address select (CAS) signals to provide timing to the chip. The write enable (WE) and output enable (OE) pins determine whether a write or read operation is performed. A DRAM is made with cells that store data as charge on capacitors. Because capacitors have a natural tendency to discharge, DRAM's require periodic charge refreshing to maintain data storage, for which we have a refresh circuitry in the figure. The row decoder receives the output lines from the refresh counter for each row, and the RAS line is turned on. The information is taken out and then put back in the same place. Each cell in the row gets refreshed as a result. Multiplexed addressing plus the use of square arrays result in a quadrupling of memory size with each new generation of memory chips. One more pin devoted to addressing doubles the number of rows and columns, and so the size of the chip memory grows by a factor of 4.

A Static Random-Access Memory (SRAM) is a digital device that uses flip-flop logic-gate configurations to store binary values. SRAM holds the data as long as the power supply is enabled. It doesn't require periodic refresh as in case of a DRAM and hence there is no refresh circuitry in SRAM. The figure below depicts the structure of cell of an SRAM.



It consists of 6 transistors in total, where 4 of the 6 transistors are cross connected in an arrangement that produces a stable logic state. In one of the state point C1 is high and C2 is low, in this state transistors T1 and T4 are off and T2 and T3 are on. In the second state the opposite of this happens where C2 is high and C1 is low, T1 and T4 are on and T2 and T3 are off. The address line in SRAM acts as a switch, where the address lines controls the transistors T5 and T6. The two transistors are switched on when there is a signal on the address line allowing for read or write operation. During the

write operation line the desired bit value is applied to line B, while its complement is applied to line B. For a read operation, the bit value is read from line B.

3.

Both EPROM and EEPROM belongs to the category of read-mostly memory. Read-mostly memory is a variation of read only memory which is useful for applications in which read operations are far more frequent than write operations but for which nonvolatile storage is required.

EPROM:

Erasable programmable read-only memory (EPROM) is read and written electrically. To perform a write operation, all the storage cells must be erased to the same initial state by exposure of the packaged chip to ultraviolet radiation. Erasure is performed by shining an intense ultraviolet light through a window that is designed into the memory chip. This Erasure process is slow and may take 20 mins to perform. The Erasure Process can be repeated. EPROM is costly compared to PROM.

EEPROM:

Electrically erasable programmable read-only memory (EEPROM) can be written into at any time without erasing prior contents. Only the byte or bytes addressed are updated. The write operation takes considerably longer than the read operation. The EEPROM advantage of non-volatility with the flexibility of being updatable in place, using ordinary bus control, address, and data lines. EEPROM is more expensive than EPROM and also is less dense.

Double Data Rate Synchronous Dynamic Random Access Memory(DDR-SDRAM) is an SDRAM that allows for data transfers on both edges of the clock cycle. DDR achieves higher data rates in three ways. First, the data transfer is synchronized to both the rising and falling edge of the clock, rather than just the rising edge. Second, DDR uses higher clock rate on the bus to increase the transfer rate. Third, a buffering scheme is used.

Synchronous DRAM is the most widely used DRAM. The traditional DRAM is asynchronous in nature, whereas the SDRAM exchanges data with the processor synchronous to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states. The traditional DRAM has an access-time delay, the processor presents address and control levels to the memory and DRAM after a delay of access time does the functions. During the access-time delay DRAM performs various other activities like activating the high capacitance of the row and column lines, sensing the data..etc. The Processor need to wait throughout the delay decreasing performance. With synchronous access, the DRAM moves data in and out under control of the system clock. The processor or other master issues the instruction and address information, which is latched by the DRAM. The DRAM then responds after a set number of clock cycles. Meanwhile, the master can safely do other tasks while the SDRAM is processing the request. The mode register and associated control logic is another key feature differentiating SDRAMs from conventional DRAMs. It provides a mechanism to customize the SDRAM to suit specific system needs. The mode register specifies the burst length.

Burst Mode is employed by the SDRAM to eliminate the address setup time and row and column precharge time after the first access. In burst mode after the first bit has been accessed a series of bits can be clocked out rapidly. Burst mode is advantageous when all bits to be accessed in a sequence are in the same row of the array as the initial access.

Since Main memory is composed of a collection of DRAM memory chips. Interleaved memory is designed to compensate for the relatively slow speed of DRAM by spreading memory addresses evenly across memory banks. A number of DRAM chips can be grouped together to form a memory

bank. Memory reads and writes use each memory bank, resulting in higher memory throughput due to reduced waiting for memory banks to become ready for the operations. A system with K banks can service K requests simultaneously, increasing memory read or write rates by a factor of K. If consecutive words of memory are stored in different banks, then the transfer of a block of memory is speeded up.

4.

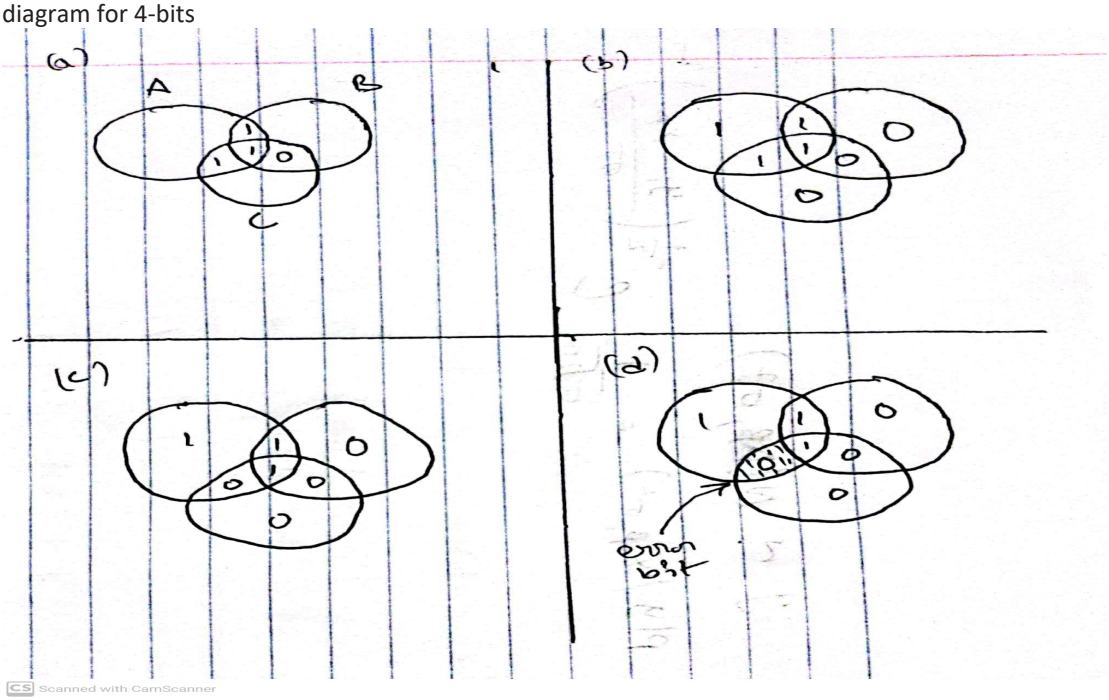
A parity bit is a check bit, which is added to a block of data for error detection purposes. The value of the parity bit is assigned either 0 or 1 that makes the number of 1s in the message block either even or odd depending upon the type of parity.

The two types of parity checking are

- Even Parity: Here the total number of bits in the message is made even.
- Odd Parity: Here the total number of bits in the message is made odd.

Given a word of M bits we add K bits to the M bits which are generated from the M bits. The new word generated is of length M+K and the K bits can be used to say whether the initial word got some errors with it or not, the K bits can be used to detect the errors and also correct the errors. The K bits or codes which has the properties mentioned are called error correcting codes. A code is characterized by the number of bit errors in a word that it can correct and detect. The simplest of the error-correcting codes is the Hamming code.

To explain about hamming code let us have a look at the example explained with the help of a venn diagram for 4-bits



Scanned with CamScanner

Lets have a word of 4-bits, the bits of the word are written in the intersections of the three circles as shown above and in the next step we consider each circle and add a even parity check bit, that if the circle has even no of ones we add a zero else we will add a one. Now if there is an error in one of the 4 bits, it is easier to detect which bit has the error by recomputing the parity for each circle and if suppose circle A and circle B has wrong parity that means the bit common for circle A and circle B has the error. The error can be corrected.

Now for a code of K bits to correct a single bit error in word of M bits it should satisfy the criteria of $2^K-1 \geq M + K$

So for a 8 bit word we need to have the value of K =4 to satisfy this criteria.

Thus, eight data bits require four check bits.

The new word has 12 bits where 8 bits is the message and 4 bits are check bits
Let us have bits numbered from 1 to 12 the check bits are present at the positions of power of 2, then the check bits are calculated by the xor operation as follows

C1 = D1 ⊕ D2 ⊕ D4 ⊕ D5 ⊕ D7
C2 = D1 ⊕ D3 ⊕ D4 ⊕ D6 ⊕ D7
C4 = D2 ⊕ D3 ⊕ D4 ⊕ D8
C8 = ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D8

Each check bit operates on every data bit whose position number contains a 1
in the same bit position as the position number of that check bit.
For the input word 00111001 the check bits output will be

C1 = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 = 1
C2 = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 = 1
C4 = 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1
C8 = 1 ⊕ 1 ⊕ 0 ⊕ 0 = 0

Suppose now that data bit 3 sustains an error and is changed from 0 to 1. When the
check bits are recalculated, we have

C1 = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 = 1
C2 = 1 ⊕ 1 ⊕ 1 ⊕ 1 ⊕ 0 = 0
C4 = 0 ⊕ 1 ⊕ 1 ⊕ 0 = 0
C8 = 1 ⊕ 1 ⊕ 0 ⊕ 0 = 0

When the new check bits are compared with the old check bits, the syndrome word
is formed:

```
    C8 C4 C2 C1
    0  1  1  1
⊕ 0  0  0  1
  0  1  1  0
```

The result is 0110, indicating that bit position 6, which contains data bit 3, is in error. The approach used in the example above is called single-error-correcting (SEC) code. More commonly called single-error-correcting-double-error-detecting (SEC-DED) code. SEC-DED are Extended Hamming codes. Extended Hamming codes allow for the distinction between when there were two-bit mistakes and when there were only one or two-bit errors.

5.

Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds. It is possible to erase just blocks of memory rather than an entire chip. Flash memory does not provide byte-level erasure. Flash memory uses only one transistor per bit, and so achieves the high density. An important characteristic of flash memory is that it is persistent memory, which means that it retains data when there is no power applied to the memory. Flash memory uses transistor logic and a second gate called floating gate is added to the transistor. Initially, the floating gate does not interfere with the operation of the transistor, this state represents a binary 1. Applying a large voltage across the oxide layer of floating gate causes electrons to tunnel through it and become trapped on the floating gate, where they remain even if the power is disconnected, and this represents binary 0.

STT-RAM(Spin-Transfer Torque RAM) is a new type of magnetic RAM (MRAM), which features non-volatility, fast writing/reading speed and high programming endurance and zero standby power. The storage capability of MRAM arises from magnetic tunneling junction (MTJ), in which a thin tunneling dielectric is sandwiched between two ferromagnetic layers. One ferromagnetic layer is designed to have its magnetization pinned, while the magnetization of the other layer can be flipped by a write event. An MTJ has a low resistance if the magnetizations of the free layer and the pinned layer are parallel. In STT-RAM, a new write mechanism, called polarization-current-induced magnetization

switching, is introduced. In STT-RAM, the magnetization of the free layer is flipped by the electrical current directly.

Phase-change RAM (PCRAM) technology is based on a chalcogenide alloy material, which is similar to those commonly used in optical storage media. The data storage capability is achieved from the resistance differences between an amorphous (high-resistance) and a crystalline (low-resistance) phase of the chalcogenide-based material. In SET operation, the phase change material is crystallized by applying an electrical pulse that heats a significant portion of the cell above its crystallization temperature. In RESET operation, a larger electrical current is applied and then abruptly cut off in order to melt and then quench the material, leaving it in the amorphous state.

ReRAM (Resistive RAM) works by creating resistance rather than directly storing charge. An electric current is applied to a material, changing the resistance of that material. The resistance state can then be measured and a 1 or 0 is read as the result. ReRAM designs are low voltage, endurance is far superior to flash memory, and the cells are much Smaller. ReRAM is a good candidate to replace or supplement both secondary storage and main memory.