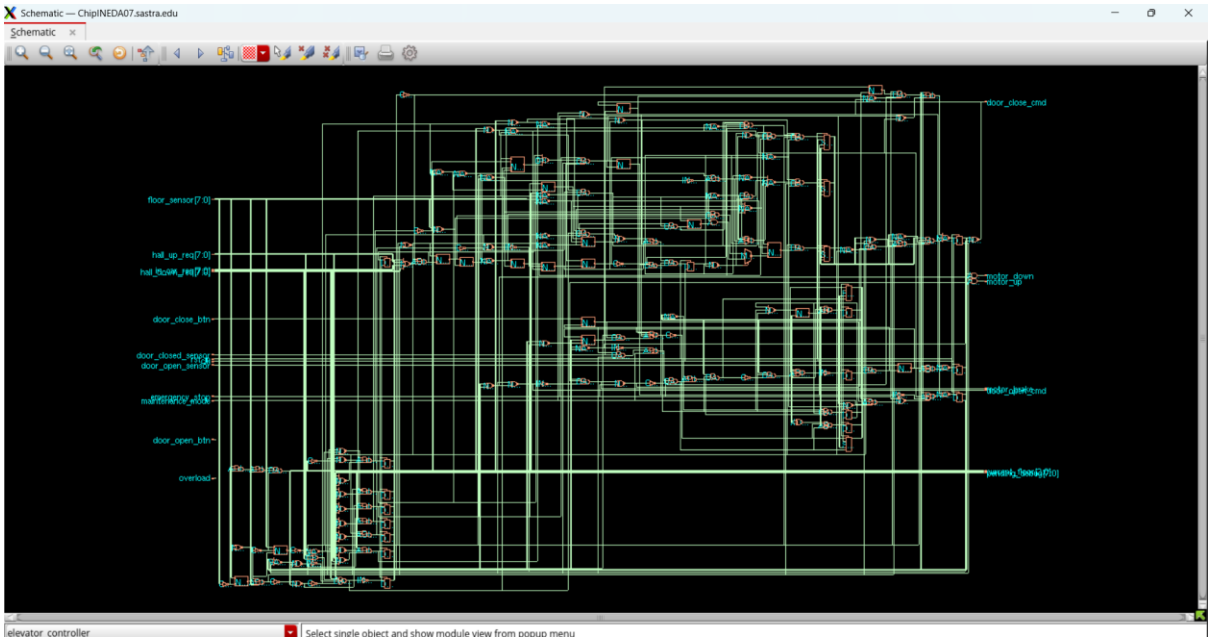
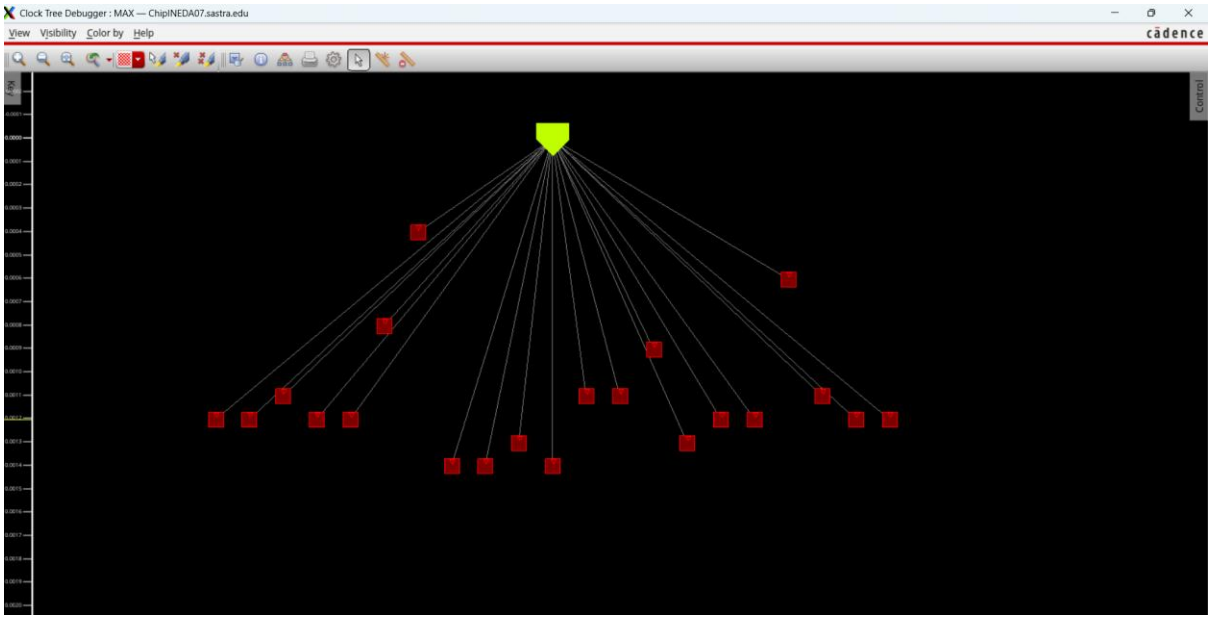
RTL to GDS II


Schematic — ChipINEDA07.sastra.edu
Schematic
floor_sensor[7:0]
hall_up_req[7:0]
door_close_btn
door_open_btn
overload
door_close_cmd
motor_down
motor_up
elevator_controller
Select single object and show module view from popup menu


Innovus(TM) Implementation System 20.14 - /home/cada2601/Elevator/elevator - elevator_controller — ChipINEDA07.sastra.edu
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
cadence
Layout
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
Poly(0)
Cont(0)
Metal1(1)
Via1(1)
Metal2(2)
Adaptive
Detail
Speed
VSS
VDD
select
Instance
Enter Instance name.
Append
coords
radius
Goto
8.71150, 11.28350 Sel: 0 Routed
26°C
Mostly sunny
Search
ENG
IN
10:22
07-01-2026




```
------------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------------

Setup views included:
 WC

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  5.689  |  6.394  |  5.689  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   47    |   31    |   42    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +-----------------+-------------+------------------|
|                |  Nr nets(terms) | Worst Vio   |  Nr nets(terms)  |
+----------------+-----------------+-------------+------------------+
|   max_cap      |      0 (0)      |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)      |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)      |     0       |      0 (0)       |
|   max_length   |      0 (0)      |     0       |      0 (0)       |
+----------------+-----------------+-------------+------------------+

Density: 69.718%
Total number of glitch violations: 0
------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.61 sec
Total Real time: 2.0 sec
Total Memory Usage: 1406.300781 Mbytes
Reset AAE Options
*** timeDesign #1 [finish] : cpu/real = 0:00:00.6/0:00:01.8 (0.3), totSession cpu/real = 0:05:25.6/0:37:55.4 (0.1), mem = 1406.3M
```