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CS M152A: Introductory Digital Design Laboratory

Section 2

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Laboratory 3 Report

Introduction & Background

The purpose of this laboratory assignment was to leverage the knowledge learned from the previous lab assignment about clocks, and apply it in conjunction with our knowledge of finite state machines to create a circuit that could model a parking meter. This parking meter should display the amount of time left on a 4-digit 7 segment display, and count down the seconds left until expiration. It also has inputs to increment the counter by various amounts of time. Depending on how much time is left, the display is also required to flash at various frequencies, which requires us to leverage knowledge we learned regarding clocks in the previous lab.

Another key point to notice is that the way a 7 segment display is set up, only 1 digit can be lit up at a time. We provide the display information about which of the 4 digits we would like to light up, as well as the 7 segment encoding that we would like to display on that digit. Because the human eye is not capable of noticing flickering at frequencies greater than around 50Hz, we can create the illusion of all 4 digits being lit up simultaneously by cycling through each of the digits of the 7 segment display very quickly.

State Diagram

This parking meter can be modeled as a Moore State Machine composed of 3 states. The output is solely affected by the current state of the FSM. Depending on the current state, we can decide what frequency (if any) the counter should be flashed at, and we can also decide whether or not the counter needs to be decremented depending on the current state. There are 3 states necessary to model the parking meter. The first is an initial ZERO state which represents when the counter is 0. The second is a LESSTHAN180 state, which represents when the counter is less than or equal to 180. Finally there is the GREATERTHAN180 state which represents when the counter is greater than 180. The “input” that controls state transitions is the counter variable, which can be influenced by a number of inputs (rst, rst1, rst2, add1-4), but for the sake of simplicity, we'll simply consider only the counter and resets as inputs.

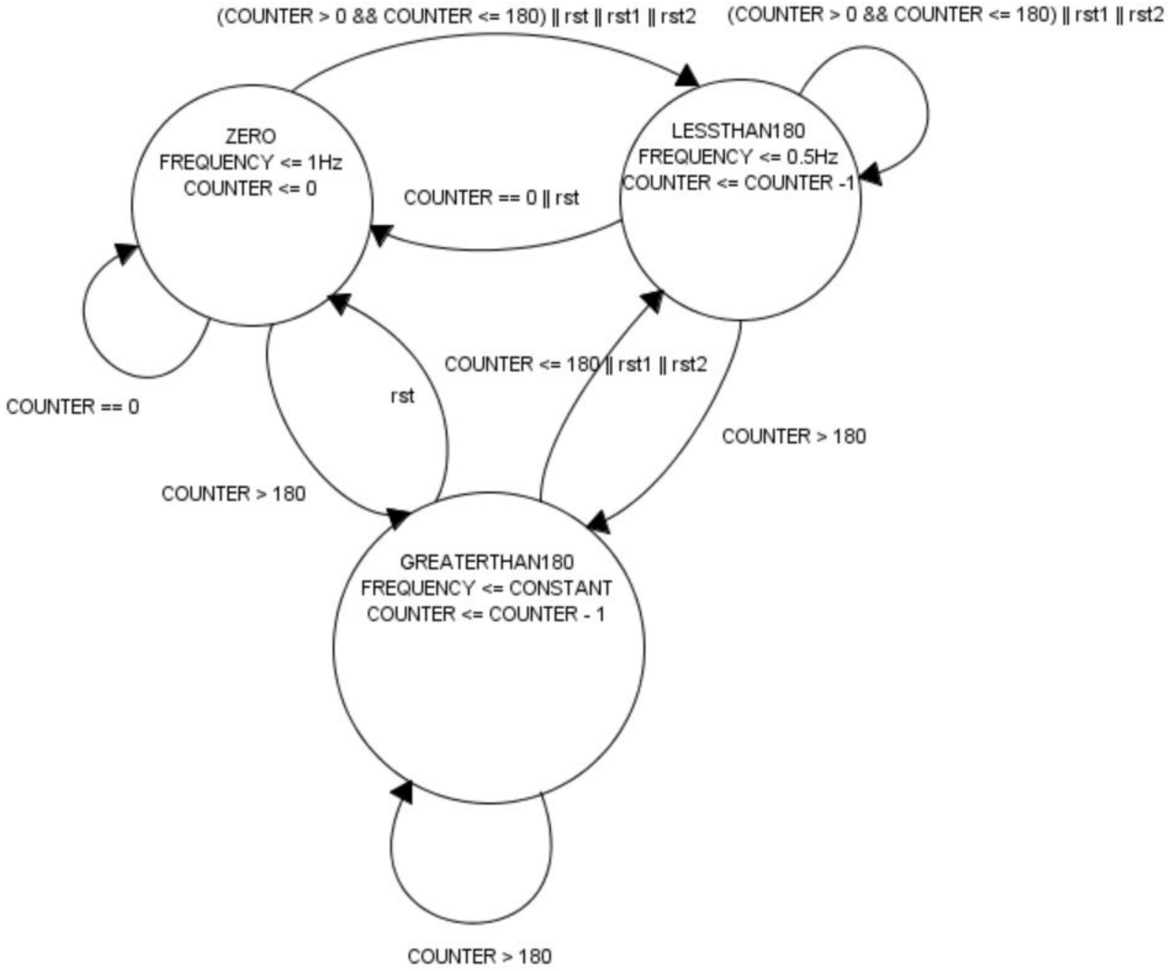


Figure 1: State Diagram for Parking Meter FSM

Design Description

Clocks

There are 3 clocks used by the parking meter module, all based on the 100Hz input clk signal given to us. Their names and purposes are briefly described below.

Name	Frequency	Period	Purpose
OneHzClk	1Hz	1000ms	To ensure the counter is decremented once a

			second, and to flash ‘0000’ in the ZERO state
HalfHzClk	0.5Hz	2000ms	To flash the counter value every other second in the LESSTHAN180 state
DisplayClk	50Hz	20ms	To be used to cycle through the digits of the 7 segment display.

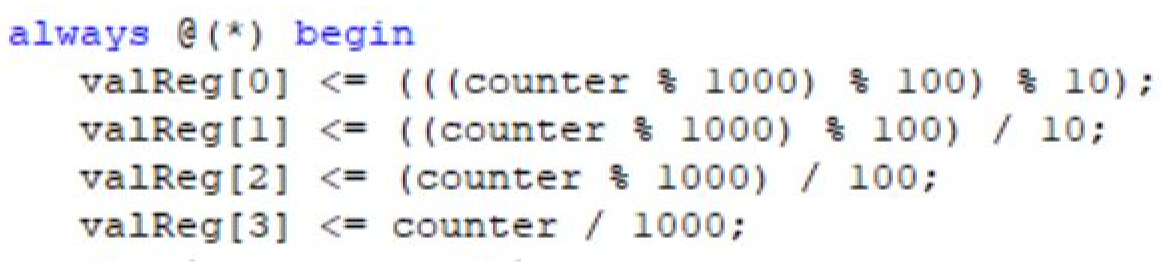
Table 1: Various clocks used within the parking_meter module, and their frequencies, periods, and purposes.

We then have an always block that runs on the posedge of the OneHzClk, which is responsible for handling the counter register that is used to control the output. If any of the add signals are high, the corresponding value will be added to the counter, and otherwise the counter will be decremented every second as long as it has a non-zero value.

Additionally, we also have a 2-bit digitCounter register, which is incremented on the posedge of DisplayClk. This will cause it to constantly cycle through 4 values again and again, perfect for the purposes of cycling through the 4 digits of the 7 segment display.

Val Output Registers

The val0-3 outputs correspond to the digits of the decimal representation of the counter register. Each of the val outputs is assigned to the corresponding index in an array of 4-bit registers. The decimal digit values can be easily extracted from the counter register using a mixture of integer division and the module operation, and then assigned to the corresponding registers as shown below.

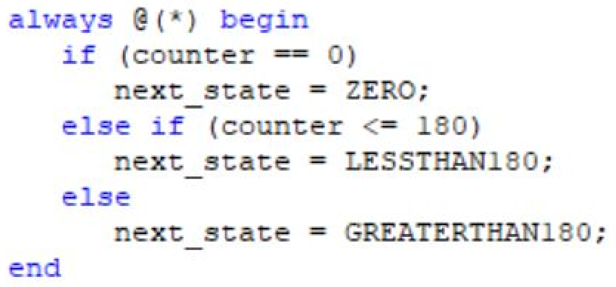


```
always @(*) begin
   valReg[0] <= (((counter % 1000) % 100) % 10);
   valReg[1] <= ((counter % 1000) % 100) / 10;
   valReg[2] <= (counter % 1000) / 100;
   valReg[3] <= counter / 1000;
```

Code 1: Extraction of decimal digits from counter register

State Transitions

The state transition portion is very simple. The next state is solely dependent on the value of the counter, so we simply have an always(*) block that assigns the appropriate value to the next state based on the current value of the countdown counter.



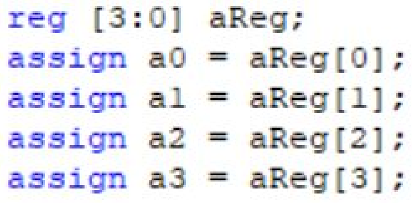
```
always @(*) begin
   if (counter == 0)
      next_state = ZERO;
   else if (counter <= 180)
      next_state = LESSTHAN180;
   else
      next_state = GREATERTHAN180;
end
```

Code 2: State transitions

7 Segment Display

There are 2 components to the 7 segment display. The first is the choice of which of the 4 digits on the display we would like to output to, and the second is the actual 7 bit value that represents which segments we would like to be lit up.

The a0-a3 outputs are assigned to their corresponding bits in a 4-bit register as shown below.

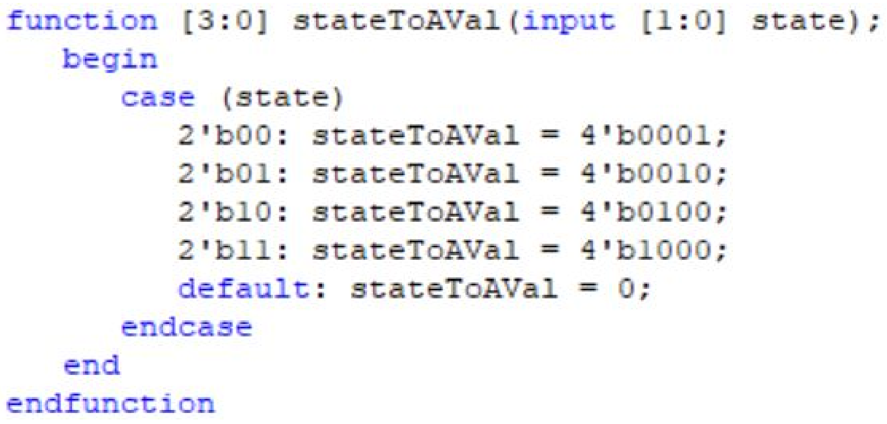


```
reg [3:0] aReg;
assign a0 = aReg[0];
assign a1 = aReg[1];
assign a2 = aReg[2];
assign a3 = aReg[3];
```

Code 3: a0-3 output assignment

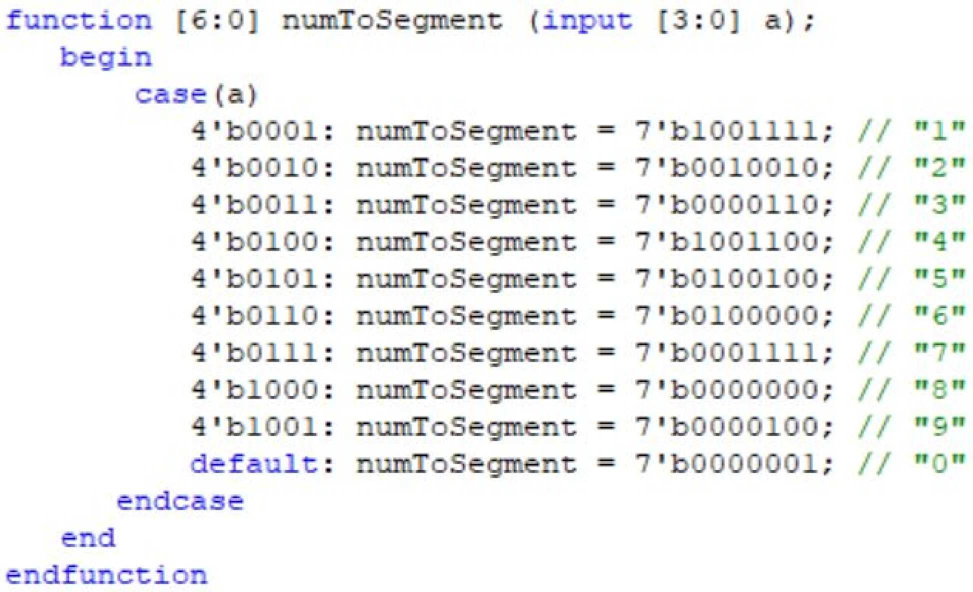
This allows us to simply assign the value 4’b0001 if we would only like the a0 output to be high, leading to cleaner code overall.

In order to display digits, we simply look at the value of digitCounter (a counter incremented at a frequency of 50Hz), and assign aReg an appropriate value to highlight the digit specified by digitCounter. For example, if digitCounter had a value of 2’b10, we would assign aReg a value of 4’b0100, since we’re trying to highlight the 3rd digit. Then we assign the led_seg output the binary sequence needed to display the corresponding digit of the counter. Since we have an array of val registers that have the individual digits of the counter register, we can use the digitCounter as an index to access the corresponding digit of the counter register. We then use this value as input to a function that is simply a case statement that returns the correct 7 bit 7 segment display representation of a digit.



```
function [3:0] stateToAVal(input [1:0] state);
   begin
      case (state)
         2'b00: stateToAVal = 4'b0001;
         2'b01: stateToAVal = 4'b0010;
         2'b10: stateToAVal = 4'b0100;
         2'b11: stateToAVal = 4'b1000;
         default: stateToAVal = 0;
      endcase
   end
endfunction
```

Code 4: Function to convert digitCounter value to a value to highlight the appropriate 'a' output register.



```
function [6:0] numToSegment (input [3:0] a);
   begin
       case(a)
          4'b0001: numToSegment = 7'b1001111; // "1"
          4'b0010: numToSegment = 7'b0010010; // "2"
          4'b0011: numToSegment = 7'b0000110; // "3"
          4'b0100: numToSegment = 7'b1001100; // "4"
          4'b0101: numToSegment = 7'b0100100; // "5"
          4'b0110: numToSegment = 7'b0100000; // "6"
          4'b0111: numToSegment = 7'b0001111; // "7"
          4'b1000: numToSegment = 7'b0000000; // "8"
          4'b1001: numToSegment = 7'b0000100; // "9"
          default: numToSegment = 7'b0000001; // "0"
      endcase
   end
endfunction
```

Code 5: Function to convert a decimal digit into its 7 segment representation. Source ([FPGA Tutorial] Seven-Segment LED Display on Basys 3 FPGA)

The final component of the 7 segment display portion is dependent on state. If in the ZERO state, we only execute the logic that outputs a digit to the display when the OneHzClk is high, and for the LESSTHAN180 state, we only execute it when the HalfHzClk is high. If in the GREATERTHAN180 state, we constantly execute the display output code.

Design Summary

My implementation of this project was able to synthesize correctly. Please refer to the end of this report to see the full Design Summary and Map Report Summary generated by the IDE. The output of both of the reports are rather daunting, as they are filled with terms that seem advanced and rather foreign to me. However, something that does stand out to me is that it appears that there is a rather large percentage of unused resources. I'm not sure what the expected standard is, but this seems to indicate to me that the Verilog code could perhaps be rewritten with optimization of the generated schematic in mind, rather than optimizing the readability of the code itself.

Simulation Documentation

This module was a little tricky to test solely leaving the module as is. As such, for ease of testing, a few extra output registers were added to ease verification of functionality. These include outputs for OneHzClk and HalfHzClk, as well as the state and the counter register value. These additional outputs were removed prior to submission.

For the following examples, note that an output will only be displayed on the seven segment display if the a0-3 registers are being cycled through. 'realClock' has a frequency of 1Hz, and 'halfRealClock' has a frequency of 0.5Hz.

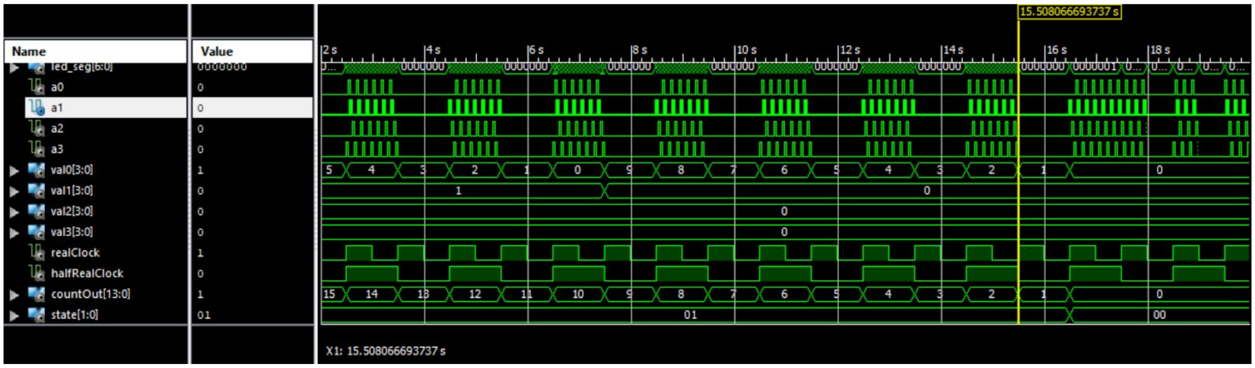


Figure 2: Displays a countdown from 15 (after rst1 was pressed). Note the a0-3 registers are only high on even values of the counter (as specified once counter reaches values < 180), matching the frequency of 'halfRealClock', and that once the counter reaches 0, the a0-3 registers are only high on the posedges of 'realClock', meaning the display is flashing with a frequency of 1Hz.

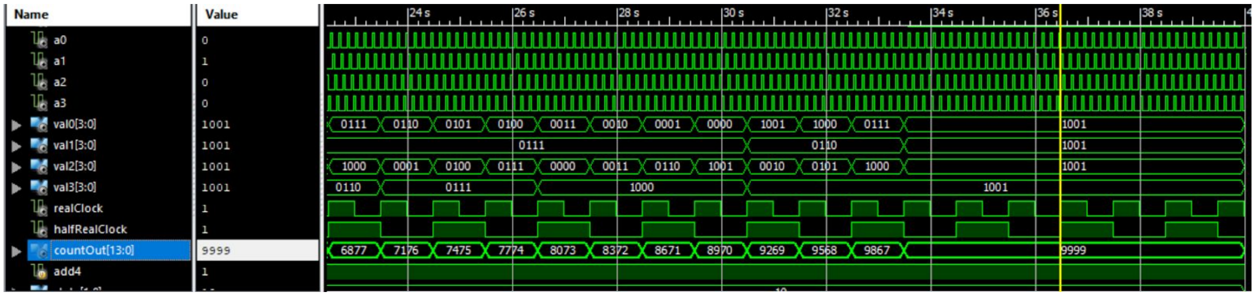


Figure 3: Note that the a0-3 registers are constantly high, as the counter value is greater than 300. Also note that when the add4 input is high when the counter value is 9867 the counter value does not exceed 9999, which is the behavior specified in the spec.

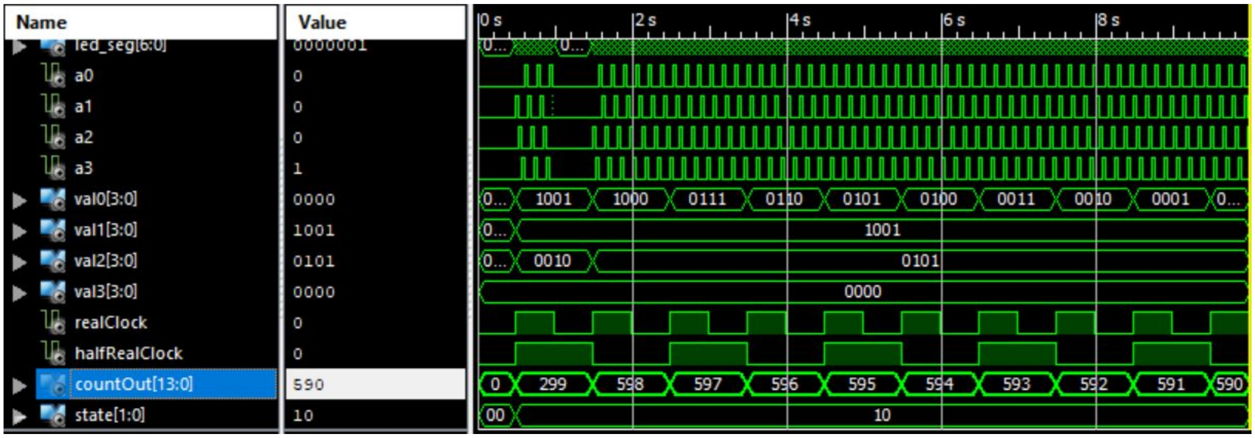


Figure 4: Note that a0-3 registers are constantly high as it counts down from a counter value > 300.

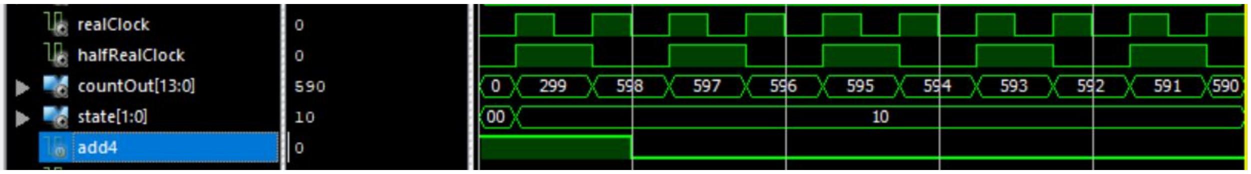


Figure 5: While the add4 register is high, 300 is added immediately on the posedge of 'realClock'.

Conclusion

I was able to successfully implement all of the required features and edge cases of the project specification, and thanks to the structure of the course, I was able to leverage the knowledge learned about clocks in Project 2 to successfully implement this Project. Implementing an FSM in Verilog is fairly intuitive, and when faced with tasks like this, I begin to see the power of Verilog and the always-block centric programmatic paradigm. At this point in time, I do not have any further improvements to suggest for this lab, other than possibly a little further description of the 7 segment display in the spec, since I had to do quite a bit of research to fully understand the concepts behind it.

Map Report Summary

```
Design Summary
--------------
Number of errors:      0
Number of warnings:    4
Slice Logic Utilization:
  Number of Slice Registers:                    35 out of  18,224    1%
    Number used as Flip Flops:                  32
    Number used as Latches:                      3
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                        286 out of   9,112    3%
    Number used as logic:                      282 out of   9,112    3%
      Number using O6 output only:             197
      Number using O5 output only:              27
      Number using O5 and O6:                   58
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   2,176    0%
    Number used exclusively as route-thrus:      4
      Number with same-slice register load:      0
      Number with same-slice carry load:         4
      Number with other load:                    0

Slice Logic Distribution:
  Number of occupied Slices:                   108 out of   2,278    4%
  Number of MUXCYs used:                        80 out of   4,556    1%
  Number of LUT Flip Flop pairs used:          288
    Number with an unused Flip Flop:           255 out of     288   88%
    Number with an unused LUT:                   2 out of     288    1%
    Number of fully used LUT-FF pairs:          31 out of     288   10%
    Number of unique control sets:              16
    Number of slice register sites lost
      to control set restrictions:              93 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        35 out of     232   15%
    IOB Latches:                                11

Specific Feature Utilization:
  Number of RAMB16BWERs:                         0 out of      32    0%
  Number of RAMB8BWERs:                          0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                 0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       2 out of      16   12%
    Number used as BUFGs:                        2
    Number used as BUFGMUX:                      0
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                  11 out of     248    4%
    Number used as OLOGIC2s:                    11
    Number used as OSERDES2s:                    0
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of      32    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of MCBs:                                0 out of       2    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                4.00

Peak Memory Usage:  4520 MB
Total REAL time to MAP completion:  14 secs
Total CPU time to MAP completion:   10 secs
```

Synthesis Design Summary

```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : parking_meter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 487
#      GND                         : 1
#      INV                         : 26
#      LUT1                        : 35
#      LUT2                        : 19
#      LUT3                        : 32
#      LUT4                        : 29
#      LUT5                        : 54
#      LUT6                        : 144
#      MUXCY                       : 65
#      MUXF7                       : 11
#      VCC                         : 1
#      XORCY                       : 70
# FlipFlops/Latches                : 41
#      FDC                         : 2
#      FDCE                        : 20
#      FDR                         : 6
#      FDRE                        : 2
#      LD                          : 11
# Clock Buffers                    : 2
#      BUFG                        : 1
#      BUFGP                       : 1
# IO Buffers                       : 52
#      IBUF                        : 7
#      OBUF                        : 45

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              30  out of  18224     0%
 Number of Slice LUTs:                  339  out of   9112     3%
    Number used as Logic:               339  out of   9112     3%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    343
   Number with an unused Flip Flop:     313  out of    343    91%
   Number with an unused LUT:             4  out of    343     1%
   Number of fully used LUT-FF pairs:    26  out of    343     7%
   Number of unique control sets:         8

IO Utilization:
 Number of IOs:                          53
 Number of bonded IOBs:                  53  out of    232    22%
    IOB Flip Flops/Latches:              11

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                2  out of     16    12%
```

```
---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
----------------------------------------------------------------------------------+-----------
-------------+-------+
Clock Signal                                                                      | Clock
buffer(FF name)  | Load  |
----------------------------------------------------------------------------------+-----------
-------------+-------+
clk                                                                               | BUFGP
| 8     |
OneHzClk                                                                          | BUFG
| 20    |
Mram_current_state[1]_GND_8_o_Mux_69_o(Mram_current_state[1]_GND_8_o_Mux_69_o11:O)|
NONE(*)(a1)            | 11    |
SegmentClk                                                                        |
NONE(SegmentCounter_0) | 2     |
----------------------------------------------------------------------------------+-----------
-------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with
BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to
the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 7.857ns (Maximum Frequency: 127.281MHz)
   Minimum input arrival time before clock: 7.419ns
   Maximum output required time after clock: 38.235ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.853ns (frequency: 350.508MHz)
  Total number of paths / destination ports: 54 / 15
-------------------------------------------------------------------------
Delay:               2.853ns (Levels of Logic = 1)
  Source:            clkCounter_3 (FF)
  Destination:       clkCounter_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: clkCounter_3 to clkCounter_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             5   0.447   1.059  clkCounter_3 (clkCounter_3)
     LUT6:I1->O           5   0.203   0.714  Mcount_clkCounter_val1 (Mcount_clkCounter_val)
     FDR:R                    0.430          clkCounter_0
    ----------------------------------------
    Total                     2.853ns (1.080ns logic, 1.773ns route)
                                       (37.9% logic, 62.1% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'OneHzClk'
  Clock period: 7.857ns (frequency: 127.281MHz)
  Total number of paths / destination ports: 93378 / 38
-------------------------------------------------------------------------
Delay:               7.857ns (Levels of Logic = 26)
  Source:            counter_3 (FF)
  Destination:       counter_13 (FF)
  Source Clock:      OneHzClk rising
  Destination Clock: OneHzClk rising

  Data Path: counter_3 to counter_13
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q           19   0.447   1.071  counter_3 (counter_3)
     INV:I->O             1   0.206   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_lut<3>_INV_0
(Madd_counter[13]_GND_1_o_add_16_OUT_lut<3>)
     MUXCY:S->O           1   0.172   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_cy<3>
(Madd_counter[13]_GND_1_o_add_16_OUT_cy<3>)
     MUXCY:CI->O          1   0.019   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_cy<4>
(Madd_counter[13]_GND_1_o_add_16_OUT_cy<4>)
     MUXCY:CI->O          1   0.019   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_cy<5>
(Madd_counter[13]_GND_1_o_add_16_OUT_cy<5>)
     MUXCY:CI->O          1   0.019   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_cy<6>
(Madd_counter[13]_GND_1_o_add_16_OUT_cy<6>)
     MUXCY:CI->O          1   0.019   0.000  Madd_counter[13]_GND_1_o_add_16_OUT_cy<7>
(Madd_counter[13]_GND_1_o_add_16_OUT_cy<7>)
     XORCY:CI->O          7   0.180   1.002  Madd_counter[13]_GND_1_o_add_16_OUT_xor<8>
(counter[13]_GND_1_o_add_16_OUT<8>)
     LUT3:I0->O           1   0.205   0.684  counter[13]_PWR_1_o_LessThan_18_o22_SW0 (N130)
     LUT6:I4->O           9   0.203   0.934  counter[13]_PWR_1_o_LessThan_18_o23
(counter[13]_PWR_1_o_LessThan_18_o)
     LUT4:I2->O           8   0.203   0.803  Mmux_counter[13]_PWR_1_o_mux_34_OUT_A1221
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_A122)
     LUT5:I4->O           1   0.205   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_lut<0>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_lut<0>)
     MUXCY:S->O           1   0.172   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<0>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<0>)
     MUXCY:CI->O          1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<1>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<1>)
     MUXCY:CI->O          1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<2>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<2>)
```

```
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<3>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<3>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<4>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<4>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<5>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<5>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<6>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<6>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<7>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<7>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<8>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<8>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<9>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<9>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<10>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<10>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<11>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<11>)
     MUXCY:CI->O           0   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<12>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<12>)
     XORCY:CI->O           1   0.180   0.580  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_xor<13>
(counter[13]_PWR_1_o_mux_34_OUT<13>)
     LUT3:I2->O            1   0.205   0.000  Mmux_counter[13]_GND_1_o_mux_37_OUT51
(counter[13]_GND_1_o_mux_37_OUT<13>)
     FDCE:D                    0.102          counter_13
    ----------------------------------------
    Total                      7.857ns (2.784ns logic, 5.073ns route)
                                       (35.4% logic, 64.6% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'SegmentClk'
  Clock period: 2.190ns (frequency: 456.663MHz)
  Total number of paths / destination ports: 3 / 2
-------------------------------------------------------------------------
Delay:               2.190ns (Levels of Logic = 1)
  Source:            SegmentCounter_0 (FF)
  Destination:       SegmentCounter_0 (FF)
  Source Clock:      SegmentClk rising
  Destination Clock: SegmentClk rising

  Data Path: SegmentCounter_0 to SegmentCounter_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             10   0.447   0.856  SegmentCounter_0 (SegmentCounter_0)
     INV:I->O              1   0.206   0.579  Mcount_SegmentCounter_xor<0>11_INV_0
(Result<0>1)
     FDC:D                     0.102          SegmentCounter_0
    ----------------------------------------
    Total                      2.190ns (0.755ns logic, 1.435ns route)
                                       (34.5% logic, 65.5% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 8 / 8
-------------------------------------------------------------------------
Offset:              3.778ns (Levels of Logic = 2)
  Source:            rst (PAD)
  Destination:       clkCounter_0 (FF)
  Destination Clock: clk rising

  Data Path: rst to clkCounter_0
```

```
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            26   1.222   1.207  rst_IBUF (rst_IBUF)
     LUT6:I5->O            5   0.205   0.714  Mcount_clkCounter_val1 (Mcount_clkCounter_val)
     FDR:R                     0.430          clkCounter_0
    ----------------------------------------
    Total                      3.778ns (1.857ns logic, 1.921ns route)
                                       (49.2% logic, 50.8% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'OneHzClk'
  Total number of paths / destination ports: 2079 / 58
-------------------------------------------------------------------------
Offset:              7.419ns (Levels of Logic = 14)
  Source:            add2 (PAD)
  Destination:       counter_13 (FF)
  Destination Clock: OneHzClk rising

  Data Path: add2 to counter_13
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            56   1.222   1.692  add2_IBUF (add2_IBUF)
     LUT2:I0->O            2   0.203   0.845  counter[13]_PWR_1_o_LessThan_21_o22_SW2_SW0
(N262)
     LUT6:I3->O            1   0.205   0.808  Mmux_counter[13]_PWR_1_o_mux_34_OUT_A1811_SW9
(N227)
     LUT6:I3->O            1   0.205   0.684
Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_lut<6>_SW0 (N208)
     LUT6:I4->O            1   0.203   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_lut<6>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_lut<6>)
     MUXCY:S->O            1   0.172   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<6>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<6>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<7>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<7>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<8>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<8>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<9>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<9>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<10>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<10>)
     MUXCY:CI->O           1   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<11>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<11>)
     MUXCY:CI->O           0   0.019   0.000  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<12>
(Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_cy<12>)
     XORCY:CI->O           1   0.180   0.580  Mmux_counter[13]_PWR_1_o_mux_34_OUT_rs_xor<13>
(counter[13]_PWR_1_o_mux_34_OUT<13>)
     LUT3:I2->O            1   0.205   0.000  Mmux_counter[13]_GND_1_o_mux_37_OUT51
(counter[13]_GND_1_o_mux_37_OUT<13>)
     FDCE:D                    0.102          counter_13
    ----------------------------------------
    Total                      7.419ns (2.811ns logic, 4.608ns route)
                                       (37.9% logic, 62.1% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'SegmentClk'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              2.858ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       SegmentCounter_0 (FF)
  Destination Clock: SegmentClk rising

  Data Path: rst to SegmentCounter_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            26   1.222   1.206  rst_IBUF (rst_IBUF)
     FDC:CLR                   0.430          SegmentCounter_0
    ----------------------------------------
    Total                      2.858ns (1.652ns logic, 1.206ns route)
                                       (57.8% logic, 42.2% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Mram_current_state[1]_GND_8_o_Mux_69_o'
  Total number of paths / destination ports: 11 / 11
-------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            sevenSeg_6 (LATCH)
  Destination:       led_seg<6> (PAD)
  Source Clock:      Mram_current_state[1]_GND_8_o_Mux_69_o falling

  Data Path: sevenSeg_6 to led_seg<6>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.498   0.579  sevenSeg_6 (sevenSeg_6)
     OBUF:I->O                 2.571          led_seg_6_OBUF (led_seg<6>)
    ----------------------------------------
    Total                      3.648ns (3.069ns logic, 0.579ns route)
                                       (84.1% logic, 15.9% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'OneHzClk'
  Total number of paths / destination ports: 15603555943 / 32
-------------------------------------------------------------------------
Offset:              38.235ns (Levels of Logic = 31)
  Source:            counter_8 (FF)
  Destination:       val0<3> (PAD)
  Source Clock:      OneHzClk rising

  Data Path: counter_8 to val0<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q            19   0.447   1.176  counter_8 (counter_8)
     LUT2:I0->O            1   0.203   0.580  counter[13]_PWR_1_o_div_53/o<4>1_SW0 (N86)
     LUT6:I5->O           14   0.205   1.302  counter[13]_PWR_1_o_div_53/o<4>1
(counter[13]_PWR_1_o_div_53/o<4>)
     LUT6:I1->O            4   0.203   1.048
counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_23_OUT[13:0]_lut<11>1
(counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_23_OUT[13:0]_lut<11>)
     LUT6:I0->O           15   0.203   1.086  val3<3>1 (val3_3_OBUF)
     LUT5:I3->O            8   0.203   1.147  counter[13]_PWR_1_o_div_53/Mmux_n0701131
(counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_25_OUT[13:0]_lut<8>)
     LUT6:I1->O            6   0.203   0.849
counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<10>2
(counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<10>2)
     LUT5:I3->O           13   0.203   0.933  val3<2>1 (val3_2_OBUF)
     LUT6:I5->O            8   0.205   1.031
counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<8>11
(counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<8>1)
```

```
     LUT6:I3->O            3   0.205   0.879
counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<10>1
(counter[13]_PWR_1_o_div_53/Madd_a[13]_GND_7_o_add_27_OUT[13:0]_lut<10>)
     LUT6:I3->O           17   0.205   1.256  val3<1>13 (val3_1_OBUF)
     LUT6:I3->O            5   0.205   0.715
counter[13]_PWR_1_o_mod_45/Mmux_a[0]_a[13]_MUX_487_o161
(counter[13]_PWR_1_o_mod_45/Madd_a[13]_GND_2_o_add_29_OUT_Madd_lut<6>)
     LUT6:I5->O            6   0.205   0.992  counter[13]_PWR_1_o_mod_45/BUS_0015_INV_287_o131
(counter[13]_PWR_1_o_mod_45/BUS_0015_INV_287_o13)
     LUT5:I1->O           13   0.203   1.180  counter[13]_PWR_1_o_mod_45/BUS_0015_INV_287_o13
(counter[13]_PWR_1_o_mod_45/BUS_0015_INV_287_o)
     LUT5:I1->O            3   0.203   1.015
counter[13]_PWR_1_o_div_52/Madd_a[9]_GND_6_o_add_17_OUT[9:0]_lut<8>11
(counter[13]_PWR_1_o_div_52/Madd_a[9]_GND_6_o_add_17_OUT[9:0]_lut<8>1)
     LUT6:I0->O            7   0.203   1.138  val2<3>1 (val2_3_OBUF)
     LUT6:I0->O            6   0.203   0.745  counter[13]_PWR_1_o_div_52/Mmux_n0403911
(counter[13]_PWR_1_o_div_52/Mmux_n040391)
     LUT4:I3->O           13   0.205   1.161  val2<2>1 (val2_2_OBUF)
     LUT4:I1->O            1   0.205   0.684  val2<1>_SW0 (N92)
     LUT5:I3->O            7   0.203   1.118  val2<1> (val2<1>1)
     LUT5:I0->O            7   0.203   1.002  counter[13]_PWR_1_o_mod_46/BUS_0010_INV_429_o11
(val2_1_OBUF)
     LUT6:I3->O            8   0.205   1.167
counter[13]_PWR_1_o_mod_46/Mmux_a[0]_a[9]_MUX_675_o151
(counter[13]_PWR_1_o_mod_46/Madd_a[9]_GND_3_o_add_21_OUT_Madd_lut<5>)
     LUT6:I0->O           10   0.203   1.201  counter[13]_PWR_1_o_mod_46/BUS_0011_INV_440_o1
(counter[13]_PWR_1_o_mod_46/BUS_0011_INV_440_o)
     LUT6:I1->O            2   0.203   0.721
counter[13]_PWR_1_o_div_50/Madd_a[6]_GND_5_o_add_11_OUT[6:0]_cy<5>3
(counter[13]_PWR_1_o_div_50/Madd_a[6]_GND_5_o_add_11_OUT[6:0]_cy<5>3)
     LUT3:I1->O            1   0.203   0.580
counter[13]_PWR_1_o_div_50/Madd_a[6]_GND_5_o_add_11_OUT[6:0]_cy<5>4
(counter[13]_PWR_1_o_div_50/Madd_a[6]_GND_5_o_add_11_OUT[6:0]_cy<5>)
     LUT6:I5->O            5   0.205   0.943  val1<2> (val1_2_OBUF)
     LUT6:I3->O            3   0.205   1.015
counter[13]_PWR_1_o_mod_47/Mmux_a[0]_a[6]_MUX_761_o141
(counter[13]_PWR_1_o_mod_47/Madd_a[6]_GND_4_o_add_13_OUT_lut<4>)
     LUT6:I0->O            6   0.203   0.992  val1<1>1 (val1_1_OBUF)
     LUT6:I2->O            1   0.203   0.000  counter[13]_PWR_1_o_mod_47/BUS_0008_INV_517_o4_G
(N303)
     MUXF7:I1->O           3   0.140   0.898  counter[13]_PWR_1_o_mod_47/BUS_0008_INV_517_o4
(counter[13]_PWR_1_o_mod_47/BUS_0008_INV_517_o)
     LUT6:I2->O            2   0.203   0.616  counter[13]_PWR_1_o_mod_47/Mmux_o41
(val0_3_OBUF)
     OBUF:I->O                 2.571          val0_3_OBUF (val0<3>)
    ----------------------------------------
    Total                     38.235ns (9.067ns logic, 29.168ns route)
                                       (23.7% logic, 76.3% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              3.820ns (Levels of Logic = 1)
  Source:            OneHzClk (FF)
  Destination:       realClock (PAD)
  Source Clock:      clk rising

  Data Path: OneHzClk to realClock
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```

```
     FDRE:C->Q             8   0.447   0.802  OneHzClk (OneHzClk)
     OBUF:I->O                 2.571          realClock_OBUF (realClock)
    ----------------------------------------
    Total                      3.820ns (3.018ns logic, 0.802ns route)
                                       (79.0% logic, 21.0% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock Mram_current_state[1]_GND_8_o_Mux_69_o
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
OneHzClk       |         |         |   37.233|         |
SegmentClk     |         |         |    3.132|         |
clk            |         |         |    2.885|         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock OneHzClk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
OneHzClk       |    7.857|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock SegmentClk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
SegmentClk     |    2.190|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.853|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 16.45 secs

-->

Total memory usage is 4510320 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   17 (   0 filtered)
Number of infos    :    4 (   0 filtered)
```