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CS M152A: Introductory Digital Design Laboratory

Section 2

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Laboratory 4 Report

Introduction & Background

The purpose of this laboratory assignment was to use our knowledge of clock cycles and basic Finite State Machine (FSM) implementation in Verilog to implement a more complex FSM, with more states and specified behaviors. The FSM described in the project requirements models a vending machine, with stocking, vending, and transaction validation functionalities. The vending machine sells 20 different snacks, each with 2-digit item codes ranging from 00 to 19. The vending machine can store up to 10 of each snack, and a buyer can purchase only one snack at a time using card payments only.

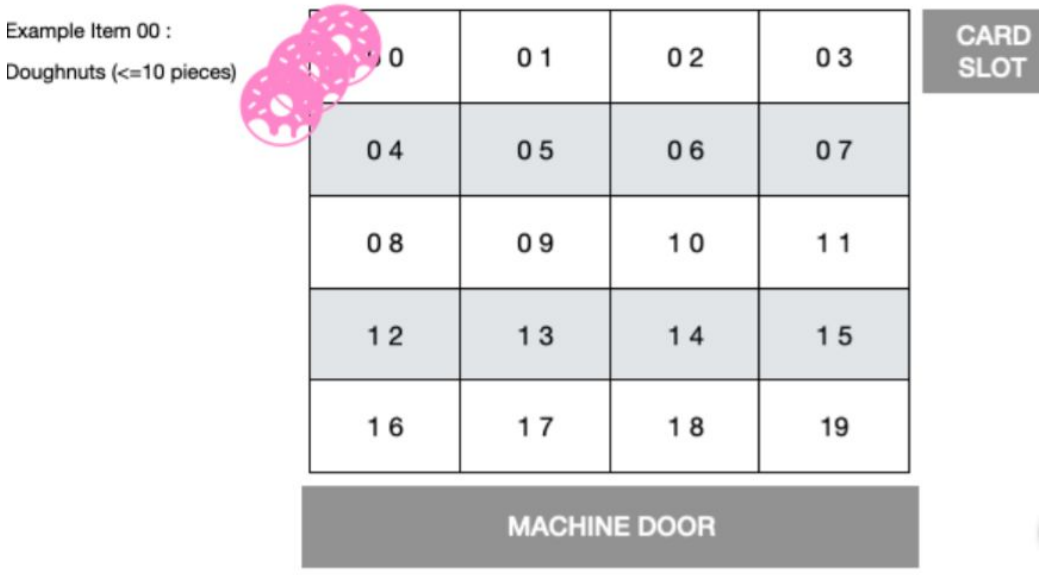


Figure 1: Vending Machine Diagram from Project Specification

Design Documentation

The FSM implementation I ultimately chose was a Moore machine of about 8 states based on the following inputs and outputs:

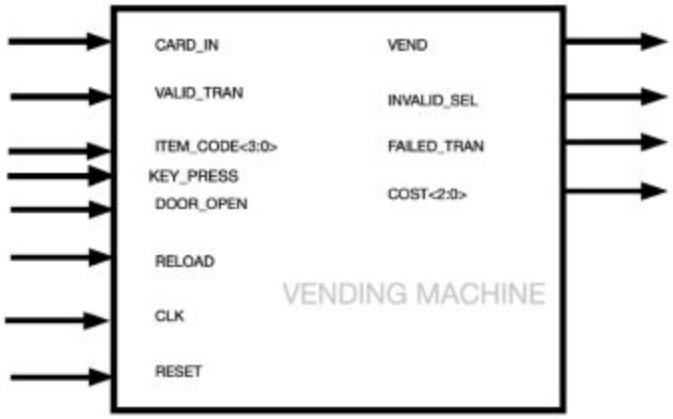


Figure 2: Vending Machine I/O from Project Specification

I will outline each state and its purpose. The transitions between states will be relatively clear based on their purpose. The RESET signal will cause the FSM to return to IDLE regardless of its current state or input.

IDLE
The IDLE state acts as the vending machine's root reset state with all the output signals being low, and the item display price being 0. If reload signal is received in IDLE state, restock all the snacks. If CARD_IN signal is received in the IDLE state, go to AWAIT_FIRST_DIGIT

AWAIT_FIRST_DIGIT
Waits for 5 cycles for the first digit of the item code. If timeout, go back to IDLE state. If a digit is entered, go to AWAIT_SECOND_DIGIT.

AWAIT_SECOND_DIGIT
Waits for 5 cycles for the second digit of the item code. If timeout, go back to IDLE state. If a second digit is entered:

- If the full item code is valid, go to AWAIT_VALIDATION
- If the full item code is invalid, go to INVALID_INPUT

AWAIT_VALIDATION
Display item price and wait 5 cycles for transaction validation. If timeout, go to FAILED_TRAN state. If validated in time, go to VEND state.

INVALID_INPUT
Set INVALID_SEL to high for 1 cycle, then return to IDLE state.

VEND - VEND
Set VEND to high, continue to display item price. Wait 5 cycles for the door to open. If timeout, return to IDLE state. If door opens in time, go to OPEN_DOOR state.

FAILED_TRAN
Set FAILED_TRAN to high for 1 cycle, continue to display item price. Then return to IDLE.

OPEN_DOOR
VEND should remain high, and continue to display item price. Once door closes, return to IDLE state.

The implementation of the FSM in Verilog is fairly straightforward. To handle states, I initialized unique 4-bit parameters to represent each state, and then I also created current_state and next_state registers, similar to the implementation of state mechanisms in Project 3. I created a counter register to be used for timeout tracking in the states with timeout resets. I also created an array of 20 4-bit registers to store the inventory count of each snack. Since item codes range from 0 to 19, they can be used as indices in the register array, and the array becomes a hashmap of item code to inventory count, which greatly cleans up the code.

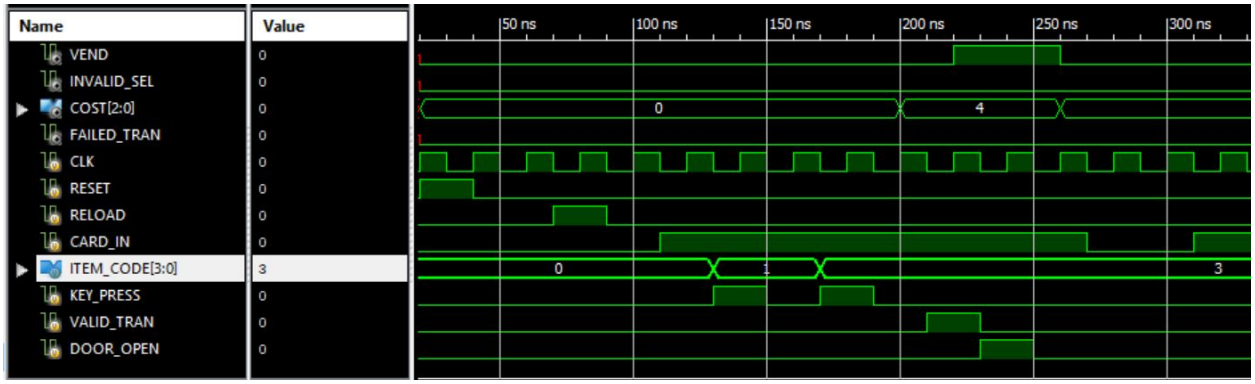
As suggested by the project specification, my implementation uses 3 always blocks for the main logic, with 2 additional blocks for timeout tracking. The first is a sequential block triggered by the positive clock edge which is responsible for updating state. The next is a combinational block triggered by state/input that decides the next state. The final block is another combinational block that decides output values based on current state and other stateful values such as the inventory count.

Simulation Documentation

My testbench runs through 5 basic test cases to check the functionality of the vending machine. I simulate a clock by waiting 10ns and then flipping the clock signal. By sequentially changing input values, I was able to run through various scenarios.

Successful purchase of valid in-stock item

First we set the RESET and RELOAD input signals to reset and restock all the inventory in the vending machine. Then CARD_IN goes high, followed by pressing ‘1’ and ‘7’ for the item code. Since this item code is valid, we display the COST, $4, and then provide the VALID_TRAN signal, after which VEND goes high and stays high until the DOOR_OPEN signal goes high and is then set back to low.

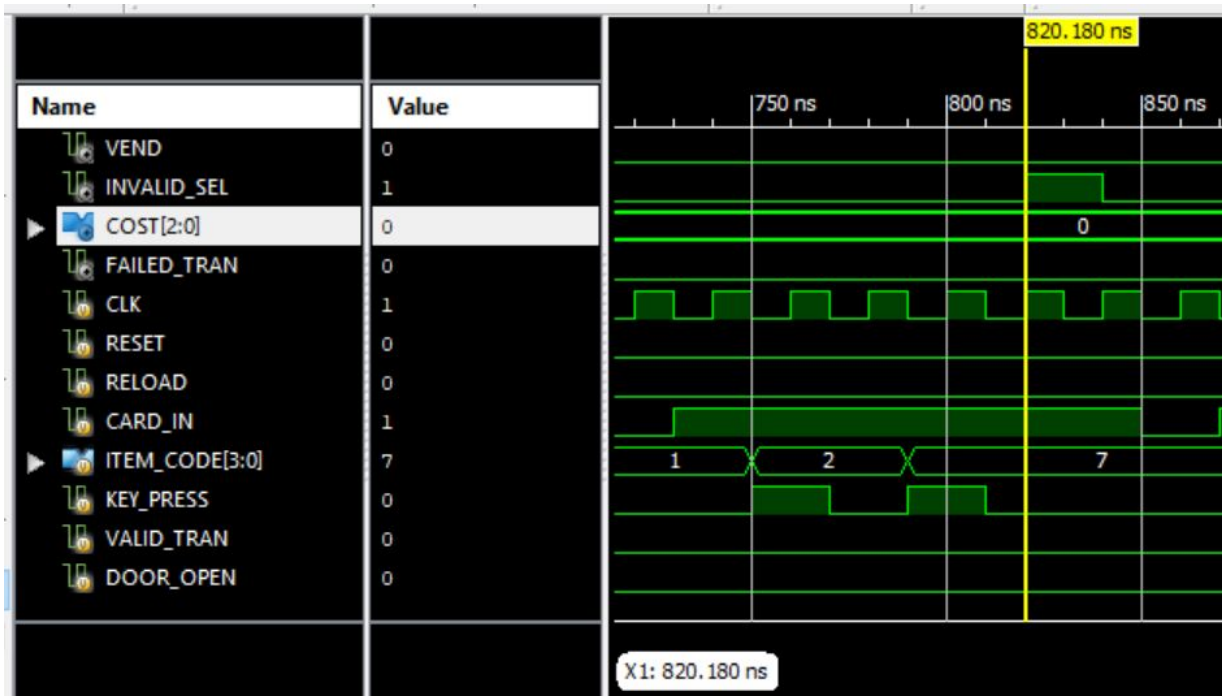


Unsuccessful purchase due to lack of key press

Here we see the CARD_IN signal go high, and on the fifth cycle after CARD_IN went high, we have not received any digit input since KEY_PRESS hasn’t gone high. On the fifth cycle, INVALID_SEL goes high and then goes low on the next cycle.

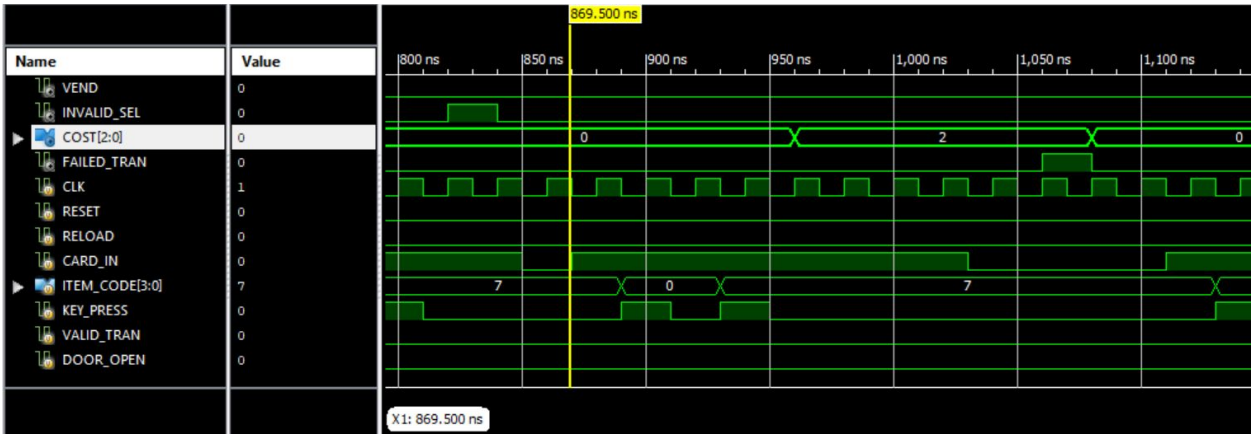
Invalid item number

Here, we insert the card, and then enter the item code ‘27’. Since this is not a valid item code, on the next clock cycle, we set INVALID_SEL high for one cycle, and then reset to the IDLE state.



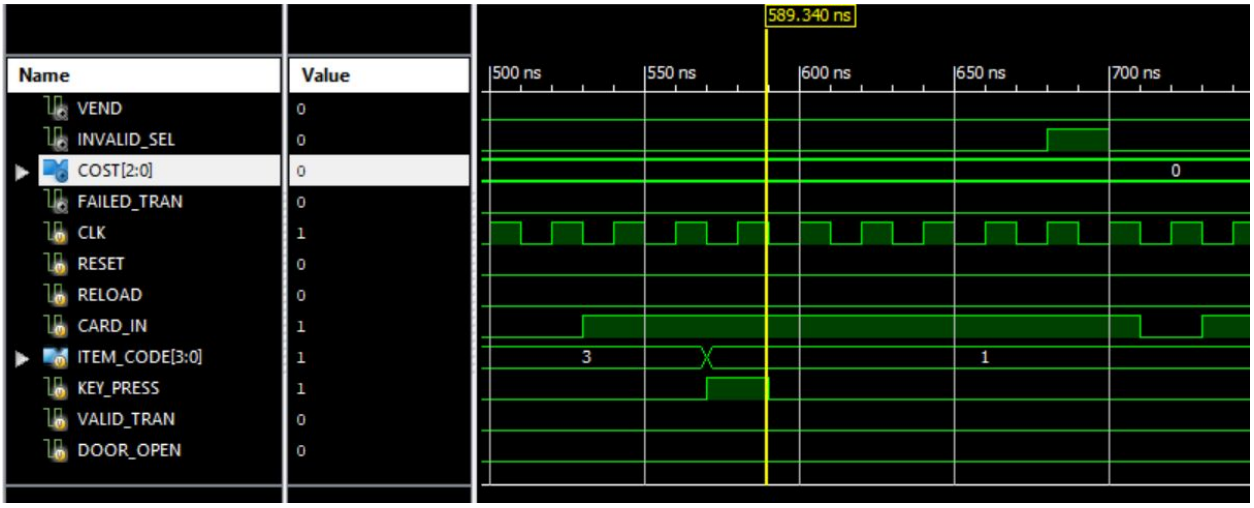
Transaction was not validated

Here, we insert the card and enter the valid item code ‘07’. On the next cycle, the price $2 is outputted to COST. However, after waiting for 5 cycles after the second digit was pressed, we did not receive a VALID_TRAN signal, so we set the FAILED_TRAN signal to high for one cycle, after which we return to the IDLE state and reset the COST output to 0.



Unsuccessful purchase due to missing second digit of item code

Here, we insert the card, press the first digit, and then on the 5th cycle after the first key was pressed, we set INVALID_SEL to high for 1 cycle, since we didn't receive a second digit, and the vending machine goes back to its initial IDLE stage. Note that the COST display remained at 0 since no second digit was provided.



Synthesis and Implementation Report

Both the Synthesis and Implementation reports have been included at the end of the report. The Design Summary reveals a substantial number of flip-flops, but this is to expected in a stateful machine. What is most striking is the large number of multiplexers, but this can likely be explained by the 20 item selections options. Although my implementation addresses different item selections very simply in Verilog code through the use of a hashmap, when synthesized, this still needs to be expanded and implemented with multiplexers.

Conclusion

After having completed the previous parking meter assignment, the implementation of the Vending Machine FSM was relatively straightforward in spite of the added complexity. By far the most helpful part in the process was first visualizing the FSM with a diagram first. Doing this not only made state transitions clear, but also made clear which logic parts could be potentially shared between states, such as the timeout counter. I have no further recommendations to improve this project.

Synthesis Report

```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : vending_machine.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 227
#      GND                         : 1
#      INV                         : 1
#      LUT1                        : 2
#      LUT2                        : 9
#      LUT3                        : 9
#      LUT4                        : 23
#      LUT5                        : 84
#      LUT6                        : 84
#      MUXCY                       : 4
#      MUXF7                       : 6
#      XORCY                       : 4
# FlipFlops/Latches                : 108
#      FD                          : 1
#      FDE                         : 84
#      FDR                         : 2
#      FDRE                        : 3
#      FDS                         : 3
#      LD                          : 15
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 16
#      IBUF                        : 10
#      OBUF                        : 6

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:             102  out of  18224     0%
 Number of Slice LUTs:                  212  out of   9112     2%
    Number used as Logic:               212  out of   9112     2%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    217
   Number with an unused Flip Flop:     115  out of    217    52%
   Number with an unused LUT:             5  out of    217     2%
   Number of fully used LUT-FF pairs:    97  out of    217    44%
   Number of unique control sets:        11

IO Utilization:
 Number of IOs:                          17
```

```
 Number of bonded IOBs:                  17  out of    232     7%
    IOB Flip Flops/Latches:               6

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
----------------------------------------------------------------------------------------------
+------------------------+-------+
Clock Signal
| Clock buffer(FF name)  | Load  |
----------------------------------------------------------------------------------------------
+------------------------+-------+
_n0491(_n04911:O)
| NONE(*)(INVALID_SEL)   | 1     |
_n0507(_n05071:O)
| NONE(*)(FAILED_TRAN)   | 1     |
_n0506(_n05061:O)
| NONE(*)(VEND)          | 1     |
current_state[3]_GND_7_o_Mux_99_o(Mmux_current_state[3]_GND_7_o_Mux_99_o11:O)
| NONE(*)(code1_3)       | 4     |
current_state[3]_GND_3_o_Mux_91_o(Mmux_current_state[3]_GND_3_o_Mux_91_o11:O)
| NONE(*)(code2_3)       | 4     |
current_state[3]_GND_11_o_Mux_107_o(Mmux_current_state[3]_GND_11_o_Mux_107_o11:O)
| NONE(*)(code1inputted) | 1     |
current_state[3]_PWR_15_o_Select_160_o(Mmux_current_state[3]_PWR_15_o_Select_160_o1:O)
| NONE(*)(COST_1)        | 3     |
CLK
| BUFGP                  | 93    |
----------------------------------------------------------------------------------------------
+------------------------+-------+
(*) These 7 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by
XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert
these buffers to the clock signals to help prevent skew problems.
```

```
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.590ns (Maximum Frequency: 178.892MHz)
   Minimum input arrival time before clock: 5.310ns
   Maximum output required time after clock: 3.648ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'CLK'
  Clock period: 5.590ns (frequency: 178.892MHz)
  Total number of paths / destination ports: 5905 / 183
-------------------------------------------------------------------------
Delay:               5.590ns (Levels of Logic = 5)
  Source:            selections_0_40 (FF)
  Destination:       selections_0_2 (FF)
  Source Clock:      CLK rising
  Destination Clock: CLK rising

  Data Path: selections_0_40 to selections_0_2
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q              2   0.447   0.864  selections_0_40 (selections_0_40)
     LUT6:I2->O            1   0.203   0.827  mux_91 (mux_91)
     LUT6:I2->O            1   0.203   0.000  mux_4 (mux_4)
     MUXF7:I0->O          48   0.131   1.520  mux_2_f7
(Msub_GND_1_o_GND_1_o_sub_21_OUT_cy<0>)
     LUT5:I4->O           11   0.205   0.883
Mmux_selections[20][3]_selections[20][3]_mux_48_OUT1011
(Mmux_selections[20][3]_selections[20][3]_mux_48_OUT101)
     LUT5:I4->O            1   0.205   0.000
Mmux_selections[20][3]_selections[20][3]_mux_48_OUT102
(selections[20][3]_selections[20][3]_mux_48_OUT<18>)
     FDE:D                     0.102          selections_0_18
    ----------------------------------------
    Total                      5.590ns (1.496ns logic, 4.094ns route)
                                       (26.8% logic, 73.2% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'current_state[3]_GND_7_o_Mux_99_o'
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------------
Offset:              1.875ns (Levels of Logic = 1)
```

```
  Source:            ITEM_CODE<3> (PAD)
  Destination:       code1_3 (LATCH)
  Destination Clock: current_state[3]_GND_7_o_Mux_99_o falling

  Data Path: ITEM_CODE<3> to code1_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.222   0.616  ITEM_CODE_3_IBUF (ITEM_CODE_3_IBUF)
     LD:D                      0.037          code1_3
    ----------------------------------------
    Total                      1.875ns (1.259ns logic, 0.616ns route)
                                       (67.1% logic, 32.9% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'current_state[3]_GND_3_o_Mux_91_o'
  Total number of paths / destination ports: 8 / 4
--------------------------------------------------------------------------
Offset:              2.625ns (Levels of Logic = 2)
  Source:            KEY_PRESS (PAD)
  Destination:       code2_3 (LATCH)
  Destination Clock: current_state[3]_GND_3_o_Mux_91_o falling

  Data Path: KEY_PRESS to code2_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            13   1.222   1.161  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT4:I1->O            1   0.205   0.000
Mmux_current_state[3]_code2[2]_Mux_92_o11 (current_state[3]_code2[2]_Mux_92_o)
     LD:D                      0.037          code2_2
    ----------------------------------------
    Total                      2.625ns (1.464ns logic, 1.161ns route)
                                       (55.8% logic, 44.2% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'current_state[3]_PWR_15_o_Select_160_o'
  Total number of paths / destination ports: 3 / 3
--------------------------------------------------------------------------
Offset:              3.461ns (Levels of Logic = 3)
  Source:            RELOAD (PAD)
  Destination:       COST_1 (LATCH)
  Destination Clock: current_state[3]_PWR_15_o_Select_160_o falling

  Data Path: RELOAD to COST_1
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   1.222   0.715  RELOAD_IBUF (RELOAD_IBUF)
     LUT5:I4->O            5   0.205   1.079  _n04911 (_n0491)
     LUT6:I0->O            1   0.203   0.000
Mmux_current_state[3]_GND_1_o_Select_159_o11 (current_state[3]_GND_1_o_Select_159_o)
     LD:D                      0.037          COST_2
```

```
    ----------------------------------------
    Total                      3.461ns (1.667ns logic, 1.794ns route)
                                       (48.2% logic, 51.8% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK'
  Total number of paths / destination ports: 51 / 13
--------------------------------------------------------------------------
Offset:              5.310ns (Levels of Logic = 5)
  Source:            KEY_PRESS (PAD)
  Destination:       current_state_FSM_FFd3 (FF)
  Destination Clock: CLK rising

  Data Path: KEY_PRESS to current_state_FSM_FFd3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            13   1.222   1.161  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT4:I1->O            1   0.205   0.580  current_state_FSM_FFd3-In2
(current_state_FSM_FFd3-In2)
     LUT6:I5->O            2   0.205   0.617  current_state_FSM_FFd3-In3
(current_state_FSM_FFd3-In3)
     LUT4:I3->O            1   0.205   0.808  _n0459<3>1_SW0 (N10)
     LUT6:I3->O            2   0.205   0.000  current_state_FSM_FFd3-In6
(current_state_FSM_FFd3-In)
     FDS:D                     0.102          current_state_FSM_FFd3
    ----------------------------------------
    Total                      5.310ns (2.144ns logic, 3.166ns route)
                                       (40.4% logic, 59.6% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock
'current_state[3]_PWR_15_o_Select_160_o'
  Total number of paths / destination ports: 3 / 3
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            COST_2 (LATCH)
  Destination:       COST<2> (PAD)
  Source Clock:      current_state[3]_PWR_15_o_Select_160_o falling

  Data Path: COST_2 to COST<2>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.498   0.579  COST_2 (COST_2)
     OBUF:I->O                 2.571          COST_2_OBUF (COST<2>)
    ----------------------------------------
    Total                      3.648ns (3.069ns logic, 0.579ns route)
                                       (84.1% logic, 15.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock '_n0506'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
```

```
  Source:            VEND (LATCH)
  Destination:       VEND (PAD)
  Source Clock:      _n0506 falling

  Data Path: VEND to VEND
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.498   0.579  VEND (VEND_OBUF)
     OBUF:I->O                 2.571          VEND_OBUF (VEND)
    ----------------------------------------
    Total                      3.648ns (3.069ns logic, 0.579ns route)
                                       (84.1% logic, 15.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock '_n0491'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            INVALID_SEL (LATCH)
  Destination:       INVALID_SEL (PAD)
  Source Clock:      _n0491 falling

  Data Path: INVALID_SEL to INVALID_SEL
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.498   0.579  INVALID_SEL (INVALID_SEL_OBUF)
     OBUF:I->O                 2.571          INVALID_SEL_OBUF (INVALID_SEL)
    ----------------------------------------
    Total                      3.648ns (3.069ns logic, 0.579ns route)
                                       (84.1% logic, 15.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock '_n0507'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            FAILED_TRAN (LATCH)
  Destination:       FAILED_TRAN (PAD)
  Source Clock:      _n0507 falling

  Data Path: FAILED_TRAN to FAILED_TRAN
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.498   0.579  FAILED_TRAN (FAILED_TRAN_OBUF)
     OBUF:I->O                 2.571          FAILED_TRAN_OBUF (FAILED_TRAN)
    ----------------------------------------
    Total                      3.648ns (3.069ns logic, 0.579ns route)
                                       (84.1% logic, 15.9% route)

==========================================================================

Cross Clock Domains Report:
```

Clock to Setup on destination clock CLK

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK	5.590			
current_state[3]_GND_11_o_Mux_107_o		4.553		
current_state[3]_GND_3_o_Mux_91_o		9.207		
current_state[3]_GND_7_o_Mux_99_o		9.424		

Clock to Setup on destination clock _n0491

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			2.184	

Clock to Setup on destination clock _n0506

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			2.226	

Clock to Setup on destination clock _n0507

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			2.138	

Clock to Setup on destination clock current_state[3]_GND_11_o_Mux_107_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			2.226	

Clock to Setup on destination clock current_state[3]_GND_3_o_Mux_91_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.981	
current_state[3]_GND_11_o_Mux_107_o			1.725	

Clock to Setup on destination clock current_state[3]_PWR_15_o_Select_160_o

```
---------------------------------+---------+---------+---------+---------+
                                 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                     |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------------------------+---------+---------+---------+---------+
CLK                              |         |         |    3.506|         |
current_state[3]_GND_3_o_Mux_91_o|         |         |    2.189|         |
current_state[3]_GND_7_o_Mux_99_o|         |         |    2.914|         |
---------------------------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 9.20 secs

-->

Total memory usage is 4510328 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   16 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```

Implementation Report

```
Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'vending_machine'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o vending_machine_map.ncd vending_machine.ngd
vending_machine.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Dec 13 19:29:21 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    7
Slice Logic Utilization:
  Number of Slice Registers:                   103 out of  18,224    1%
    Number used as Flip Flops:                  93
    Number used as Latches:                      9
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                1
  Number of Slice LUTs:                        189 out of   9,112    2%
    Number used as logic:                      189 out of   9,112    2%
      Number using O6 output only:             164
      Number using O5 output only:               2
      Number using O5 and O6:                   23
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   2,176    0%

Slice Logic Distribution:
  Number of occupied Slices:                    63 out of   2,278    2%
  Number of MUXCYs used:                         4 out of   4,556    1%
  Number of LUT Flip Flop pairs used:          195
    Number with an unused Flip Flop:            92 out of     195   47%
    Number with an unused LUT:                   6 out of     195    3%
    Number of fully used LUT-FF pairs:          97 out of     195   49%
    Number of unique control sets:               7
    Number of slice register sites lost
      to control set restrictions:              34 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        17 out of     232    7%
    IOB Latches:                                 6
```

```
Specific Feature Utilization:
  Number of RAMB16BWERs:                        0 out of      32    0%
  Number of RAMB8BWERs:                         0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:            0 out of      32    0%
  Number of BUFG/BUFGMUXs:                      1 out of      16    6%
    Number used as BUFGs:                       1
    Number used as BUFGMUX:                     0
  Number of DCM/DCM_CLKGENs:                    0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                  0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:        0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                  6 out of     248    2%
    Number used as OLOGIC2s:                    6
    Number used as OSERDES2s:                   0
  Number of BSCANs:                             0 out of       4    0%
  Number of BUFHs:                              0 out of     128    0%
  Number of BUFPLLs:                            0 out of       8    0%
  Number of BUFPLL_MCBs:                        0 out of       4    0%
  Number of DSP48A1s:                           0 out of      32    0%
  Number of ICAPs:                              0 out of       1    0%
  Number of MCBs:                               0 out of       2    0%
  Number of PCILOGICSEs:                        0 out of       2    0%
  Number of PLL_ADVs:                           0 out of       2    0%
  Number of PMVs:                               0 out of       1    0%
  Number of STARTUPs:                           0 out of       1    0%
  Number of SUSPEND_SYNCs:                      0 out of       1    0%

Average Fanout of Non-Clock Nets:               4.93

Peak Memory Usage:  4520 MB
Total REAL time to MAP completion:  9 secs
Total CPU time to MAP completion:   7 secs

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Section 1 - Errors
------------------

Section 2 - Warnings
--------------------
WARNING:PhysDesignRules:372 - Gated clock. Clock net
```

```
   current_state[3]_GND_11_o_Mux_107_o is sourced by a combinatorial pin. This
   is not good design practice. Use the CE pin to control the loading of data
   into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net
   current_state[3]_GND_3_o_Mux_91_o is sourced by a combinatorial pin. This is
   not good design practice. Use the CE pin to control the loading of data into
   the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net
   current_state[3]_PWR_15_o_Select_160_o is sourced by a combinatorial pin.
   This is not good design practice. Use the CE pin to control the loading of
   data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net _n0491 is sourced by a
   combinatorial pin. This is not good design practice. Use the CE pin to
   control the loading of data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net _n0507 is sourced by a
   combinatorial pin. This is not good design practice. Use the CE pin to
   control the loading of data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net _n0506 is sourced by a
   combinatorial pin. This is not good design practice. Use the CE pin to
   control the loading of data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net
   current_state[3]_GND_7_o_Mux_99_o is sourced by a combinatorial pin. This is
   not good design practice. Use the CE pin to control the loading of data into
   the flip-flop.

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------
   1 block(s) optimized away

Section 5 - Removed Logic
-------------------------

Optimized Block(s):
TYPE         BLOCK
GND          XST_GND

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
--------------------------
```

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
CARD_IN	IOB	INPUT	LVCMOS25						
CLK	IOB	INPUT	LVCMOS25						
COST<0>	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		
COST<1>	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		
COST<2>	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		
DOOR_OPEN	IOB	INPUT	LVCMOS25						
FAILED_TRAN	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		
INVALID_SEL	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		
ITEM_CODE<0>	IOB	INPUT	LVCMOS25						
ITEM_CODE<1>	IOB	INPUT	LVCMOS25						
ITEM_CODE<2>	IOB	INPUT	LVCMOS25						
ITEM_CODE<3>	IOB	INPUT	LVCMOS25						
KEY_PRESS	IOB	INPUT	LVCMOS25						
RELOAD	IOB	INPUT	LVCMOS25						
RESET	IOB	INPUT	LVCMOS25						
VALID_TRAN	IOB	INPUT	LVCMOS25						
VEND	IOB	OUTPUT	LVCMOS25		12	SLOW	OLATCH		

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.