Wideband Impedance Matching of 6G Wireless Application Using High Gain Patch Antenna

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OBJECTIVES

The objective of this project was to analyze and understand the important topics of the Electromagnetic Devices for RF and Wireless Communications(EECE-5693) and then choose the project that would best cover all of those topics so that we could comprehend it more thoroughly.

Then we choose the paper which focus on Develop a method for wideband impedance matching in Sub-Terahertz (THz), understanding transmission lines(2 port network), subarray design, four antenna elements are combined with 4-way power divider to form 4×1 array, we get to know about return loss also the use of S-matrix, impedance matching using Smith chart also using in CST, Aimed to minimize reflection coefficients and maximize power transfer efficiency , designed to resonate at different frequencies, providing wideband impedance matching, Improved transmission efficiency, Fabrication, Integration and Packaging. Later we found the paper "Stub-loaded Via Transition for Wideband Impedance Matching of Sub-THz 6G Antenna-in-Package" [1] **did not have much details on which antenna is used or how its designed with the transmission line to match the whole networks for Sub-Terahertz** [1] **so we had to research new paper for the antenna part which operates at high frequencies which is "High gain Antenna Design for 6G wireless Applications"** [2]**.**

After analysis which antenna is best for our high frequency which operate in Sub-Terahertz (THz) we deiced to use the patch antenna [3]**for our project and since we only had student version of CST software, so we had to scale down our frequency 10x times to get equivalent results.**

ABSTRACT

This paper introduces wideband impedance matching for 6G Wireless Application using CST(Computer simulation technology). The frequency used for this design operation is 148 Ghz. The proposed design includes a high gain patch antenna that is connected to the beamforming IC via transition for impedance matching. The design will then be fabricated using advanced PCB technology. Since the CST student edition cannot handle high frequencies, 14.2 GHz is used as it is 10 times lower than the actual frequency used for the design which is 142 GHz. The results can then be scaled up once the simulation is finalized. The simulated design showed a return loss of -34.2 dB with a frequency of 14.2 GHz.

The paper introduces the sixth generation (6G) of wireless systems. In order to achieve better performance, a new patch antenna design for radar communication systems is presented in this work.

Milestone 1:- Impedance Matching Network Techniques, Smith chart , S-matrix, equivalent circuit analysis.

Milestone 2:- Design and Simulation, Patch antenna design in CST, analysis and calculation of all the design length, width, thickness/height etc., understanding the radiation pattern and other results.

Milestone 3:- Fabrication Process, details on how to fabricate and make the device.

Milestone 4:- Future Activity.

Milestone 5:- Q&A.

INTRODUCTION

The paper is about impedance matching for sub Thz antenna-in-package based on multi-layer PCB via transition shown in Figure 1. The operating range for the device is from 136 to 148 GHz with a center frequency of 142 Ghz. The beam scanner does a sweep through the antenna array and scans for incoming RF signals. The signals will then be routed via transition to the beamforming IC. The Beamforming IC regulates the phase and amplitude of the signal before it is sent back to the antenna array for beamforming. The purpose of beamforming is to improve signal strength and the signal to noise ratio. The BGA(Ball Grid Array) is used as a surface-mount packaging for integrated circuits.

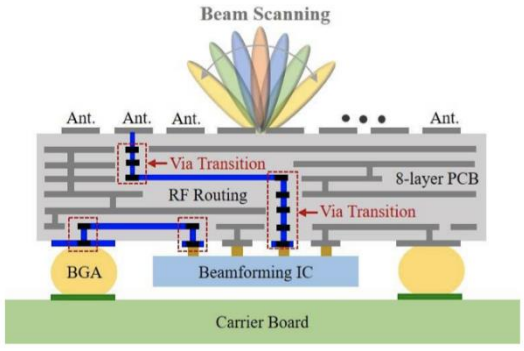


Fig. 1. Cross-sectional view of conventional antenna-in-package (AiP)

Figure 1

The Figure 2 below shows the 4x1 Subarray on 14-layer PCB. Between the cores of the PCB layers is the PPG which stands

for Prepreg which acts as an insulating layer. Between M5 to M8 is a 4-Way Divider which converges the four signals transmitted by the antenna into one big signal to be sent via transition for impedance matching in the bottom layers of the PCB.

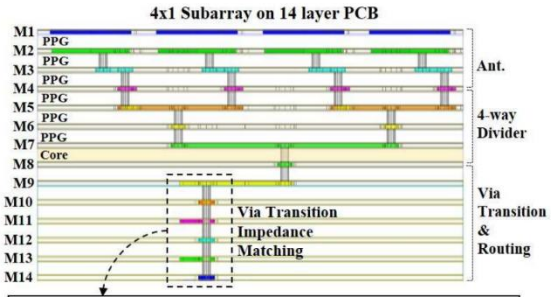


Figure 2

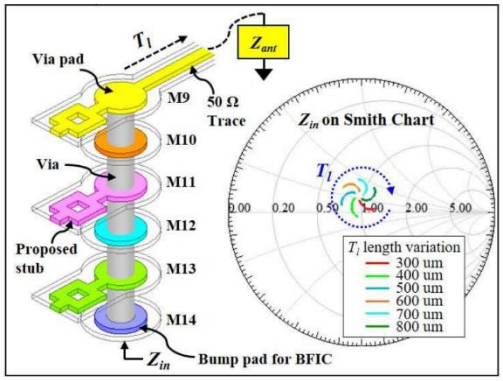


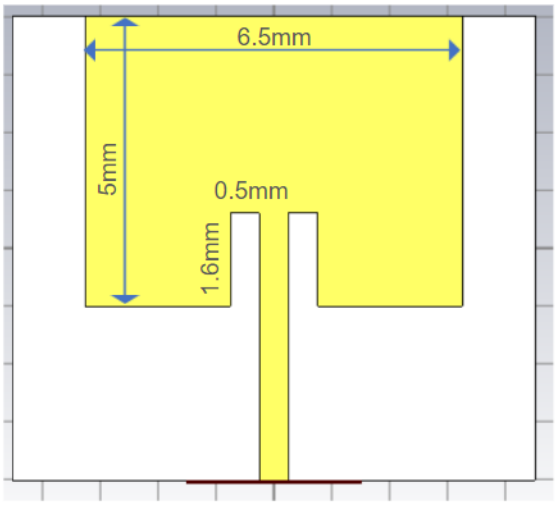
Figure 3

The Figure 3 above shows the PCB layers from M9 to M14 with 50-ohm transmission line in between. The transmission line must be matched with the impedance of the antenna in all layers of the PCB. The input impedance is shown on the Smith Chart in the figure.

The High Gain Patch Antenna Design using CST is considered because mobile communications have changed quickly in the last few years; these changes usually occur in cycles of 10 years or so. Technological developments, usually denoted by a generation number, such as 5G [4], signify each new stage of growth. Now that 5G systems are becoming commercially accessible on a large scale, there is a lot of curiosity about what comes next, which is commonly referred to as 6G and represents the future of wireless technology [5].

In order to achieve better performance, a new patch antenna design for radar communication systems is presented in this work. At a frequency of 142 GHz, the antenna works in the Sub-Terahertz band (CST student edition will not support above 20GHz so we scale down to 14.2GHz then scale it up 10X for these results) . The power transmission efficiency of the antenna was assessed using simulations, and according to FCC regulations, it was able to achieve an impedance bandwidth (S11 < -10 dB) approximately 14.2 GHz, which is comparable to -34.2 dB (scaled up to 142 GHz) for 6G applications. Additionally, simulations show the expected antenna output, emphasizing how important antenna design is to achieving future performance standards. These simulations evaluate characteristics like isolation and bandwidth to make sure the antenna performs up to par in real-world scenarios.FR-4 is a low-loss / cost substrate and we used in designs.

For 6G frequencies, the required bandwidth should be more than 20GHz, which is desirable for future reference/work [6]. In our instance, we obtained a bandwidth of 0.82GHz for a frequency of 14.2GHz; however, scaling up 10X would result in 8.2GHz, which is not ideal. Therefore, in order to obtain the bandwidth, we must truly build the patch antenna design for 142GHz.



MILESTONE I: IMPEDANCE MATCHING NETWORK TECHNIQUES

For a simple two-port network, the S-matrix is:

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

- S_{11}: Reflection coefficient at port 1.
- S_{21}: Transmission coefficient from port 1 to port 2.
- S_{12}: Transmission coefficient from port 2 to port 1.
- S_{22}: Reflection coefficient at port 2.

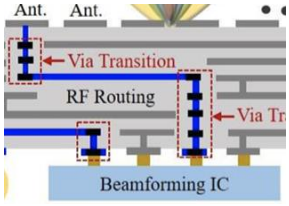


Figure 4

Smith chart - Design of impedance matching:

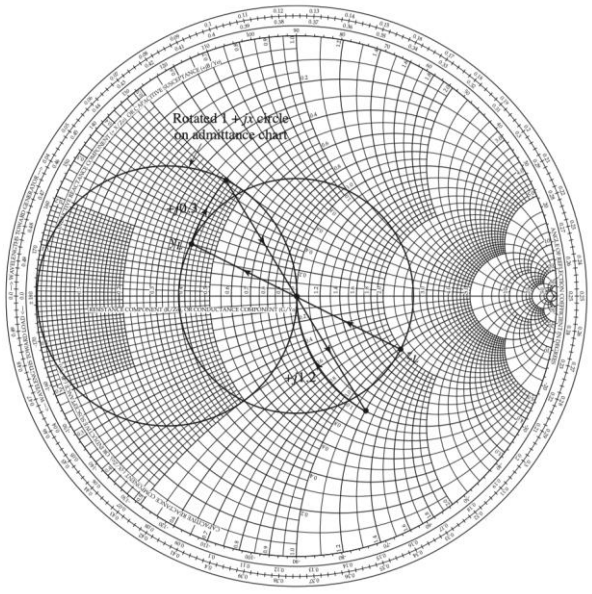


Figure 5

$$C = \frac{b}{2\pi f Z_0} \quad ; \quad L = \frac{x Z_0}{2\pi f}$$

Here we take example in our case to explain how we calculate the L-section matching network to match a series RC load with an impedance ZL = 200 − j100 ohm to a 100 ohm line at a frequency of 14.2 GHz.

The normalized load impedance is zL = 2 − j1, which is plotted on the Smith chart of Figure 5.3a. This point is inside the 1 + jx circle, so we use the matching circuit of Figure 5.2a. Because the first element from the load is a shunt susceptance, it makes sense to convert to admittance by drawing the SWR circle through the load, and a straight line from the load through the center of the chart, as shown in Figure 5. After we add the shunt susceptance and convert back to impedance, we want to be on the 1 + jx circle so that we can add a series reactance to cancel jx and match the load. This means that the shunt susceptance must move us from yL to the 1 + jx circle on the admittance Smith chart. Thus, we construct the rotated 1 + jx circle as shown in Figure 5 (center at r = 0.333). (A combined ZY chart may be convenient to use here, if it is not too confusing.) Then we see that adding a susceptance of jb = j0.3 will move us along a constant-conductance circle to y = 0.4 + j0.5 (this choice is the shortest distance from yL to the shifted 1 + jx circle). Converting back to impedance leaves us at z = 1 − j1.2, indicating that a series reactance of x = j1.2 will bring us to the center of the chart. For comparison, the formulas (Figure 5) and (Figure 6) give the solution as b = 0.29, x = 1.22.

This matching circuit consists of a shunt capacitor and a series inductor, as shown below in Figure 6. For a matching frequency of 500 MHz, the capacitor has a value of C = b / 2π f Z0 = 0.92 pF, and the inductor has a value of L = x / Z0 2π f = 38.8 nH. It is also interesting to look at the second solution to this matching problem. If instead of adding a shunt susceptance of b = 0.3, we use a shunt susceptance of b = −0.7, we will move to a point on the lower half of the shifted 1 + jx circle, to y = 0.4 − j0.5. Then converting to impedance and adding a series reactance of x = −1.2 leads to a match as well. Formulas (Figure 5) and (Figure 6) give this solution as b = −0.69, x = −1.22. This matching circuit is also shown in Figure 6 and is seen to have the positions of the inductor and capacitor reversed from the first matching network. At a frequency of f = 500 MHz, the capacitor has a value of C = −1 / 2π fxZ0 = 2.61 pF.

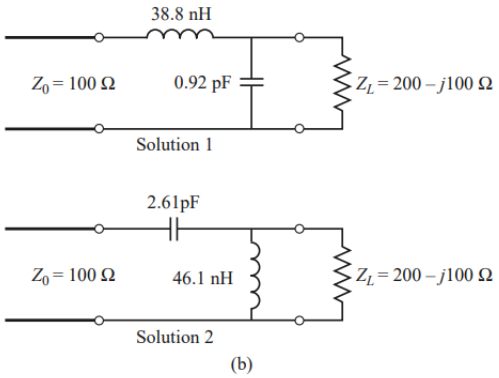


Figure 6

Similarly, we calculated for the device which gets the same results as mentioned in the **paper**.

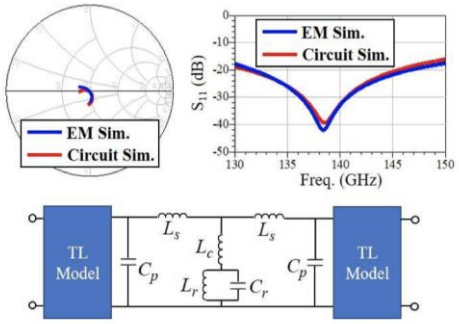
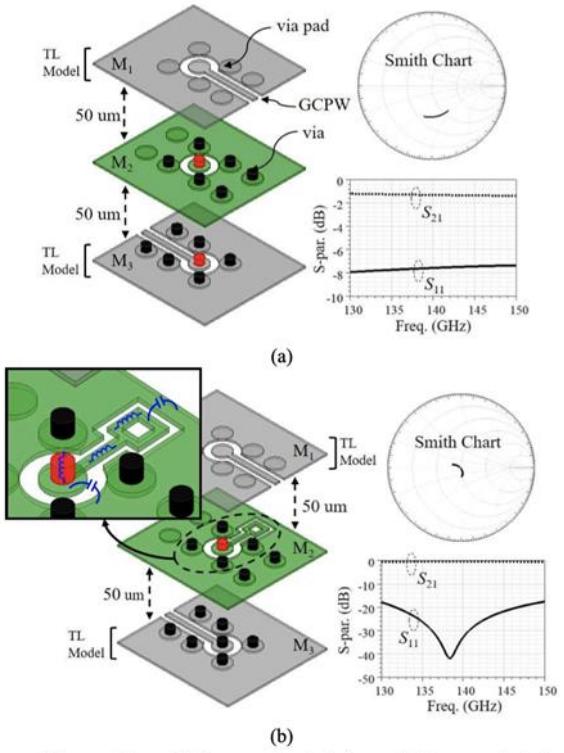


Fig. 3. Circuit simulation of proposed stub-loaded via transition (C_p=18.2 fF, L_s=17.3 pH, L_c=166 pH,, C_r=11.5 fF, and L_r=165.6 pH).

Figure 7

Figure 7 presents equivalent circuit analysis of the proposed stub loaded via transition. From the circuit analysis, it is found that the resonant frequency is dominantly affected by Ls, Lc, Lr, and Cr.



Via transitions of (a) conventional design and (b) proposed design.

Figure 8

Figure 8 (a) presents two stacked vias and its frequency response characteristic. As shown in Figure 8 (a), the via transition causes capacitive impedance mismatching between two 50-ohm transmission lines. Figure 8 (b) depicts the proposed stub-loaded via transition with brief illustration of the stub's parasitic components.

We got some extra time to 3d print a layer as shown below Figure 9, we could not design complete design yet, this is kept as future work.

Figure 9

MILESTONE II: DESIGN AND SIMULATION

A. High Gain Patch Antenna Design using CST

Patch Antenna: A type of radio antenna with a low profile, which can be mounted on a flat surface. It consists of a flat rectangular sheet or "patch" of metal, mounted over a larger sheet of metal called a ground plane.
Target Frequency: 14.2 GHz, which is typically used in Ku-band applications for satellite communication, radar, and other high-frequency communication systems [4].

Patch antennas are used in this project because of their compact size, low profile, ease of fabrication, wide bandwidth, directional radiation pattern, high efficiency, integration capabilities, and adaptability to different polarization requirements.

Key Design Parameters

1. **Frequency (f0)**: 14.2 GHz
2. **Dielectric Constant (εr)**: Determines the speed of the electromagnetic wave in the substrate. FR-4 = 4.3
3. **Substrate Thickness (h)**: Thickness of the dielectric material. =1.1mm
4. **Loss Tangent (tan δ)**: Represents the dielectric losses in the substrate material.

Formula for patch antenna design parameters

The Length, Width, Effective dielectric constant, Fringing Length are calculated below

$$L \approx 0.49\lambda_d = 0.49\frac{\lambda}{\sqrt{\varepsilon_r}} \qquad L = 0.49\left(\frac{0.0211}{\sqrt{4.3}}\right) = 5\ mm$$

$$W = \frac{\lambda}{2}\left[\frac{\varepsilon_r + 1}{2}\right]^{-1/2} \qquad W = \frac{0.0211}{2}\left(\frac{4.3+1}{2}\right)^{-\frac{1}{2}} = 6.5\ mm$$

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{10\,t}{W}\right)^{-0.5} \qquad \varepsilon_{re} = \frac{4.3+1}{2} + \frac{4.3-1}{2}\left(1 + \frac{10(0.16)}{6.5}\right)^{-0.5} = 4.128$$

$$\Delta L = 0.412\,\frac{(\varepsilon_{re} + 0.3)\left(\frac{W}{t} + 0.264\right)}{(\varepsilon_{re} - 0.258)\left(\frac{W}{t} + 0.8\right)}\,t \qquad \Delta L = 0.412\left[\frac{(4.128+0.3)\left(\frac{6.5}{0.16}+0.264\right)}{(4.128-0.258)\left(\frac{6.5}{0.16}+0.8\right)}\right] = 7.44 \cdot 10^{-5}$$

Now keeping all these calculated values, we try to adjust and test for the best efficiency in CST for other values. We used several test cases and changed all materials finally we took FR-4 substrate to get best results and other parameters shown in Figure 10.

Parameter List

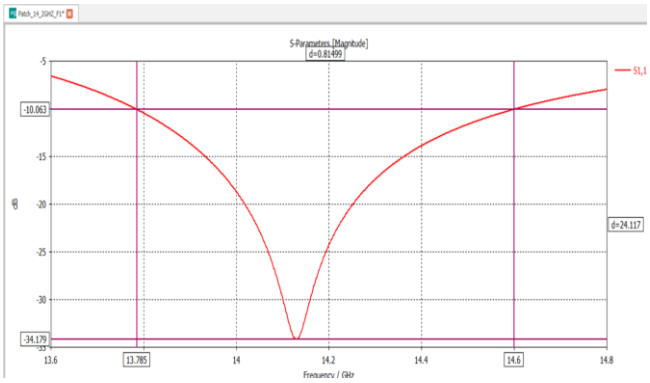
Name	Expression	Value	Description
Ws	= 9	9	Substrate width
Ls	= 8	8	Substrate Length
Hs	= 1.1	1.1	Substrate Height
Wp	= 6.5	6.5	Patch Width
Lp	= 5	5	Patch Length
Hp	= 0.0035	0.0035	Patch Hight
DL	= 0.000074	0.000074	Delta L
Wf	= 0.5	0.5	Feed Width
Yo	= 1.6	1.6	Inset Height

Figure 10

B. Simulation Overview

CST simulation result of Patch Antenna S11 bandwidth

The measured return loss (S11) of -34.179 dB signifies that the antenna under test exhibits excellent performance in minimizing reflected power. This outcome suggests a highly effective impedance match, which is critical for efficient power transfer and minimal signal loss in RF systems. Given the standard benchmarks, this result would be considered very good to excellent, suitable for most high-performance and critical applications.



S11 result when f= 14.129GHz

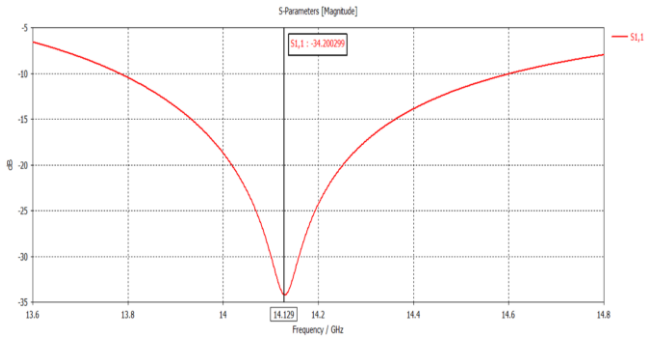
In RF antenna design, S11 (or return loss) is a measure of how much power is reflected back from the antenna due to impedance mismatch. A return loss of -34 dB indicates that very little power (approximately 0.03% of the incident power) is being reflected back, which generally suggests a good match between the antenna and the transmission line or system it is connected to.

However, whether -34 dB is "good" for S11 depends on the specific requirements of your RF system. In many applications, particularly in RF and microwave engineering, a return loss of -10 dB or better (-10 dB being a reflection coefficient of 0.1 or less) is often considered acceptable for efficient power transfer and minimal signal loss.

Here's a general guideline for return loss (S11 in dB) and its corresponding reflection coefficient:

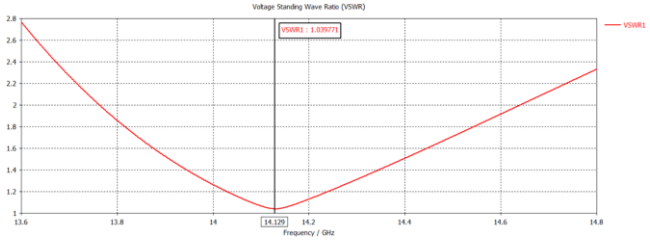
Return Loss (S11):
Greater than -10 dB: Generally good for most applications.
Greater than -20 dB: Very good, suitable for most high-performance applications.
Greater than -30 dB: Excellent, typical for critical applications requiring very low reflection.
Therefore, -34 dB for S11 typically indicates excellent performance in minimizing reflected power. It suggests that the antenna is well-matched to its operating frequency and impedance, which is beneficial for maximizing power transfer efficiency and minimizing losses in the RF system.

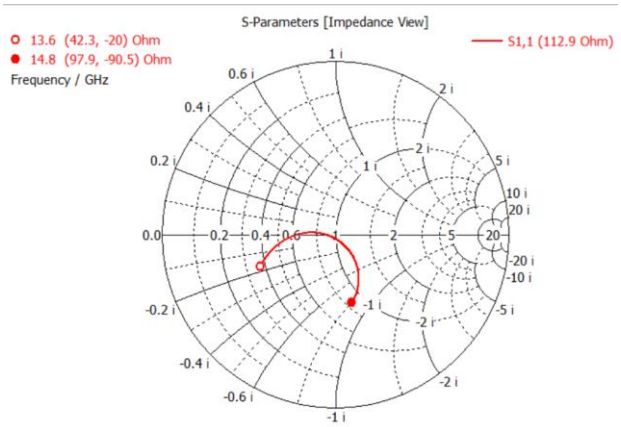
If our application requires very precise performance or if we have specific specifications to meet, you should check the detailed requirements for your antenna system. However, in many cases, -34 dB would indeed be considered quite good for S11 in an RF antenna context so we stopped analysis here.



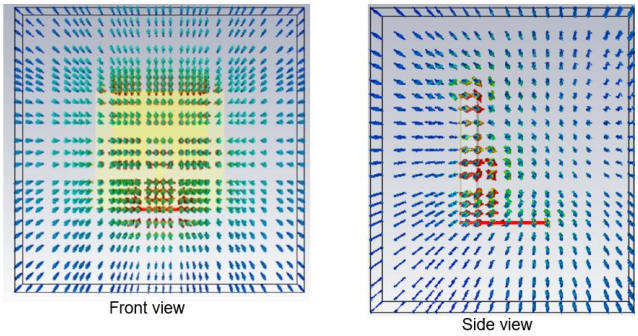
VSWR

The Voltage Standing Wave Ratio (VSWR) is a key parameter in antenna design and analysis, reflecting the efficiency of power transmission from the transmission line to the antenna. It is a measure of the impedance matching between the antenna and the transmission line. A low VSWR value indicates good impedance matching, meaning that most of the input power is transmitted to the antenna with minimal reflections. This is crucial for efficient antenna operation and maximum radiation efficiency. Conversely, a high VSWR indicates poor matching, leading to significant power reflections, reduced efficiency, and potential damage to the transmitter. In the context of our patch antenna design, the measured VSWR value is 1.03. This very low value indicates excellent impedance matching.





E-field



e-field (f=14.2) [1]	
Type	E-Field
Frequency	14.2 GHz
Wavelength	21.1121 mm
Plot attribute	Instantaneous
Phase	199.25 °
Maximum (Solver)	27483.3 V/m
Max. pos. (X, Y, Z)	3.250, -1.000, 1.100 mm

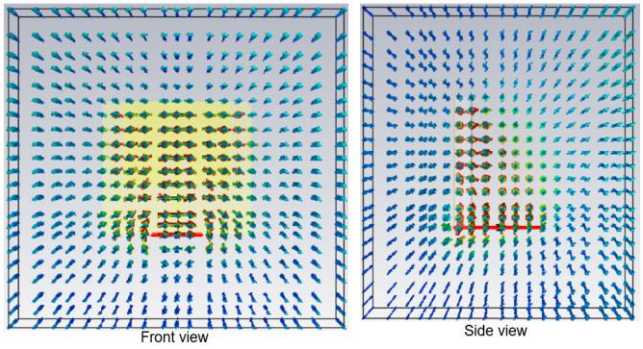
Figure 11

The E-field is perpendicular to the patch and forms a standing wave pattern with maximum values at the edges and minimum values at the center. This is similar to the current density pattern but offset by 90 degrees in phase

The fringing fields at the edges of the patch contribute to the radiation of electromagnetic waves and the impedance of the antenna.

The combination of the fringing fields from both edges of the patch constructively interferes in the broadside direction, leading to efficient radiation

H-field



h-field (f=14.2) [1]	
Type	H-Field
Frequency	14.2 GHz
Wavelength	21.1121 mm
Plot attribute	Instantaneous
Phase	168.75 °
Maximum (Solver)	147.298 A/m
Max. pos. (X, Y, Z)	-0.625, 0.400, 0.916 mm

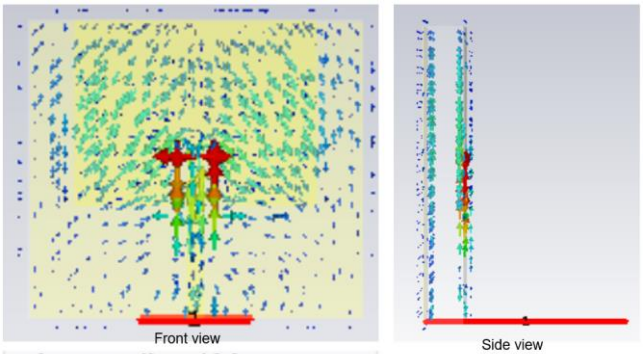
Figure 12

The H-field is predominantly tangential to the width of the patch and forms a standing wave pattern with maximum values at the edges. The interaction between the E-field and H-field at the patch edges results in the radiation of electromagnetic waves.

The H-field in CST simulations is essential for understanding the magnetic field intensity in electromagnetic systems.

The location of the feed point affects the H-field distribution and impedance matching. At the centerline of the patch, the impedance is generally higher due to lower H-field intensity.

Surface current



surface current (f=14.2) [1]	
Type	Surface current
Frequency	14.2 GHz
Wavelength	21.1121 mm
Plot attribute	Instantaneous
Phase	131.75 °
Maximum (Plot)	127.943 A/m
Max. pos. (X, Y, Z)	-0.750, 0.600, 1.100 mm

Figure 13

The current is maximum at the center of the patch and decreases towards the edges.

The current is zero at the edges perpendicular to the length of the patch due to boundary conditions.

At the edges of the patch, the currents cannot continue and hence create fringing fields which extend into the air above the patch.

These fringing fields are crucial for radiation. The interaction between the electric fields and the magnetic fields generates electromagnetic waves that propagate away from the antenna.

Current density

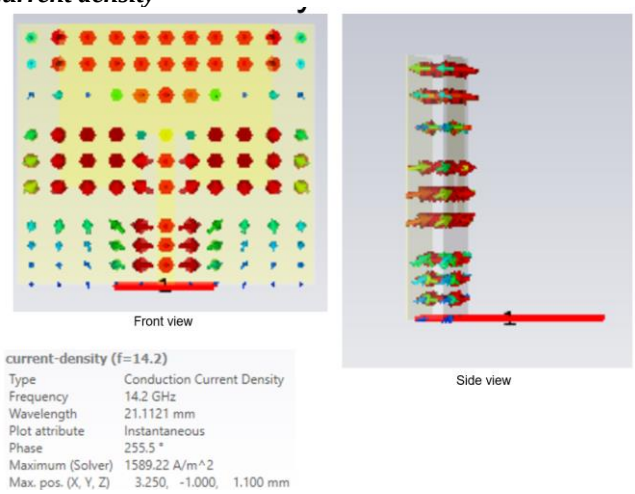


Figure 14

The current density in a patch antenna is a critical aspect that determines its performance, including radiation patterns, impedance matching, and efficiency.

The current density is maximum along the centerline of the patch (at the feed point) and decreases towards the edges.

We choose FR-4 (lossy) as our material for substrate which has dielectric constants of 4.3 [7], and thicker substrates tend to concentrate the current density more towards the center of the patch.

Farfield Directivity for radiation

The far-field region, or radiation zone, of a patch antenna is where the electromagnetic waves radiated by the antenna propagate and where the radiation pattern is fully formed and becomes stable.

The far-field region of a patch antenna is where the radiation pattern stabilizes and becomes independent of the distance from the antenna. This region is characterized by a well-defined directive radiation pattern, typically broadside for rectangular patches. The fringing fields at the patch edges play a crucial role in the radiation mechanism. Understanding the far-field characteristics, including the radiation pattern, polarization, and efficiency, is essential for designing and optimizing patch antennas.

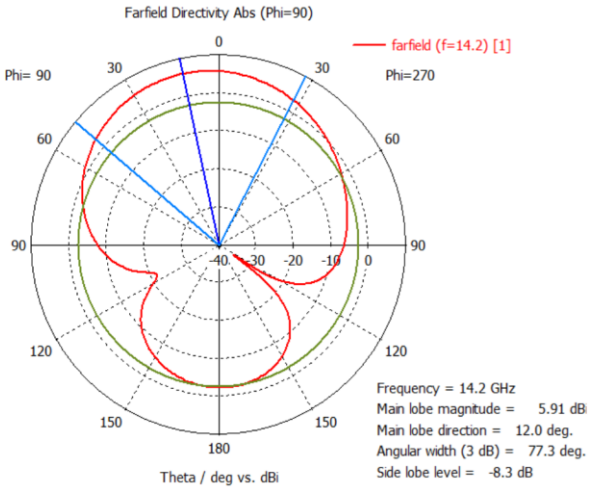


Figure 15: 1D

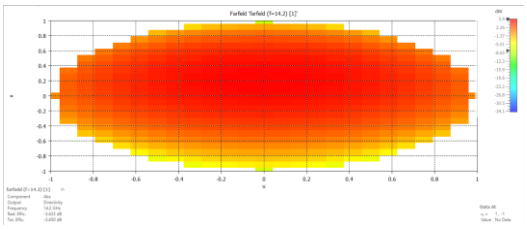


Figure 16: 2D

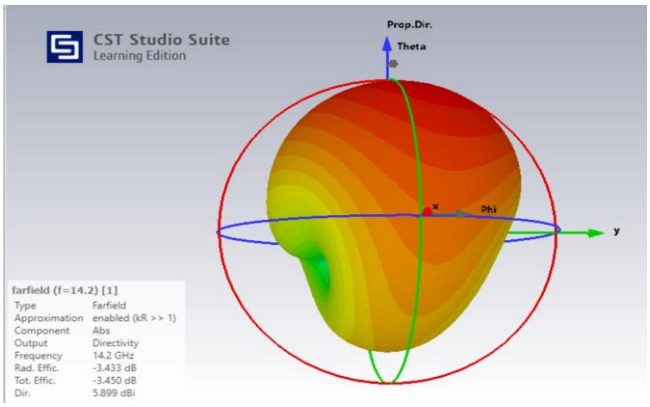
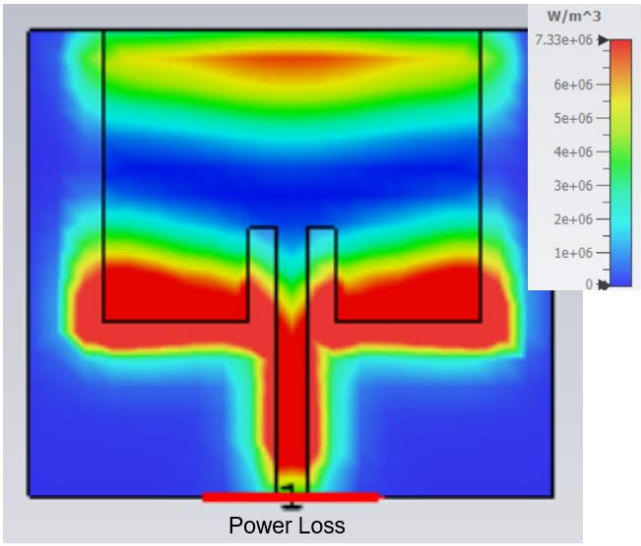


Figure 17: 3D

For a standard rectangular patch, the polarization is typically linear.

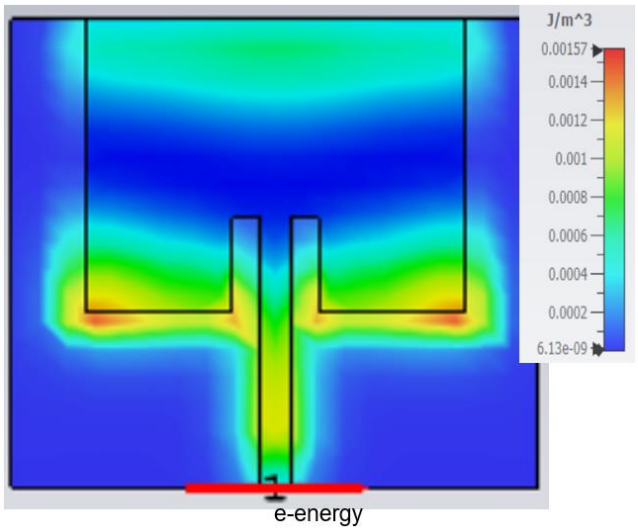
Power loss



loss (f=14.2)

Type	Power Loss Density
Frequency	14.2 GHz
Wavelength	21.1121 mm
Maximum (Solver)	1.13875e+07 W/m^3
Max. pos. (X, Y, Z)	-3.250, -1.399, 0.732 mm
Minimum (Solver)	0 W/m^3
Min. pos. (X, Y, Z)	-9.778, -9.278, -5.282 mm

E-energy



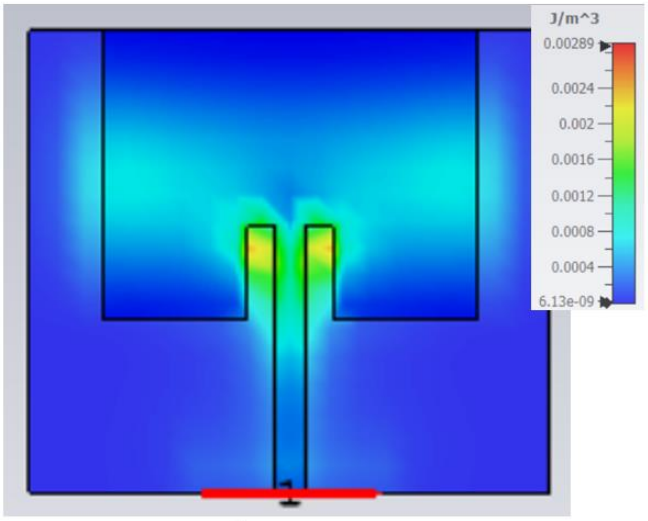
e-energy (f=14.2)

Type	Electric Energy Density (time average)
Frequency	14.2 GHz
Wavelength	21.1121 mm
Maximum (Solver)	0.00220062 J/m^3
Max. pos. (X, Y, Z)	2.812, -1.000, 0.732 mm
Minimum (Solver)	1.69901e-09 J/m^3
Min. pos. (X, Y, Z)	-0.000, 1.822, -0.004 mm

The CST simulation results for the rectangular patch antenna highlight significant variations in power density within the antenna structure. The maximum power density of 1.13857×10^7 W/m3 at (−3.250, 1.399, 0.732 mm) underscores the effectiveness of the feed mechanism, while the minimum power density of 0 W/m3 (−9.778, −9.278, −5.282mm) delineates regions of low electromagnetic activity. These insights are crucial for further optimization and enhancement of the antenna design, aiming to achieve better performance and higher efficiency.

The CST simulation results for the rectangular patch antenna reveal significant variations in electric energy density within the antenna structure. The maximum electric energy density of 0.00220062 W/m3 at (2.812, −1.0, 0.732 mm) underscores regions of intense electric field concentration, crucial for the antenna's radiation mechanism. In contrast, the minimum electric energy density of 1.69901×10−9 W/m3 at (0.0, 1.822, −0.004 mm) delineates areas of minimal electric field activity.

H-energy



h-energy

h-energy (f=14.2)	
Type	Magnetic Energy Density (time average)
Frequency	14.2 GHz
Wavelength	21.1121 mm
Maximum (Solver)	0.0039731 J/m^3
Max. pos. (X, Y, Z)	-0.750, 0.200, 0.732 mm
Minimum (Solver)	2.34155e-11 J/m^3
Min. pos. (X, Y, Z)	-0.250, 2.300, -0.004 mm

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The CST simulation results for the rectangular patch antenna reveal significant variations in magnetic energy density within the antenna structure. The maximum magnetic energy density of 0.0039371 J/m3 at (−0.750, 0.200, 0.732 mm) highlights regions of intense magnetic field concentration, which are crucial for the antenna's radiation mechanism. In contrast, the minimum magnetic energy density of 2.34155×10−11 J/m3 at (−0.250, 2.300, −0.004 mm) delineates areas of minimal magnetic field activity.

MILESTONE III: FABRICATION PROCESS

A. About Fabrication Process

Fabrication Process for 4×1 subarray

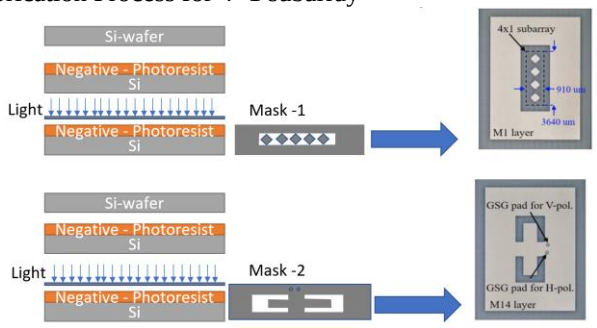


Figure 18

In this part of the report, we will go through the fabrication process. This includes all the details, for example mask pattern, choice of etchant, and cleaning process. The cross section of the device along with masks will also be shown as steps proceed.
The steps are as below.

1. Start with a Silicon wafer.
2. RCA clean
3. LPCVD, deposit a 3 microns of oxide layer as sacrificial layer.
4. Photolithography, spin coat 4 microns of positive photoresist and expose with mask 1. (To create space to anchors)
5. Mask 1 (UV light shines through blue area):
6. BOE etch through oxide layer.
7. Use piranha to remove photoresist and perform RCA clean.
8. Photolithography, spin coat 4 microns of positive photoresist and expose with mask 2.
9. Dry-etch polysilicon using reactive-ion etching.
10. Use piranha to remove photoresist and perform RCA clean.
11. Used buffered HF to remove sacrificial layer.
12. RCA clean.
13. Rinse and dry to critical point.

The lithography process – We involved in applying negative photoresist(Normally always we use positive photoresist was mentioned) onto the wafer, baking it, cooling it, and then printing into the wafer using UV light with a mask in between. Used the developer solution to remove the soluble photoresist after the wafer has been exposed to UV light, and then wash the wafer with water to get rid of any leftover developer or photoresist. Use a nitrogen cannon to dry the wafer off then Check to see if pattern has been imprinted on the wafer. Later, we needed to measure the photoresist layer's thickness.

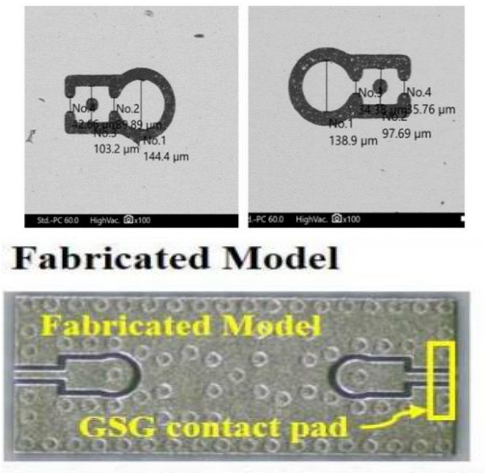
Mask Design:

The lithography process begins with the design of a mask, which contains the pattern that will be transferred onto the semiconductor wafer(Here we used a mask which had Northeastern logo in it to print to the Si wafer).

Substrate Preparation:

Before the lithography process begins, the Si wafer undergoes several preparation steps. These will include cleaning to remove any contaminants, as well as processes to ensure the surface is uniform and flat. The wafer was taken straight out of the lab for testing purposes; we did not clean it for unknown or expensive reasons. When we printed the logo onto the wafer, there were several faulty areas since the wafer wasn't quite clean.

Similarly, we make the mask for the below and fabricate it.



Details on how to do Fabrication Process

There are two main types of photoresists: positive and negative. In positive photoresist, exposure to light makes the material more soluble in developer solution, while in negative photoresist, exposure to light makes the material less soluble.
In the below figure shown, where we applied the negative photoresist onto the Si wafer and spin it for 60 sec @4000 rpm and a small black bottle which you see in the image was the negative photoresist. When we spin, we get a thickness of 2.7micron of photoresist.

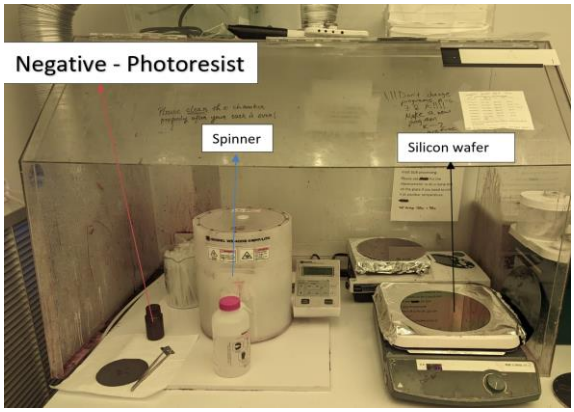
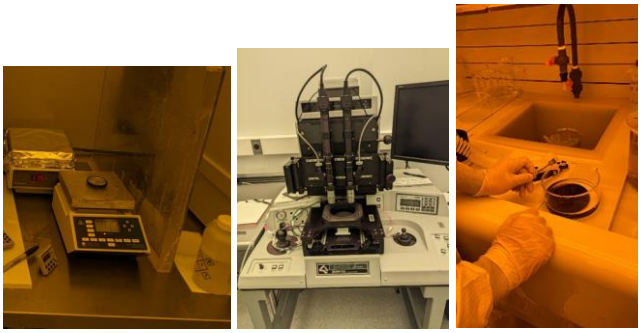


Figure 19

Exposure:

The masked pattern is transferred onto the photoresist-coated wafer using a photolithography tool shown below. This tool projects light through the mask onto the wafer, exposing areas of the photoresist according to the desired pattern. The exposure causes chemical changes in the photoresist, creating a latent image of the 4×1 subarray.
Note before the exposure of UV light we had to bake the wafer to 110C and later cool the wafer then place it in the UV light. We Bake Si wafer for 60 sec shown in below figure.



Development:

After exposure, the wafer is immersed in a developer solution (AZ726 MIF). The developer selectively removes either the exposed or unexposed areas of the photoresist, depending on whether positive or negative photoresist is used. This step reveals the patterned areas of the wafer. We used negative resist, so the developer removes the resist which was un-exposed to light.

Etching:

We can use any of the two different tools to do the etching which are ,

1) IPC plasma etch 790 series (Anisotropic etch) (Figure 20) , we utilize this technique because that aims to preferentially remove a material in specific directions to obtain intricate and often flat shapes.

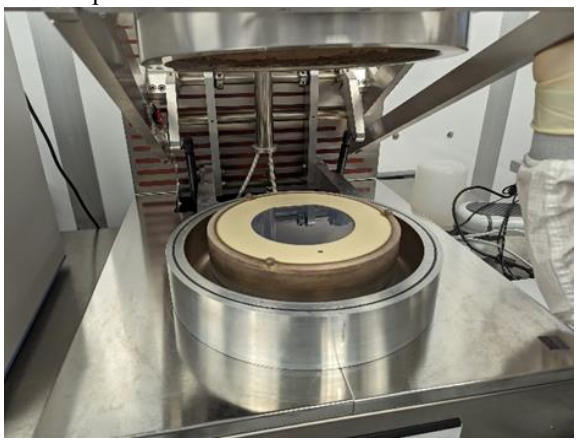


Figure 20

2) XACTIX (isotropic etch) (Figure 21) this method etch all sides so we will not use it for this project.

Figure 21

Preparation:
We obtain silicon wafers which was processed in a previous lithography lab, ensuring they have a patterned photoresist layer. (we cut this wafer into small piece using cutting tool then use it for etching)
We got familiarize with the IPC and XACTIX tools, understanding their functionalities

Alternative methods for isotropic silicon etching:
1. Wet chemical etching:
Hydrofluoric acid (HF): This is the most common isotropic wet etchant for silicon. It reacts readily with silicon but requires careful handling due to its hazardous nature.
Potassium Hydroxide (KOH): While primarily an anisotropic etchant, it can achieve isotropic etching under specific conditions like high temperature and certain additives.
Ethylenediamine Pyrocatechol (EDP): This is a safer alternative to HF, offering isotropic etching with moderate etch rates.

Plasma etching with different etch chemistries:
Chlorine-based gases (Cl2, CHF3): These can achieve isotropic etching of silicon but may leave residues and require careful control of parameters.
Bromine-based gases (Br2, BrF3): Similar to chlorine-based options, these offer isotropic etching but need proper handling due to their toxicity.

Cryogenic etching with SF6:
This method uses SF6 gas at cryogenic temperatures to achieve isotropic etching with minimal sidewall damage. However, it requires specialized equipment and expertise.

Laser ablation:
Pulsed lasers can be used for isotropic removal of silicon, offering high precision and flexibility. However, it's a complex and expensive technique.

Can we get similar results with anisotropic etch? : NO
Achieving exactly similar results to isotropic etching with an anisotropic approach is generally **not possible.**
The fundamental difference in directionality leads to distinct etch profiles.
However, if your application allows for some level of sidewall angle, we might be able to manipulate an anisotropic etch process to achieve similar functionalities.
This could involve:
Optimizing etch parameters: Adjusting parameters like pressure, temperature, and gas composition can influence the etch profile to some extent.
Using masking techniques: Selective masking of specific areas can guide the anisotropic etch and create features resembling isotropic etching.
Combining multiple steps: Employing a sequence of anisotropic and isotropic etching steps can achieve specific profile requirements

Deep Reactive-Ion Etching (DRIE):
If we need the absolute deepest features, DRIE is the clear winner.

However, if you need moderate depth (tens of micrometers), other options like plasma etching or wet etching might be sufficient and more cost-effective.

PACKAGING

This part of the report will discuss some key steps of packaging starting with chip dicing. A brief explanation on which dicing technique we choose, and its advantages will be reported. Then we will quickly walk through how to combine fabrication process with chip dicing in our case and move on to packaging type and package dimensions.

Blade Dicing

Blade dicing is water involved, and dicing generates heat due to friction between the cutting blade and the semiconductor material. Water is used as a coolant to dissipate this heat and prevent overheating of both the blade and the semiconductor wafer. Cooling is crucial to maintain the integrity of the semiconductor devices and prevent damage to the sensitive electronic components.

Water also acts as a lubricant during the dicing process. It reduces friction between the cutting blade and the semiconductor material, which helps in achieving a smoother and more precise cut. This is important for preventing damage to the delicate structures of the semiconductor devices.

Since blade dicing is chosen and water is involved, now we must consider when to apply blade dicing along with fabrication process. This best way to implement blade dicing is to cut the chip before releasing the device which is step 11 “Used buffered HF to remove sacrificial layer”. In this case,

cutting the chip before removing sacrificial layer will not cause the device to break down.

MILESTONE IV : FUTURE ACTIVITY

- Fabricate/Package the design - we do not have resources for now so we could not complete it.
- Scale up 10x frequency - we got results for 14.2GHz but we need to get for 142GHz. So the device parameter will scale down 10x times.
- To design the 8-layer PCB design we need to use HFSS and understand it.

MILESTONE V : Q&A

1) In the paper Do they simulate the whole antenna, or they just model that with circuits?

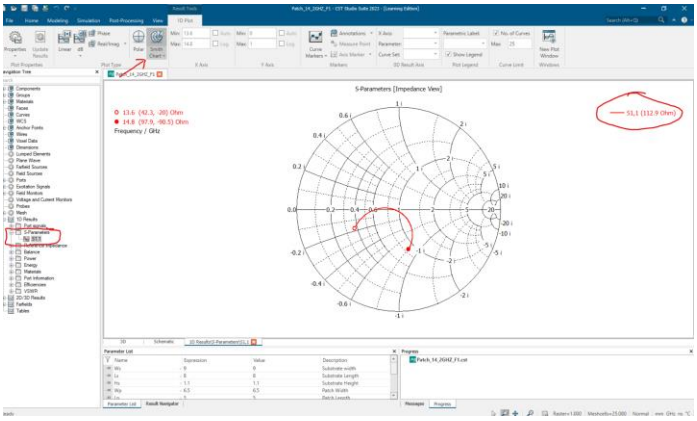
Ans; The paper focuses on the modeling and simulation of antennas using equivalent circuits rather than simulating the entire physical structure of the antenna. This method simplifies the complex electromagnetic behaviors of antennas by representing them with circuits that are easier to analyze and simulate, especially for specific parameters like impedance and power transfer efficiency. This approach is particularly useful for certain applications, though it may not fully capture all aspects of an antenna's performance, especially in complex environments, because of this we used the High gain Antenna Design paper.

2) How do they obtain the equivalent circuit model for the system?

Ans; To derive an equivalent circuit model from an EM simulation, you first perform the simulation using tools like HFSS or CST Microwave Studio, extracting parameters such as S-parameters over the desired frequency range. Convert these to Y-parameters or Z-parameters if necessary, identifying key features like resonances. Construct an initial circuit model based on the device's physical layout, starting with simple RLC networks and adding complexity as needed. Optimize the component values using fitting algorithms to match the EM data, often employing least-squares fitting. Finally, validate the model by comparing its response to additional EM simulation results or experimental data, making adjustments for improved accuracy.

3) Did we create the Smith chart ?

Ans; Yes, we simulated it using CST for the patch antenna as shown using S11.



In general Smith chart is very useful tool for an RF engineer and guide us how to match by looking into S11, by seeing the smith chart we can see if it acts more inductive or it acts more like a capacitance while looking into the values in smith chart, we can understand all this.

4) What was the side view and front view mean ?

Ans; In CST simulations, the side view and front view of an antenna are essential for understanding the flow of current and magnetic fields. The front view shows the patch antenna as if you are looking at it head-on, which helps visualize the surface current distribution. The side view, on the other hand, shows the antenna from the side, which is useful for analyzing the vertical distribution of the fields and currents. These perspectives allow for a comprehensive understanding of the antenna's performance characteristics.

5) In the feeding for the antenna 4x1 subarray is it in same phase?

Ans; it is in uniform phase.

CONCLUSION

The conclusion a stub-loaded via transition is introduced for simple and compact impedance matching in sub-THz 6G AiP designs, offering wide bandwidth by cascading proposed stubs to form a multi-stage impedance matching network. This method eliminates the need for frequency-dependent quarter-wavelength impedance transformers, simplifying routing in AiP design. The proposed design is validated through both simulated and measured results.

The conclusion encompasses a comprehensive review of previous work conducted by various researchers on 6G antennas. Each researcher focused on different objectives and outcomes, employing diverse parameters such as height, frequency selection, patch antenna types, substrate materials, fabrication methods, and improvement techniques.

In this study, I successfully designed a novel microstrip patch antenna specifically for 6G applications through simulation. The simulated results for the inset-fed patch antenna achieved an operating frequency of 14.2 GHz with a wide bandwidth of 0.814 GHz. Additionally, the return loss (S11) was recorded at -34.2 dB, indicating excellent performance characteristics for 6G communications.

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WORK DIVISION BETWEEN GROUP MEMBERS

Common Work :-

Understanding and applying all the concept of class which include impedance matching, Smith chart , S-matrix, develop a method for wideband impedance matching in Sub-Terahertz, Design and Configuration of antenna using CST, applying different test cases for highly efficient design, trial and error method to get the proper values for substrate etc.,
Also had lot of fun working together!

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NUID: 002816190
Work exp: Senior Embedded Software Engineer with 7 years of expertise (4+ years @BOSCH and 2+ years in Apsis solutions)

Expertise in efficient simulation and design of patch antennas using CST involves the initial setup of simulation parameters, designing the patch antenna with precise dimensions and insets, and updating all necessary software parameters using appropriate formulas. Includes conducting thorough Return Loss (S11) and VSWR analysis to ensure minimal reflection and efficient power transmission. Additionally, the radiation pattern and gain are simulated and evaluated to ensure optimal performance. Experimental validation through trial and error refines the design for high efficiency, and the process is concluded with a detailed fabrication procedure to ensure precision and quality in manufacturing the patch antenna.

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NUID: 001083648
Work exp: Electronics Engineer with 6 months of experience @JEOL USA and 6 months of experience @Jacobs

Expertise in antenna design calculations encompasses a comprehensive approach, starting with a robust design methodology tailored to meet specific performance requirements. This includes the careful selection of substrates and materials, considering factors such as dielectric constant, loss tangent, and thermal properties to ensure optimal performance. Precise calculations for patch dimensions are performed to achieve the desired resonant frequency and bandwidth. The design of the feed line is meticulously planned to ensure efficient power transfer and impedance matching. Ground plane configuration is also a critical aspect, as it influences the radiation pattern and overall efficiency of the antenna. Each step of the design process is meticulously documented and reported, ensuring clarity and precision in the development of high-performance antennas.

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NUID: 002837343
Work exp: 2 years' experience working for kreate energy private limited and 4 months as a research assistant in University of Petroleum and Energy Studies

Expertise in the analysis of electromagnetic fields encompasses a comprehensive examination of electric fields (E-fields), magnetic fields (H-fields), surface currents, and current density. This involves a detailed assessment of how these fields interact and propagate, as well as their impact on the overall performance of the system. Additionally, expertise includes evaluating far-field directivity to understand the radiation patterns and efficiency of antennas or other radiating structures. By analyzing these parameters, one can optimize the design for better performance, ensuring minimal losses and maximum radiation efficiency.