

# ANALYSIS OF PERFORMANCE METRICS FOR DIFFERENT CACHE CONFIGURATIONS UNDER DIFFERENT BENCHMARKS

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## INTRODUCTION:

This is a comprehensive project on performance parameters of different cache configurations performed on different set of benchmarks. Simple Scalar and SPEC2000 benchmark is used to evaluate and the parameters tweaked are cache size, block size, associativity to study about Instruction Per Cycle (IPC), Loads/Stores and Miss Rate.

## METHODOLOGY:

In this project we tweak different values of crucial performance parameters and study the results of its effects. We initially skip 100 million instructions to warm up the cache and actually analyze the performance of next 100 million instructions. The cache sizes, block sizes, associativity were all tweaked from the default value and different benchmark standards from bzip to wupwise were studied. A prototype command is as follows il1:512:32:1 and it signifies (cache type: number of sets: block size: associativity) in the same order.

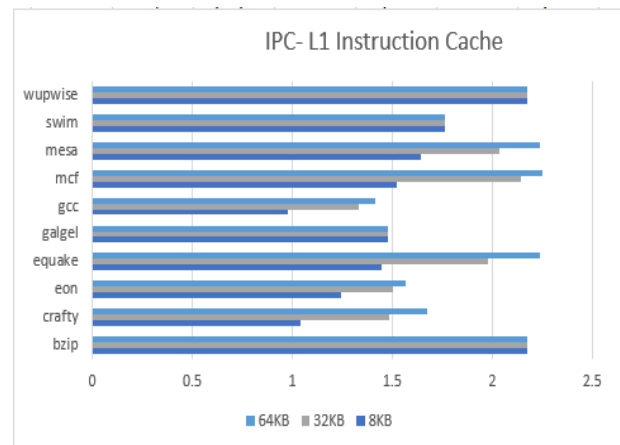
## EXPERIMENTAL RESULTS:

The results of different benchmarks are as follows

### IPC Analysis on L1 Caches:

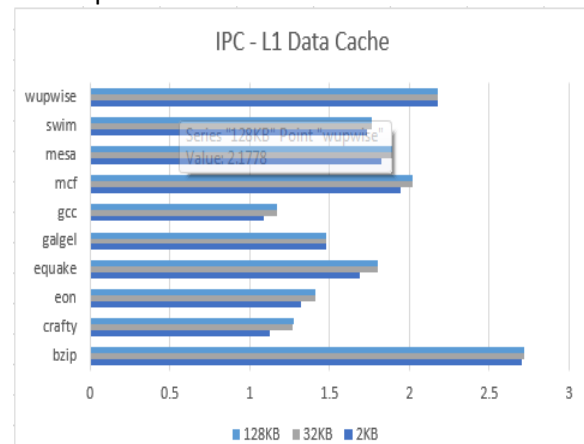
#### Instruction Cache

The graph below shows IPC of various benchmarks for various sizes from 8KB, 32KB and 64KB. Bzip and wupwise seem to perform similarly on all size configurations.



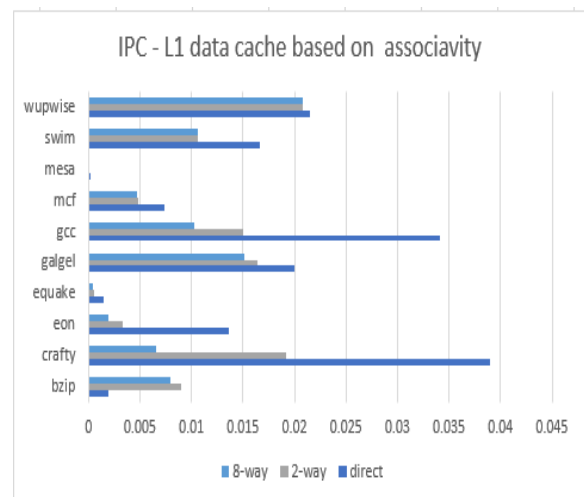
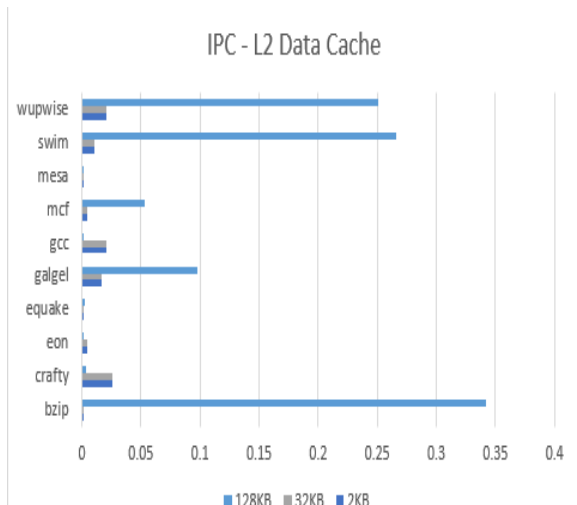
#### DATA Cache

IPC report on different sizes of L1 data cache from the default configuration. Bzip has better performance for IPC for data cache.



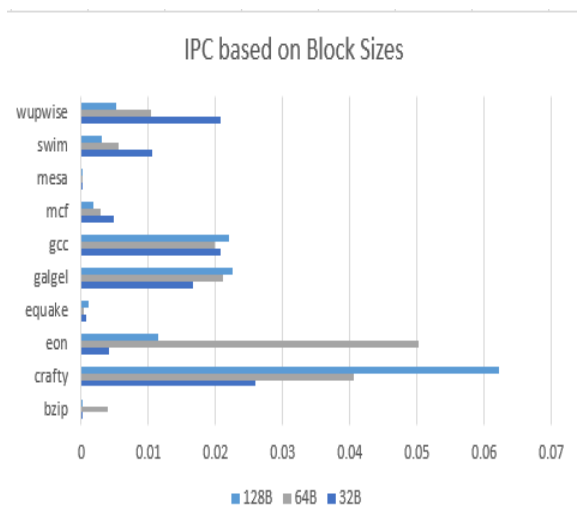
#### L2 DATA CACHE

This graph shows IPC for change in L2 data cache. 2KB, 32KB, 128KB were the sizes used. Bzip outperforms all the configurations for L2 Data Cache.



### IPC based on Block Sizes

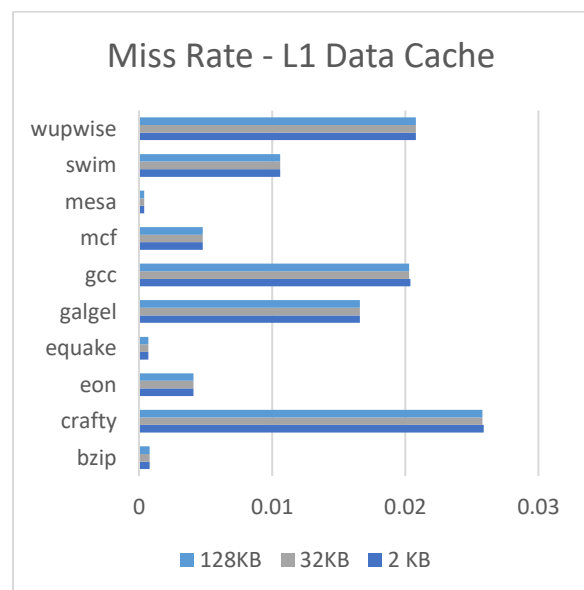
The parameter for changing has now moved to block sizes. 32B, 64B, 128B blocks were checked and crafty yielded best performance among all.



### MISS RATE ANALYSIS

#### L1 Data Cache

The miss rate was tested for configurations for 2KB, 32KB, 128KB. The miss rate for all benchmarks seems pretty consistent except a slight deviation. This cannot be seen in the graph as the deviations are very minute. Bzip and mesa has the least ratio of misses and hence have very good performance.

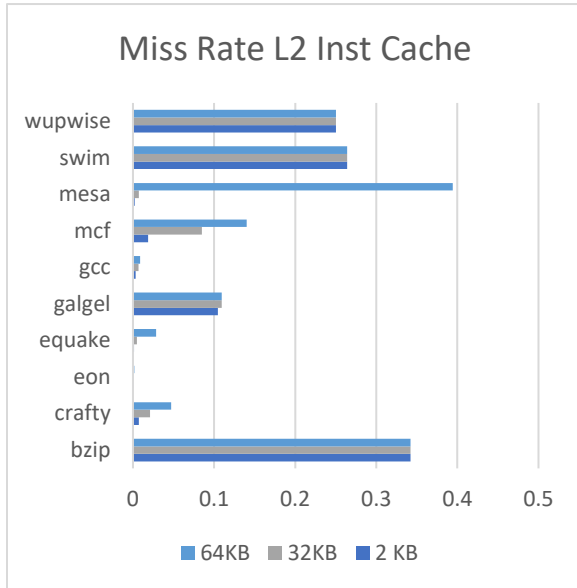


### IPC based on Associativity

For associativity based performance direct (1-way) cache gave better performance in crafty benchmark. From the graph it can be seen that the 1-way access performs better than 2 way or 8 way when the metric is IPC.

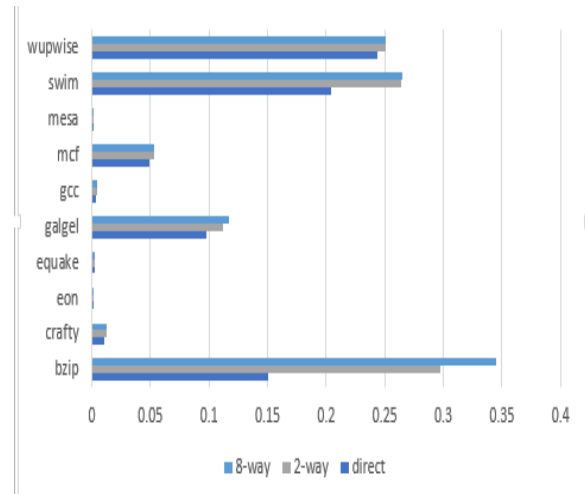
### Miss Rate – Instruction Cache

Miss Rate of instruction cache for sizes 2, 32, 128KB are noted. Gcc and eon have the least miss rates for instruction type.



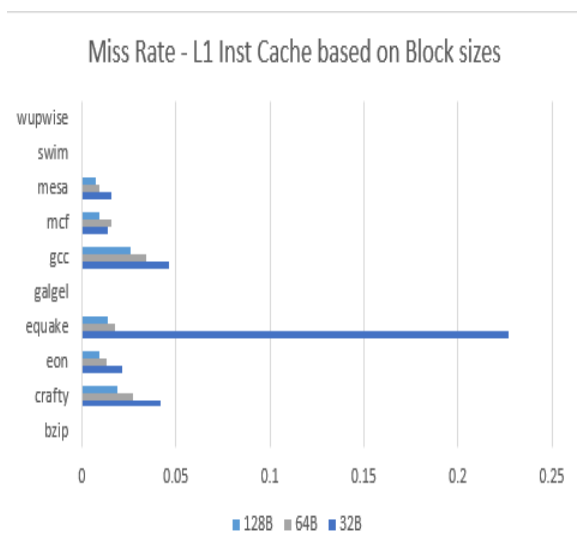
### Miss Rate- Associativity

Miss rate of a 32KB data cache for various associative configurations. Bzip seems to have higher miss rate and directly mapped seems to have lesser miss rates in all configurations again.



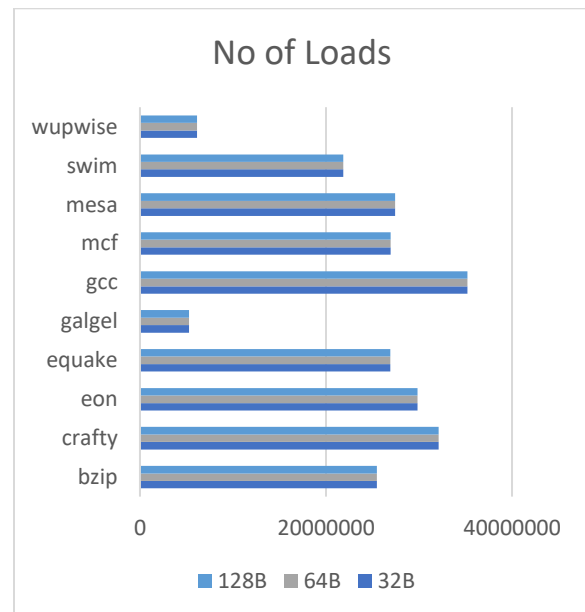
### Miss Rate for Different Block Sizes

This report is from a 32KB instruction cache with different block sizes of 128, 64 and 32 Bytes. Equake has the worst miss rate among all.



### No of Loads/Stores

No of loads and stores have remained almost constant for every different configuration.





## CONCLUSION:

A total of 450 simulations were run. For IPC performance bzip and wupwise had higher count and performed consistently. For miss rates gcc and eon had better performance. A comprehensive report is made through the collected data.