INTRODUCTION TO VLSI DESIGN

PROJECT – II

SPRING 2017

Submitted by:

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CONTENTS

1. INTRODUCTION

1.1 Flip-Flops

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems. A flip-flop stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic.

1.2 D Flip-Flop

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle. That captured value becomes the Q output. At other times, the output Q does not change. The advantage of the D flip-flop is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event.

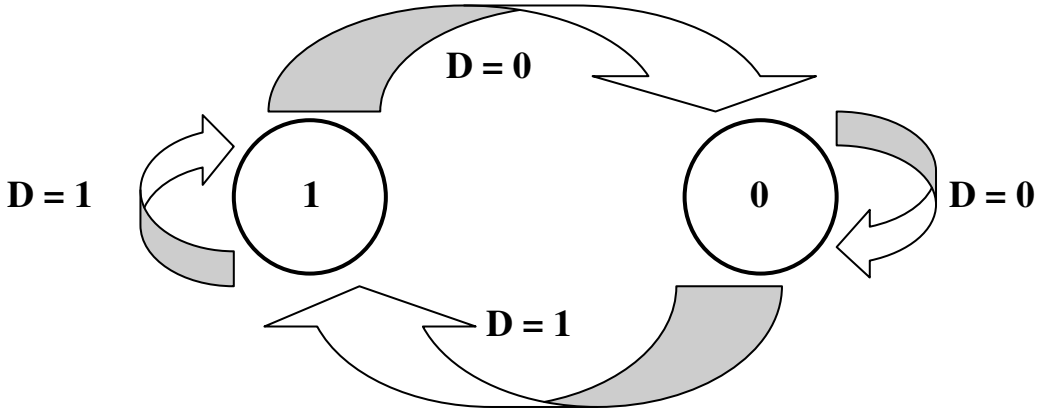
1.3 Truth Table of D Flip-Flop

The truth table of the D flip-flop is shown below.

Input		Output
D	Clock	Next Level
x	↓	Q (Previous Level)
0	↑	0
1	↑	1

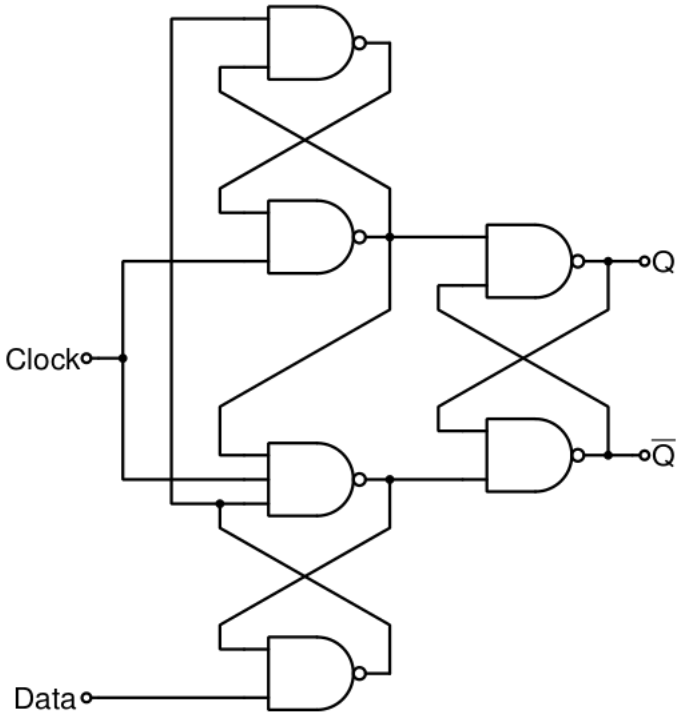
1.4 State Diagram of D Flip-Flop

The state diagram of D flip-flop is shown below.



1.5 Schematic of D Flip-Flop

The schematic of D flip-flop is given below.



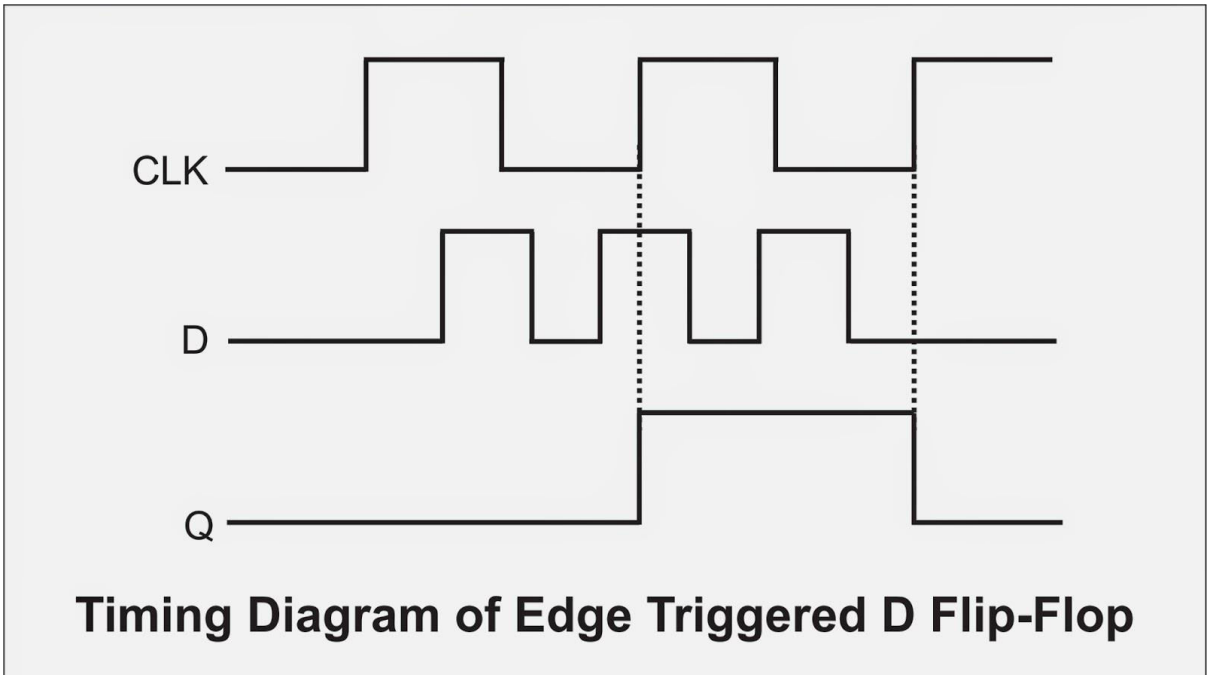
1.6 Explanation of Schematic

NAND Gates are preferred to NOR Gates in the schematic of flip-flops due to the following reasons.

- NAND Gates offer less delay
- NOR Gates occupy more area and size as the diffusion capacitance and gate capacitance are higher when compared to that of NAND Gates
- NAND Gates uses transistors of similar size that indicates that the rise time and fall time of the circuit will be equal

1.7 Output Waveform of D Flip-Flop

The output waveform of the D flip-flop is given below.



Timing Diagram of Edge Triggered D Flip-Flop

2. SCHEMATIC SECTION OF ‘D’ FLIP-FLOP

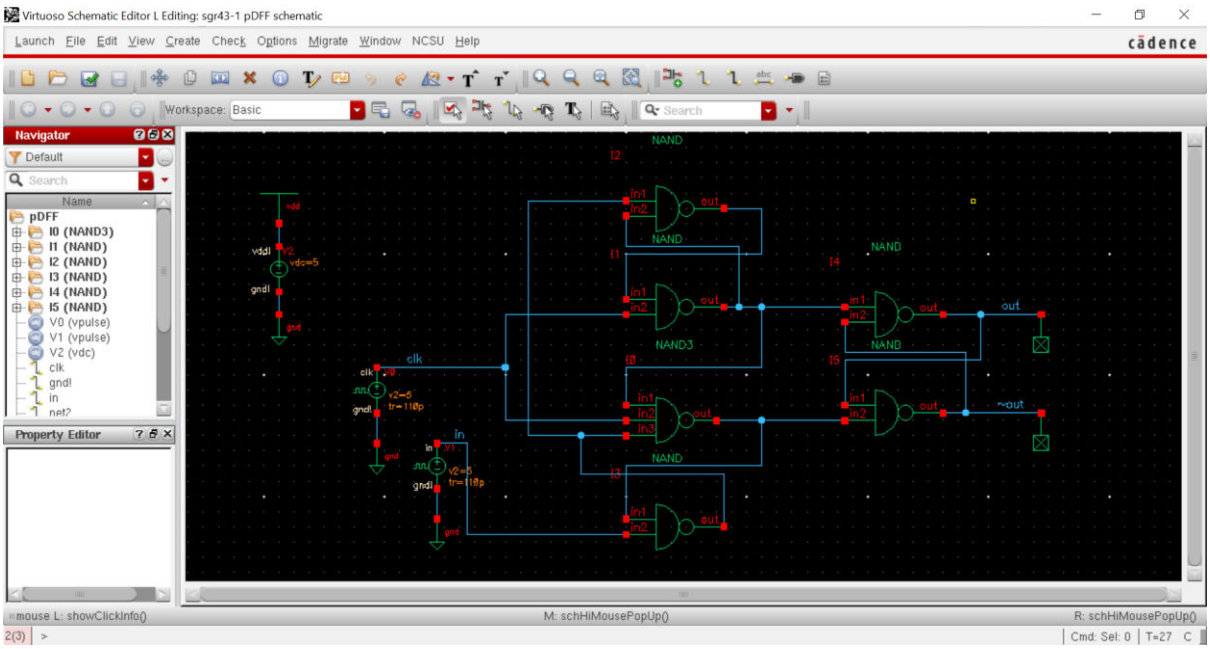


Fig.: Schematic of ‘D’ Flip-Flop

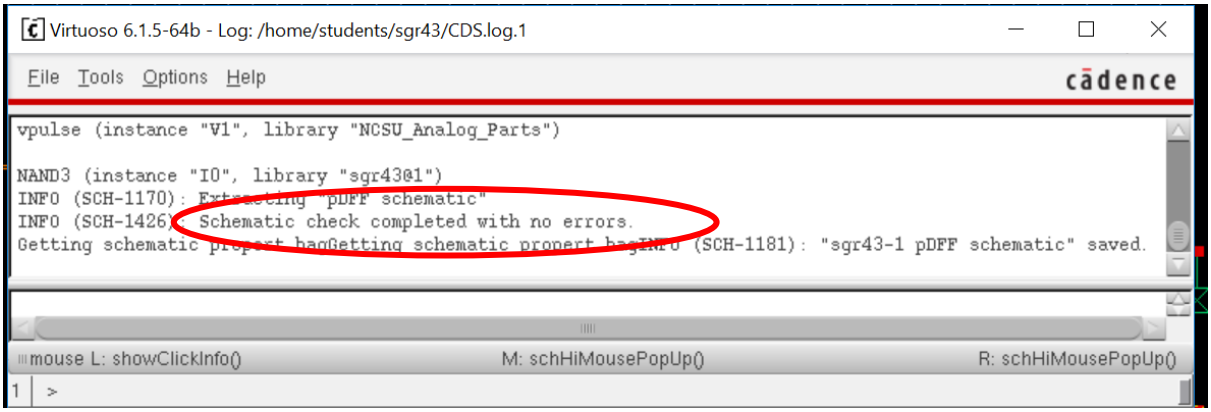


Fig.: Error Check of Schematic

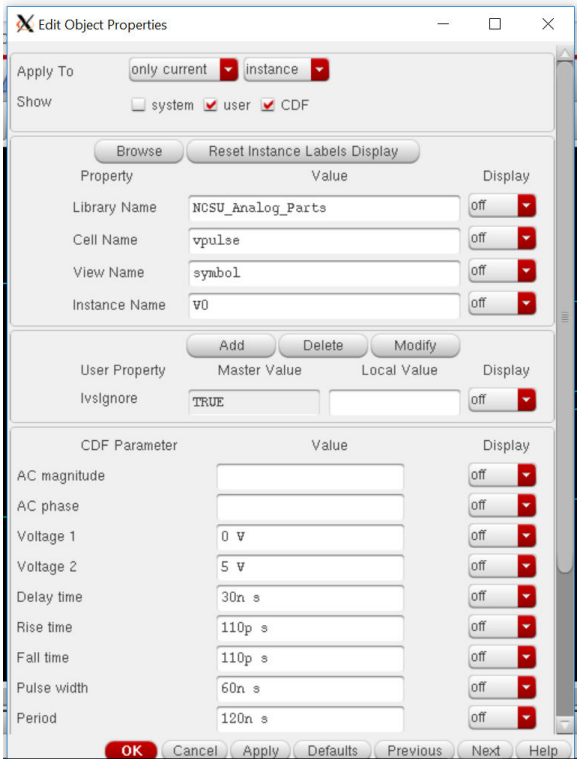


Fig.: Input Attributes of 'D' Flip-Flop

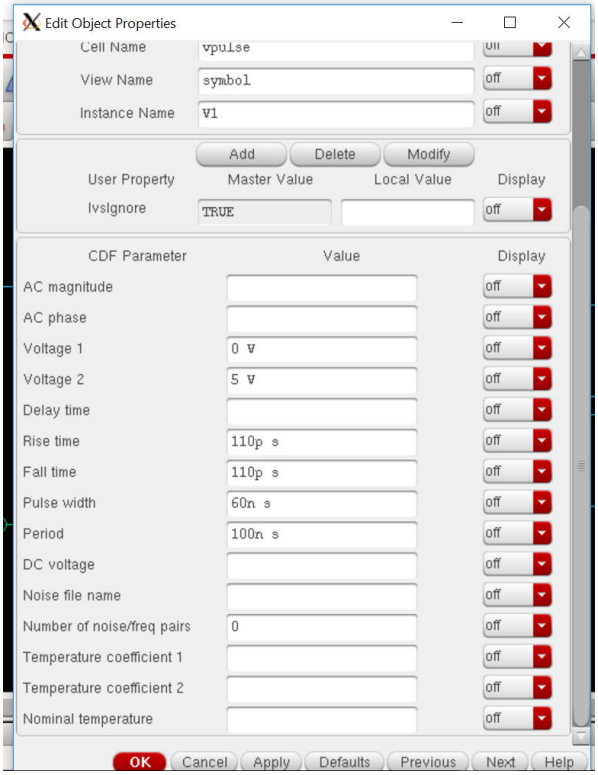


Fig.: Clock Attributes of 'D' Flip-Flop

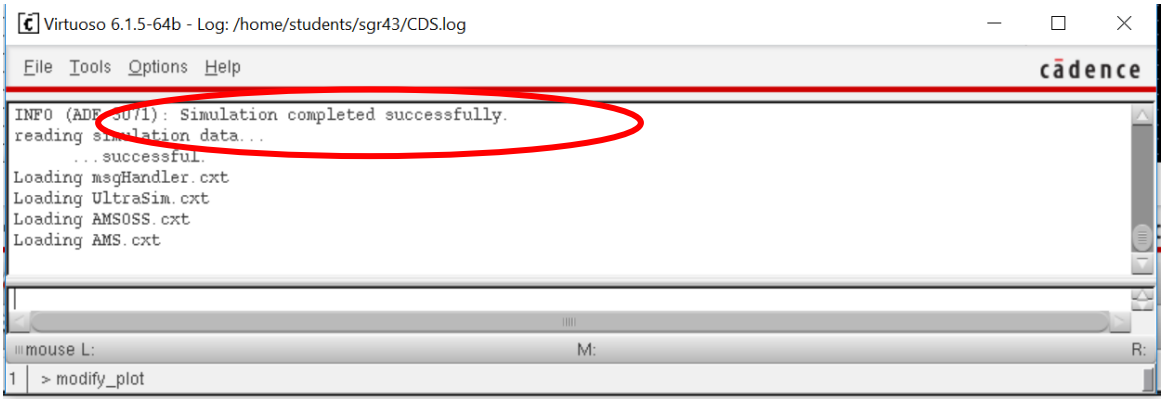


Fig.: Simulation Check of Schematic

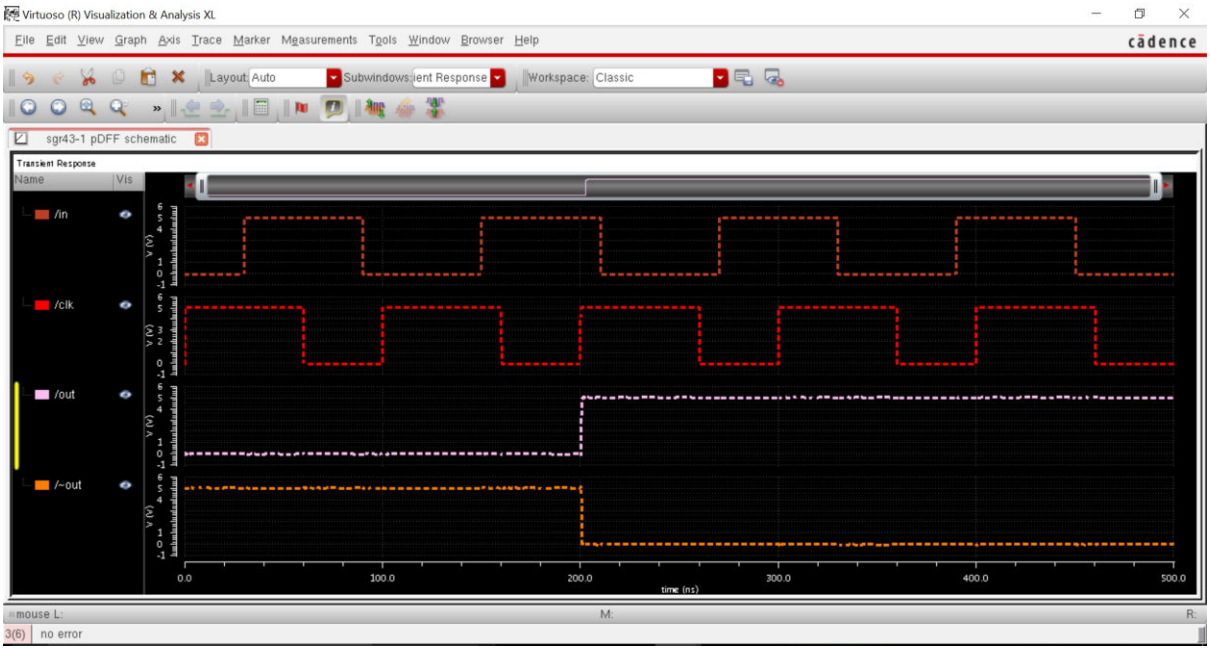


Fig.: Waveforms of 'D' Flip-Flop Schematic

3. SYMBOLIC SECTION OF ‘D’ FLIP-FLOP

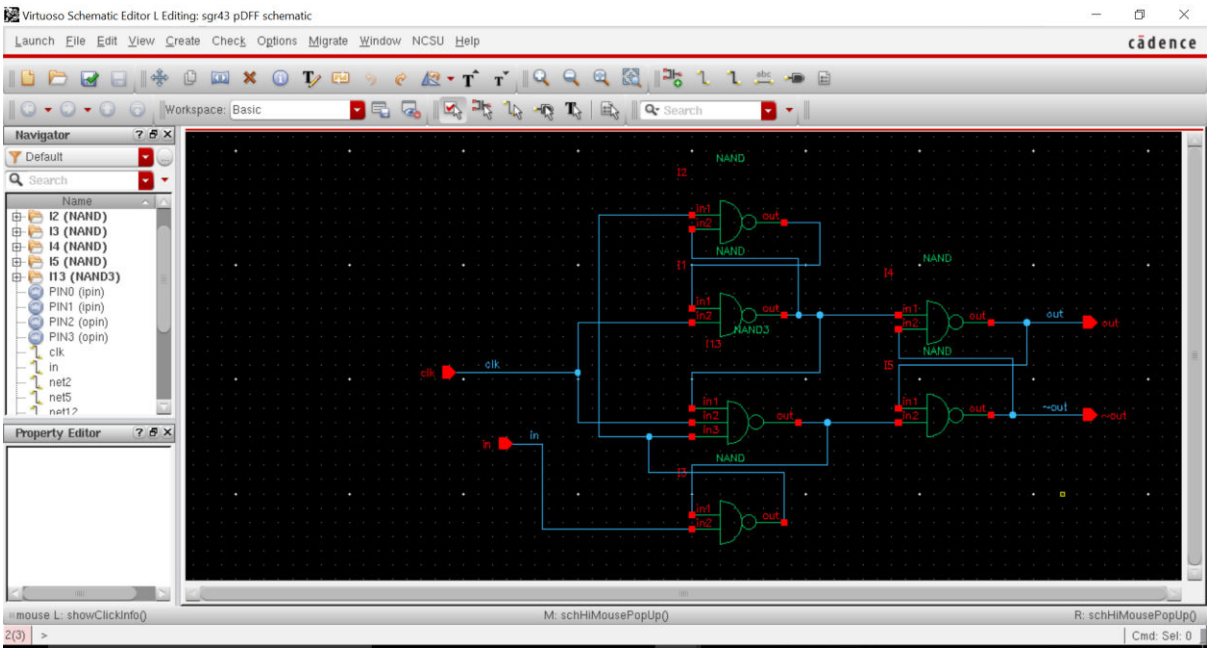


Fig.: Pinned Form of ‘D’ Flip-Flop

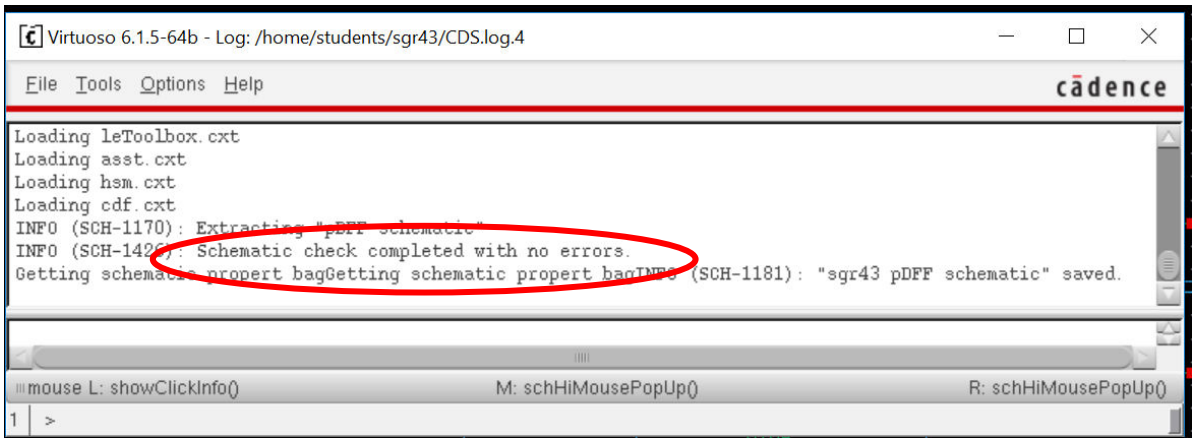


Fig.: Error Check of pinned form

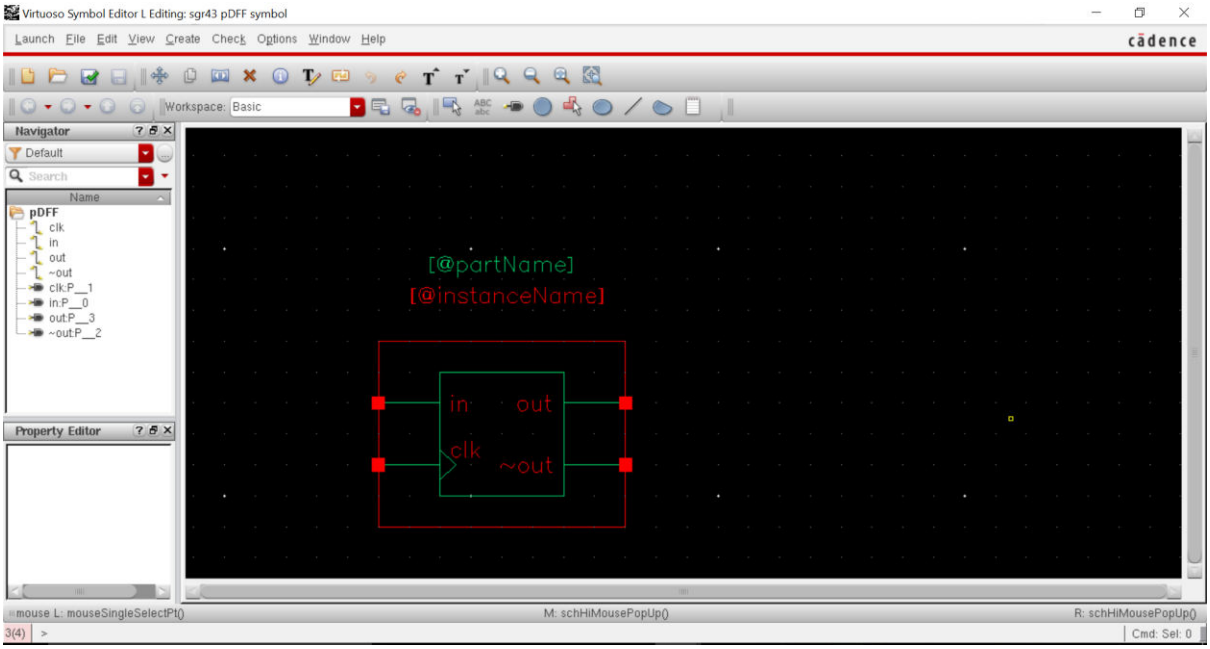


Fig.: Symbol of 'D' Flip-Flop

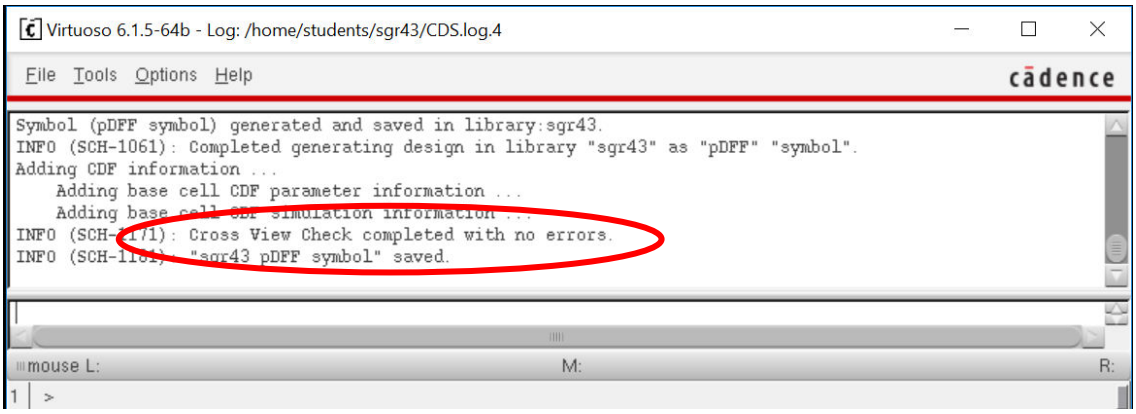


Fig.: Cross-view Check of 'D' Flip-Flop Symbol

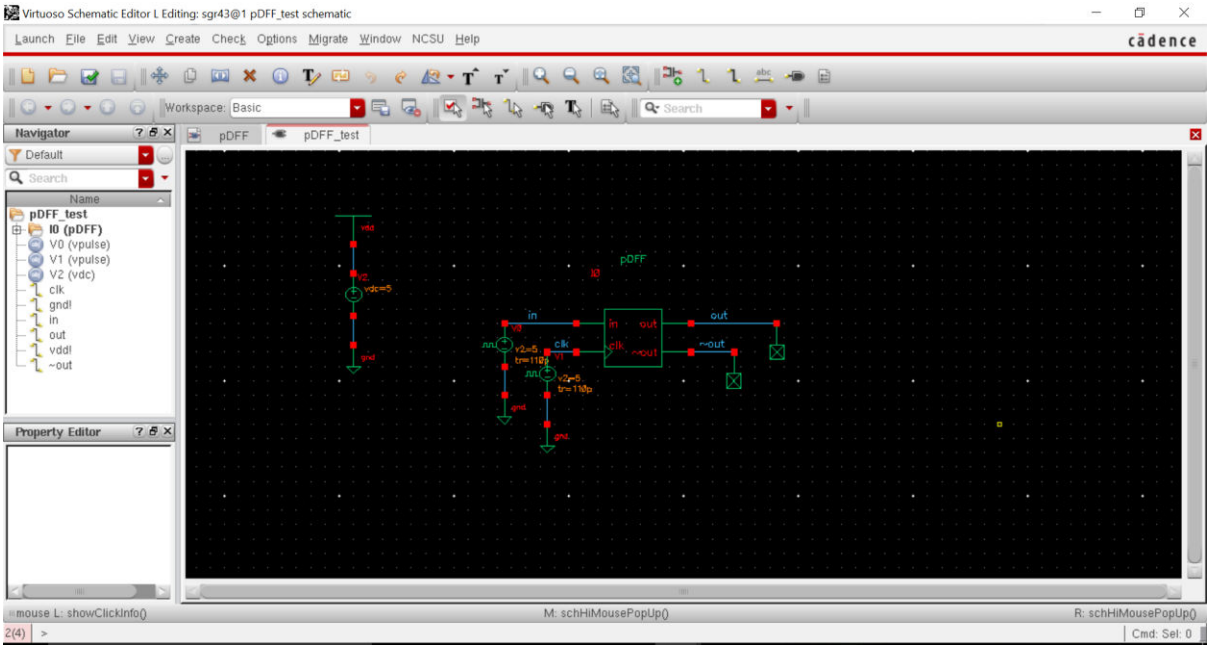


Fig.: Symbolic Representation of 'D' Flip-Flop Symbol

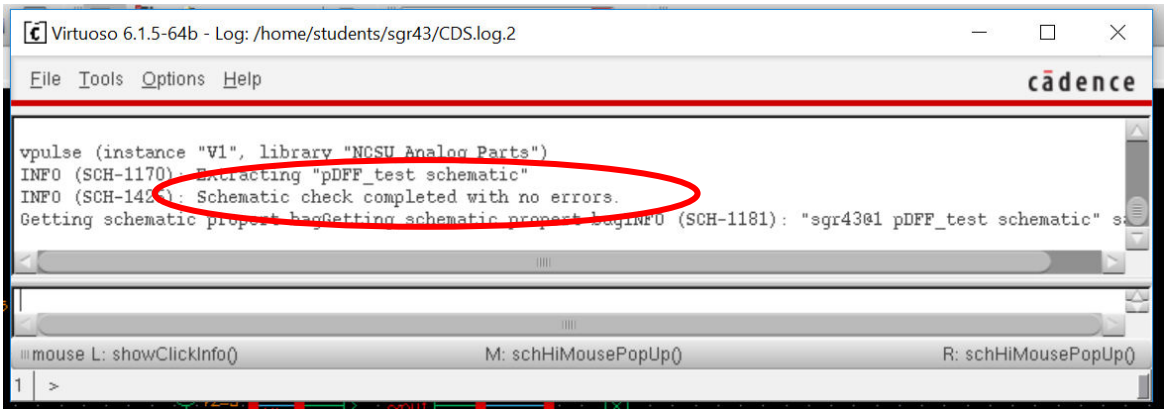


Fig.: Error Check of 'D' Flip-Flop Symbol

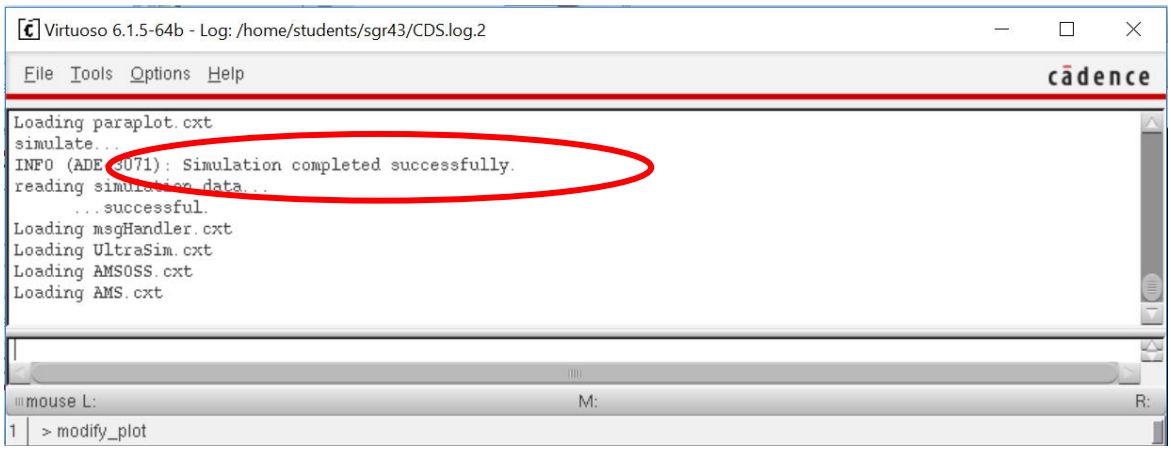


Fig.: Simulation Check of 'D' Flip-Flop Symbol

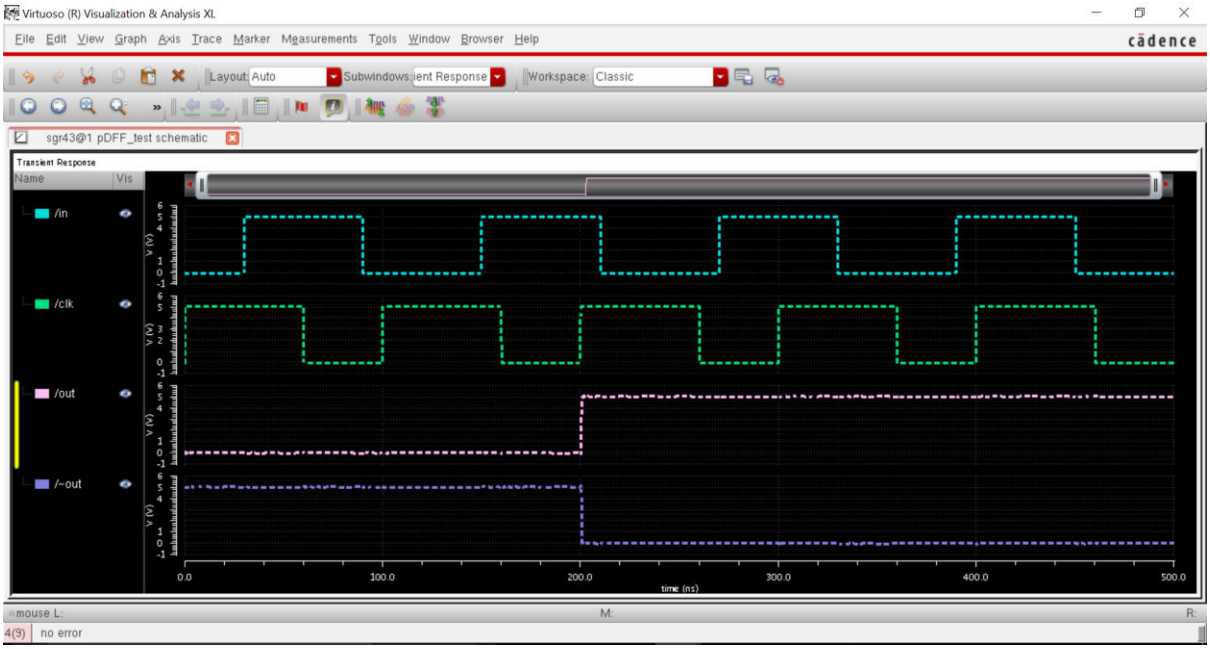


Fig.: Waveforms of ‘D’ Flip-Flop Symbol

4. LAYOUT SECTION OF ‘D’ FLIP-FLOP

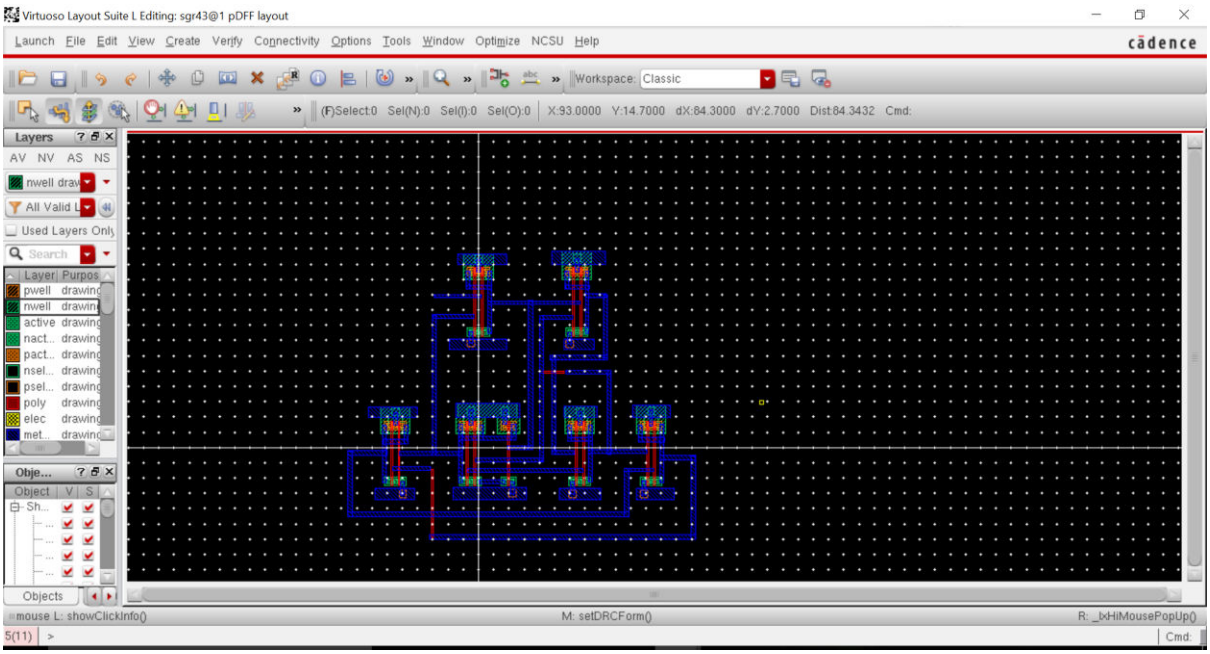


Fig.: Layout of ‘D’ Flip-Flop

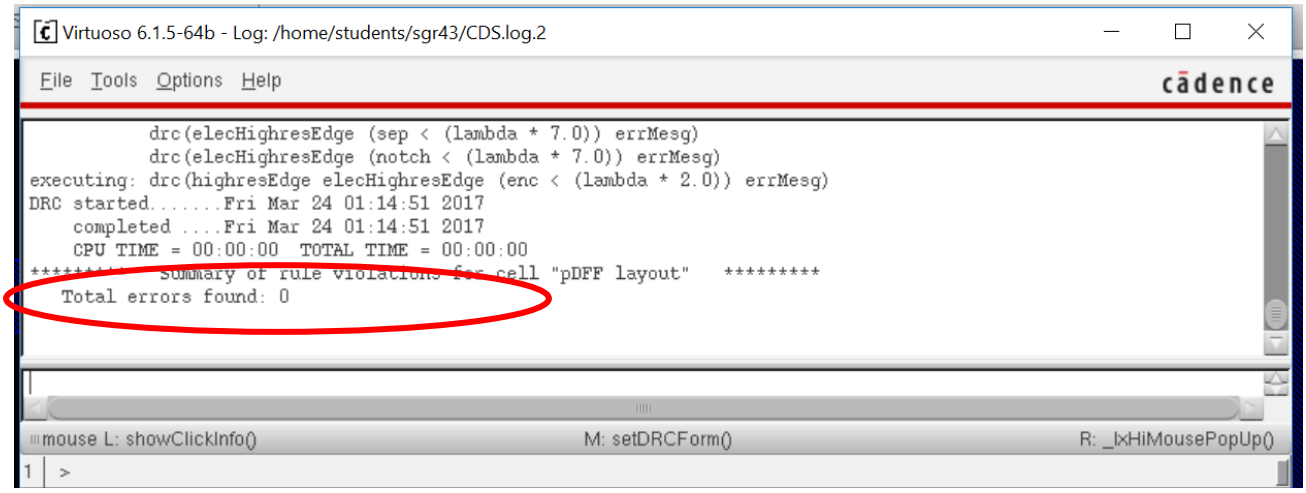


Fig.: Error Check of ‘D’ Flip-Flop

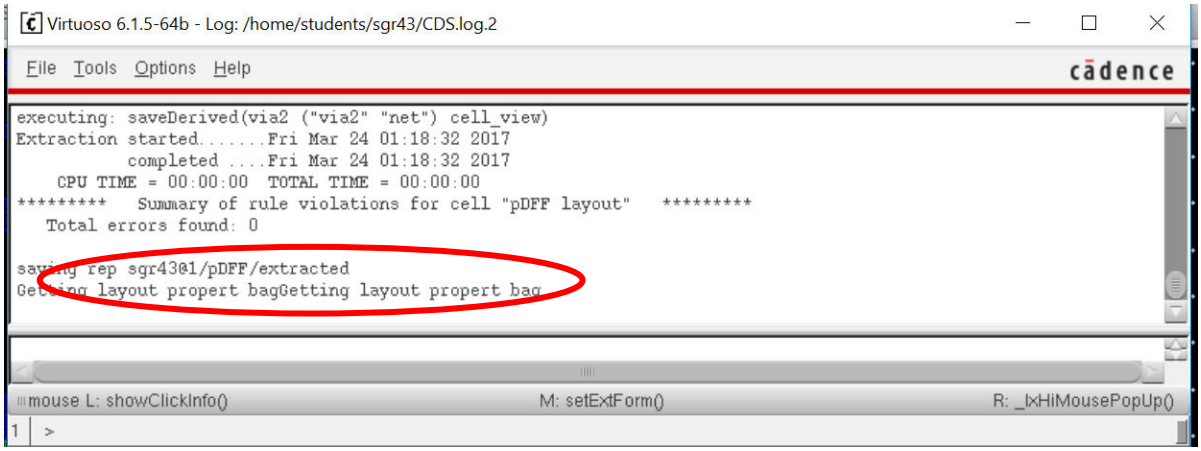


Fig.: Extraction Message of Layout

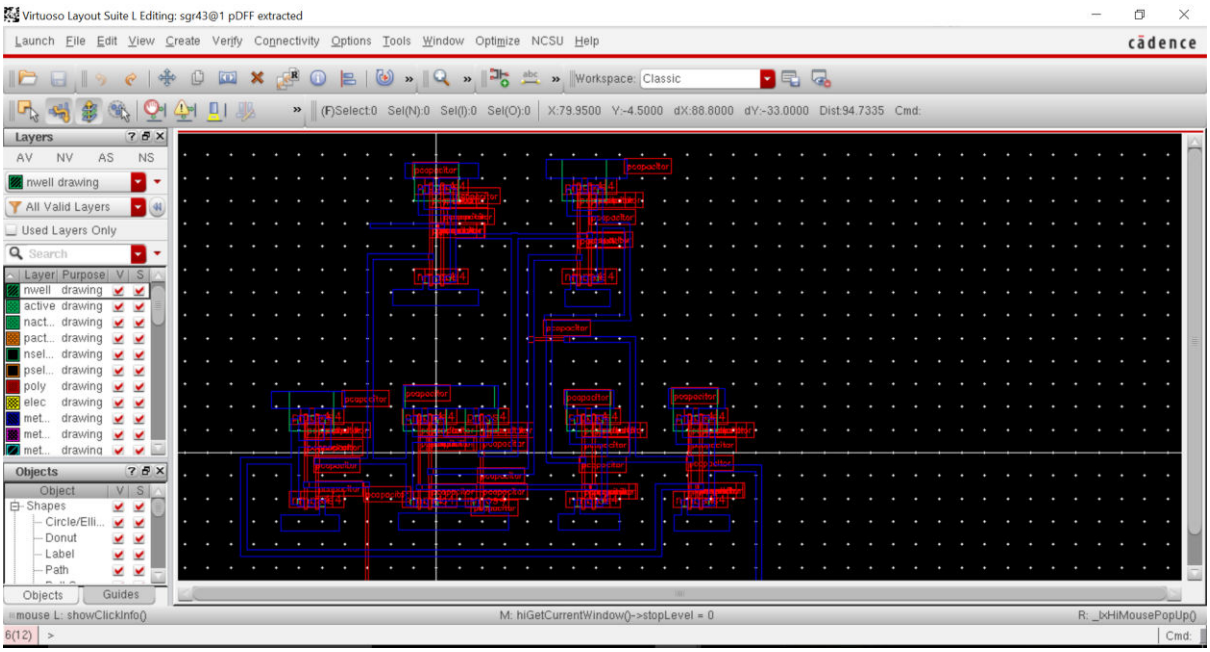


Fig.: Extracted Form of Layout

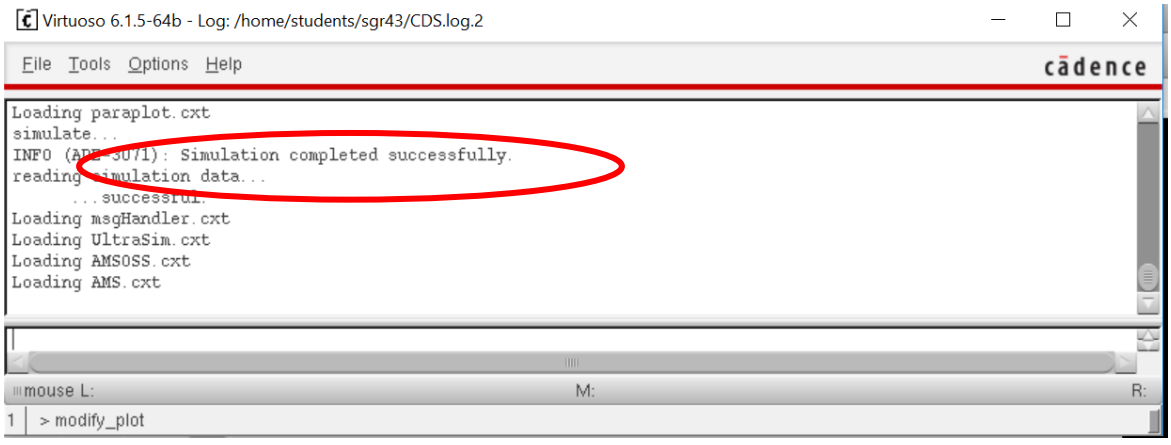


Fig.: Simulation Check of Layout

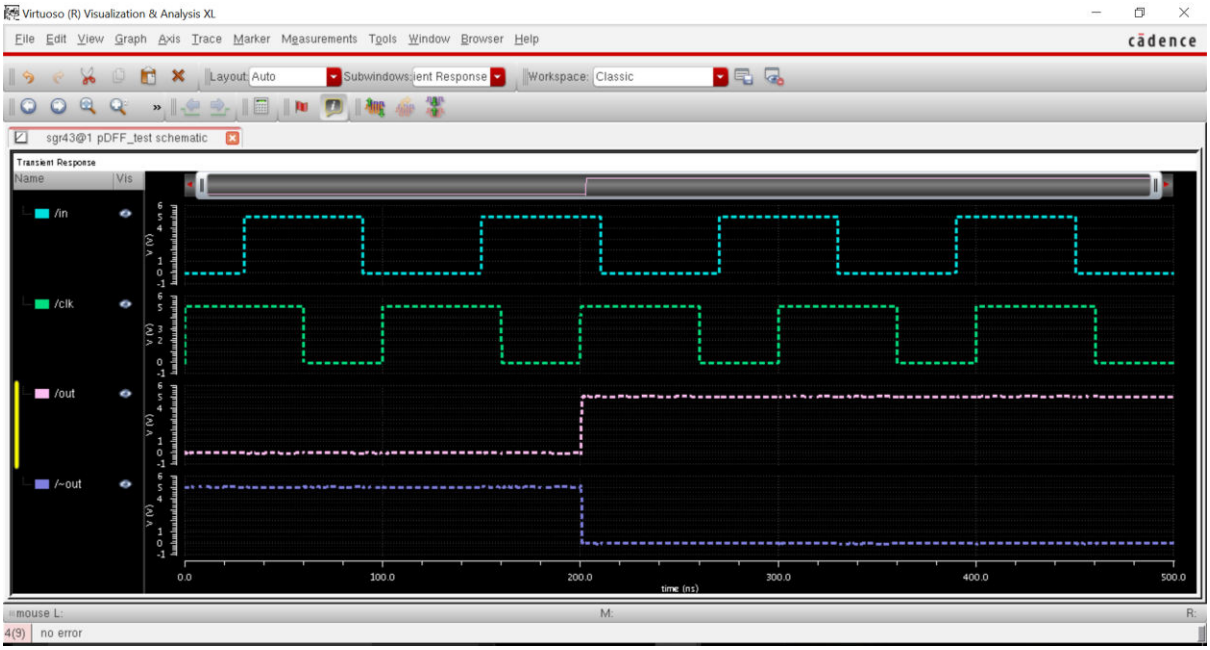


Fig.: Waveforms of Layout

5. FREQUENCY CONSTRAINTS

The frequency considered in this project is 100 GHz. After experimenting with various frequency values, this value is considered apt for the input attributes which has been mentioned above.

6. APPLICATIONS OF D FLIP-FLOP

These flip-flops can be used in many digital electronic circuits as:

- Registers
- Counters
- Event Detectors
- Data Synchronizers
- Frequency Dividers