

INTRODUCTION TO VLSI DESIGN

PROJECT – I

SPRING 2017

Submitted by:

Sri Sai Anusha Gandu

Student ID: 16230560

CONTENTS

TITLE	Pg. No.
1. Introduction	1
2. Implementation of NOT Gate	2
2.1 Schematic Section of NOT Gate	3
2.2 Symbolic Section of NOT Gate	4
2.3 Layout Section of NOT Gate	7
3. Implementation of AND Gate	9
2.1 Schematic Section of AND Gate	10
2.2 Symbolic Section of AND Gate	11
2.3 Layout Section of AND Gate	14
4. Implementation of OR Gate	16
2.1 Schematic Section of OR Gate	17
2.2 Symbolic Section of OR Gate	18
2.3 Layout Section of OR Gate	21
5. Implementation of XOR Gate	23
2.1 Schematic Section of XOR Gate	24
2.2 Symbolic Section of XOR Gate	25
2.3 Layout Section of XOR Gate	28
6. Implementation of NAND Gate	30
2.1 Schematic Section of NAND Gate	31
2.2 Symbolic Section of NAND Gate	32
2.3 Layout Section of NAND Gate	35

1. INTRODUCTION

Cadence is one of the most popular, efficient and commercial custom IC design tool. There are some sequential steps that we have to follow strictly for fruitful IC design. These steps are mentioned below-

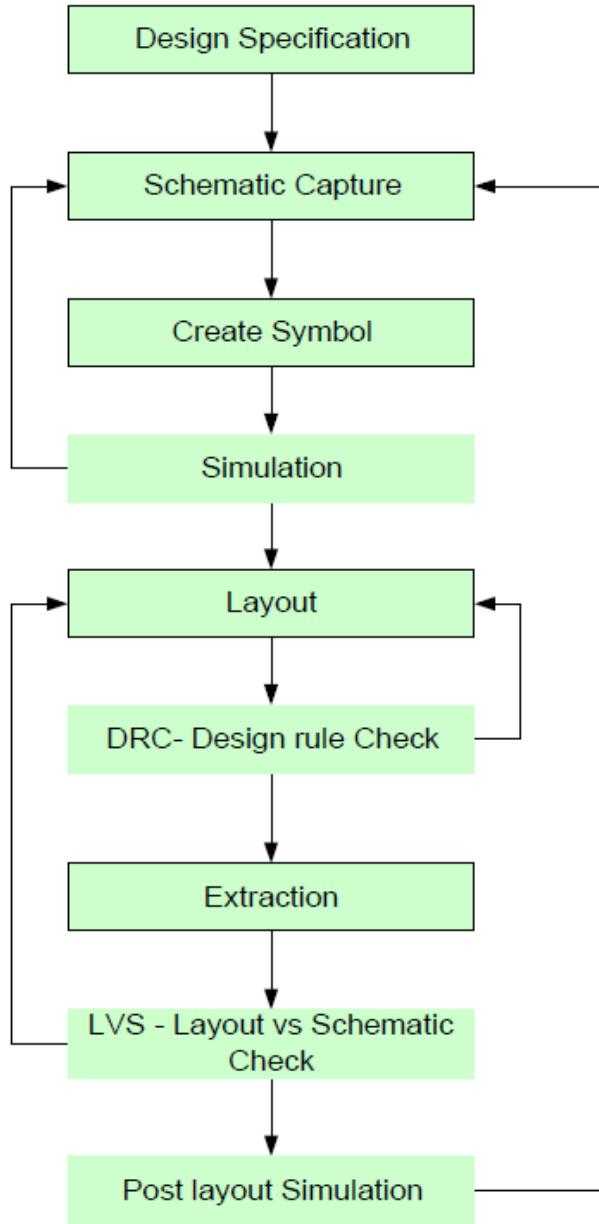


Figure 1: Flowchart of design steps

2. Implementation of NOT Gate

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. The truth table is shown below.

Input	Output
A	NOT A
0	1
1	0

The symbol of a NOT Gate is shown below.

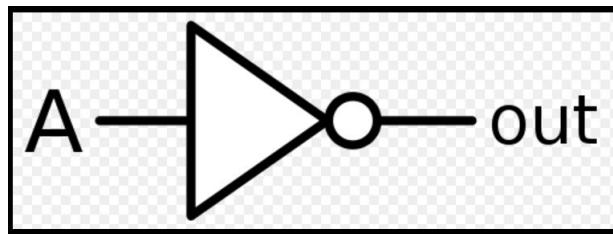


Fig.: Symbol of NOT Gate

The static CMOS circuit is shown below.

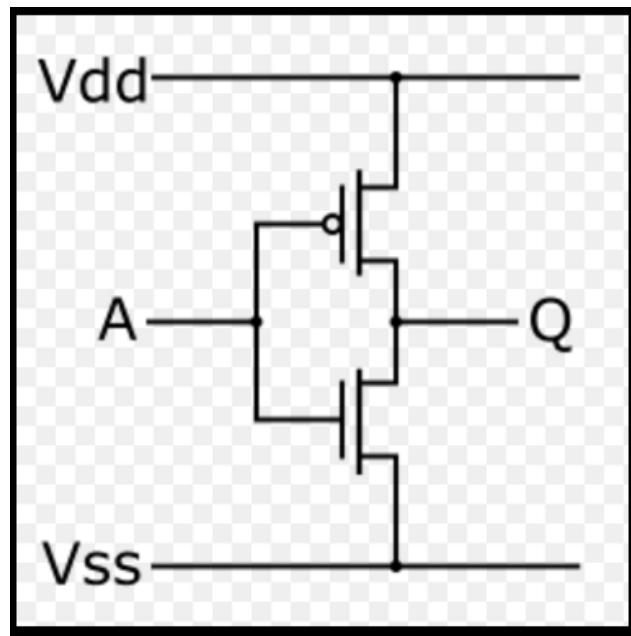


Fig.: Static CMOS circuit of NOT Gate

2.1 Schematic Section of NOT Gate

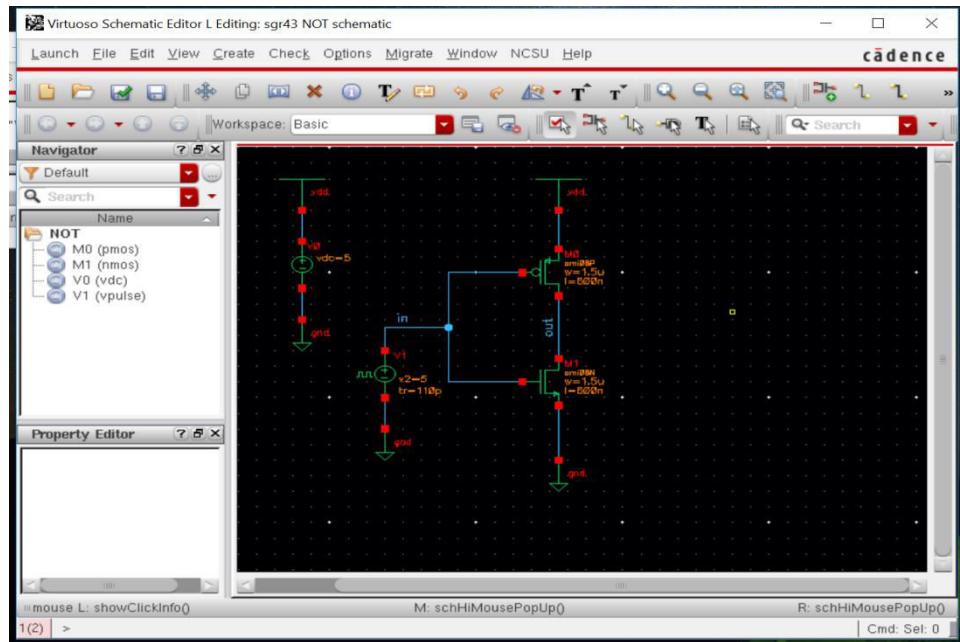


Fig.: Schematic of NOT Gate

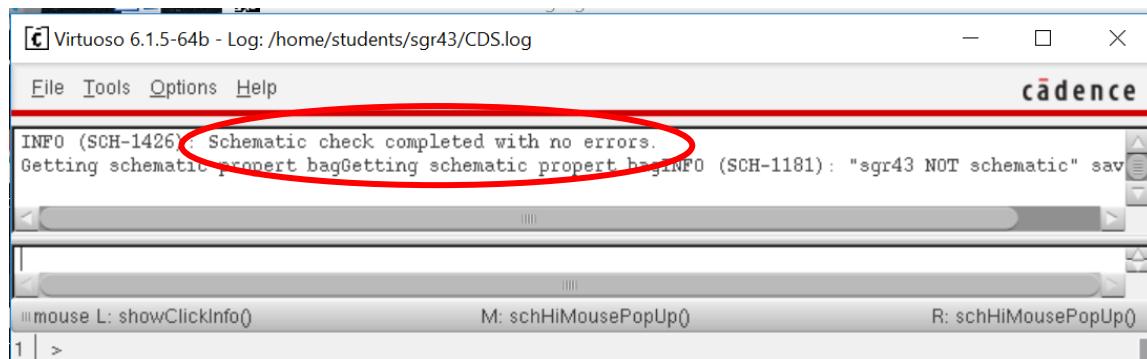


Fig.: Error Check of Schematic

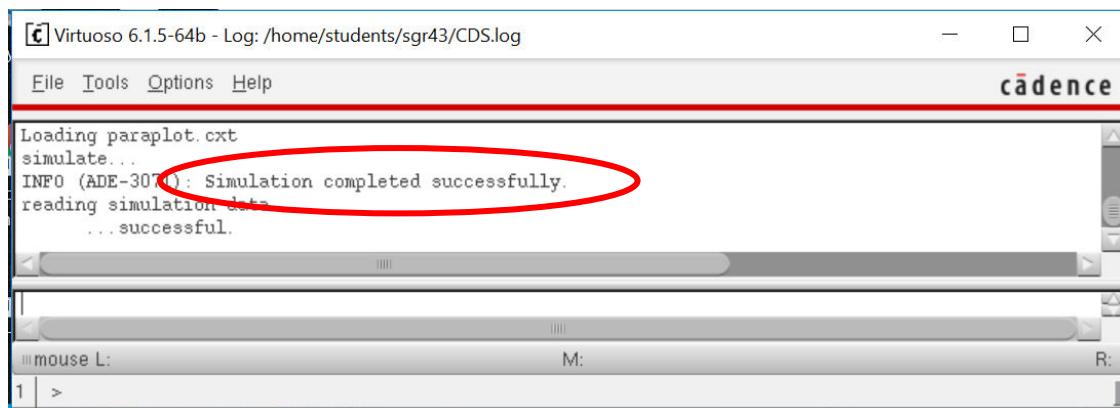


Fig.: Simulation Check of Schematic



Fig.: Waveforms of NOT Schematic

2.2 Symbolic Section of NOT Gate

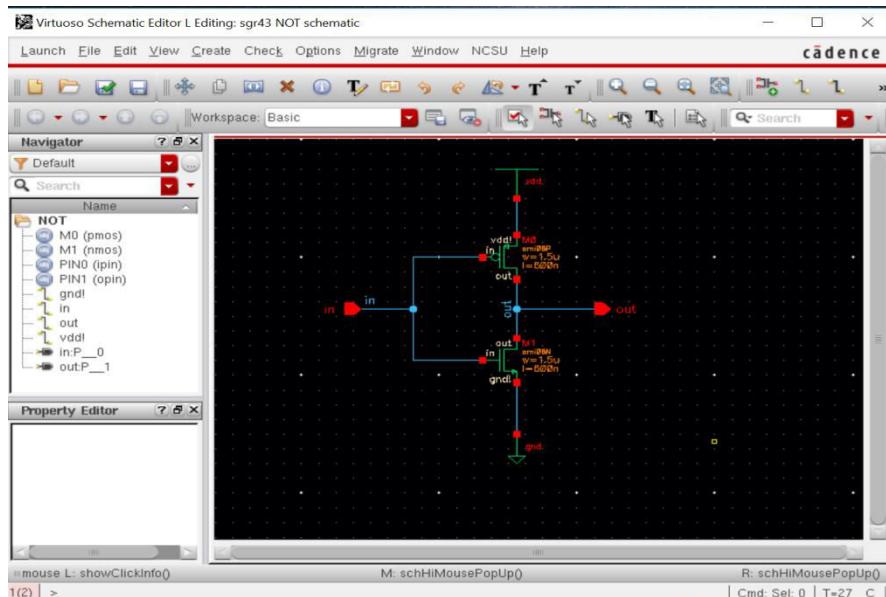


Fig.: Pinned Form of NOT Gate

```

[ Cadence Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log ]
[ File Tools Options Help ]
[ INFO (SCH-1170): Executing NOT schematic ]
[ INFO (SCH-1176): Schematic check completed with no errors. ]
[ Getting schematic property bagINFO (SCH-1181): "sgr43 NOT schematic" saved ]

```

Fig.: Error Check of pinned form

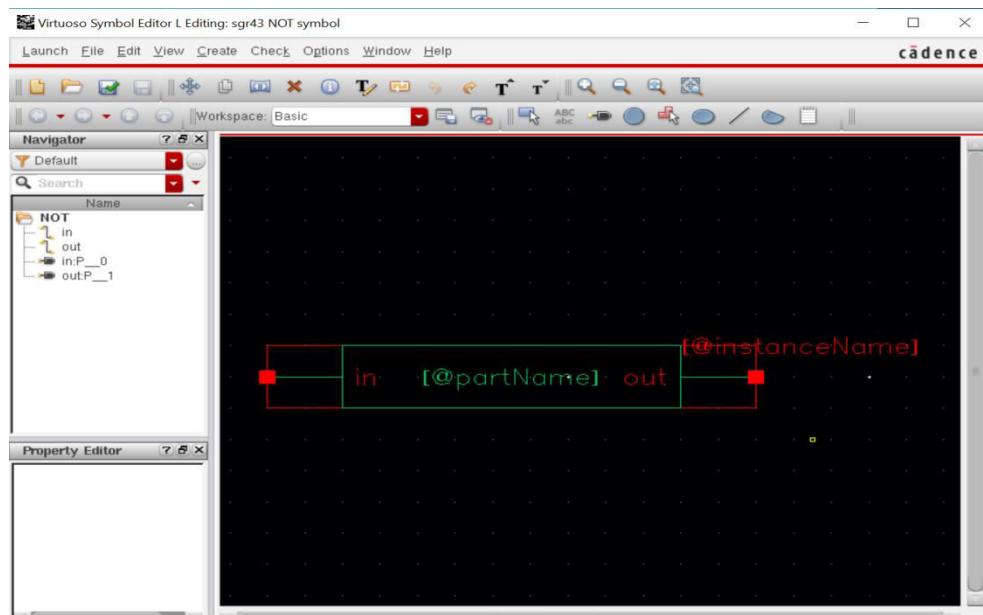


Fig.: Extracted Form of NOT Gate

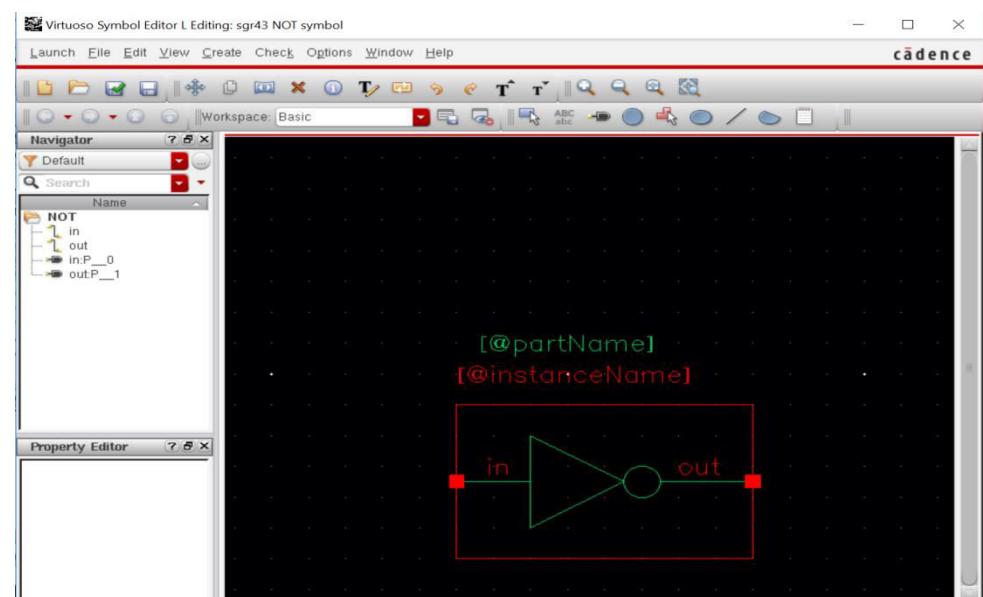


Fig.: Symbol of NOT Gate

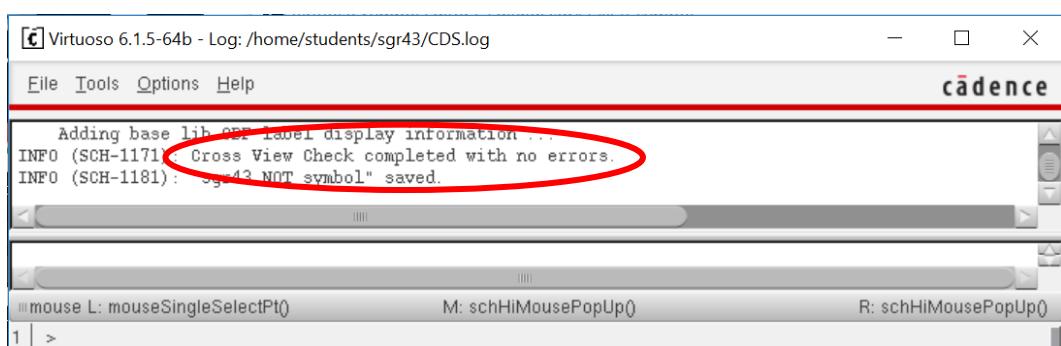


Fig.: Cross-view Check of NOT Symbol

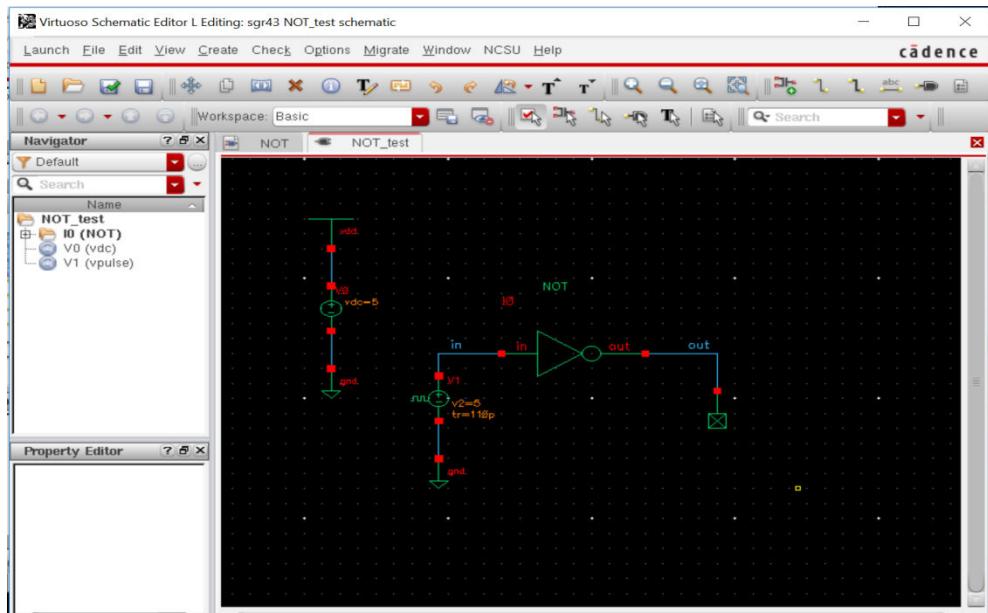


Fig.: Symbolic Representation of NOT Gate

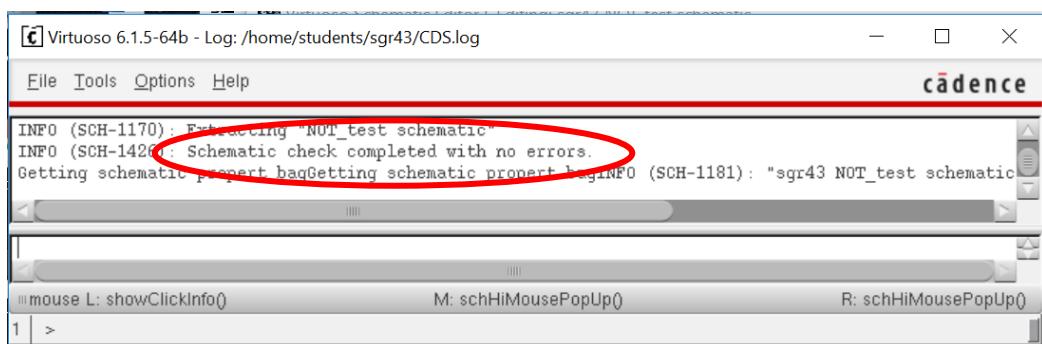


Fig.: Error Check of NOT Symbol



Fig.: Waveforms of NOT Symbol

2.3 Layout Section of NOT Gate

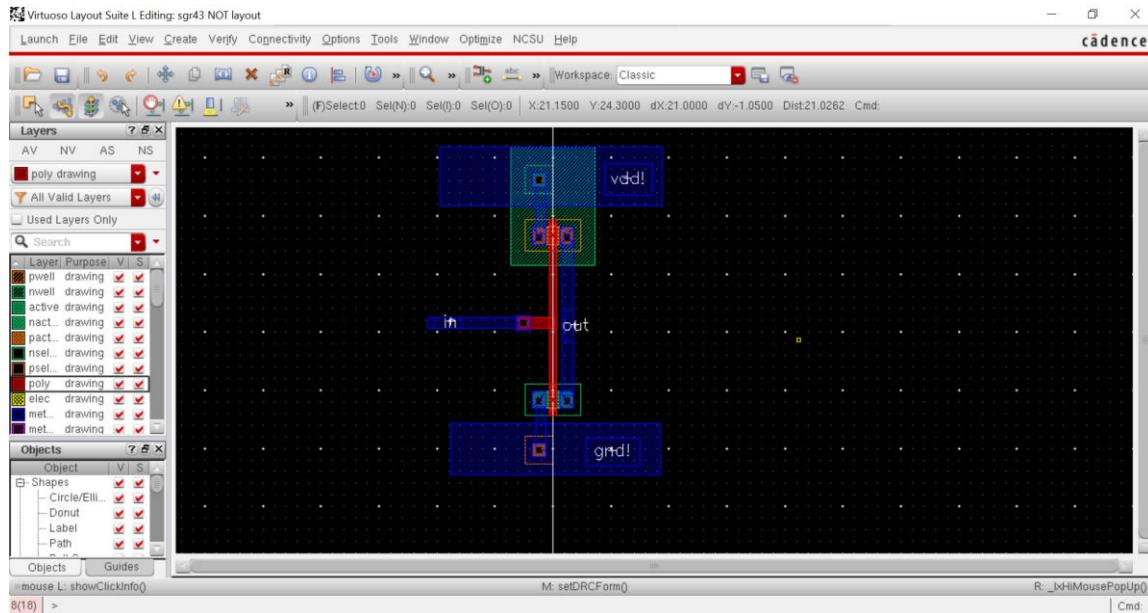


Fig.: Layout of NOT Gate

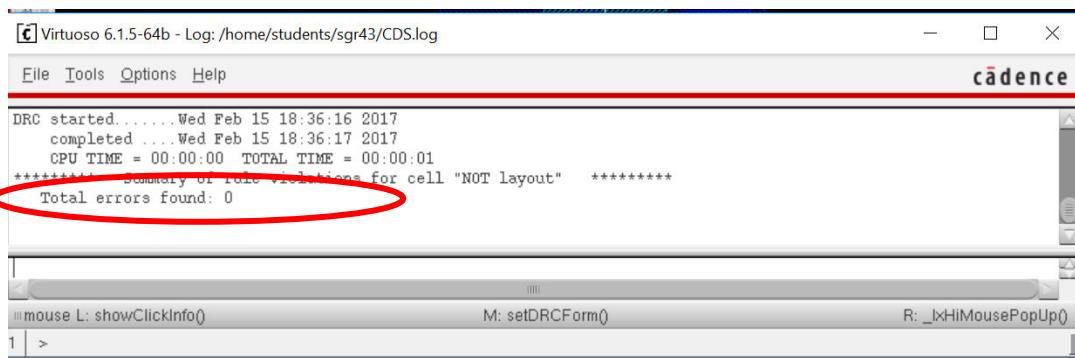


Fig.: Error Check of NOT Layout

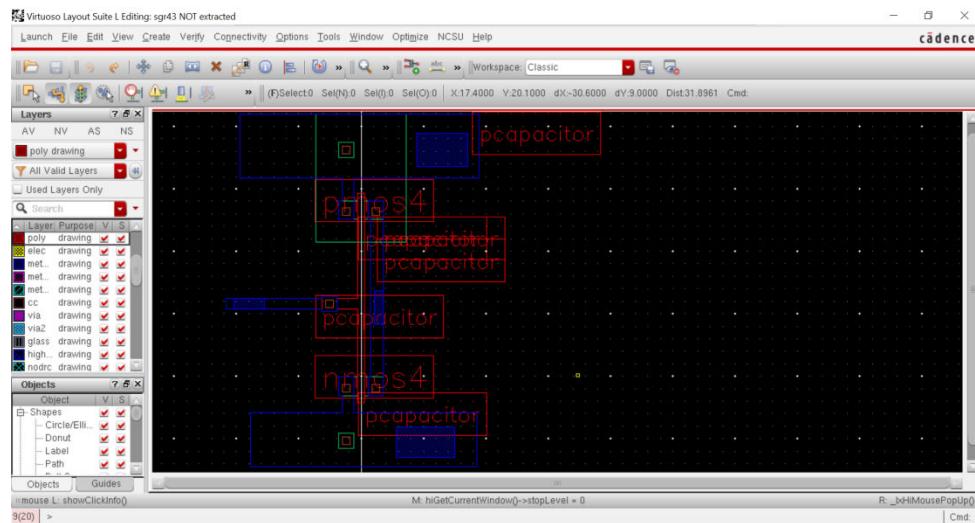


Fig.: Extracted Form of NOT Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log

***** Summary of rule violations for cell "NOT layout" *****
Total errors found: 0
saving rep sgr43/NOT/extracted
Getting layout prop bagGetting layout property bag

mouse L: showClickInfo() M: setExtForm() R: _lxHiMousePopUp()

Fig.: Extraction Message of NOT Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log

File Tools Options Help

start simulator if needed...
...successful.
simulate
INFO (AE-3071): Simulation completed successfully.
reading simulation data...
...successful.

mouse L: M: R:

Fig.: Simulation Check of Layout

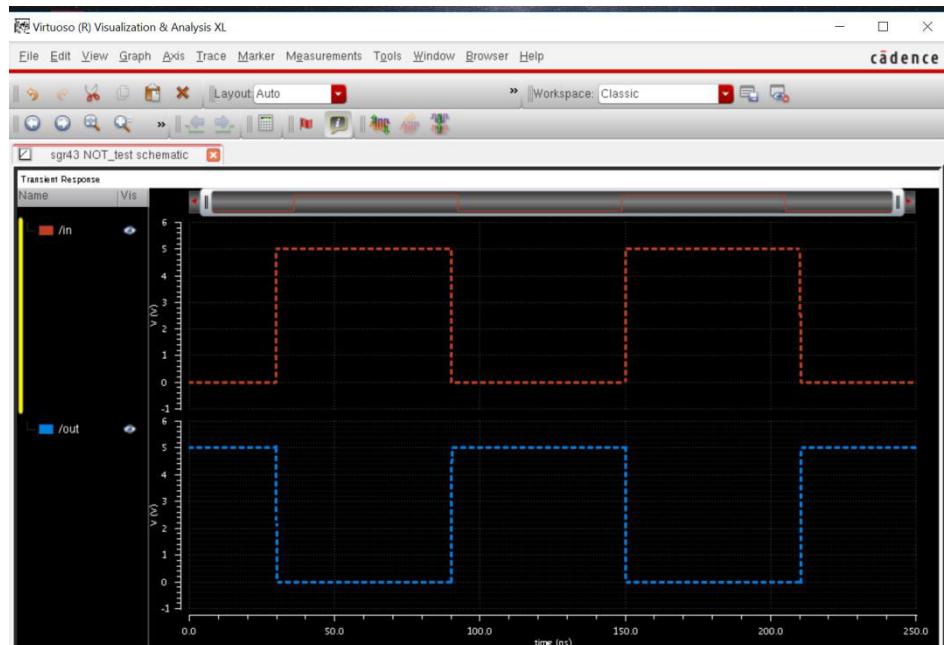


Fig.: Waveforms of NOT Layout

3. Implementation of AND Gate

The AND gate is a basic digital logic gate that implements logical conjunction. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. The truth table is shown below.

Input		Output
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

The symbol of an AND Gate is shown below.

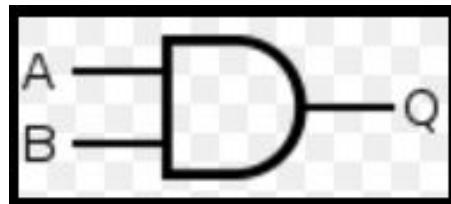


Fig.: Symbol of AND Gate

The static CMOS circuit is shown below.

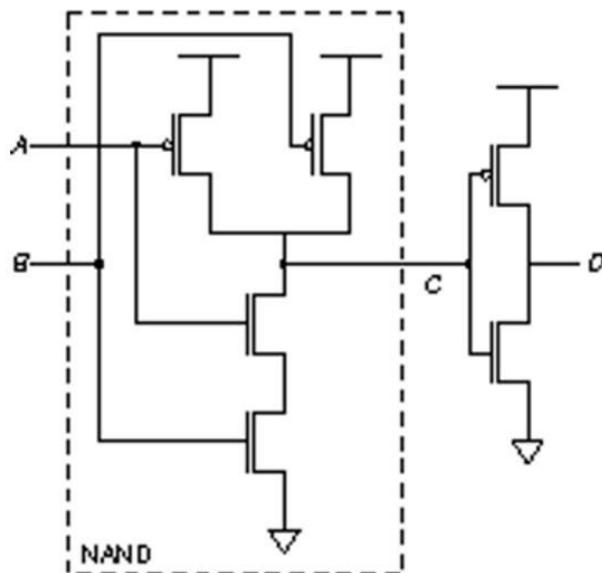


Fig.: Static CMOS circuit of AND Gate

3.1 Schematic Section of AND Gate

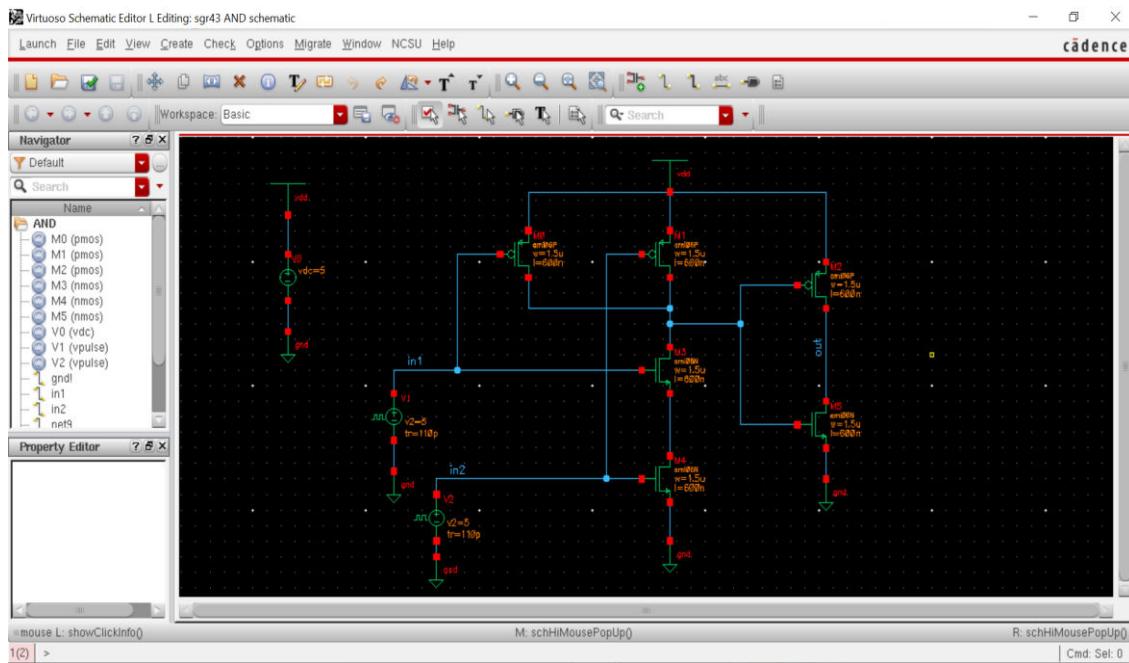


Fig.: Schematic of AND Gate

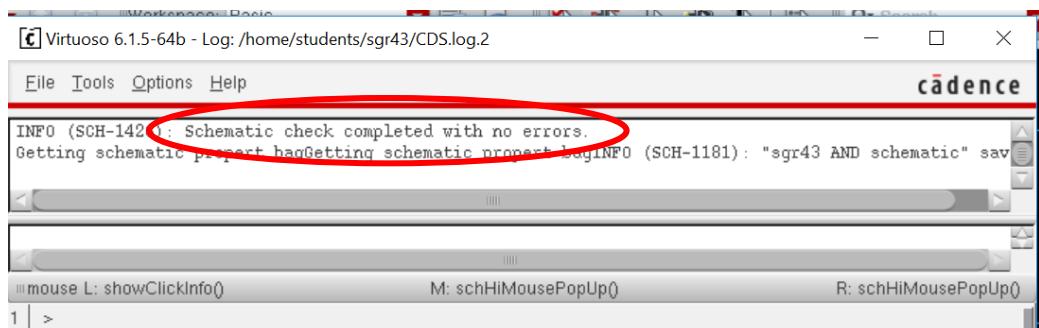


Fig.: Error Check of Schematic

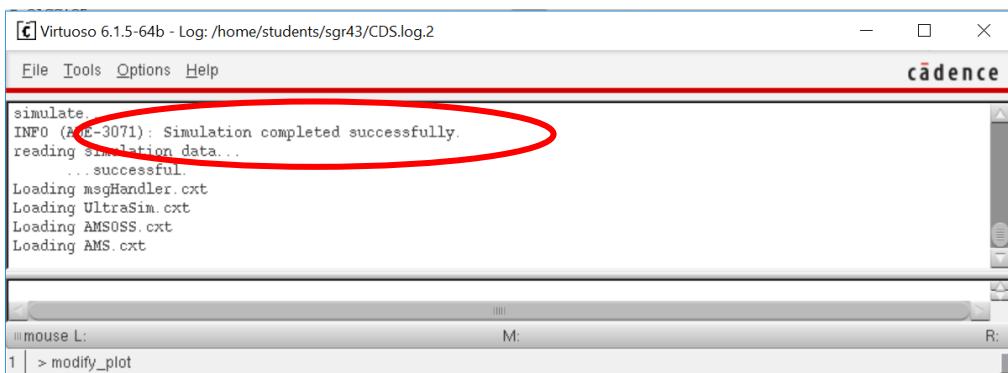


Fig.: Simulation Check of Schematic

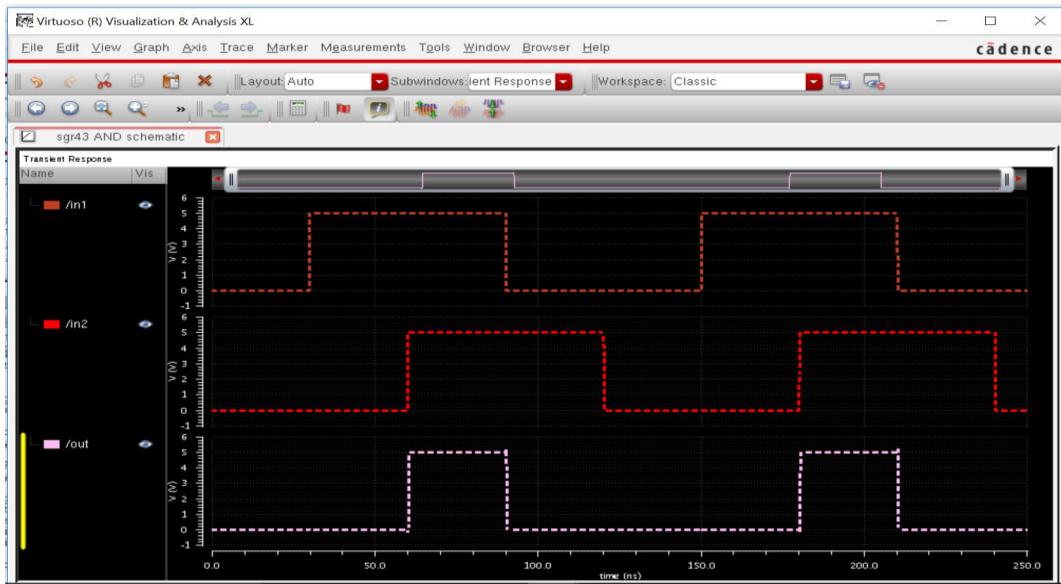


Fig.: Waveforms of AND Schematic

2.2 Symbolic Section of AND Gate

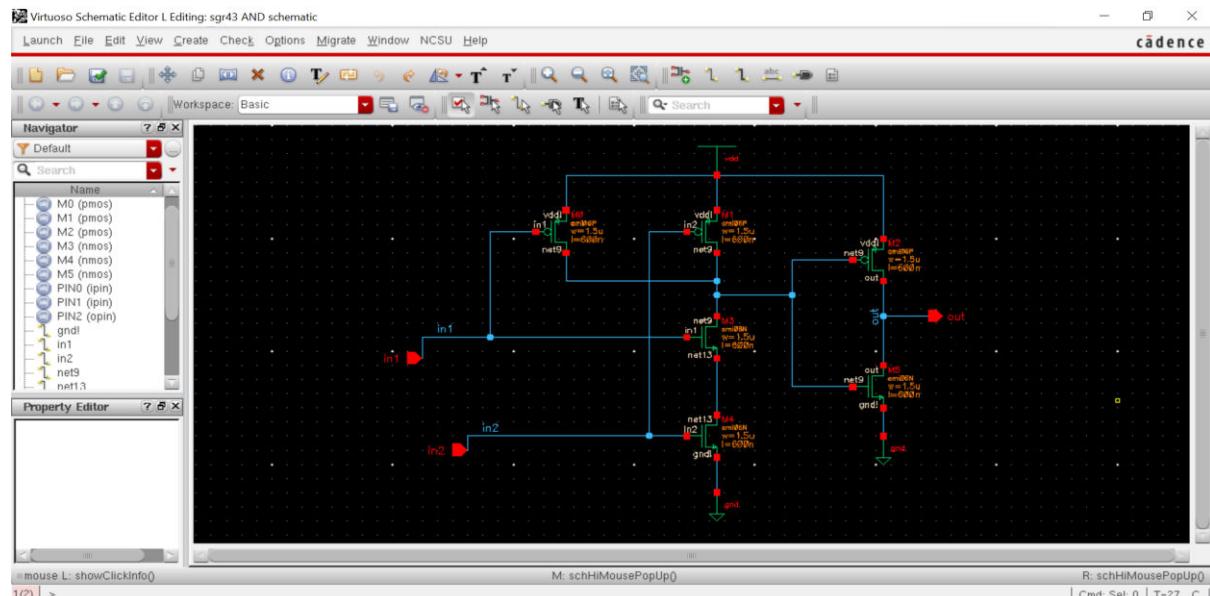


Fig.: Pinned Form of AND Gate

```
Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
*c Error* hiCloseWindow: argument #1 should be a window type (type template = "w") - nil
INFO (SCH-1170): Extracting "AND schematic"
INFO (SCH-1426): Schematic check completed with no errors.
Getting schematic property bagGetting schematic property bag (SCH-1181): "sgr43 AND schematic" saved.
```

Fig.: Error Check of pinned form

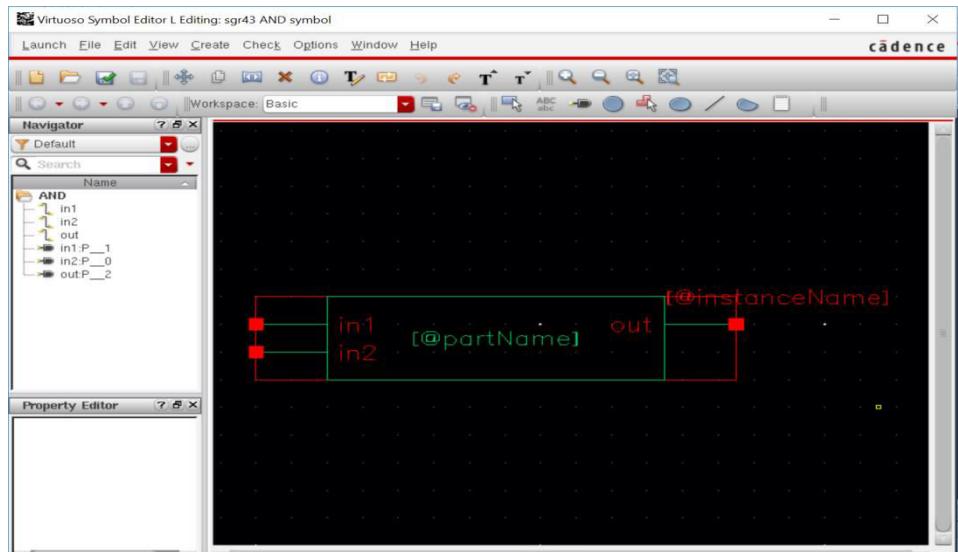


Fig.: Extracted Form of AND Gate

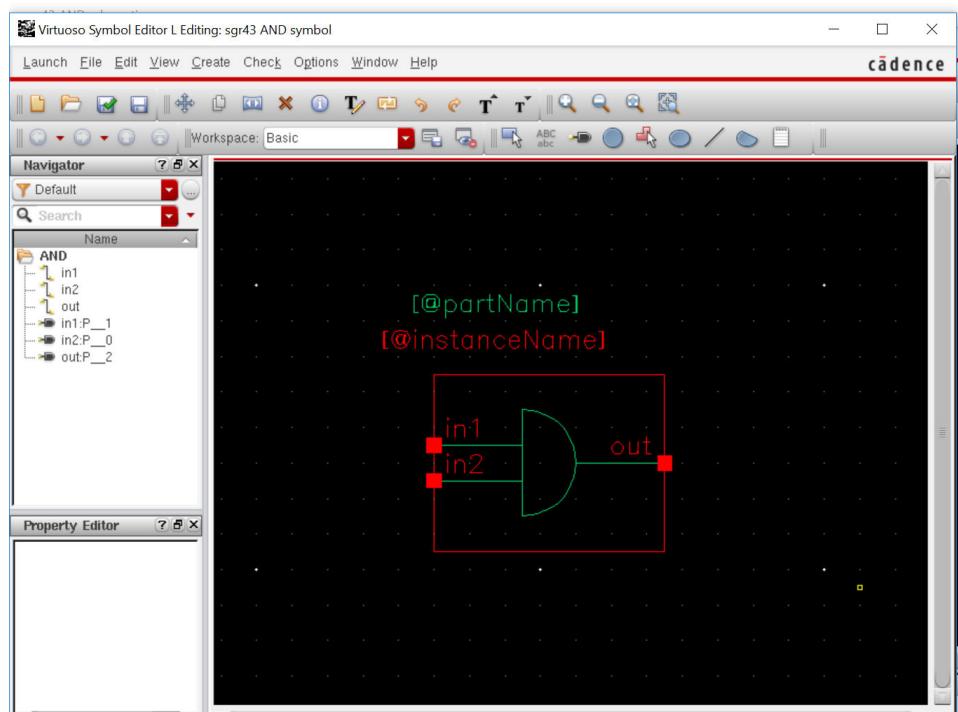


Fig.: Symbol of AND Gate

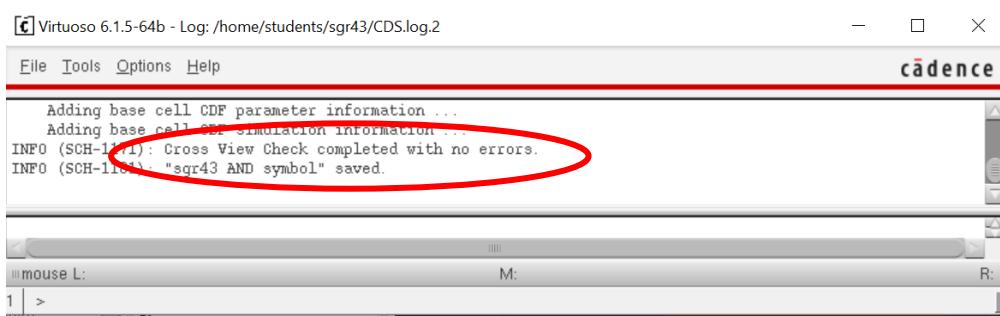


Fig.: Cross-view Check of AND Symbol

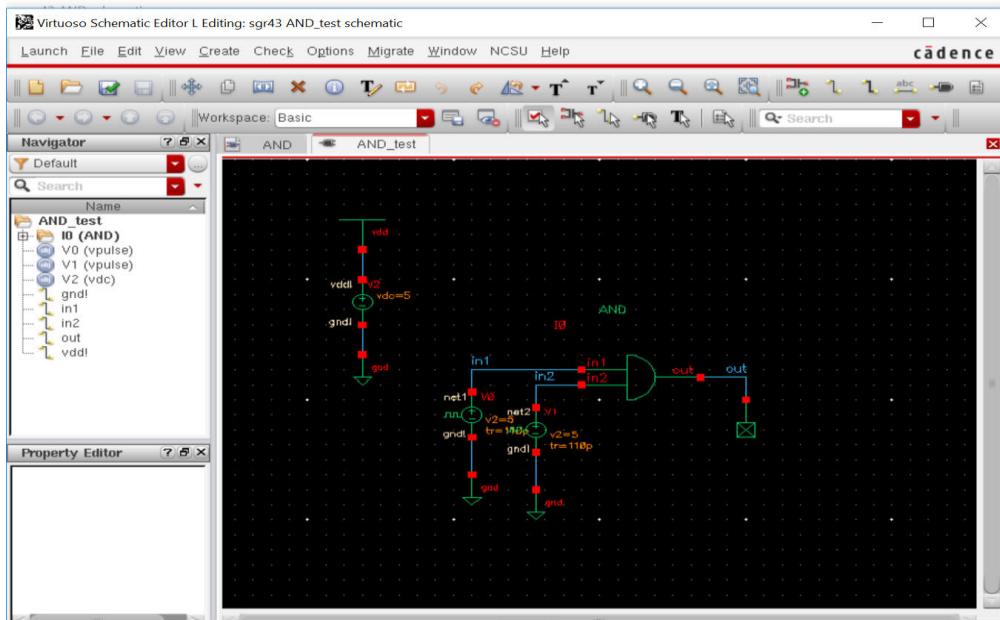


Fig.: Symbolic Representation of AND Gate

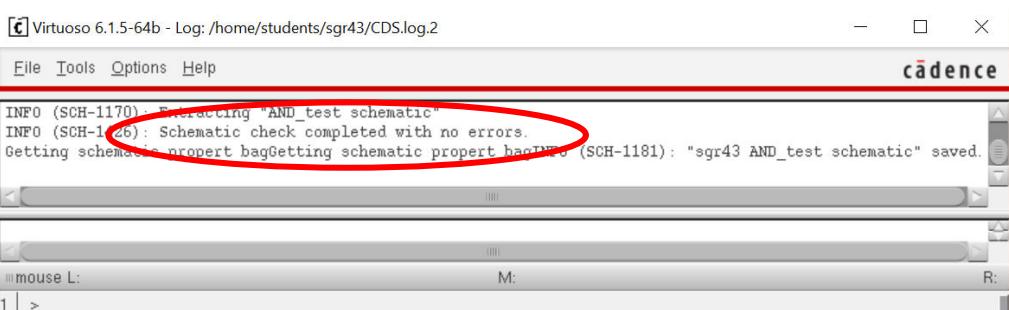


Fig.: Error Check of AND Symbol

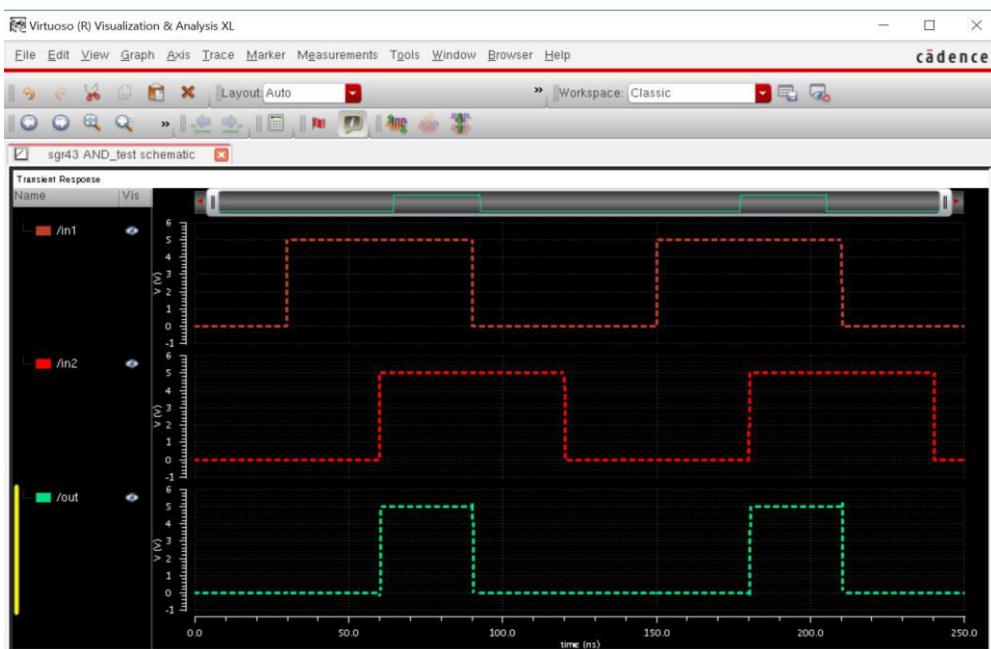


Fig.: Waveforms of AND Symbol

3.3 Layout Section of AND Gate

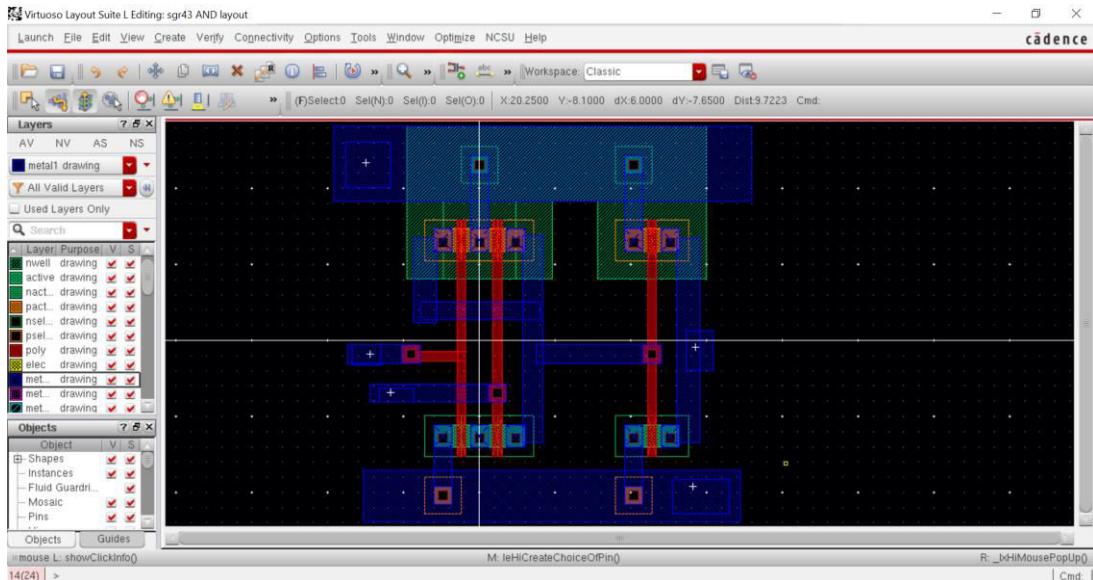


Fig.: Layout of AND Gate

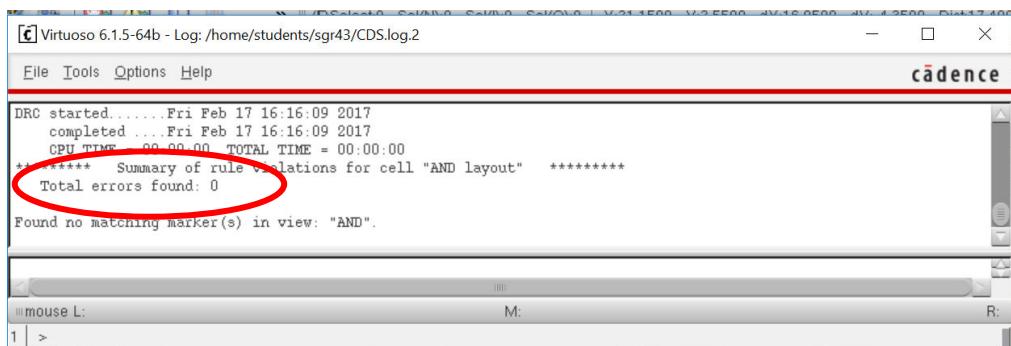


Fig.: Error Check of AND Gate

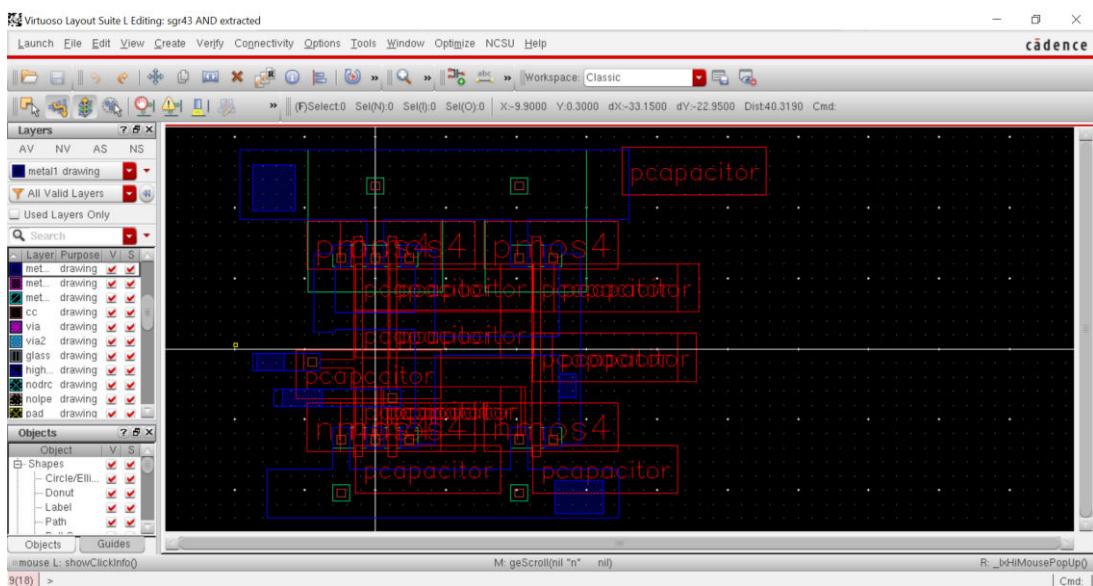


Fig.: Extracted Form of AND Layout

```

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
completed ... Fri Feb 17 16:17:22 2017
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "AND layout" *****
Total errors found: 0

saving rep sgr43/AND/extracted
getting layout property bagGetting layout property bag

mouse L: showClickInfo() M: setExitForm() R: _lxHiMousePopUp()
1 | >

```

Fig.: Extraction Message of AND Layout

```

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
... successful.
start simulator if needed...
... successful.
simulate...
INFO (ADE-3071): Simulation completed successfully.
reading simulation data...
... successful.

mouse L: M: R:
1 | > modify_plot

```

Fig.: Simulation Check of AND Layout



Fig.: Waveforms of AND Layout

4. Implementation of OR Gate

The OR gate is a digital logic gate that implements logical disjunction. A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results. The truth table is shown below.

Input		Output
A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

The symbol of OR Gate is shown below.

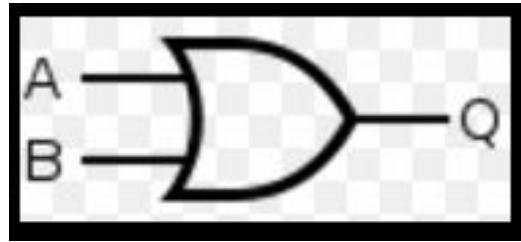


Fig.: Symbol of OR Gate

The static CMOS circuit of OR Gate is shown below.

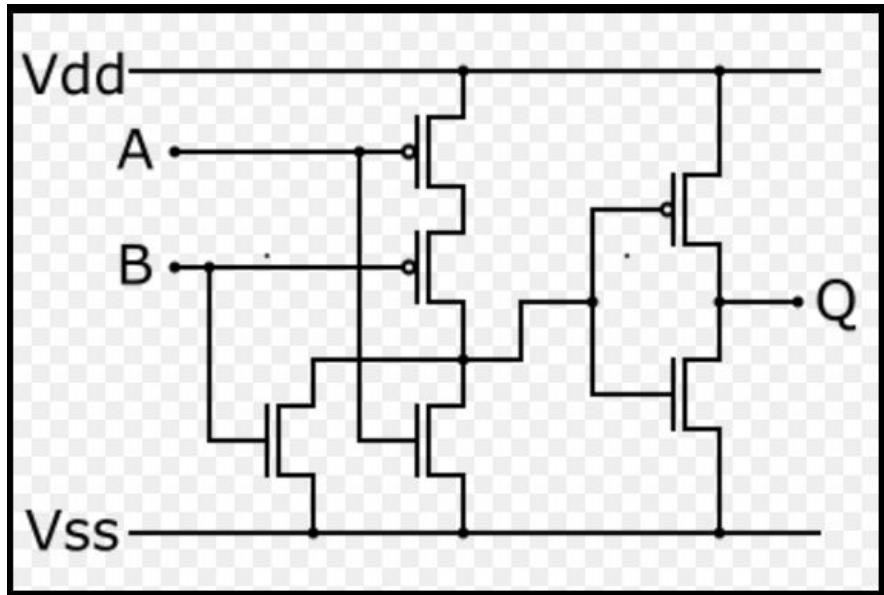


Fig.: Static CMOS circuit of OR Gate

3.1 Schematic Section of OR Gate

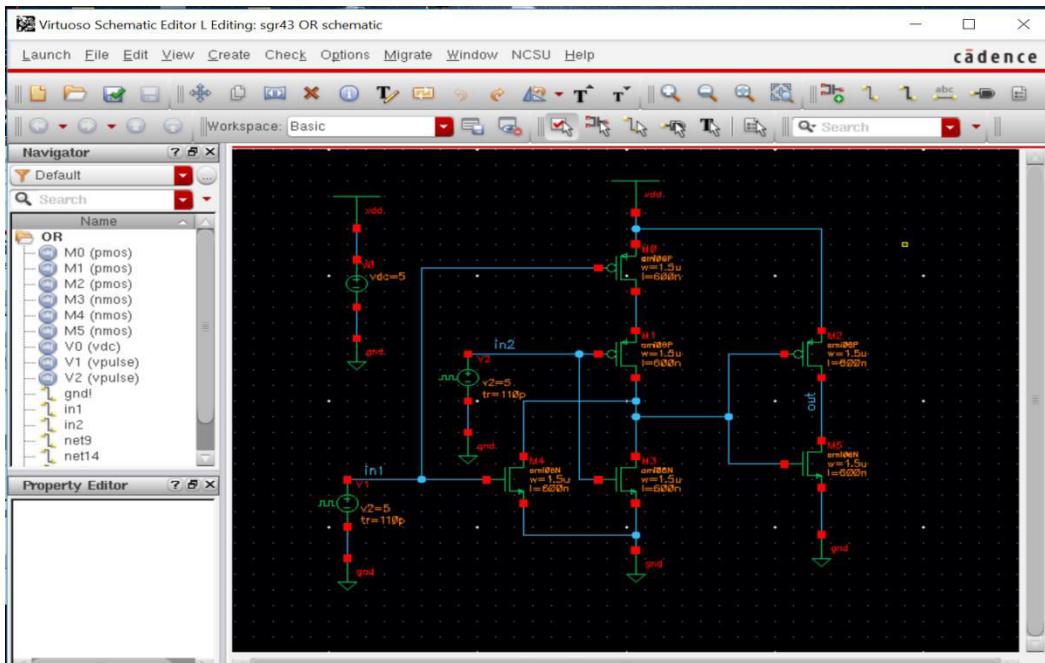


Fig.: Schematic of OR Gate

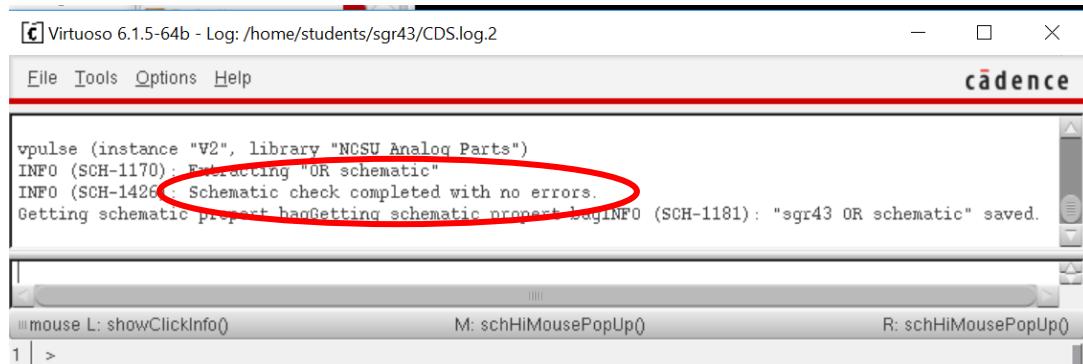


Fig.: Error Check of Schematic



Fig.: Simulation Check of Schematic



Fig.: Waveforms of OR Gate

3.2 Symbolic Section of OR Gate

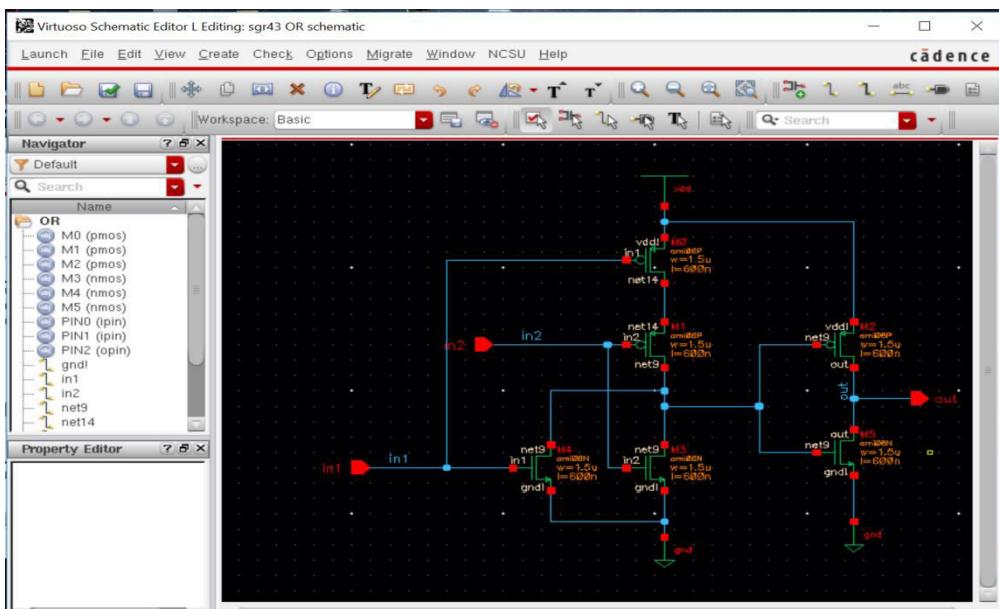


Fig.: Pinned Form of OR Gate

```
Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence

Trying to check out the license Virtuoso_Schematic_Editor_XL ("95115") instead.
+INFO* (iclic-25) License Virtuoso_Schematic_Editor_XL ("95115") was used to run Schematics L.
Getting schematic property bag
Getting schematic property bag
Getting schematic property bag
INFO (SCH-1170): Extracting "OR schematic"
INFO (SCH-1426): Schematic check completed with no errors.
Getting schematic property bag
Getting schematic property bag
INFO (SCH-1181): "sgr43 OR schematic" saved.
```

Fig.: Error Check of pinned form

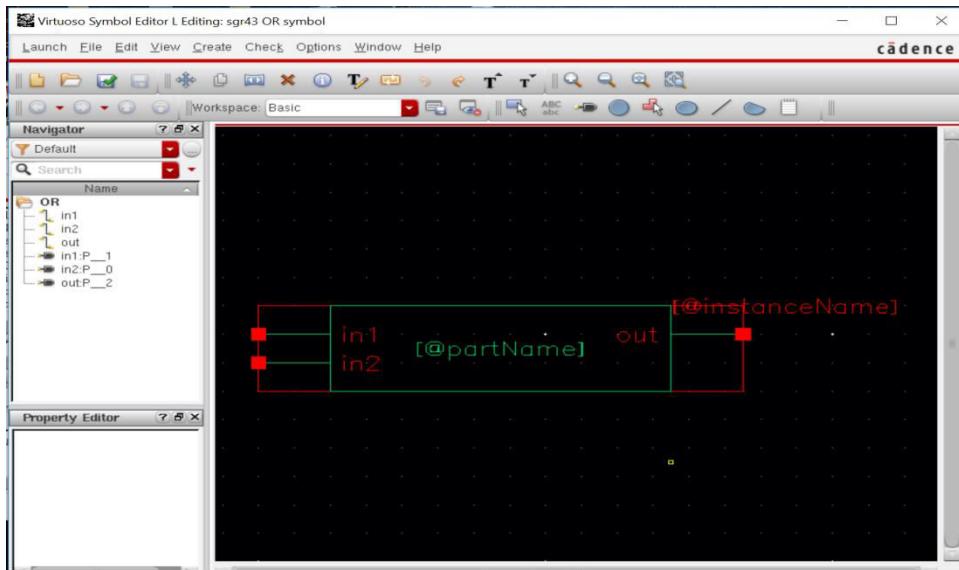


Fig.: Extracted Form of OR Gate

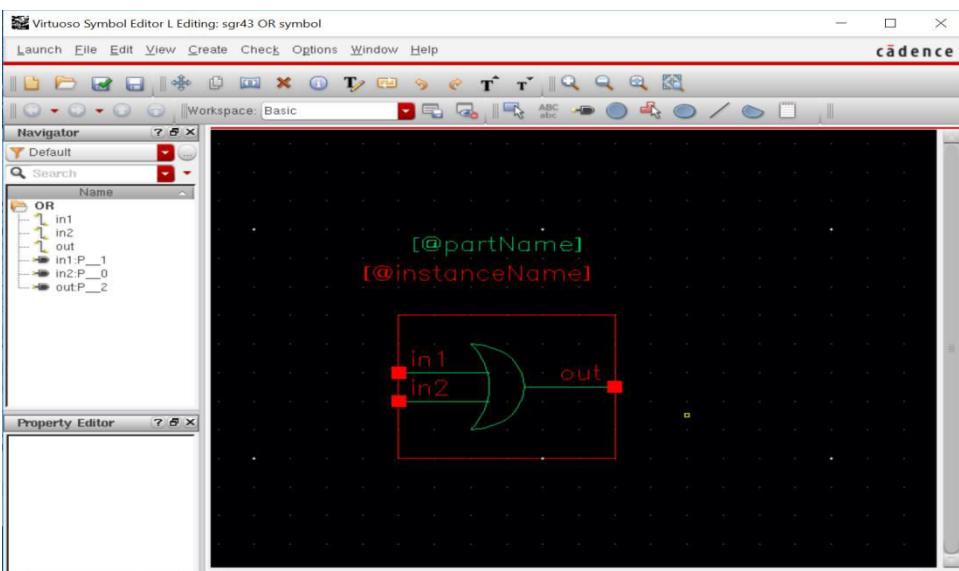


Fig.: Symbol of OR Gate

```

[+] Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence

Getting schematic property bagINFO (SCH-1181): "sgr43 OR schematic" saved.
Symbol (OR symbol) generated and saved in library:sgr43.
INFO (SCH-1061): Completed generating design in library "sgr43" as "OR" "symbol".
Adding CDF information ...
    Adding base cell CDF parameter information
    Adding base cell CDF simulation information ...
INFO (SCH-1171): Cross View Check completed with no errors.
INFO (SCH-1169): "sgr43 OR symbol" saved.

mouse L: mouseSingleSelectPt()          M: schHiMousePopUp()          R: schHiMousePopUp()
1 | >

```

Fig.: Cross-view Check of OR Symbol

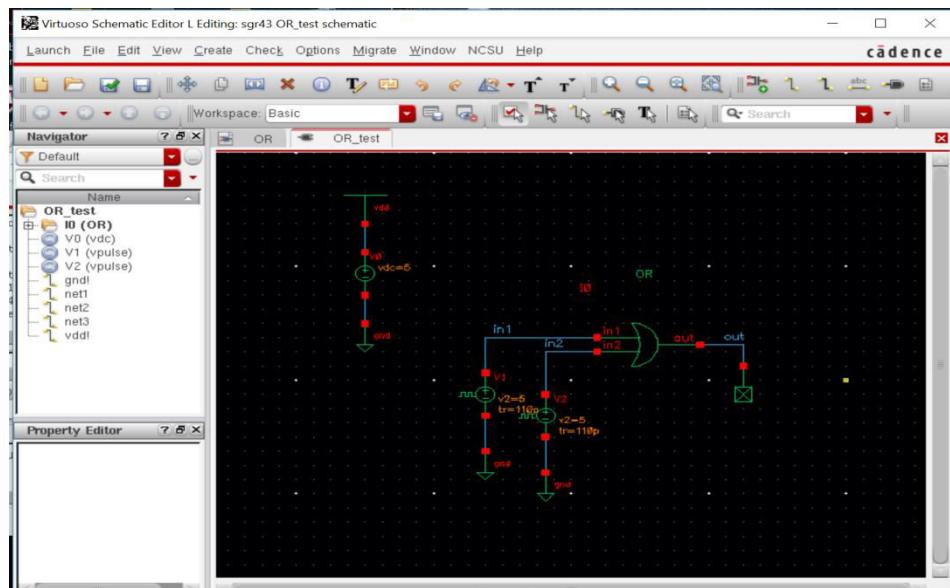


Fig.: Symbolic Representation of OR Gate

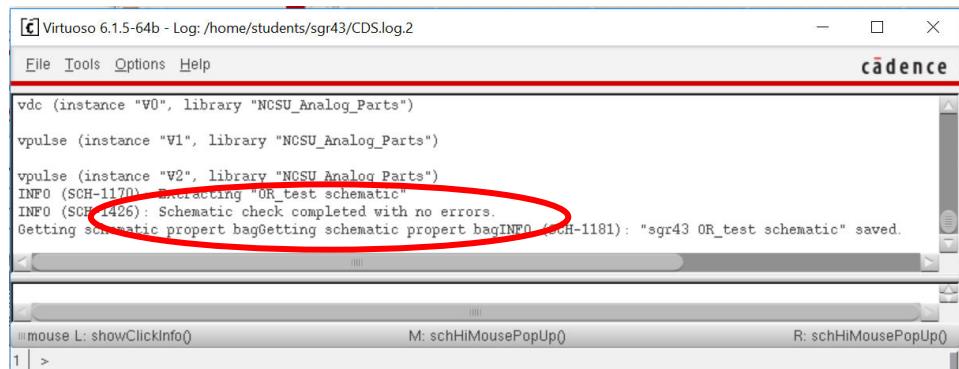


Fig.: Error Check of OR Symbol



Fig.: Waveforms of OR Symbol

3.3 Layout Section of OR Gate

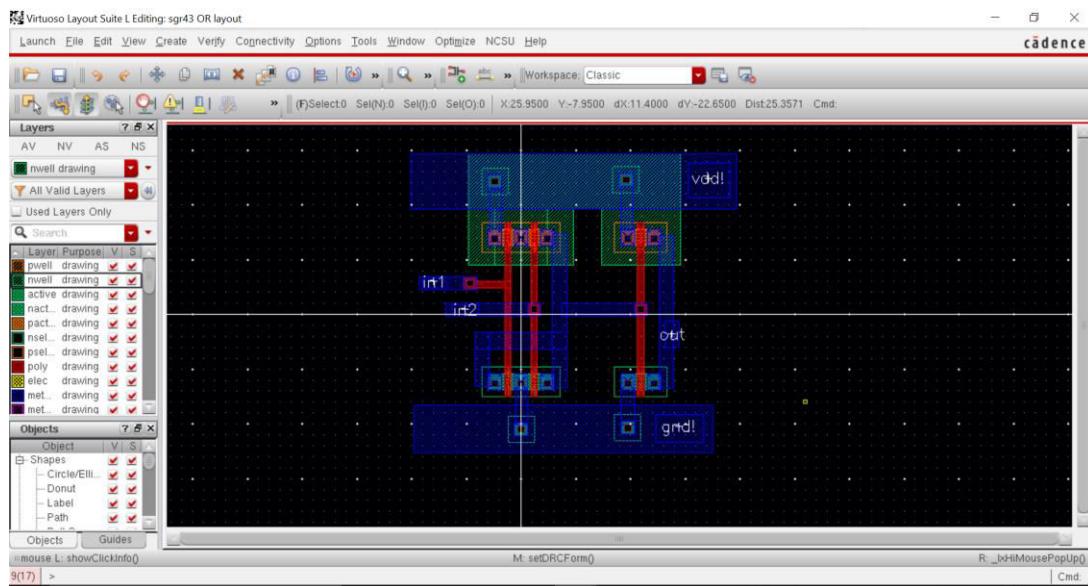


Fig.: Layout of OR Gate

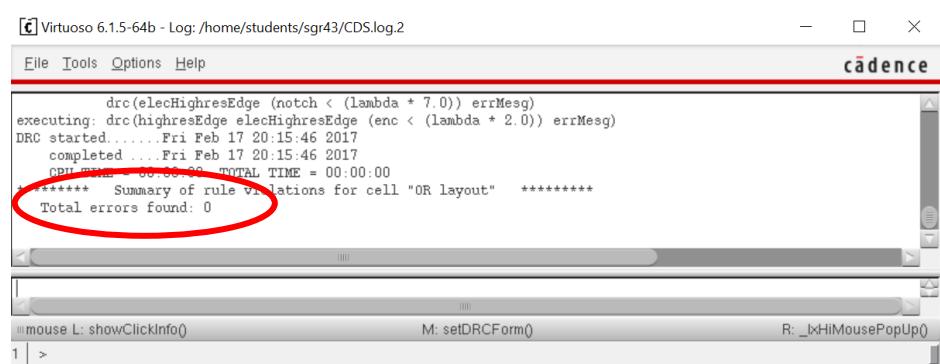


Fig.: Error Check of OR Layout

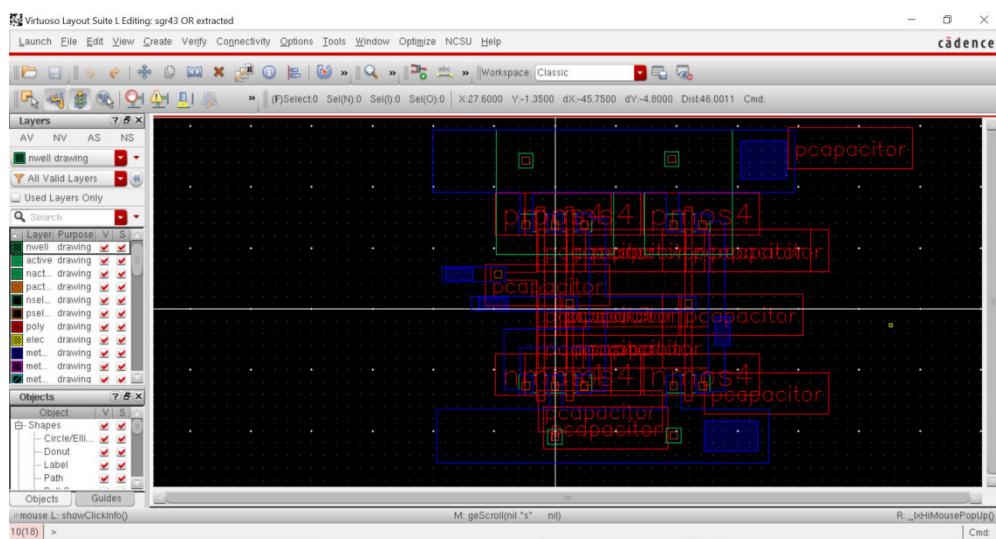


Fig.: Extracted Form of OR Layout

```

[C] Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence
Extraction started.....Fri Feb 17 20:17:40 2017
completed ....Fri Feb 17 20:17:40 2017
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "OR layout" *****
Total errors found: 0

saving rep sgr43/OR/extracted
setting layout property bagGetting layout property bag

```

mouse L: showClickInfo() M: setExtForm() R: _JxHiMousePopUp()

Fig.: Extraction Message of OR Layout

```

[C] Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence
compose simulator input file...
...successful.
start simulator if needed...
...successful.
simulate...
INFO (ADM-3071): Simulation completed successfully.
reading simulation data...
...successful.

mouse L: M: R:
1 | > modify_plot

```

Fig.: Simulation Check of OR Layout

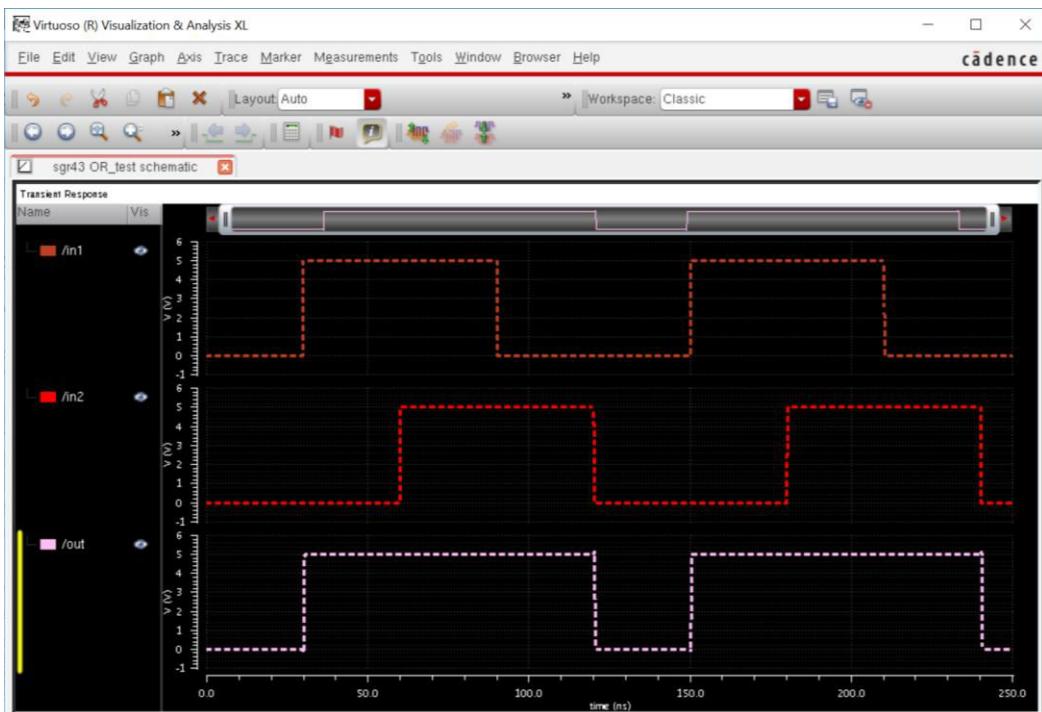


Fig.: Waveforms of OR Layout

5. Implementation of XOR Gate

The XOR gate is a digital logic gate that gives a true (1/HIGH) output when the number of true inputs is odd. The truth table is shown below.

Input		Output
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

The symbol of XOR Gate is shown below.

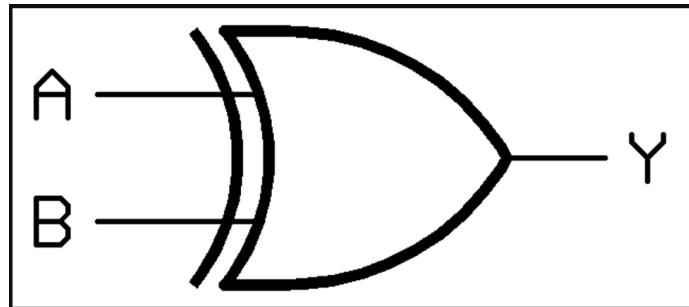


Fig.: Symbol of XOR Gate

The static CMOS circuit of XOR Gate is shown below.

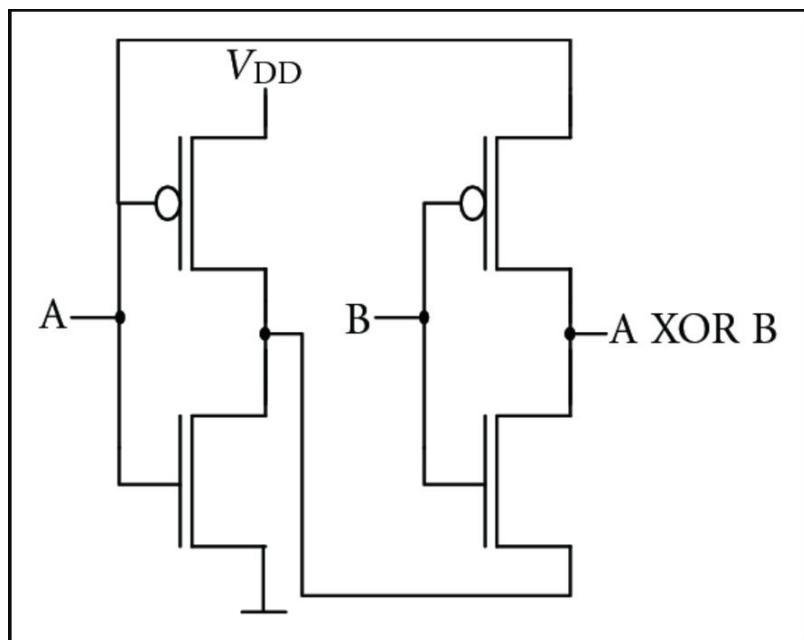


Fig.: Static CMOS circuit of XOR Gate

4.1 Schematic Section of XOR Gate

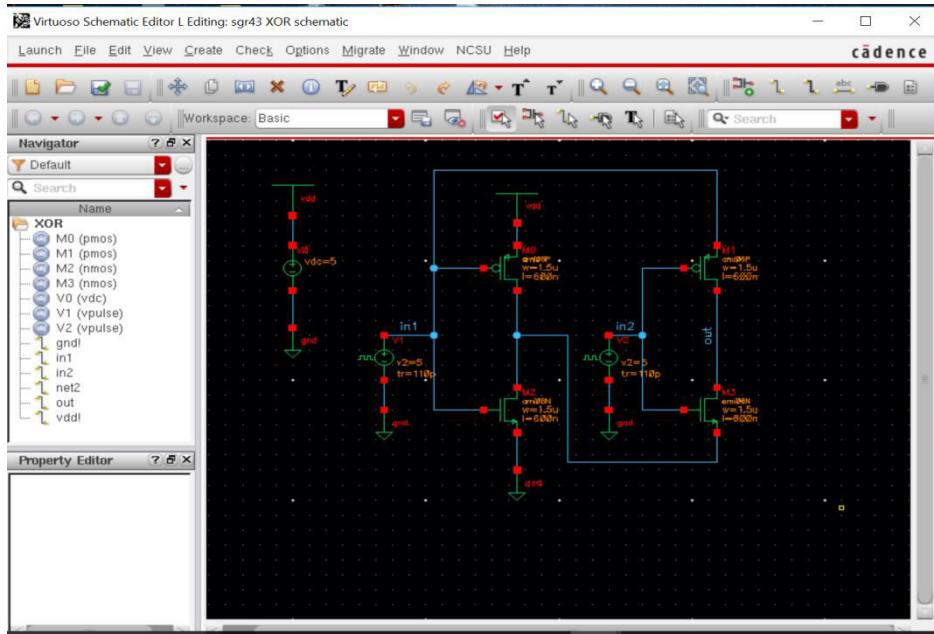


Fig.: Schematic of XOR Gate

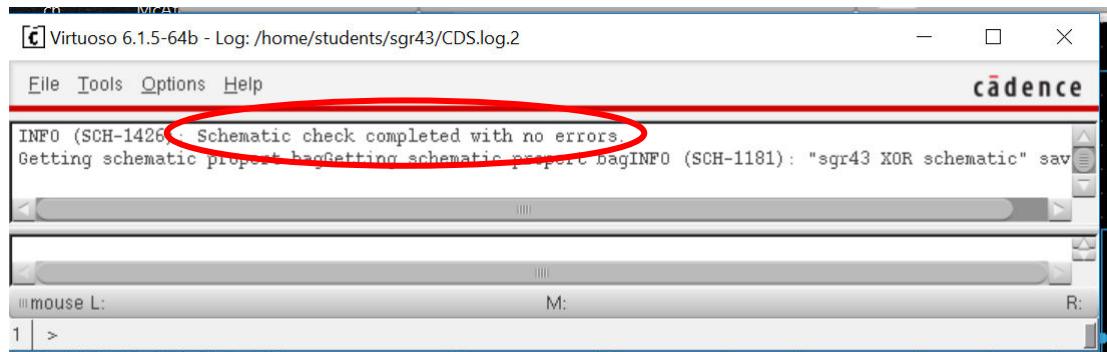


Fig.: Error Check of Schematic

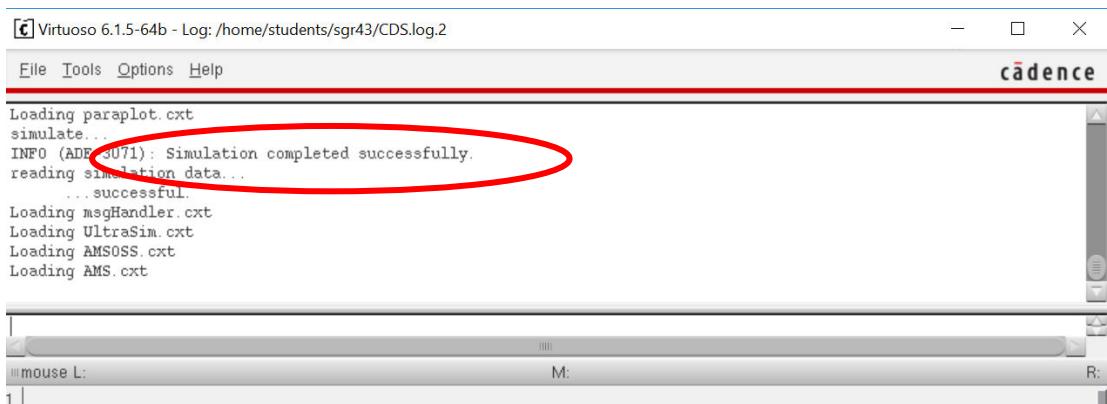


Fig.: Simulation Check of Schematic



Fig.: Waveforms of XOR Gate

3.2 Symbolic Section of XOR Gate

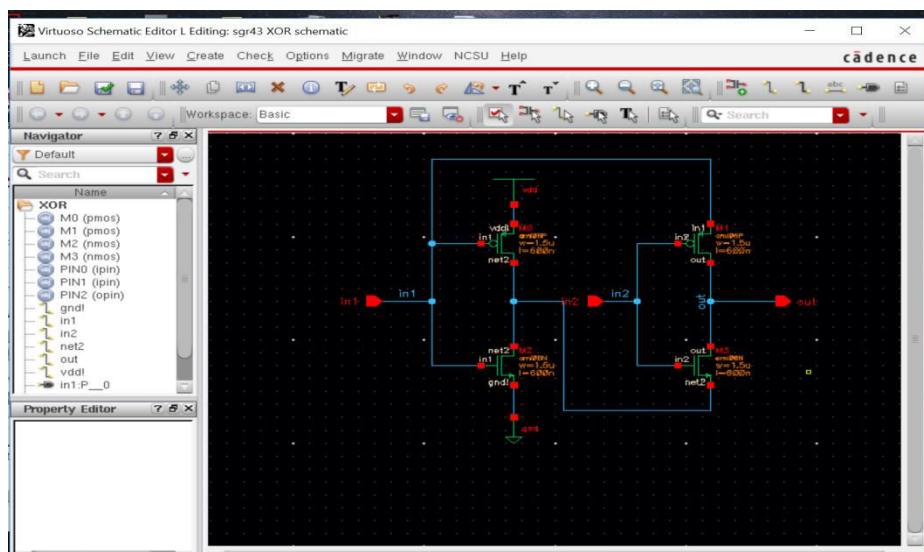


Fig.: Pinned Form of XOR Gate

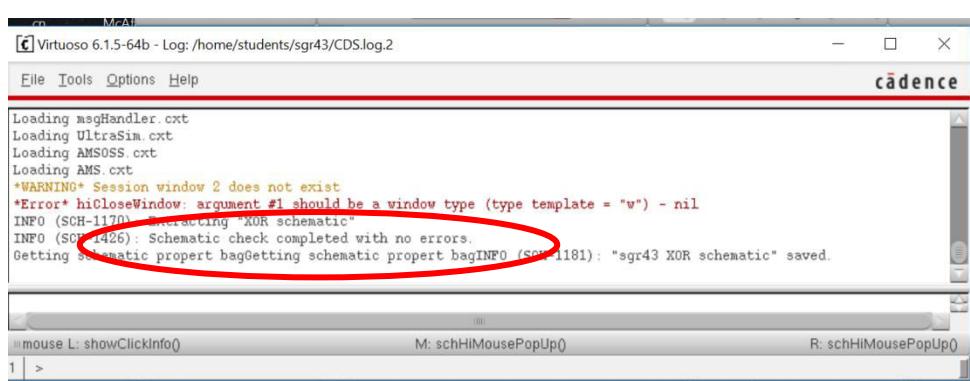


Fig.: Error Check of pinned form

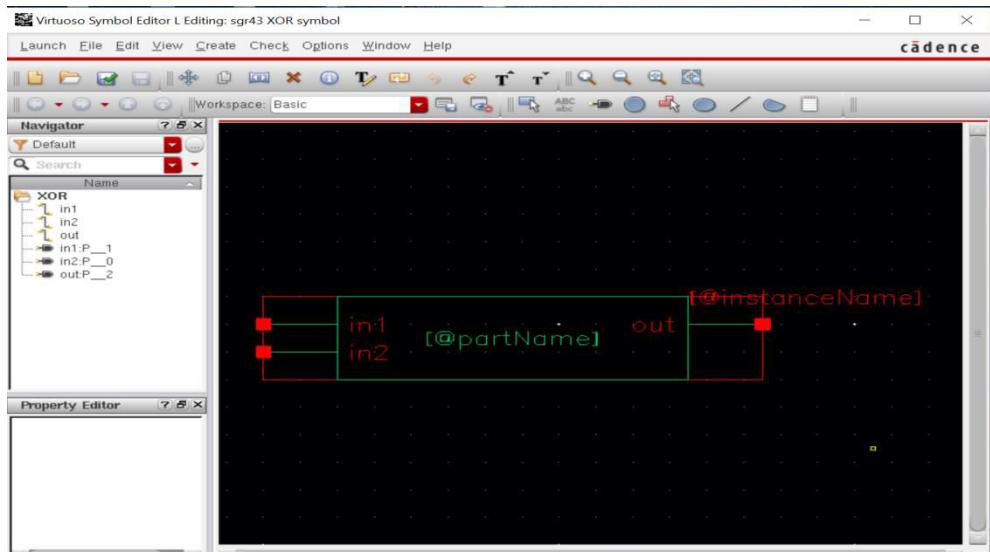


Fig.: Extracted Form of XOR Gate

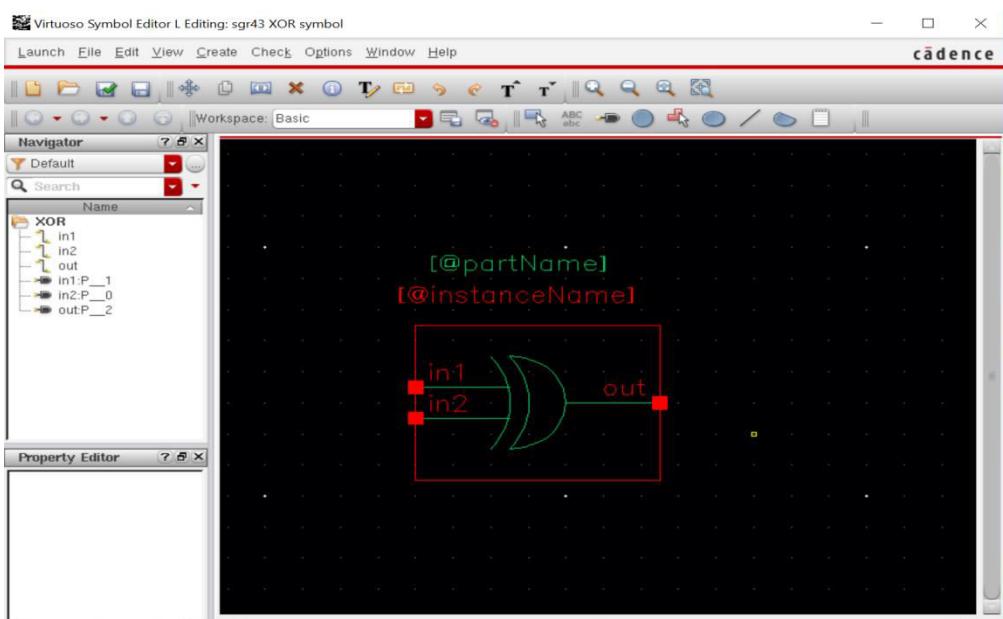


Fig.: Symbol of XOR Gate

```

INFO (SCH-1426): Schematic check completed with no errors.
Getting schematic property bagGetting schematic property bagINFO (SCH-1181): "sgr43 XOR schematic" saved.
Symbol (XOR symbol) generated and saved in library:sgr43.
INFO (SCH-1061): Completed generating design in library "sgr43" as "XOR" "symbol".
Adding CDF information ...
    Adding base cell CDF parameter information ...
    Adding base cell CDF simulation information ...
INFO (SCH-1171): Cross View Check completed with no errors.
INFO (SCH-1181): "sgr43 XOR symbol" saved.

```

Fig.: Cross-view Check of XOR Symbol

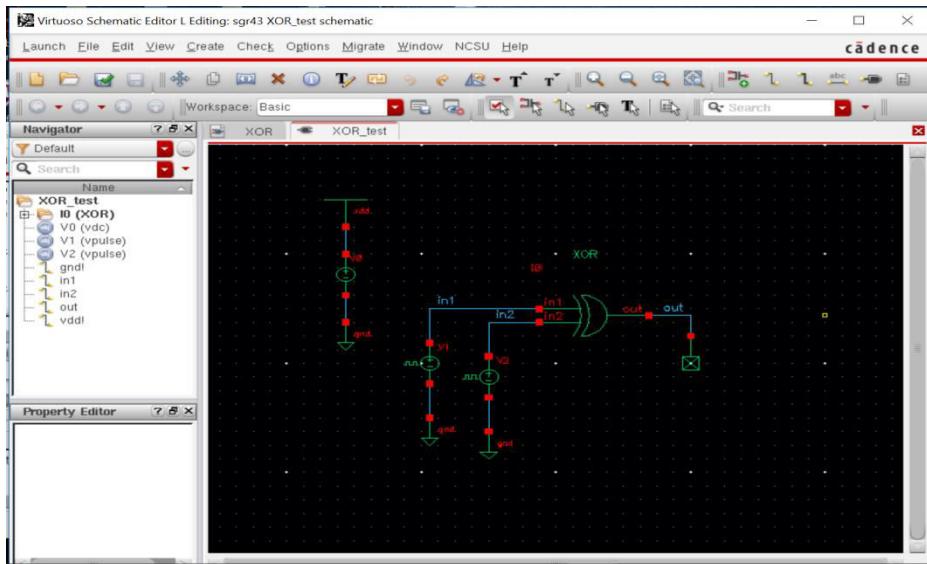


Fig.: Symbolic Representation of XOR Gate

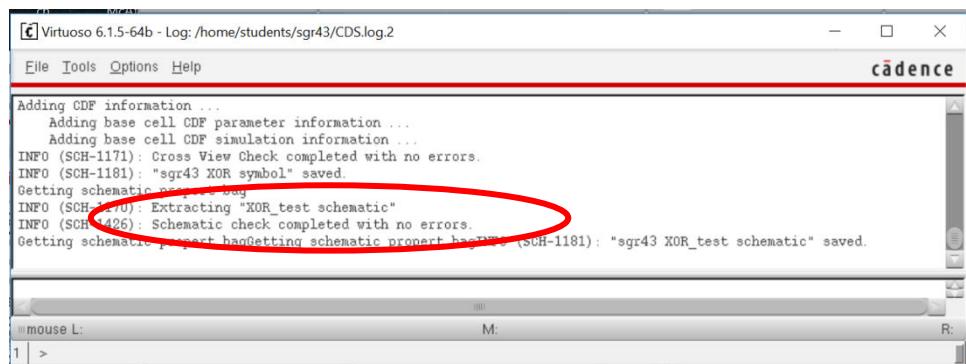


Fig.: Error Check of XOR Symbol



Fig.: Waveforms of XOR Symbol

4.3 Layout Section of XOR Gate

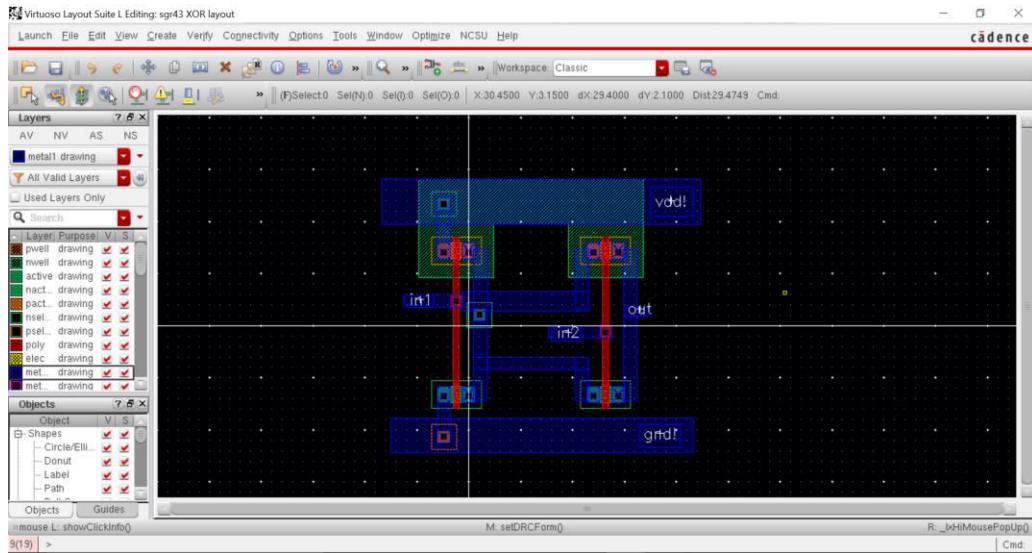


Fig.: Layout of XOR Gate

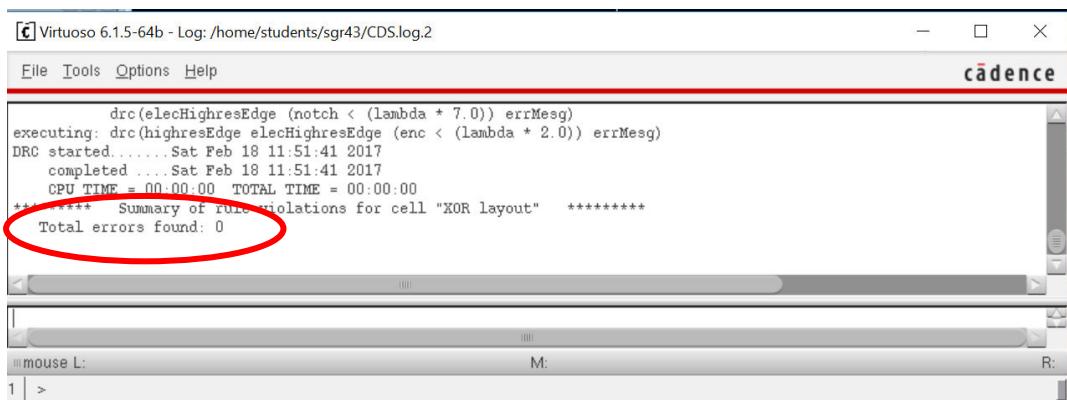


Fig.: Error Check of XOR Layout

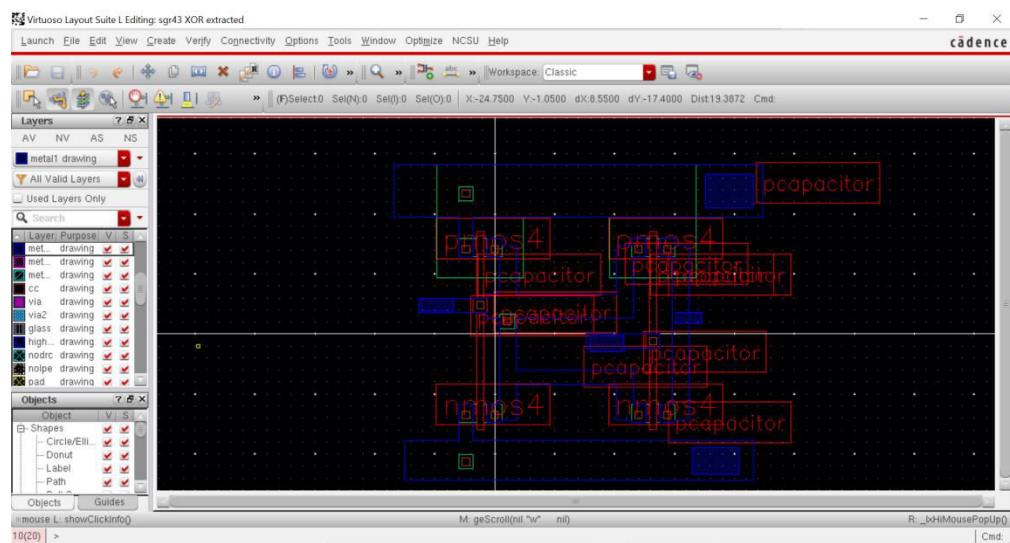


Fig.: Extracted Form of XOR Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2

File Tools Options Help

cadence

```

executing: saveDerived(via2 ("via2" "net") cell_view)
Extraction started..... Sat Feb 18 11:53:11 2017
completed ... Sat Feb 18 11:53:11 2017
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "XOR layout" *****
Total errors found: 0

Saving rep sgr43/XOR/extracted
Getting layout property bagGetting layout property bag

```

mouse L: showClickInfo() M: setExtForm() R: _IxHiMousePopUp()

Fig.: Extraction Message of XOR Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2

File Tools Options Help

cadence

```

compose simulator input file...
...successful.
start simulator if needed...
...successful.
simulate
INFO (ADE-3071): Simulation completed successfully.
reading simulation data...
...successful.

```

mouse L: M: R:

Fig.: Simulation Check of XOR Layout

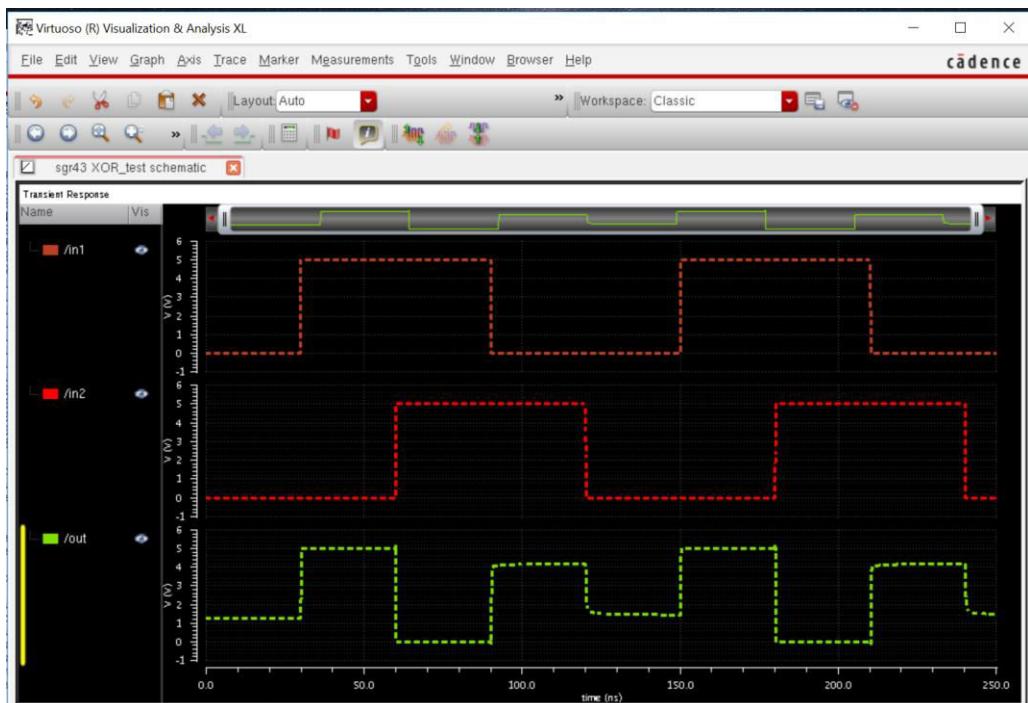


Fig.: Waveforms of XOR Layout

6. Implementation of NAND Gate

In digital electronics, a NAND gate (negative-AND) is a logic gate which produces an output which is false only if all its inputs are true; thus its output is complement to that of the AND gate. The truth table is shown below.

Input		Output
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

The symbol of NAND Gate is shown below.

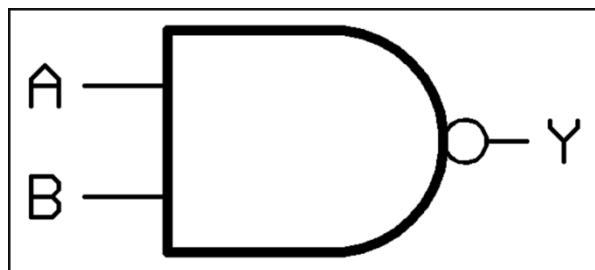


Fig.: Symbol of NAND Gate

The static CMOS circuit of NAND Gate is shown below.

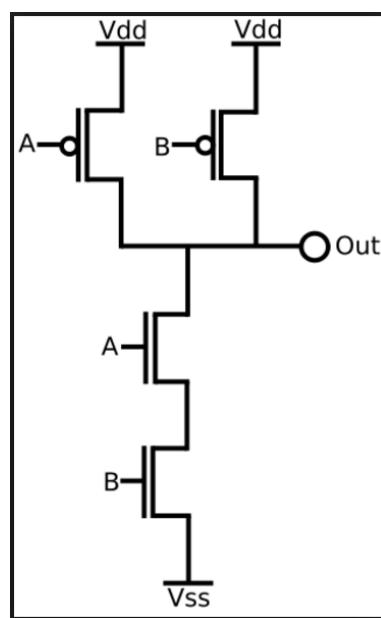


Fig.: Static CMOS circuit of NAND Gate

6.1 Schematic Section of NAND Gate

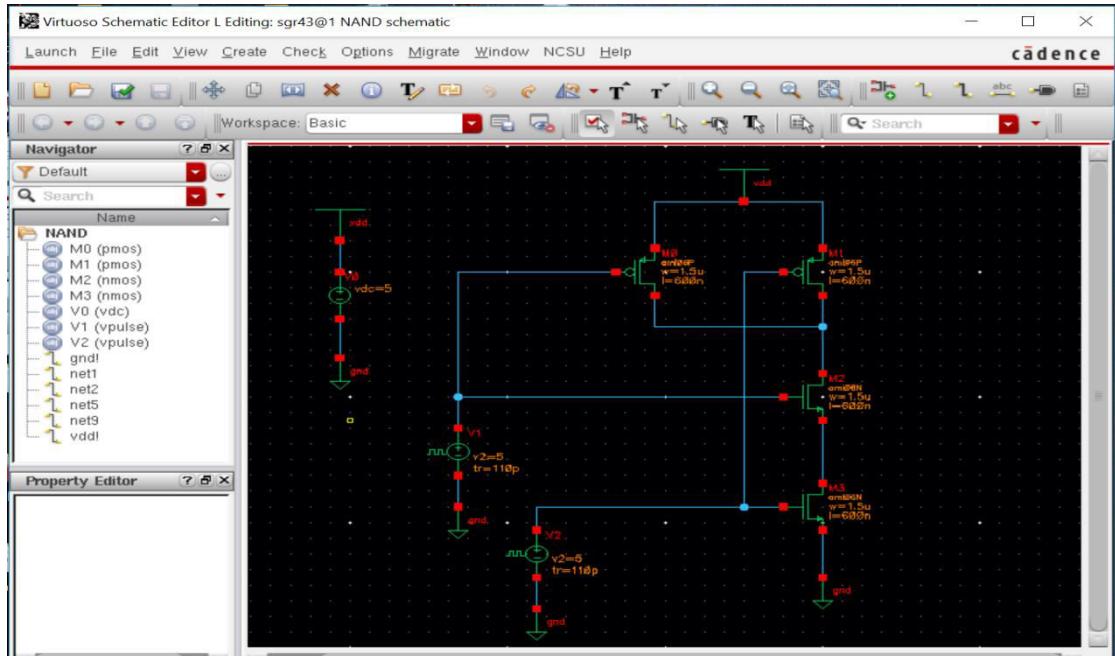


Fig.: Schematic of NAND Gate

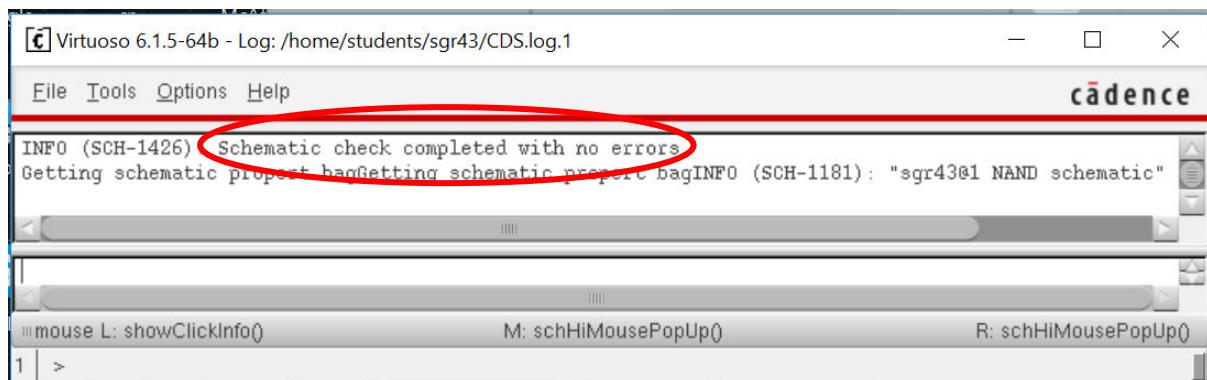


Fig.: Error Check of NAND Schematic

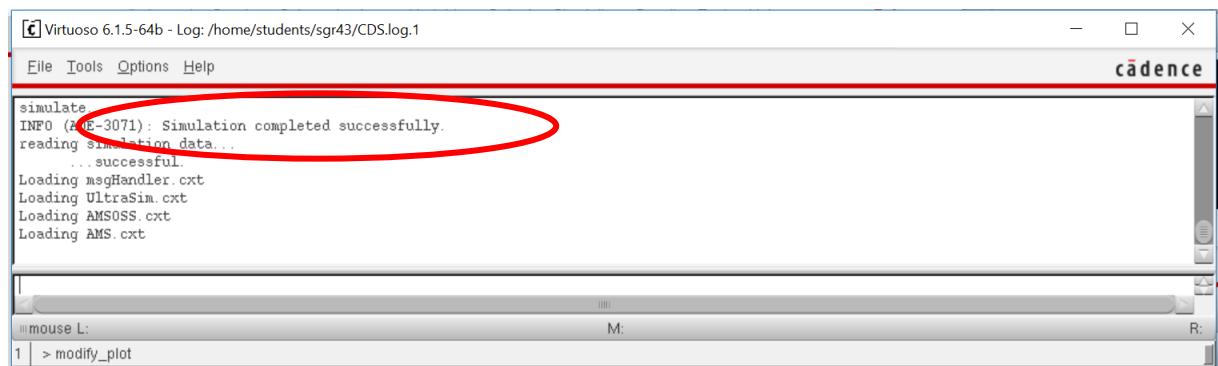


Fig.: Simulation Check of NAND Schematic

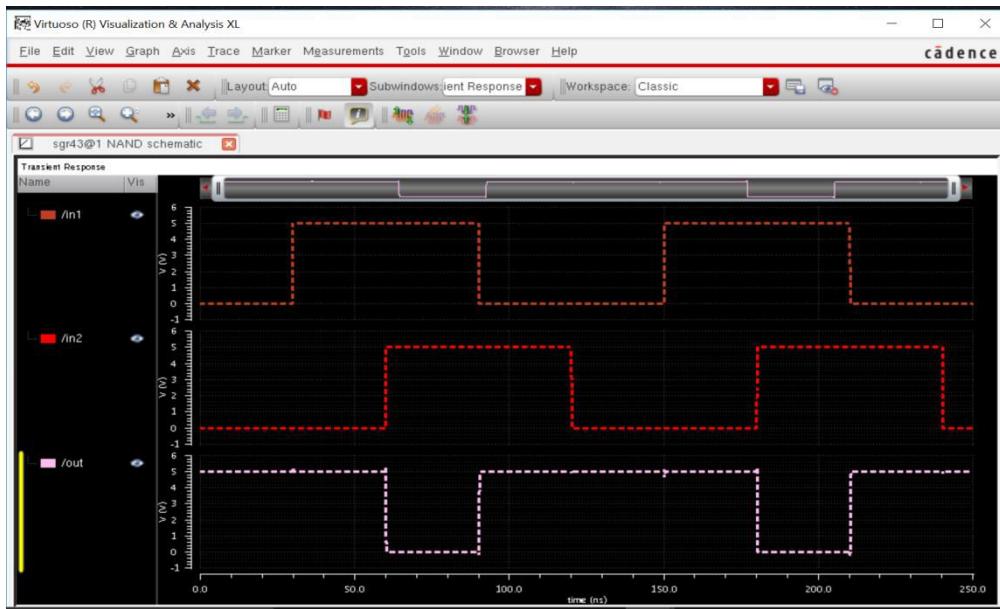


Fig.: Waveforms of NAND Schematic

6.2 Symbolic Section of NAND Gate

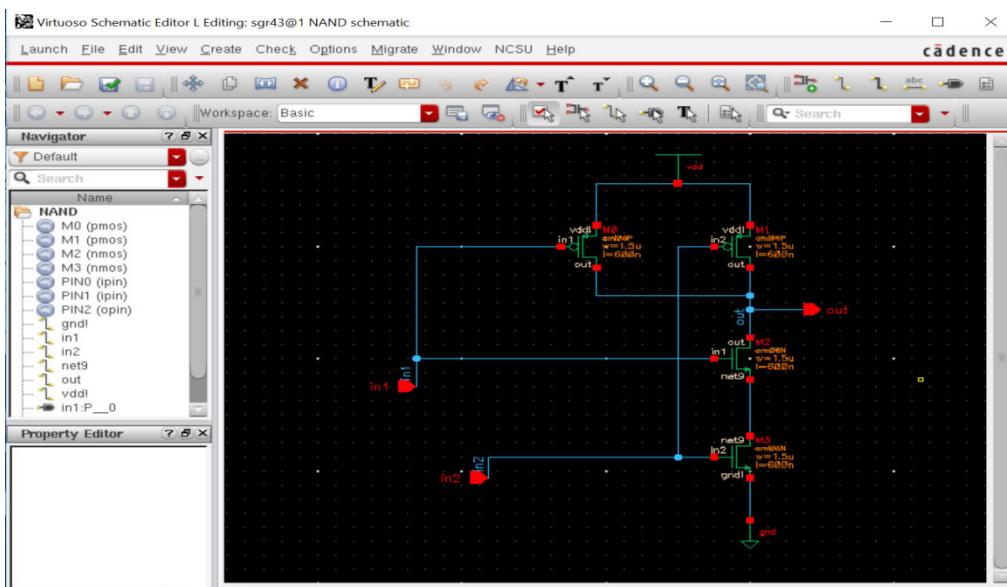


Fig.: Pinned Form of NAND Gate

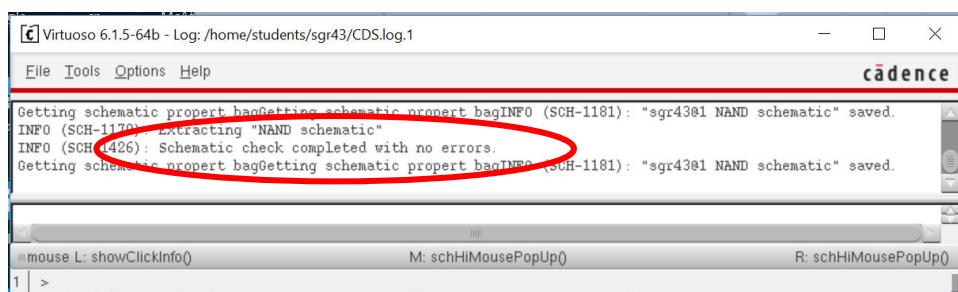


Fig.: Error Check of pinned form

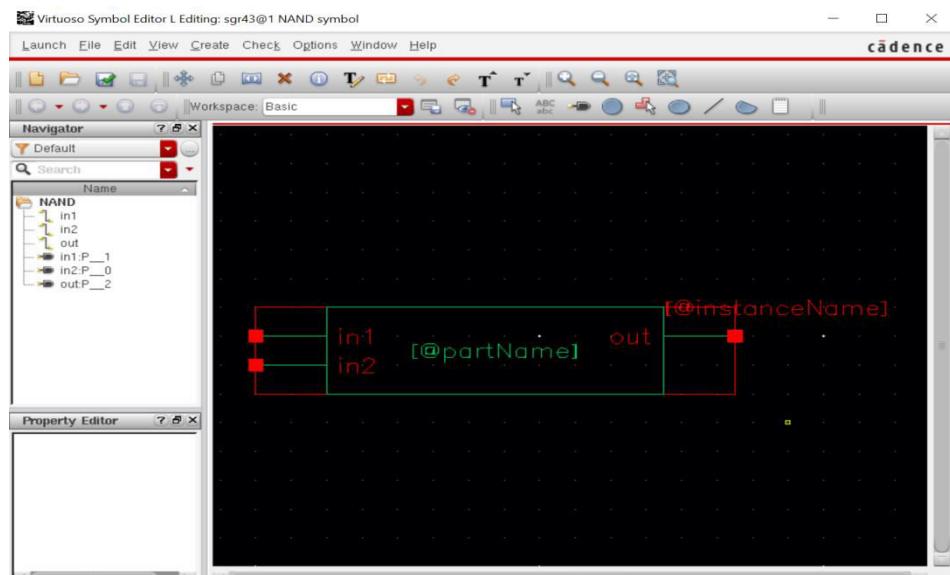


Fig.: Extracted Form of NAND Gate

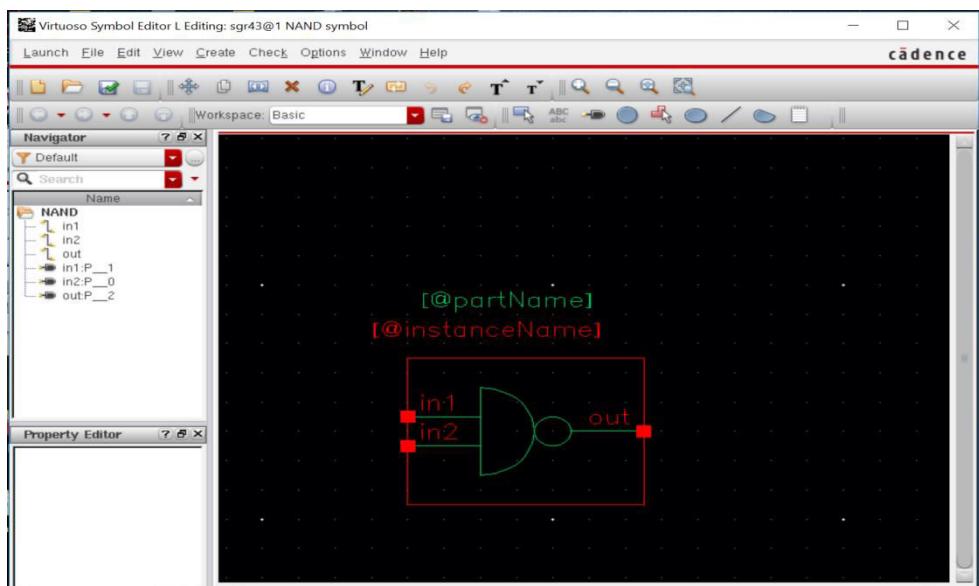


Fig.: Symbol of NAND Gate

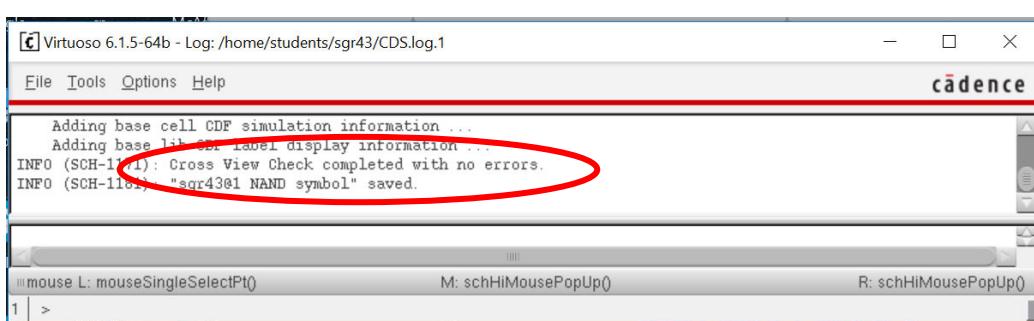


Fig.: Cross-view Check of NAND Symbol

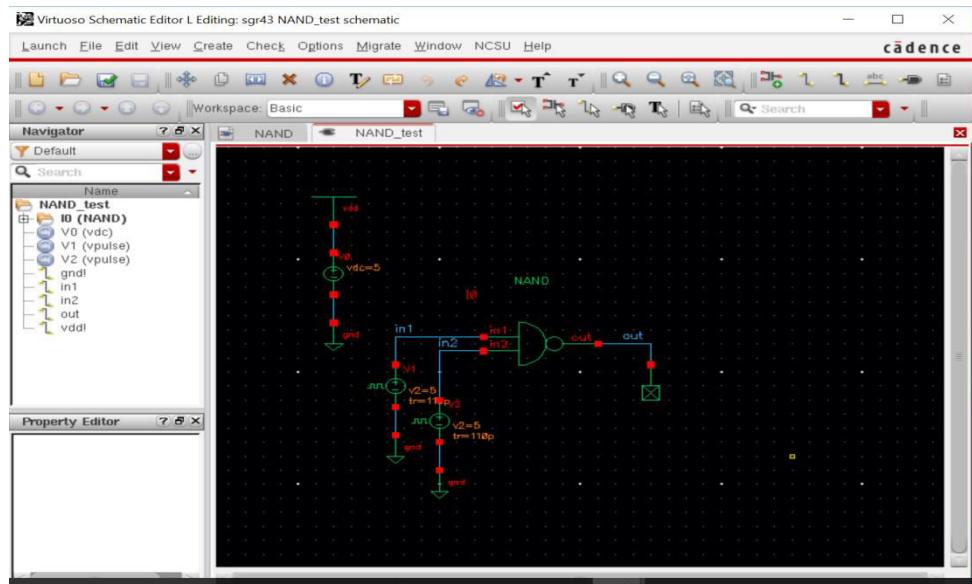


Fig.: Symbolic Representation of NAND Gate

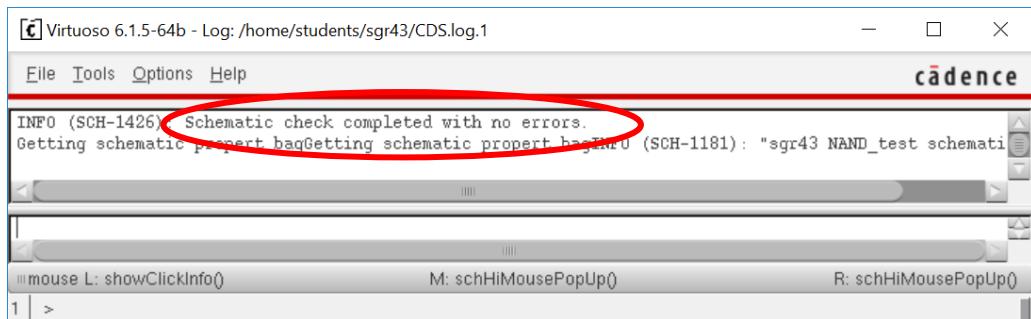


Fig.: Error Check of NAND Symbol

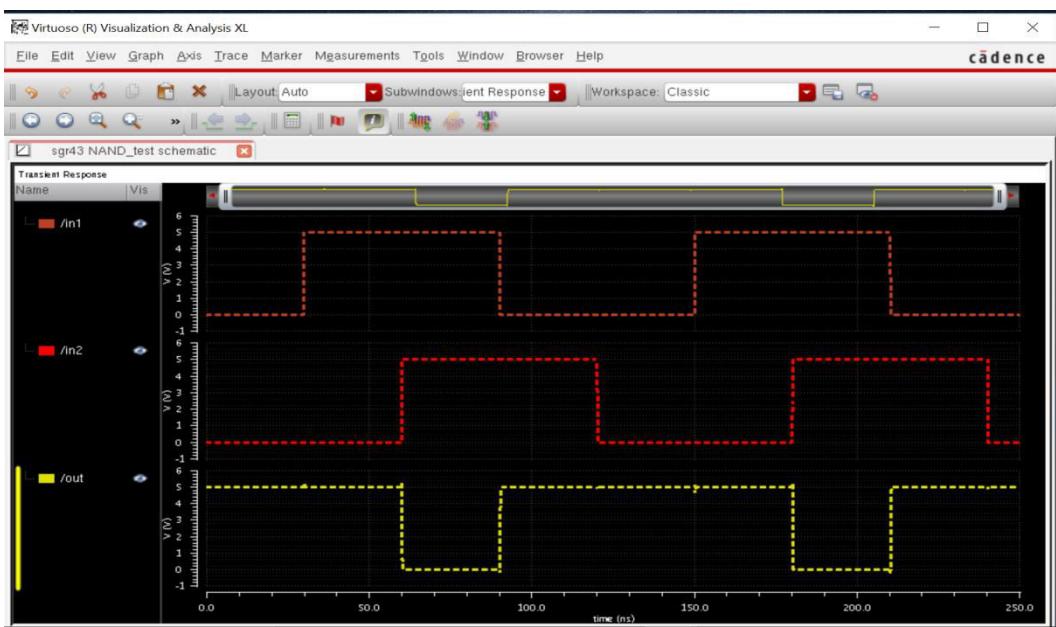


Fig.: Waveforms of NAND Symbol

6.3 Layout Section of NAND Gate

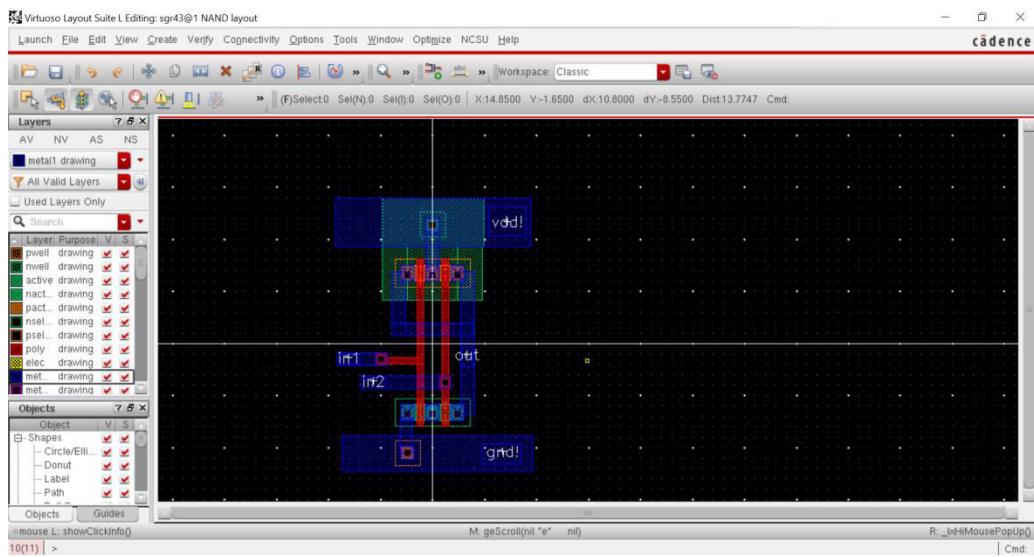


Fig.: Layout of NAND Gate

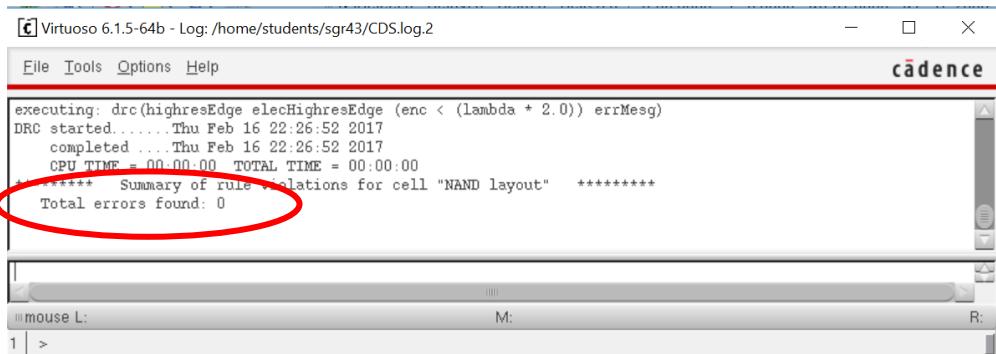


Fig.: Error Check of NAND Layout

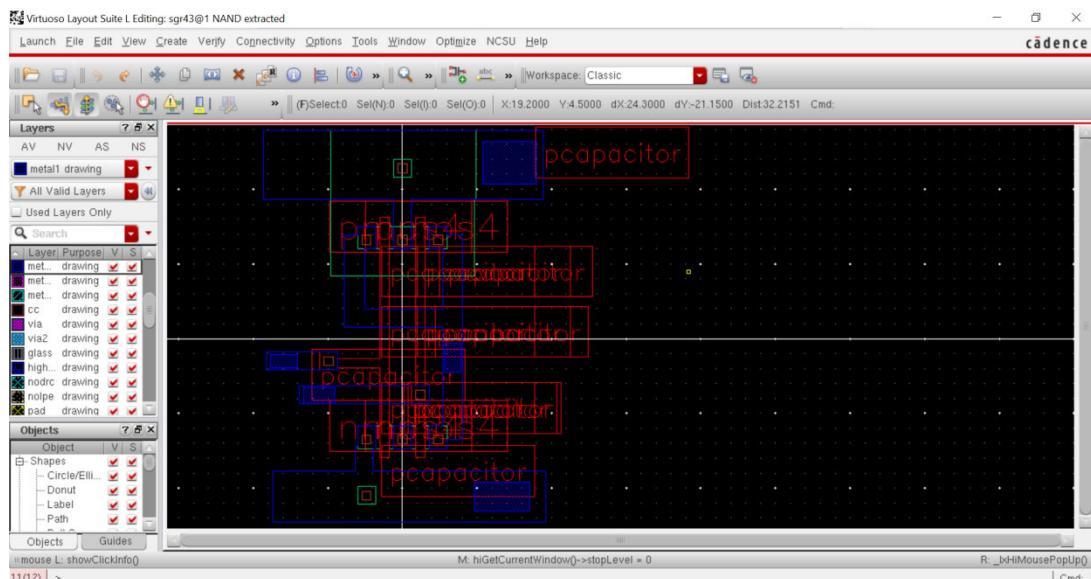


Fig.: Extracted Form of NAND Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2

completedThu Feb 16 22:32:23 2017
 CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
 ***** Summary of rule violations for cell "NAND layout" *****
 Total errors found: 0

Saving rep sgr43@1/NAND/extracted
 Setting layout propert bagGetting layout property log

mouse L: showClickInfo()
 M: setExtForm()
 R: _lxHiMousePopUp()

Fig.: Extraction Message of NAND Layout

Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2

simulate...
 INFO (ML-3071): Simulation completed successfully.
 reading simulation data...
 ...successful.
 Loading msgHandler.cxt
 Loading UltraSim.cxt
 Loading AMSOSS.cxt

mouse L:
 M:
 R:

Fig.: Simulation Check of NAND Layout

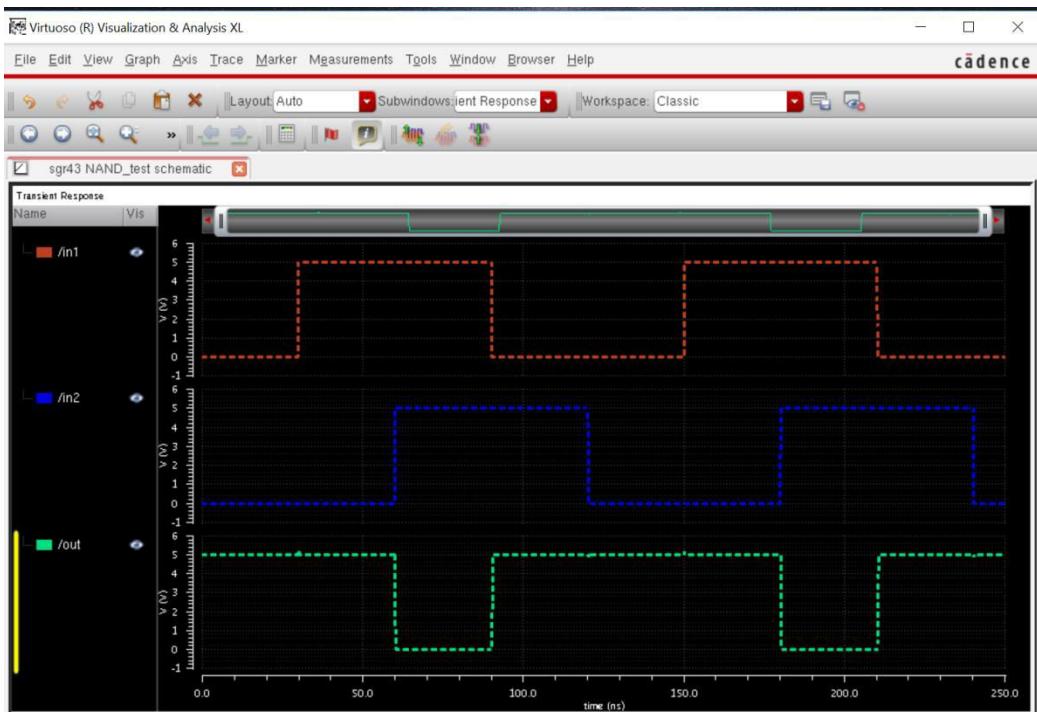


Fig.: Waveforms of NAND Layout