

UNIVERSITY OF MISSOURI – KANSAS CITY

INTRODUCTION TO VLSI DESIGN (EC 5542)

SPRING 2017

**PROJECT – III : MOD 13 SYNCHRONOUS BINARY UP
COUNTER**

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ABSTRACT

The circuit that is being designed in this project is “MOD 13 SYNCHRONOUS BINARY UP COUNTER”. It requires a 4-bit counter whose states would be from ‘0000’ to ‘1111’. Each bit is the output of a single flip-flop. But, we are required to count only 13 states from ‘0000’ to ‘1100’. Since the designed model is a synchronous counter, the external clock signal is connected to every flip-flop within the counter so that all of the flip-flops are clocked simultaneously at the same time. The changes in the output occur in synchronization with the clock signal due to which there would be no propagation delay.

1. INTRODUCTION

1.1 Counter

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

1.2 Synchronous Counter

These counters are classified into different types, one of which is a synchronous counter. A synchronous counter is a type of counter where the clock signals to all the flip-flops are clocked simultaneously. This feature provides us with the output of all the flip-flops at the same time, with no propagation delay.

1.3 Synchronous Up Counter

A synchronous up counter specifies that the count starts from the least (0000) and reaches the maximum limit with all the flip-flops triggered at the same time.

1.4 4-bit Synchronous Up Counter

A 4-bit synchronous up counter consists of 4 flip-flops triggered simultaneously to obtain the output at the same time without any propagation delay. A 4-bit up counter counts from ‘0000’ to ‘1111’, each bit obtained from each flip-flop.

1.5 MOD-13 Synchronous Up Counter

A mod-13 synchronous up counter is obtained from a 4-bit counter in which only 13 states are considered, from ‘0000’ to ‘1100’. The remaining states are neglected. Once the counter reaches ‘1100’, the next state to be counted will be ‘0000’, that means the counter resets after reaching 13 states.

1.6 Truth Table

The counter remains in the previous state as long as the clock signal remains low.

Present State				Clock	Next State			
A	B	C	D		Q _A	Q _B	Q _C	Q _D
0	0	0	0	↑	0	0	0	1
0	0	0	1	↑	0	0	1	0
0	0	1	0	↑	0	0	1	1
0	0	1	1	↑	0	1	0	0
0	1	0	0	↑	0	1	0	1
0	1	0	1	↑	0	1	1	0
0	1	1	0	↑	0	1	1	1
0	1	1	1	↑	1	0	0	0
1	0	0	0	↑	1	0	0	1
1	0	0	1	↑	1	0	1	0
1	0	1	0	↑	1	0	1	1
1	0	1	1	↑	1	1	0	0
1	1	0	0	↑	0	0	0	0
1	1	0	1	↑	x	x	x	x
1	1	1	0	↑	x	x	x	x
1	1	1	1	↑	x	x	x	x

Table no.: 1.1

1.7 State Diagram

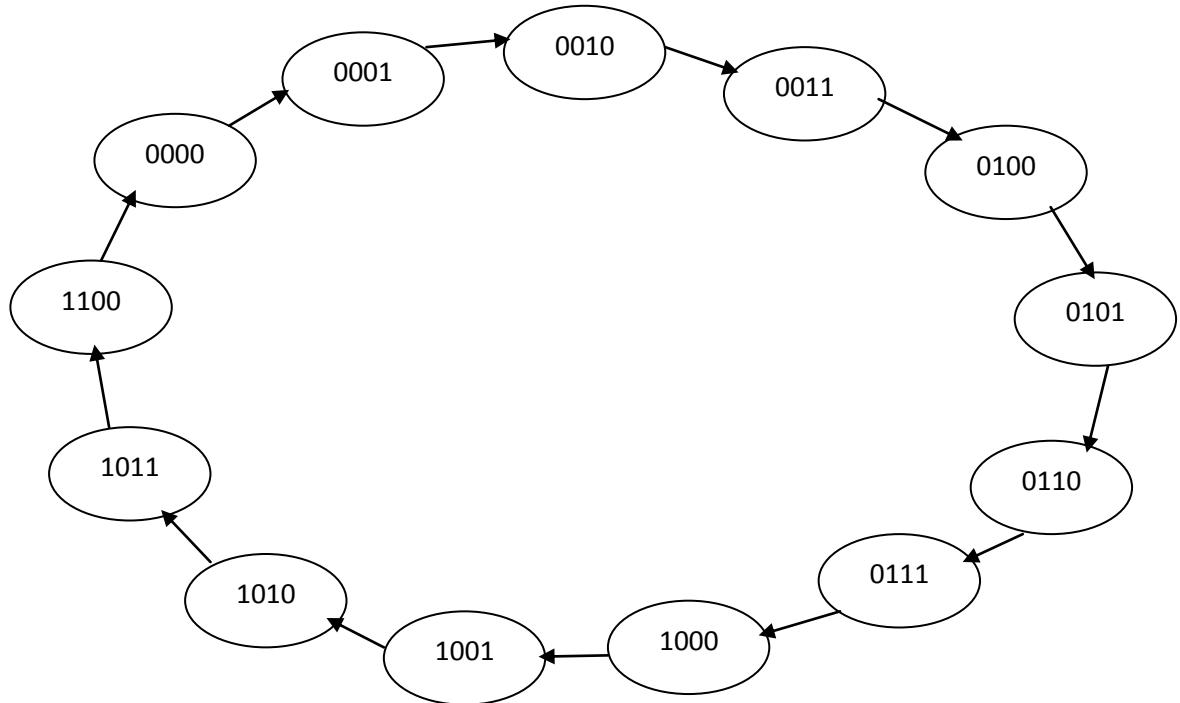


Fig. no.: 1.1

1.8 Next State Equations

We obtain the equations for next state from the truth table using K-map (Karnaugh Map Method). The equations thus obtained are multiplied by an extra signal called Enable signal (E) which is considered as the driving signal along with the clock signal.

For Q_A :

Q_A	$C'D'$	$C'D$	CD	CD'
$A'B'$				
$A'B$			1	
AB		x	x	x
AB'	1	1	1	1

Table no.: 1.2

$$Q_A = (AB' + BCD) E$$

For Q_B :

Q_B	$C'D'$	$C'D$	CD	CD'
$A'B'$			1	
$A'B$	1 1			1
AB		x	x	x
AB'			1	

Table no.: 1.3

$$Q_B = (A'B'C' + A'BD' + B'CD) E$$

$$Q_B = (A'B(CD)' + B'CD) E$$

For Q_C :

Q_C	$C'D'$	$C'D$	CD	CD'
$A'B'$		1		1
$A'B$		1		1
AB		x	x	x
AB'	1			1

Table no.: 1.4

$$Q_C = (C'D + CD') E$$

For Q_D :

Q_D	$C'D'$	$C'D$	CD	CD'
$A'B'$	1			1
$A'B$	1			1
AB		x	x	x
AB'	1			1

Table no.: 1.5

$$Q_D = (A'D' + B'D') E$$

$$Q_D = (D' (AB)') E$$

1.9 Applications

- Digital clocks
- Timers
- Oven timers
- VCR Clocks

2. DESIGN SPECIFICATIONS

2.1 Transistor Count

Each D flip-flop has a count of 70 transistors. As we have 4 flip-flops, it comes to a total of 280 transistors. The input to first flip-flop counts to 26 transistors, second flip-flop to 32 transistors, third flip-flop to 24 transistors and fourth flip-flop to 12 transistors.

2.2 Frequency of Operation

The enable signal is maintained at a constant dc voltage of 5V. The clock signal applied has a frequency of about 100GHz.

3. SCHEMATIC SECTION

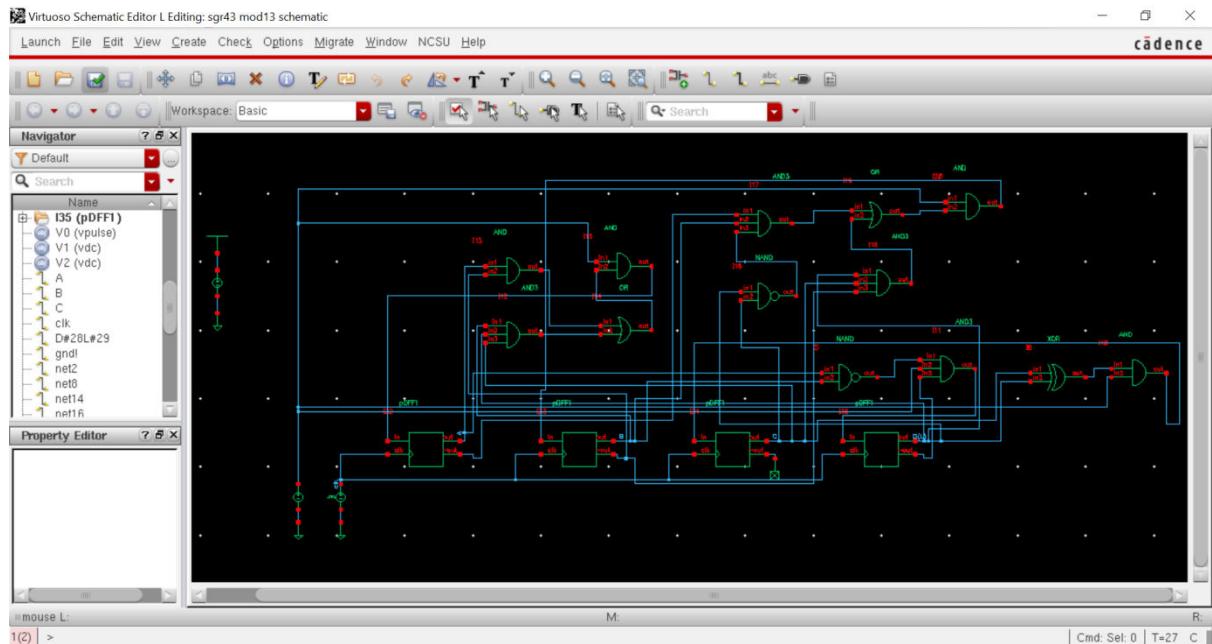


Fig. no.: 3.1

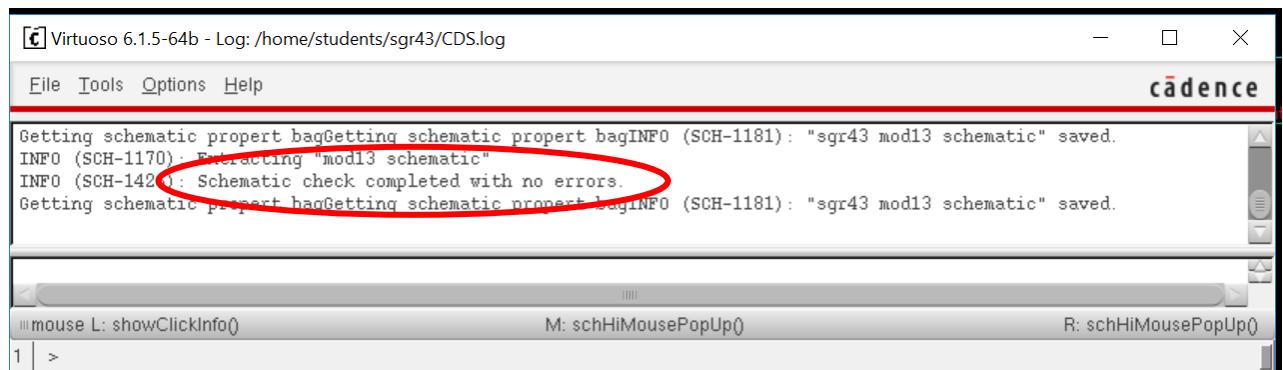


Fig. no.: 3.2

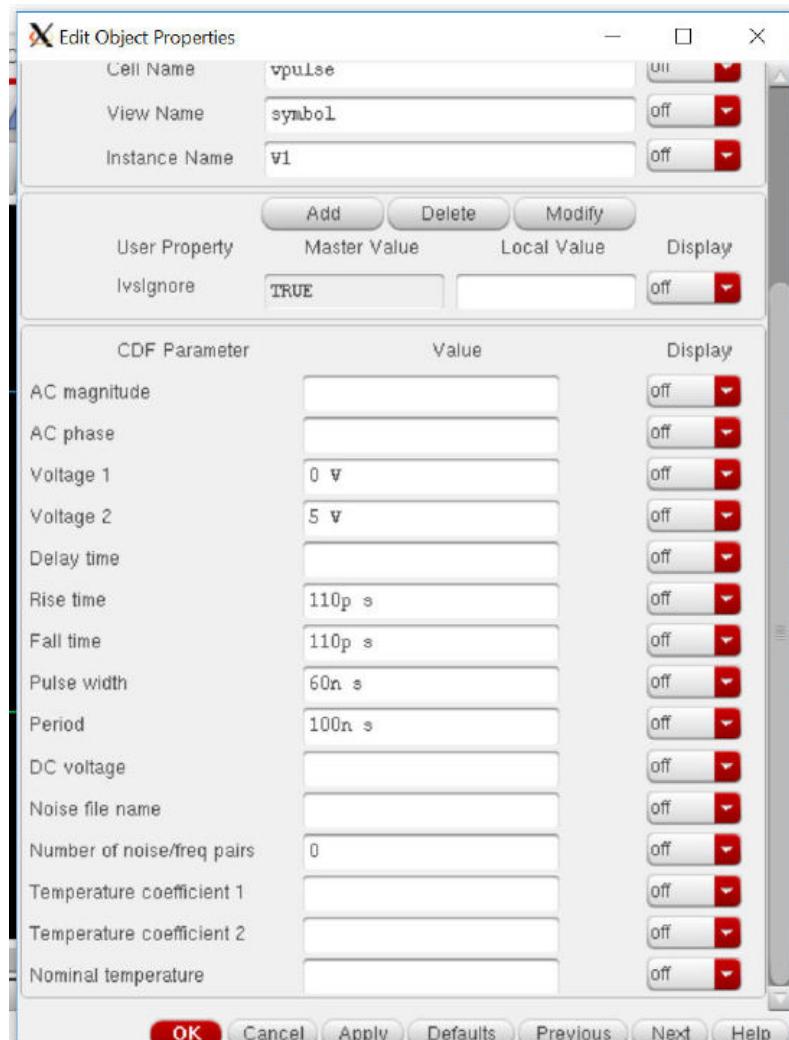


Fig. no.: 3.3

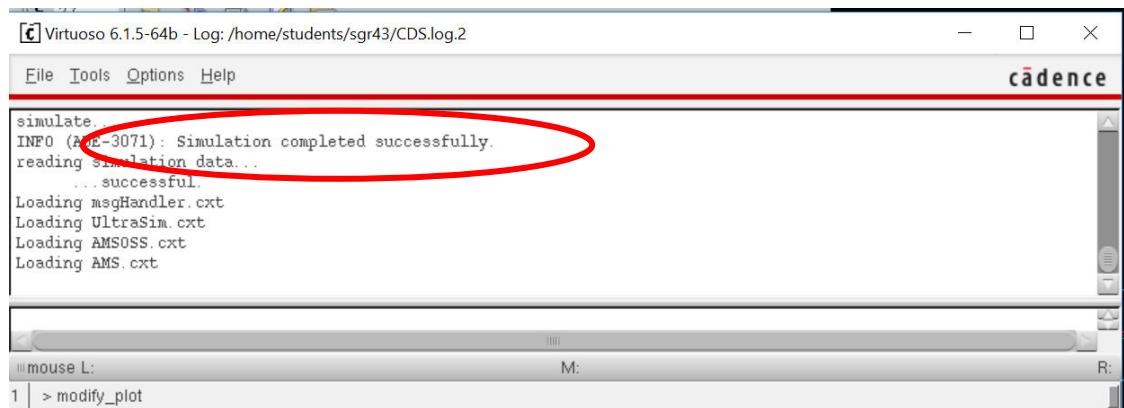


Fig. no.: 3.4

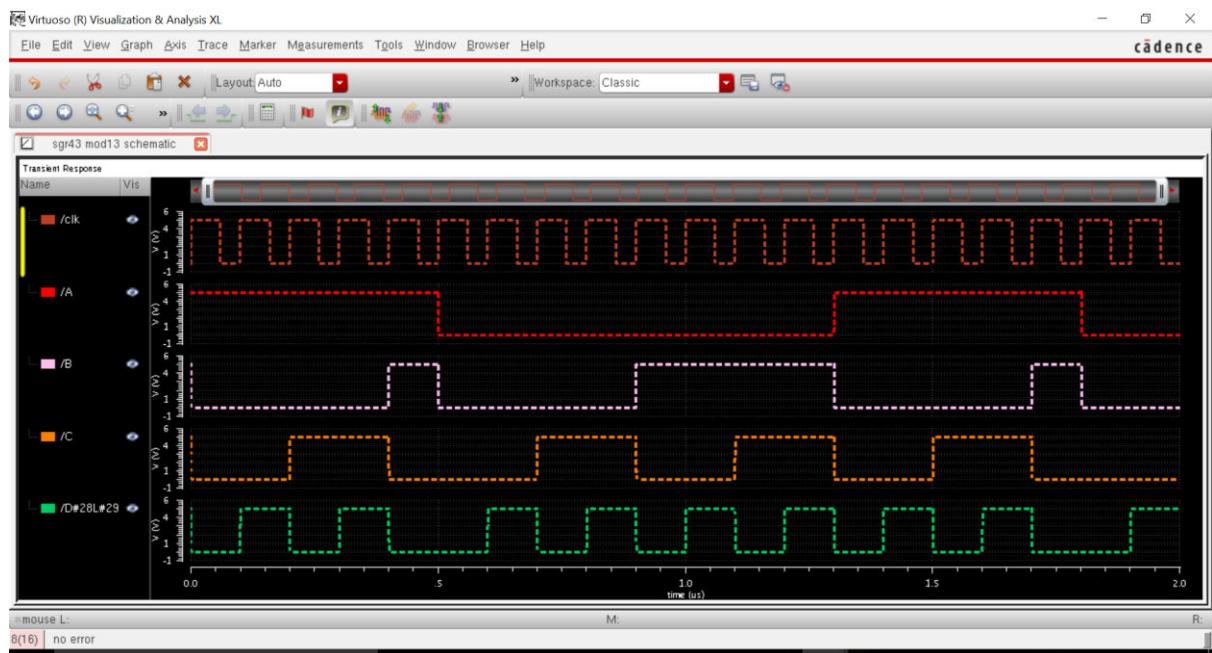


Fig. no.: 3.5

4. SYMBOLIC SECTION

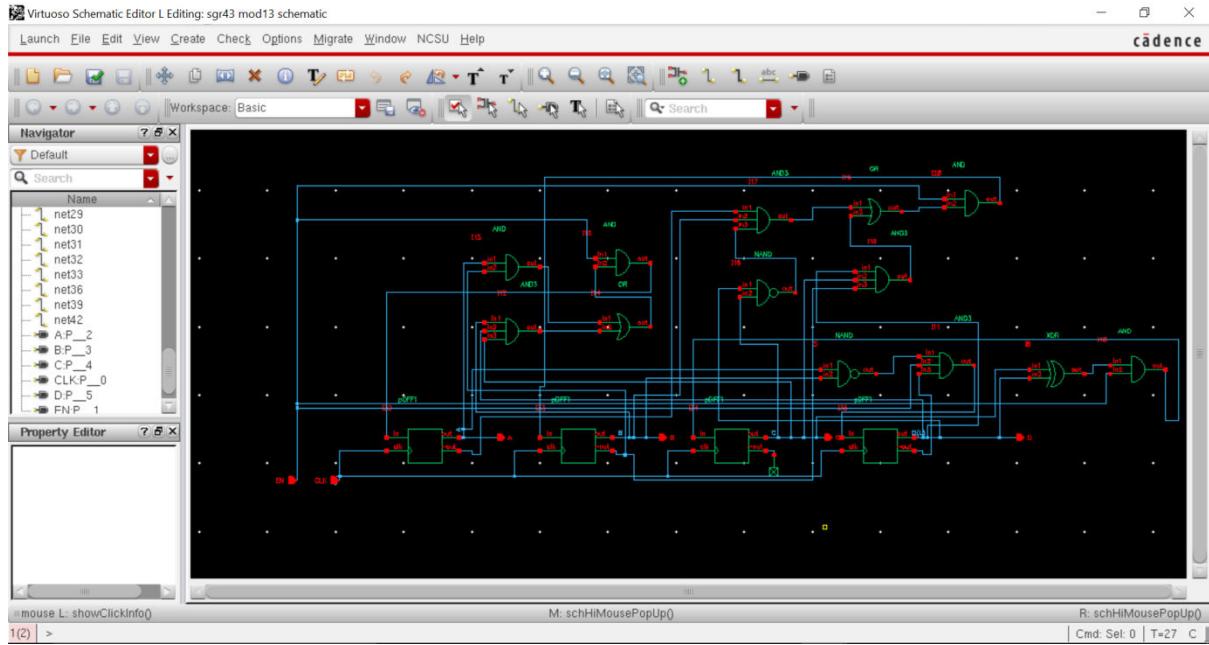


Fig. no.: 4.1

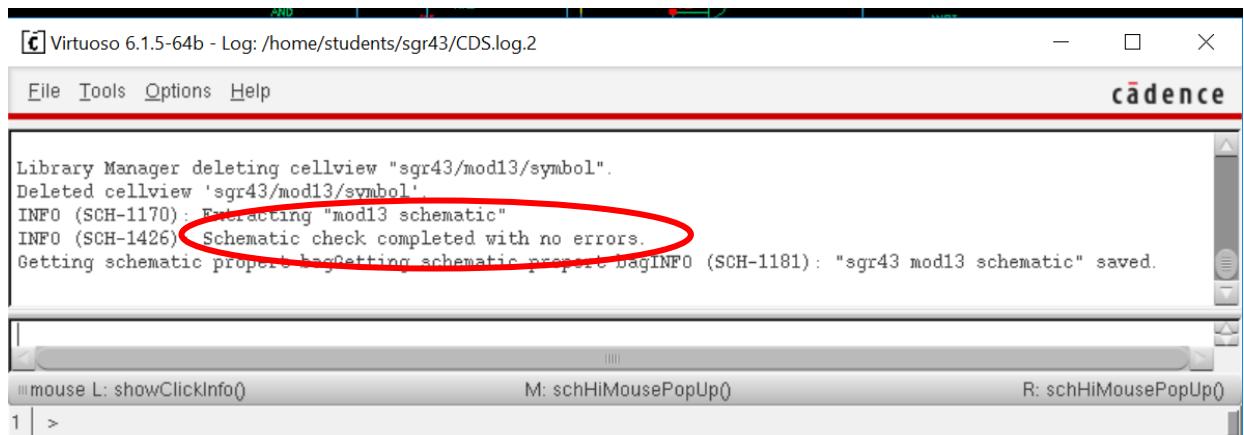


Fig. no.: 4.2

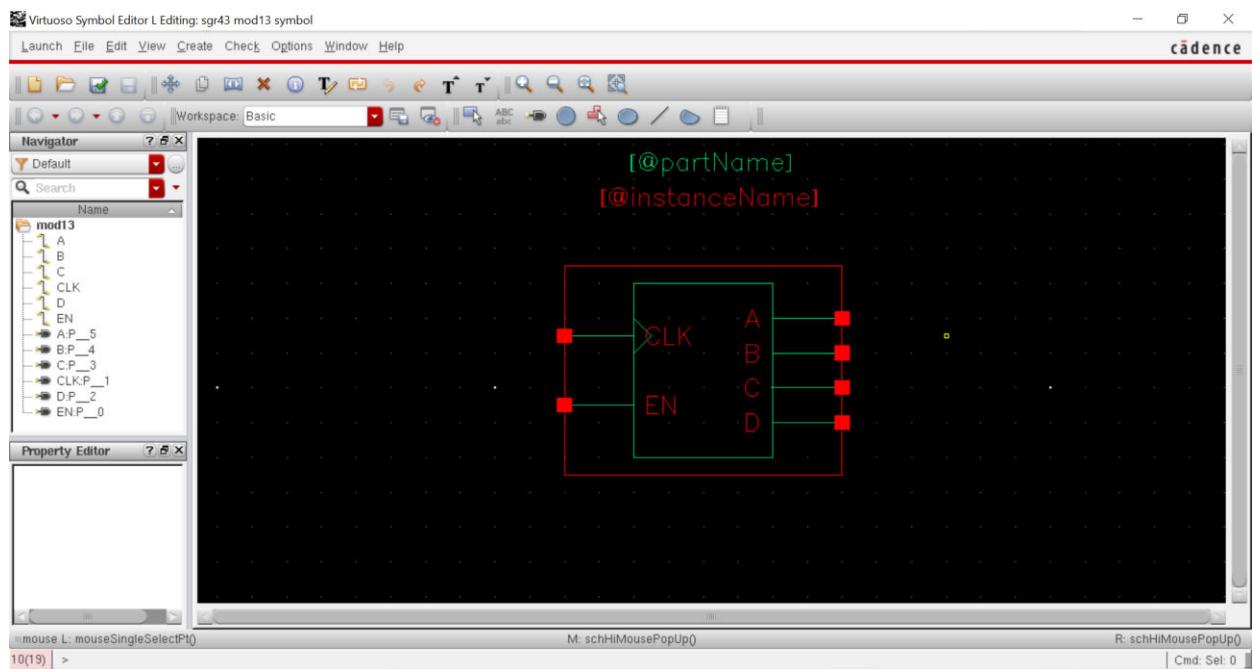


Fig. no.: 4.3

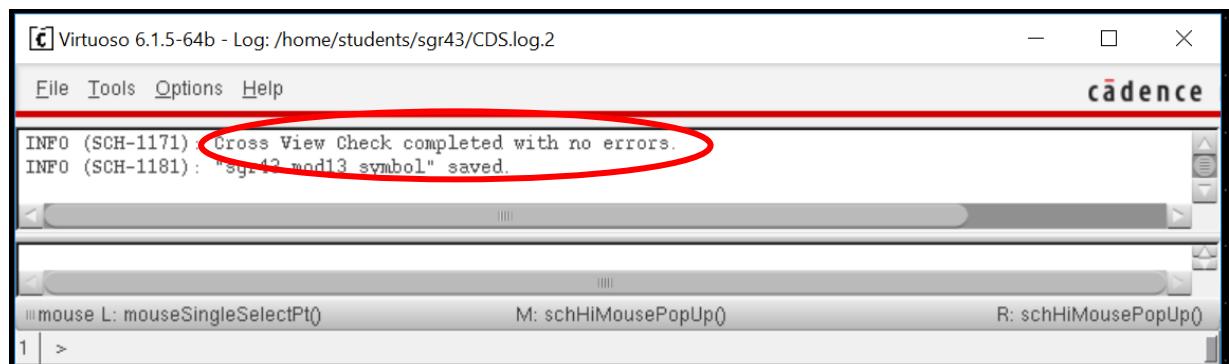


Fig. no.: 4.4

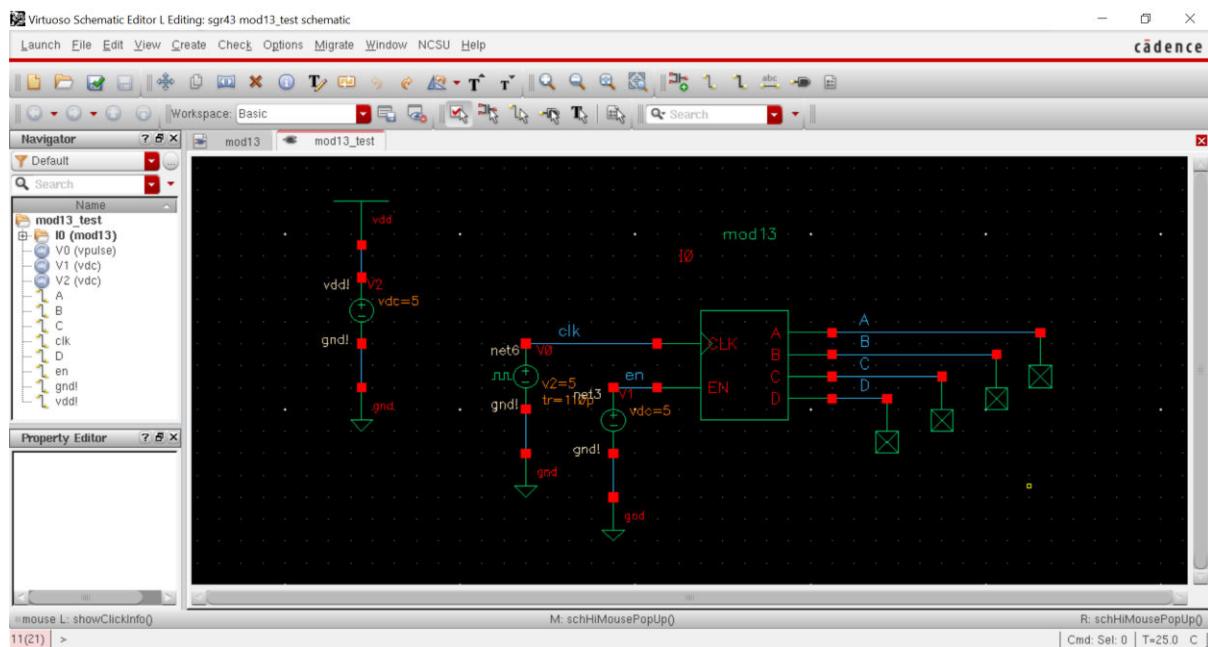


Fig. no.: 4.5

```

[c] Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence

Getting schematic property bag

vdc (instance "V2", library "NCSU Analog Parts")
INFO (SCH-1170): Extracting "mod13_test schematic"
INFO (SCH-1476): Schematic check completed with no errors.
Getting schematic property bag
INFO (SCH-1181): "sgr43 mod13_test schematic" saved.

[mouse L: showClickInfo() M: schHiMousePopUp() R: schHiMousePopUp()]
1 | >

```

Fig. no.: 4.6

```

[c] Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.2
File Tools Options Help
cadence

simulate...
INFO (ADE-3071): Simulation completed successfully.
reading simulation data...
...successful.
Getting schematic property bag

[mouse L: M: R: schHiMousePopUp()]
1 | >

```

Fig. no.: 4.7

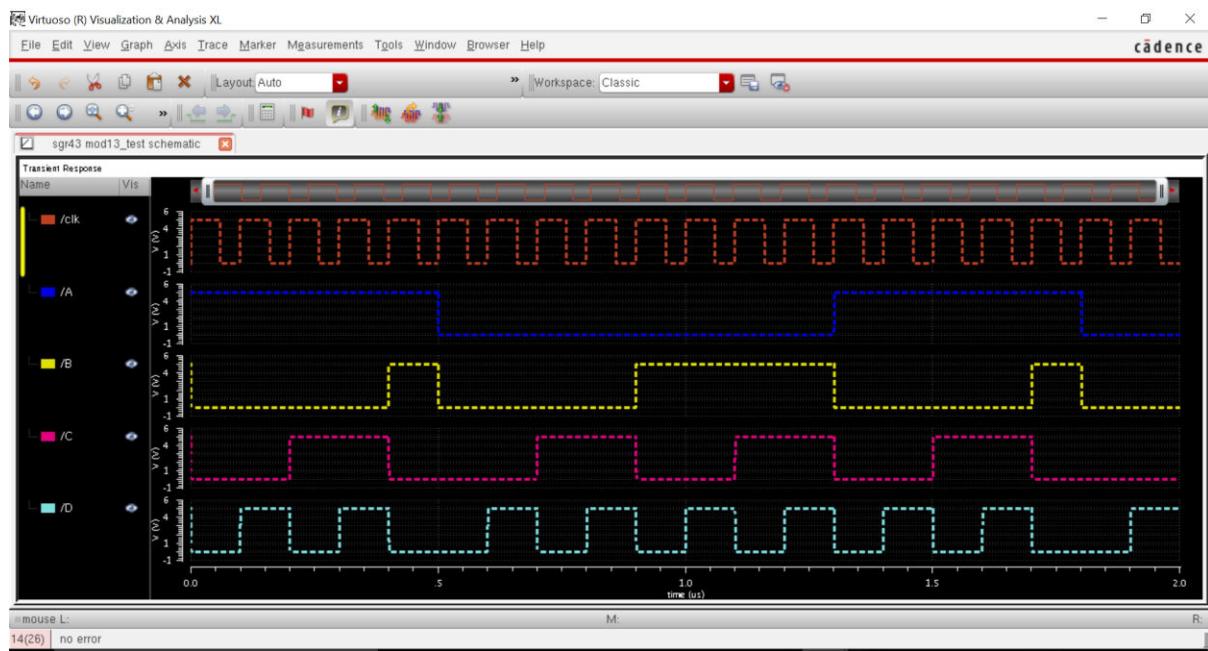


Fig. no.: 4.8

5. LAYOUT SECTION

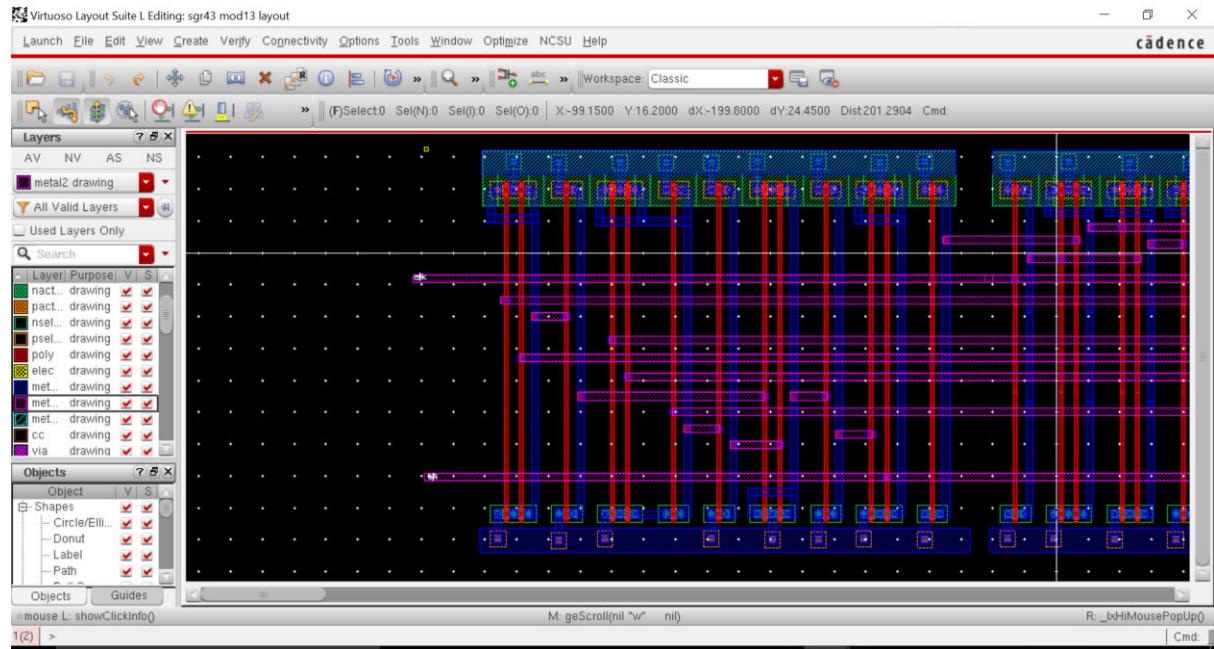


Fig. no.: 5.1

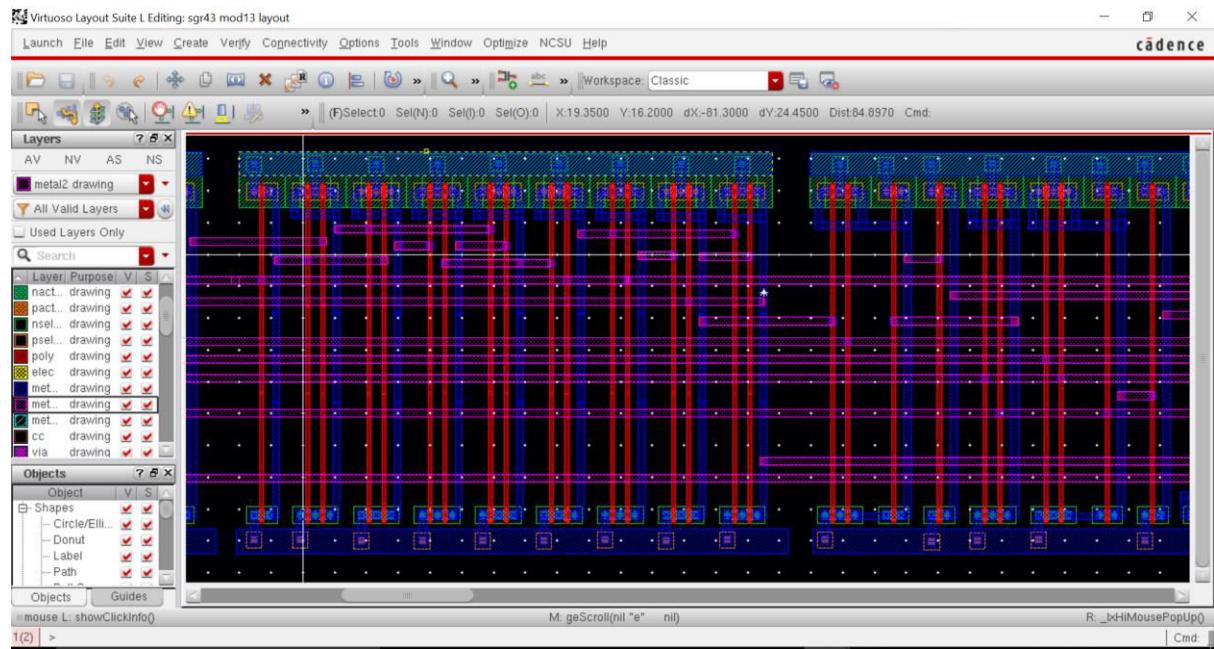


Fig. no.: 5.2

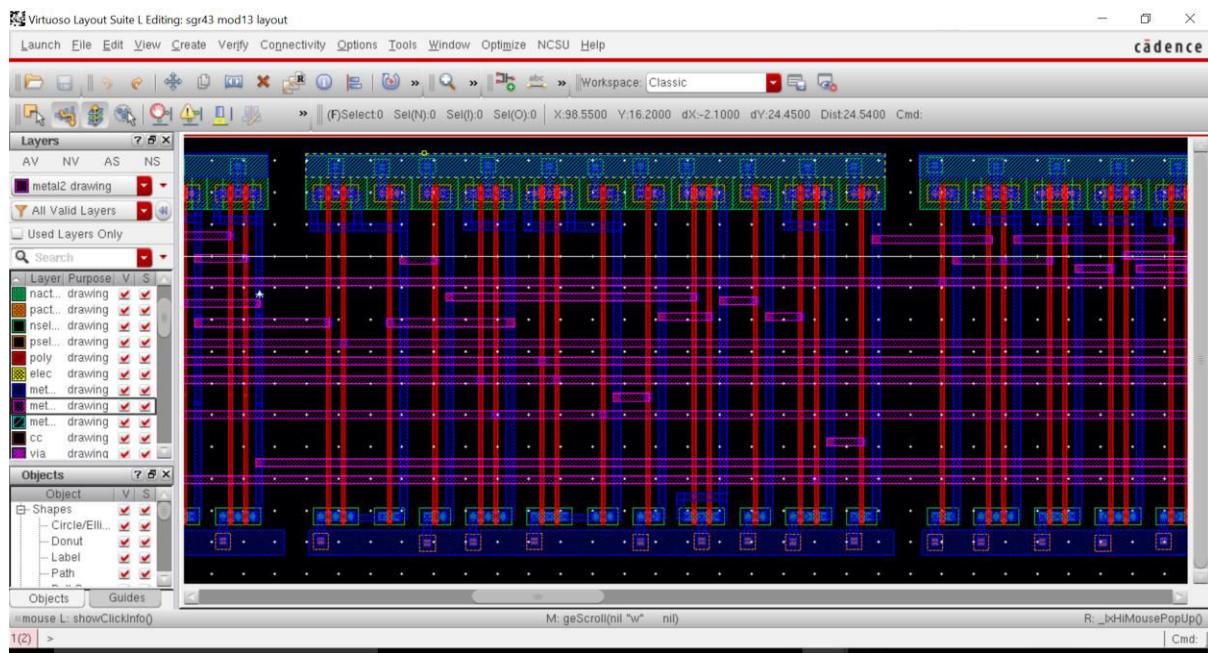


Fig. no.: 5.3

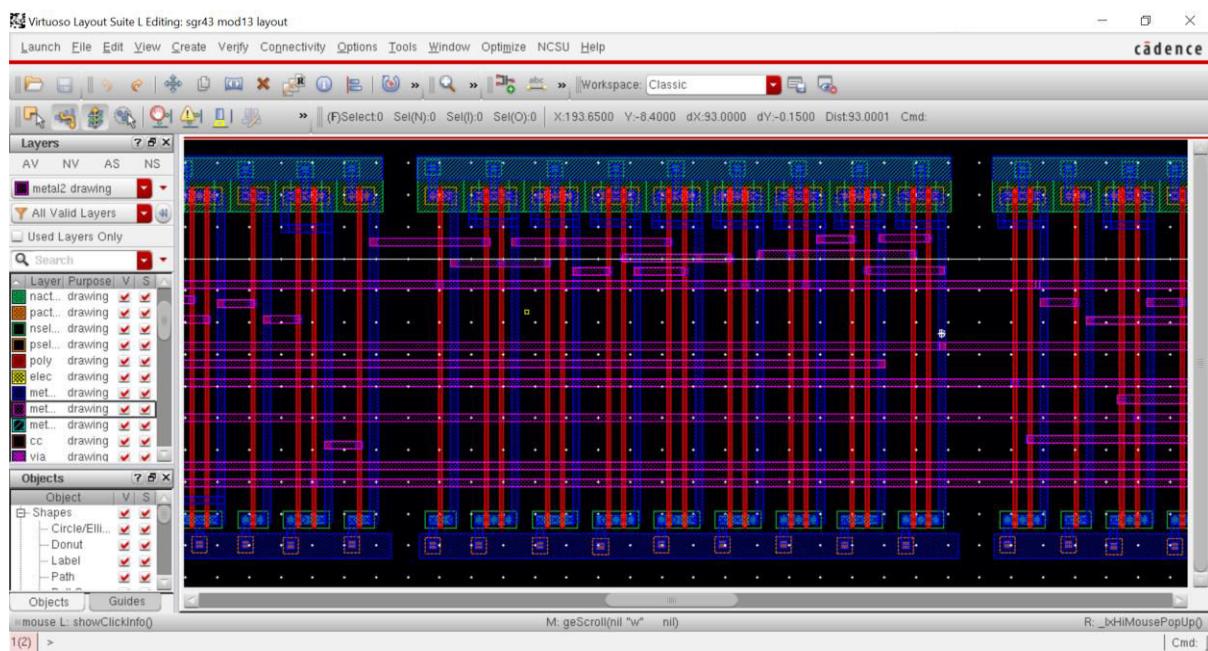


Fig. no.: 5.4

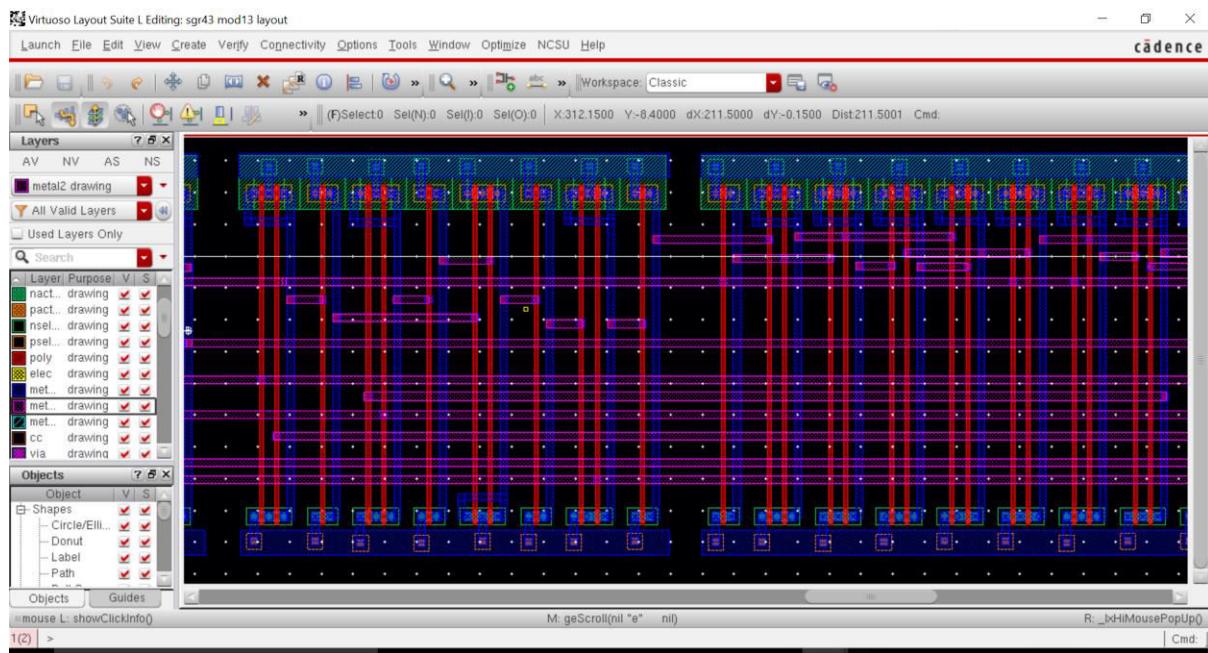


Fig. no.: 5.5

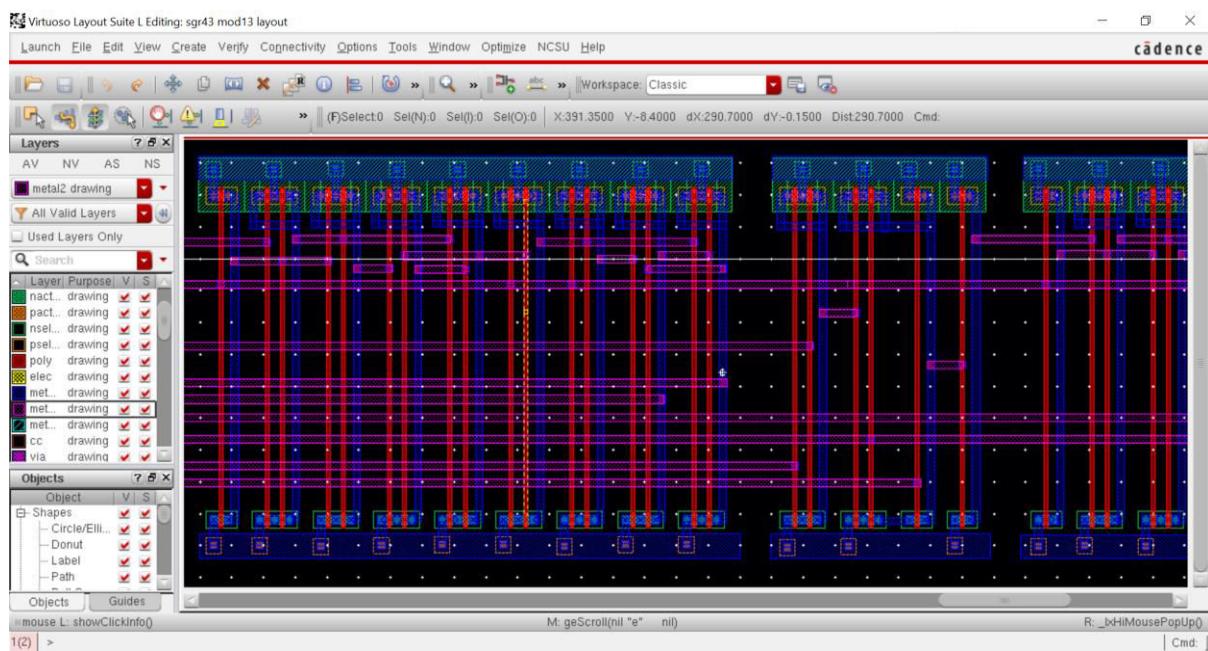


Fig. no.: 5.6

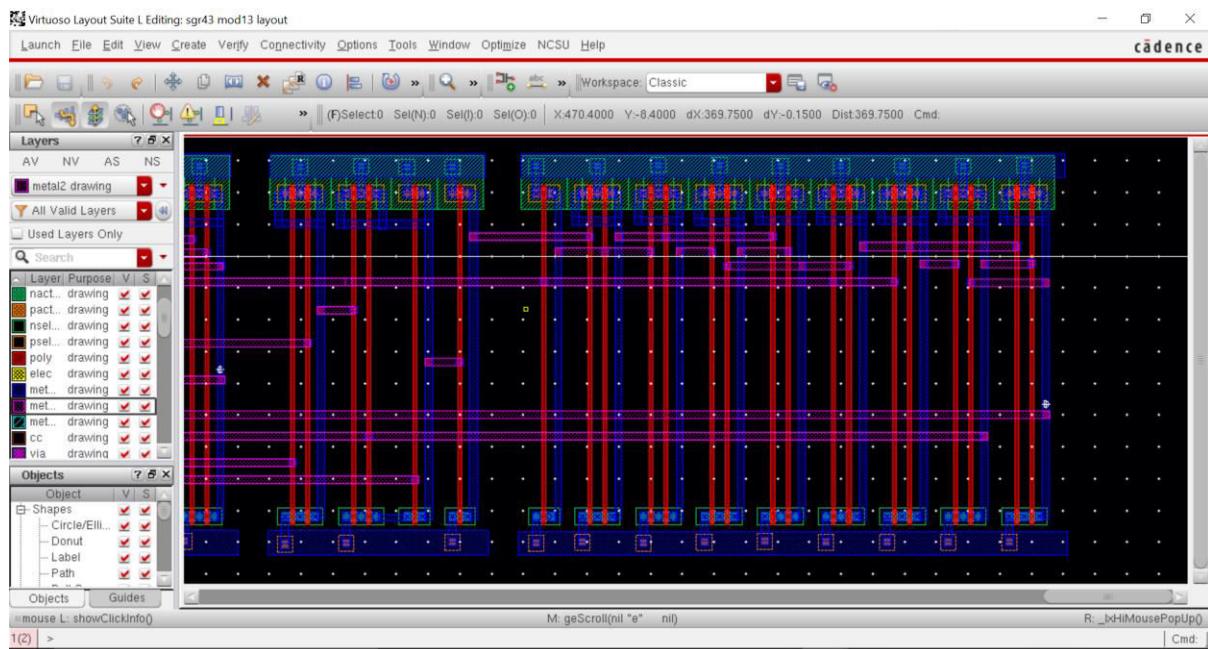


Fig. no.: 5.7

```
Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.1
File Tools Options Help
DRC started.....Fri Apr 21 21:42:01 2017
completed ....Fri Apr 21 21:42:02 2017
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "mod13 layout" *****
Total errors found: 0
```

Fig. no.: 5.8

```
Virtuoso 6.1.5-64b - Log: /home/students/sgr43/CDS.log.1
File Tools Options Help
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "mod13 layout" *****
Total errors found: 0
Saving rep sgr43/mod13/extracted
Setting layout property bag@Getting layout property bag
```

Fig. no.: 5.9

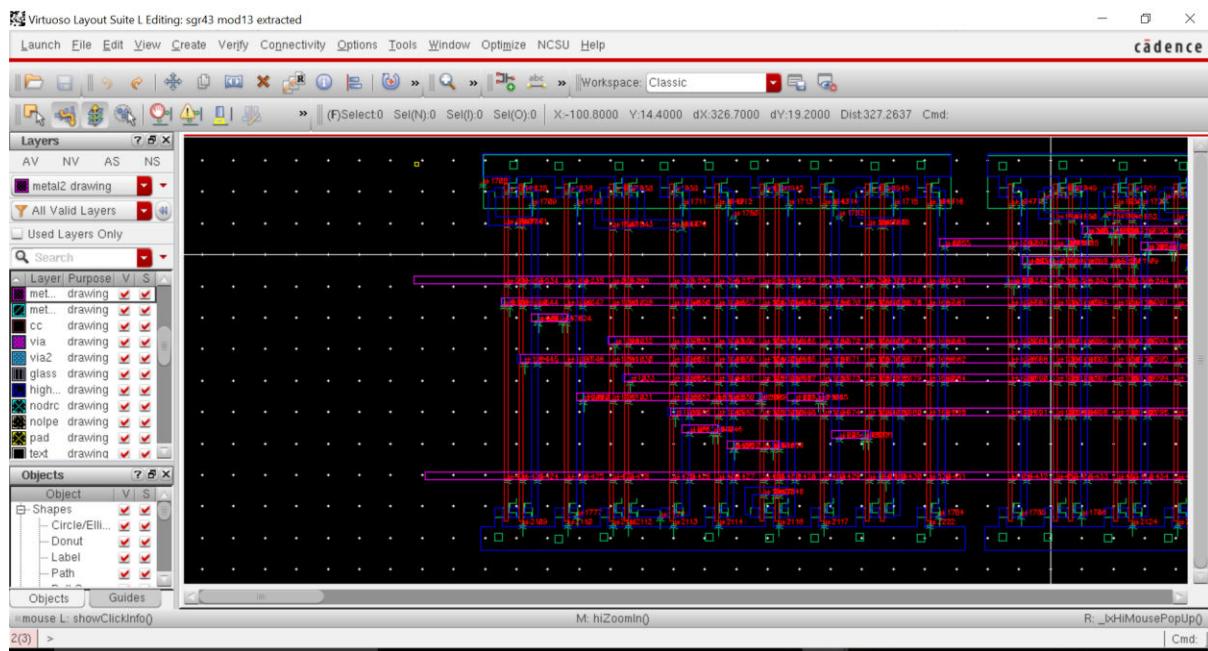


Fig. no.: 5.10

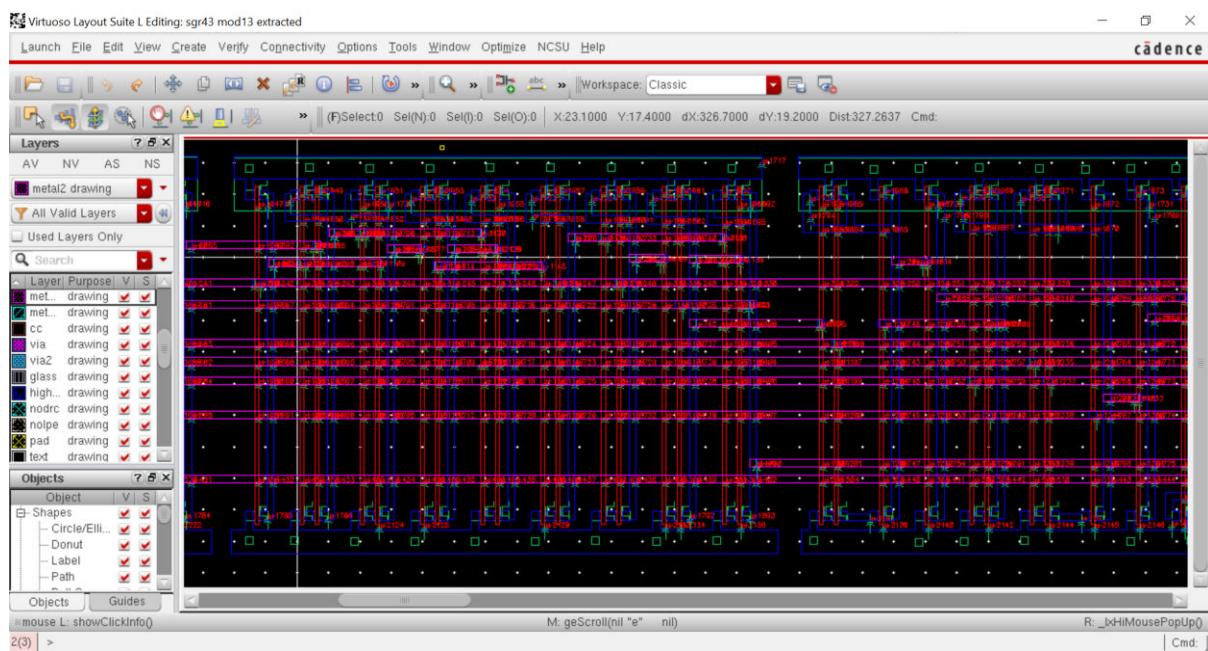


Fig. no.: 5.11

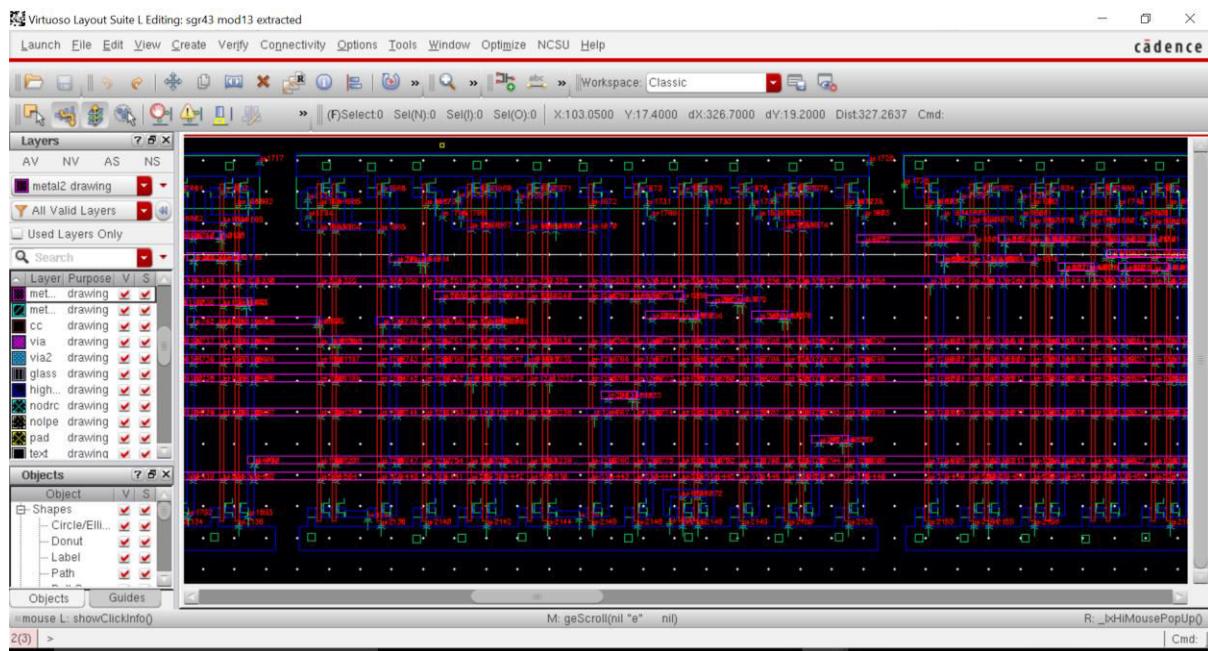


Fig. no.: 5.12

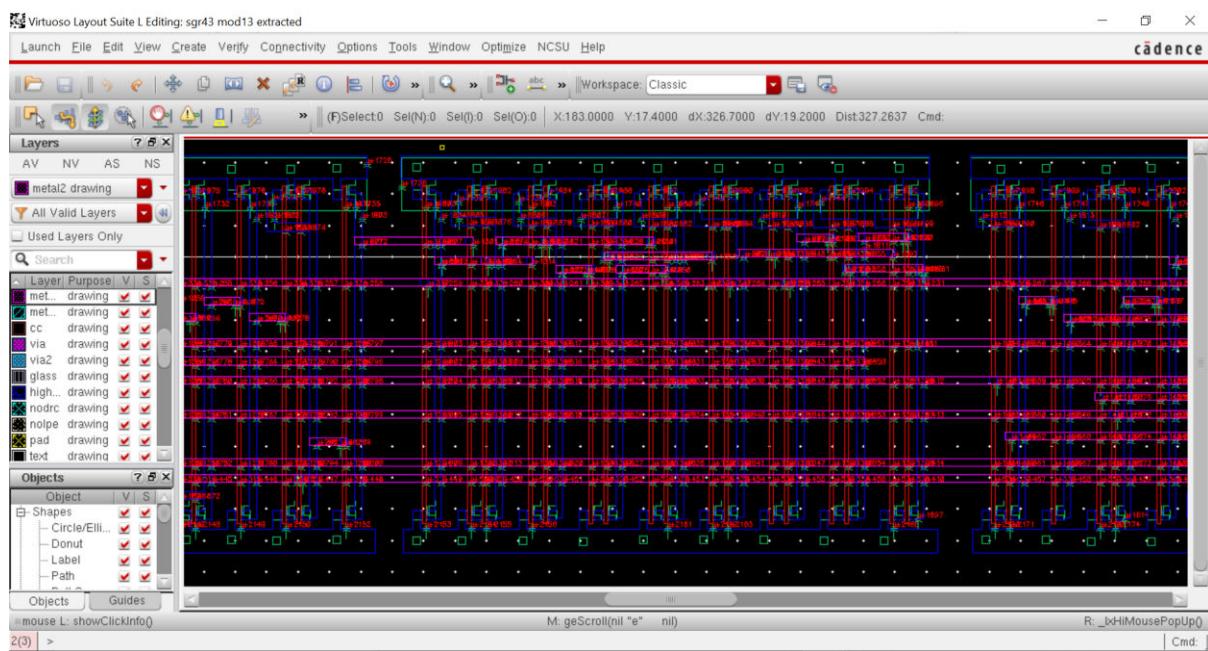


Fig. no.: 5.13

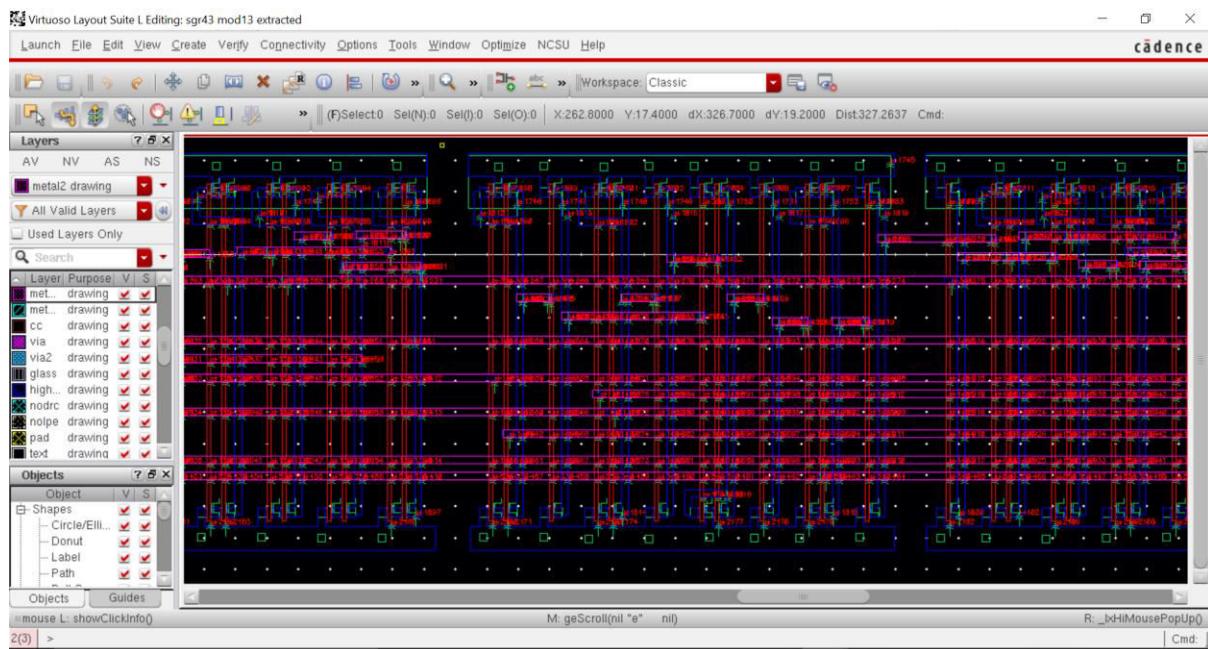


Fig. no.: 5.14

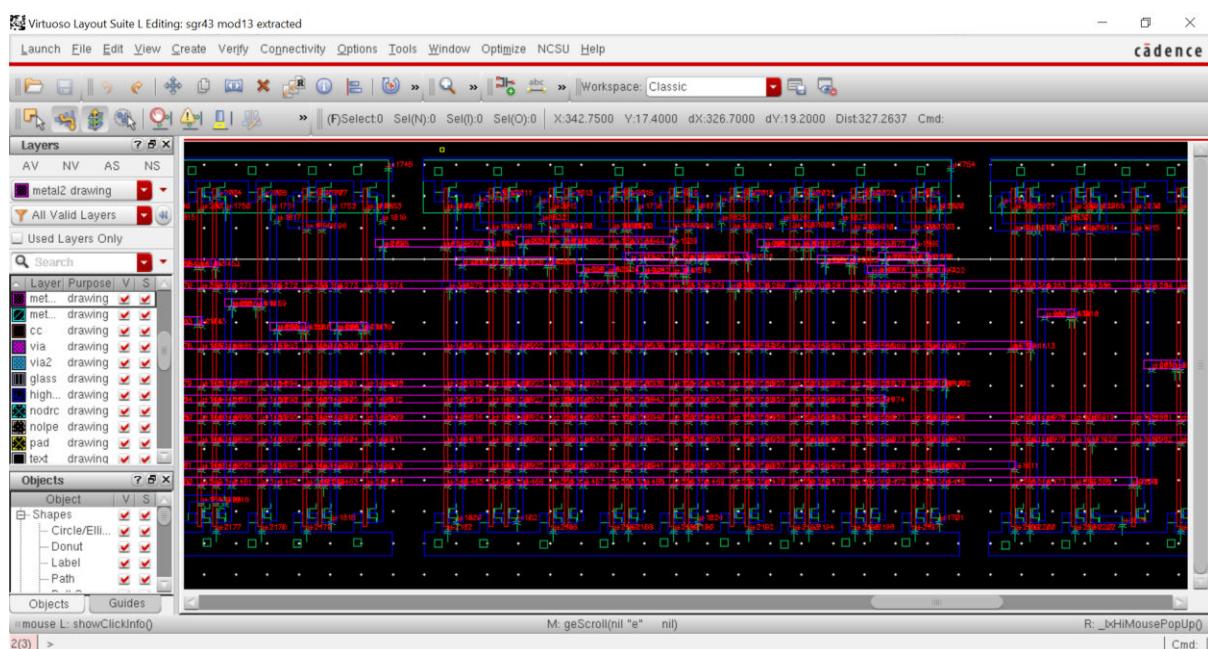


Fig. no.: 5.15

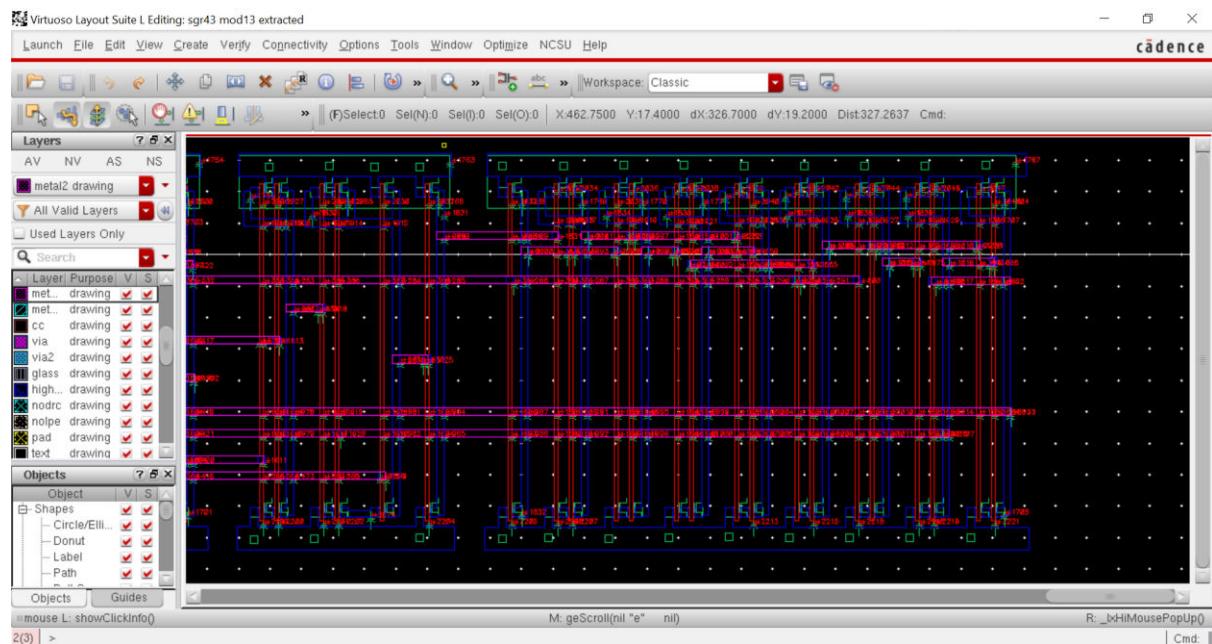


Fig. no.: 5.16



Fig. no.: 5.17



Fig. no.: 5.18

6. CONCLUSION

The design and implementation of MOD-13 synchronous up counter is successful. At the rising edge of the clock is the transition from one state to another. As the counter reaches the 13th state, it then resets to ‘0000’ and the cycle continues.

Attributes	Value
Rise-time of output waveform	110 ps
Fall-time of output waveform	110 ps
Delay	30 ns
Maximum Operating Frequency	100 GHz

Table no.: 6.1

REFERENCES

- Project 1 and Project 2 of this course (EC-5542)
- [https://en.wikipedia.org/wiki/Counter_\(digital\)](https://en.wikipedia.org/wiki/Counter_(digital))
- http://www.electronics-tutorials.ws/counter/count_3.html