# Digital Electronic Circuits
# Section 1 (EE, IE)

## Lecture 1

# Why Digital?

- **Popular terms of current times:**

  **- Digital Clock, Digital Camera, Digital Money, Digital Media, …**

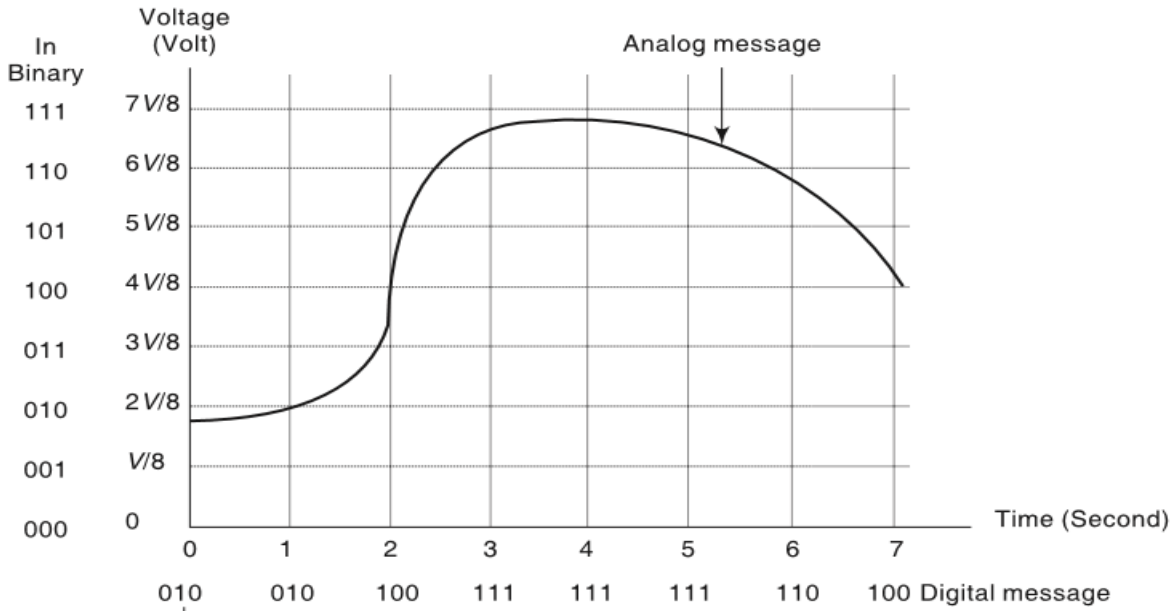
- **Prefix ‘Digital’ associates a term with digital technology.**

- **Digital technology is considered more efficient for reasons such as:**

  **- Easy to store, copy, compress**
  **- Various transmission options**
  **- Flexibility in processing**
  **- Inexpensive building block**
  **- Immunity: noise, interference**
  **- Error correction, encryption**
  **- Analysis of data**

# What is Digital?

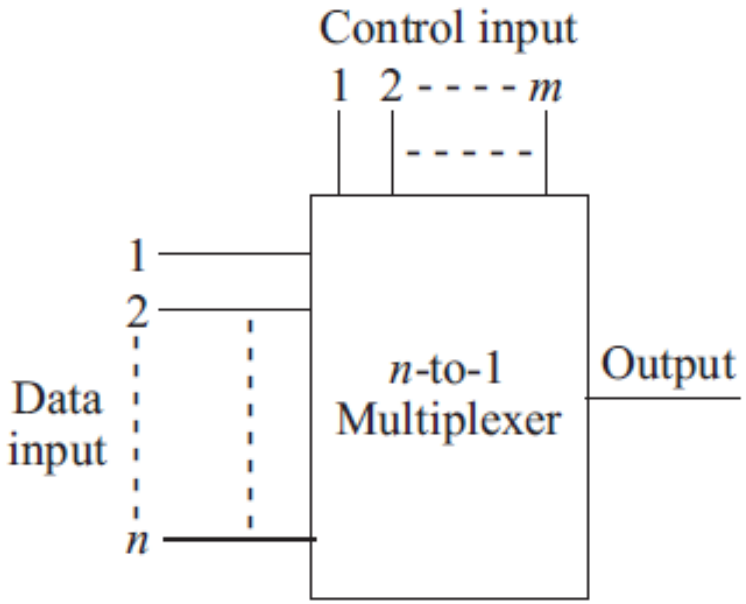
- **Digital signals represent only finite number of discreet values (2 valued: Binary).**
  **- Signal is discreet by nature - Signal, analog by nature, converted to discreet**

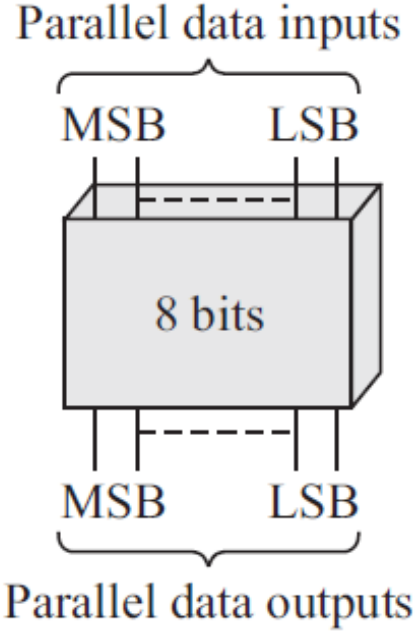



- **Digital systems represent and manipulate digital signals.**

# Manipulation of Digital Signals

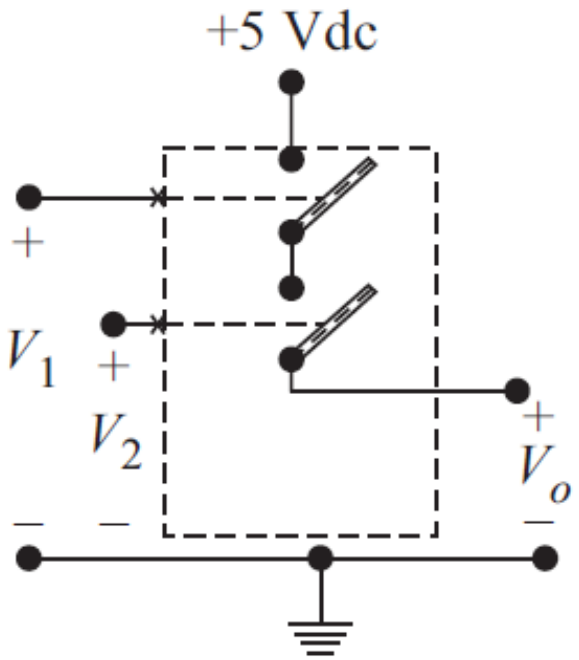
- **Switching is key to manipulation of digital signals.**
- **Digital data storage involves switching.**



# Switching & Logic Operation

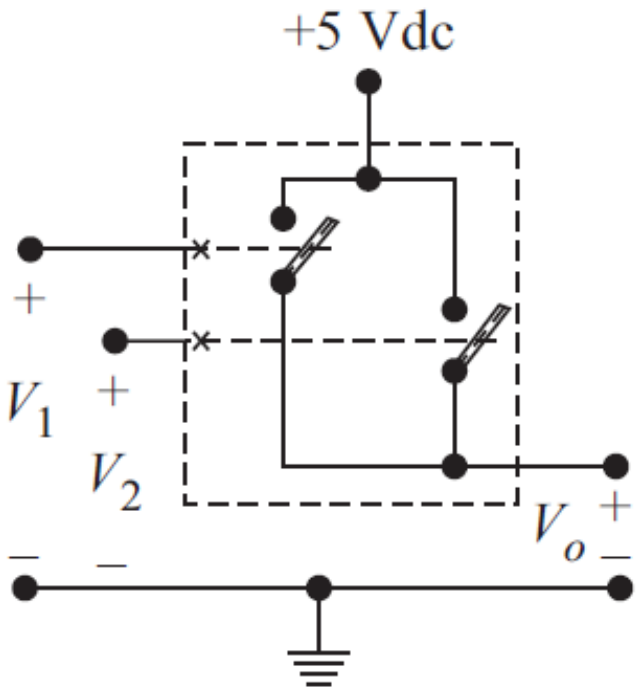
## Realization of AND




| $V_1$ | $V_2$ | $V_o$ |
|---|---|---|
| $L$ | $L$ | $L$ |
| $H$ | $L$ | $L$ |
| $L$ | $H$ | $L$ |
| $H$ | $H$ | $H$ |

# Switching & Logic Operation

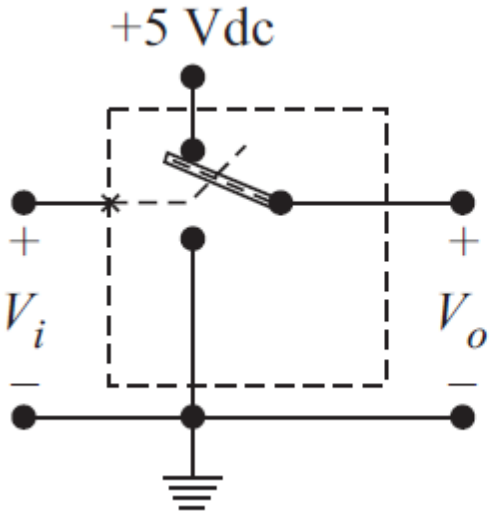
## Realization of OR



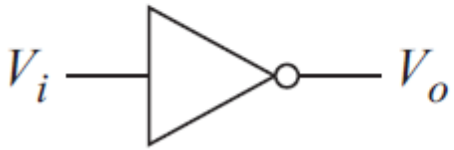

| $V_1$ | $V_2$ | $V_o$ |
|---|---|---|
| $L$ | $L$ | $L$ |
| $H$ | $L$ | $H$ |
| $L$ | $H$ | $H$ |
| $H$ | $H$ | $H$ |

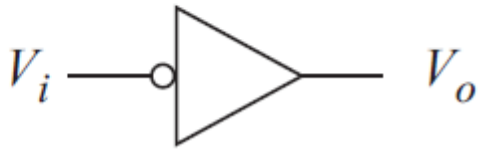
# Switching & Logic Operation

## Realization of NOT



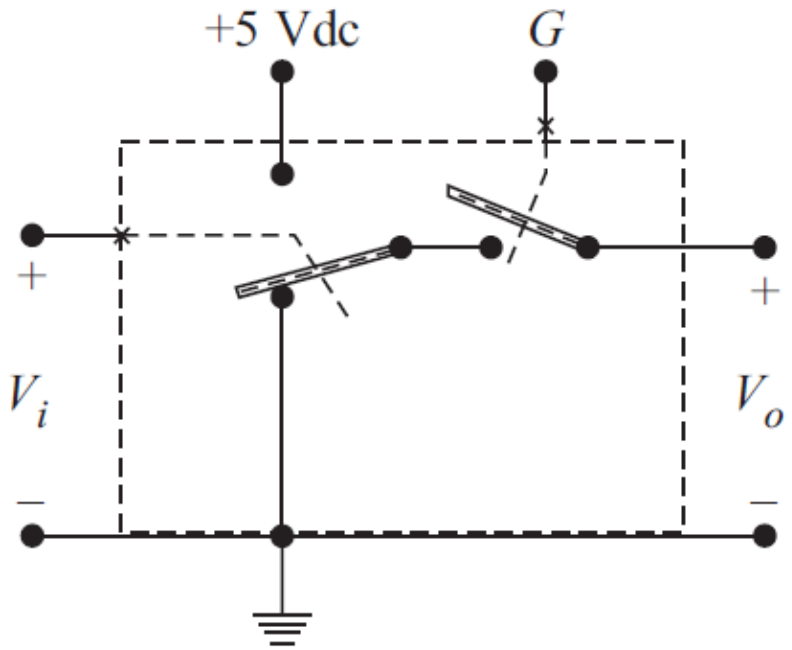

| $V_i$ | $V_o$ |
|---|---|
| $L$ | $H$ |
| $H$ | $L$ |



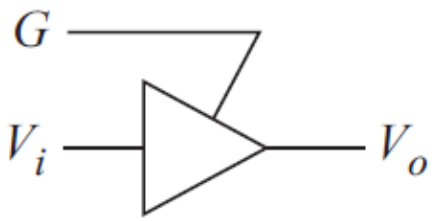



# Switching Circuits

## Realization of Tristate

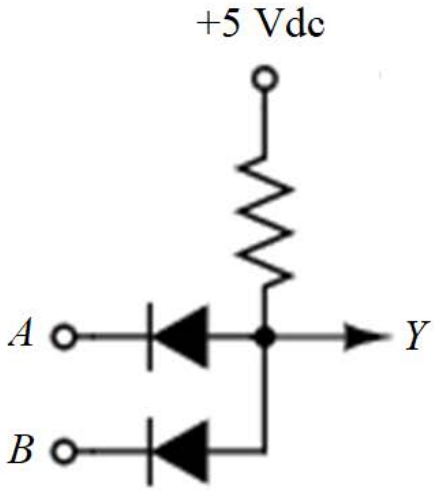



| $V_i$ | $G$ | $V_o$ |
|---|---|---|
| $L$ | $L$ | Open |
| $H$ | $L$ | Open |
| $L$ | $H$ | $L$ |
| $H$ | $H$ | $H$ |

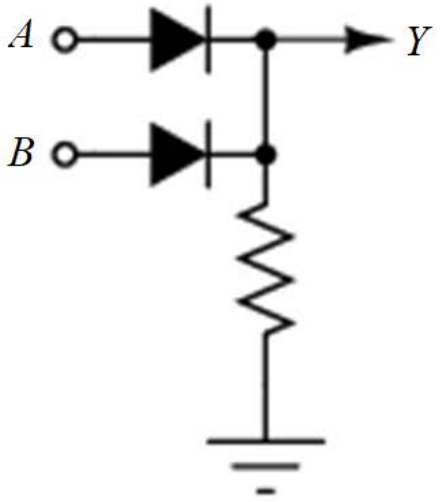


# Diode as a switch

- **Realization of AND, OR logic**




| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

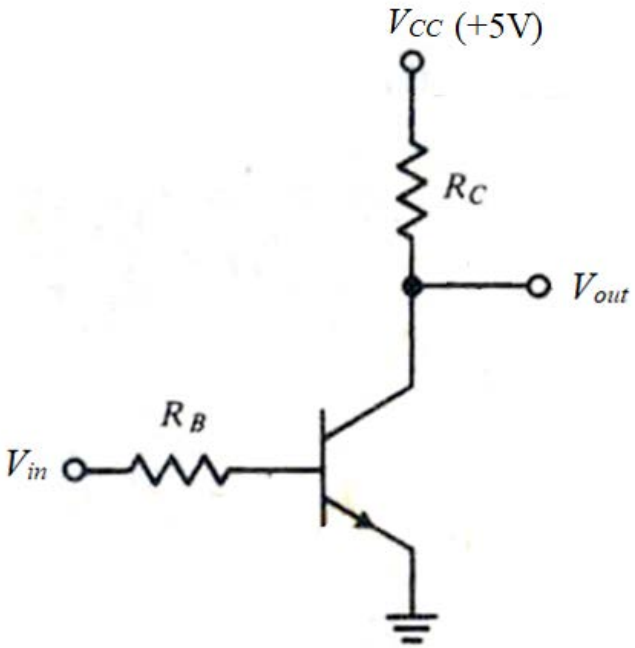


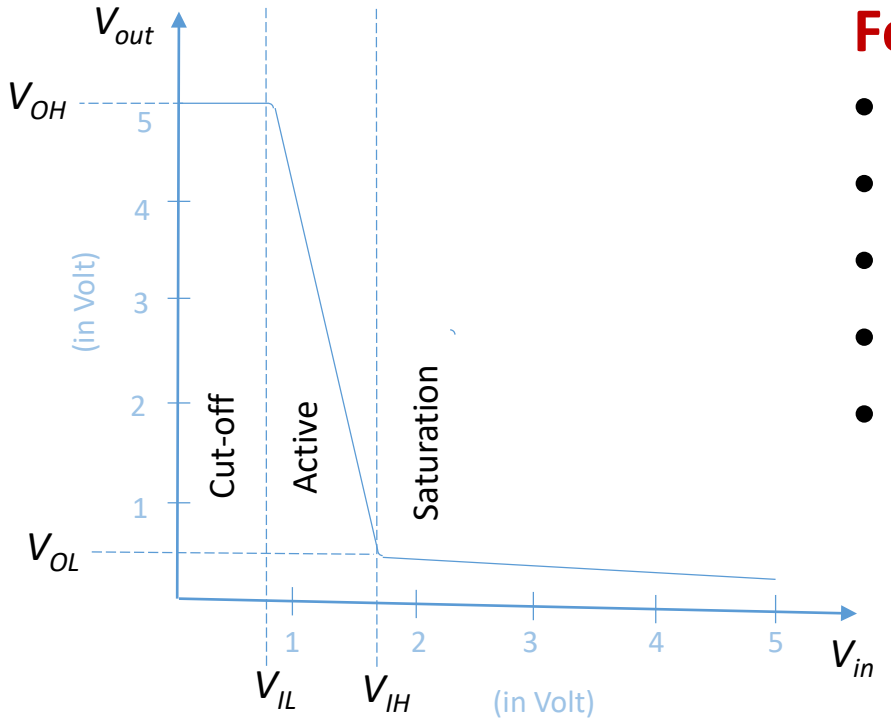

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

- **Possibility of realizing NOT logic**

# Transistor as a switch

## Realization of NOT gate (inverter), Input-Output Characteristics



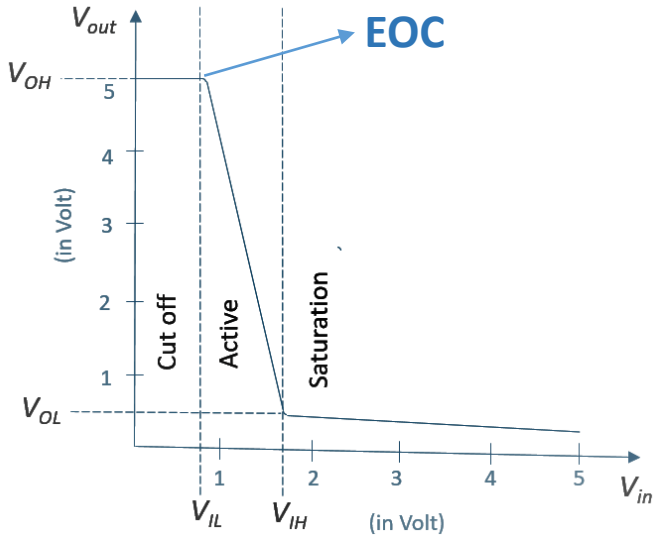

**For quantitative analysis:**

- $R_B = 10\ k\Omega$
- $R_C = 1\ k\Omega$
- $\beta_F = 50$
- $V_{BE(ON)} = V_{BE(Sat)} = 0.7V$
- $V_{CE(Sat)} = 0.2V$

# Transistor as a switch

## Cut-off region

- Base current $I_B = 0$ till $V_{BE} < 0.7V$ i.e. $V_{in} < 0.7V$.
- Transistor is *cut off* and $I_C = 0$ with $V_{out} = 5V$ over entire range.
- When $V_{in}$ is increased beyond 0.7V, base current begins to flow and the transistor moves from *cut off* region to *normal active* region.
- The coordinate, $V_{in} = 0.7V$, $V_{out} = 5V$ mark first transition point in the transfer function of this circuit. This is also termed as *breakpoint* or *edge of cutoff* (EOC).

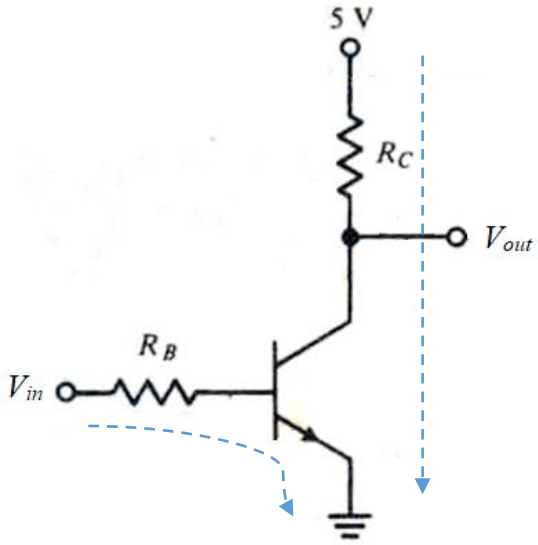


# Transistor as a switch

## Active region

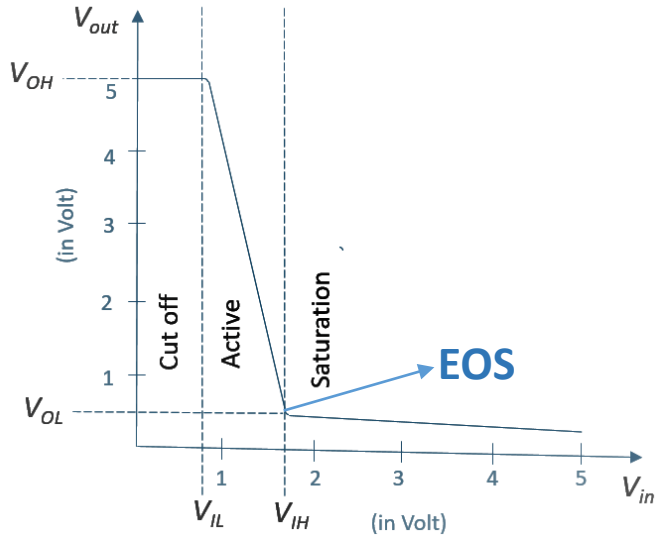
- Applying KVL along $V_{in}$, $R_B$, $V_{BE}$, Ground
  $I_B = (V_{in} - V_{BE(on)})/R_B$
- In active region, $I_C = \beta_F I_B$ (as long as $V_{CE} < V_{CE(sat)}$)
- Applying KVL along $V_{cc}$, $R_C$, $V_{CE}$, Ground
  $V_{out} = V_{CC} - I_C R_C = V_{CC} - \beta_F I_B R_C$

- Combining,
  $V_{out} = V_{CC} - \beta_F R_C (V_{in} - V_{BE(on)})/R_B$



# Transistor as a switch

## Saturation region




- As $V_{in}$ (or $I_B$) is increased a second transition point is reached when $V_{out} = V_{CE(sat)}$.

- The values of $I_C$ and $I_B$ for this condition (the subscript EOS means *edge of saturation*):

  $$I_{C(EOS)} = (V_{CC} - V_{CE(sat)})/R_C = (5\text{-}0.2)/1 = 4.8\text{mA}$$

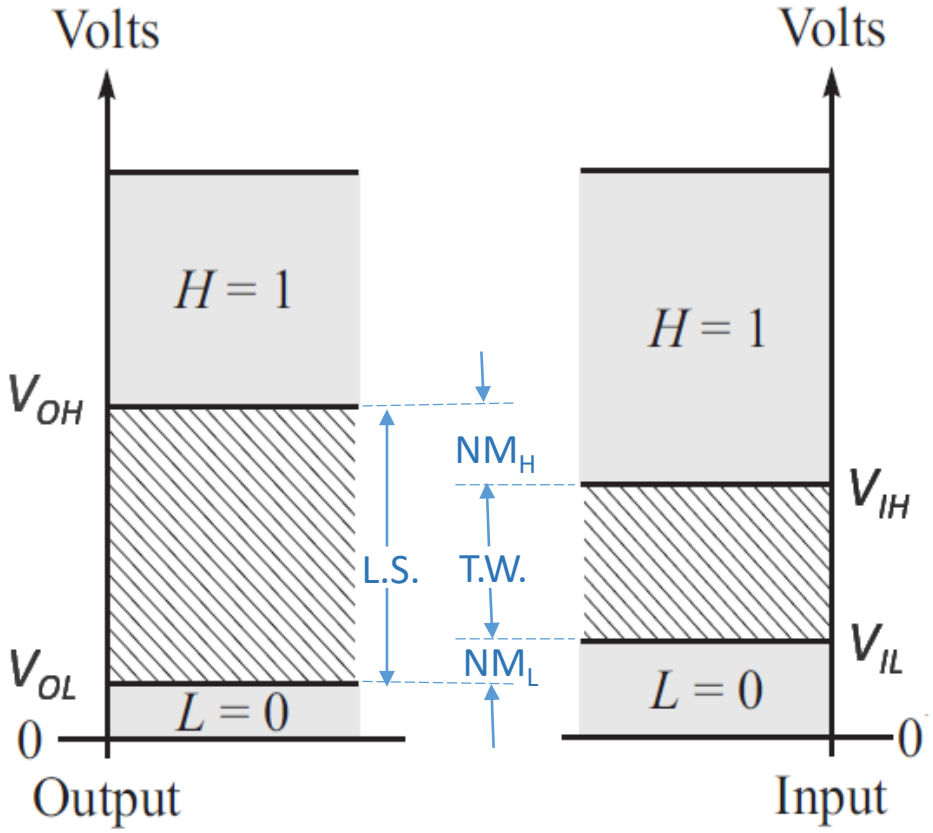
  and $I_{B(EOS)} = I_{C(EOS)}/\beta_F = 4.8/50 = 0.096\text{mA}$

  Then $V_{in(EOS)} = V_{BE(on)} + I_{B(EOS)} R_B = 0.7 + (0.096)(10) = 1.66\text{V}$

- Thus $V_{in} \geq 1.66\text{V}$ the transistor saturates. (Saturating Logic)

# Input-Output Mapping

## Noise Margin, Transition width and Logic swing




$NM_L = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5V$

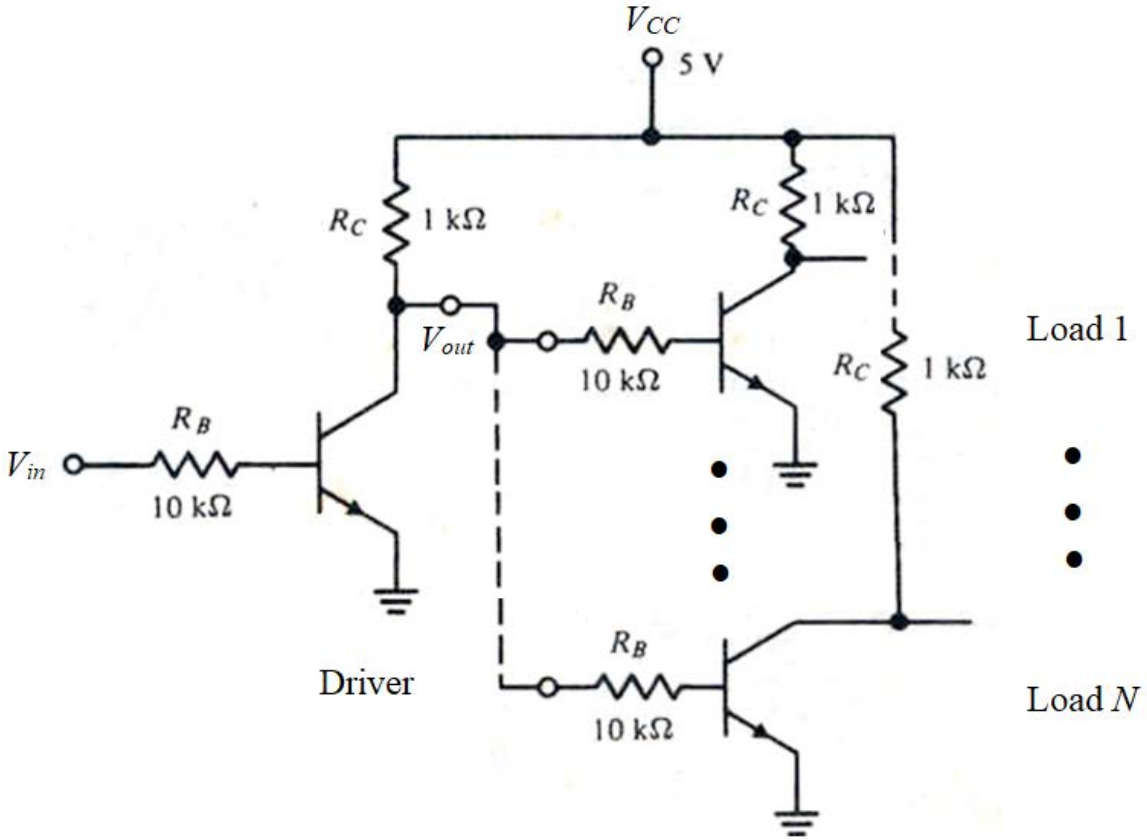
$NM_H = V_{OH} - V_{IH} = 5.0 - 1.66 = 3.34V$

Transition width = $V_{IH} - V_{IL}$
$= 1.66 - 0.7 = 0.96V$

Logic swing = $V_{OH} - V_{OL}$
$= 5 - 0.2 = 4.8V$

# Fanout

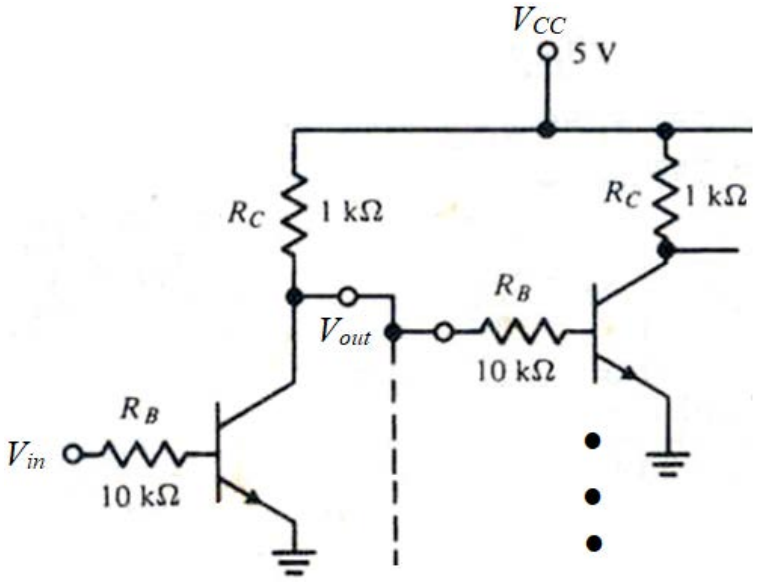
## Input to driver transistor: HIGH




- When $V_{in}$ is HIGH, driver transistor is saturated and $V_{out}$ will be LOW.
- With $V_{CE(sat)}$ = 0.2V all the load gates will be in the OFF state.
- No restriction on number of load gates

# Fanout

## Input to driver transistor: LOW




- When $V_{in}$ is LOW, driver transistor will be OFF and $V_{out}$ will be at HIGH level.
- A limit in the fanout is set when the voltage at $V_{out}$ is insufficient to saturate load gate transistors.

- Note that $V_{IH} = 1.66V$
- For driver, $I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5 - 1.66)/1 = 3.34$ mA
- For load, $I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B$

$= (1.66 - 0.7)/10 = 0.096$ mA

$N = I_{C(driver)}/I_{B(load)} = 34.79 \rightarrow 34$

# Fanout

## Effect of noise margin

- For a 0.5V noise margin,

  Minimum HIGH level voltage at $V_{out}$

  $V_{OH} = V_{IH} + NM_H = 1.66 + 0.5 = 2.16V$

- Similar calculation as before with $V_{out}$ at 2.16V gives

  $I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5 - 2.16)/1 = 2.84$ mA

  $I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B = (2.16 - 0.7)/10 = 0.15$ mA

  $N = I_{C(driver)}/I_{B(load)} = 19.4 \rightarrow 19$

- An increased $NM_H$ reduces fanout even further

**Other factors:**

Variation in $\beta_F$, $V_{BE(sat)}$, $V_{CE(sat)}$, $V_{CC}$, $R_C$, $R_B$.

# References:


- Grinich, V.H., and H.G. Jackson, Introduction to Integrated Circuits, McGraw-Hill
- Donald P. Leach, Albert P. Malvino and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Herbert Taub, and Donald Schilling, Digital Integrated Electronics, McGraw Hill
- M. Morris Mano, and Michael D. Ciletti, Digital Design 5e, Pearson