Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 18

Class Test 2:
27-10-2020 (TUE): Starting 10:15 AM
(additional holiday after Dusserah)

Syllabus: Logic families (not covered in CT1) and primarily post CT1, shall include concept dealt in pre-CT1 part which forms the pre-requisite.

Binary Multiplication

0 x 0 = 0
0 x 1 = 0
1 x 0 = 0
1 x 1 = 1

x	*y*	*m*
0	0	0
0	1	0
1	0	0
1	1	1

m = x.y

```
  1101
    10
 ---------
  0000
 1101
---------------
 11010
```

$(13)_{10}$
$(2)_{10}$

$(26)_{10}$

```
  1101
    11
Carry 11---------
  1101
 1101
---------------
100111
```

$(13)_{10}$
$(3)_{10}$

$(39)_{10}$

Factors { Multiplicand, Multiplier

Product

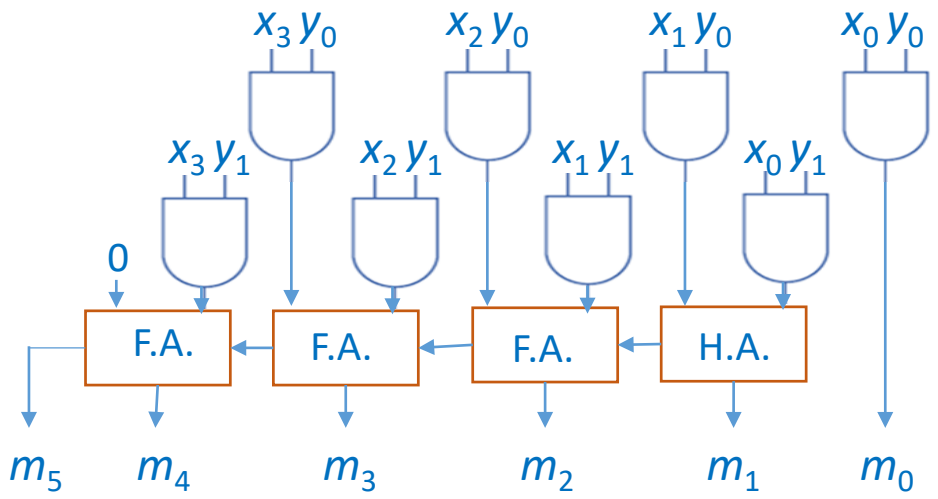
```
  1101
  1011
Carry 1111---------
  1101
 1101
0000
1101
------------------
10001111
```

$(13)_{10}$
$(11)_{10}$

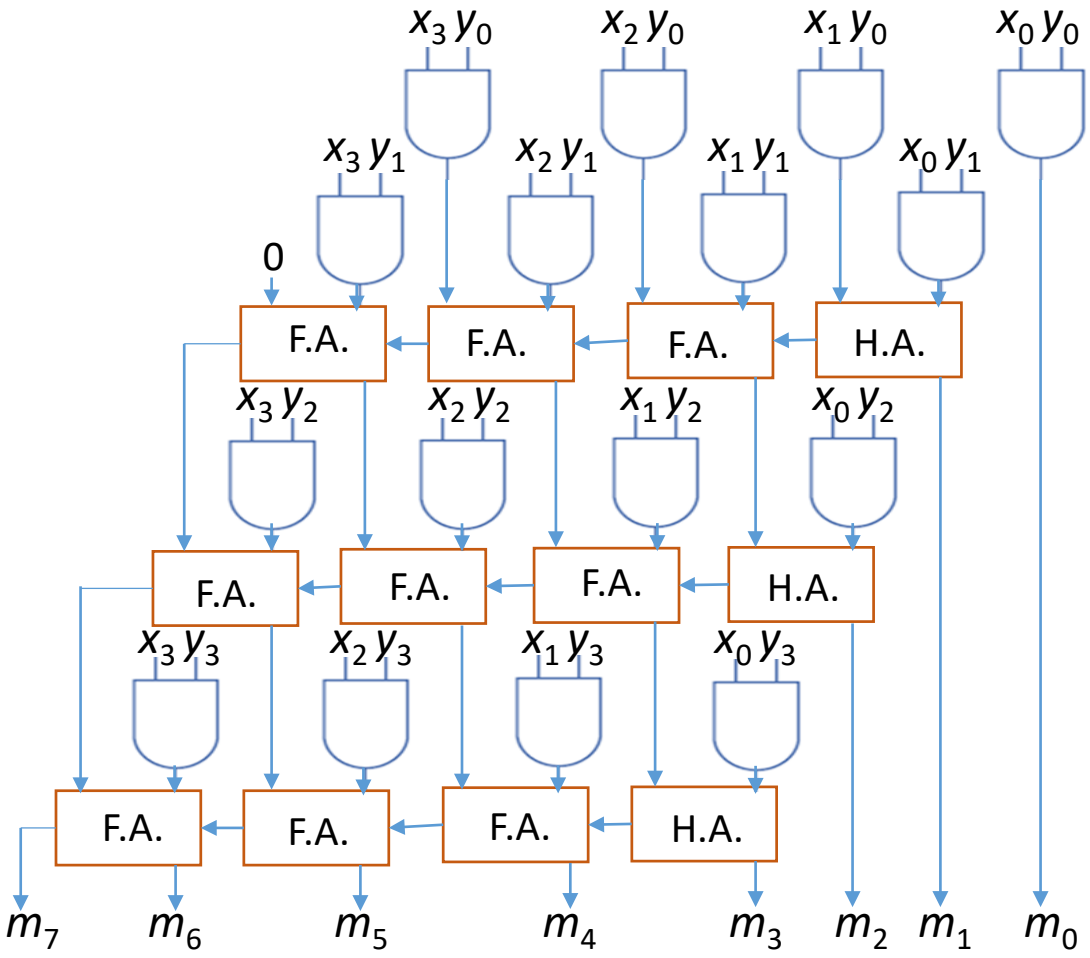
$(143)_{10}$

4-bit x 2-bit Multiplication

$$
\begin{array}{rrrrrr}
 & & & x_3 & x_2 & x_1 \; x_0 \\
 & & & & y_1 & y_0 \\
\hline
 & & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\
 & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & \\
\hline
m_5 & m_4 & m_3 & m_2 & m_1 & m_0
\end{array}
$$



4-bit x 4-bit Multiplication



Example: $x_3x_2x_1x_0$: 1101
$y_3y_2y_1y_0$: 1011

0 1 1 1 1 0 0 1 **1** ← 1st row adder

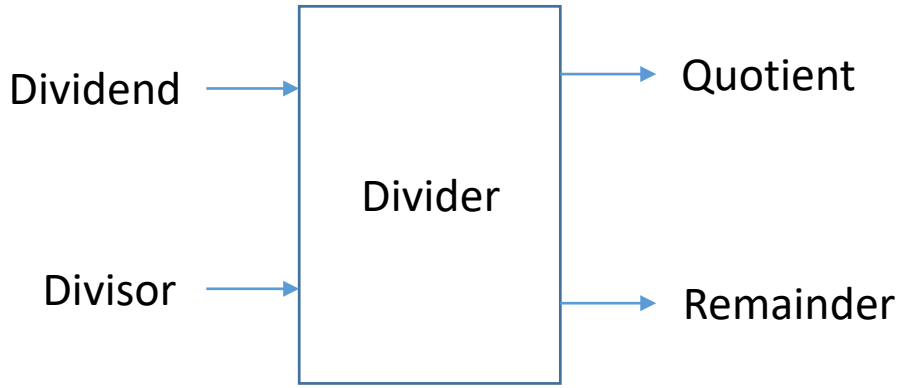
1 0 0 0 0 0 1 0 **1** ← 2nd row adder

0 1 1 1 0 0 0 1 **1** ← 3rd row adder

1 0 0 0 1

Result: 10001111

Binary Division



Dividend = Divisor x Quotient + Remainder

$$D = d \times q + r$$

```
      (0)11
   11 | 1011
        00
        ---
        101
         11
        ---
        101
         11
        ---
         10
```

$D = (1011)_2 = (11)_{10}$

$d = (11)_2 = (3)_{10}$

$q = (11)_2 = (3)_{10}$

$r = (10)_2 = (2)_{10}$

```
        1001
  1101 | 1110101
         1101
         ----
         0011
         0000
         ----
          0110
          0000
          ----
          1101
          1101
          ----
```

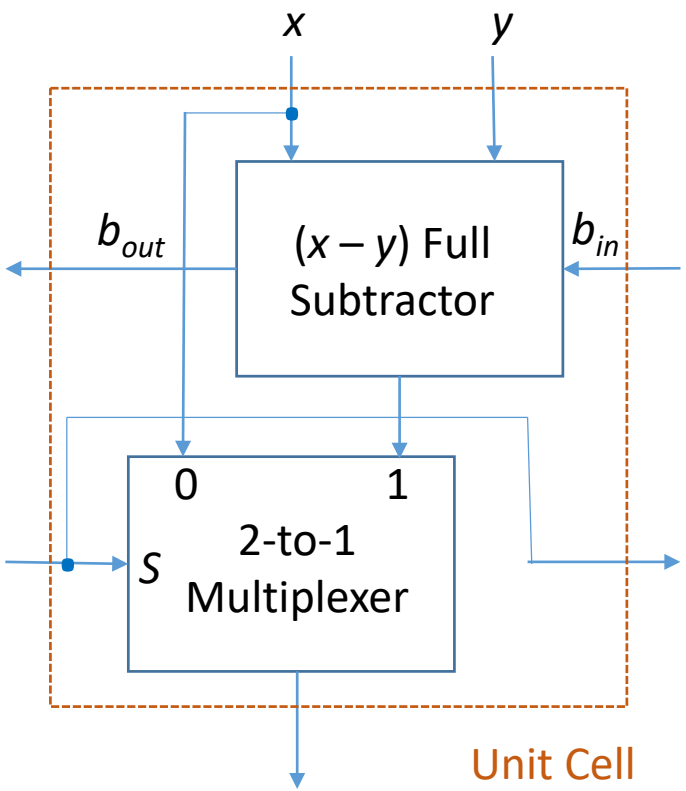
$D = (1110101)_2 = (117)_{10}$

$d = (1101)_2 = (13)_{10}$

$q = (1001)_2 = (9)_{10}$

$r = 0$

Unit Cell for Divider Array



b_{in}	x	y	d	b_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Full Subtractor

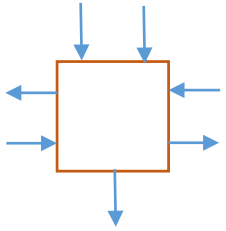
$d = x \oplus y \oplus b_{in}$

$b_{out} = x'.y + x'.b_{in} + y.b_{in}$

S	Y
0	D_0
1	D_1

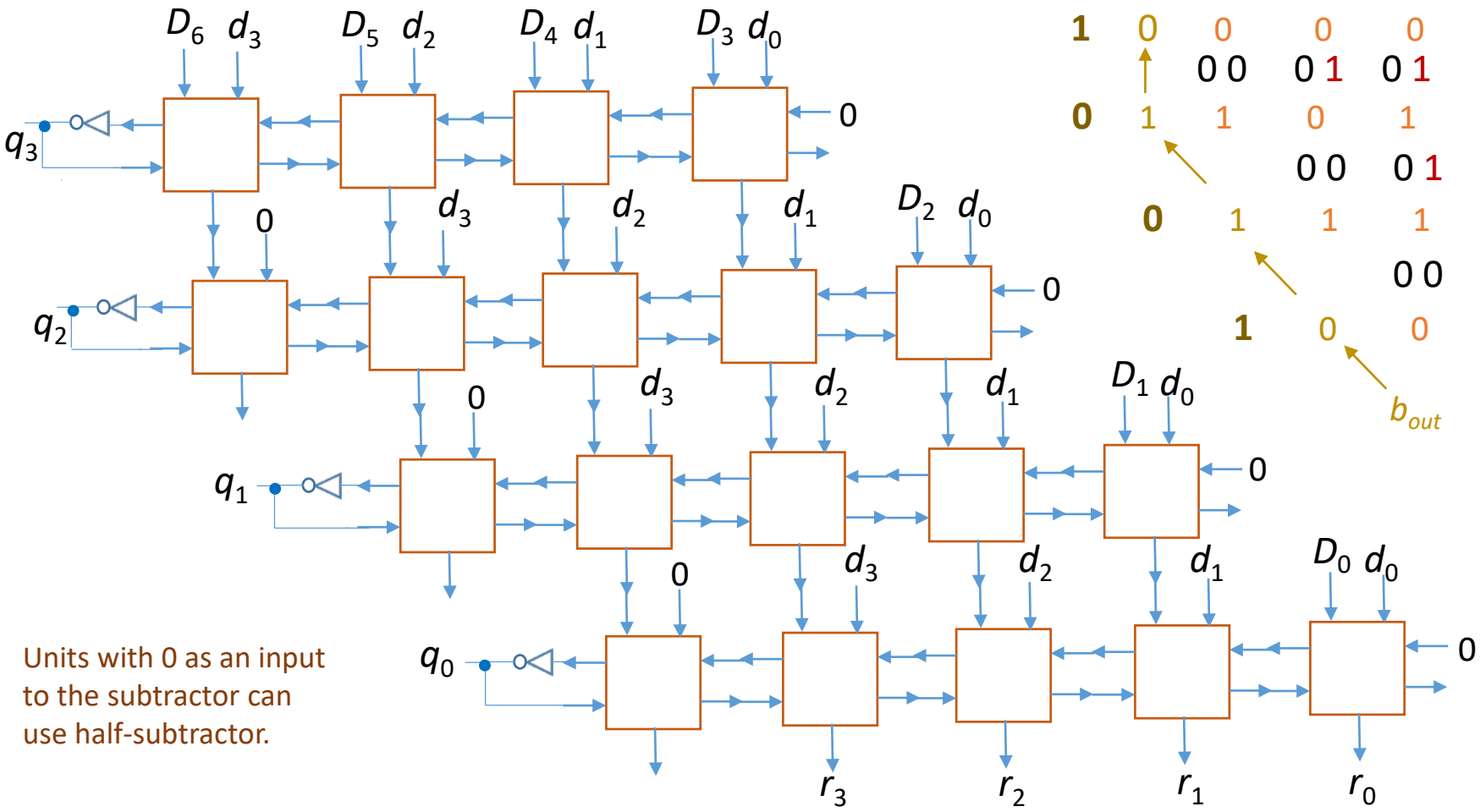
$Y = S'.D_0 + S.D_1$

2-to-1 Multiplexer

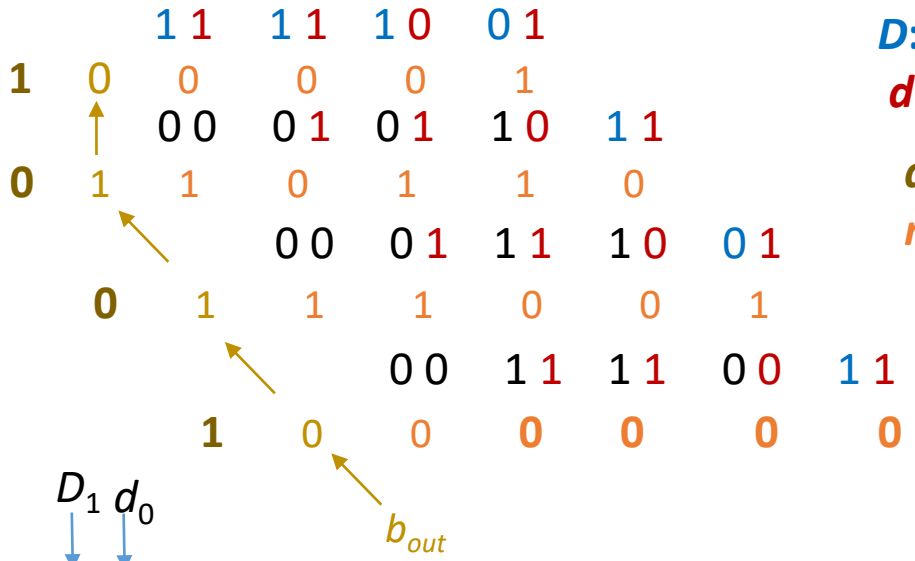


Unit Cell

A Divider Circuit



Units with 0 as an input to the subtractor can use half-subtractor.



Example:

***D*: 1110101**

***d*: 1101**

***q*: 1001**

***r*: 0000**

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Lloris Ruiz A., Castillo Morales E., Parrilla Roure L., García Ríos A. Number Systems. In: Algebraic Circuits. Intelligent Systems Reference Library, vol 66. Springer, Berlin, Heidelberg