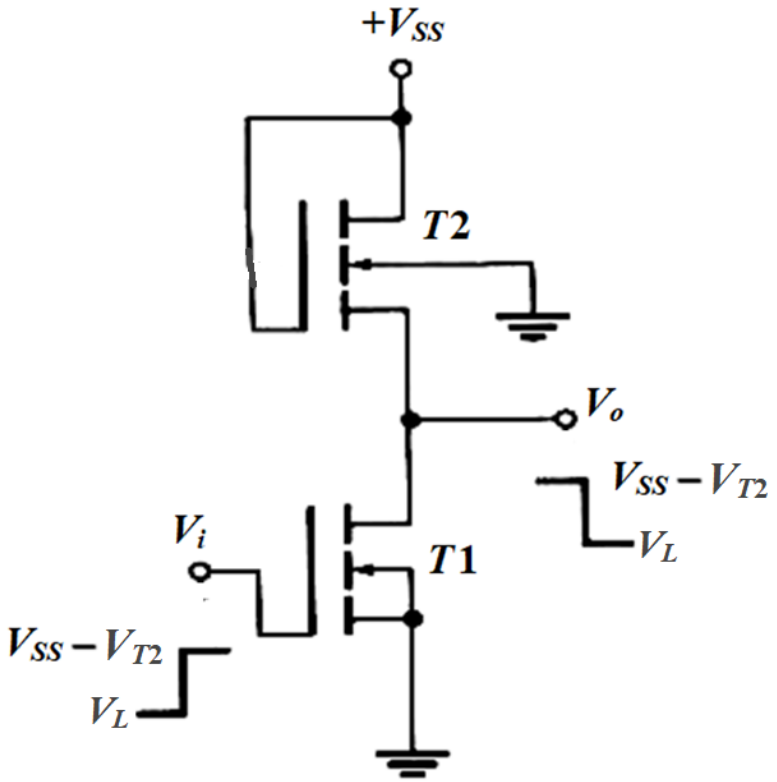
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 29

NMOS Gate



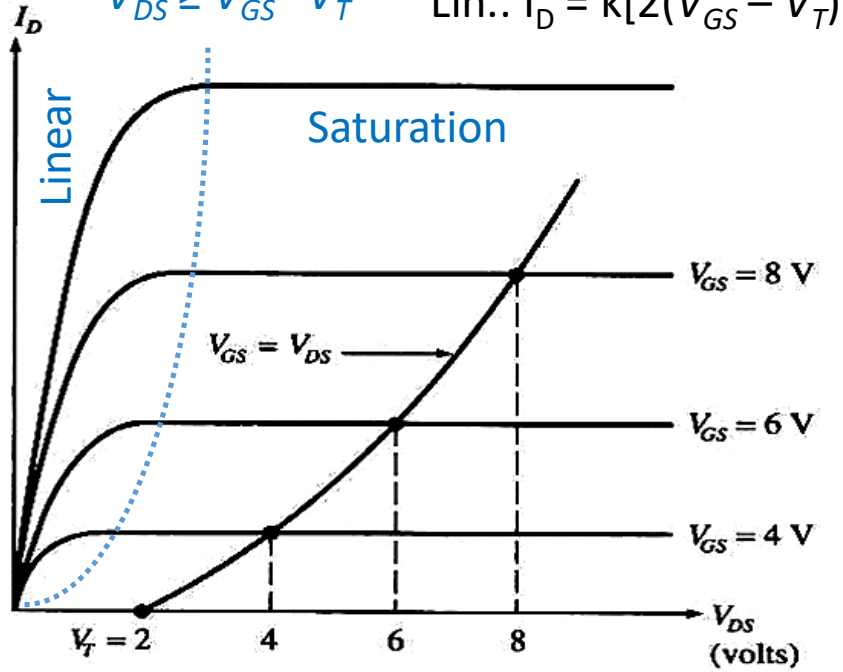
Inverter with NMOS as resistance

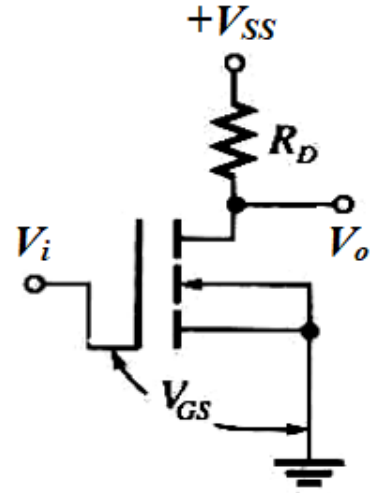
Pinch-off

$V_{DS} \geq V_{GS} - V_T$

Sat.: $I_D = k(V_{GS} - V_T)^2$

Lin.: $I_D = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$



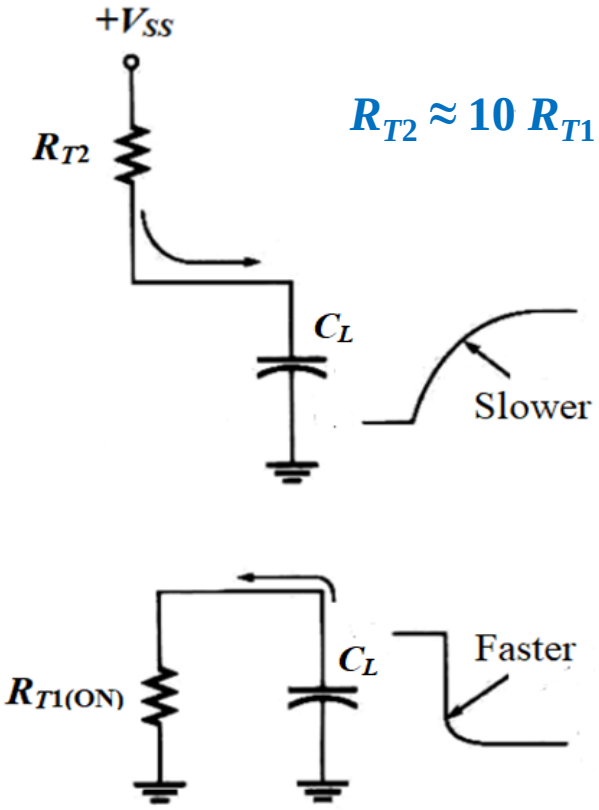


Saturation region:
Note the difference between TTL and MOS

NOR: T_{1A}, T_{1B} in parallel

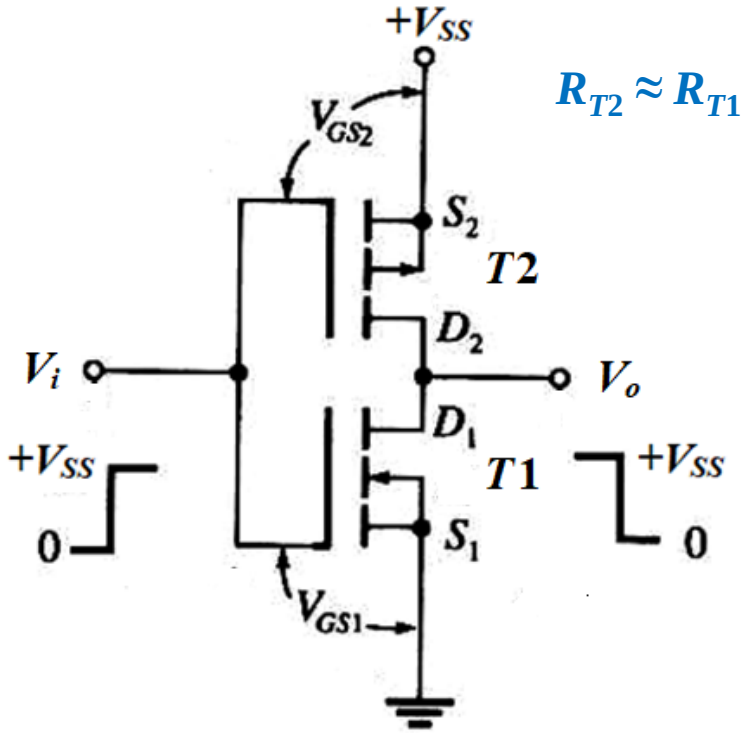
NAND: T_{1A}, T_{1B} in series

CMOS Inverter



$R_{T2} \approx 10\ R_{T1}$

NMOS: Charging / discharging of C_L



$R_{T2} \approx R_{T1}$

CMOS Inverter

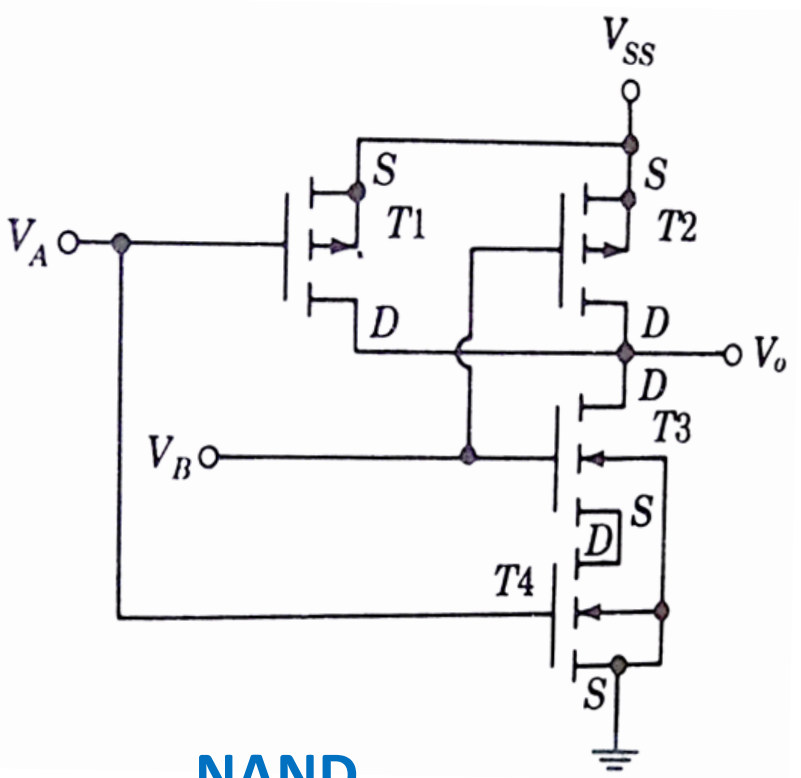
Output resistance = 1 KΩ
(for both H and L)

Input resistance = 10^{12} Ω

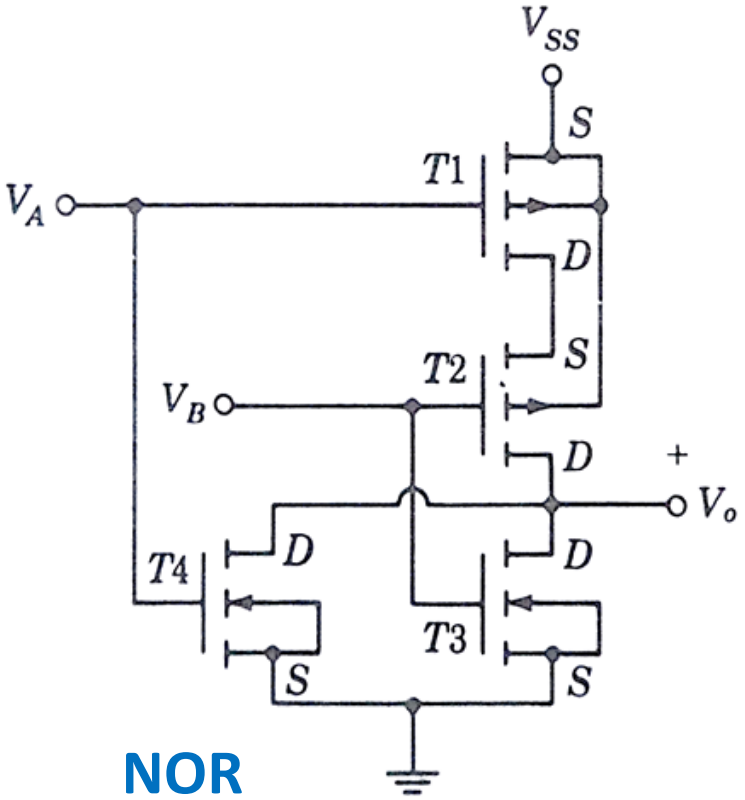
Input capacitance = 5 pF
(shunt)

CMOS NAND and NOR Gates

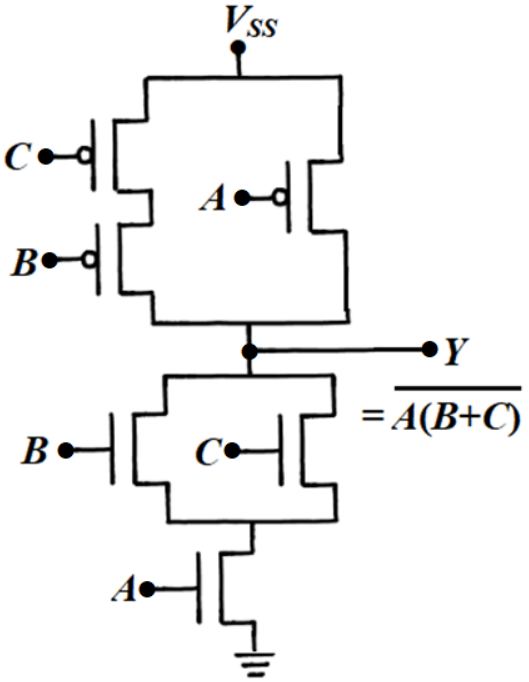
Combinatorial Logic



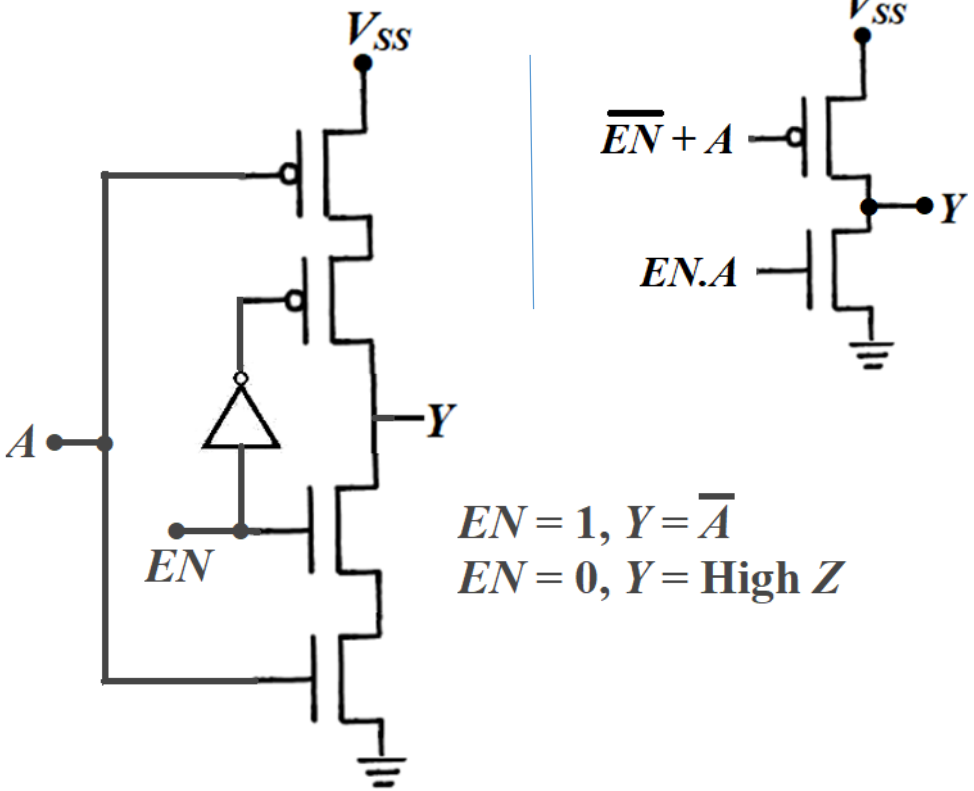
NAND



NOR

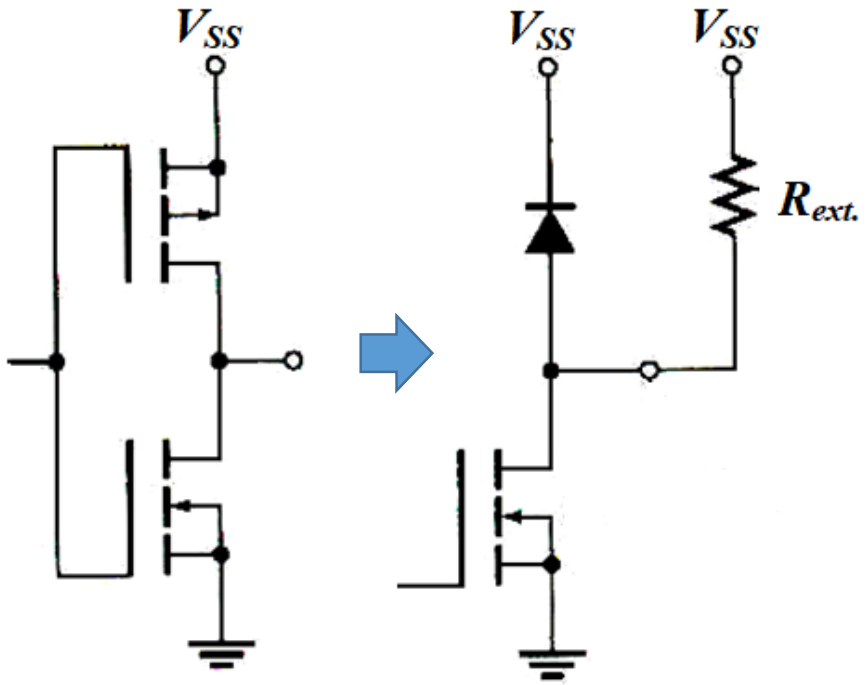


CMOS Tristate and Open-drain



$EN = 1, Y = \overline{A}$

$EN = 0, Y =$ High Z



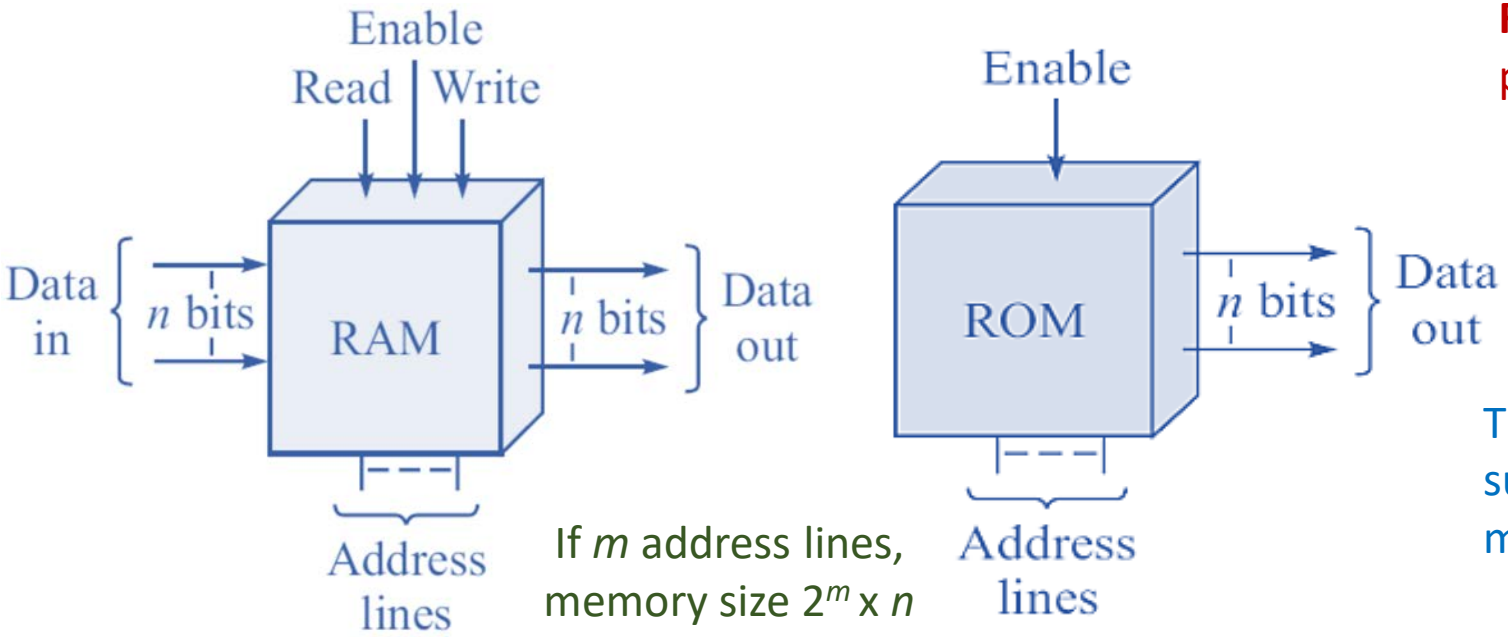
Open-drain with protective diode

Similar to open-collector: Provides wired-AND

Part II

Types of Memory

- Circuits and/or systems designed specifically for data storage are referred to as memory.
- Memory may be flip-flop, register, semiconductor memory chips (also magnetic, optical).
- RAM (Random Access Memory) is volatile, meant for multiple read and write (Read/Write Memory).
- ROM (Read Only Memory) is non-volatile, meant for multiple reading, also random access.



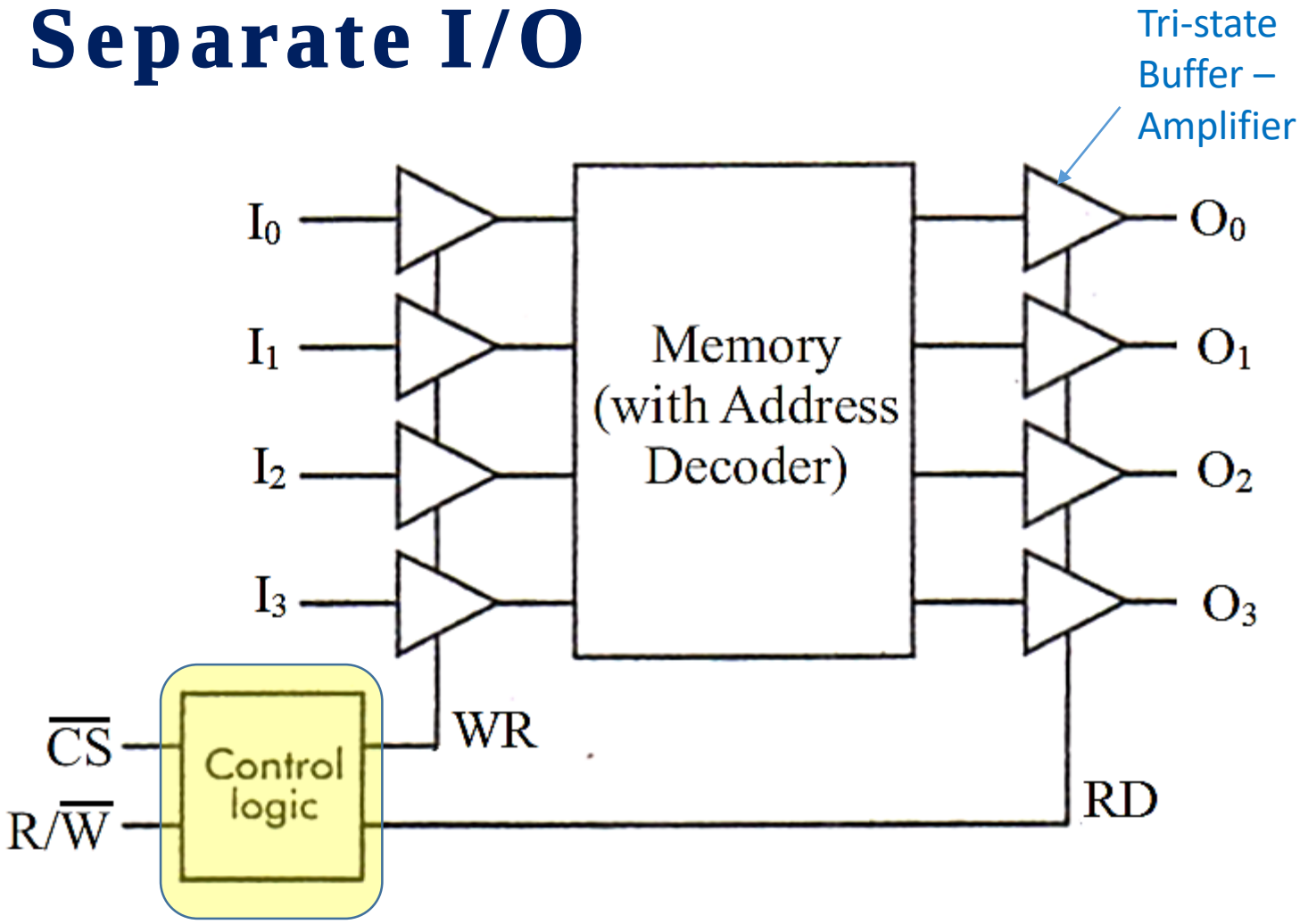
If *m* address lines, memory size 2^m x *n*

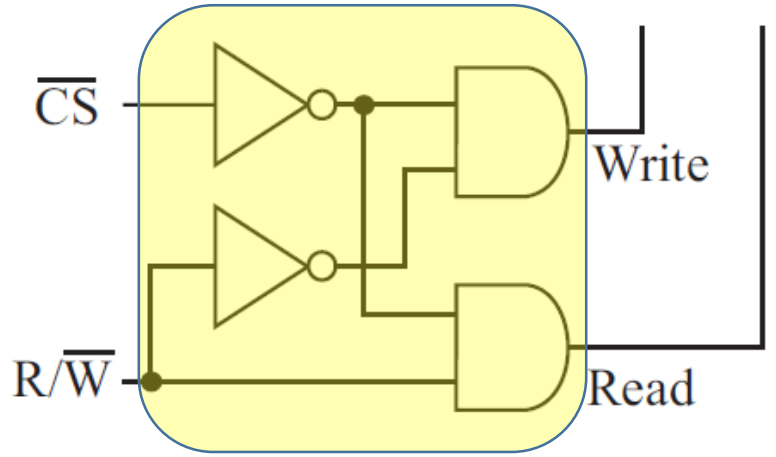
Random access: Independent of the physical position of the memory within memory block.

Bit organized: 1-bit stored in one address
Word organized: Group of bits stored in one address

There are further subdivisions of each memory type.

Separate I/O



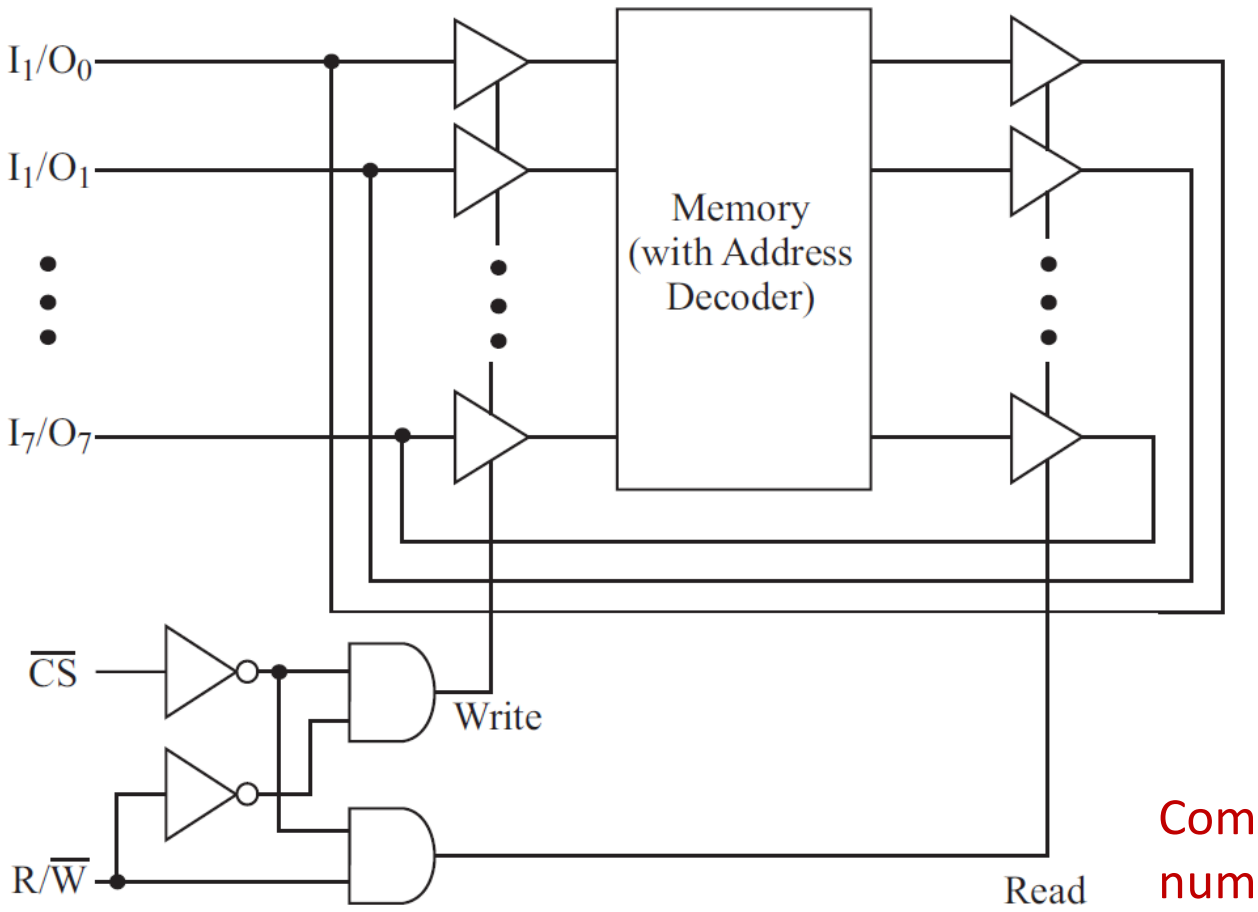


$$WR = CS'.W$$
$$= CS'.\bar{R}$$

$$RD = CS'.R$$
$$= CS'.\bar{W}$$

CS	R	WR	RD
0	0	1	0
0	1	0	1
1	0	0	0
1	1	0	0

Common I/O



Memory IC	Organization	No. of pins	Type
2114	1K x 4	18	Common
2115	1K x 1	16	Separate
2147	4K x 1	18	Separate
6168 (CMOS)	4K x 4	20	Common

All these Static RAM (doesn't require refresh) have $\overline{CS}$ and $R/\overline{W}$ as control logic i/p.

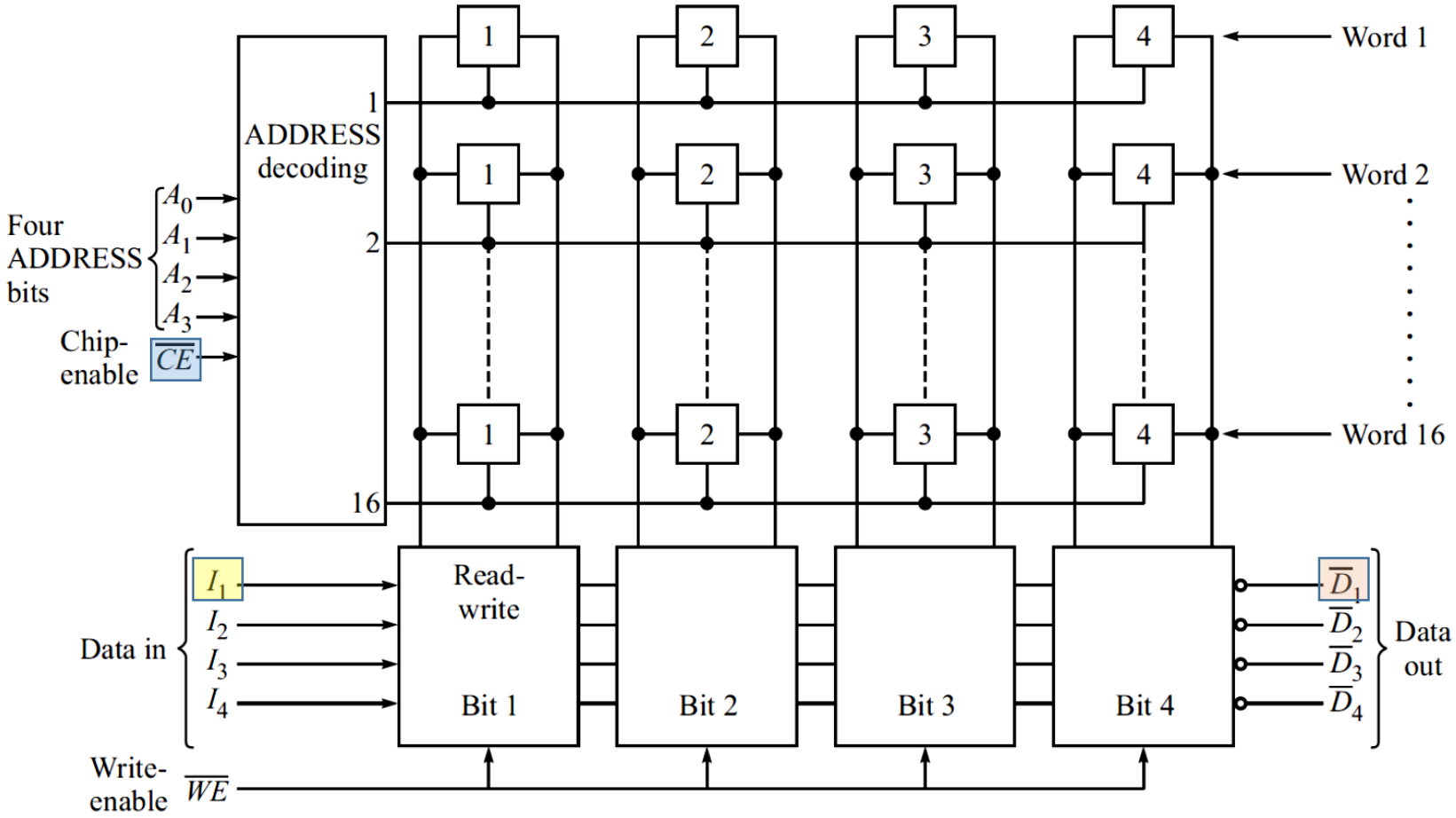
CMOS IC 6116 (2K x 8, 24 pins, Common) and 6264 (8K x 8, 28 pins, Common) have $\overline{CS}$, $\overline{WE}$, $\overline{OE}$ as control inputs where,

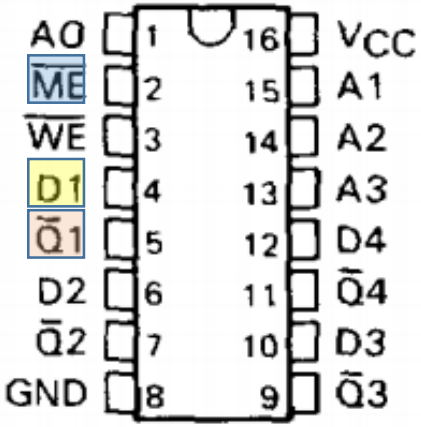
$$\boldsymbol{WR = CS'.WE'}$$

$$\boldsymbol{RD = CS'.OE'.WE}$$

Common I/O lines save number of external pins.

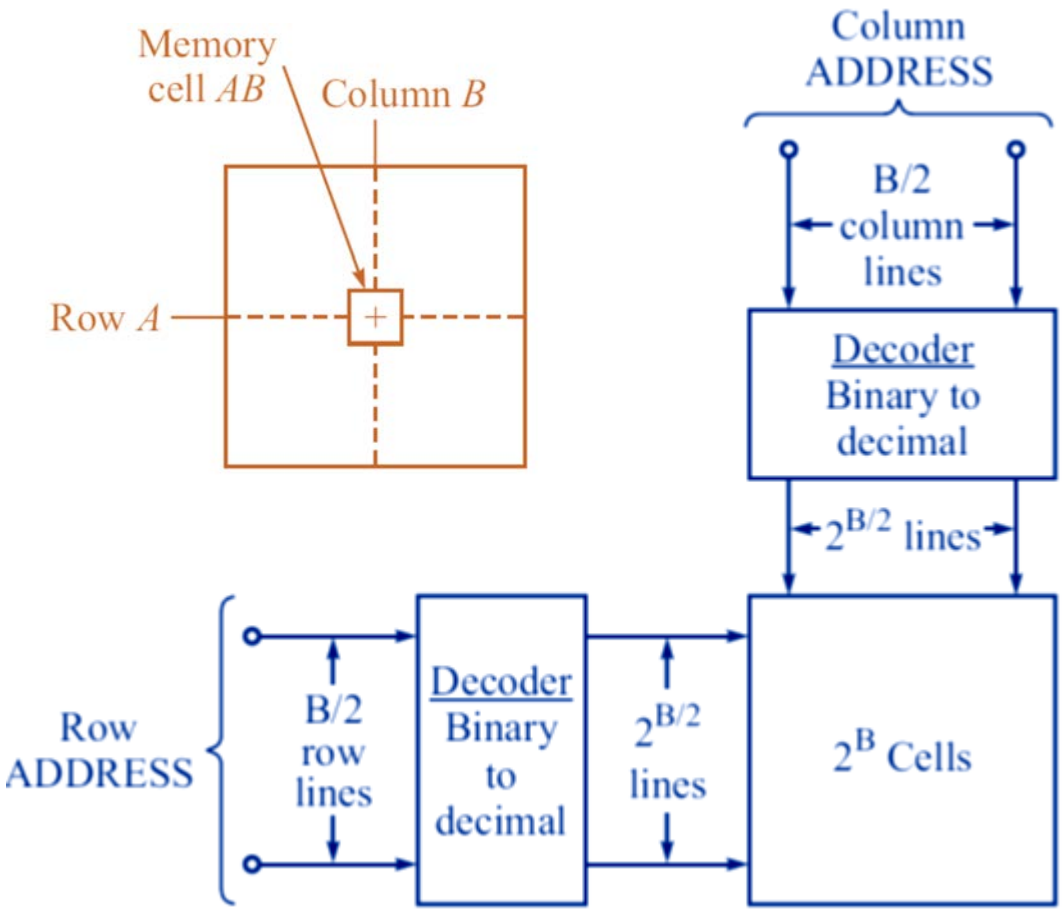
Linear Addressing

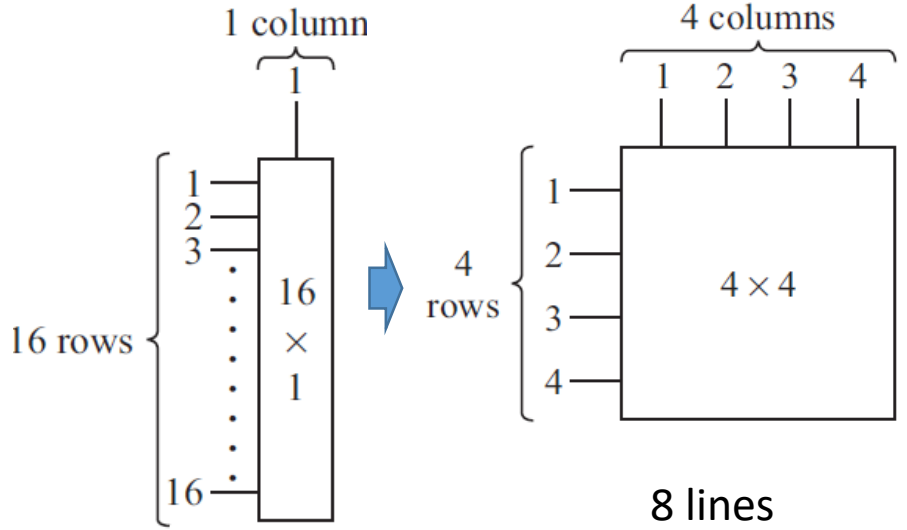




IC 7489, 16 x 4, 64 bit RAM follows this (word addressing)

Matrix Addressing





16 lines

8 lines (preferred)

- Square array requires fewest lines to address a cell / group of cells (word-organized) in particular location.
- Note that no. of address bits coming to address decoder(s) of memory IC remains same.
- Row address and col. address may be time-multiplexed (saves pins).

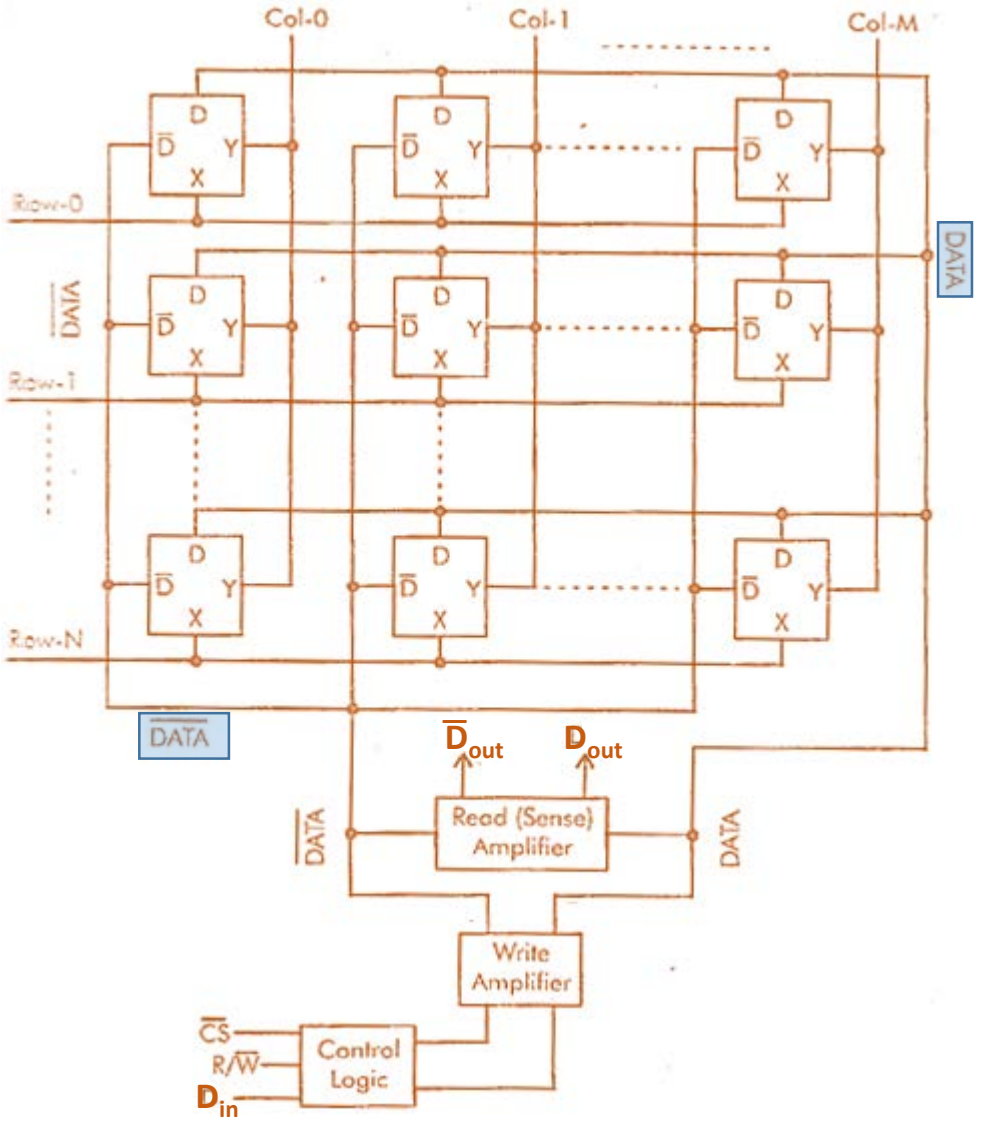
SRAM using BJT

SRAM (Static RAM: BJT, MOS) in contrast to DRAM (Dynamic RAM: MOS) does not require refreshing.

Control Logic: It decides when the chip is selected whether D_{in} is to be written in the cell or the cell is to be read out through D_{out}.

Write Amplifier: It contains circuitry to send current to memory cell as per D_{in} to effect switching when required.

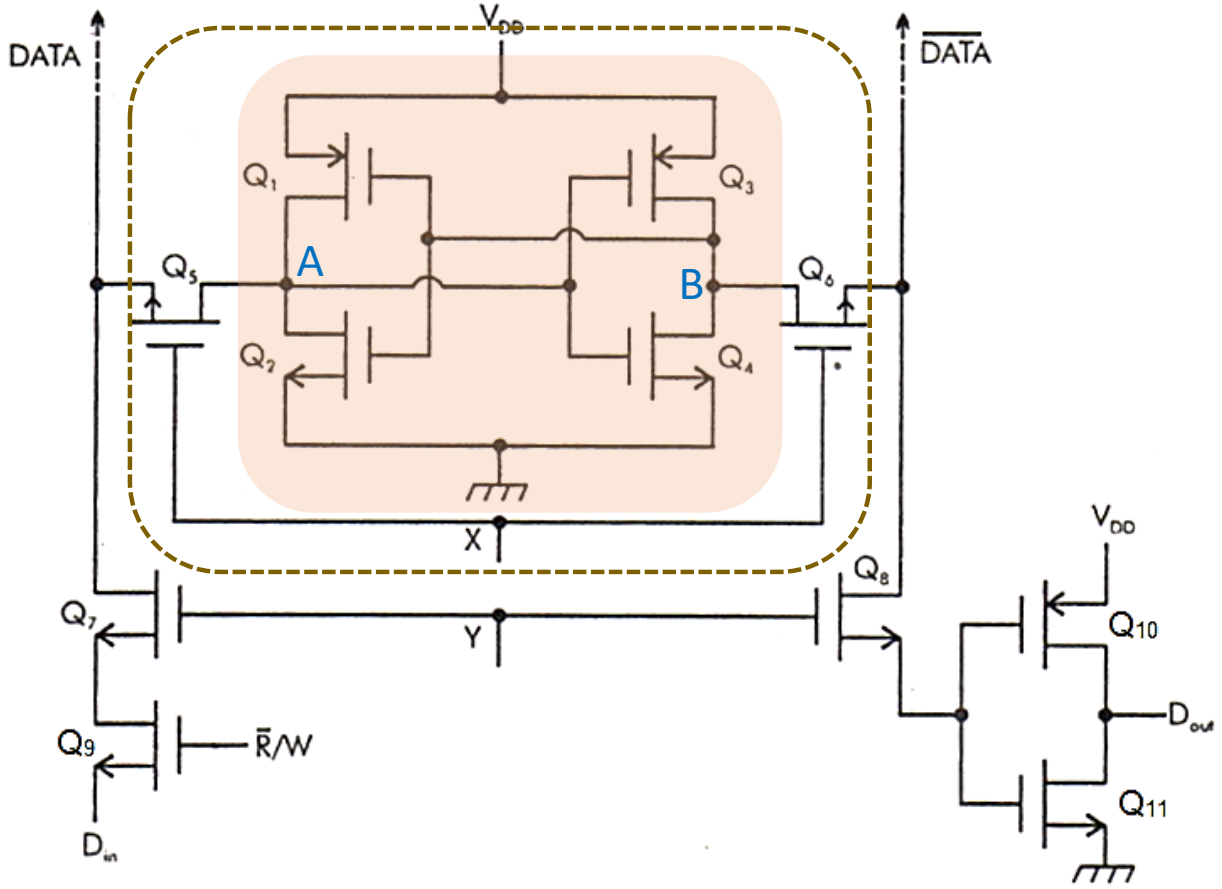
Read Amplifier: It contains circuitry to sense the current from a cell and delivers appropriate output D_{out}.



Memory Cell: A multi-emitter transistor pair operating in bistable mode.

Representation of a BJT based bit-organized SRAM with array of cells (M x N) cells using 2-dimensional matrix based addressing.

SRAM using CMOS



- Basic memory cell is cross-coupled CMOS inverters.
- If Q_2 is ON, V_A = L, Q_4 is OFF and V_B = H (vice versa)
- Q_1 to Q_6: Basic cell and access to bitlines: 6T configuration
- Q_5, Q_6, Q_7, Q_8, Q_9 are pass transistors.
- Q_{10}, Q_{11} form CMOS inverter: output buffer.
- X=L, Y=L: Q_5, Q_6, Q_7, Q_8 are OFF, cell not addressed. (Additional circuitry for *CS*)

Read:

X=H, Y=H, $\overline{R}/W$=L: Q_9 is OFF, Data = V_A = L, $\overline{Data}$ = H, D_{out} = L (Similarly for V_A = H)

There can be differential sensing of bitlines.

Write:

X=H, Y=H, $\overline{R}/W$=H: Q_9 is ON.

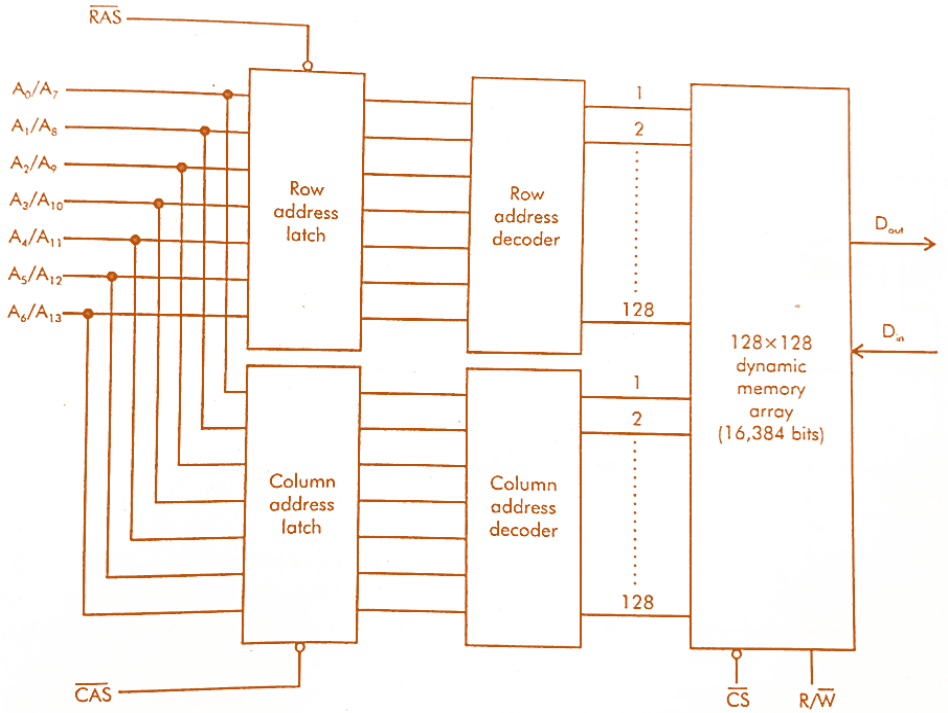
Consider, D_{in} = H.

Forced input makes V_A = H

which in turn makes V_B = L.

DRAM Basics and Multiplexed Addressing

- MOSFET has nearly infinite input impedance and very low leakage current from gate.
- Charge can be stored on the MOSFET gate capacitance for a short time.
- The capacitance can act as a memory cell providing a simple circuit that gives higher packing density at less cost.
- The cell needs to be charged periodically (ms order) even when no memory read or write. This is called *refreshing of cells*, characteristic of Dynamic Random Access Memory (DRAM).
- DRAM timing cycles are more complicated than SRAM timing cycles.



16 Kbit DRAM

For larger sized memory, more address lines required as input. Addressing can be multiplexed to save pins.

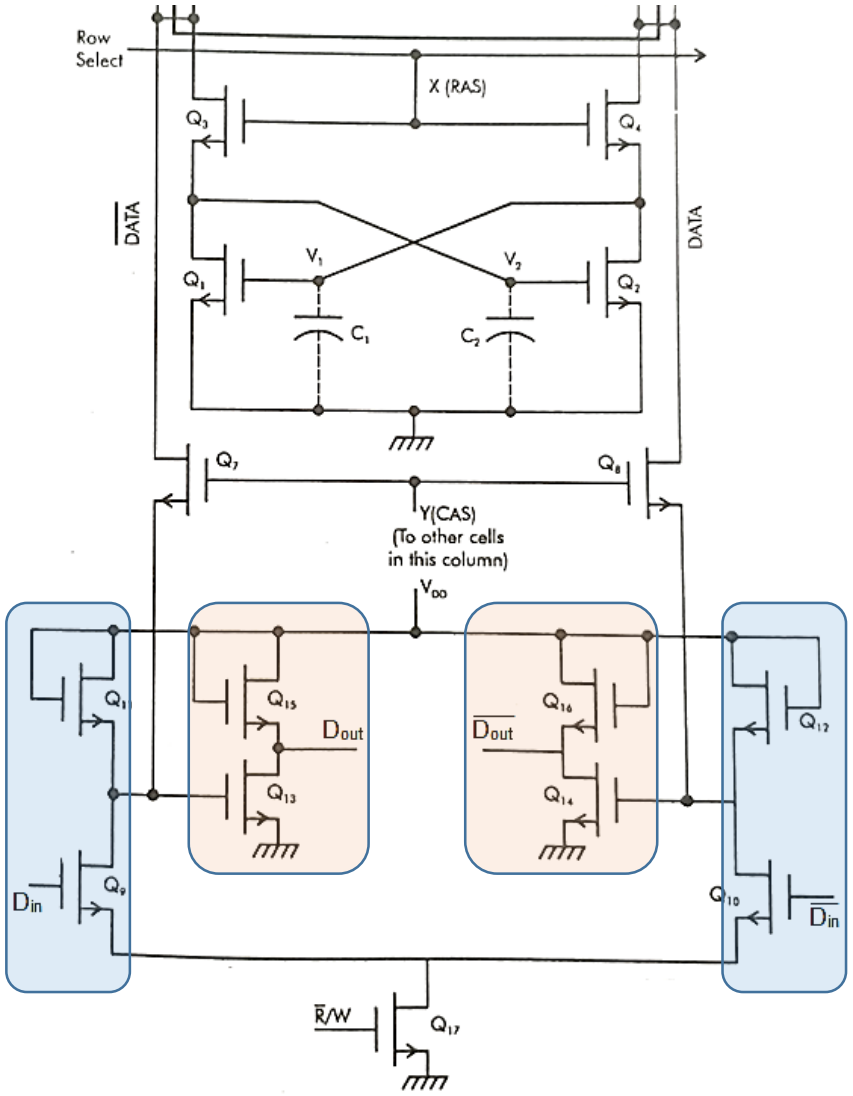
Row addr. and col. addr. use same pins but latched into respective registers through strobing.

Write and Read

X = H: Q_3, Q_4 ON
Y = H: Q_7, Q_8 ON
} Cell is addressed

Write:

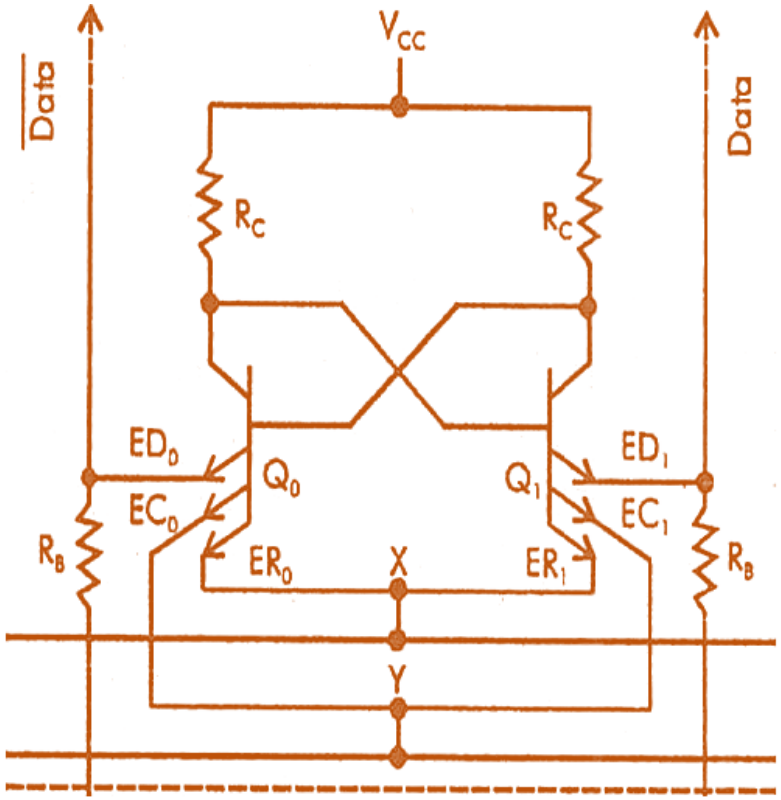
$\overline{R}/W$ = H: Q_{17} ON
D_{in} = L, $\overline{D}_{in}$ = H: Q_9 OFF, Q_{10} ON
V_{DQ9} = H (V_{DD} through load Q_{11})
V_{DQ10} = L
$\overline{Data}$ = H
Data = L
C_2 becomes H, Q_2 ON
C_1 goes L (previous charge if any, discharges through $Q_{2(ON)}$.)



Read:

$\overline{R}/W$ = L: Q_{17} OFF (no ground path through it or Q_9, Q_{10})
$V_{GQ13} = \overline{Data} = C_2$ = L (say, Q_1 ON)
$D_{out} = V_{GQ13}'$ = H (inverter, amplifier)
V_{GQ14} = Data = C_1 = H
$\overline{D_{out}} = V_{GQ14}'$ = L

BJT Memory Cell



Many such cells in parallel connect to Data lines with common Read / Write circuit. Individual cell is addressed by row select (X) and column select (Y) lines.

Logic LOW is ≤ 0.3V and logic HIGH is ≥ 3.0V.
A bias voltage of 0.5V is applied to emitters ED_0 and ED_1.

X = L and / or Y = L: if Q_0 is ON then Q_1 will be off (vice versa).

No current through ED_1 as Q_1 is OFF.
No current through ED_0 as EC_0 / ER_0 is at 0.5V – 0.3V = 0.2V lower potential.

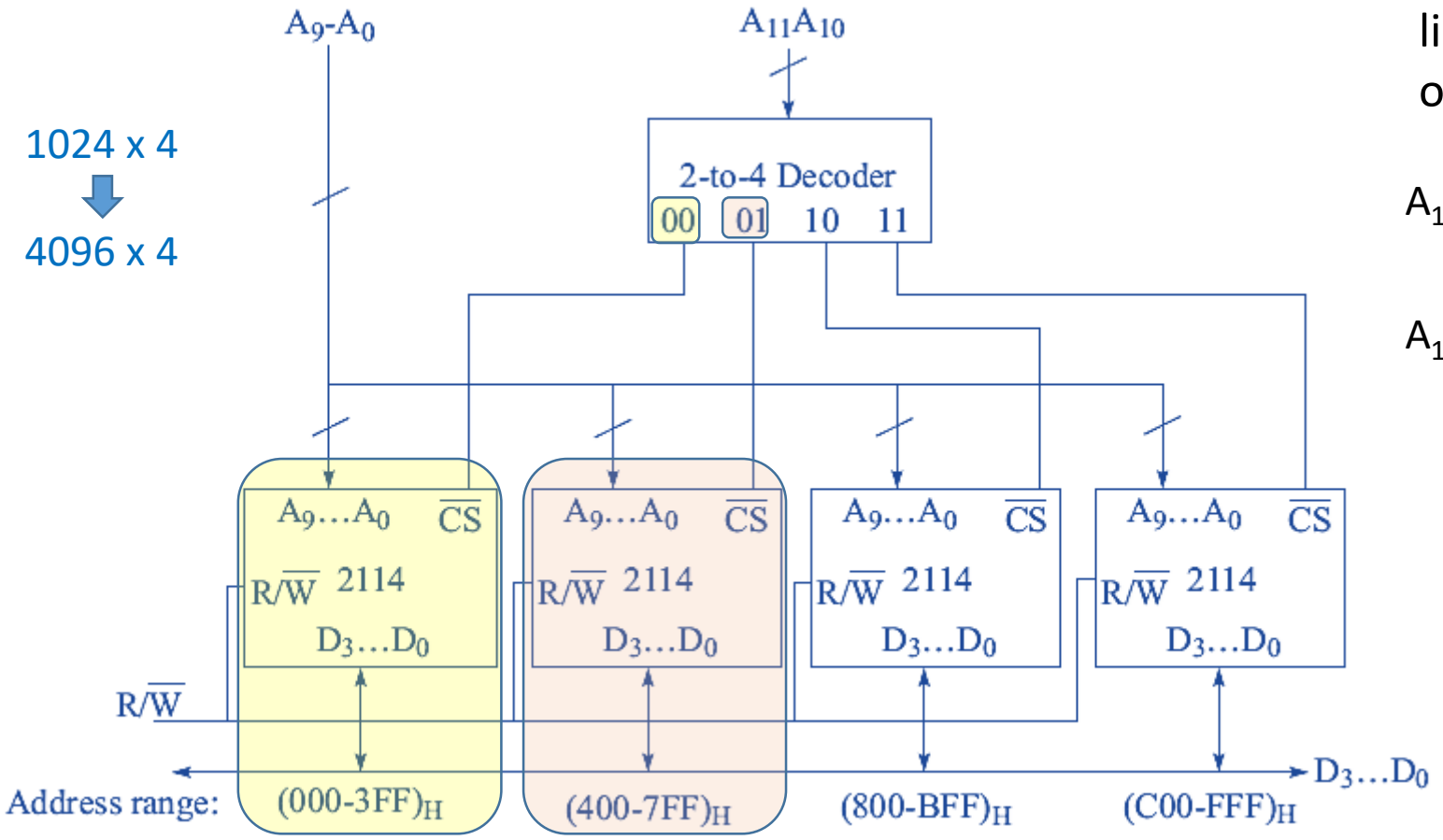
Both X and Y are H: ED_0 and ED_1 come into consideration (cell is read or written into) i.e. the cell gets addressed.

Address Range Expansion

1024 x 4

⇩

4096 x 4



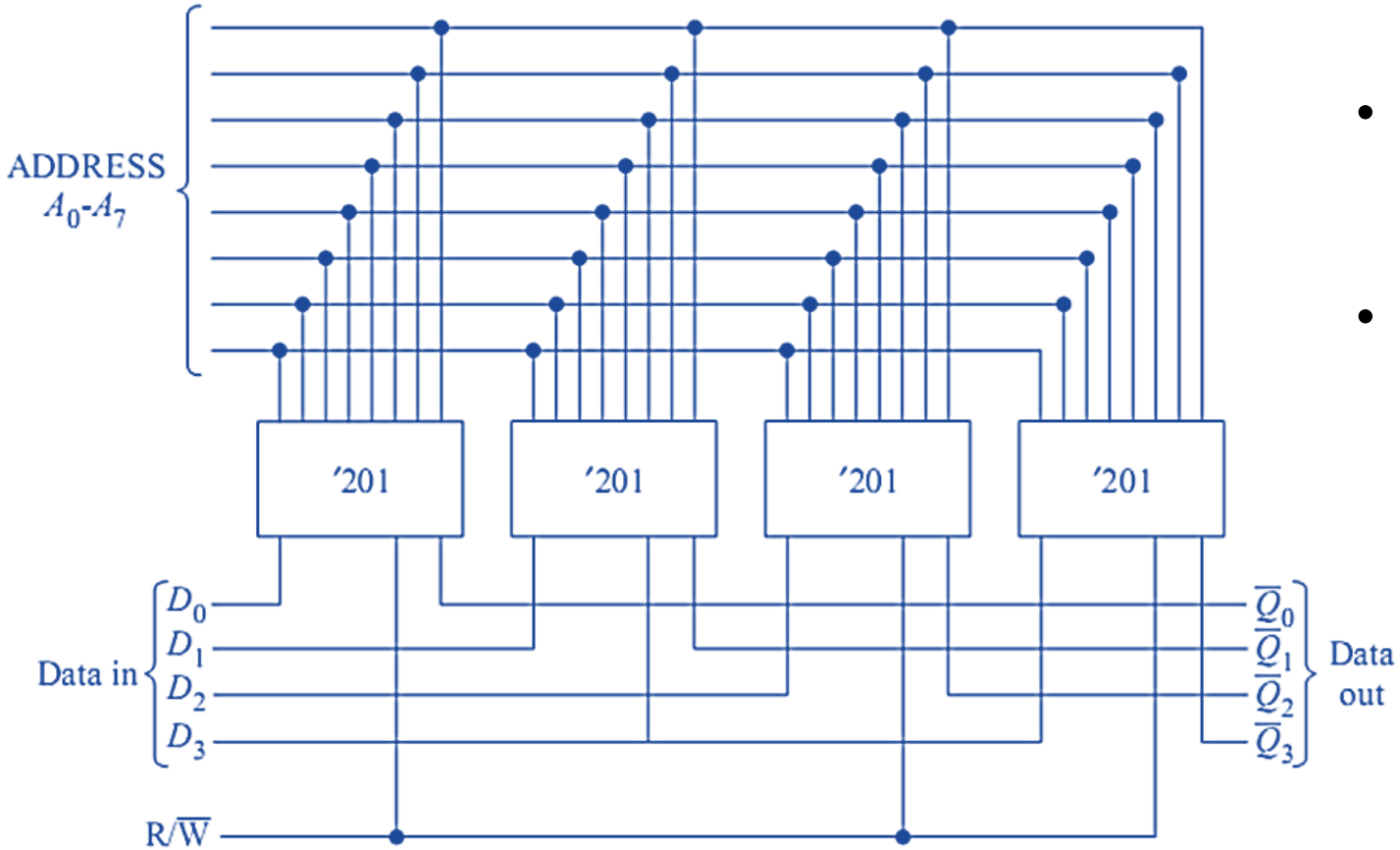
- IC 2114 is a 1024 x 4 bits Memory chip.
- In this arrangement, $A_{10}A_{11}$ address lines are decoded and the decoder output goes to chip select inputs.

$A_{11}A_{10}A_9 \ldots A_0$: 0000 0000 0000 ($000_H$)
0011 1111 1111 ($3FF_H$)

$A_{11}A_{10}A_9 \ldots A_0$: 0100 0000 0000 ($400_H$)
0111 1111 1111 ($7FF_H$)

.
.
.

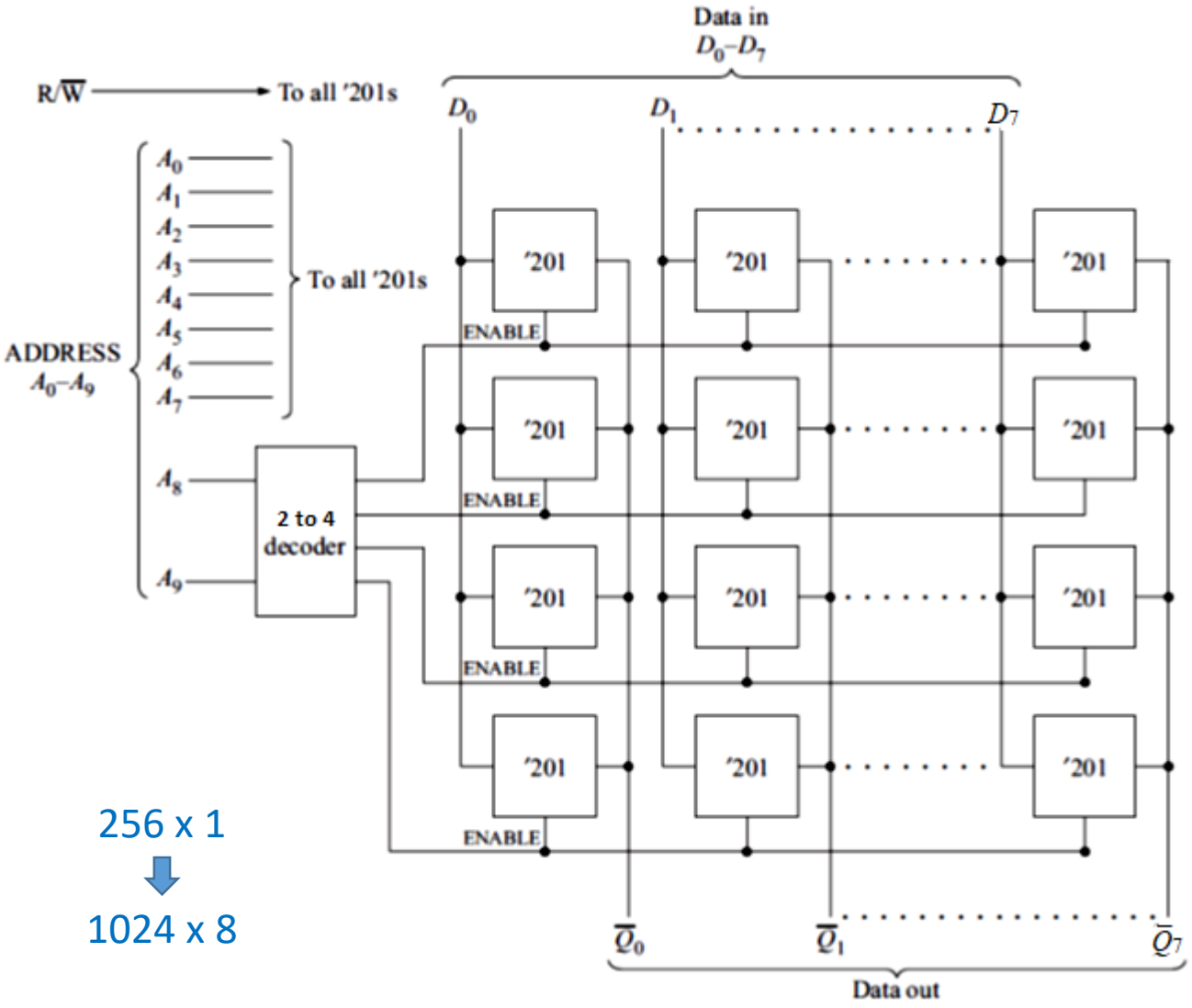
Data Range Expansion



- IC 74201 is a 256 x 1 bit Memory chip.
- 8 address inputs $A_0 - A_7$ are used to locate 256 memory cells.
- 4 such IC 74201 connected as shown (common address lines) expands the memory to 256 x 4.
- In this arrangement, in each location, 4 bit words can be written or read from.

256 x 1

256 x 4



256 x 1

⇩

1024 x 8

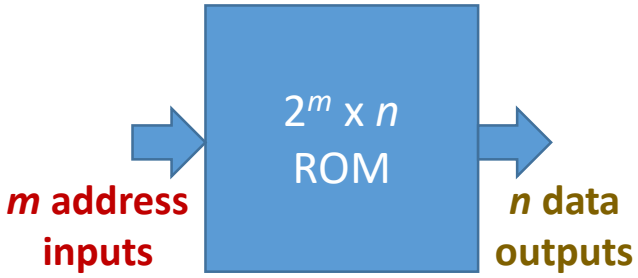
Both Address and Data Range Expansion

Thirty two IC 74201 Memory chip (each 256 x 1) is arranged in a matrix formation (4 x 8) by which the resulting memory bank has 10 bit address lines providing 1024 memory locations with 8 bit data storage in each location.

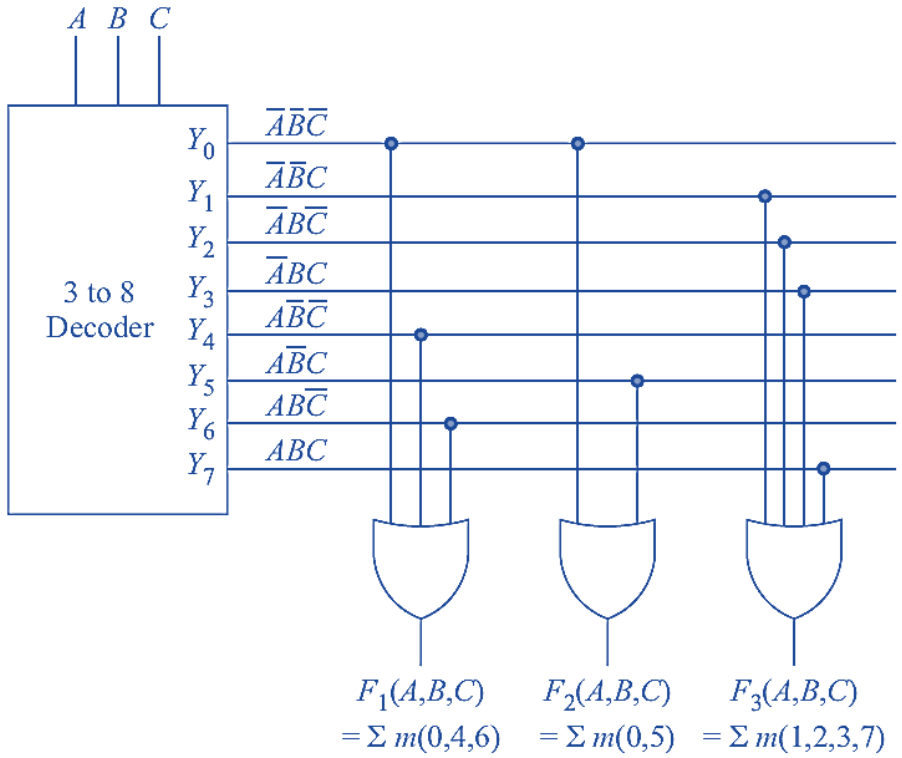
Part III

Decoder-OR Circuit and ROM

A Read Only Memory (ROM) is memory device where binary information is stored in certain interconnection pattern that is non-volatile.



A_{2-0}			D_{2-0}		
A	**B**	**C**	F_1	F_2	F_3
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	0	0	1

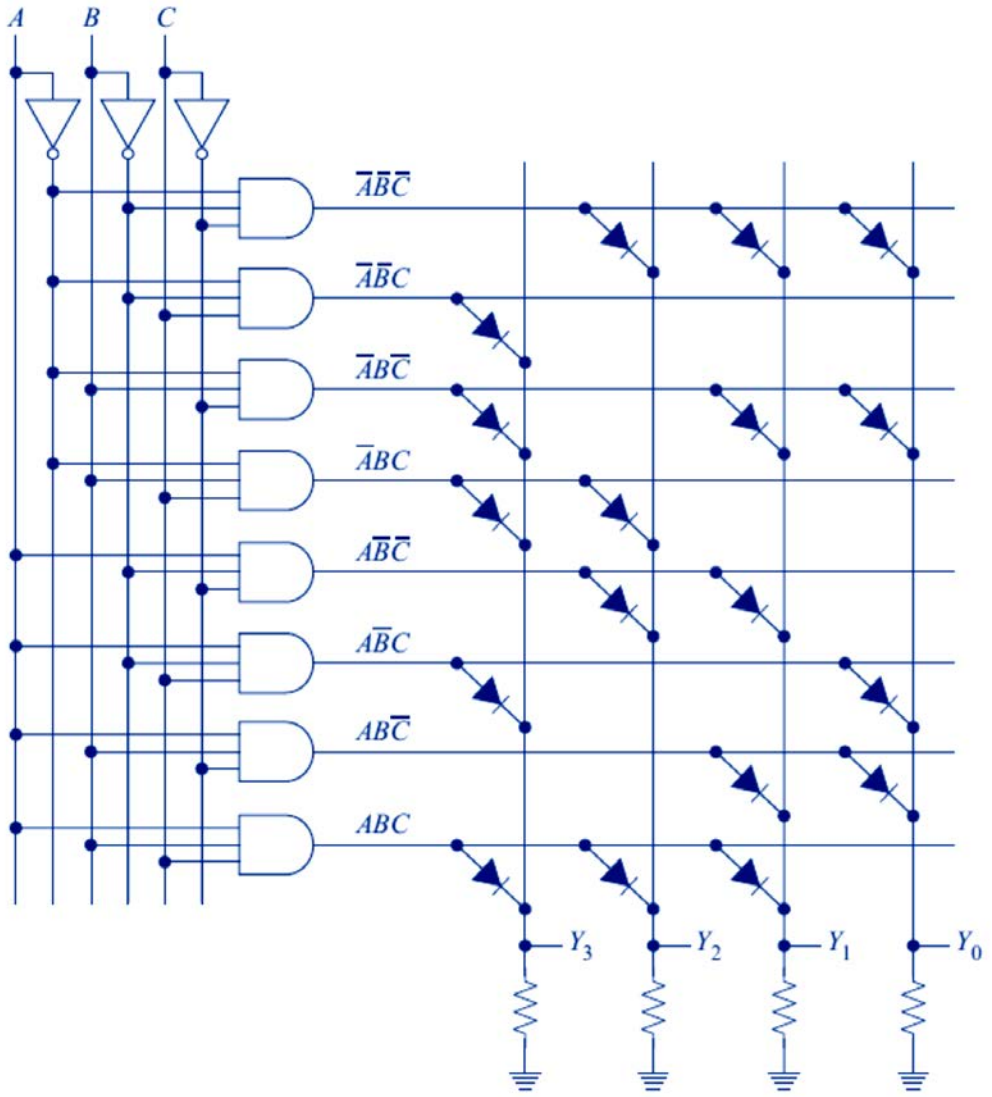


Decoder – OR circuit that is equivalent to 8 x 3 ROM

ROM is essentially a combinatorial circuit.

Diode Switch and ROM

$A_{2\text{-}0}$			$D_{3\text{-}0}$			
A	**B**	**C**	Y_3	Y_2	Y_1	Y_0
0	0	0	0	1	1	1
0	0	1	1	0	0	0
0	1	0	1	0	1	1
0	1	1	1	1	0	0
1	0	0	0	1	1	0
1	0	1	1	0	0	1
1	1	0	0	0	1	1
1	1	1	1	1	1	0



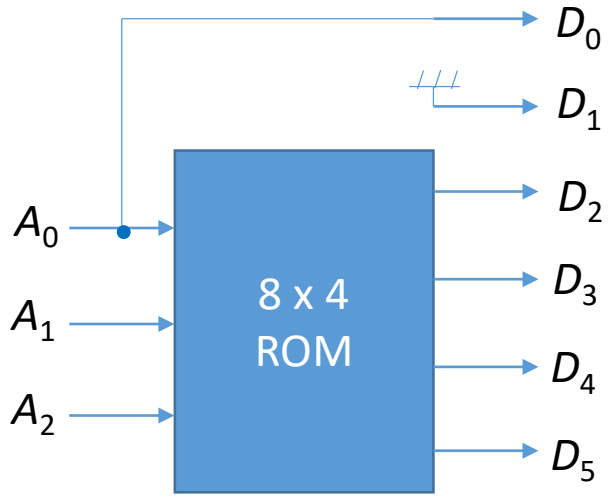
From the list of data to be stored, IC manufacturer produces a *mask* (photographic template) of the circuit which is used in the production of ROM.

$$Y_3 = \sum m(1,2,3,5,7)$$
$$Y_2 = \sum m(0,3,4,7)$$
$$Y_1 = \sum m(0,2,4,6,7)$$
$$Y_0 = \sum m(0,2,5,6)$$

A Squarer Circuit using ROM

Consider a squarer circuit with 3-bit input in this example.

Input				Output						
A_2	A_1	A_0	**Dec.**	D_5	D_4	D_3	D_2	D_1	D_0	**Dec.**
0	0	0	**0**	0	0	0	0	0	0	**0**
0	0	1	**1**	0	0	0	0	0	1	**1**
0	1	0	**2**	0	0	0	1	0	0	**4**
0	1	1	**3**	0	0	1	0	0	1	**9**
1	0	0	**4**	0	1	0	0	0	0	**16**
1	0	1	**5**	0	1	1	0	0	1	**25**
1	1	0	**6**	1	0	0	1	0	0	**36**
1	1	1	**7**	1	1	0	0	0	1	**49**



$D_0 = A_0$

$D_1 = 0$

$D_2 = \sum m(2,6)$

$D_3 = \sum m(3,5)$

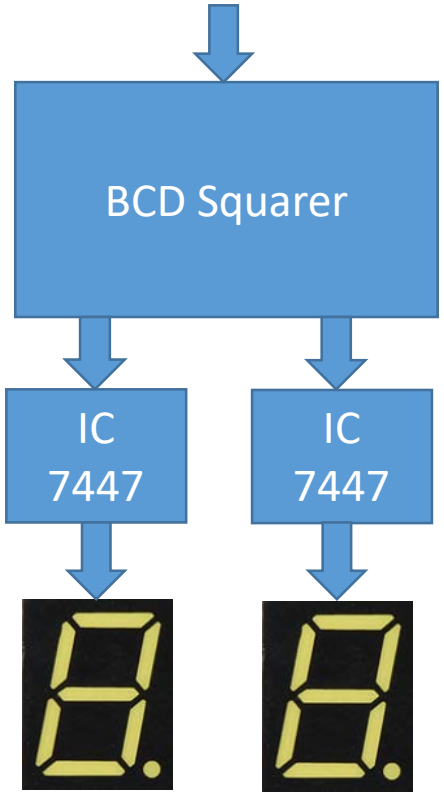
$D_4 = \sum m(4,5,7)$

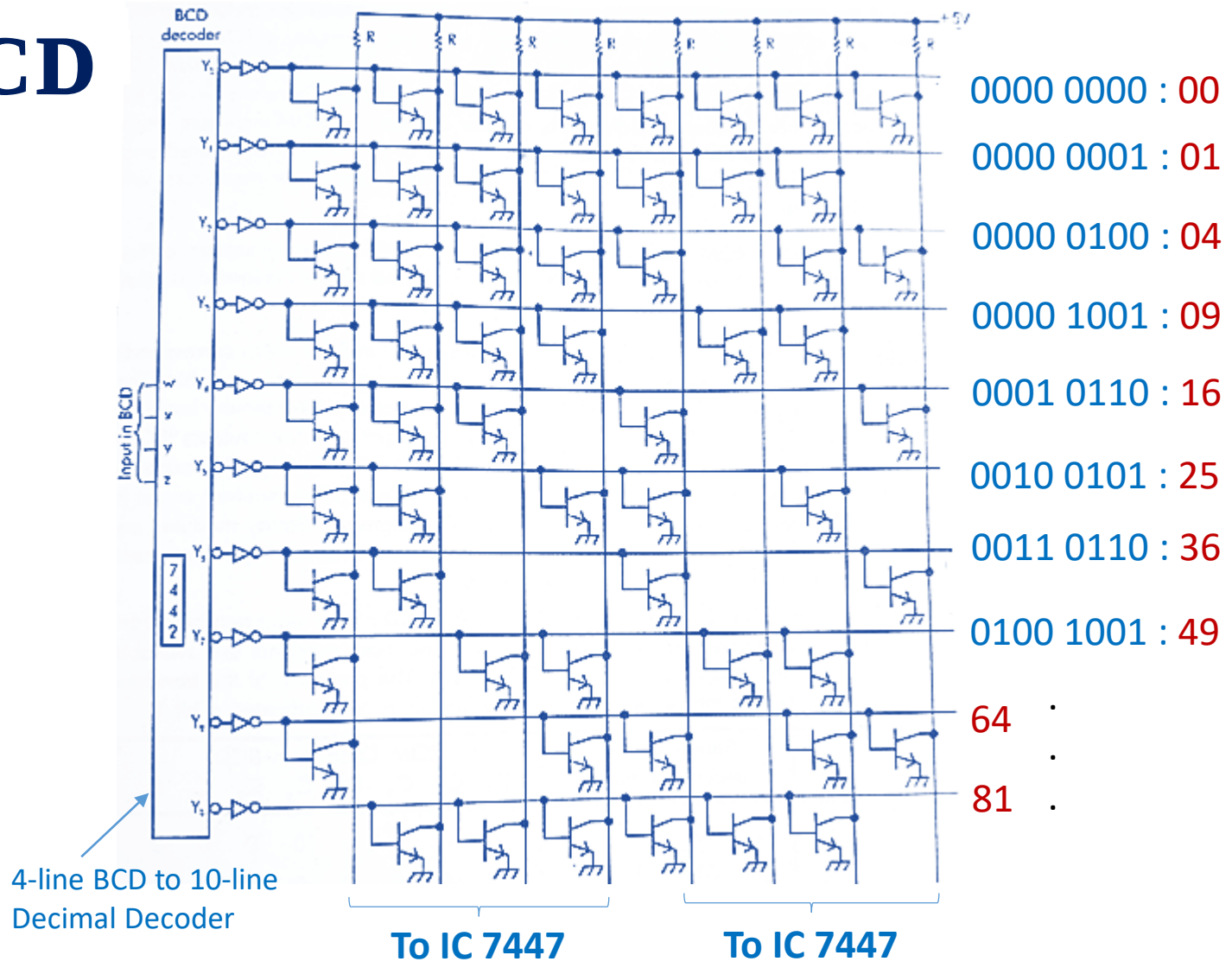
$D_5 = \sum m(6,7)$

Less than 8 x 6 ROM does.

Squaring BCD

BCD Input (0 – 9)





0000 0000 : 00

0000 0001 : 01

0000 0100 : 04

0000 1001 : 09

0001 0110 : 16

0010 0101 : 25

0011 0110 : 36

0100 1001 : 49

64 .

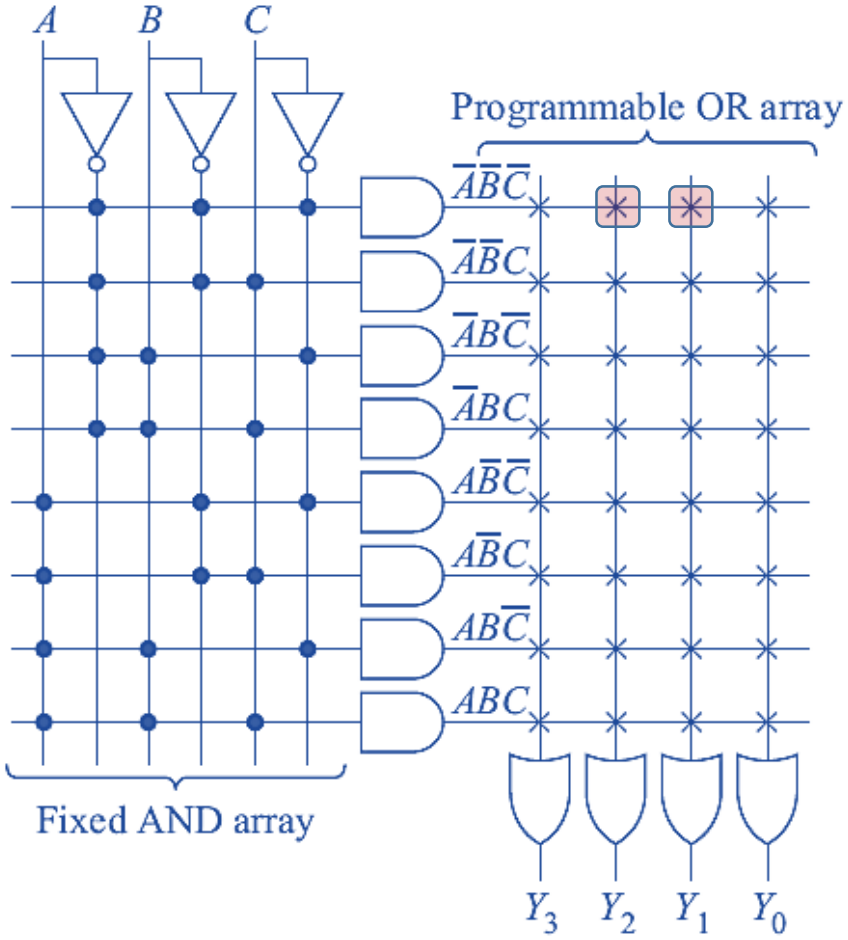
. .

81 .

Other than Diode, BJT and MOSFET can also be used as switch.

Programmable ROM (PROM)

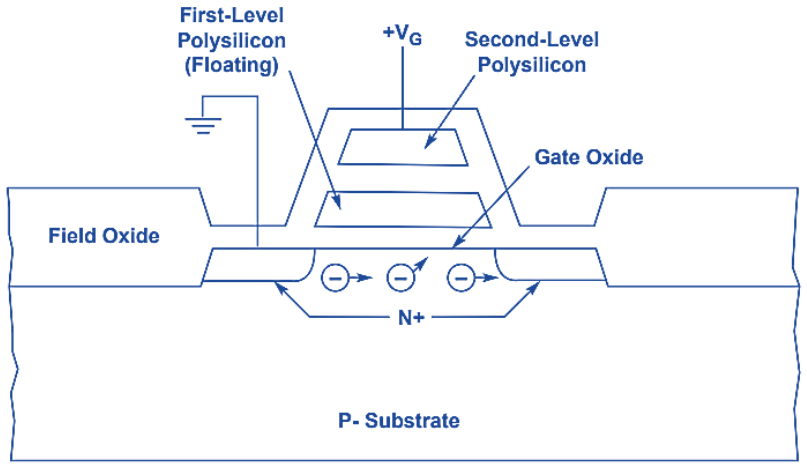
- PROM allows the user, instead of the manufacturer, to store the data.
- An instrument called a *PROM programmer* stores the words by "burning in."
- Originally, all diodes with a *fusible link* remain connected at the cross points.
- The PROM programmer sends destructively high currents through diodes that are to be removed.



To store 1001 ($Y_{3\text{-}0}$) in the address location ABC = 000, fuses at the cross points of Y_2 and Y_1 in the $\bar{A}\bar{B}\bar{C}$ row need to be burnt. Similarly for other cross points according to what is stored in each address.

EPROM, EEPROM

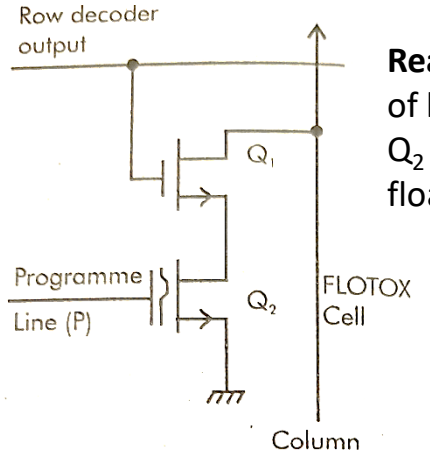
- The *erasable PROM* (*EPROM*) uses MOSFETs.
- Data is stored with an EPROM programmer.
- All stored data can be erased by shining ultraviolet light through a quartz window that releases all stored charges.
- There is one time programmable EPROM without window.



Electrical charge is forced on floating gate. When electron is present, threshold voltage is higher than normal which is usually considered as logic '0'; else, logic '1'.

Electrically Erasable PROM (*EEPROM*) is similar to EPROM where data is erased from target cells by removing the charge for which a pulse of opposite polarity is sent. EEPROM is very slow.

Flash Memory is further advancement of EEPROM. It is much faster as data writing is in block (say, 512 bytes) instead of 1 byte at a time.

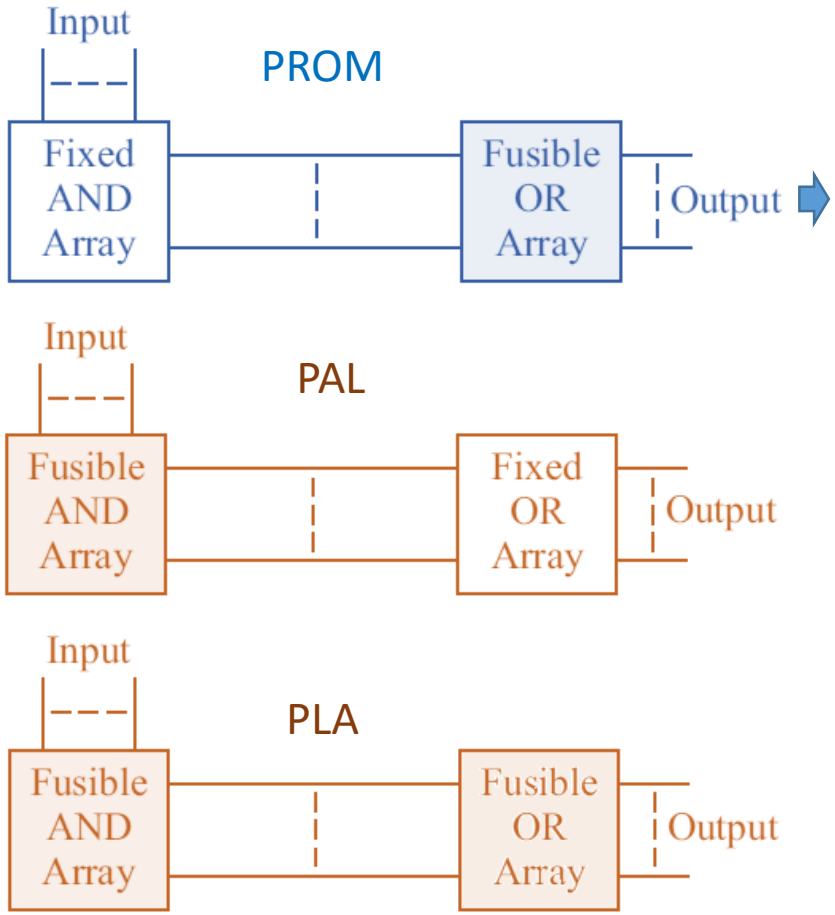


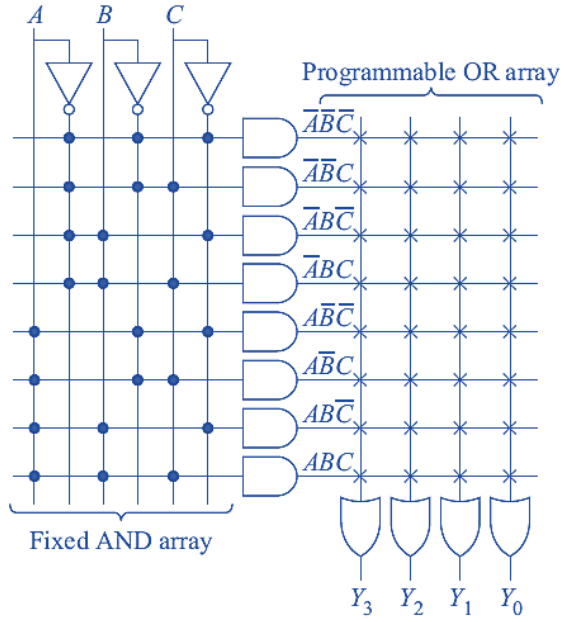
Reading: 5V to gates of both Q_1 and Q_2. Q_2 OFF if charge in floating gate.

Not included in Class Test 3

PROM to PAL, PLA

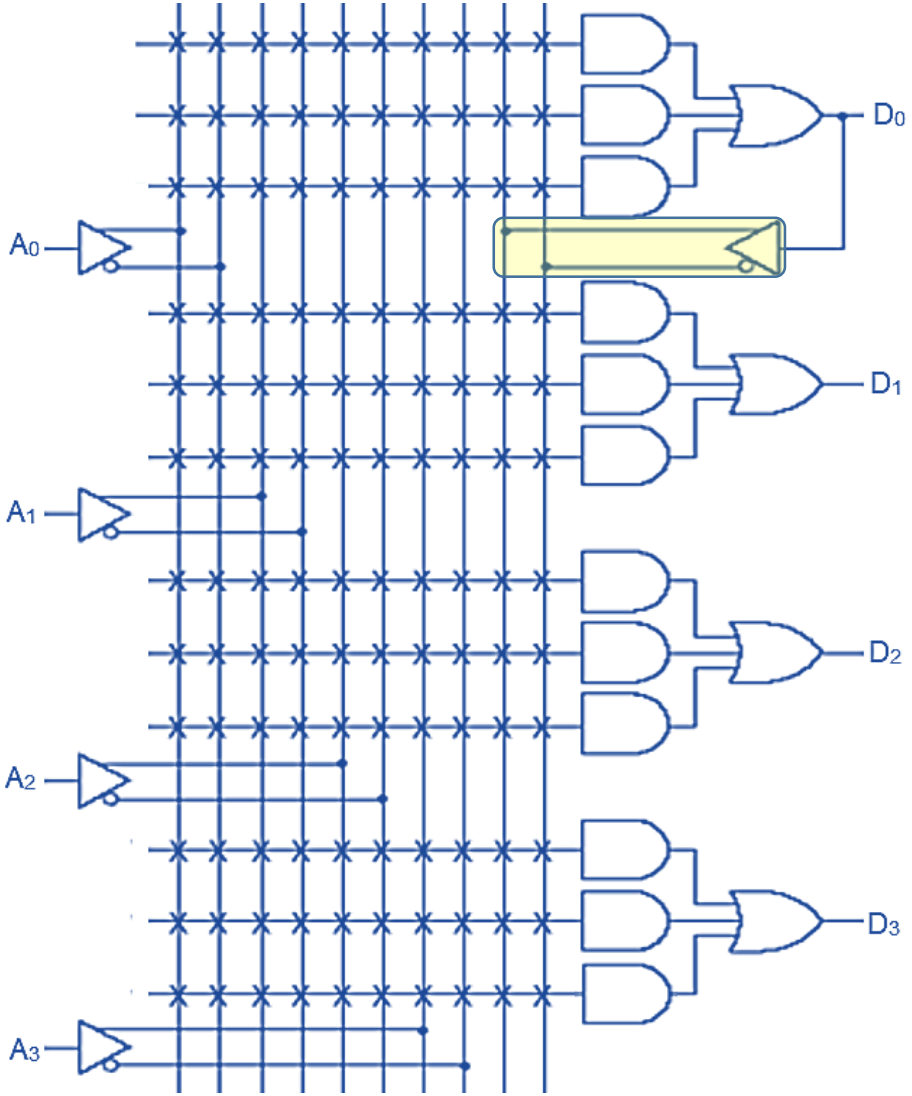
- In PROM (Programmable Read Only Memory), AND array is fixed and OR array is programmable.
- In PAL (Programmable Array Logic), OR array is fixed, AND array is programmable.
- In PLA (Programmable Logic Array), both AND and OR array are programmable.



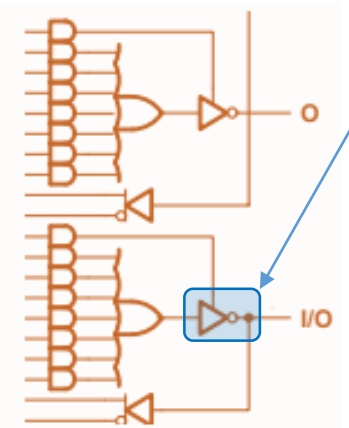


PAL

- A representative Programmable Array Logic (PAL) circuit is shown.
- Each input is complemented as well as uncomplemented.
- Output comes from *three wide* AND-OR array sections.
- One of the output is fed back and is available to AND gate as input (complemented and uncomplemented).
- Each AND gate along the horizontal line has 10 programmable input connections that connect to vertical lines.



PAL IC 16L8 has 10 dedicated inputs; 8 tristated outputs out of which 6 can be fed back (I/O).



Part of layout

Not included in Class Test 3

PAL : Example

$W = \sum m(2,12,13)$

$X = \sum m(7,8,9,10,11,12,13,14,15)$

$Y = \sum m(0,2,3,4,5,6,7,8,10,11,15)$

$Z = \sum m(1,2,8,12,13)$

Individually, minimizing

$W = AB\bar{C} + \bar{A}\bar{B}C\bar{D}$

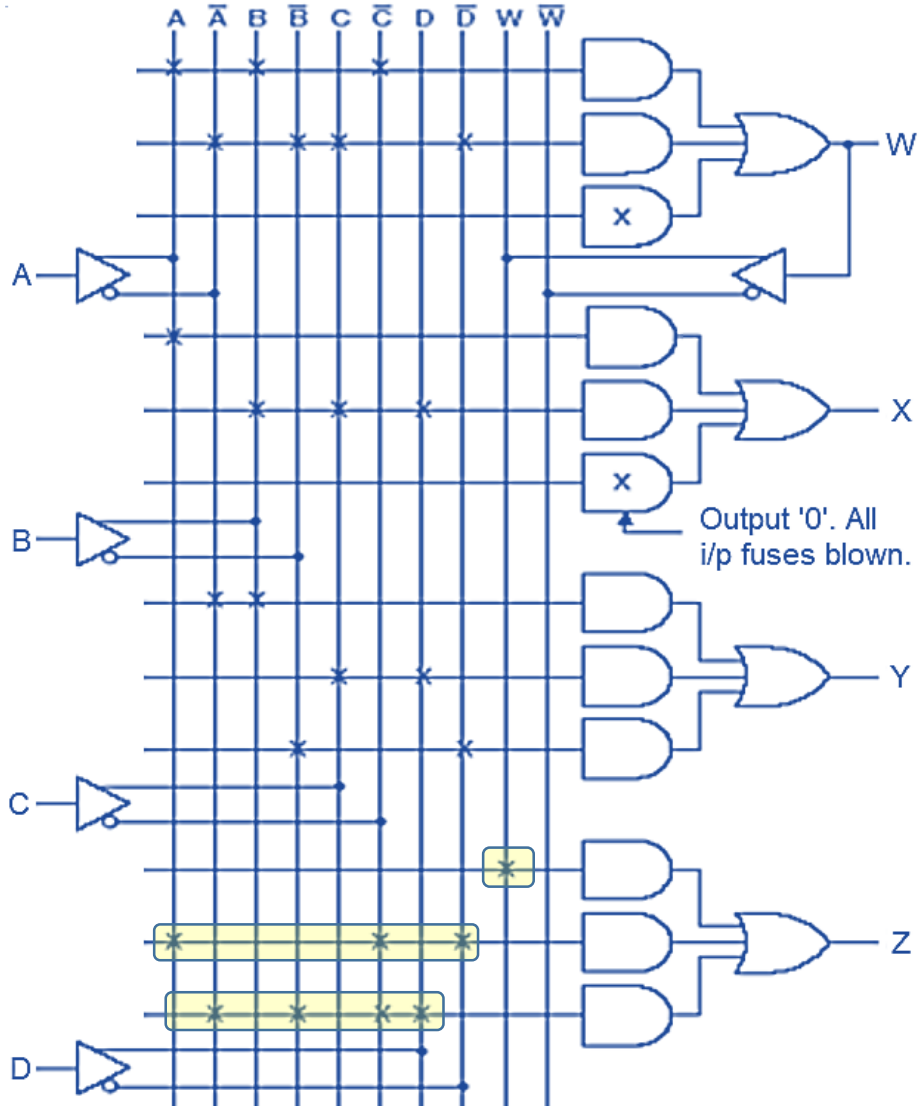
$X = A + BCD$

$Y = \bar{A}B + CD + \bar{B}\bar{D}$

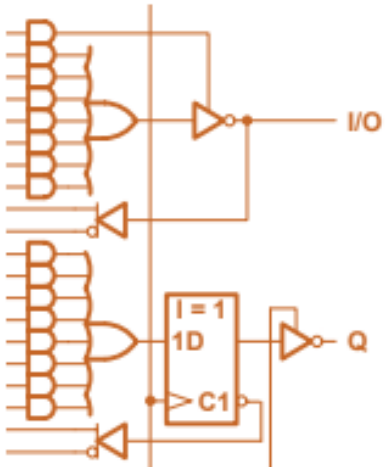
$Z = AB\bar{C} + \bar{A}\bar{B}C\bar{D} + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$

4 inputs

$Z = W + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$



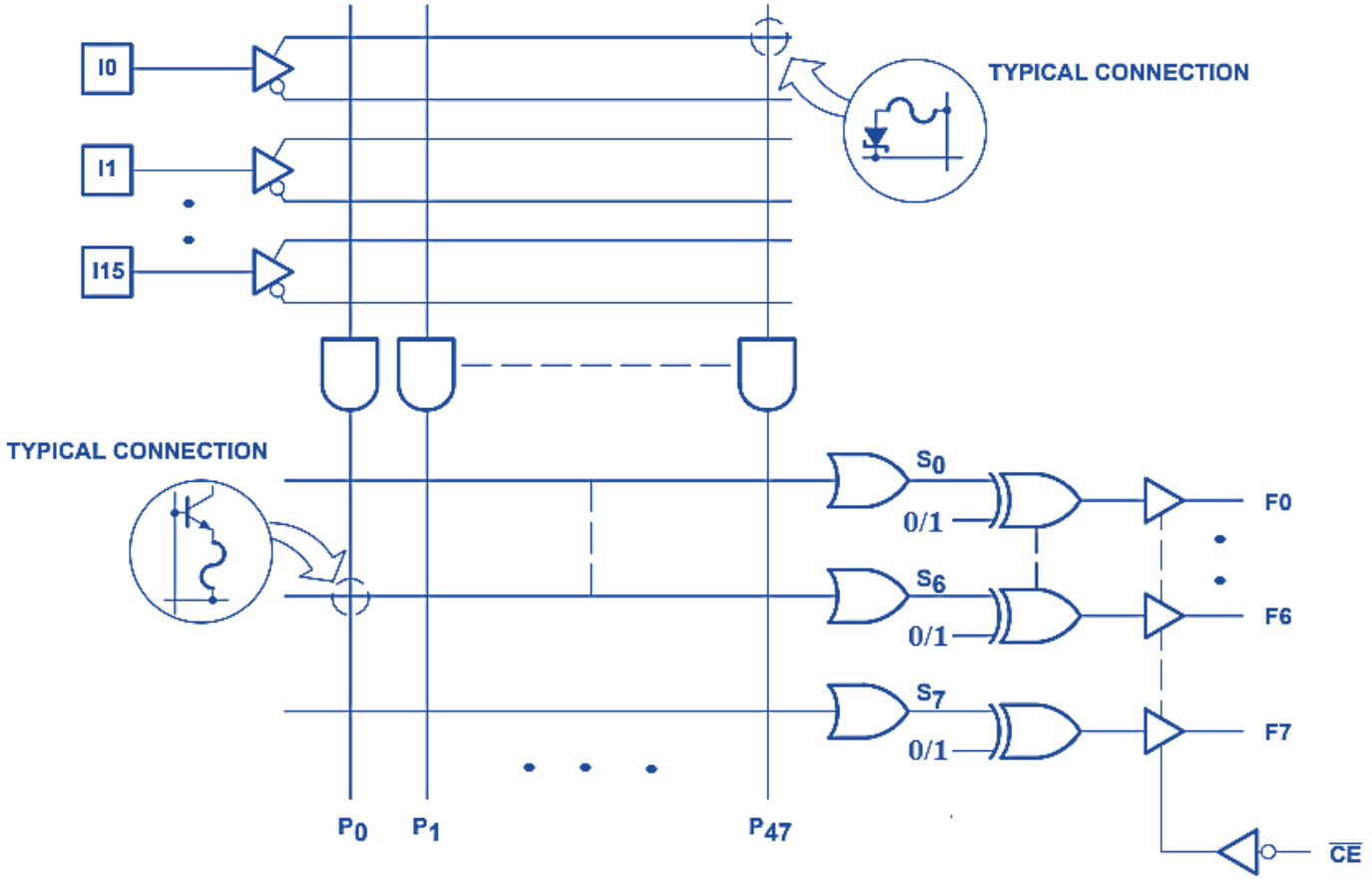
PAL IC 16R6 has 8 dedicated inputs; 2 tristated combinatorial I/O and 6 tristated registered outputs.



Part of layout

Not included in Class Test 3

PLA : Functional Diagram



Programmable Logic Array
PLS100 has

- 16 inputs,
- 48 AND gates,
- 8 OR gates,
- 8 Ex-OR gates (complements OR output if 1 is at the other input)
- Final output is tristated by chip enable.
- Also referred as 16 x 48 x 8 PLA

Not included in Class Test 3

PLA : Example

$F_1 = \sum m(2,4,5,7)$

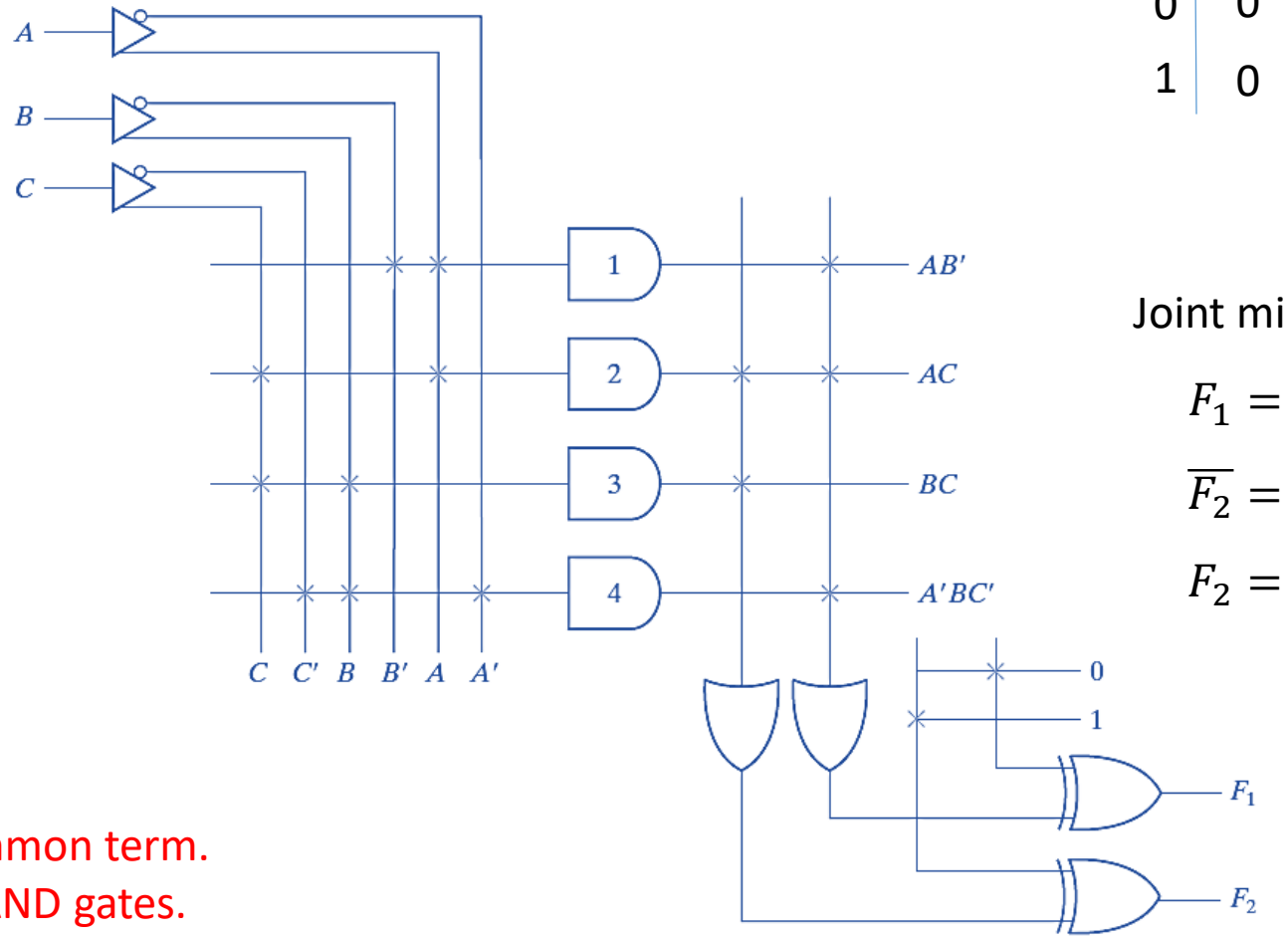
$F_2 = \sum m(0,1,2,4,6)$

A \ BC	00	01	11	10
0	0	0	0	1
1	1	1	1	0

F_1

A \ BC	00	01	11	10
0	1	1	0	1
1	1	0	0	1

F_2



A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	0

$\bar{F}_2$

AC : Common product

Joint minimization:

$$F_1 = A\bar{B} + AC + \bar{A}B\bar{C}$$

$$\overline{F_2} = AC + BC$$

$$F_2 = \overline{AC + BC}$$

Six product terms. No common term.
Problem if there are less AND gates.

Not included in Class Test 3

References:

- Herbert Taub, and Donald Schilling, Digital Integrated Electronics, McGraw Hill
- Technical documents from http://www.ti.com accessed on Oct. 08, 2018