Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 23

Register

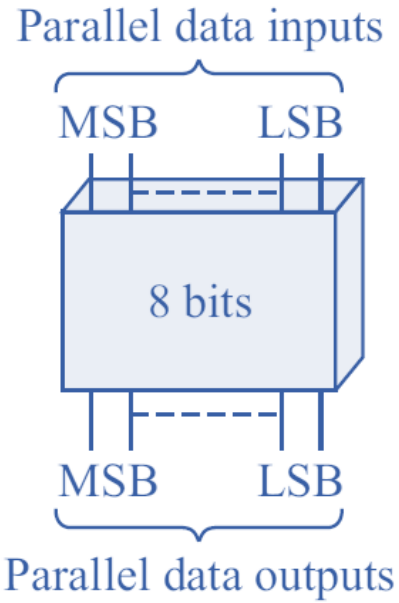
- A register is a group of flip-flops that can be used to store a binary number.
- There must be one flip-flop for each bit in the binary number. (To store an 8-bit binary number there must be 8 flip-flops.)

Key Operations

- Storing data (writing) in the register
- Retrieving data (reading) from the register.

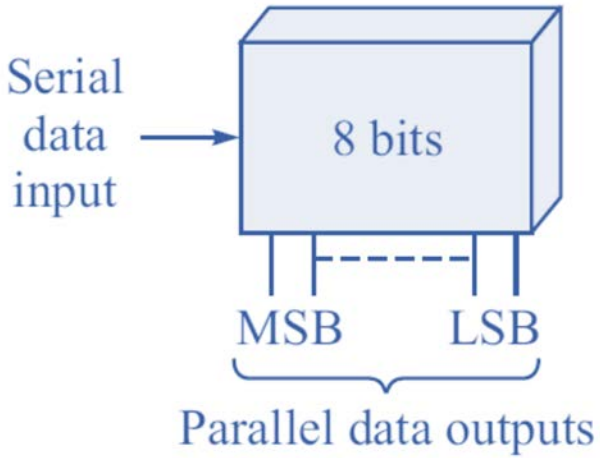
Considerations

- Availability of input – output pins
- Time to write / read data
- Non-destructive / Destructive reading

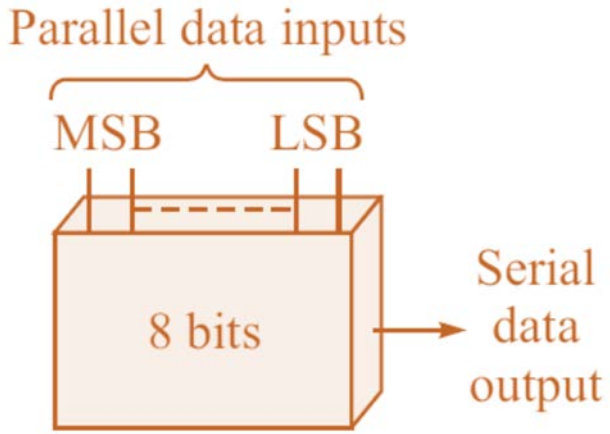


(PIPO)

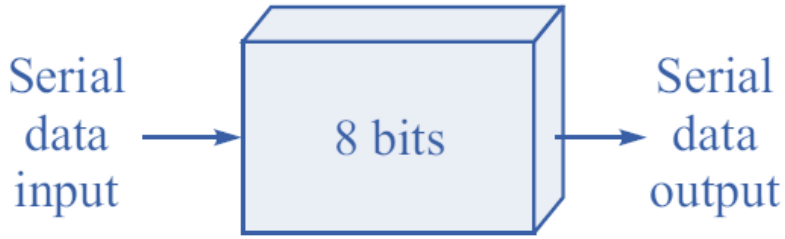
Shift Register



(**SIPO**)



(**PISO**)

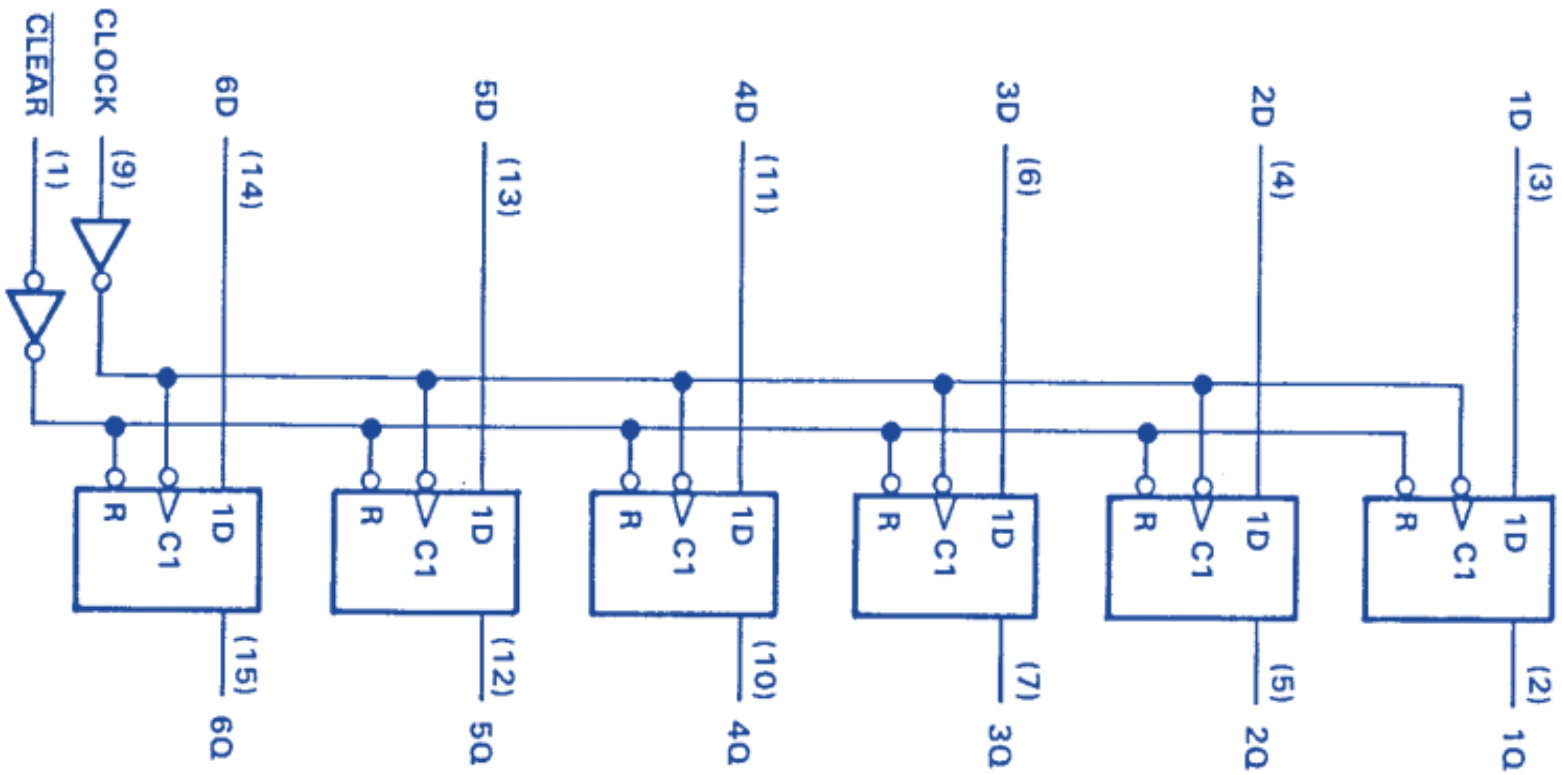


(**SISO**)

PIPO and SIPO :
Non-destructive reading

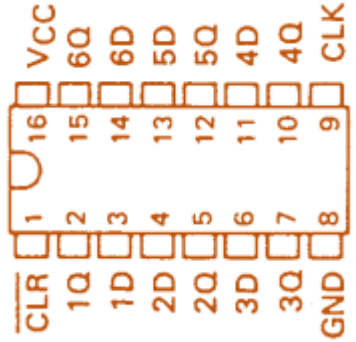
PISO and SISO :
Destructive reading ➡ External feedback for non-destructive reading

PIPO (IC 74174)



(EACH FLIP-FLOP)

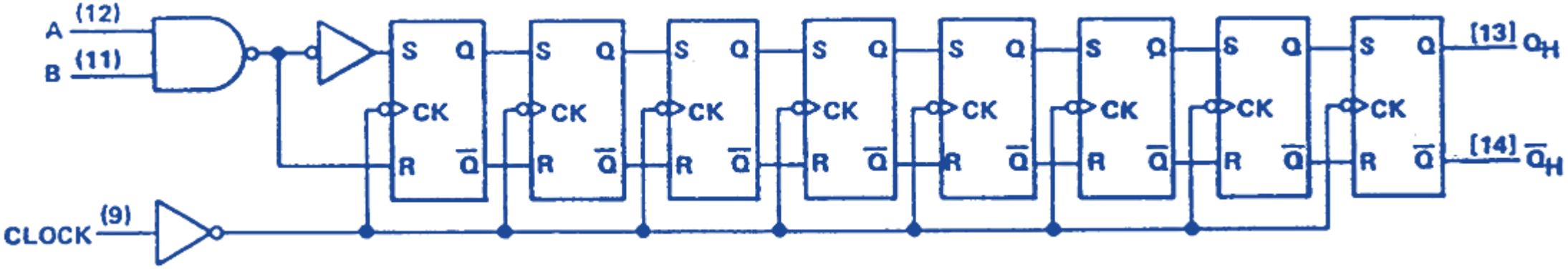
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

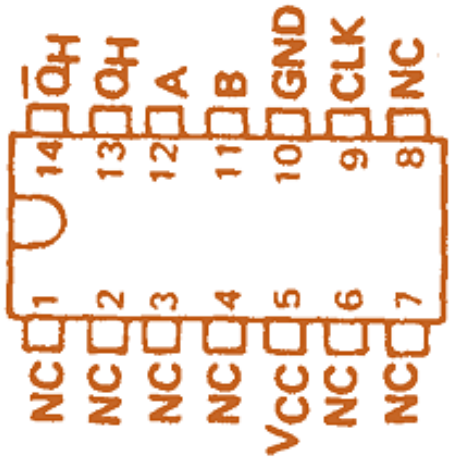


IC 74174

Note: **IC 74175** contains **4 D Flip-Flops** but both ***Q* and *Q'*** outputs in 16 pin package.

SISO (IC 7491)

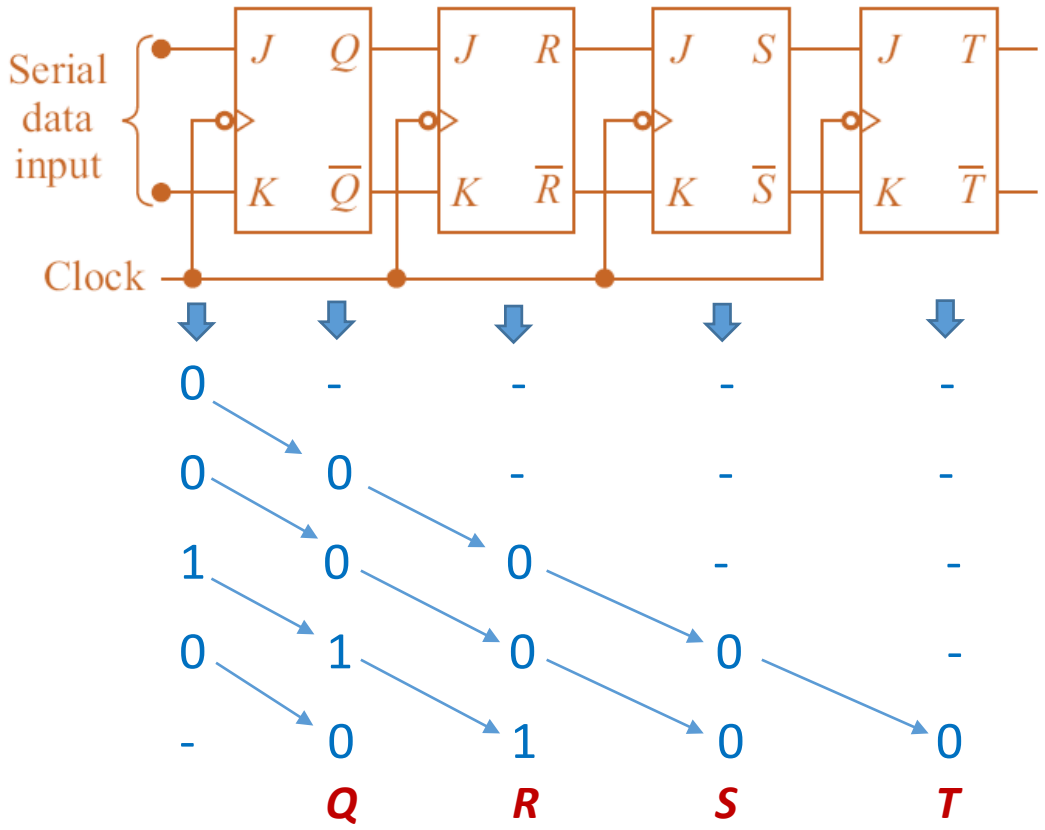


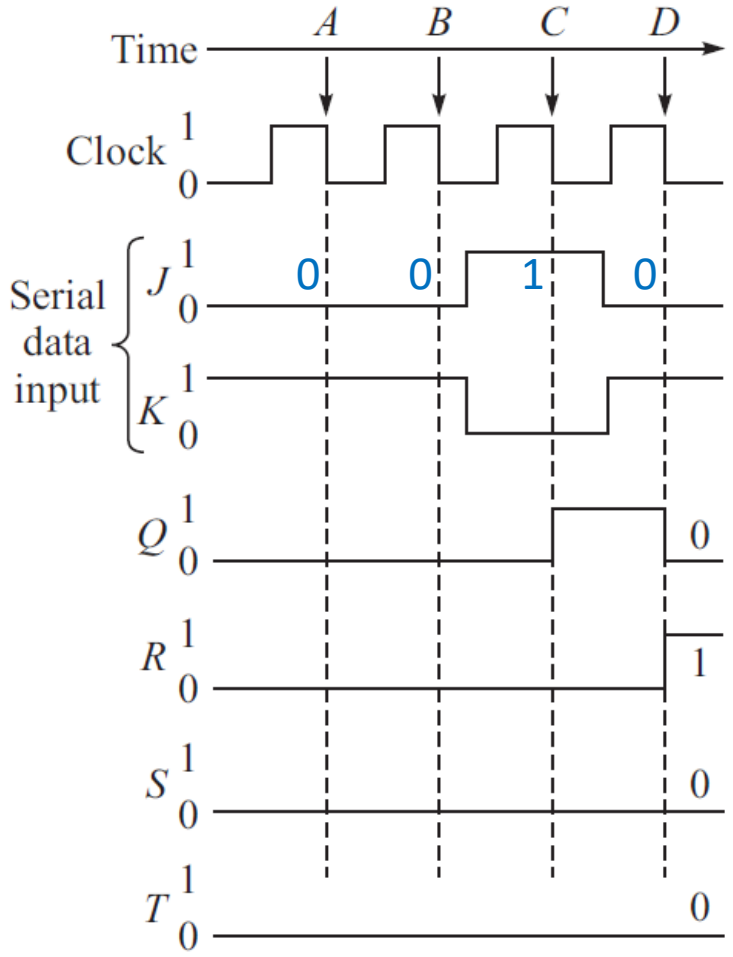


INPUTS AT t_n		OUTPUTS AT t_n+8	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

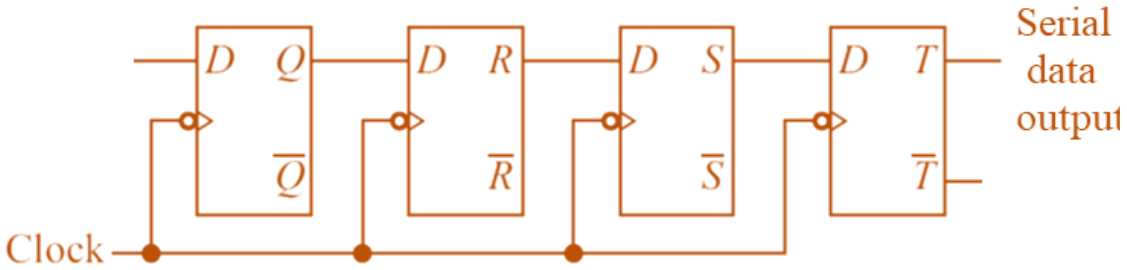
Trade-off with time

Serial in: Writing

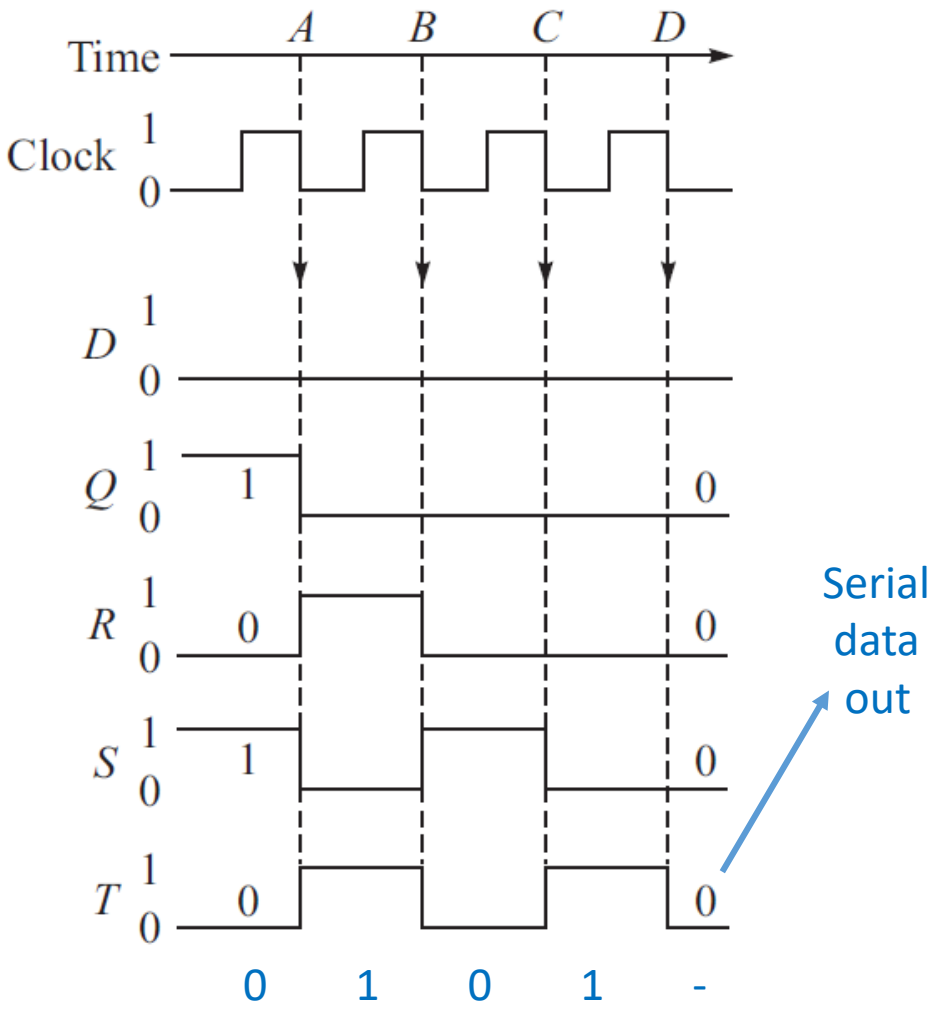




Serial out: Reading

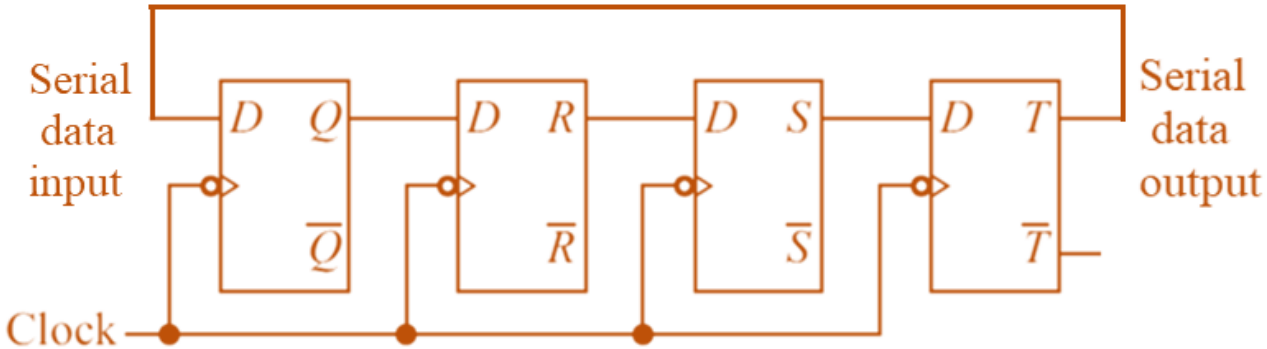


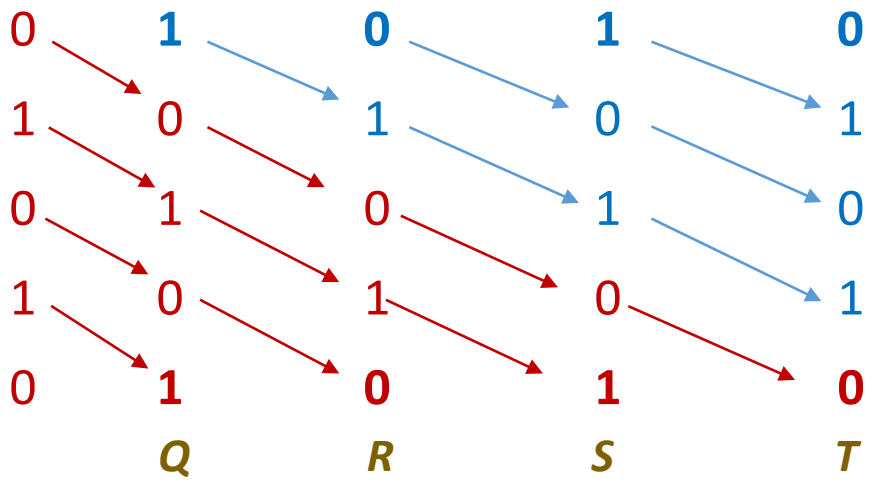
-	1	0	1	0
-	-	1	0	1
-	-	-	1	0
-	-	-	-	1
	Q	***R***	***S***	***T***



Destructive Reading: 3 clock cycles

Serial out: Reading

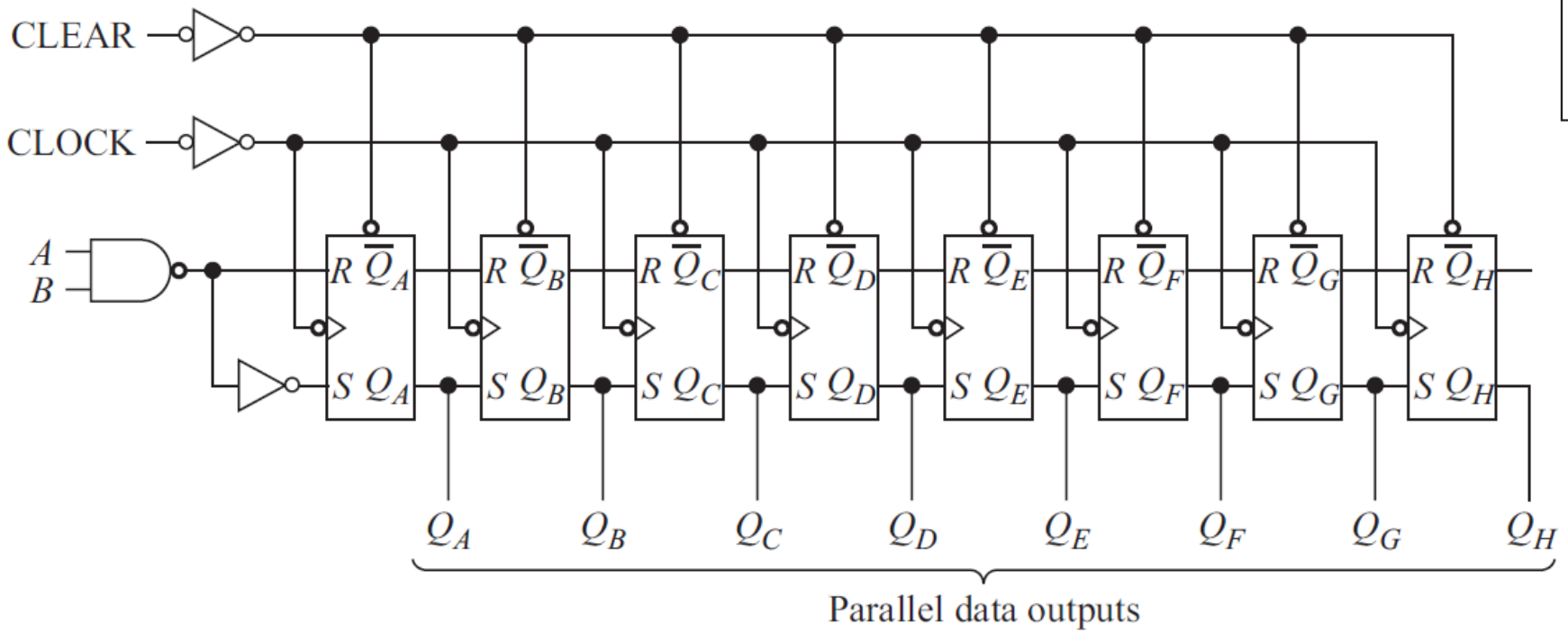


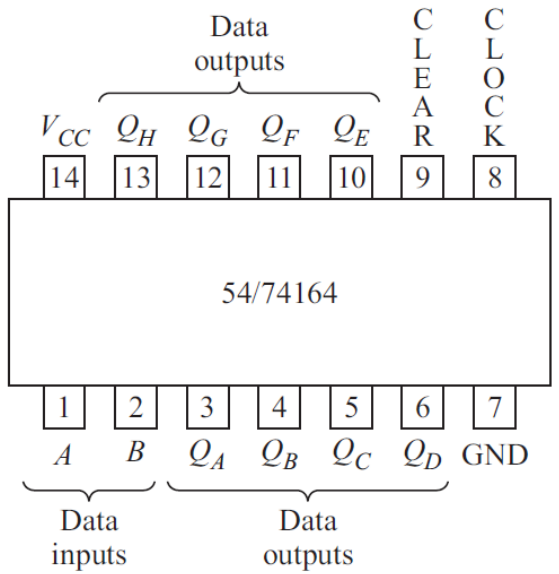


Non-destructive
Reading:
4 clock cycles

Data is rewritten while reading through external feedback.

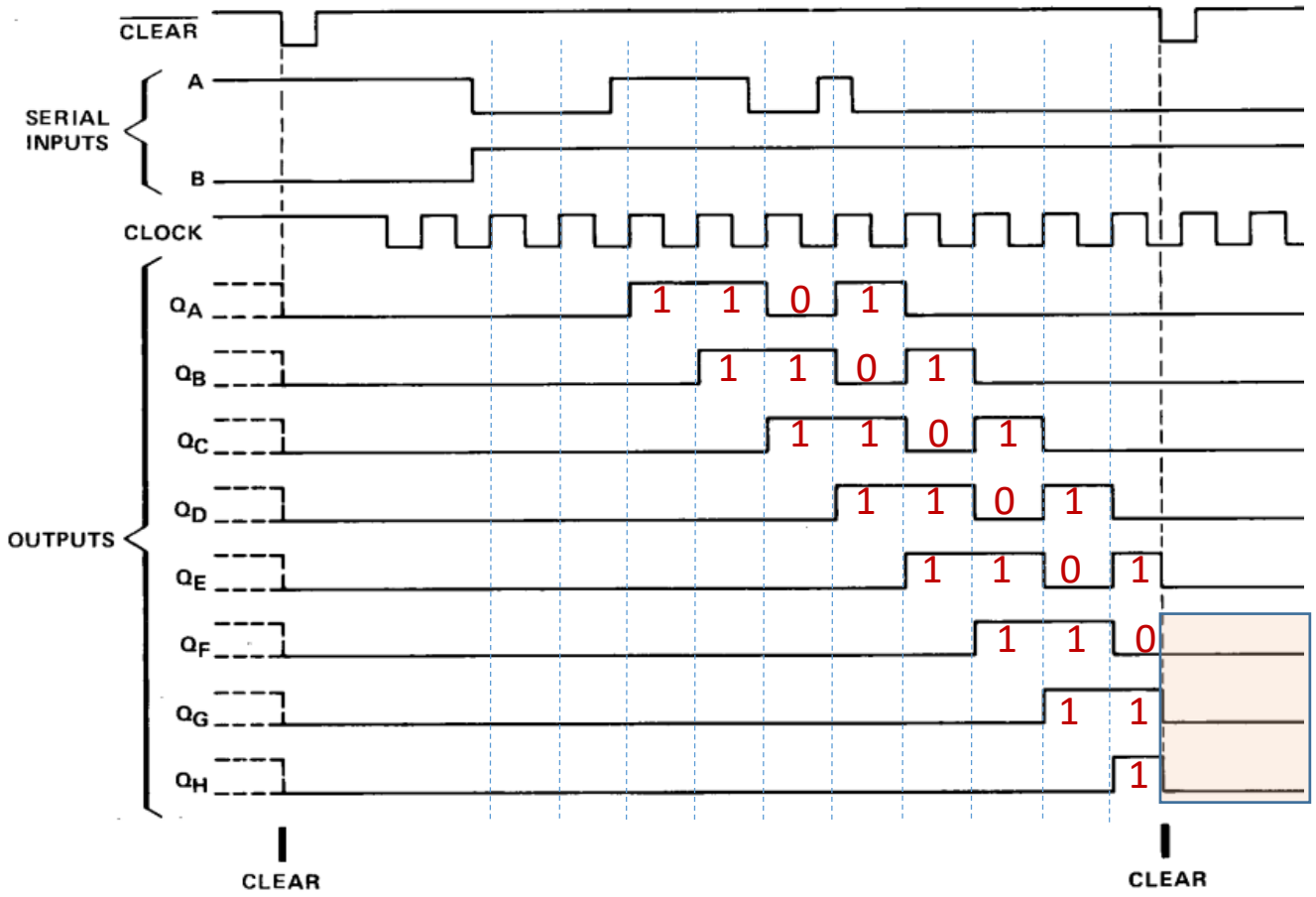
Serial In Parallel Out





Also, serial out from Q_H

Serial In and Asynchronous Reset

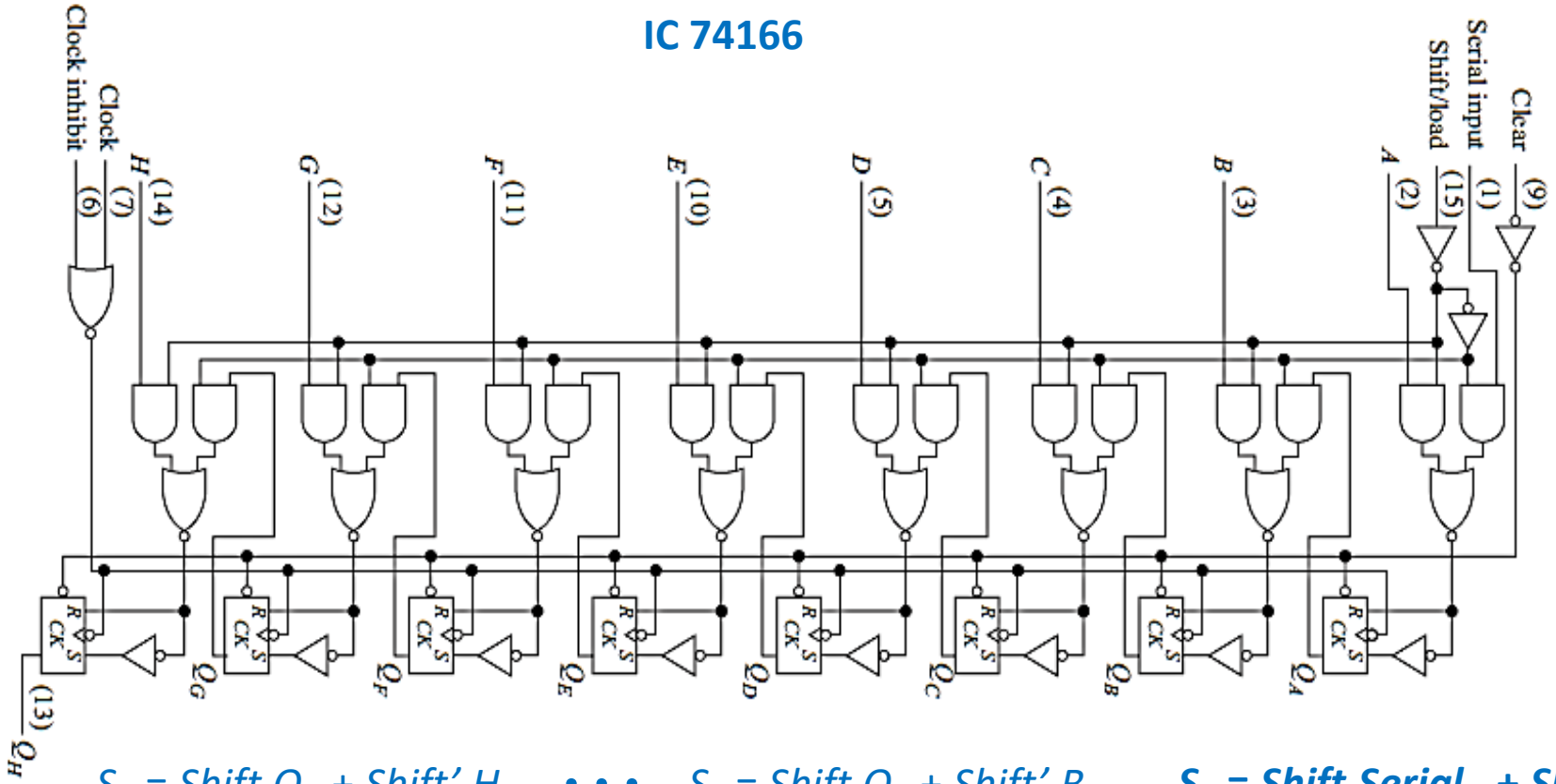


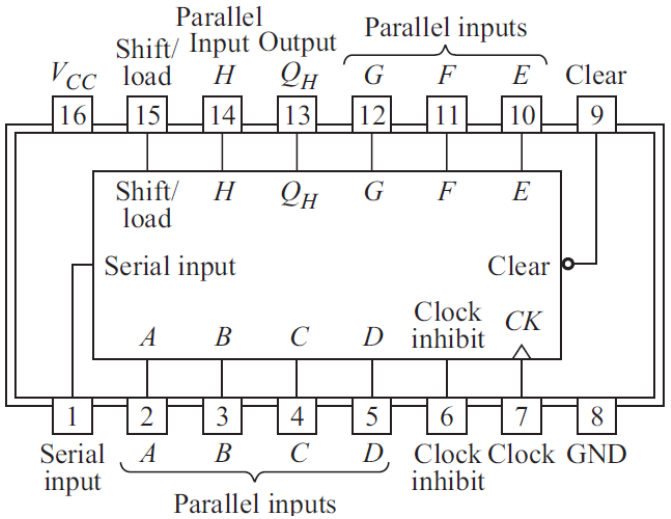
INPUTS				OUTPUTS			
$\overline{\text{CLEAR}}$	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

Q_{Xn}: Level of Q_X before last clock trigger

Parallel In Serial Out

IC 74166





It also has serial in

Pin 15 = 1: Shift

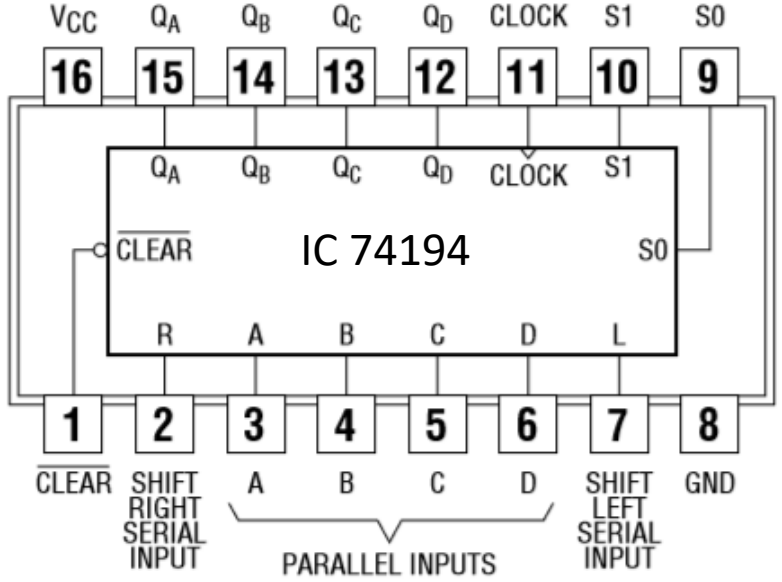
= 0: Load

$S_H = Shift.Q_G + Shift'.H$ • • • $S_B = Shift.Q_A + Shift'.B$ $\mathbf{S_A = Shift.Serial_{in} + Shift'.A}$

Universal Shift Register

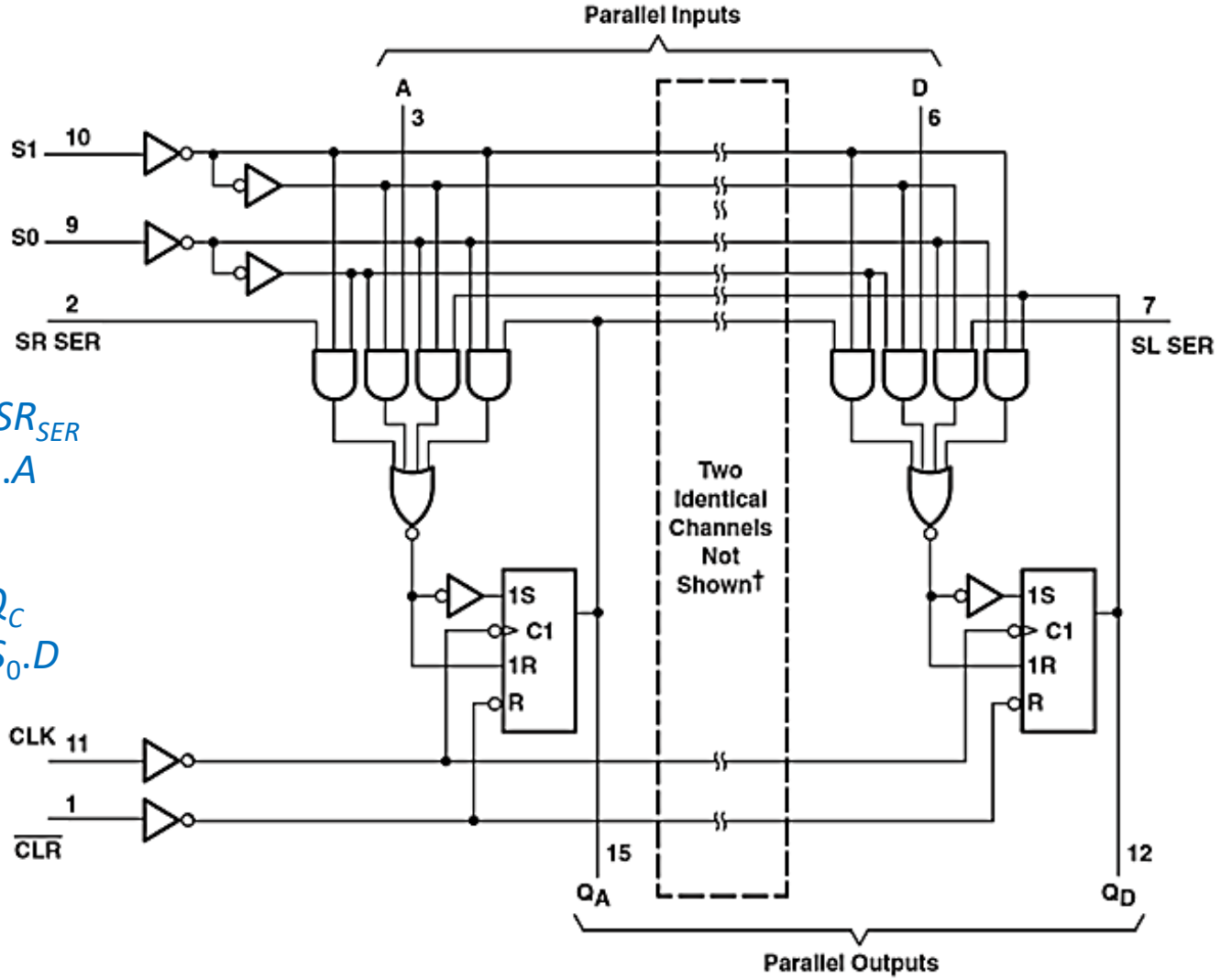
- A universal shift register can perform all four operations: PIPO, SISO, SIPO, PISO
- The shift is bidirectional.
  - Left shift: $Q_A \leftarrow Q_B \leftarrow Q_C \leftarrow Q_D \leftarrow$ Data in
  - Right shift: Data in $\rightarrow Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$

INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}



IC 74194 is a 4-bit universal shift register

IC 74194



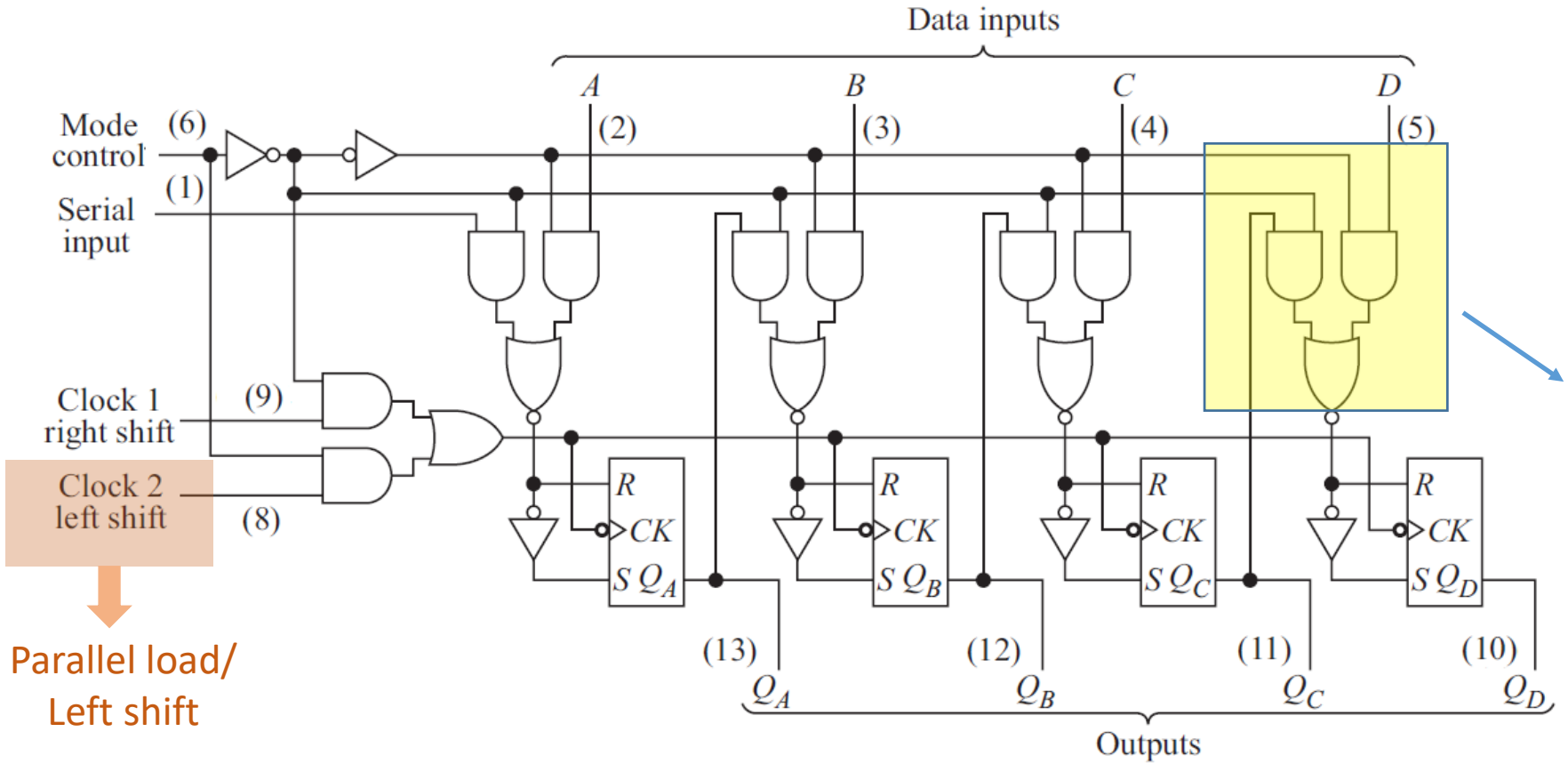
$$S_A = S_1'.S_0'.Q_A + S_1'.S_0.SR_{SER} + S_1.S_0'.Q_B + S_1.S_0.A$$

• • •

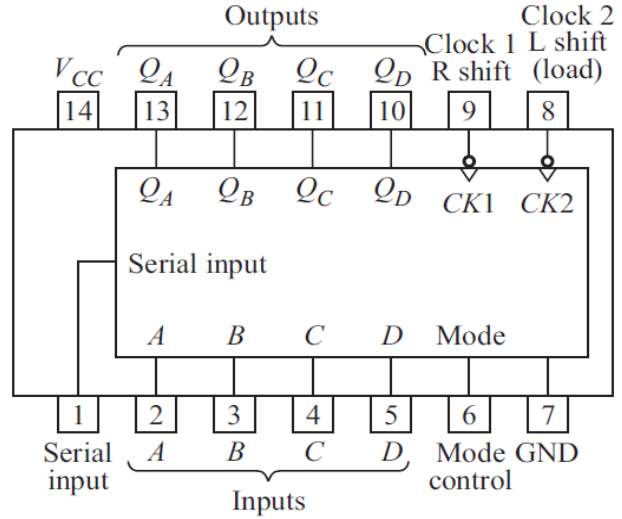
$$S_D = S_1'.S_0'.Q_D + S_1'.S_0.Q_C + S_1.S_0'.SL_{SER} + S_1.S_0.D$$

S_1	S_0	Operation
0	0	No change
0	1	Right shift
1	0	Left shift
1	1	Parallel load

IC 7495A



Parallel load/
Left shift

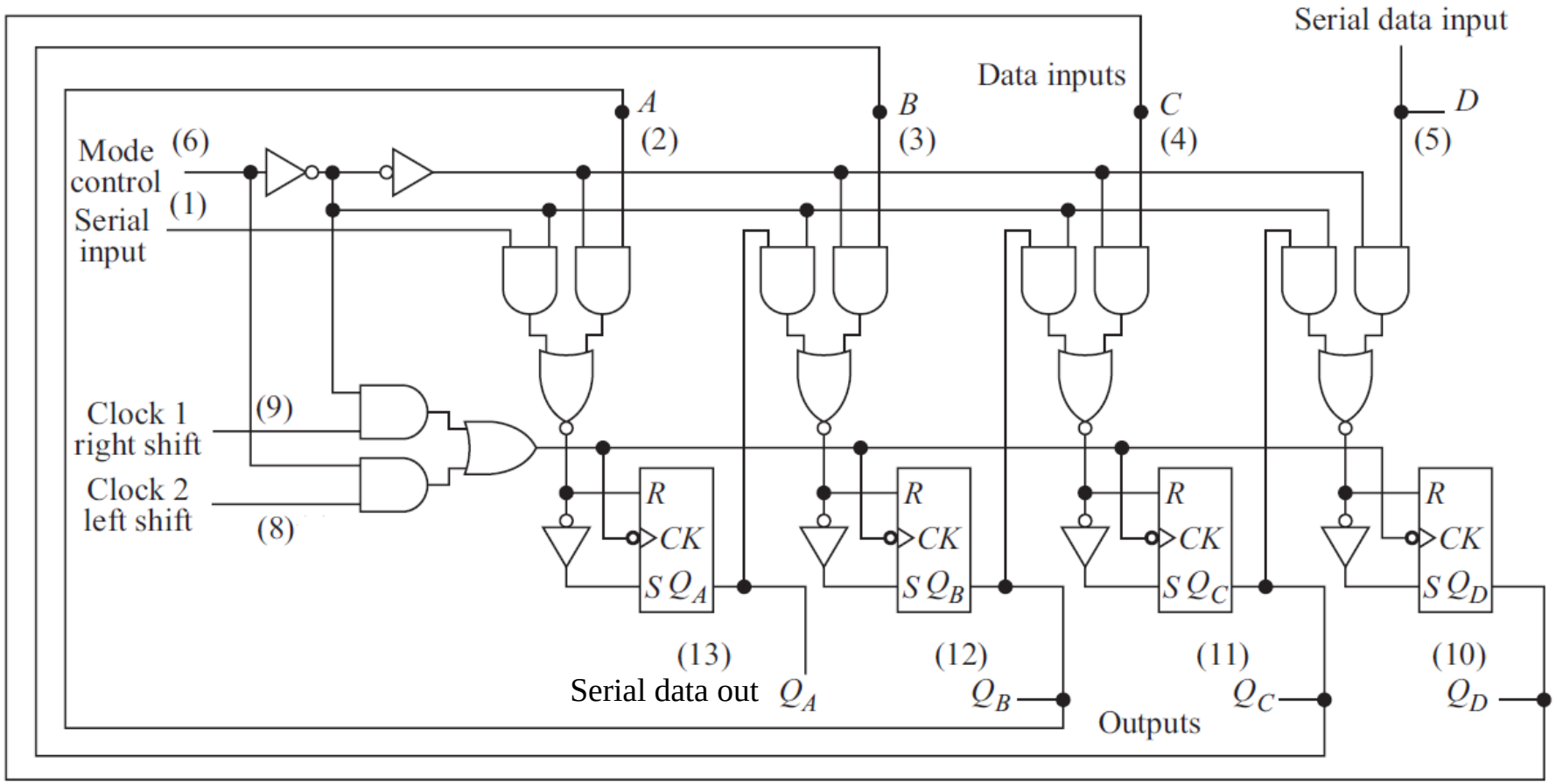


No built-in left shift!

M = 1: Parallel load

M = 0: Right shift

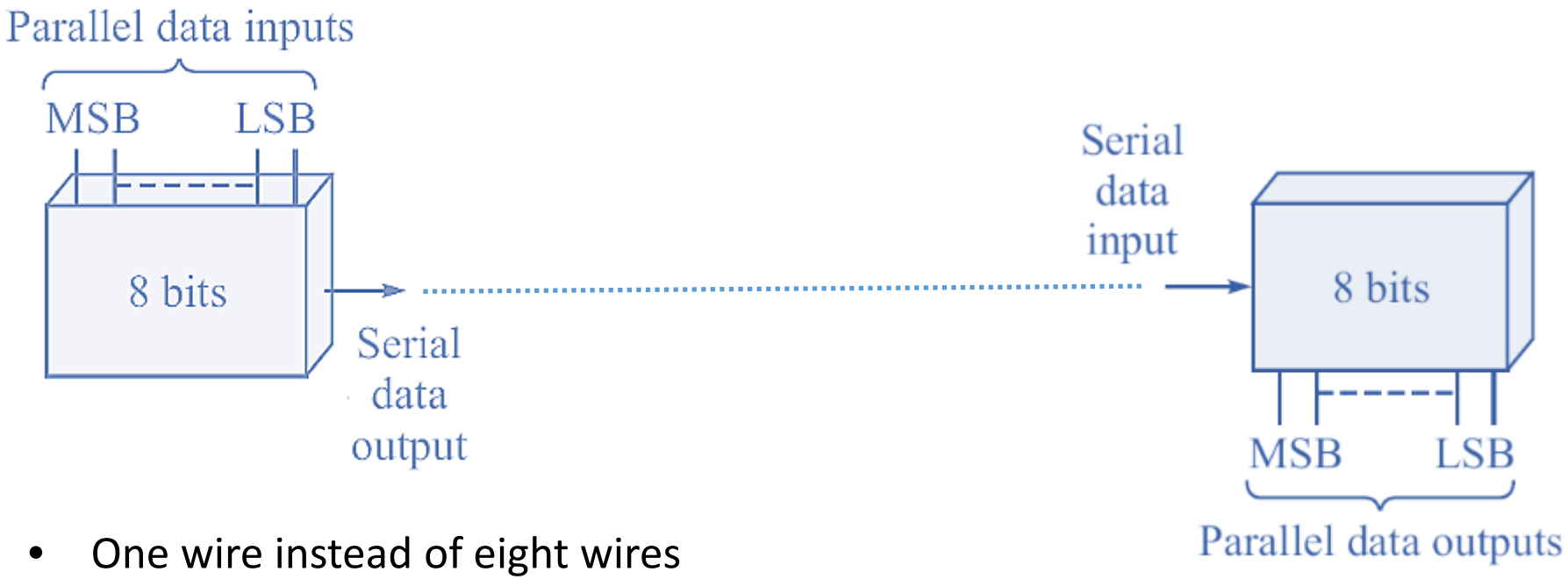
IC 7495A



Left shift through parallel load when Mode Control = 1

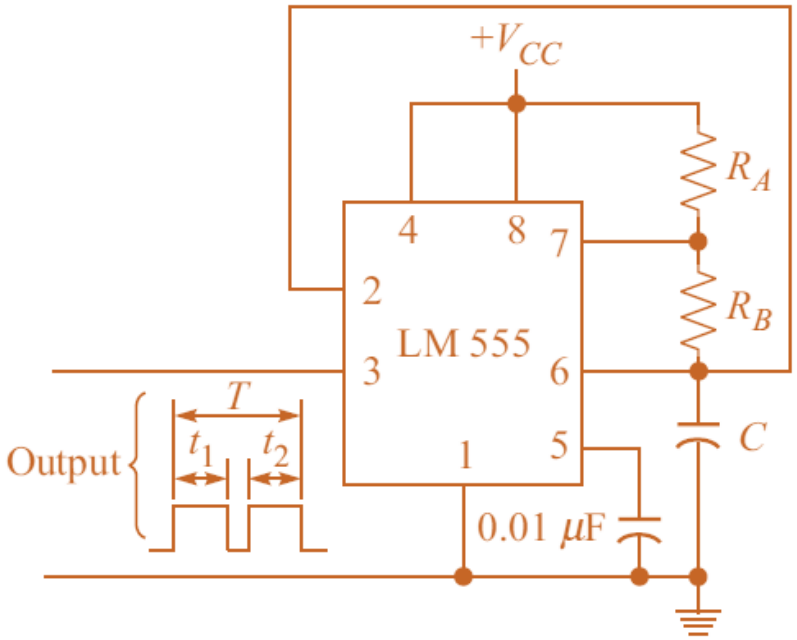
Serial Data Transmission

Appropriate protocol between transmitter and receiver on start of data and its stop.



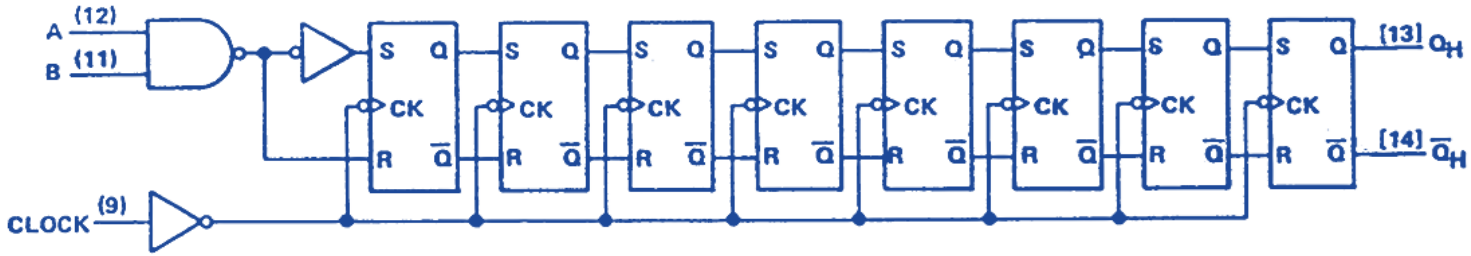
- One wire instead of eight wires
- Reduction in number of wires in transmission line reduces cost
- Trade-off is with time taken for transmission

Introducing Time Delay



- Charging time = $0.693(R_A + R_B)C$
- Discharging time = $0.693R_BC$
- Time period, $T = 0.693(R_A + 2R_B)C$

IC 7491



INPUTS AT t_n		OUTPUTS AT $t_n + 8$	
A	B	Q_H	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

Q_H Delay = 8 x T

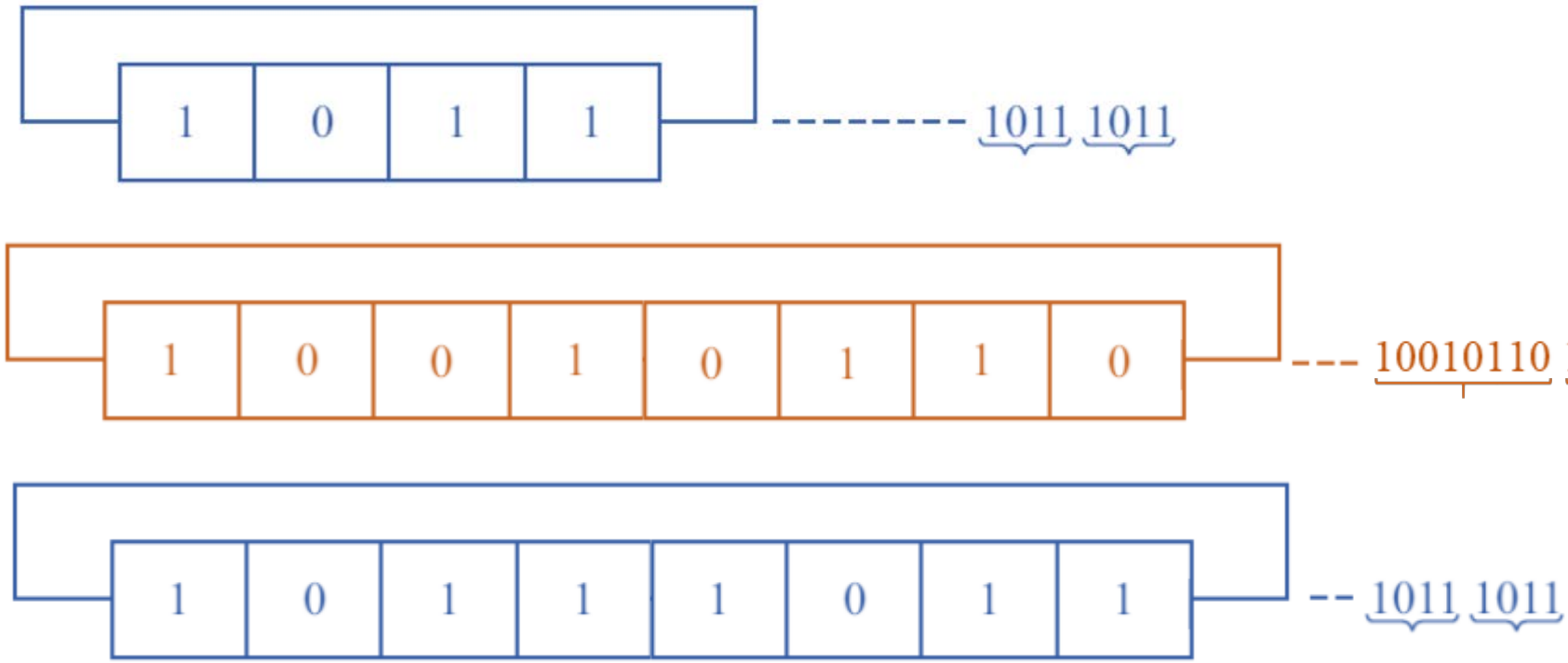
T = Time period of clock

Output after n-bit is delayed by nT time.

If T = 1 µs, then delay here is 8 µs.

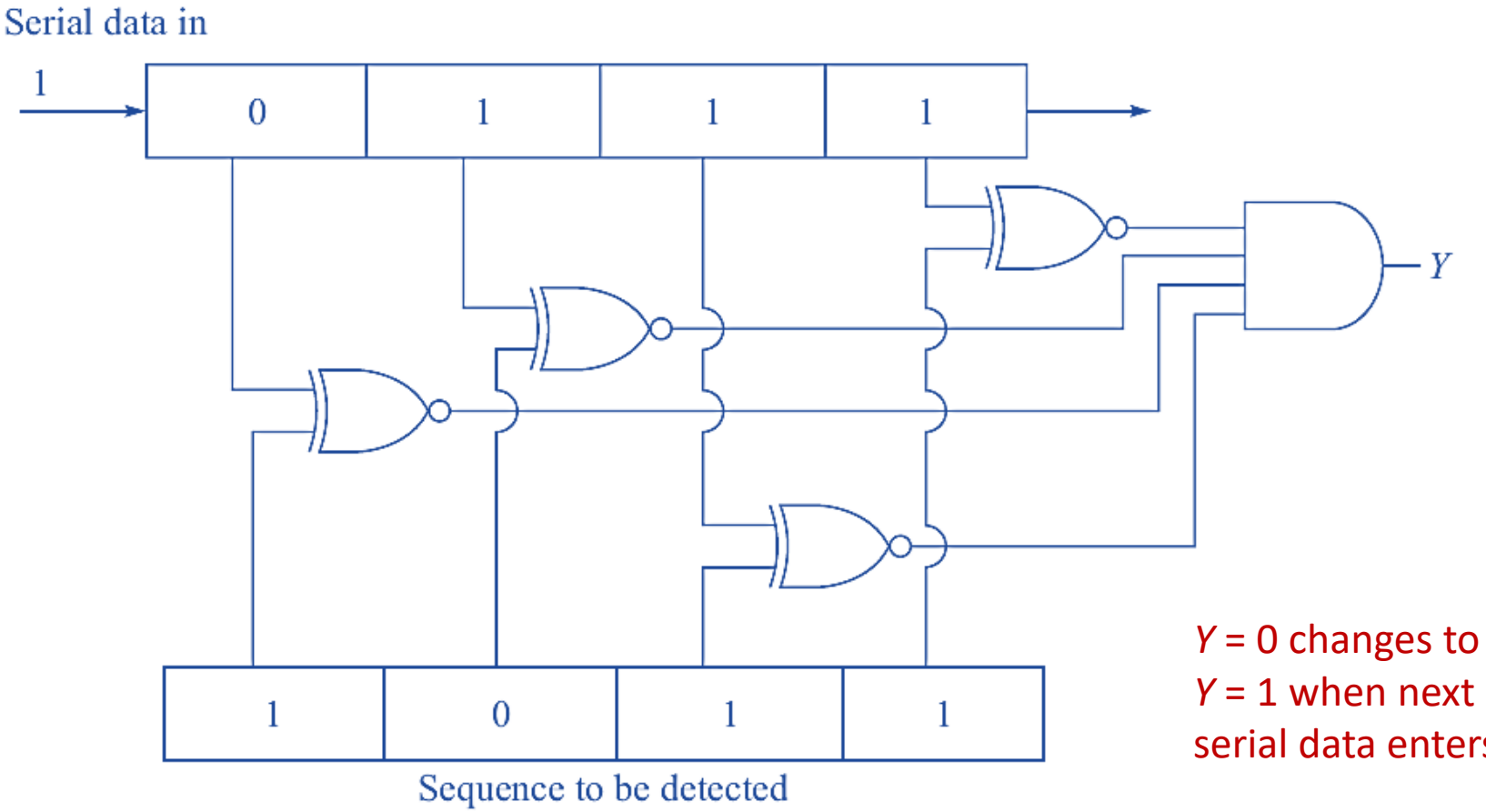
Sequence Generator

- Sequence generator is useful in generating a pattern repetitively.



With serial data out fed back directly as serial data in, *n*-bit shift register can generate up to *n*-bit long pattern.

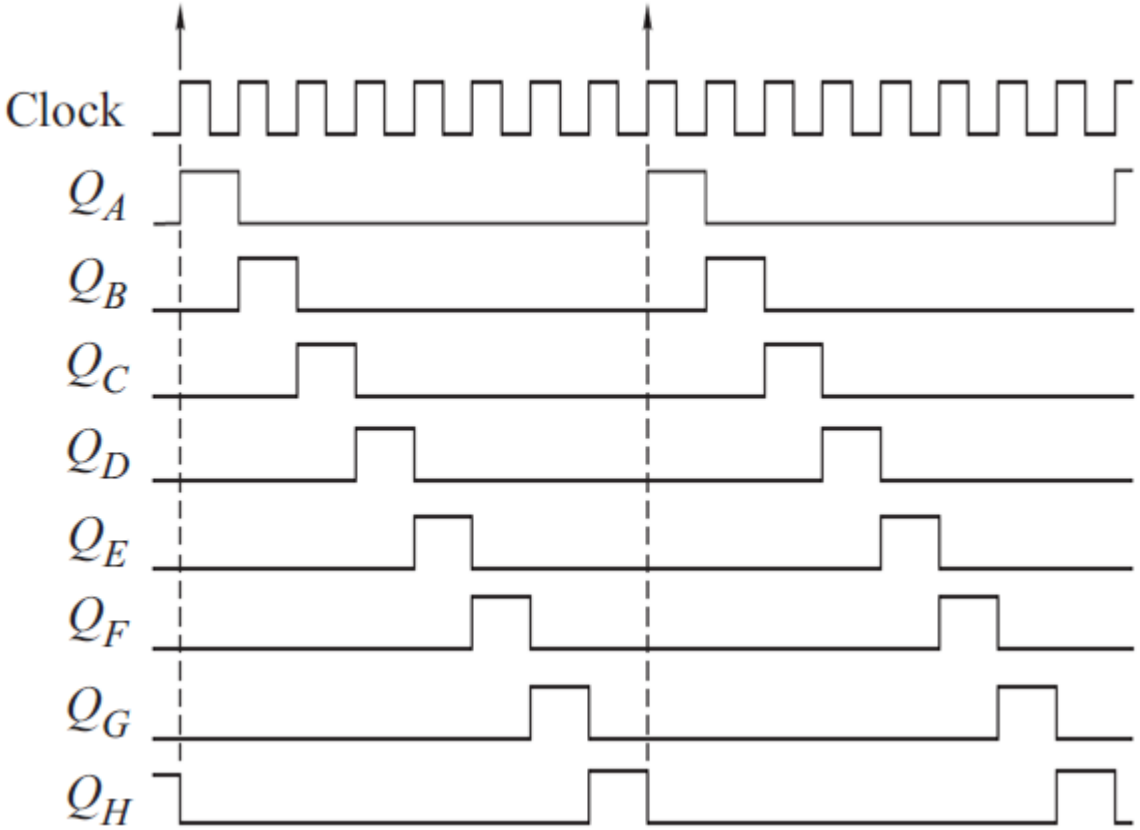
Sequence Detector



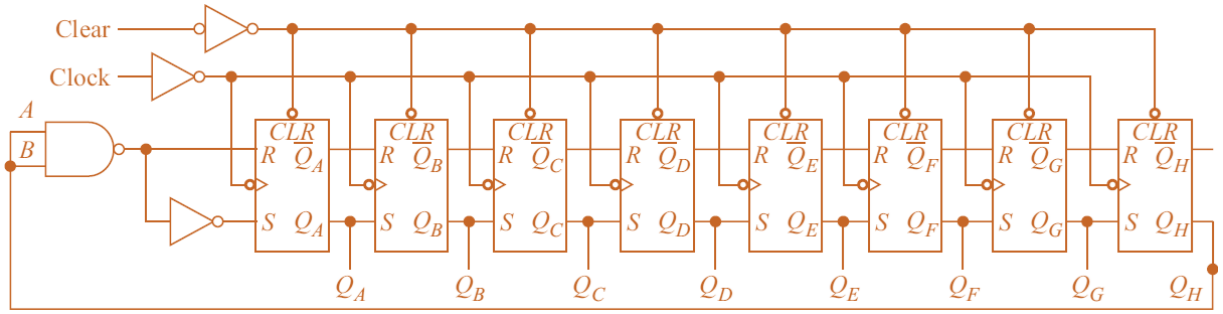
Y = 0 changes to *Y* = 1 when next serial data enters.

- Sequence detector identifies a specific pattern from incoming bit string.
- Sequence to be detected can be hard-wired to V_{CC} and GND in the circuit.
- The register gives a convenient option to change the pattern to be detected.

Ring Counter



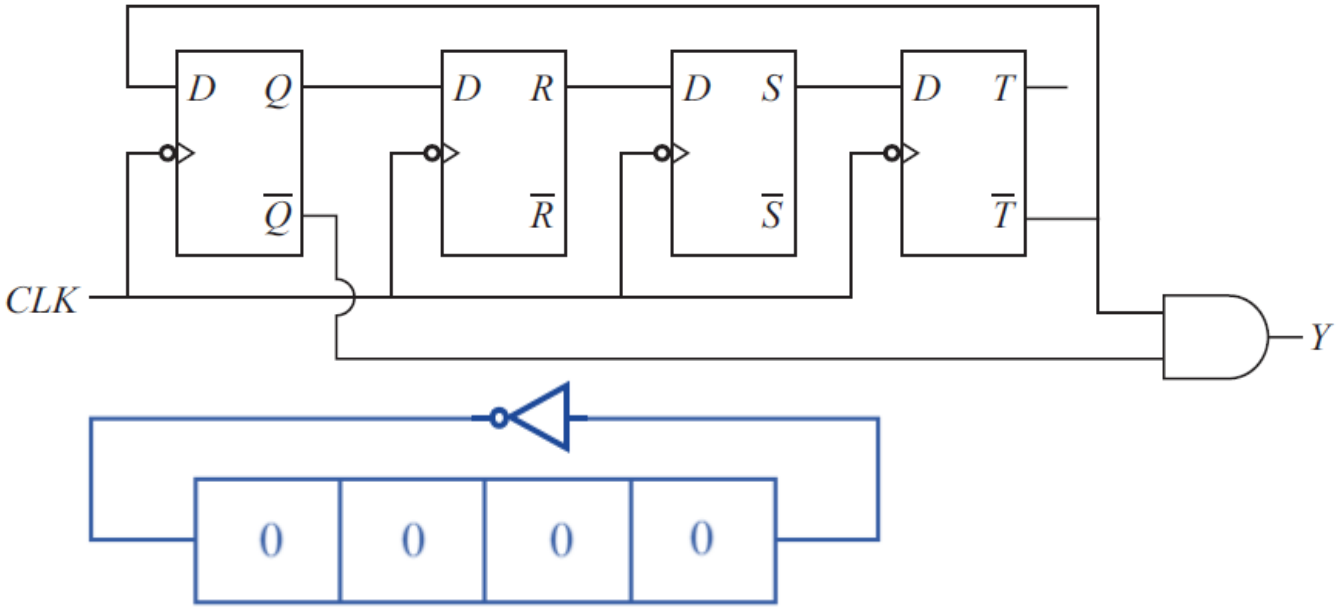
IC 74164



Serial data out = 1 once in every *n* clock cycle for a *n*-bit shift register connected as shown.

Johnson Counter

Clock	Serial in $= T'$	Q	R	S	T	$Y = Q'T'$
0	1	0	0	0	0	1
1	1	1	0	0	0	0
2	1	1	1	0	0	0
3	1	1	1	1	0	0
4	0	1	1	1	1	0
5	0	0	1	1	1	0
6	0	0	0	1	1	0
7	0	0	0	0	1	0
8	1	0	0	0	0	1
9	1	1	0	0	0	0 repeats



- Also called Switched-Tail or Twisted-Tail Counter.
- **With *n*-bit register a count of 2*n* can be obtained.**
- Different initialization possible.
- 2-input gate to decode.

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Texas Instrument's Digital Logic Pocket Data Book (2007)