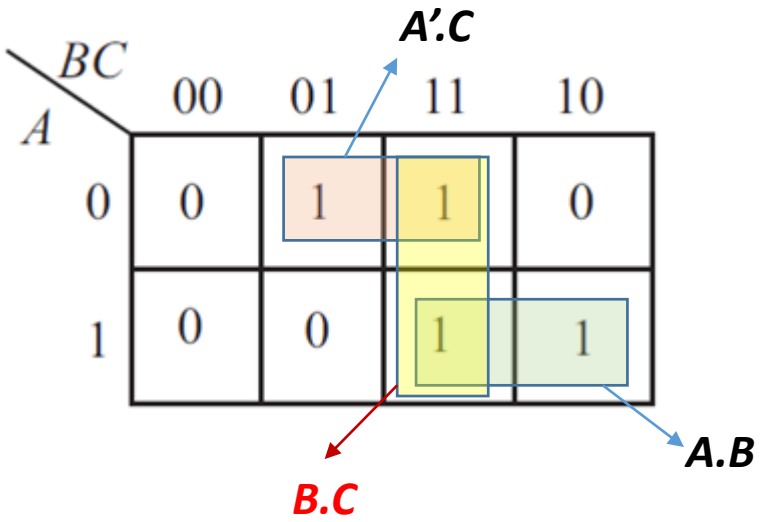
Digital Electronic Circuits
Section 1 (EE, IE)

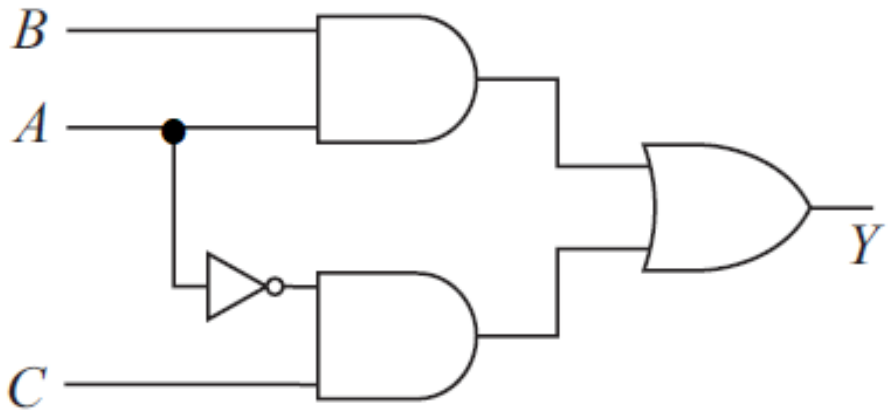
Lecture 9

Minimization and Propagation Delay



Truth Table is realized by

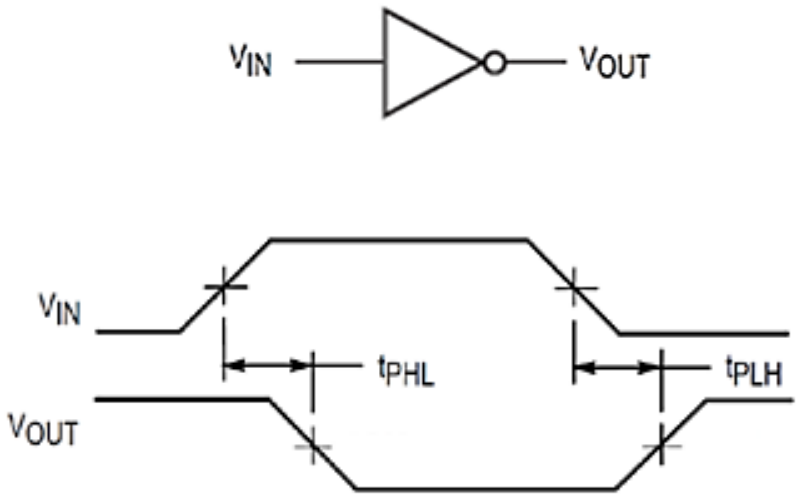
$Y = A'.C + A.B$

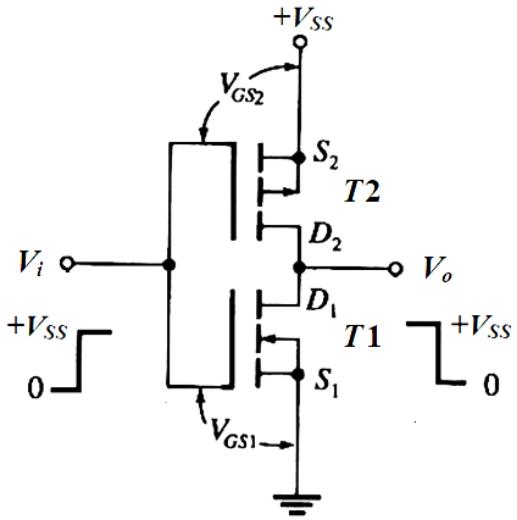


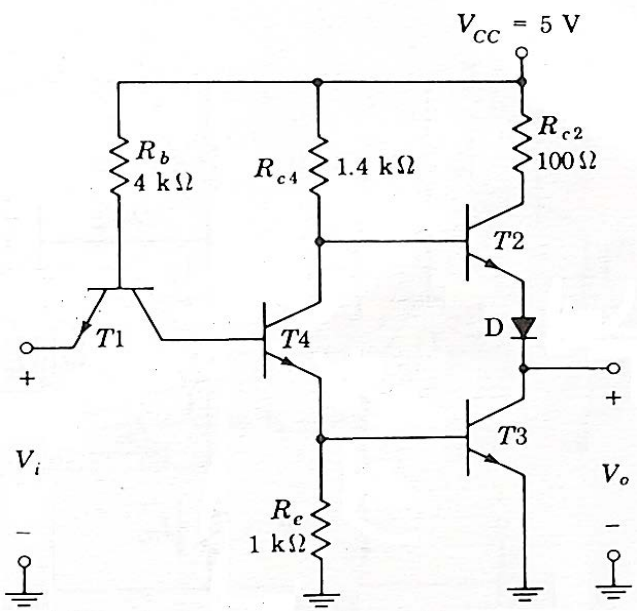
B.C : Redundant P.I. Its inclusion increases cost 'unnecessarily'.

In this, effect of propagation delay in logic gates is not considered.

Propagation Delay in Logic Gate





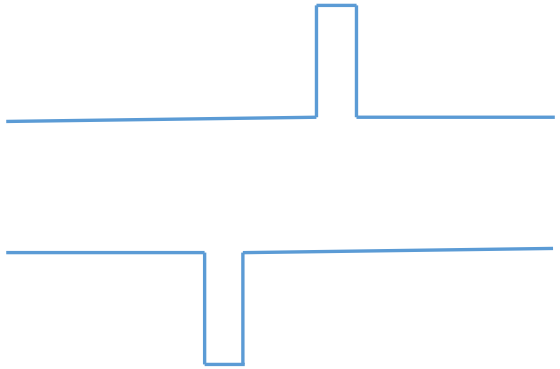


Logic operations realized by logic gates have finite propagation delay.

Prop. Delay: TTL ≈ 10 ns
CMOS ≈ 50 ns
(depends on load; also, supply voltage for CMOS)

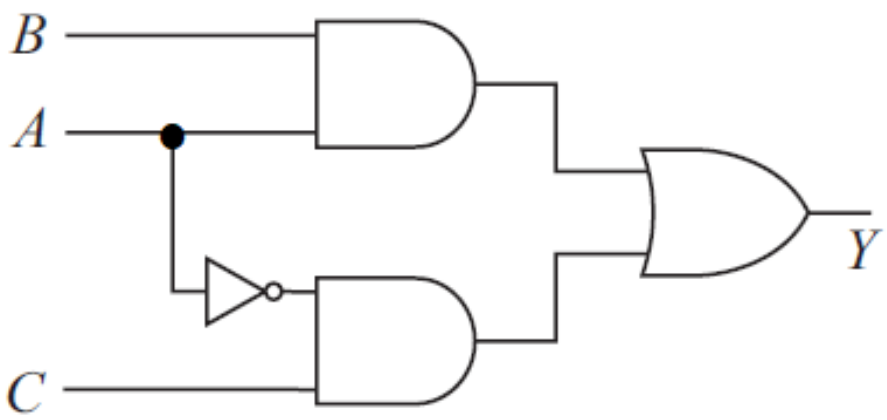
Glitches and Hazards in Logic Circuit

- Glitches are undesired positive or negative going pulse in a digital logic circuit.
- Glitch occurs due to finite propagation delay of logic gates and occurs for specific combinations of input (not for other combinations)
- Glitch is transient in nature and has short duration (≈ ns).



- A logic circuit has Hazard if there is a potential for glitch.
- A circuit with hazard may generate glitch depending on input combination.

Example of Glitch



$Y = A'.C + A.B$

Consider, $B = 1$, $C = 1$

Then, $Y = A'.1 + 1.A$
$= A' + A$
$= 1$

i.e. $Y = 1$, always
for $B = 1$, $C = 1$
as per Boolean Algebra

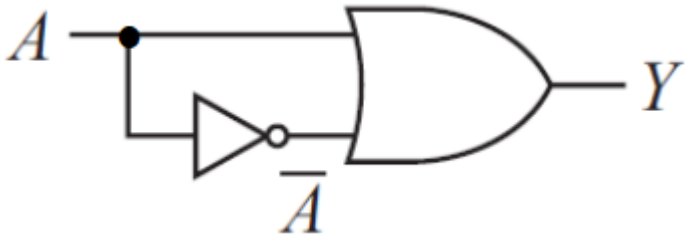
$B = 1, C = 1, A : 1 \rightarrow 0$

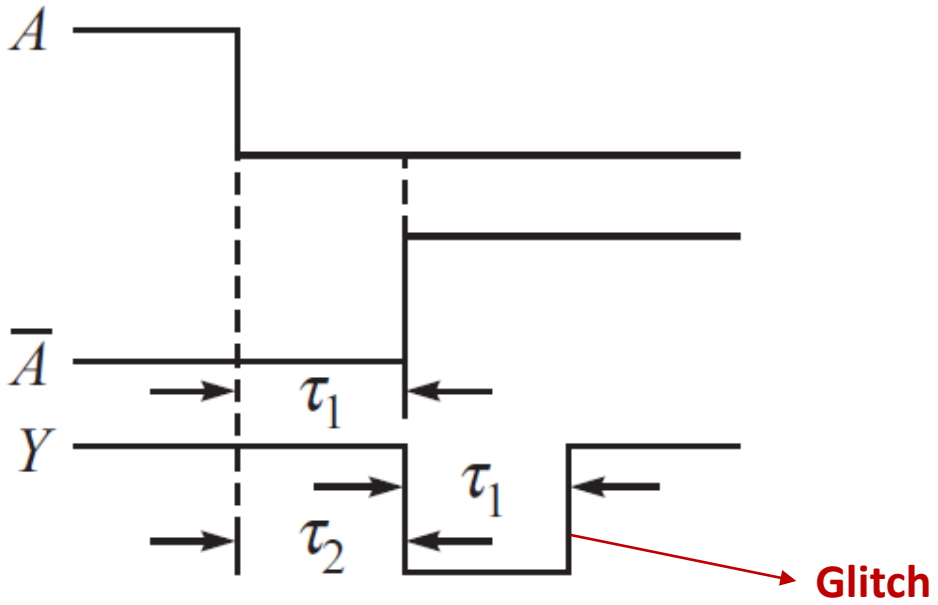
Glitch occurs: Due to propagation delay of NOT gate, both AND Gates have 0 in one of the inputs for a short duration.

Glitch: $B = 1, C = 1, A : 1 \rightarrow 0$
No Glitch: $B = 1, C = 1, A : 0 \rightarrow 1$

Static 1 Hazard

$A' + A = 1$





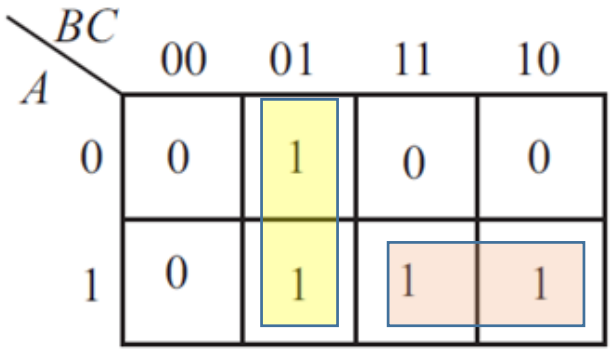
In Static 1 Hazard, output should remain static at 1 according to Boolean Logic but glitch occurs under certain conditions.

τ_1 = NOT gate delay

τ_2 = OR gate delay

Detecting Static 1 Hazard

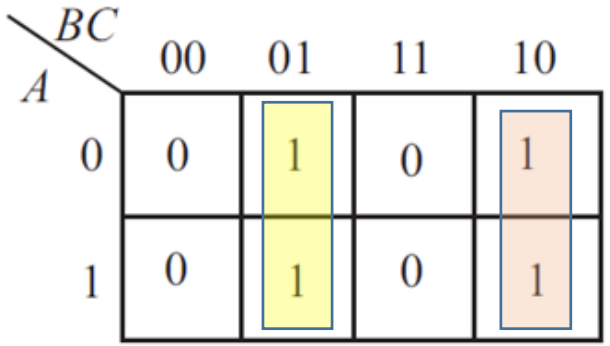
- Two logically adjacent cells with output 1 in K-Map not covered by a common product term.
- Boolean expression produces (*A* + *A'*) for certain condition.



Y = B'.C + A.B

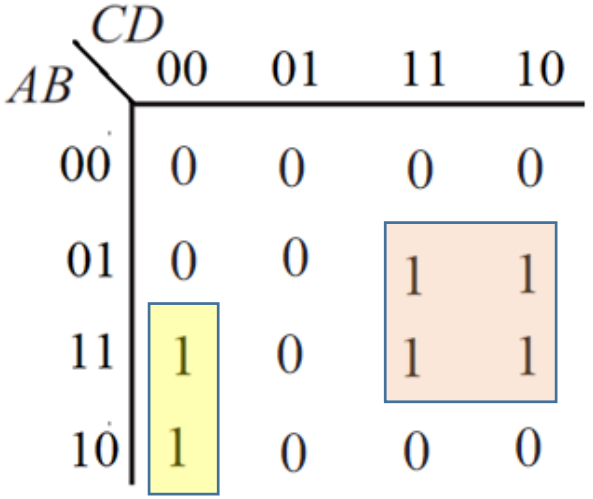
AC* = 11, *Y = B + B'

Glitch, *ABC* : 111 → 101



Y = B'.C + B.C'

No Hazard for one variable changing



Y = B.C + A.C'.D'

ABD* = 110, *Y = C + C'

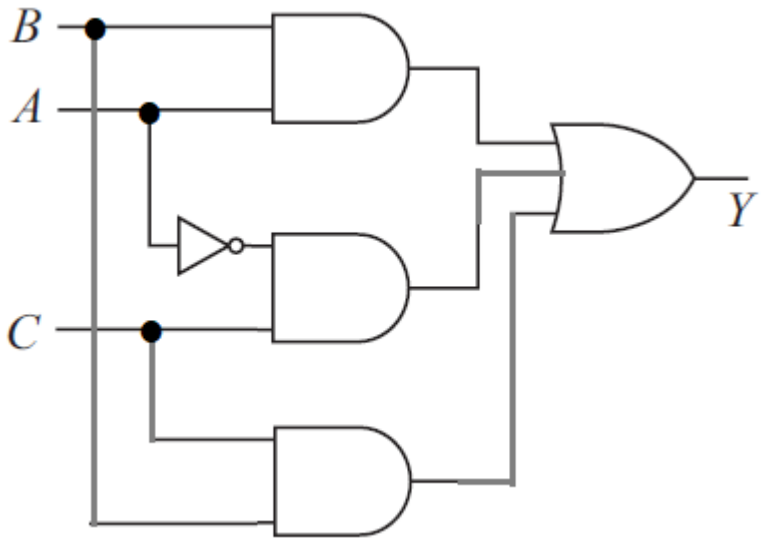
Glitch: Static 1 Hazard

***ABCD* : 1110 → 1100**

Covering Static 1 Hazard

A \ BC	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$Y = A'.C + A.B + B.C$



Hazard-free circuit

Hazard-free by covering with common product term (redundant in SOP minimization)

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	1	0	1	1
10	1	0	0	0

$Y = B.C + A.C'.D' + A.B.D'$

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Technical documents from http://www.ti.com accessed on Oct. 08, 2018