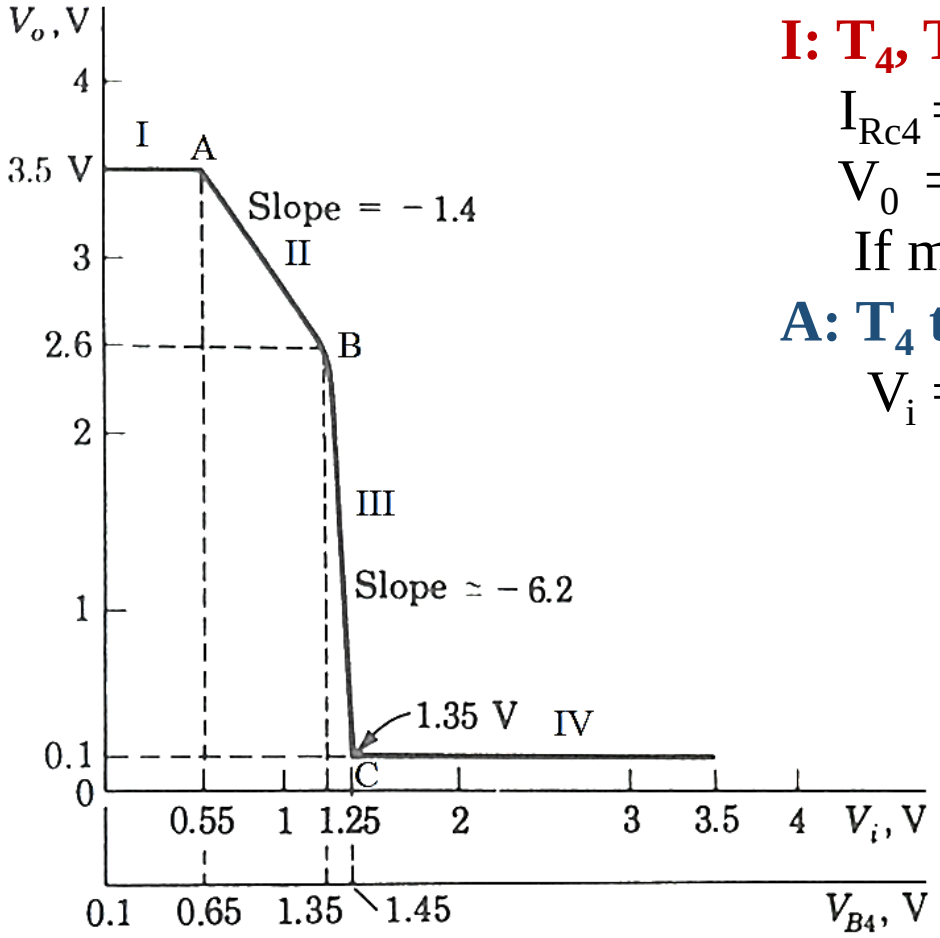
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 3

TTL: Transfer Characteristics



I: T_4, T_3 Cut-off. T_1 Sat., T_2 Active

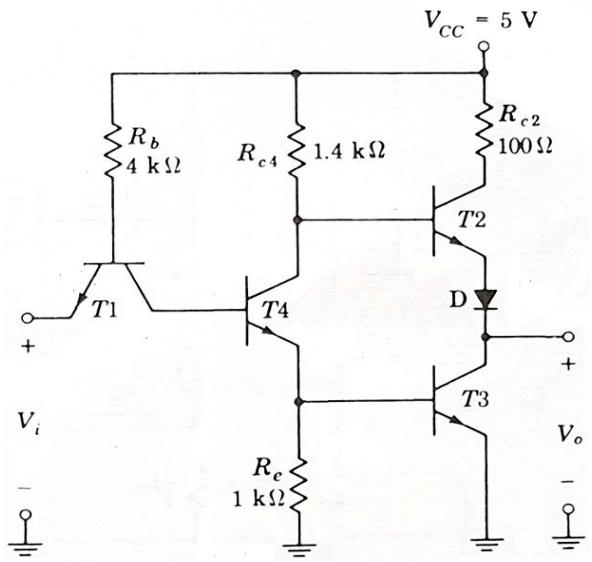
$I_{Rc4} = I_{B2}$ negligible

$V_0 = 5 - 2x0.7 = 3.6V$

If more load, $V_0 = 5 - 2x0.75 = 3.5V$

A: T_4 turns on at $V_{BE4} = 0.65$ V

$V_i = 0.65 - V_{CE1(Sat)} = 0.55$ V



II: T_4 active. T_3 Cut-off. T_1 Sat., T_2 Active

$I_{RC4} \approx I_{C4}$ NOT negligible

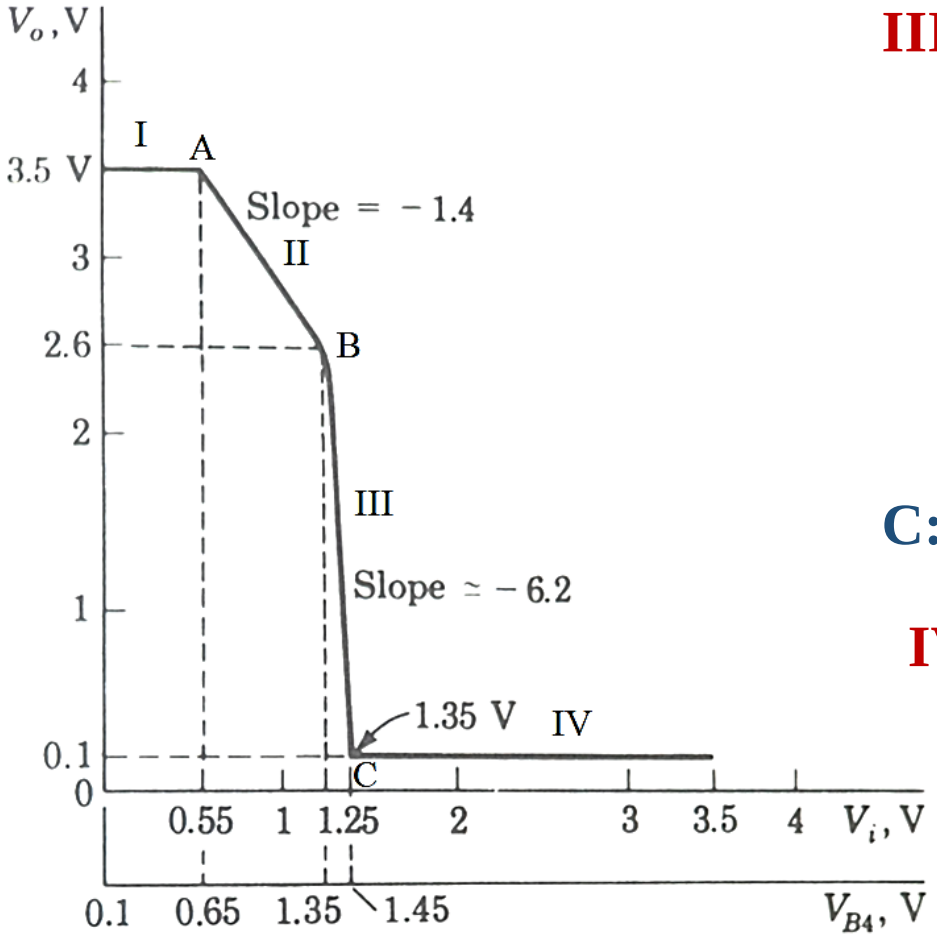
$A_{V4} = -(R_{c4} / R_e) = -1.4$

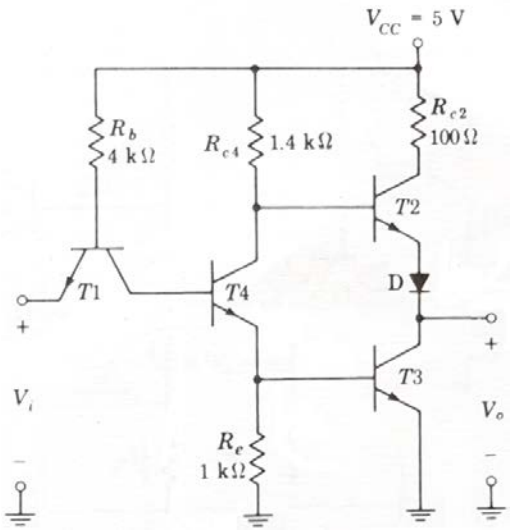
$A_{V2} = 1$ (emitter follower)

B: T_3 turns on at $V_i = 0.7 + 0.65 - 0.1$

$V_o = 3.5 - (1.4 \times 0.65/1) = 2.6$ V

TTL: Transfer Characteristics





III: T_4, T_3 Active. T_1 Sat. T_2 Active to Off

$A_{V4} = - (R_{c4} / R_e \| r_d) = -2.8$

$A_{V3} = \Delta V_0 / \Delta V_{B3} = - (\beta_F R_{c3(eff.)} / r_d)$

$R_{c3(eff.)} = (r_{d(D)} + r_{d(T2)} + R_{c4})/\beta_F$

$A_{V3} = - (1.4 + 1 + 1) / 1 = - 3.4$

$\Delta V_0 = A_{V4} \Delta V_{B4} + A_{V3} \Delta V_{B3}$

$A_V = A_{V4} + A_{V3} = - 6.2$ [as $\Delta V_{B4} = \Delta V_{B3}$]

C: T_3 saturates at $V_i = 0.75 + 0.7 – 0.1$ V

IV: T_4, T_3 Sat. T_2 Cut-off. T_1 inverse

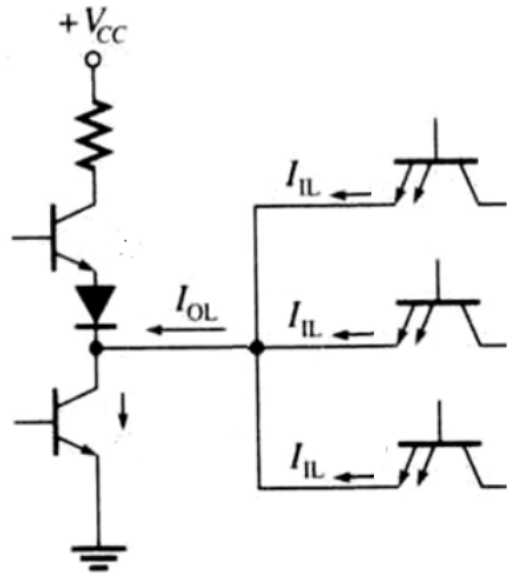
T_4, T_3 saturate at $V_i = 2 \times 0.75 – 0.1$ V

$V_0 = 0.1$V

SN7404 Datasheet

Texas Instruments (Revised 2004)

Parameter	Min.	Typical	Max.	Unit
V_{IH}	2			V
V_{IL}			0.8	V
I_{OH}			-0.4	mA
I_{OL}			16	mA
V_{OH}	2.4	3.4		V
V_{OL}		0.2	0.4	V
I_{IH}			40	µA
I_{IL}			-1.6	mA
t_{PLH}		12	22	ns
t_{PHL}		8	15	ns



Fanout = Lower [$|I_{OH}/I_{IH}|$, [$|I_{OL}/I_{IL}|$]=10

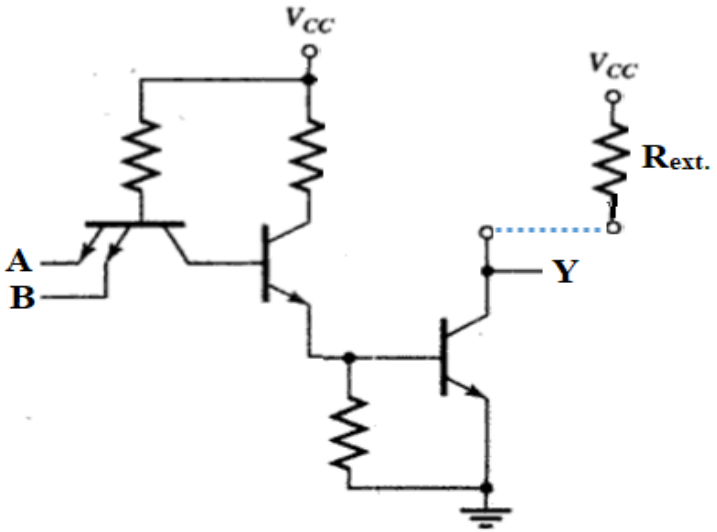
$NM_L = V_{IL} - V_{OL} = 0.8 - 0.4 = 0.4V$

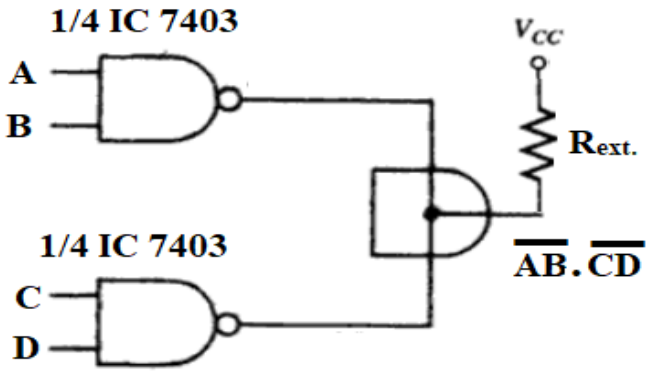
$NM_H = V_{OH} - V_{IH} = 2.4 - 2 = 0.4V$

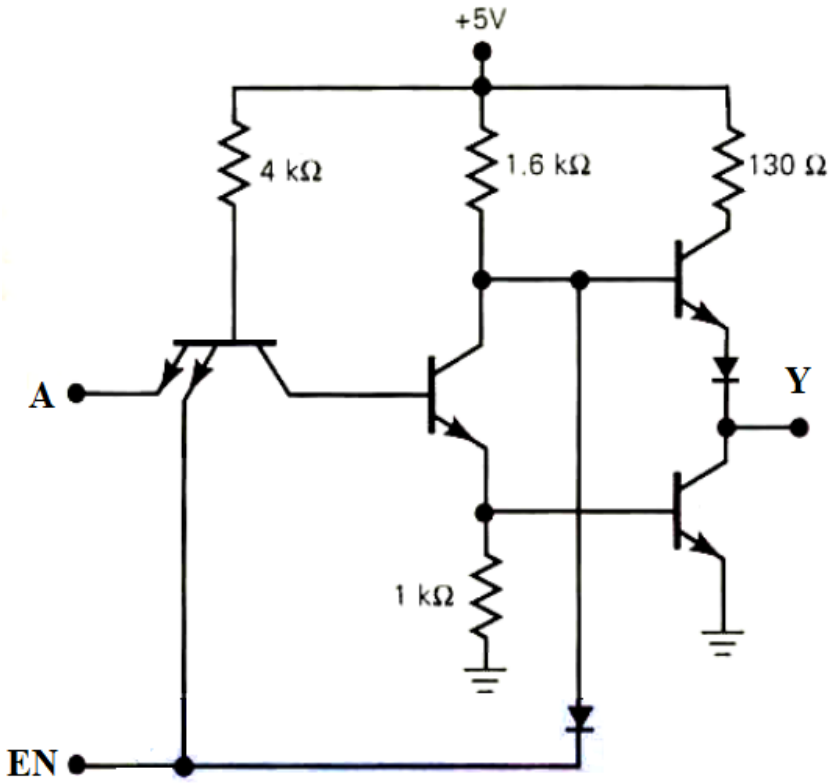
P_D = 10mW

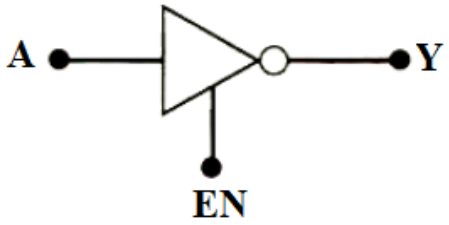
Note: Under specific test condition
e.g. R_L=400Ω, C_L=15pF

TTL: Open Collector, Tri-state

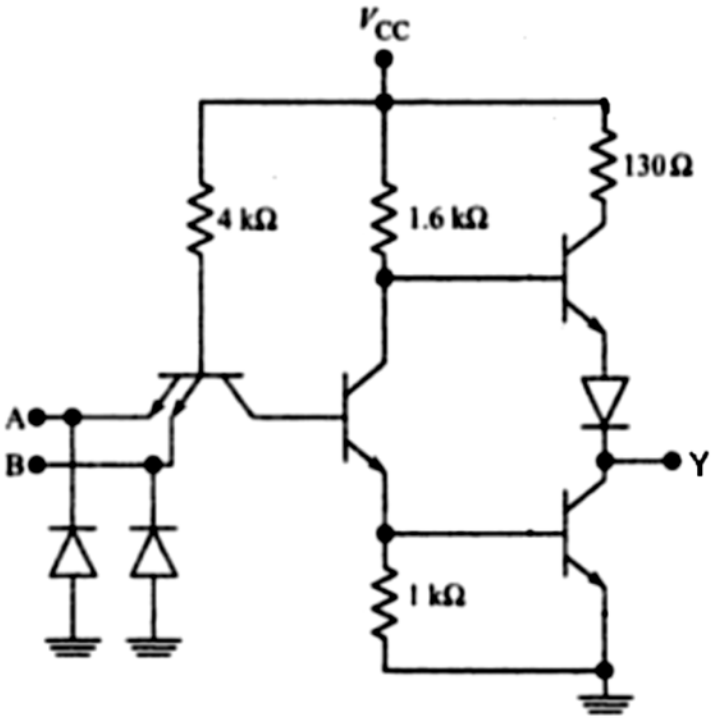




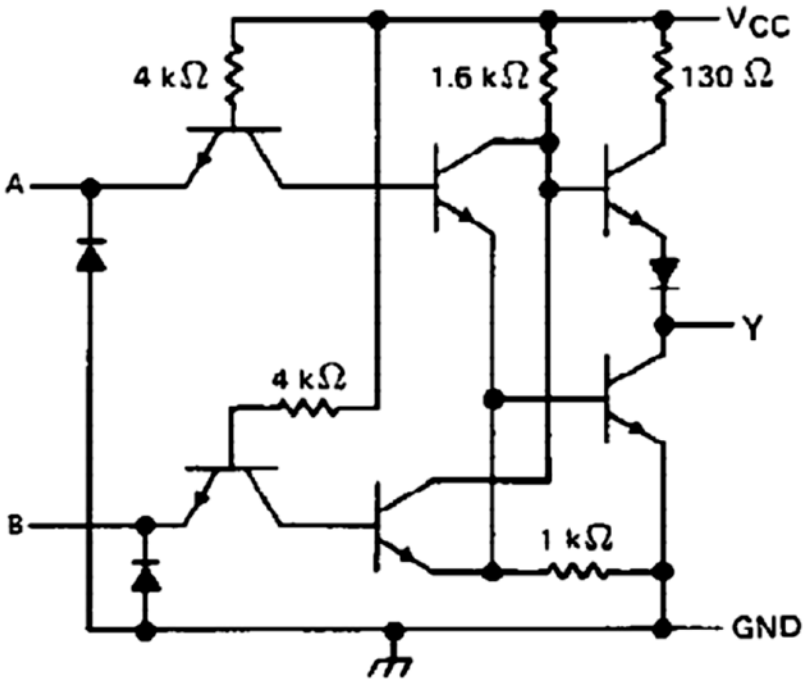




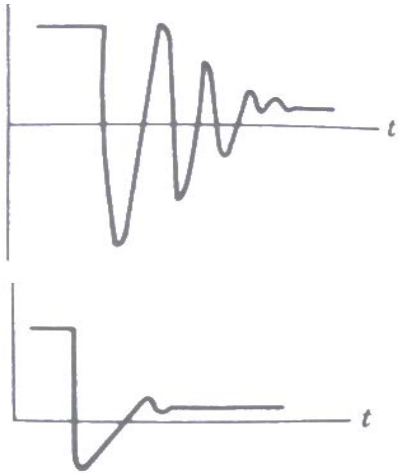
TTL Gates: NAND, NOR



2-input NAND gate



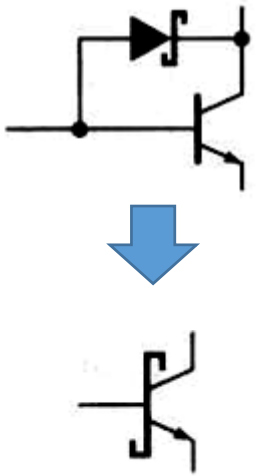
From TI SN7402 (2-input NOR) datasheet

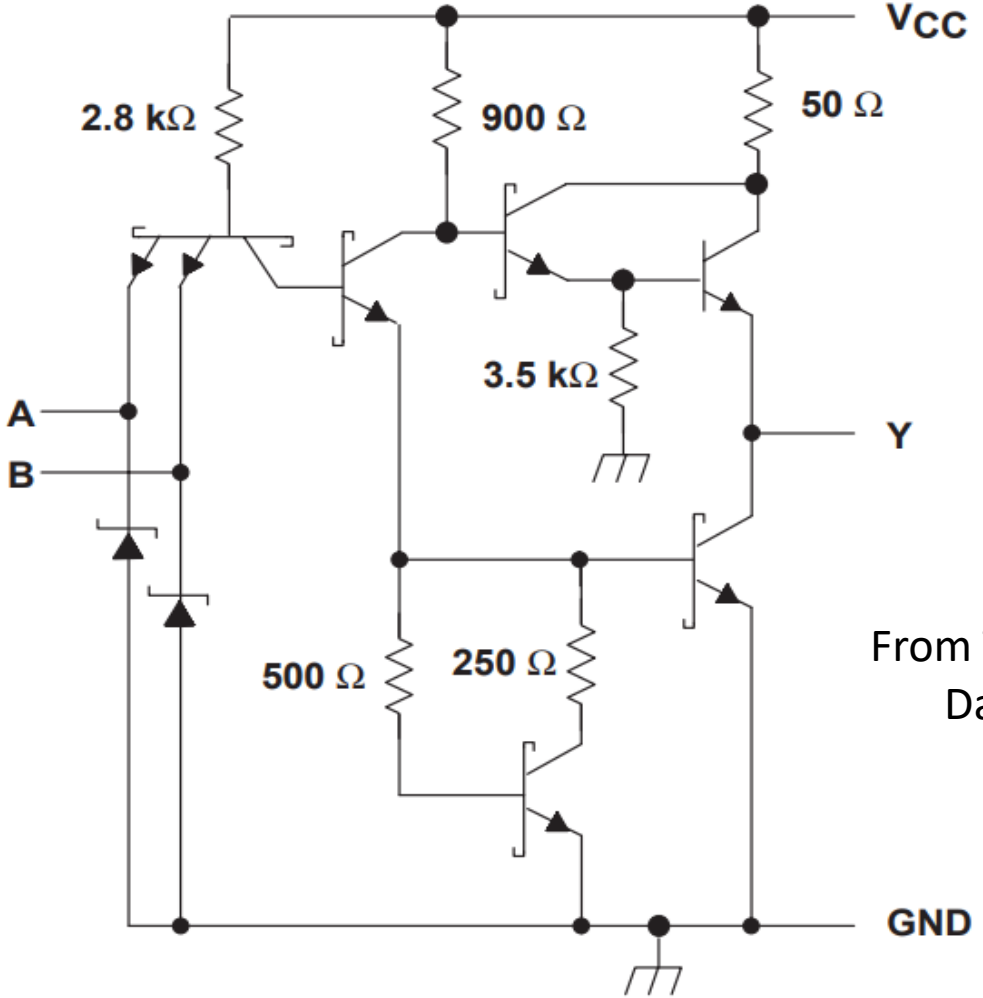


Input diodes supress ringing

Schottky TTL

Cut-in ≈ 0.35V
(range 0.2-0.5V)





Qty.	Typ.	Max.	Unit
t_{PLH}	3	4.5	ns
t_{PHL}	3	5	ns

Under test condition
R_L=280Ω, C_L=15pF

From TI SN74S00 Datasheet

References:

- Herbert Taub, and Donald Schilling, Digital Integrated Electronics, McGraw Hill
- Grinich, V.H., and H.G. Jackson, Introduction to Integrated Circuits, McGraw-Hill
- Technical documents from http://www.ti.com accessed on Oct. 08, 2018