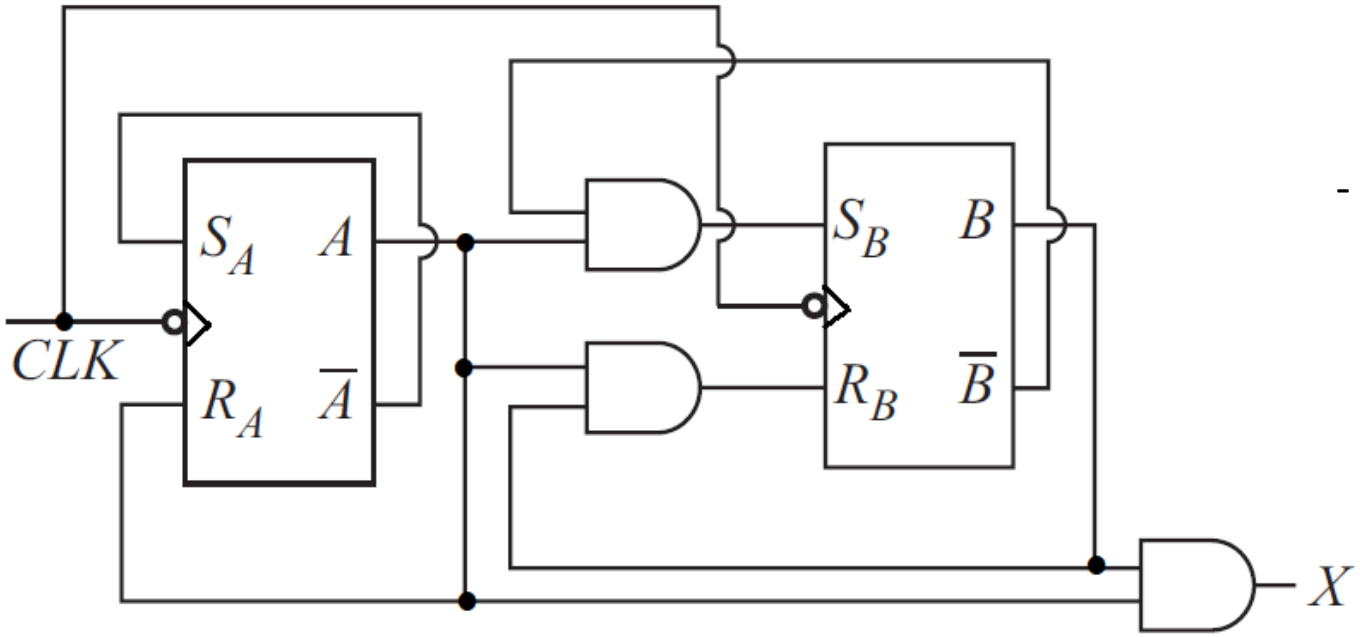
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 22

An Example

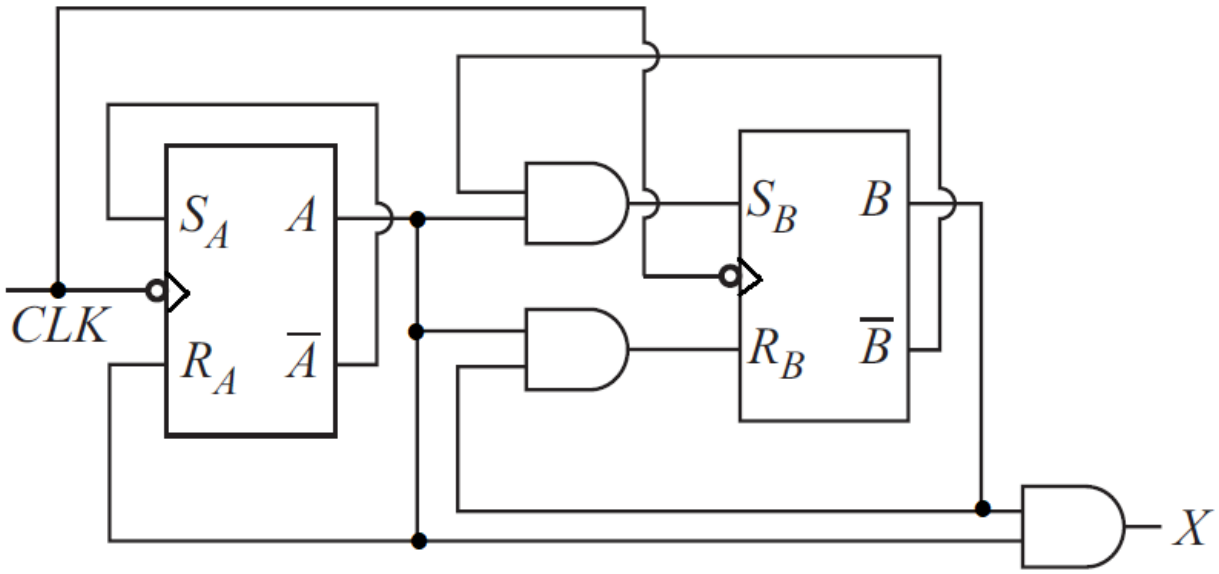
- To analyse the circuit and find how states change with the input clock and how output is generated.



Note that,

- for the basic logic gate part of the circuit, output will be considered as immediately available when input is presented and
- for the flip-flop / memory element part of the circuit, its output change as per **Truth Table / Characteristic Eqn.** waits till the clock trigger.
- Basic gate delay is negligible compared to clock time period. Effect of those delay will be considered later.

Defining Flip-Flop Inputs and Output



For Flip-Flop *A*,

$S_A = A_n'$

$R_A = A_n$

For Flip-Flop *B*,

$S_B = A_n.B_n'$

$R_B = A_n.B_n$

For Output,

$X = A_n.B_n$

State Analysis Table

	Current State		Current Flip-Flop Input				Next State		Output
CLK	B_n	A_n	S_B	R_B	S_A	R_A	B_{n+1}	A_{n+1}	X
0	0	0	0	0	1	0	0	1	0
1	0	1	1	0	0	1	1	0	0
2	1	0	0	0	1	0	1	1	0
3	1	1	0	1	0	1	0	0	1
4	0	0	0	0	1	0	0	1	0
5	0	1			…				

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	N.A.

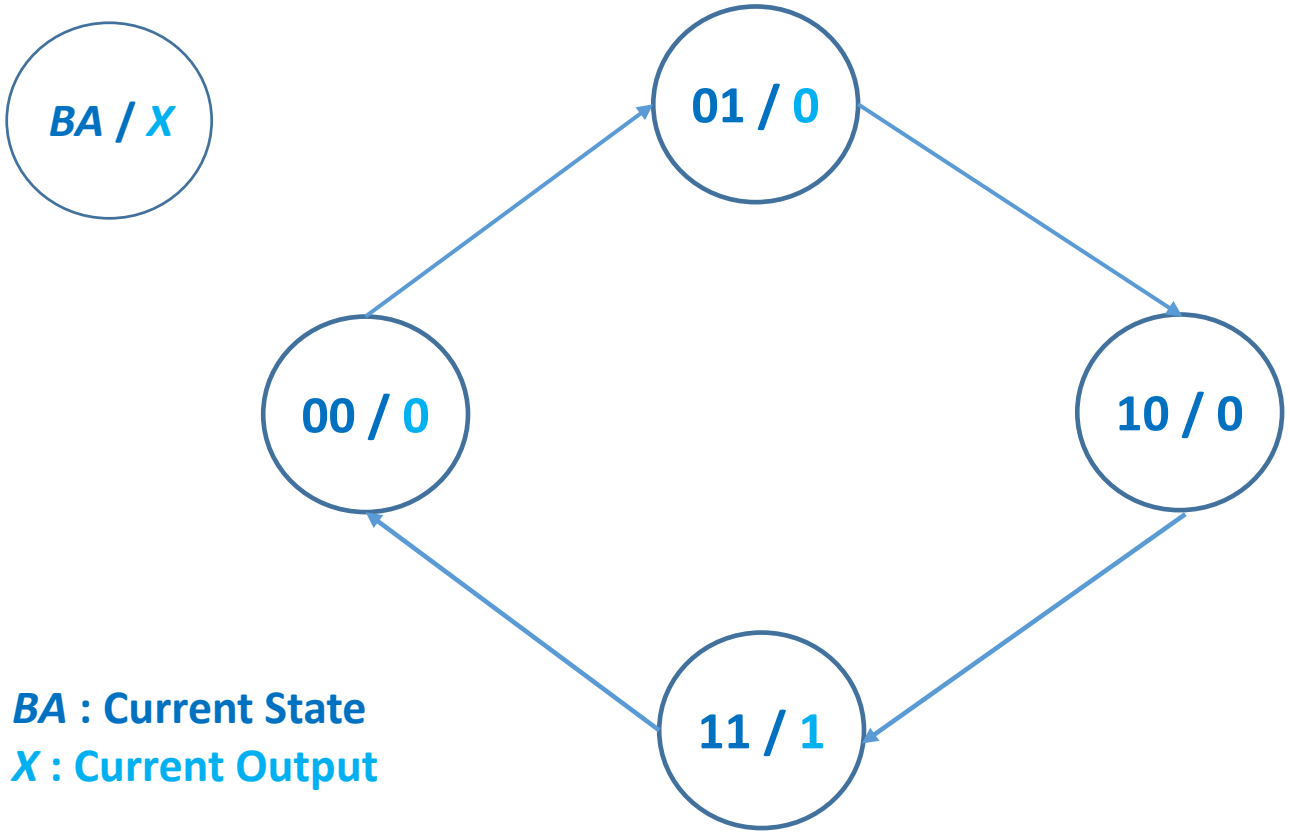
$S_A = A_n'$
$R_A = A_n$

$X = A_n.B_n$

$S_B = A_n.B_n'$
$R_B = A_n.B_n$

- Clock 0: The initial state is assumed to be 0 for each flip-flop.
- Clock *n*: Next state of clock (*n* – 1) is the present state at clock *n* and the circuit evolves.
- State transition as per Flip-Flop Truth Table for the input present.

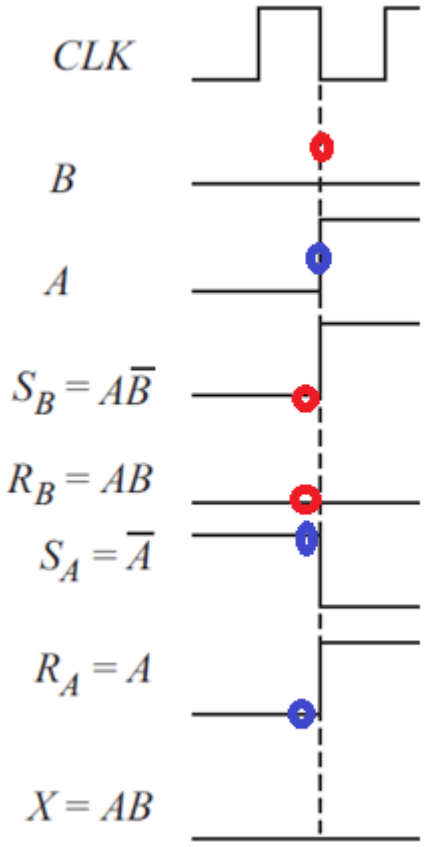
Analysis Result



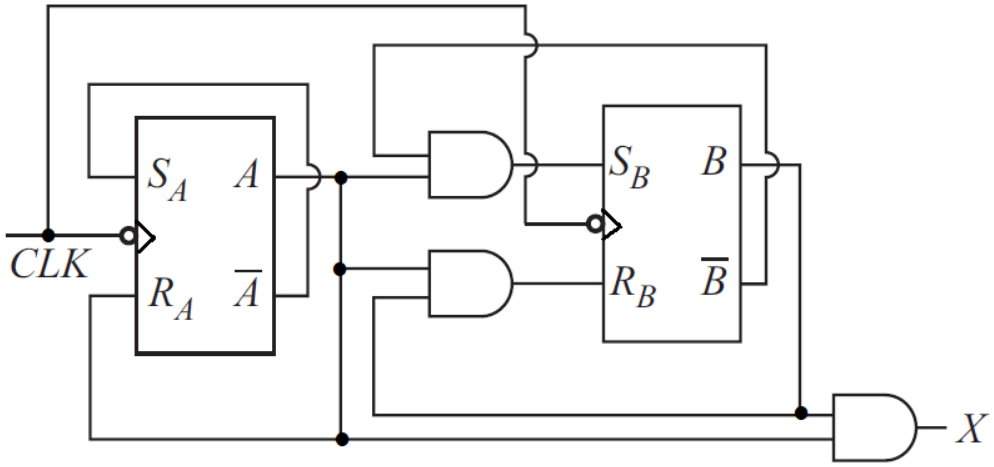
***BA* : Current State**
***X* : Current Output**

The circuit generates an **output = 1** at **every 4th clock** trigger when it reaches the state ***BA* = 11** and repeats the state transition
00 → 01 → 10 → 11 → 00 → …

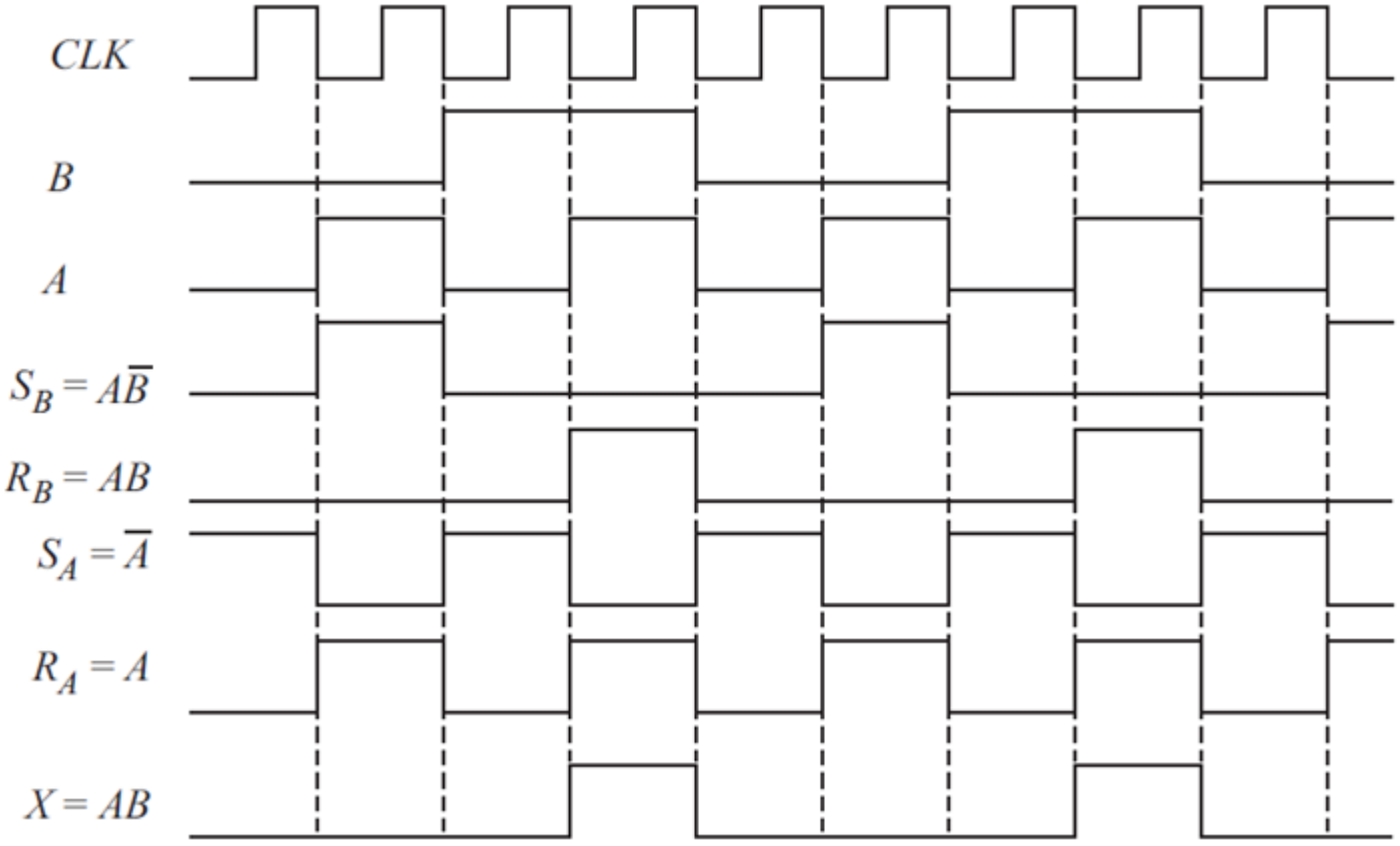
Using Timing Diagram

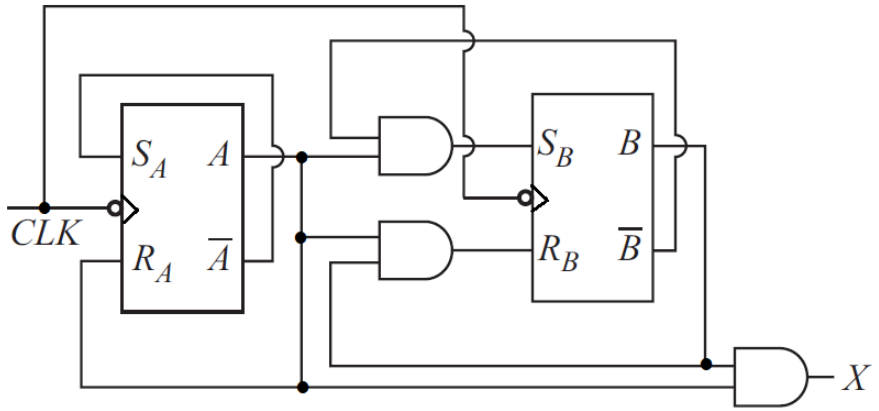


- Starting with initial 00 state, progress with time where Flip-Flop can change state only at –ve edge of the clock.
- Timing diagram can show the effect of delay in various elements and any deviation in performance due to propagation delay.



Using Timing Diagram





Using Characteristic Equation

SR Flip-Flop Characteristic Eqn.: $Q_{n+1} = S + R'.Q_n$

$S_A = A_n'$
$R_A = A_n$

$A_{n+1} = S_A + R_A'.A_n$

Substituting,
$A_{n+1} = A_n' + A_n'.A_n$
$= A_n'$

$S_B = A_n.B_n'$
$R_B = A_n.B_n$

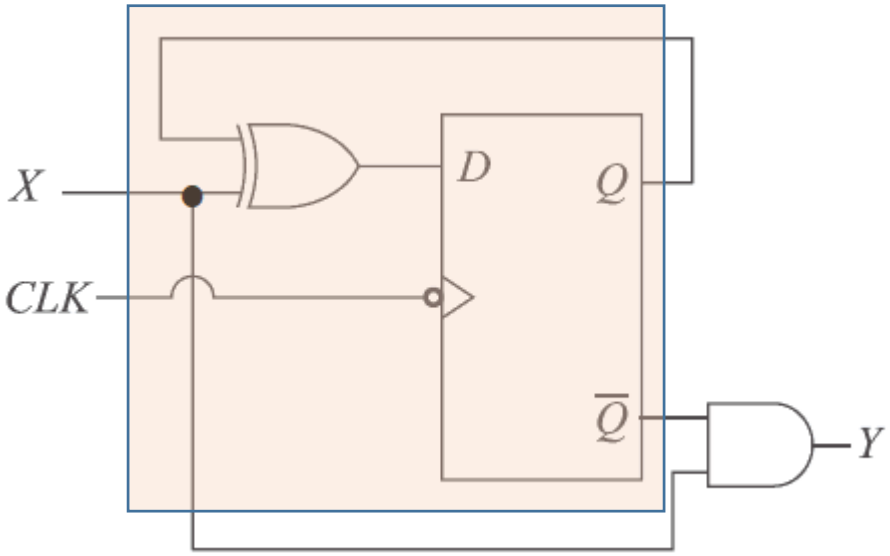
$B_{n+1} = S_B + R_B'.B_n$

Substituting,
$B_{n+1} = A_n.B_n' + (A_n.B_n)'.B_n$
$= A_n.B_n' + (A_n' + B_n)'.B_n$
$= A_n.B_n' + A_n'.B_n + B_n'.B_n$
$= A_n.B_n' + A_n'.B_n$
$= A_n \oplus B_n$

CLK	B_n	A_n	B_{n+1}	A_{n+1}	X
0	0	0	0	1	0
1	0	1	1	0	0
2	1	0	1	1	0
3	1	1	0	0	1
4	0	0	0	1	0
5	0	1		…	

$X = A_n.B_n$

Another Example



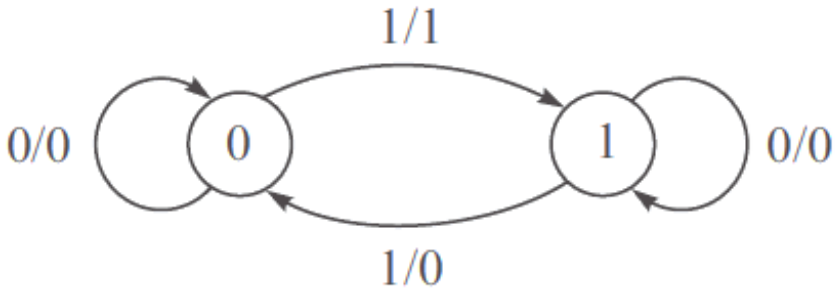
Q_n	X	D	Q_{n+1}	Y
0	0	0	0	0
0	1	1	1	1
1	0	1	1	0
1	1	0	0	0

T Flip-Flop

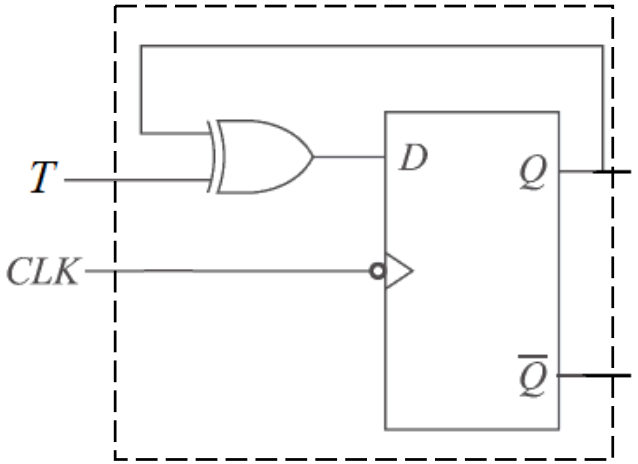
State toggles when input is 1, else maintains previous state. Output is 1 when input received at State 0 is 1, else output is 0.

$D = X \oplus Q_n$

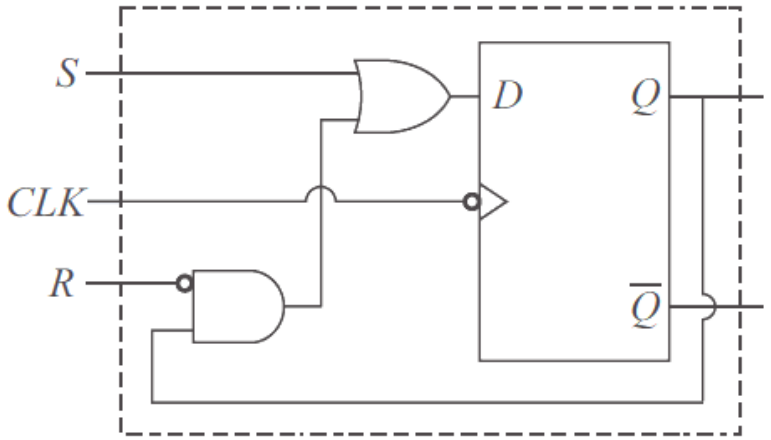
$Y = X.Q_n'$



D to other Flip-Flops



$Q_{n+1} = D$



$Q_{n+1} = T.Q_n' + T'.Q_n$

$D = T.Q_n' + T'.Q_n$

$Q_{n+1} = J.Q_n' + K'.Q_n$

$D = J.Q_n' + K'.Q_n$

$Q_{n+1} = S + R'.Q_n$

$D = S + R'.Q_n$

SR, JK Flip-Flops to D Flip-Flop

$Q_{n+1} = S + R'.Q_n$

Consider,

$S = D$

$R = D'$

Then,

$Q_{n+1} = D + (D')'.Q_n$

$= D + D.Q_n$

$= D.(1 + Q_n)$

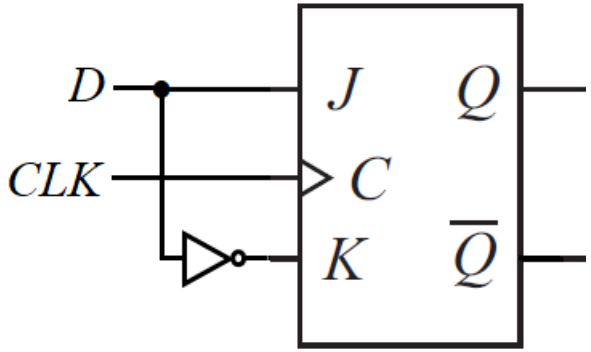
$= D.1 = D$

$Q_{n+1} = J.Q_n' + K'.Q_n$

Consider,

$J = D$

$K = D'$



Then,

$Q_{n+1} = D.Q_n' + (D')'.Q_n$

$= D.Q_n' + D.Q_n$

$= D.(.Q_n' + Q_n)$

$= D.1 = D$

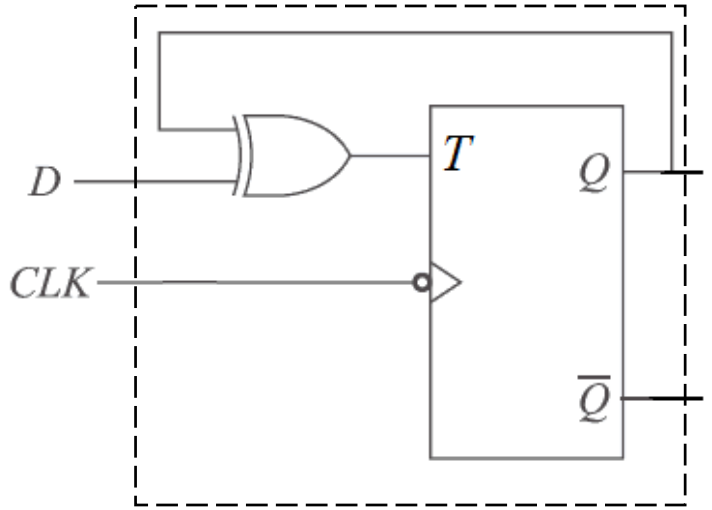
$Q_{n+1} = T.Q_n' + T'.Q_n$

?

D Flip-Flop from *T* Flip-Flop

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Q_n \ D	0	1
0	0	1
1	1	0



$$T = D.Q_n' + D'.Q_n$$

Truth Table

Excitation Table

$$\begin{aligned} Q_{n+1} &= T.Q_n' + T'.Q_n \\ &= (D.Q_n' + D'.Q_n).Q_n' + (D.Q_n' + D'.Q_n)'.Q_n \\ &= D.Q_n' + (D'.Q_n' + D.Q_n).Q_n \\ &= D.Q_n' + D.Q_n = D \end{aligned}$$

Conversion: *SR* and *JK*

- *JK* Flip-Flop can directly replace *SR* Flip-Flop as the Truth Table differs only for 11 input which is avoided in a circuit that uses *SR* Flip-Flop.

J_n	K_n	Q_n	Q_{n+1}	S_n	R_n
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

To obtain *JK* Flip-Flop from *SR* Flip-Flop

Conversion: *SR* and *JK*

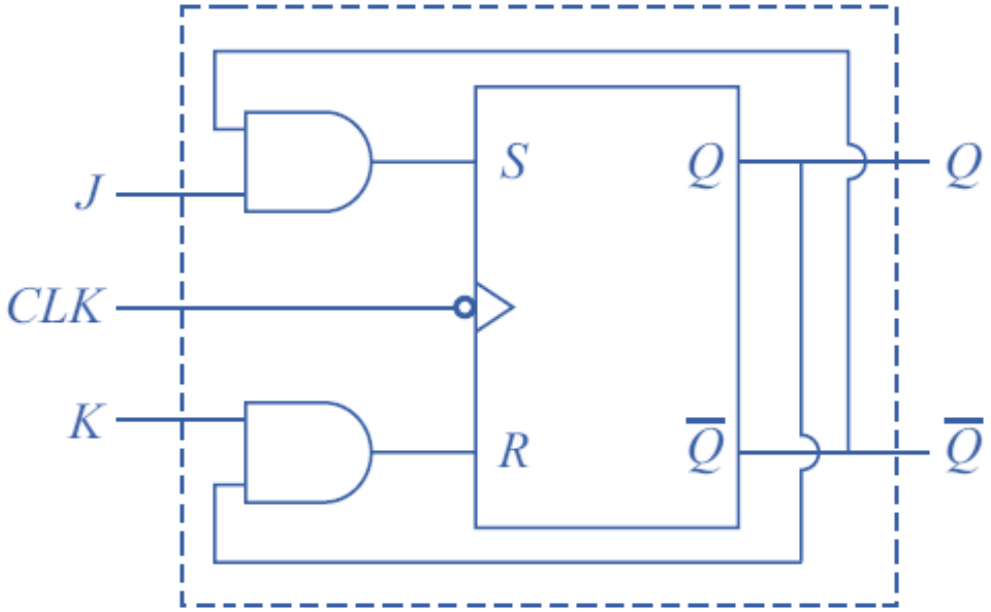
J_n	K_n	Q_n	Q_{n+1}	S_n	R_n
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

Q_n \ $J_n K_n$	0 0	0 1	1 1	1 0
0	0	0	1	1
1	×	0	0	×

$$S_n = J_n \overline{Q}_n$$

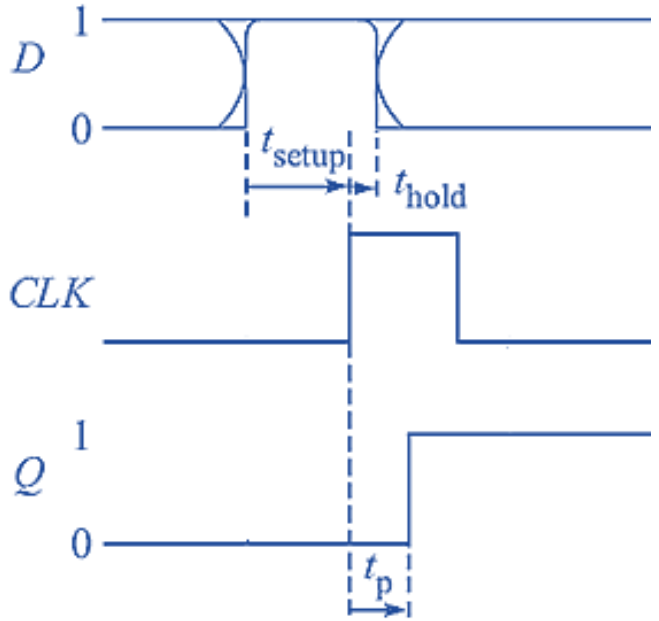
Q_n \ $J_n K_n$	0 0	0 1	1 1	1 0
0	×	×	0	0
1	0	1	1	0

$$R_n = K_n Q_n$$



Flip-Flop Timing Parameters

Setup time: Minimum amount of time data must be present before clock trigger arrives.
Hold time: Minimum amount of time data must be held after clock trigger.
Propagation delay: Time taken for the output to change after clock trigger in response to the input.



Parameter	74LS74A (V_{CC}=5V)	74HC74 (V_{CC}=4.5V)
t_{setup} (Data)^	20	25
t_{hold} ^	5	≈ 0
t_p (CLK to Q)#	25/40*	44
f_{max} $	33	50
	TTL	CMOS

^:minimum time in ns
#:maximum time in ns

*:L to H / H to L
$:typical in MHz

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill