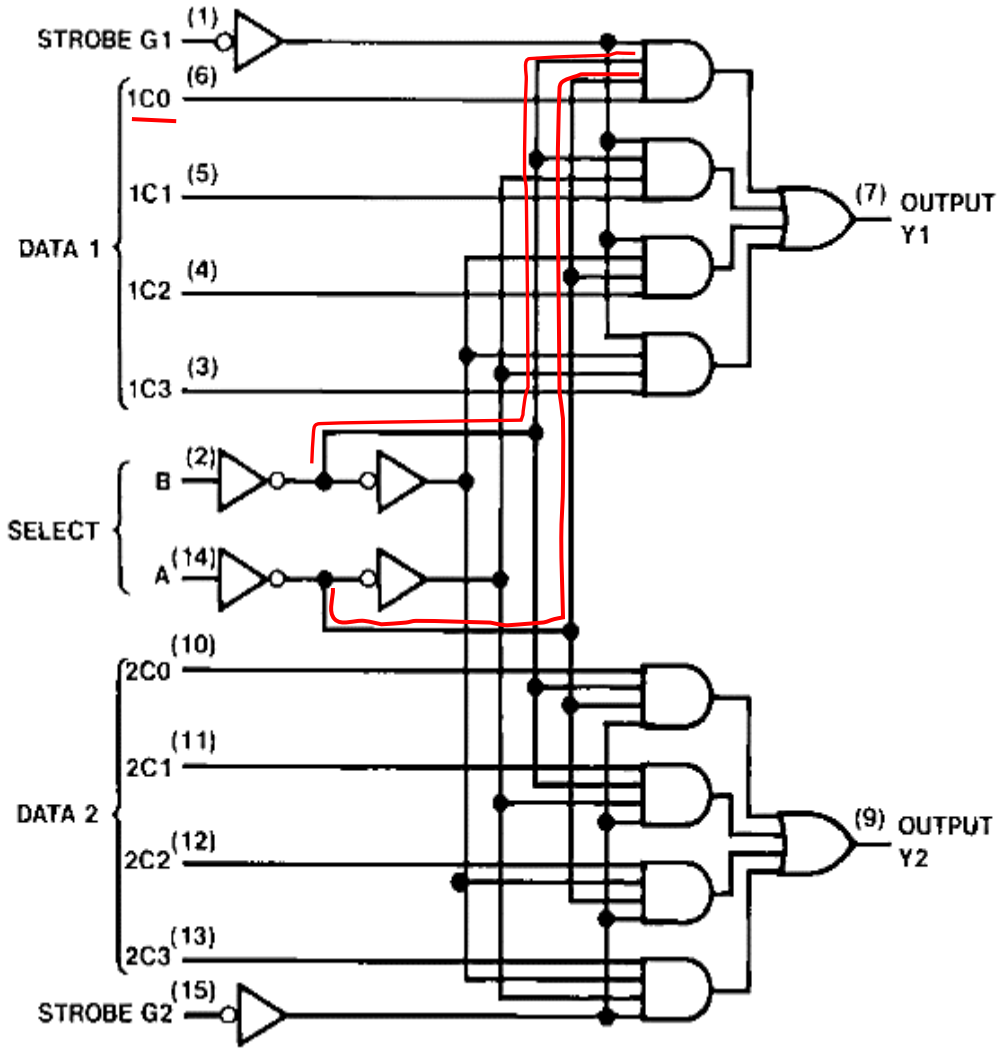
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 11

MUX: non-inverted output

IC 74153

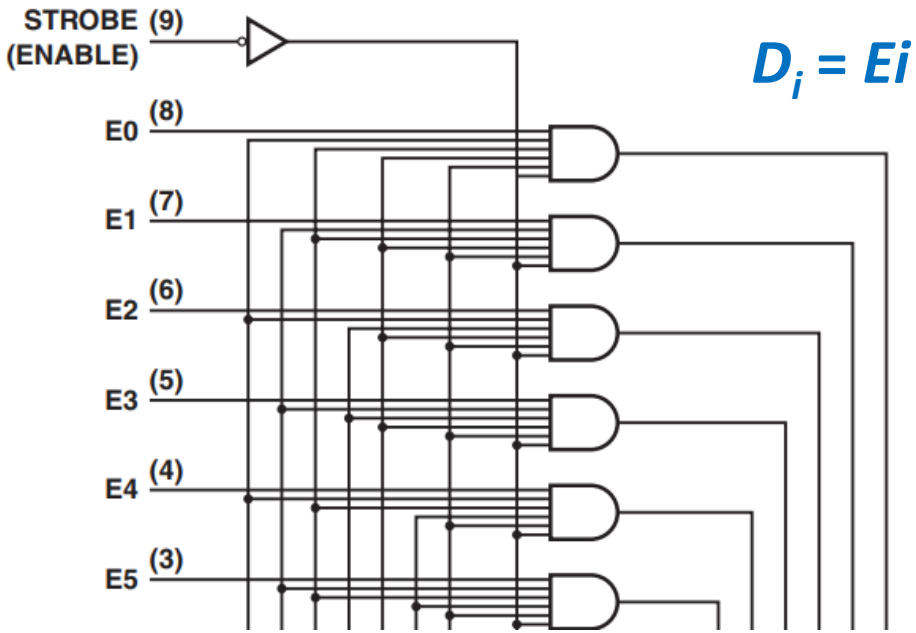
$Y = E'.[(B'.A').C0 + (B'.A).C1 + (B.A').C2 + (B.A).C3]$



STROBE (G)	B	A	Y
H	X	X	L
L	L	L	C0
L	L	H	C1
L	H	L	C2
L	H	H	C3

MUX: inverted output (IC 74150)

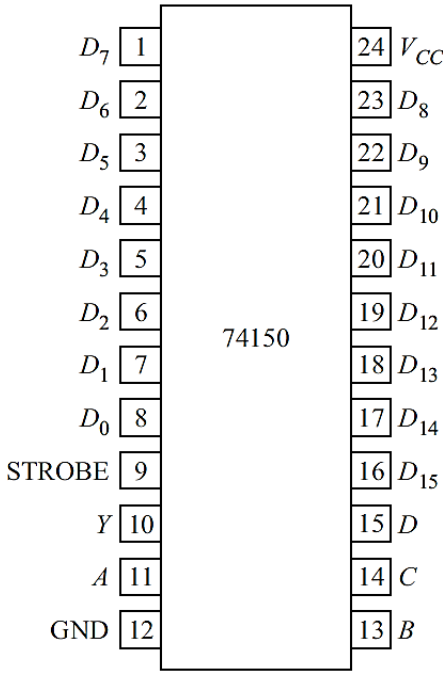
INPUTS					OUTPUT
SELECT				STROBE	W
A	B	C	D	$\overline{G}$	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

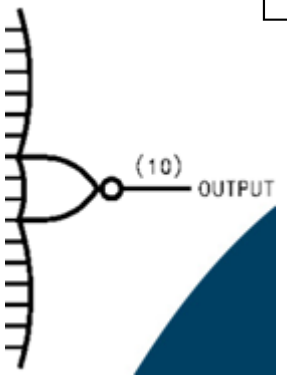


$D_i = Ei$

Control inputs

$Y = (E'.A'B'C'D'.D_0 + E'.A'B'C'D.D_1 + \ldots$
$\ldots. + E'.ABCD'.D_{14} + E'.ABCD.D_{15})'$





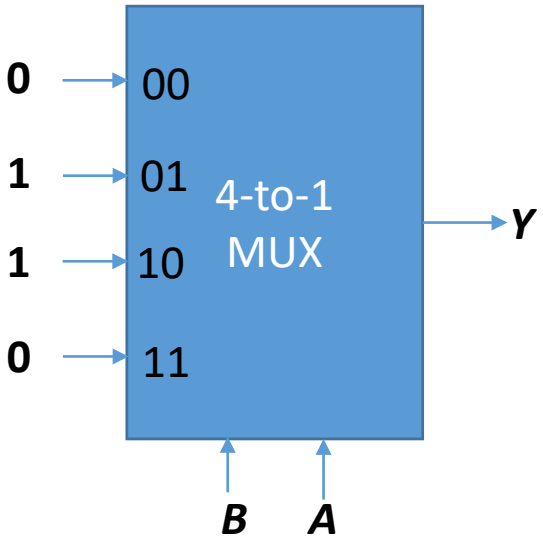
IC 74153

$Y = E'.[(B'.A').C0 + (B'.A).C1 + (B.A').C2 + (B.A).C3]$

	B	A	Y
F(0,0)	L	L	0
F(0,1)	L	H	1
F(1,0)	H	L	1
F(1,1)	H	H	0

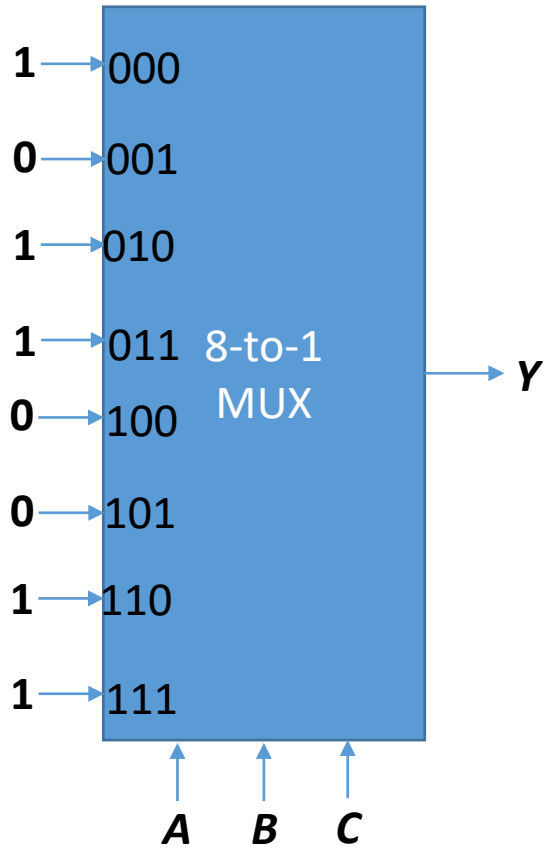
$Y = B'.A + B.A'$

$Y = (B'.A').0 + (B'.A).1 + (B.A').1 + (B.A).0$



½ IC 74153, $E = 0$

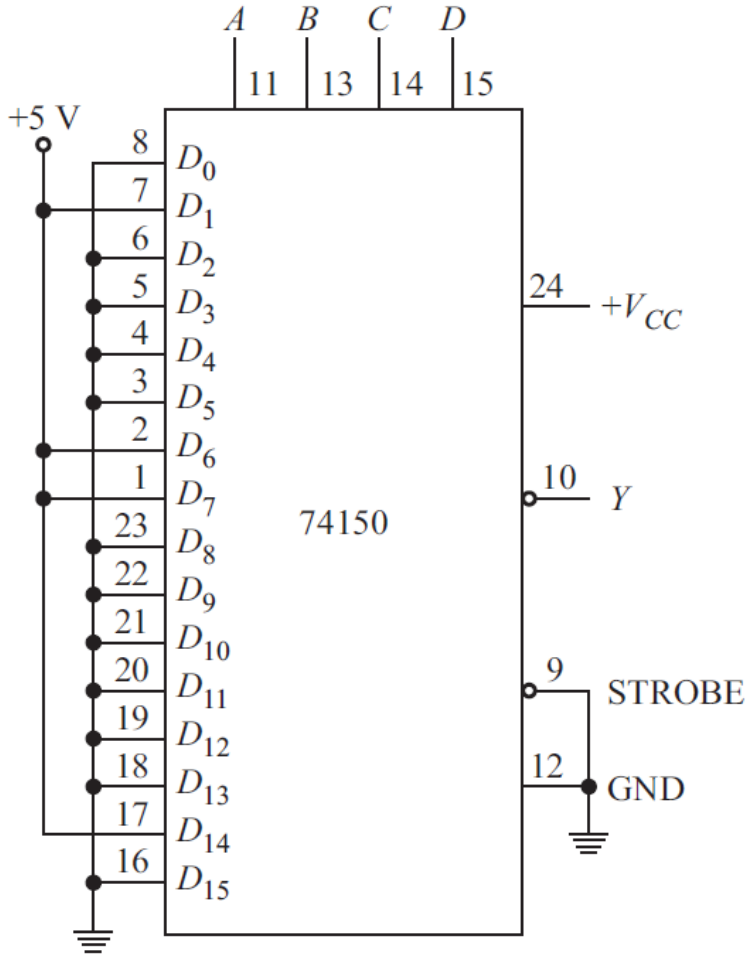
$Y = F(A,B,C)$
$= \sum m (0,2,3,6,7)$



IC 74151
8-to-1 MUX
with STROBE (EN'),
both non-inverted and inverted output

Multiplexer as Universal Logic Circuit

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



$Y = (E'.A'B'C'D'.D_0 + E'.A'B'C'D.D_1 + \ldots$
$\ldots + E'.ABCD'.D_{14} + E'.ABCD.D_{15})'$

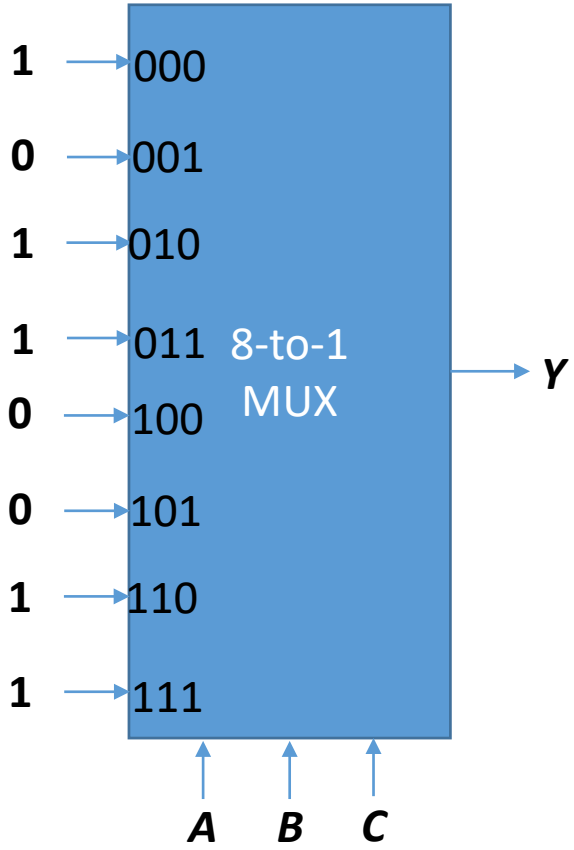
$E = 0,$

$Y' = A'B'C'D'.D_0 + A'B'C'D.D_1 + \ldots$
$\ldots + ABCD'.D_{14} + ABCD.D_{15}$

$Y = F(A,B,C,D)$
$= \sum m\,(0,2,3,4,5,8,9,$
$10,11,12,13,15)$

$Y' = \sum m(1,6,7,14)$

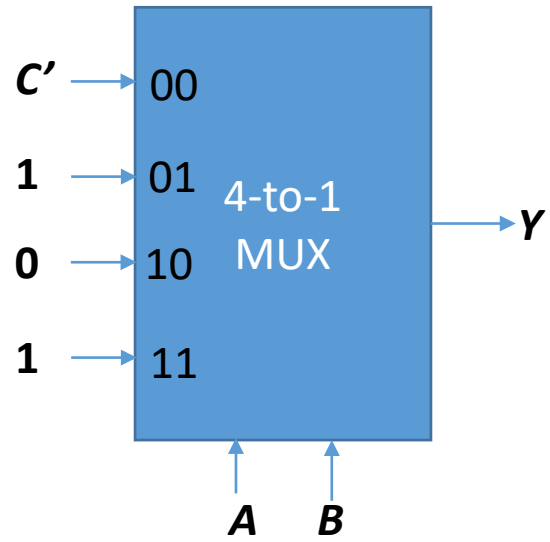
Entered Variable and Multiplexer



	A	B	C	Y
Y=C’	0	0	0	1
	0	0	1	0
Y=1	0	1	0	1
	0	1	1	1
Y=0	1	0	0	0
	1	0	1	0
Y=1	1	1	0	1
	1	1	1	1

A	B	Y
0	0	C’
0	1	1
1	0	0
1	1	1

$Y = F(A,B,C)$
$= \sum m\,(0,2,3,6,7)$

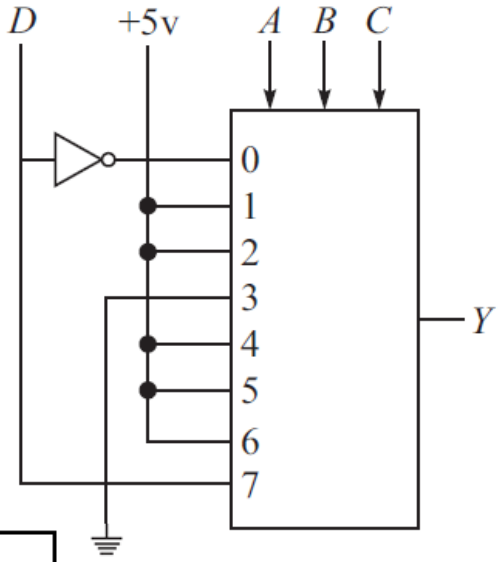


½ IC 74153, $E = 0$

8-to-1 MUX and 4-variable function

$Y = F(A,B,C,D)$
$= \sum m\,(0,2,3,4,5,8,9,10,11,12,13,15)$

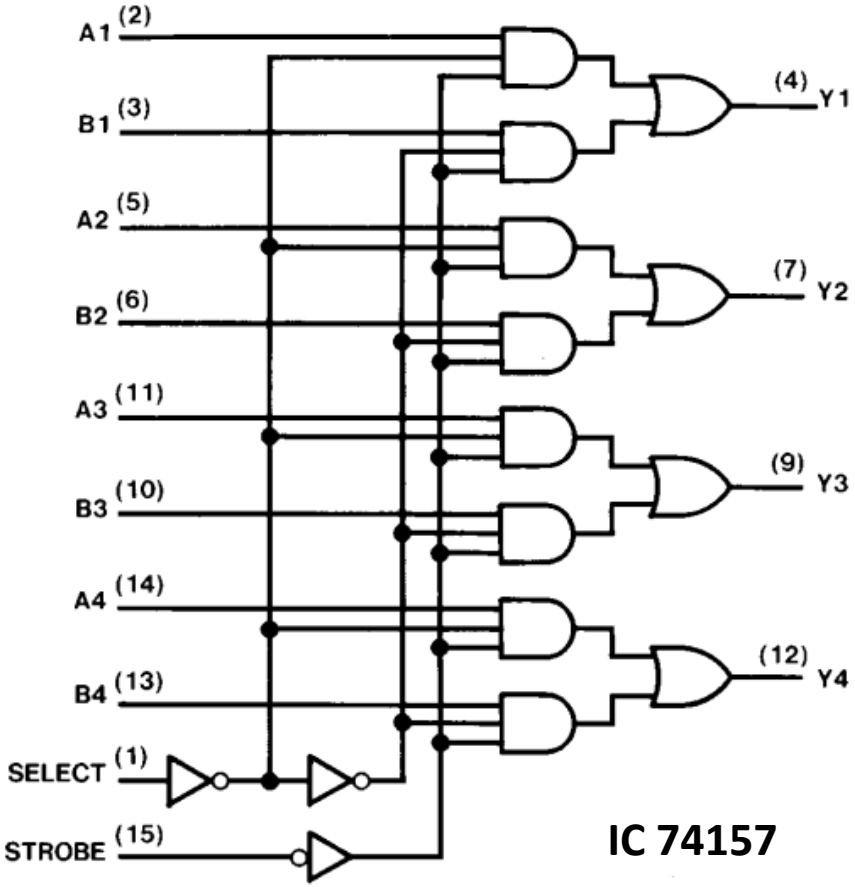
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1



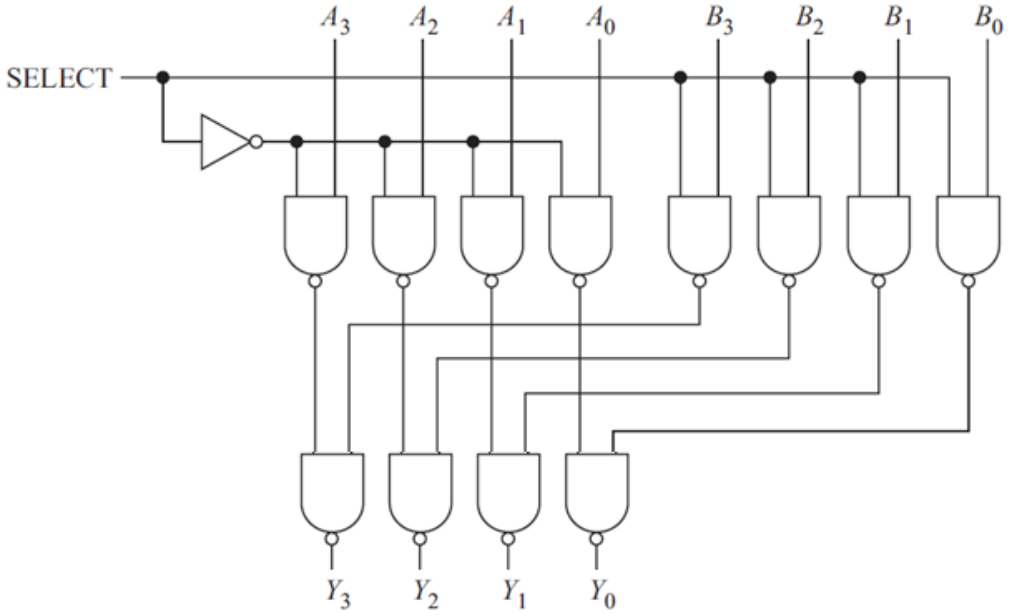
IC 74151
EN = 0

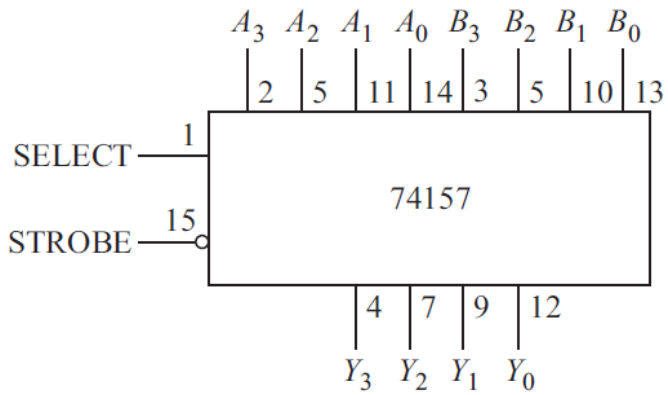
ABC	000	001	010	011	100	101	110	111
$D = 0$	1	1	1	0	1	1	1	0
$D = 1$	0	1	1	0	1	1	1	1
Y	D'	1	1	0	1	1	1	D
8-to-1 MUX data input	$D_0 = D'$	$D_1 = 1$	$D_2 = 1$	$D_3 = 0$	$D_4 = 1$	$D_5 = 1$	$D_6 = 1$	$D_7 = D$

Nibble Multiplexer

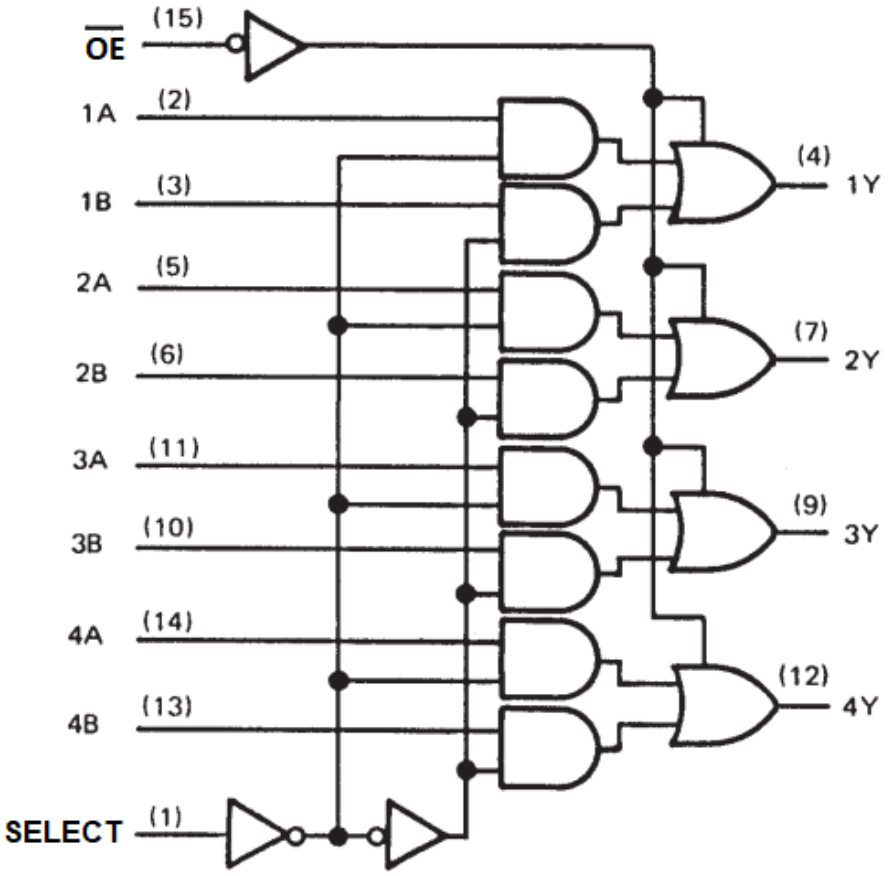


IC 74157





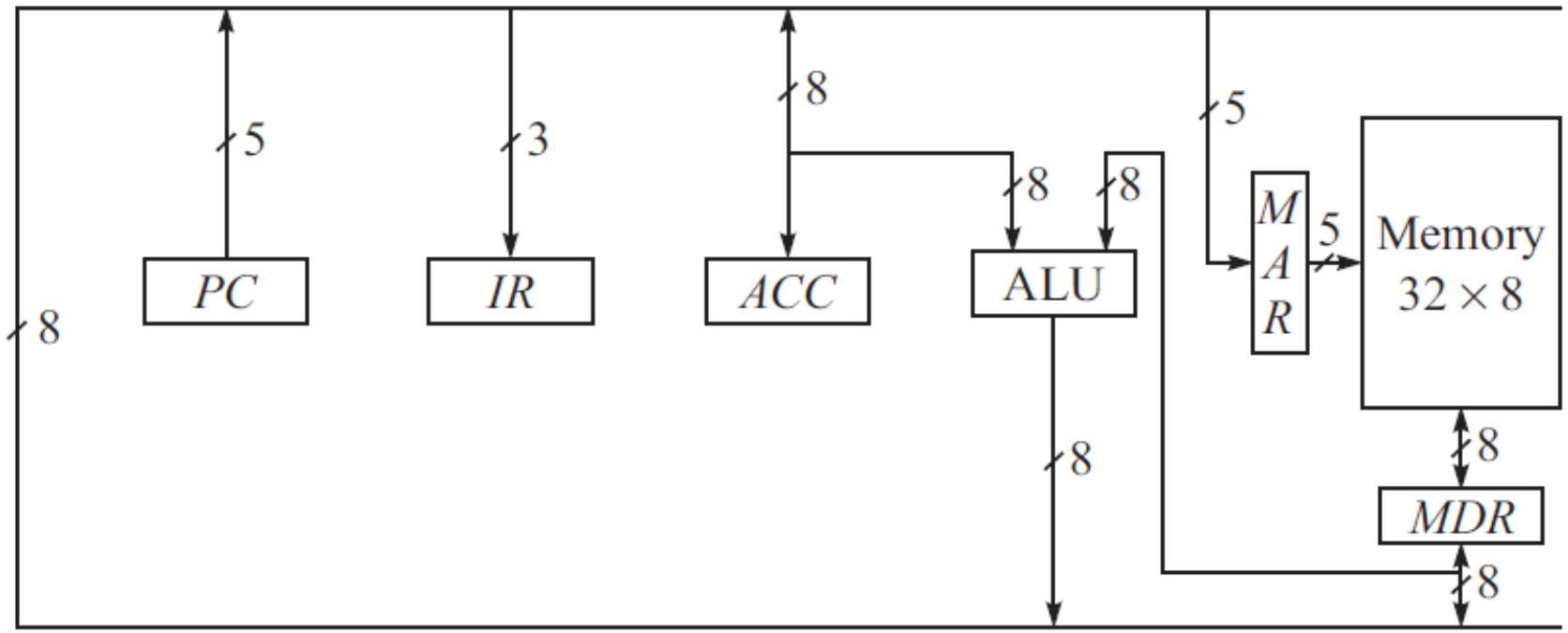
Nibble Multiplexer with Tristated Output



OE’	SELECT	Y
H	X	High Z
L	L	A
L	H	B

IC 74257

BUS Architecture and Tristated Output



An Example

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill\
- Technical documents from http://www.ti.com accessed on Oct. 08, 2018