Digital Electronic Circuits
Section 1 (EE, IE)

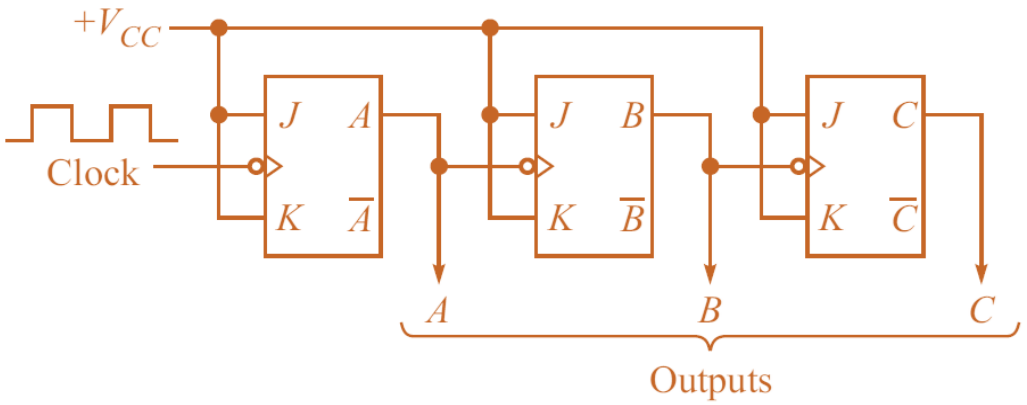
Lecture 25

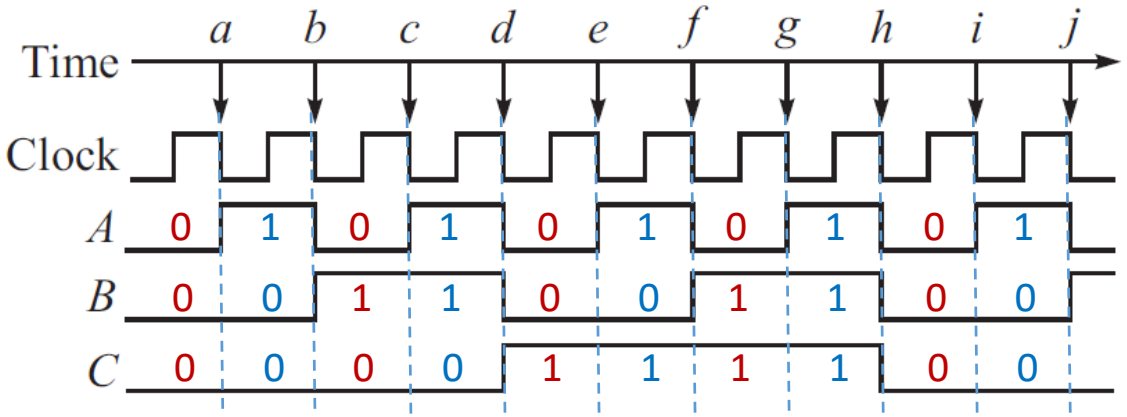
Counter Basics

- A counter keeps a record of the number of times a particular event has occurred by advancing its state.
- In counter, a unique state of the digital circuit is associated with a particular count.
- With every trigger, the state advancement can be
  - in any random order
  - a sequential increase (up counter)
  - a sequential decrease from a pre-defined value (down counter)
- All the flip-flops defining the state of the count get the trigger:
  - simultaneously in synchronous counter
  - at different point of time in asynchronous counter
- A modulo-*n* or mod-*n* counter has *n* different states. It returns to initial value after *n* triggers. For *m* flip-flops used in counter design, $2^m \geq n$.
- Usually, clock is given as input trigger. Mod-*n* counter is also called divided-by-*n* counter.

Asynchronous Up Counter

Also, called
Ripple Counter

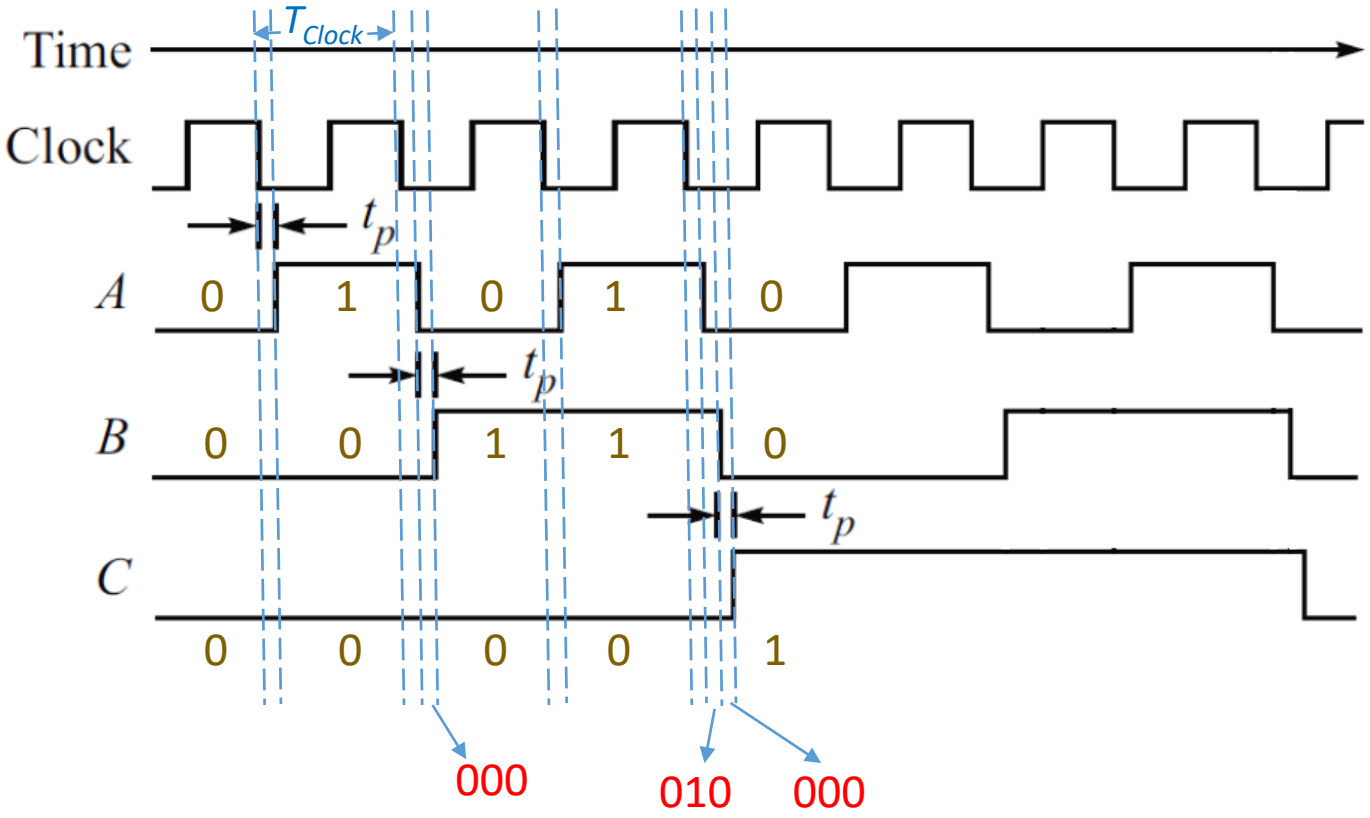


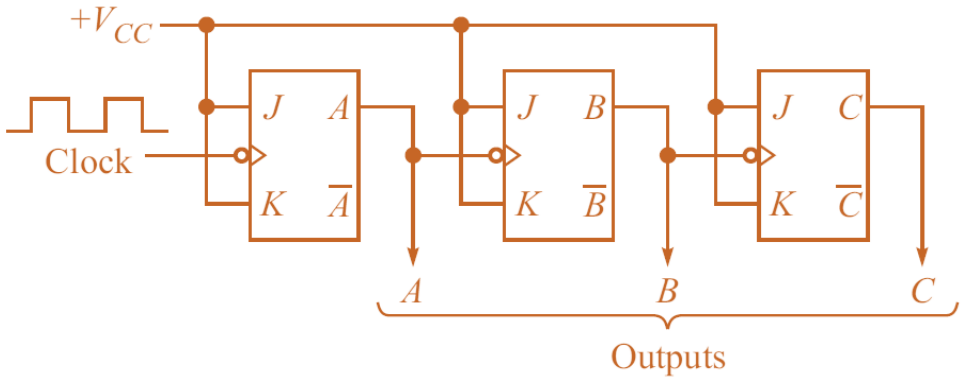


CLK↓	C	B	A	Count
-	0	0	0	0
a	0	0	1	1
b	0	1	0	2
c	0	1	1	3
d	1	0	0	4
e	1	0	1	5
f	1	1	0	6
g	1	1	1	7
h	0	0	0	0

- $f_A = f_{Clock} / 2$
- $f_B = f_{Clock} / 4$
- $f_C = f_{Clock} / 8$

Cumulative Delay

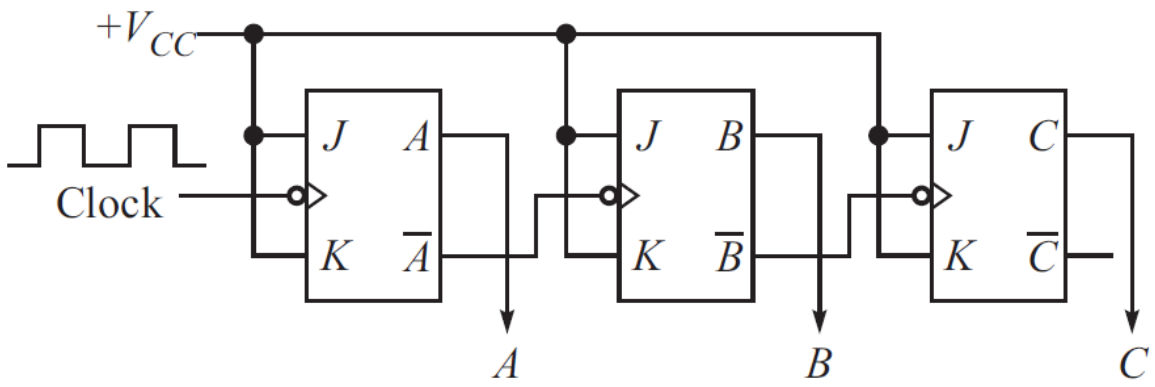


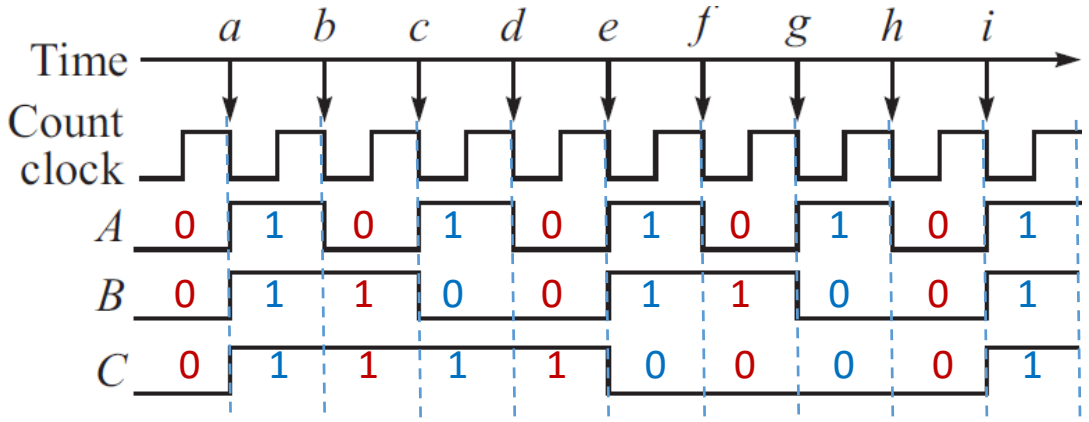


For n flip-flops, the delay is $n\tau$ where τ is propagation delay of each flip-flop.

- No miss till $n\tau < T_{clock}$
- Glitch

Asynchronous Down Counter



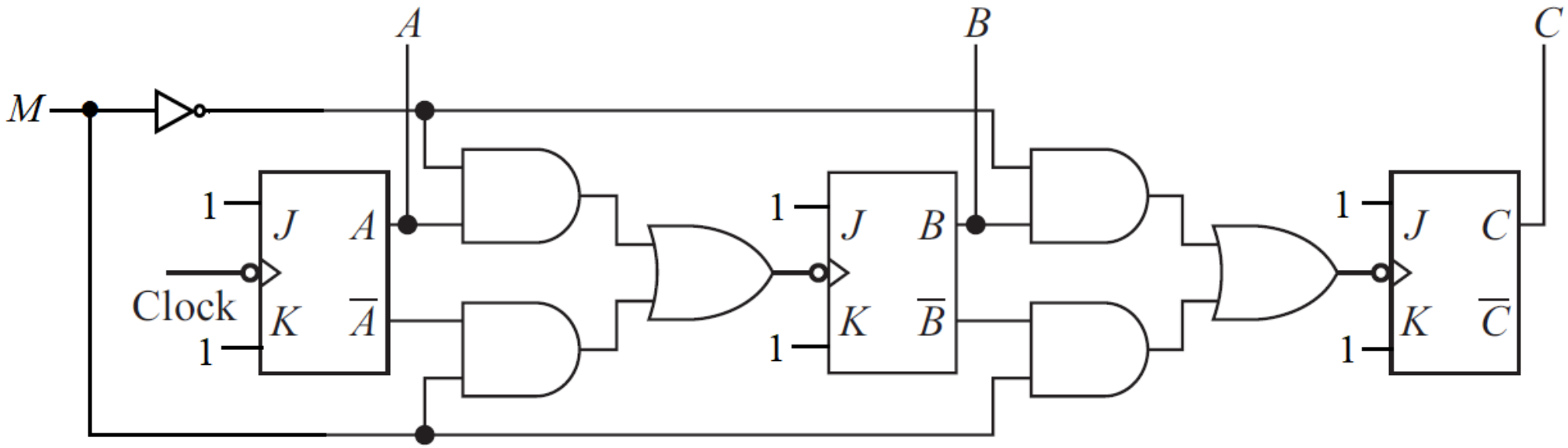


CLK↓	C	B	A	Count
-	0	0	0	0
a	1	1	1	7
b	1	1	0	6
c	1	0	1	5
d	1	0	0	4
e	0	1	1	3
f	0	1	0	2
g	0	0	1	1
h	0	0	0	0

Here, if output as *C'B'A'*, then up counter

Similarly, previous up counter circuit gives down count at its inverted outputs.

Asynchronous Up – Down Counter



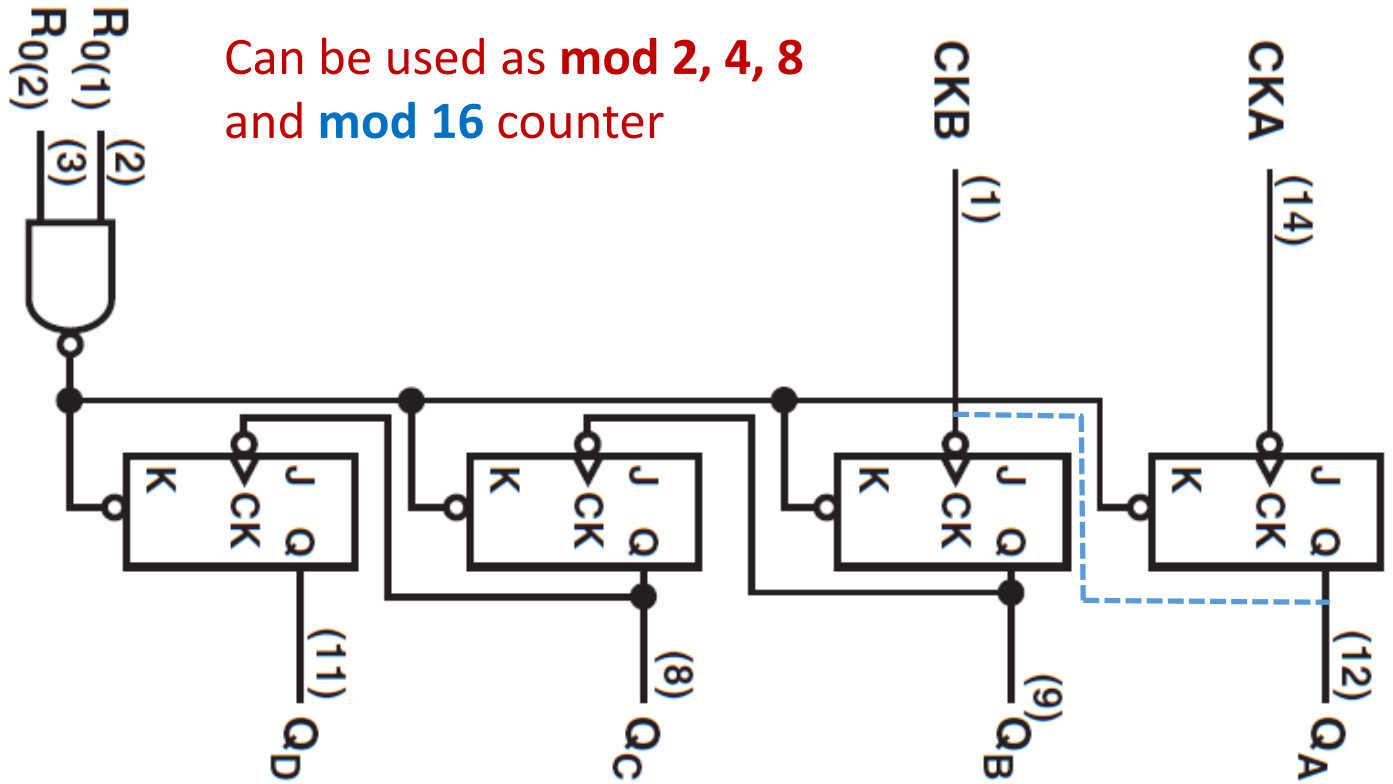
Mode, M = 0: Up counter

M = 1: Down counter

IC 7493

4-bit Asynchronous Binary Up Counter

Can be used as **mod 2, 4, 8** and **mod 16** counter



RESET/COUNT

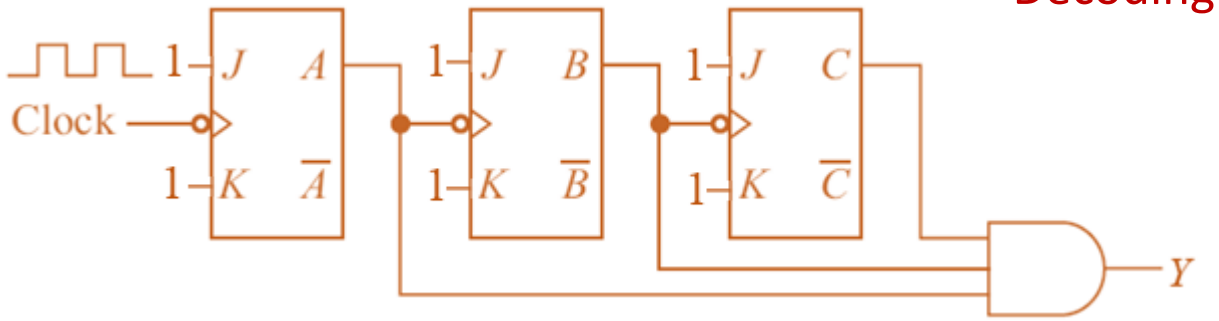
RESET INPUTS		OUTPUTS			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

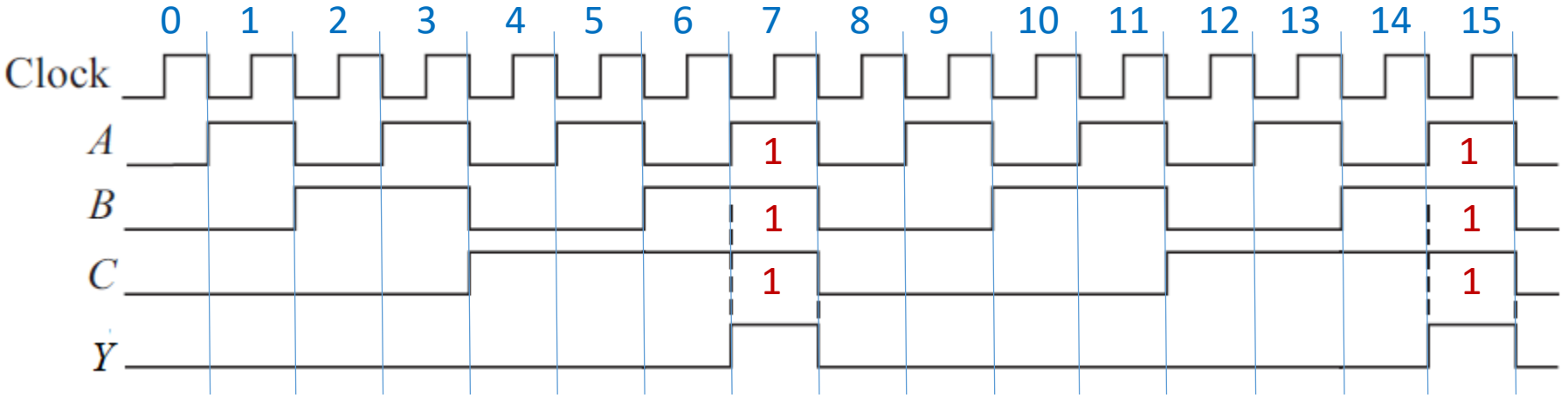
Mod 8: CKA unused, CKB triggered

External connection (Q_A to CKB) when used as mod 16 and CKA triggered.

Decoding Counter State

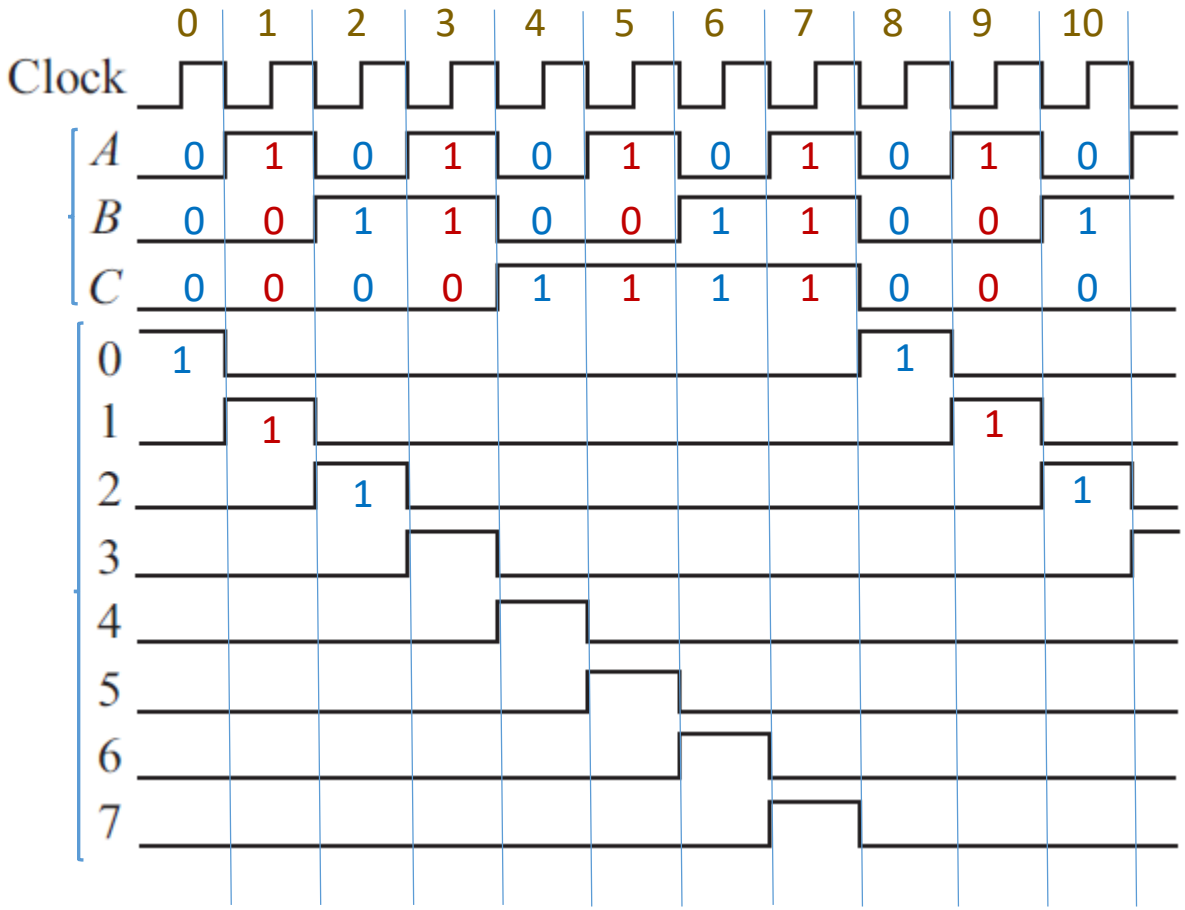
Decoding 111

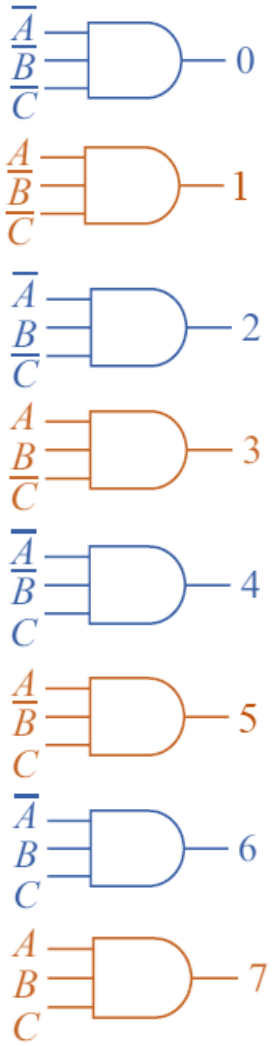


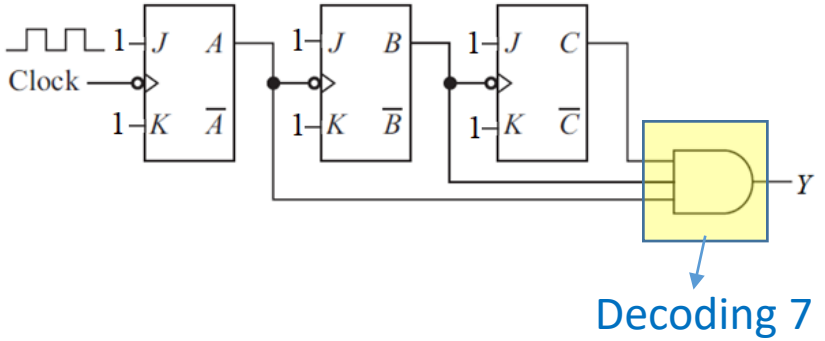


Once in every 8 clock cycles, *Y* = 1 for 1 clock cycle whenever the state of the counter, *CBA* = 111

Decoding Logic



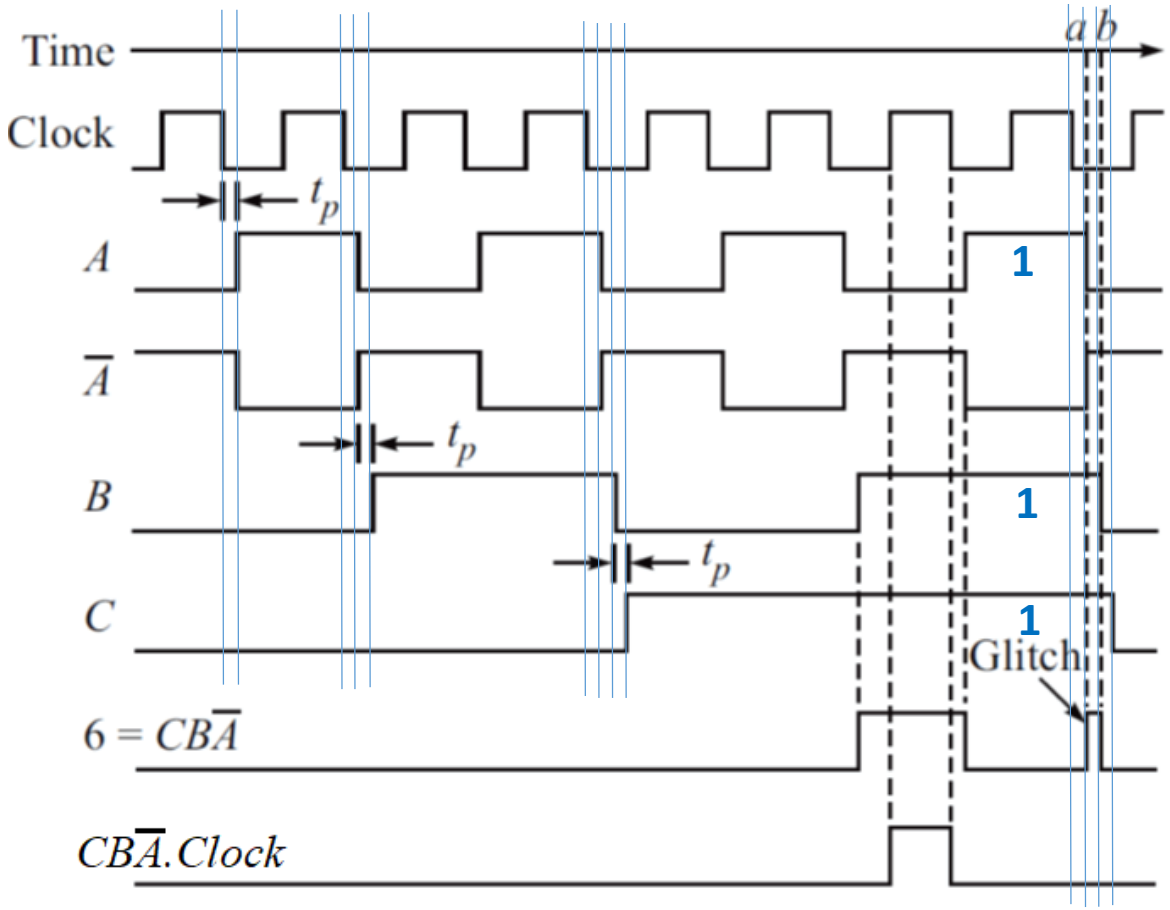


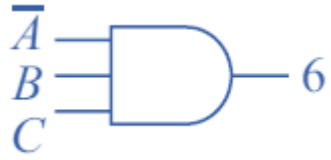


A decoding gate connected to the outputs of a counter is activated **only when the counter content is equal to a given state**.

Mod-16 Counter:
4-input logic gate
for decoding

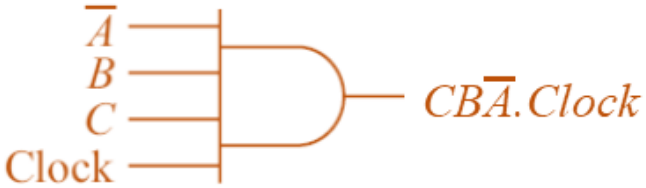
Glitch and Strobed Decoding Gate





111→000

111→(110)→(100)→**000**



Strobed gate

Glitch between *a* and *b*

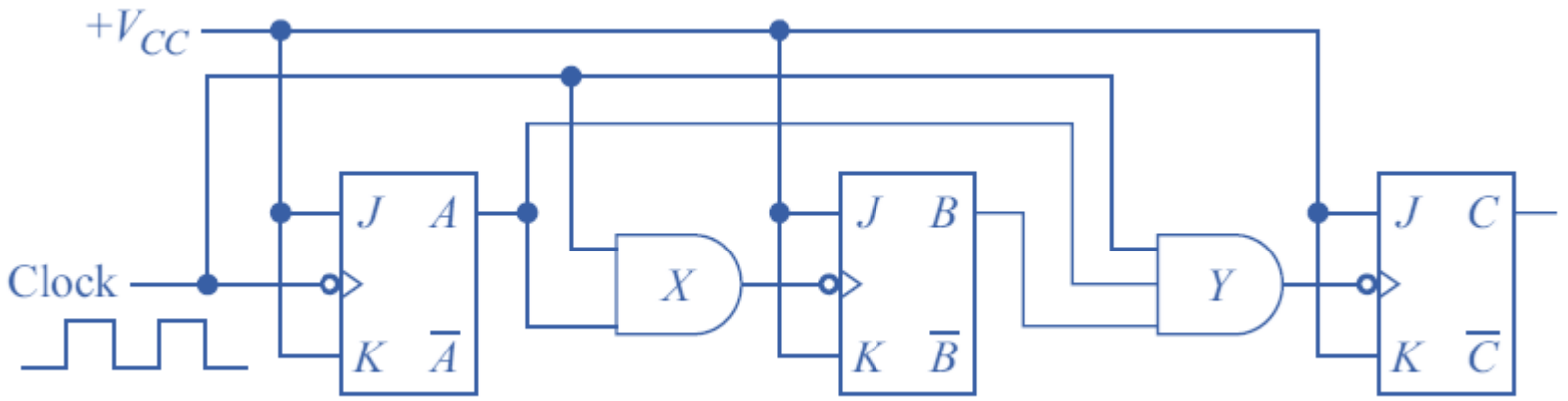
Glitch removed

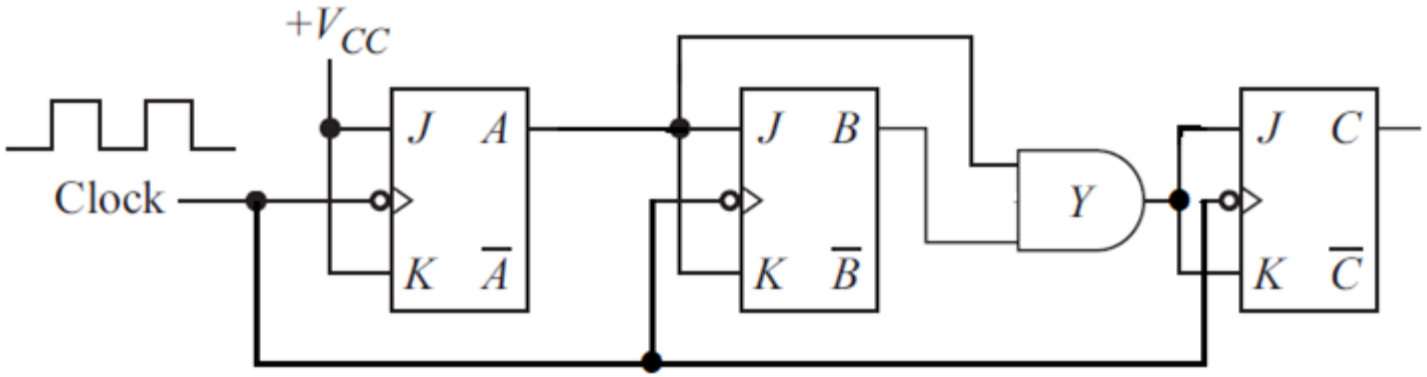
t_p = FF Propagation delay

Note that the basic gate delay for the decoding logic which is smaller than FF, is not shown in diagram .

T_{Clock} usually much larger than t_p

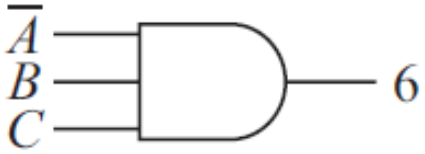
Synchronous Up Counter



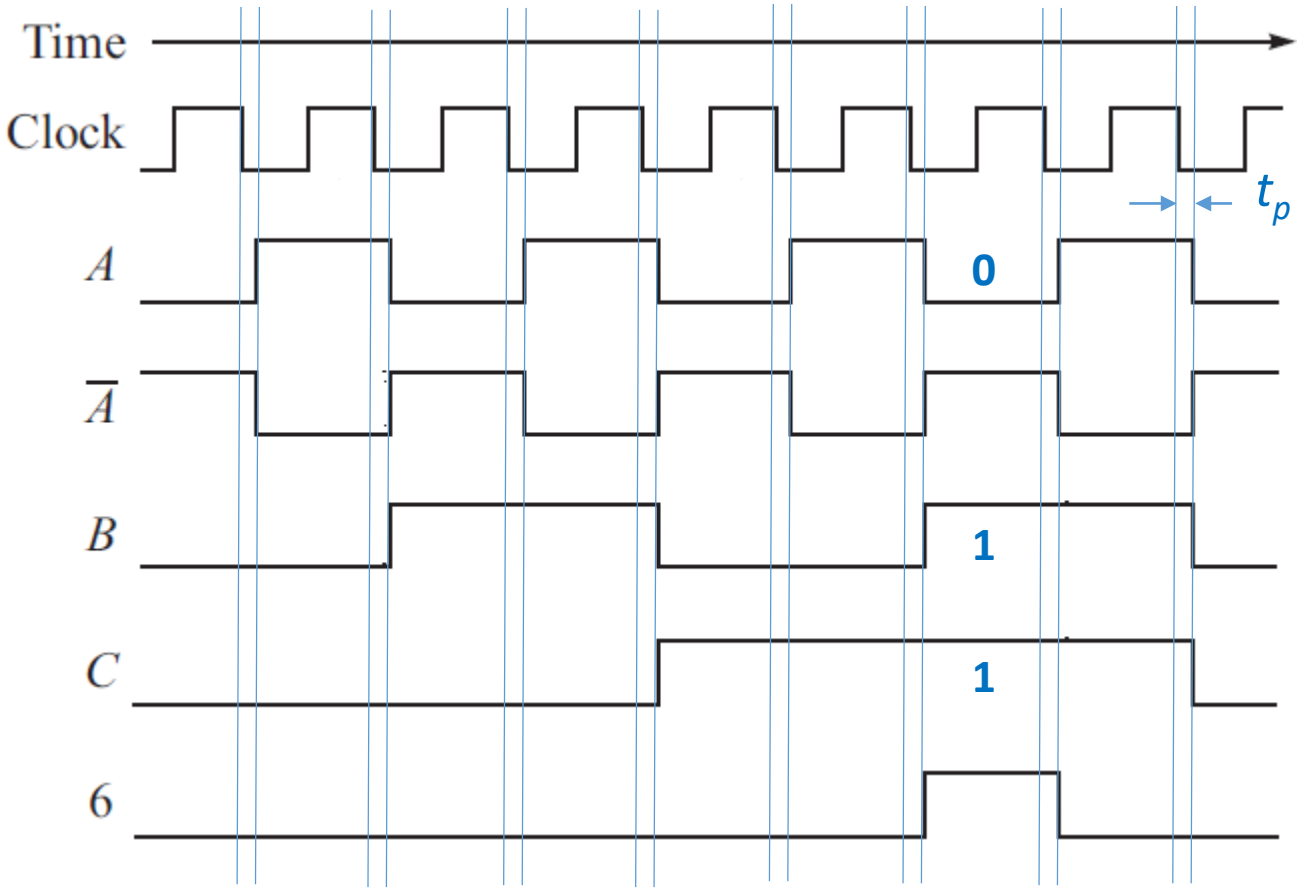


C	B	A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	0

Timing Diagram



Decoding 6

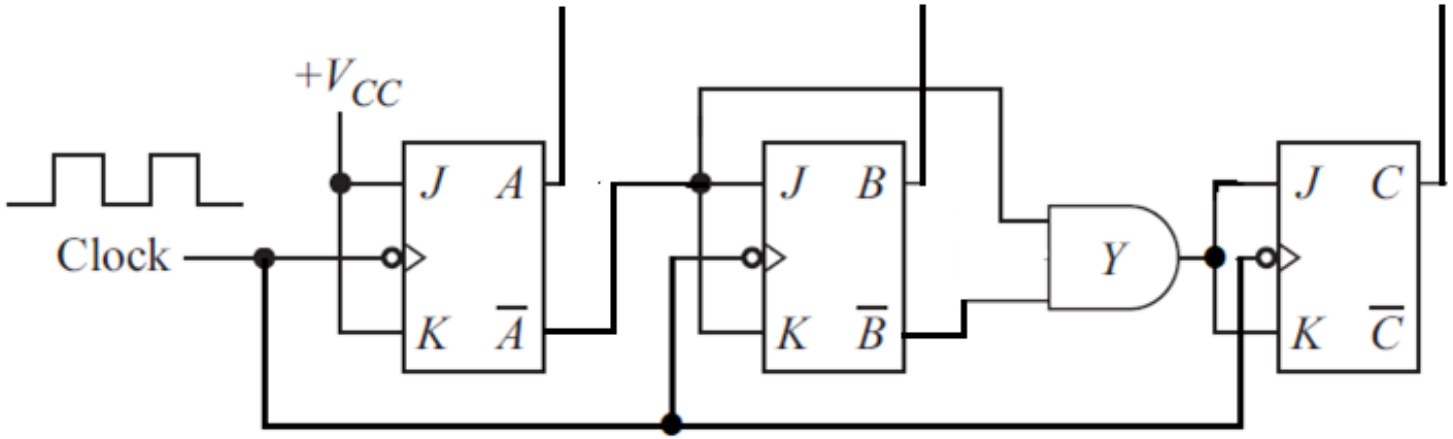


t_p = FF Propagation delay

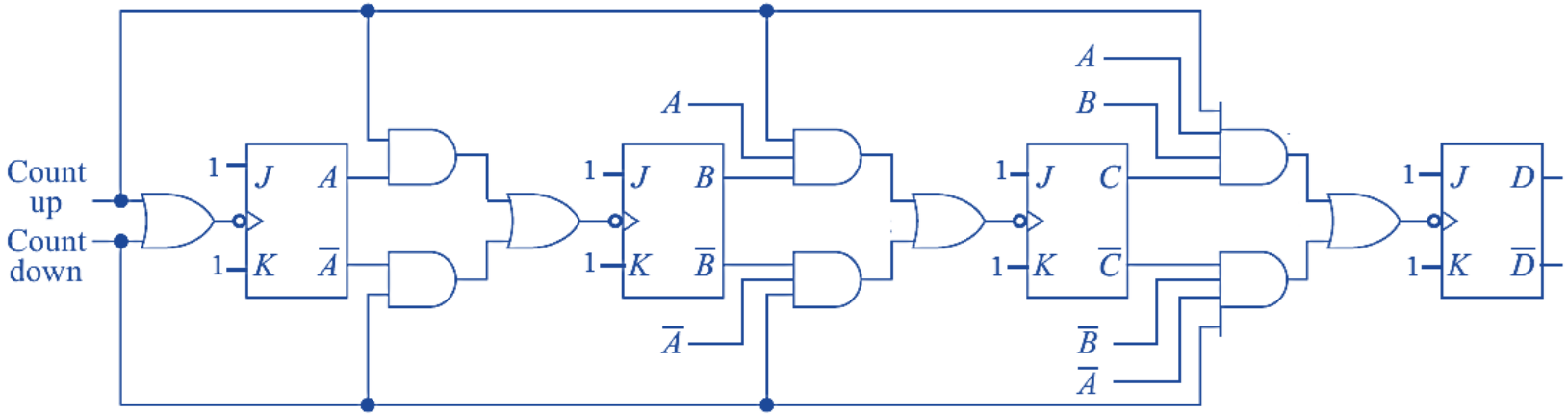
- No cumulative delay
- No glitch

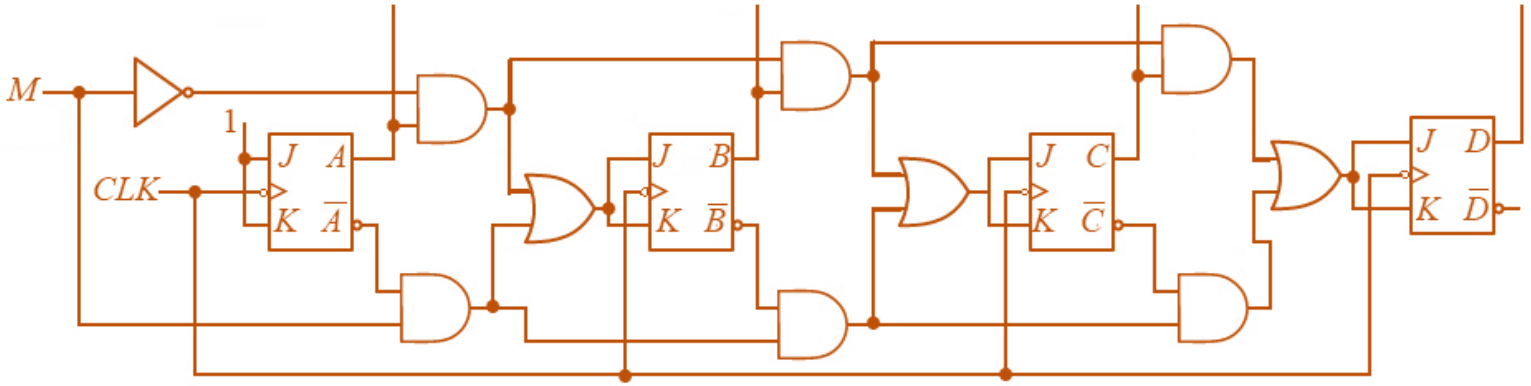
Synchronous Down Counter

C	B	A	Count
0	0	0	0
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0
1	1	1	7



Synchronous Up-Down Counter





Count states: *DCBA*

Up Counter: Clock to 'Count up' while 'Count down' held at 0.

Down Counter: Clock to 'Count down' while 'Count up' held at 0.

M is mode of counter

***M* = 0: Up**

***M* = 1: Down**

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Texas Instrument's Digital Logic Pocket Data Book (2007)