Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 20

Class Test 2:

29-10-2020 (THU):

8:00 – 8:55 AM

Syllabus: Logic families (not covered in CT1) and primarily post CT1, shall include concept dealt in pre-CT1 part which forms the pre-requisite.

Hamming Distance and Parity Code

- The number of bit positions by which code words differ is called Hamming distance.
- It can be found by counting number of 1s in bit-wise Ex-OR of two code words.

Parity bit

Data 1: 10100011
Data 2: 11011001

Code word 1: 010100011
Code word 2: 111011001

Even parity coded

Bit-wise Ex-Or output: 101111010 : Hamming distance, $d = 6$

Data 1: 00000000
Data 2: 00000001

Code word 1: 000000000
Code word 2: 100000001

Bit-wise Ex-Or output: 100000001 : Hamming distance, $d = 2$

Parity Code:
Data with a parity bit

Can detect 1 bit error.
Cannot correct any.

- To detect b bit errors, minimum hamming distance, $d_{min} = b + 1$.
- To correct b bit errors, minimum hamming distance, $d_{min} = 2b + 1$.

Hamming Code

- Useful for correcting 1-bit error. It uses more than 1 parity bits.
- Parity bits in the code word are positioned at 2^i-th positions.
  Rest of the positions are filled by data bits.

2^0	2^1		2^2				2^3							
P_1	**P_2**	D_3	**P_4**	D_5	D_6	D_7	**P_8**	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

- If m parity bits ($m \geq 2$) are used to code n data bits then,

$$2^m > m + n$$

Parity bits	Max. data bits	Max. total length
2	1	3
3	4	7
4	11	15

Hamming Code Generation

	$\mathbf{P_1}$	$\mathbf{P_2}$	D_3	$\mathbf{P_4}$	D_5	D_6	D_7
Binary coded position	0001	0010	0011	0100	0101	0110	0111

$P_1 = D_3 \oplus D_5 \oplus D_7$: All with 1 in 1's place of position

$P_2 = D_3 \oplus D_6 \oplus D_7$: All with 1 in 2's place of position

$P_4 = D_5 \oplus D_6 \oplus D_7$: All with 1 in 4's place of position

(7,4) Code: Rate = 4/7

Extending:

$\mathbf{P_1}$	$\mathbf{P_2}$	D_3	$\mathbf{P_4}$	D_5	D_6	D_7	$\mathbf{P_8}$	D_9	D_{10}	D_{11}	D_{12}
0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100

$d_{min} = 3$

Can detect all 2 bit error.

Can correct all 1 bit error.

$P_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11}$ …

$P_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11}$ …

$P_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12}$ …

$P_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12}$: All with 1 in 8's place of position

Example

Data: 10110101

P_1	P_2	1	P_4	0	1	1	P_8	0	1	0	1
0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100

$P_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} = 1 \oplus 0 \oplus 1 \oplus 0 \oplus 0 = 0$

$P_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$

$P_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} = 0 \oplus 1 \oplus 1 \oplus 1 = 1$

$P_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} = 0 \oplus 1 \oplus 0 \oplus 1 = 0$

Coded Data: 001**1**01**1**00101

One bit Error Correction

$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus P_1$

$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus P_2$

$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus P_4$

$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus P_8$

- If $C_8C_4C_2C_1 = 0000$: No error
- Else, it gives position of the error bit
  e.g. $C_8C_4C_2C_1 = 0111$ means 7^{th} bit is erroneously received
- Invert the erroneous bit to correct.

Example:

Coded Data: 001101100101
Data with : 001101100111
1-bit error
In 11^{th} pos.

$C_1 = 1 \oplus 0 \oplus 1 \oplus 0 \oplus 1 \oplus 0 = 1$

$C_2 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 1$

$C_4 = 0 \oplus 1 \oplus 1 \oplus 1 \oplus 1 = 0$

$C_8 = 0 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 1$

1011: 11^{th} bit 1 is erroneous
It is to be made 0 to correct

Note: If $C_8C_4C_2C_1 = 1000$ then 8^{th} position bit i.e. P_8 is erroneous.

Two bit Error Detection

$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus P_1$

$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus P_2$

$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus P_4$

$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus P_8$

$C_8C_4C_2C_1 = 0010$

$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus P_1$

$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus P_2$

$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus P_4$

$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus P_8$

$C_8C_4C_2C_1 = 0110$

⟸ Two bits flip

$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus P_1$

$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus P_2$

$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus P_4$

$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus P_8$

$C_8C_4C_2C_1 = 0001$

$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus P_1$

$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus P_2$

$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus P_4$

$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus P_8$

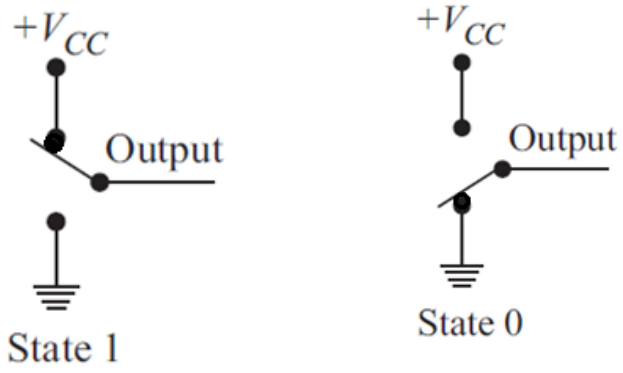
$C_8C_4C_2C_1 = 0000$

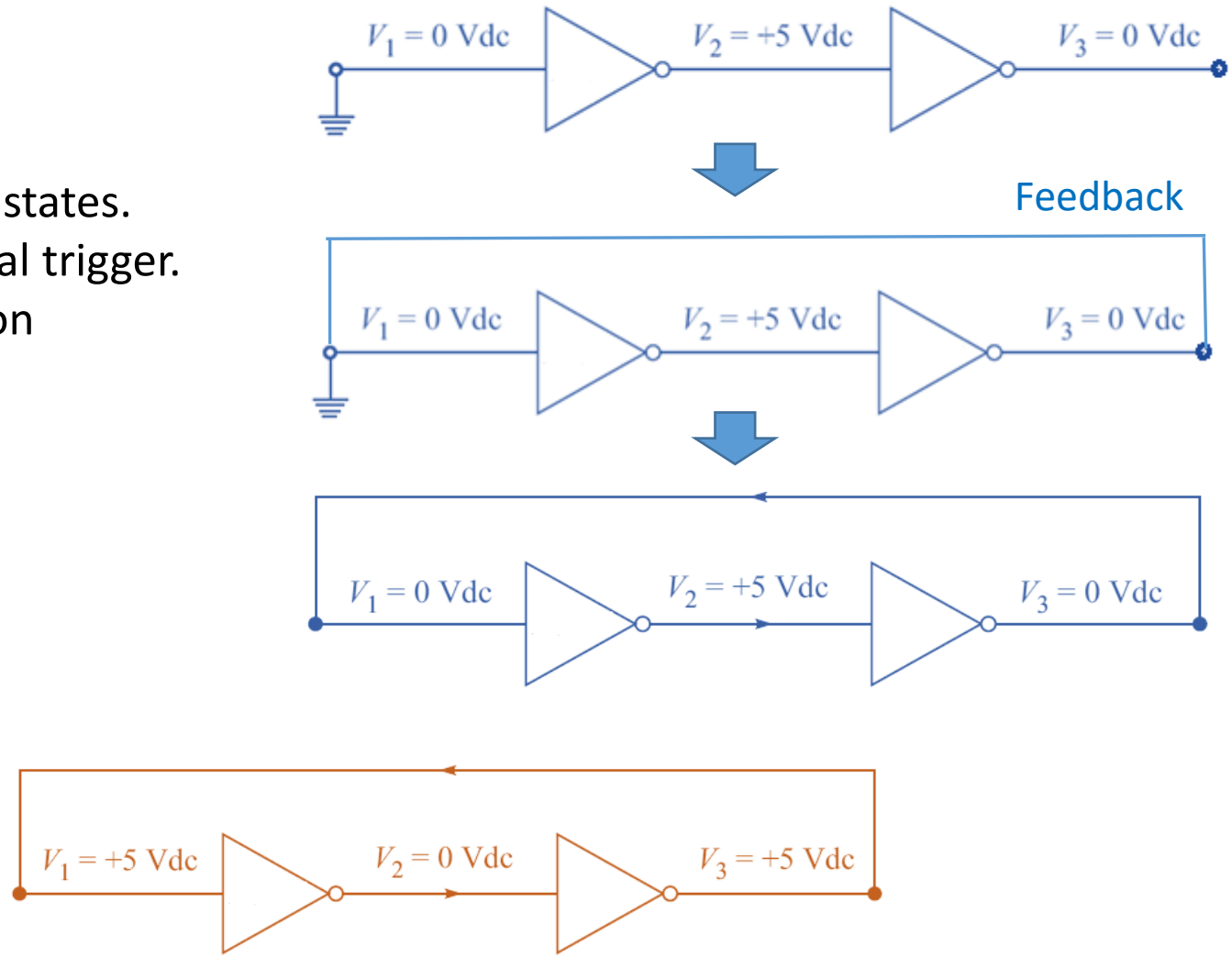
⟸ Three bits flip

Sequential Logic Circuit

Bistable Circuit

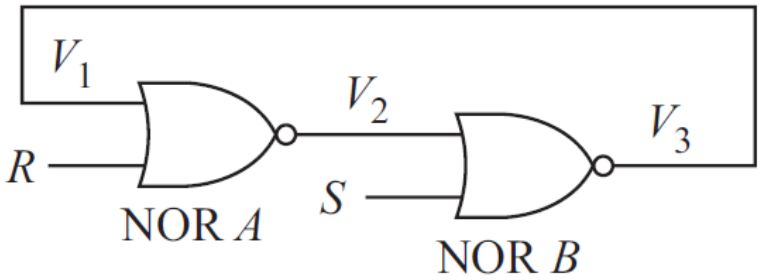
- A bistable circuit has two stable states.
- Its value changes only by external trigger.
- It can store one bit of information

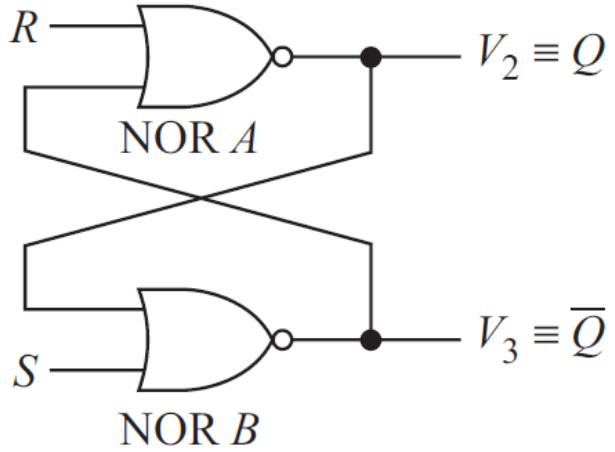




Inconvenient to apply input / trigger

SR Latch





S	R	Q_{last}	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	N.A.
1	1	1	N.A.

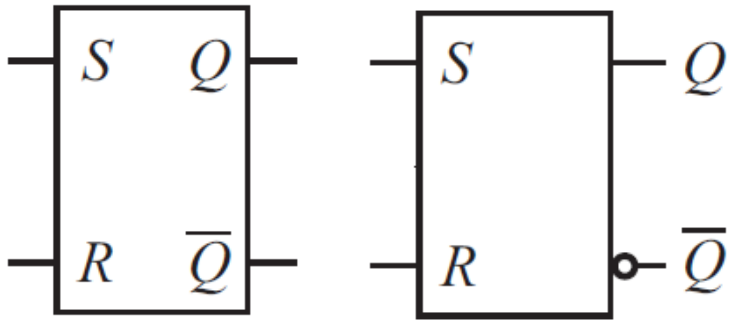
N.A.: Not allowed

S	R	V_2	V_3
1	1	0	0

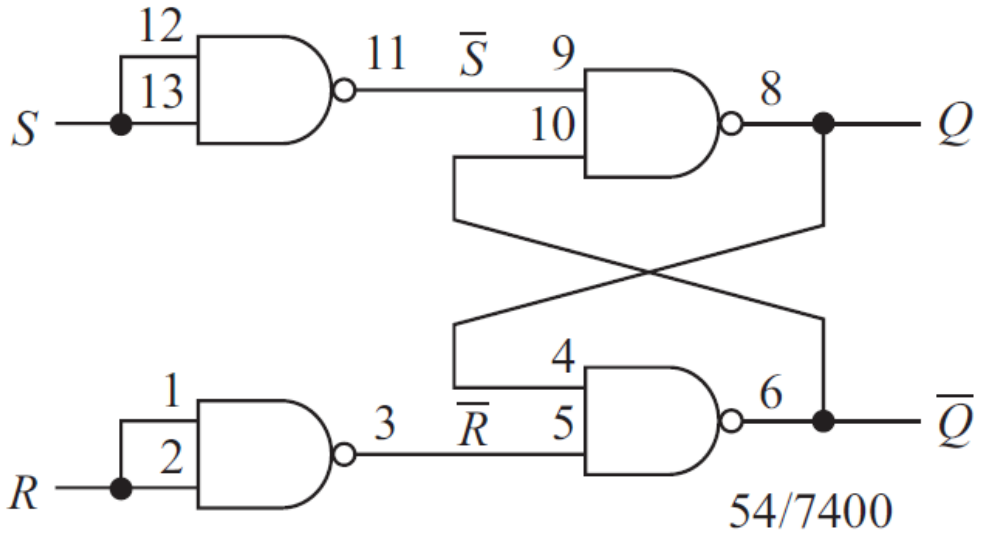
If SR = 00 follows SR = 11, then there is a **race** between two gates and depending on who responds faster, V_2V_3 settles at one of 01 or 10.

Latches to prior state

SR Latch



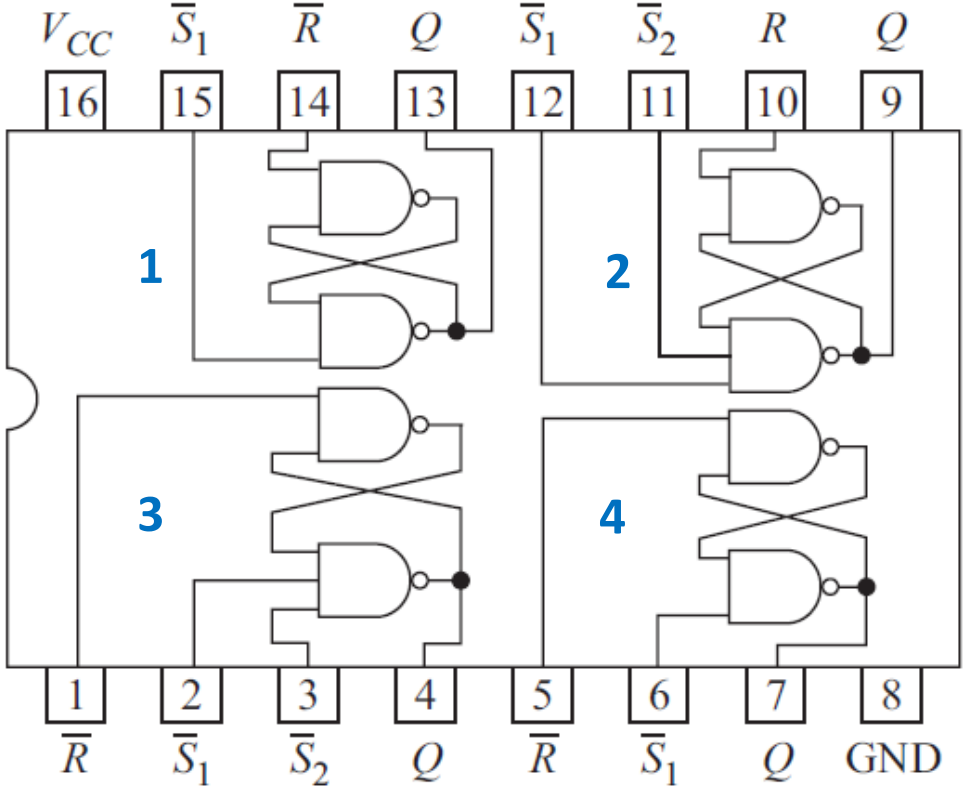
S	*R*	Q^+
0	0	Q^-
0	1	0
1	0	1
1	1	N.A.



Realizing *SR* Latch using only NAND gate

$\overline{S}$	$\overline{R}$	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	Last state

IC 74279



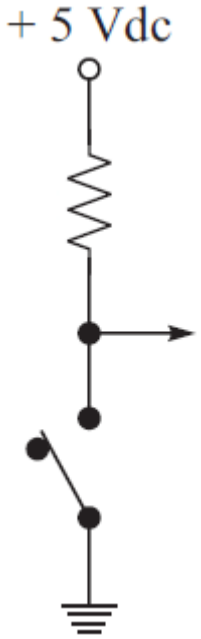
$\overline{S}_1$	$\overline{S}_2$	$\overline{R}$	Q
0	0	0	Forbidden
0	X	1	1
X	0	1	1
1	1	0	0
1	1	1	Last state

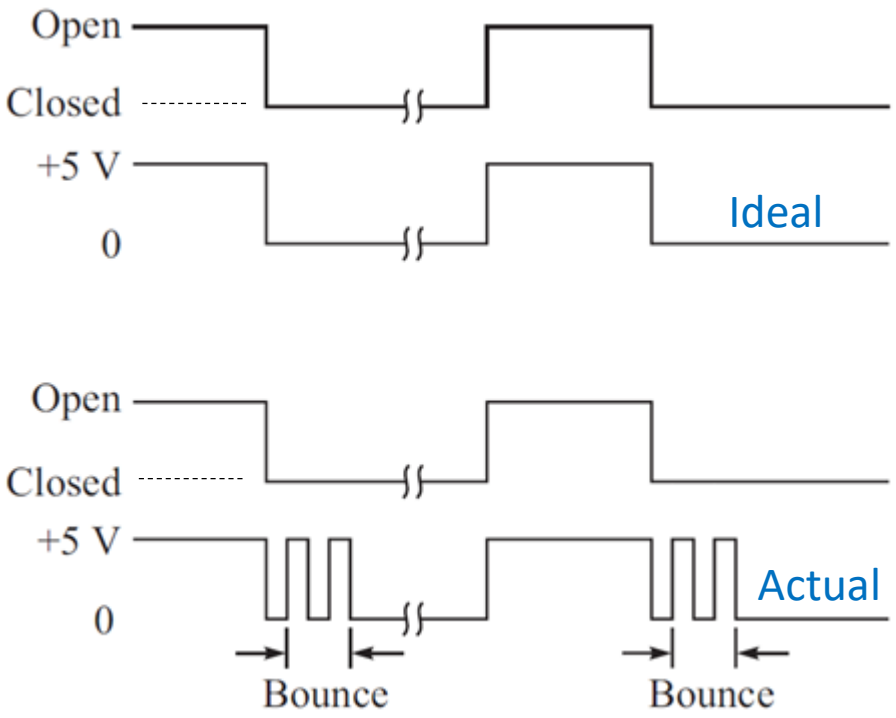
Truth Table of 2 and 3

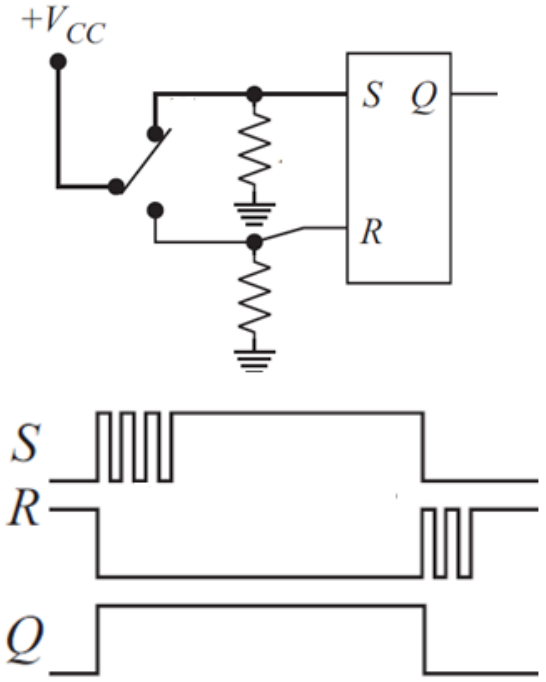
$\overline{S}_1$	$\overline{R}$	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	Last state

Truth Table of 1 and 4

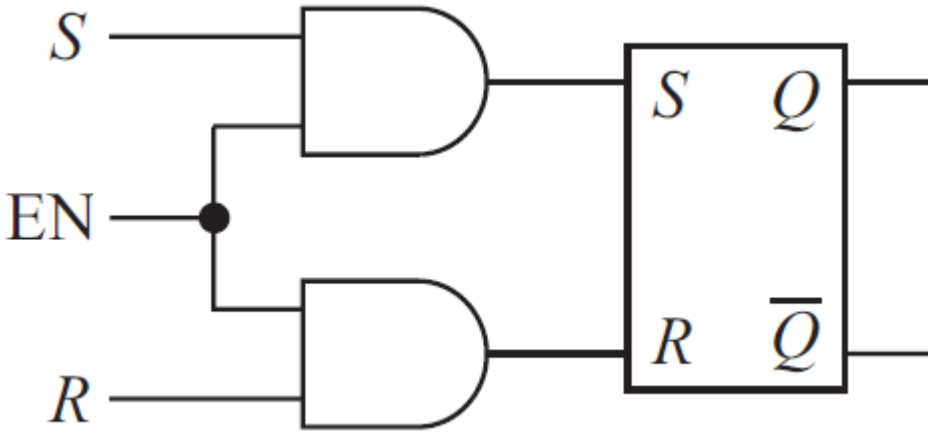
Debounce Switch





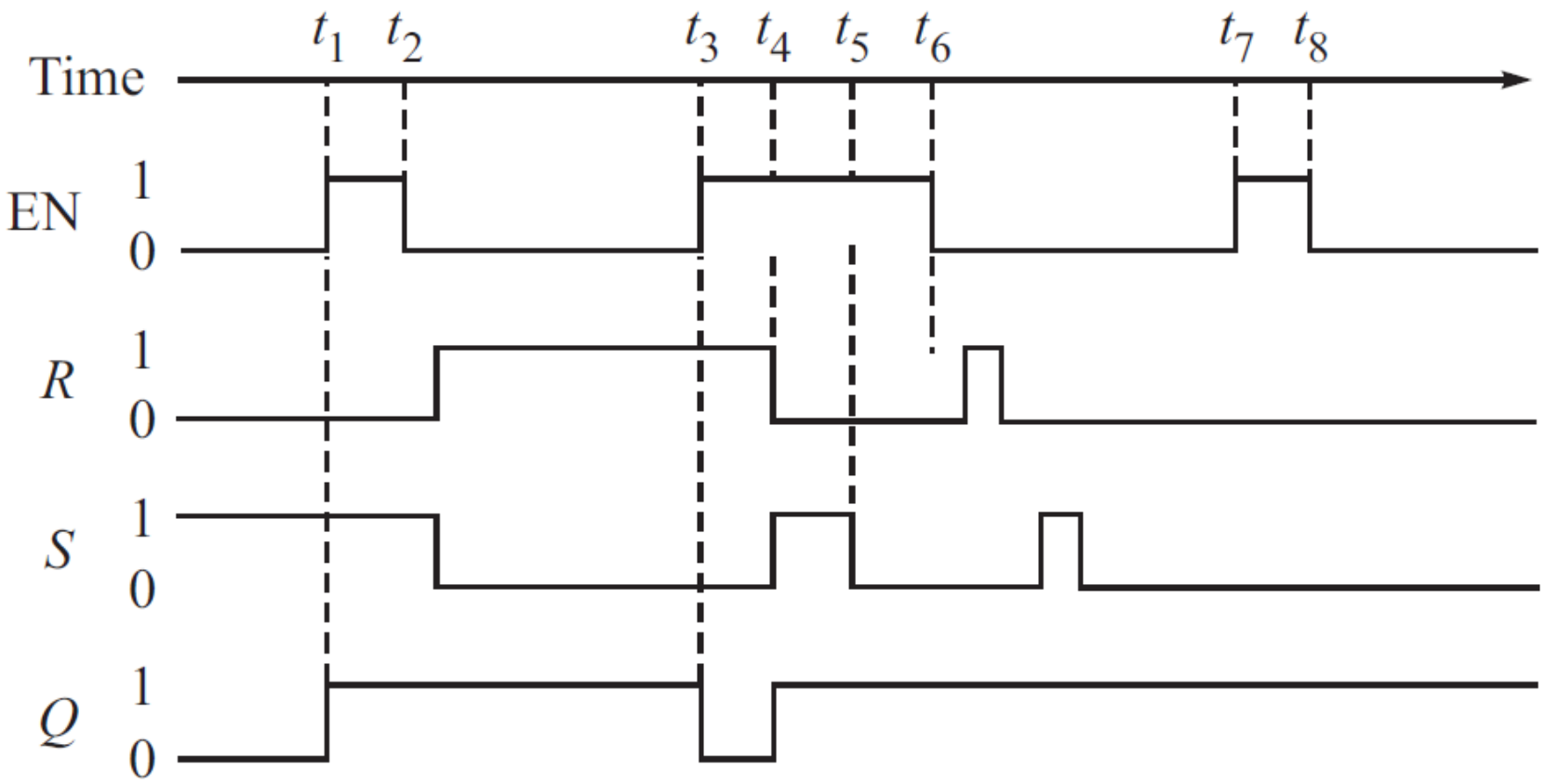


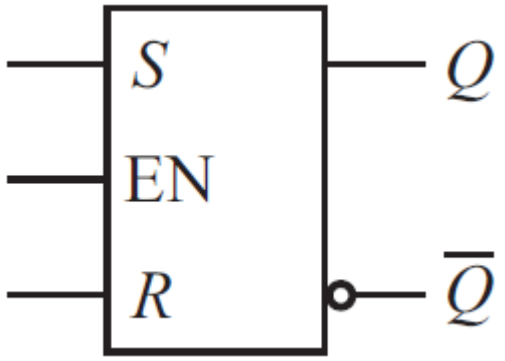
Gated Latch



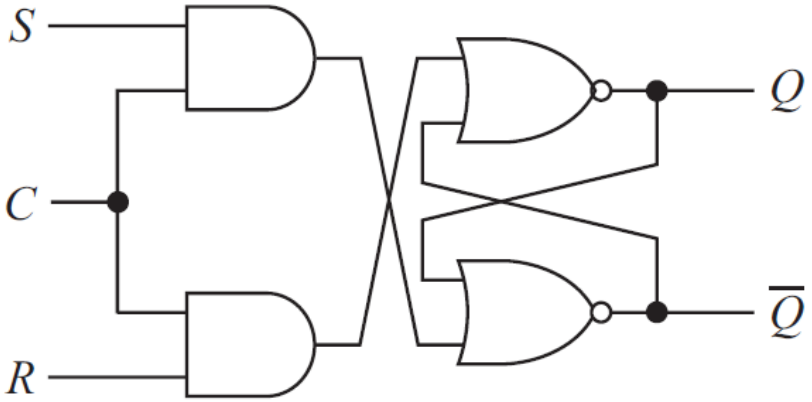
EN	S	R	Q_{n+1}
1	0	0	Q_n (no change)
1	0	1	0
1	1	0	1
1	1	1	Forbidden
0	X	X	Q_n (no change)

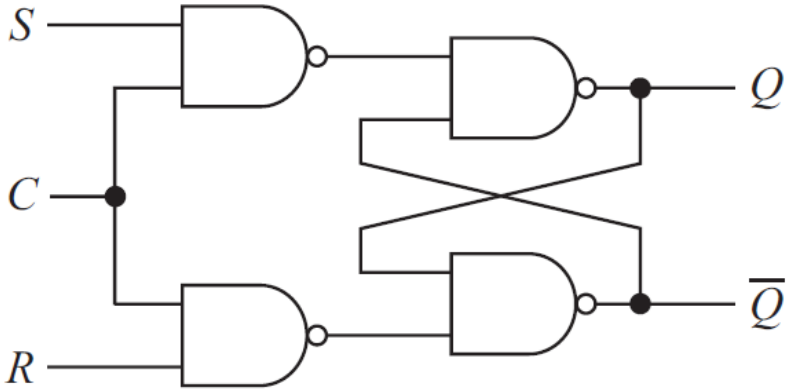
Gated Latch





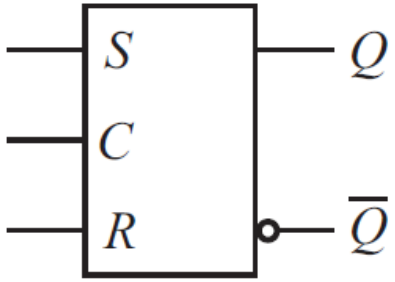
Clocked *SR* Flip-Flop





Usually, Latch with clock / enable input is referred as Flip-Flop.

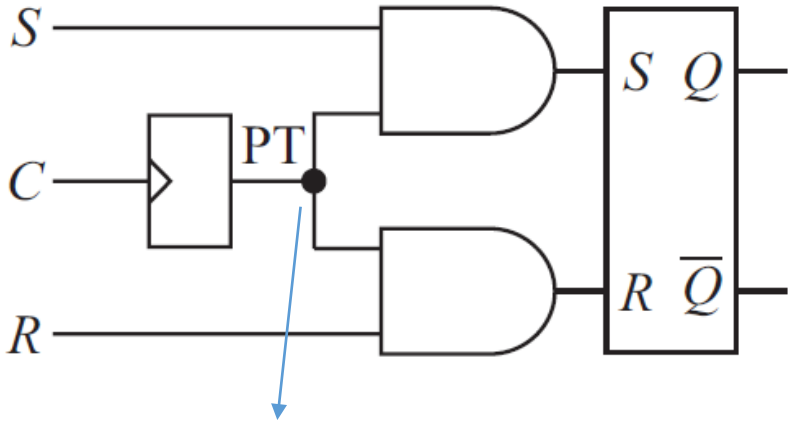
When *C* is at HIGH level, state can change according to *SR* input.



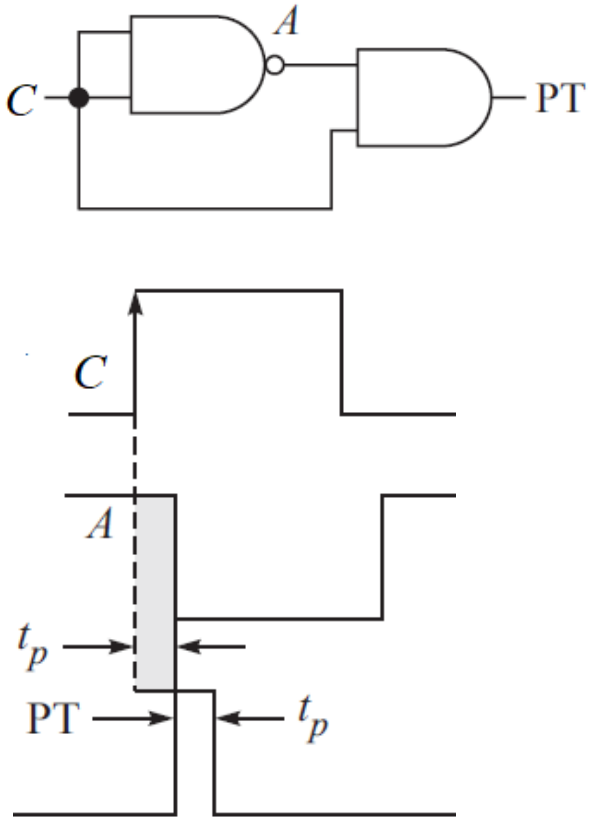
Level-triggered *SR* Flip-Flop

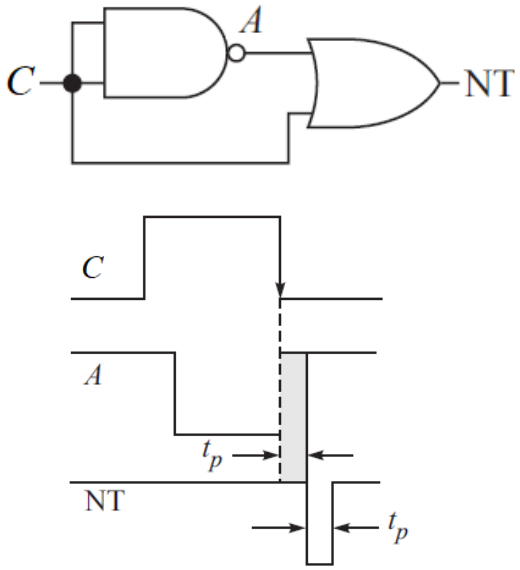
Triggering with Narrow Pulse

- Synchronous digital system requires one state change per clock cycle, synchronized with clock.
- More than one state change can occur in level-triggered flip-flop if there is feedback / input changes when clock remains enabled.

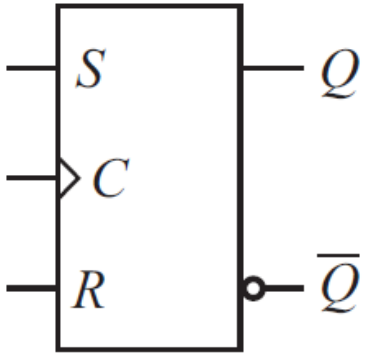


A very narrow pulse width positive trigger (effectively edge-triggered)

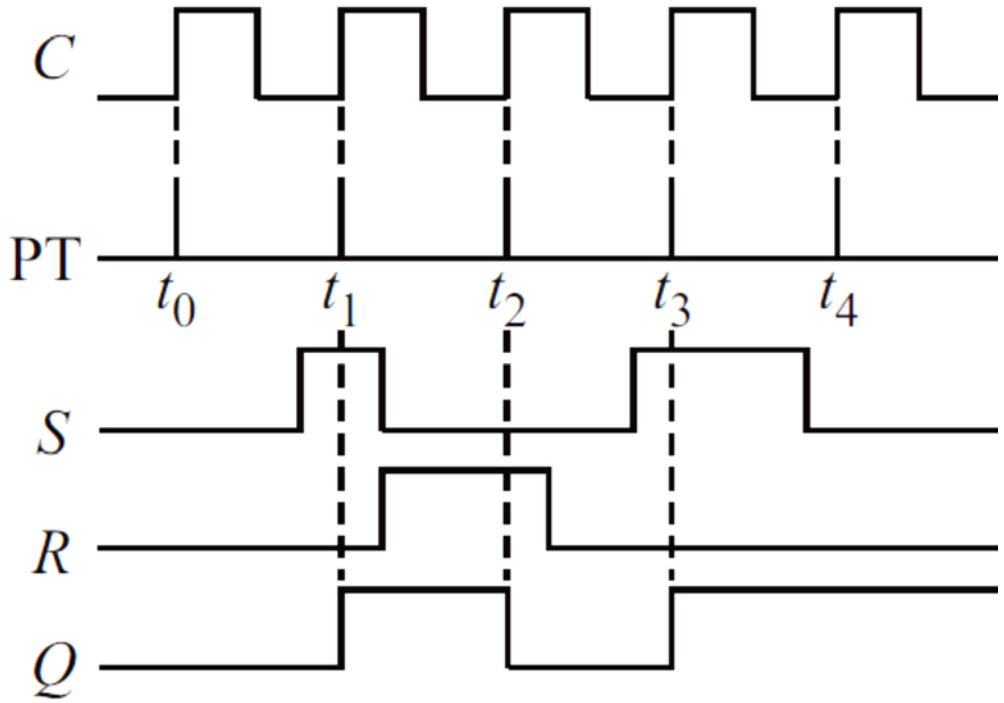




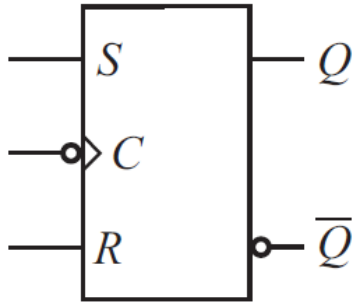
Edge Triggered *SR* Flip-Flop



C	S	R	Q_{n+1}	Action
↑	0	0	Q_n	No change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	Forbidden	

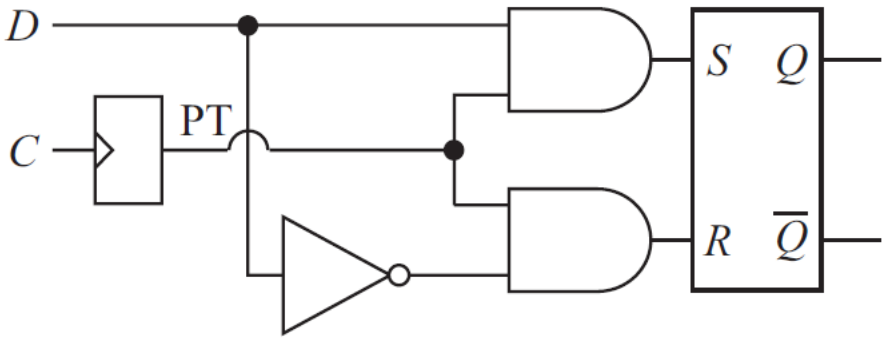


+ve edge triggered SR Flip-Flop

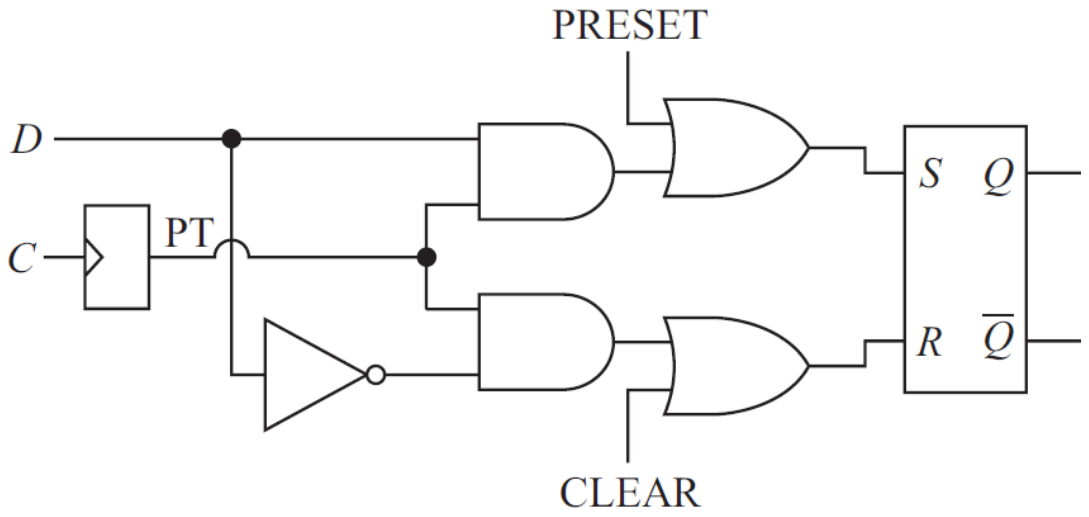


-ve edge triggered SR Flip-Flop

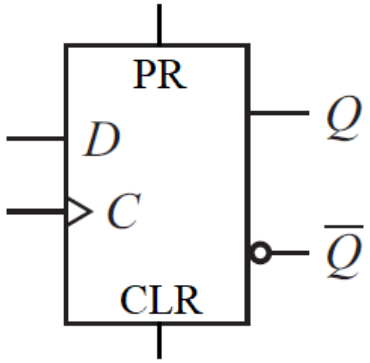
D Flip-Flop



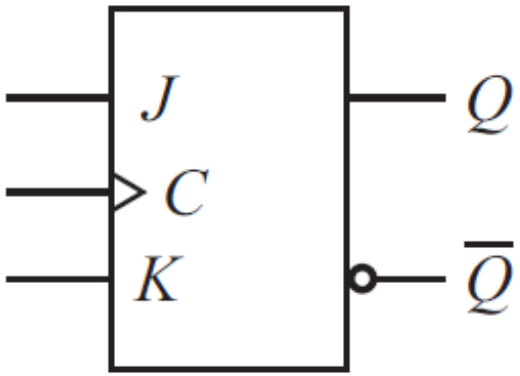
C	D	Q_{n+1}
0	X	Q_n (last state)
↑	0	0
↑	1	1

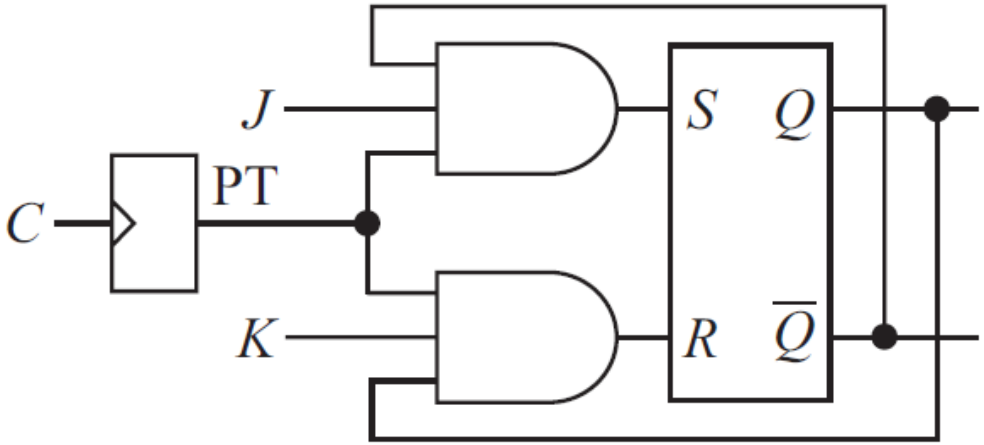


D Flip-Flop with asynchronous preset and clear

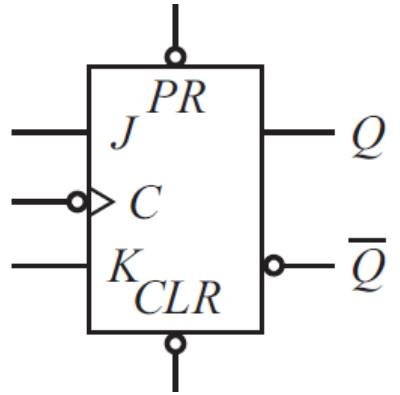


JK Flip-Flop



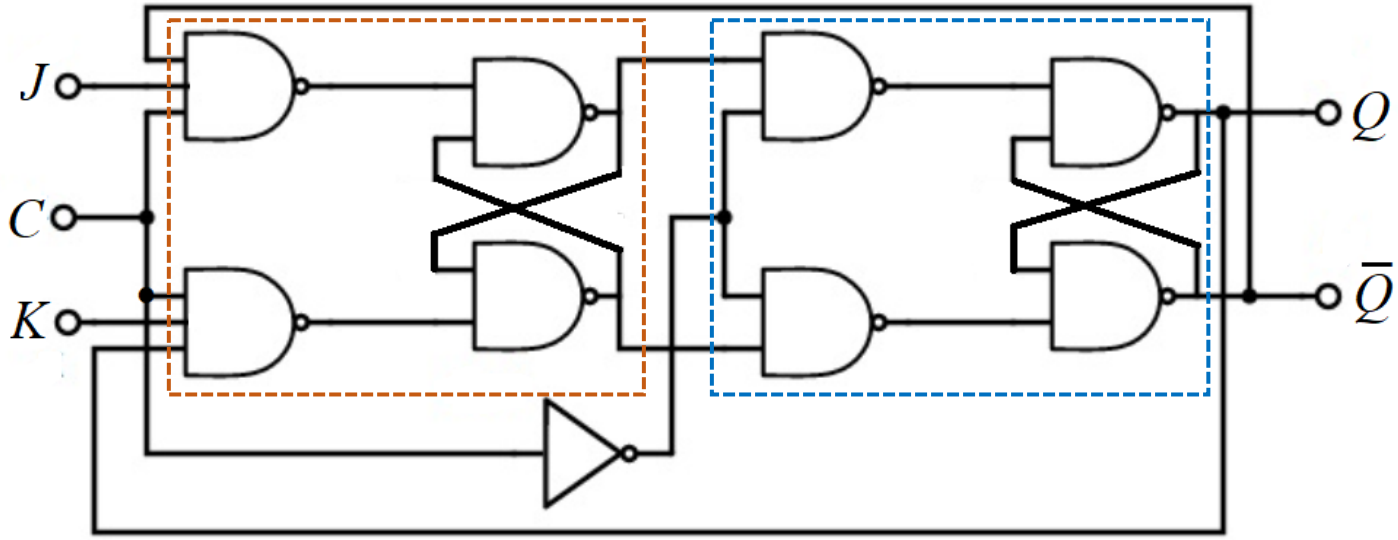


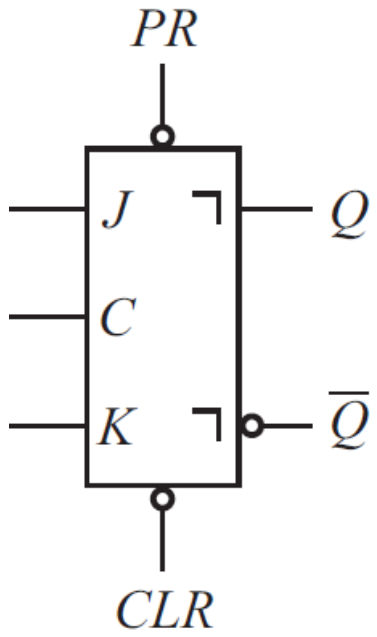
C	J	K	Q_{n+1}	Action
↑	0	0	Q_n (last state)	No change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	$\overline{Q}_n$ (toggle)	Toggle



Dual -ve edge triggered JK Flip-Flop with active low PRESET and CLEAR

Master-Slave Flip-Flop





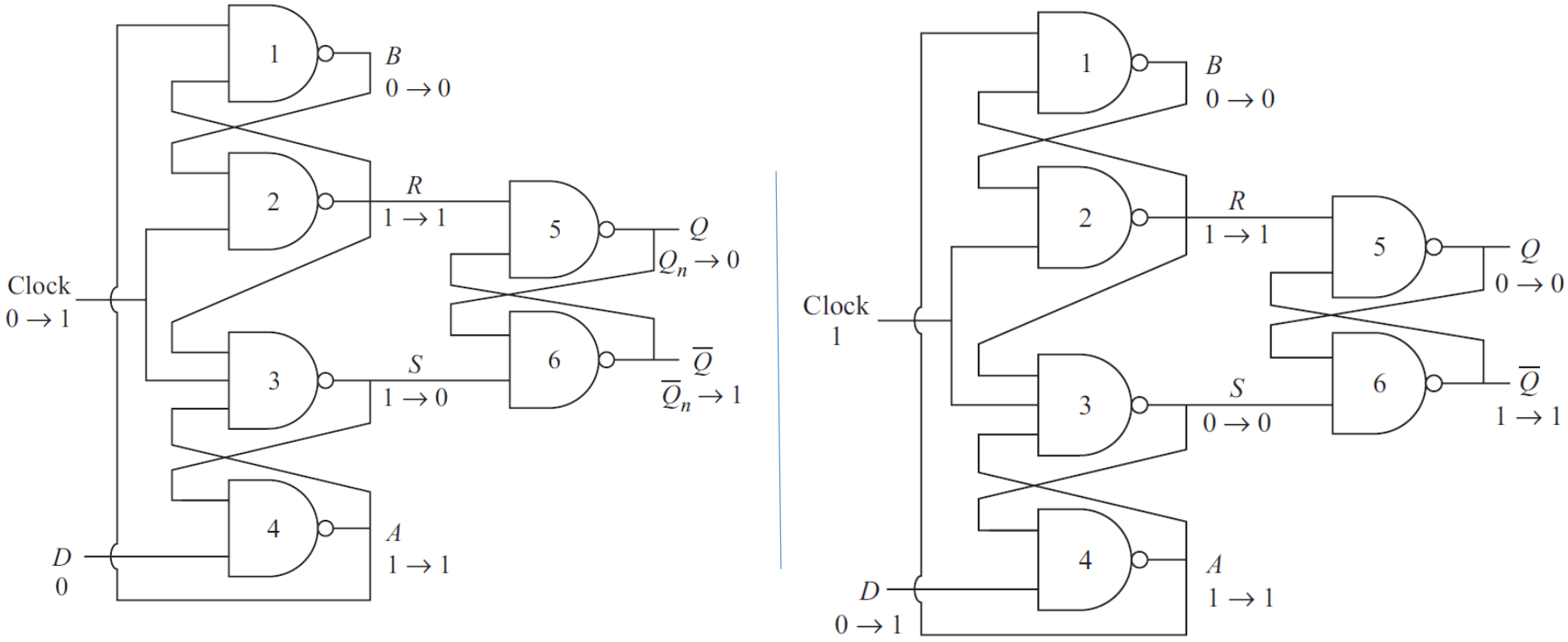
IC 7476
JK Master-Slave with asynch. preset and clear

Master Flip-Flop: According to type of Flip-Flop i.e. *JK*, *SR*, *D*.

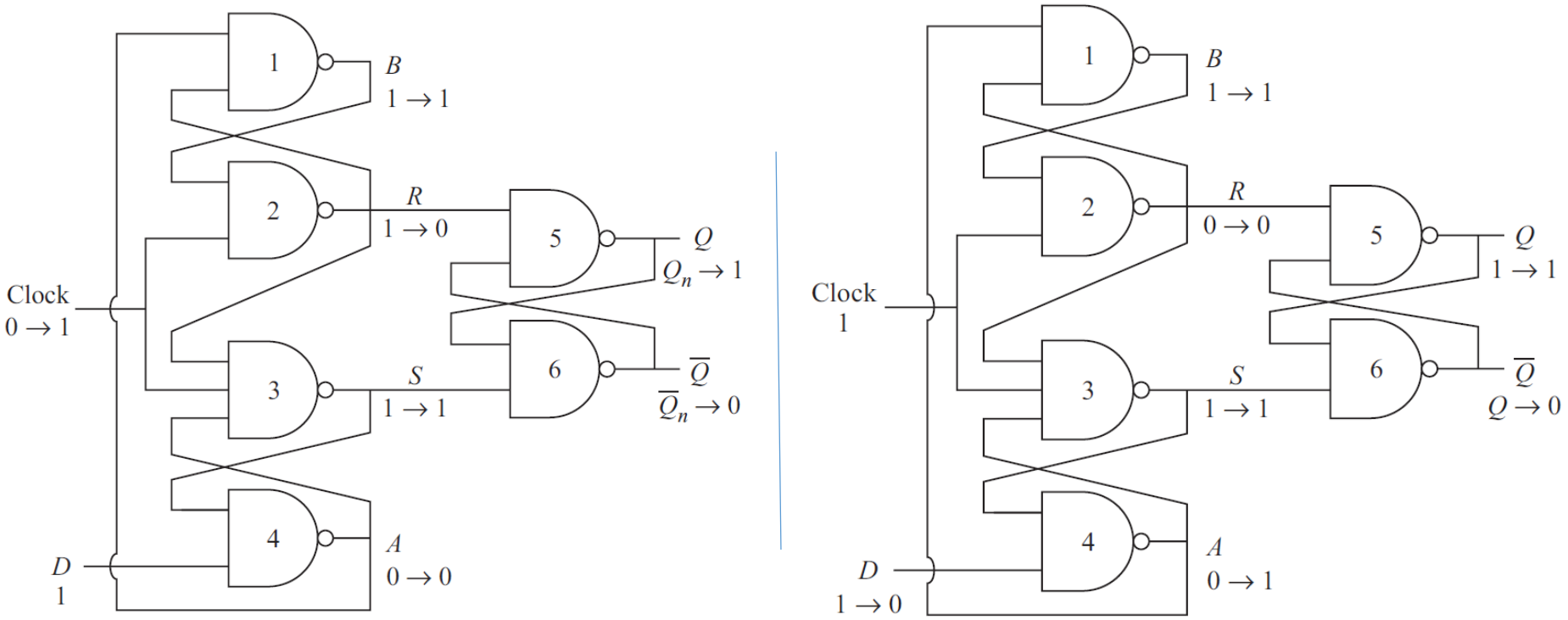
Slave Flip-Flop: Always *SR* Flip-Flop.

Individually level-triggered, changes in different phases of clock, effectively edge-triggered.

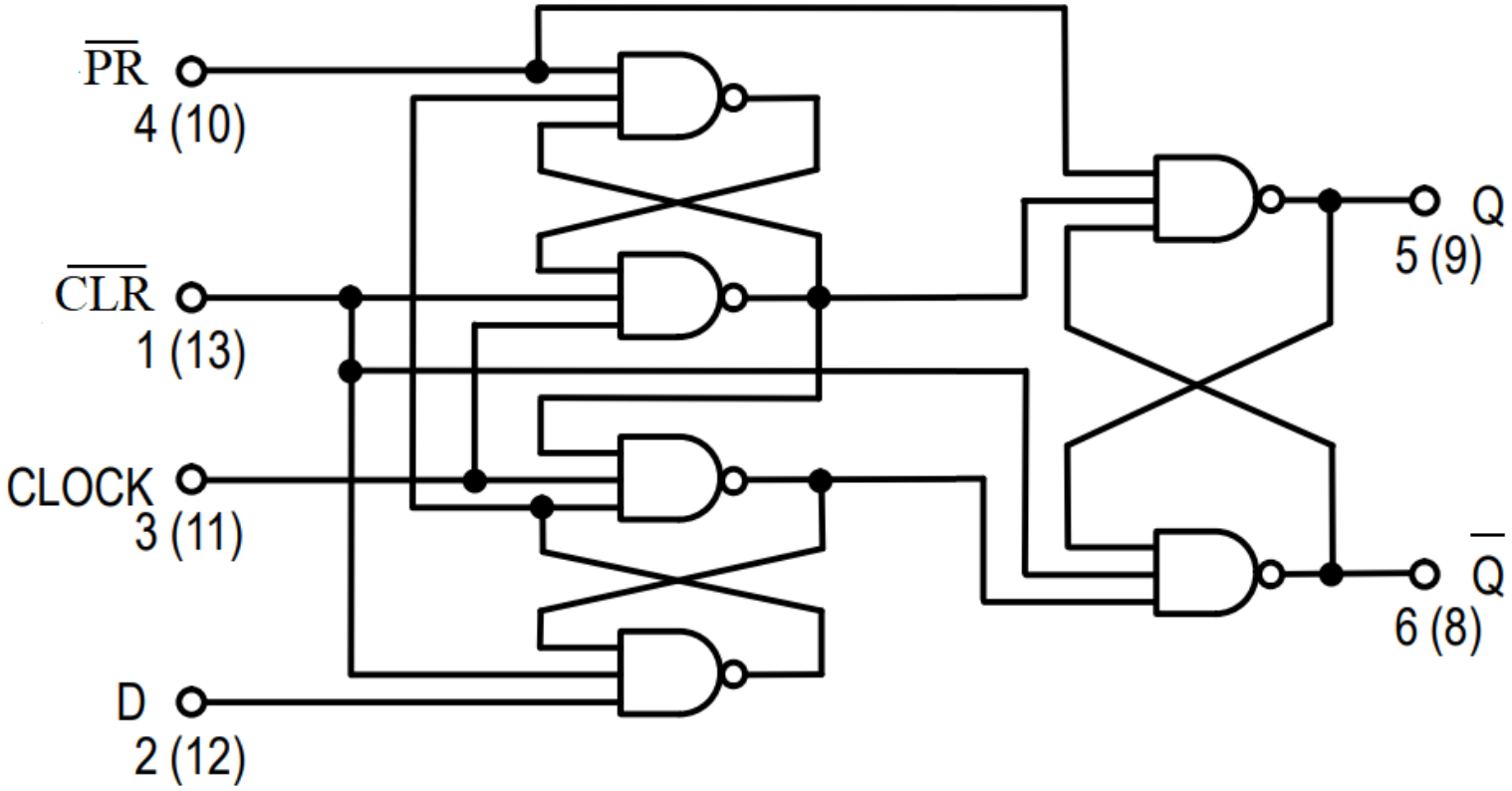
Edge-Triggering by Input Lockout



Edge-Triggering by Input Lockout



IC 7474



IC 7475 is a Quad D latch with two enables (one each for 2 latch).

IC 7476A: Dual -ve edge triggered JK Flip-Flop with active low PRESET and CLEAR

IC 7474: Dual +ve edge-triggered D Flip-Flop with asynch. active low preset and clear.

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- Texas Instrument's Digital Logic Pocket Data Book (2007)