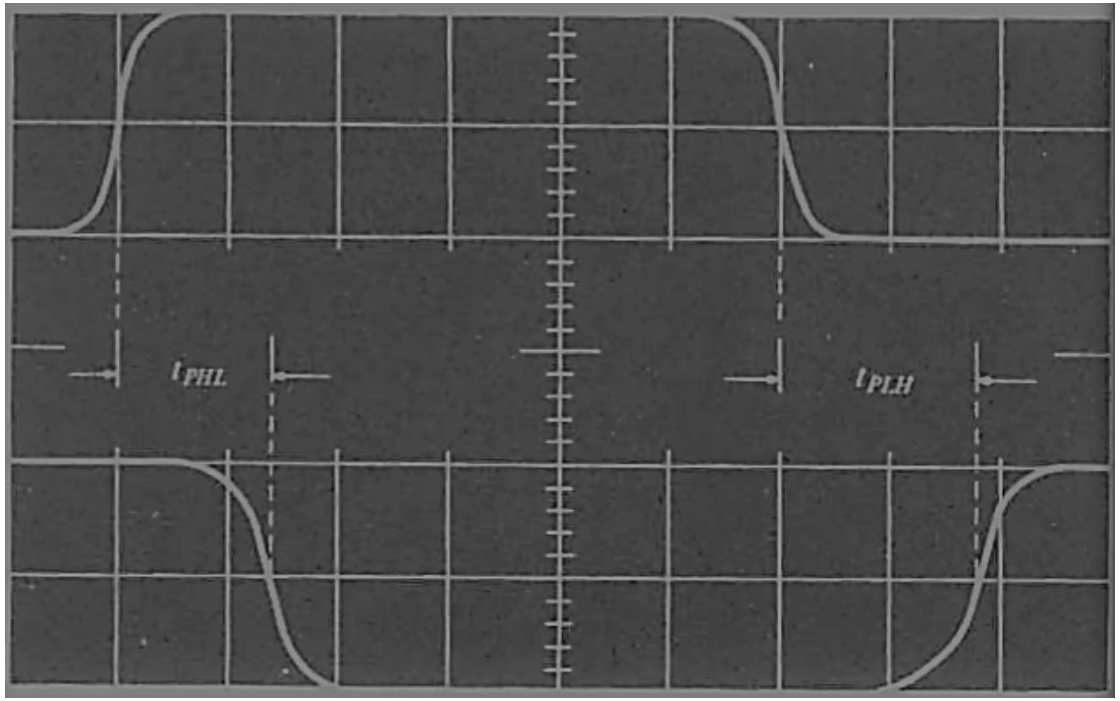
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 2

Propagation Delay

- Due to finite switching speed of transistors and circuit capacitances



t_{PHL}: Delay in changing output from H to L
t_{PLH}: Delay in changing output from L to H

Propagation delay, $t_{PD} = (t_{PHL} + t_{PLH})/2$

t_r: Rise time → 10% to 90% of max.
t_f: Fall time → 90% to 10% …

Power dissipation

- **Static power dissipation**
  - when transistor is either ON or OFF
  - depends on current drawn in each case
  - power dissipation, P_D is average of these two
  - significant in switching of Bipolar Junction Transistor

- **Dynamic power dissipation**
  - when transistor switches
  - depends on switching speed
  - significant in switching of CMOS Transistor

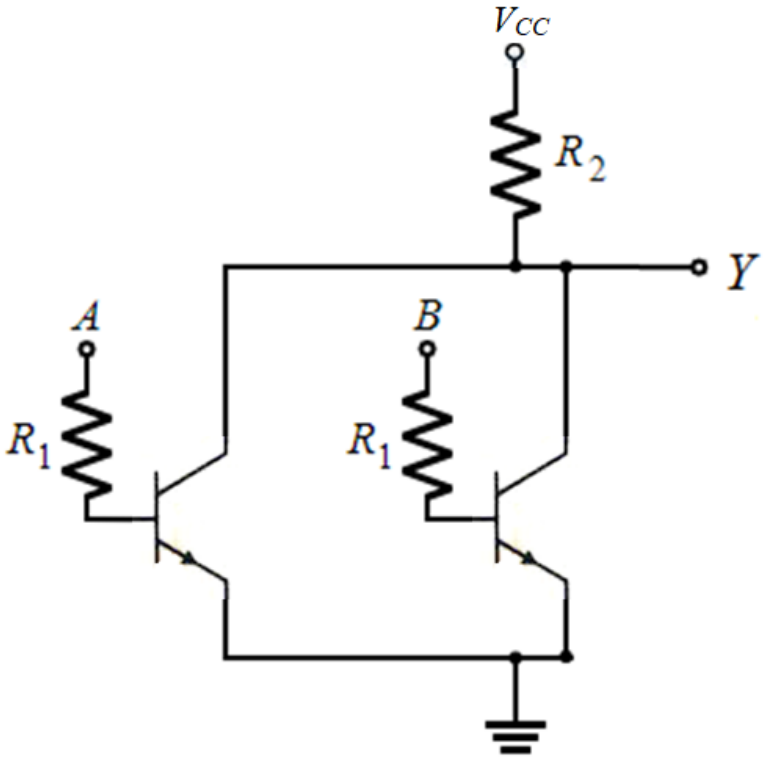
Figure of Merit,

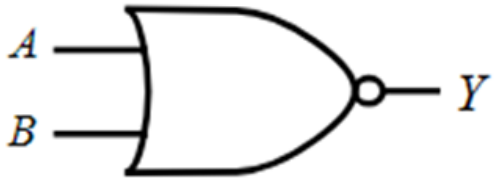
$F = P_D \times t_{PD}$

The lower the F, the better.

RTL NOR Gate

RTL: Resistance Transistor Logic

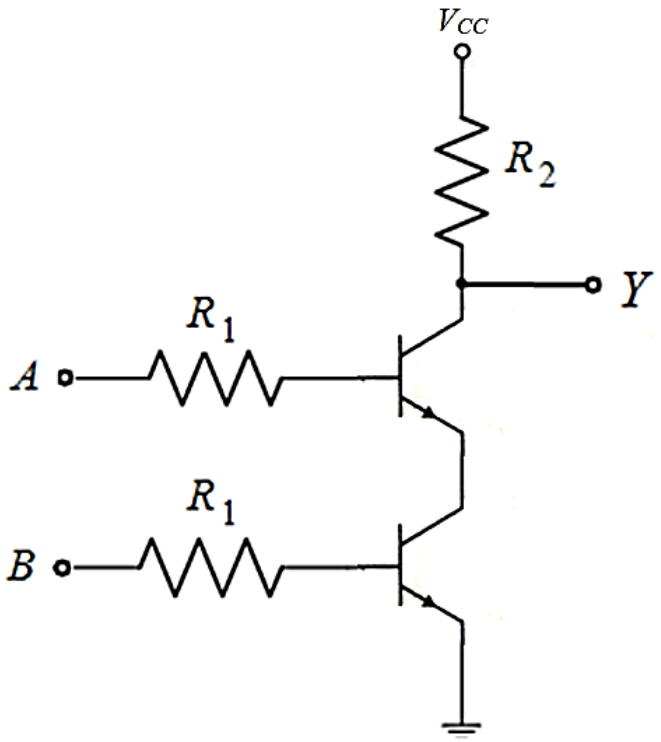


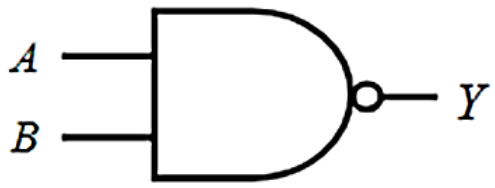


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

- For 3 input NOR gate, another input would come in parallel with *A* and *B.*
- More no. of inputs increases delay
- *Fan-in*: Max. number of inputs a gate can handle

RTL NAND Gate





A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

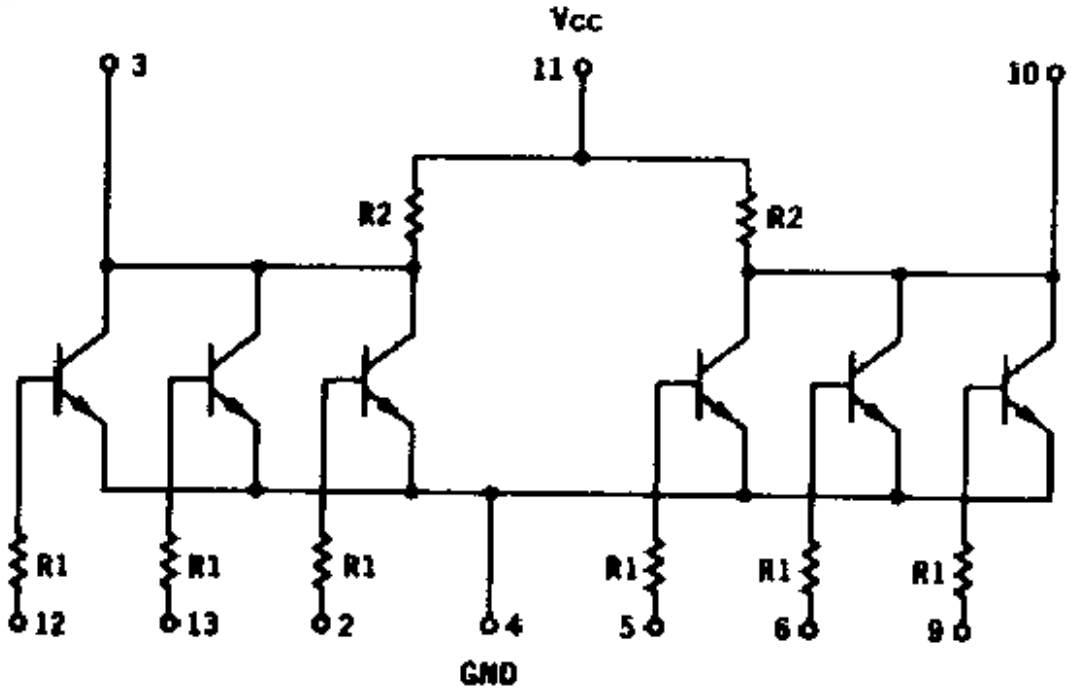
It will be shown that any other logic gates can be obtained using only NAND gate or NOR gate.

From Archive (Motorola datasheet)

DUAL 3-INPUT GATES

PLASTIC MRTL MC700P/800P series

MC715P • MC815P



Two 3-input NOR gates

R1 = 450Ω , R2 = 640Ω

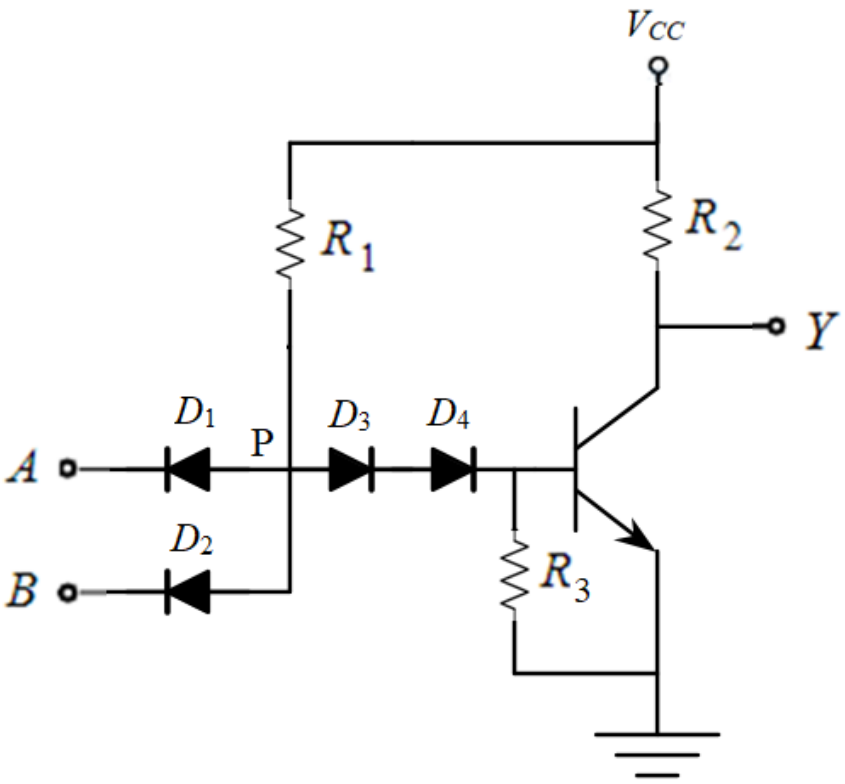
P_D = 55 mW (input H), 15 mW (input L)

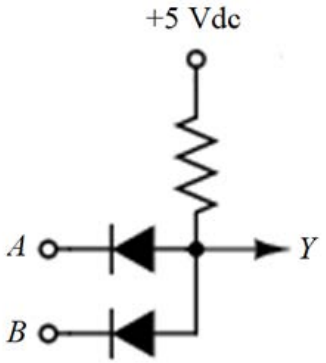
t_{PD} = 12 ns

The MRTL family of resistor-transistor logic offers the industry's broadest line of digital circuits. Devices in this section are medium-power circuits; low-power mW MRTL circuits are also available.

DTL NAND Gate

DTL: Diode Transistor Logic



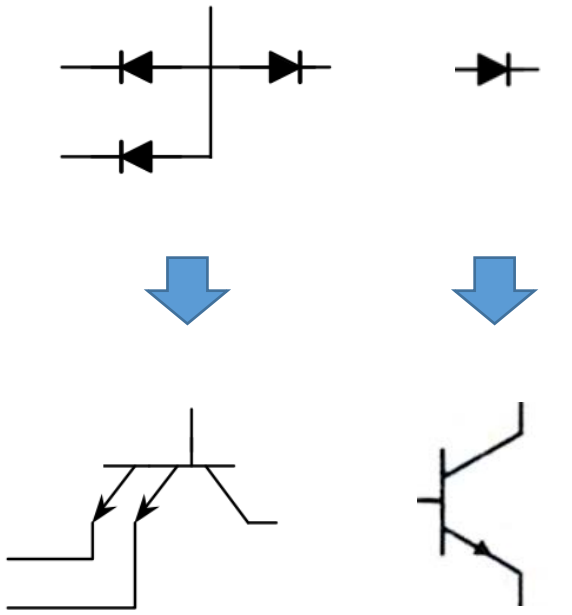


A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- D_1, D_2, R_1, V_{CC} : AND logic at P.
- D_3 and D_4 are level shifters (V_P = 3 x 0.7V turns ON transistor.)
- R_3 provides discharge path of stored charge at BE junction that reduces t_{PLH}.
- Any of A or B low (0.2 V), V_P = 0.9 V, insufficient to turn ON the transistor.

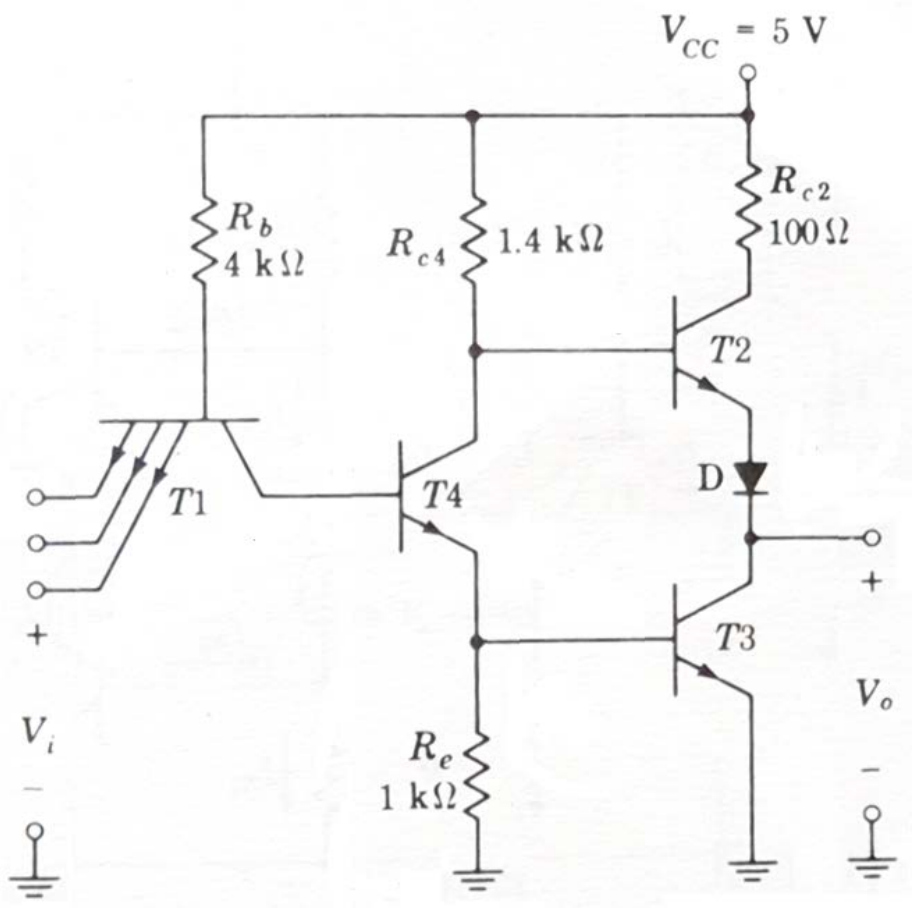
TTL: Transistor Transistor Logic

NAND Gate



Multi-emitter Transistor

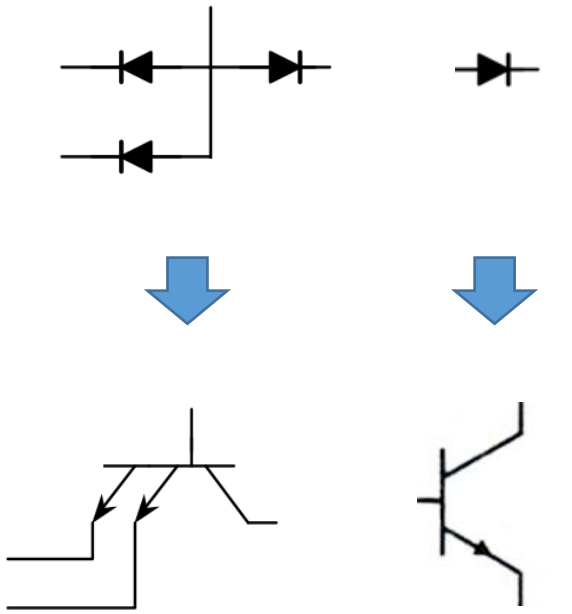
Phase splitter



- Totem pole output reduces output resistance when at H.
- R_3 cannot be made zero.
- D_1 to avoid indeterminate output.

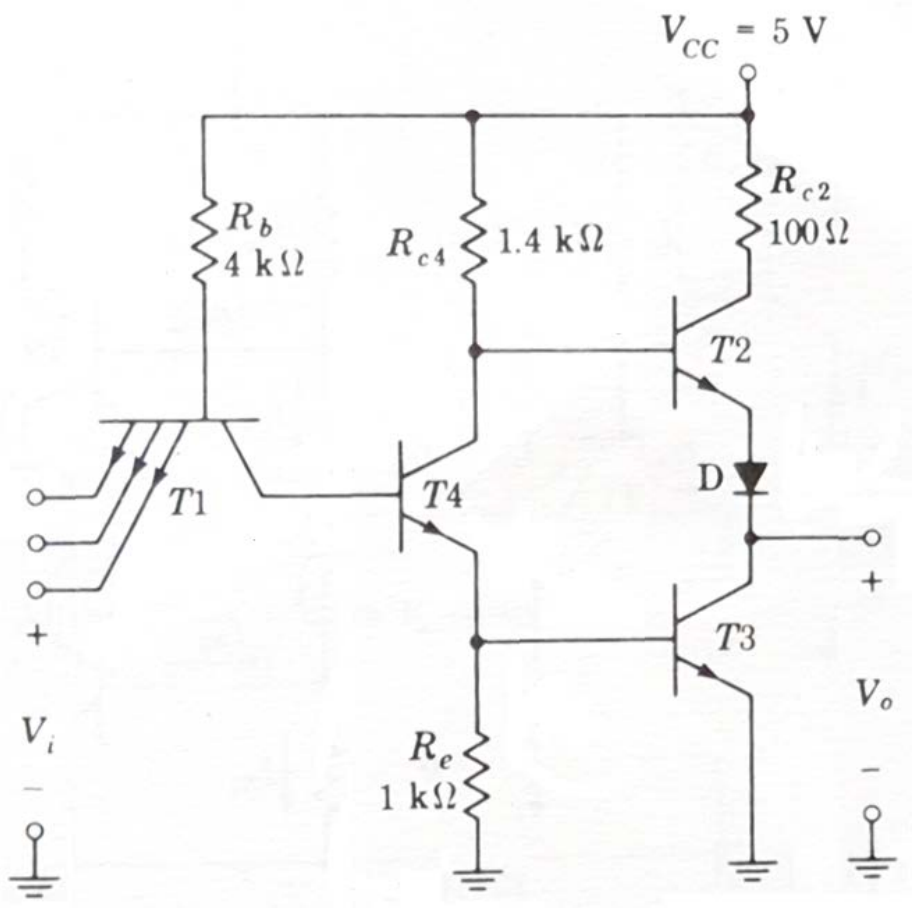
TTL: Transistor Transistor Logic

NAND Gate



Multi-emitter Transistor

Phase splitter



- Totem pole output reduces output resistance when at H.
- R_{c2} cannot be made zero.
- D_1 to avoid indeterminate output.

References:

- Grinich, V.H., and H.G. Jackson, Introduction to Integrated Circuits, McGraw-Hill
- Herbert Taub, and Donald Schilling, Digital Integrated Electronics, McGraw Hill
- Motorla Datasheet accessed on Oct. 08, 2018 from

http://willowdaledesign.com/17_MRTL_700P_800P_text.pdf