Tutorial 1

EC31003 – Digital Electronics Circuits

12/09/2020

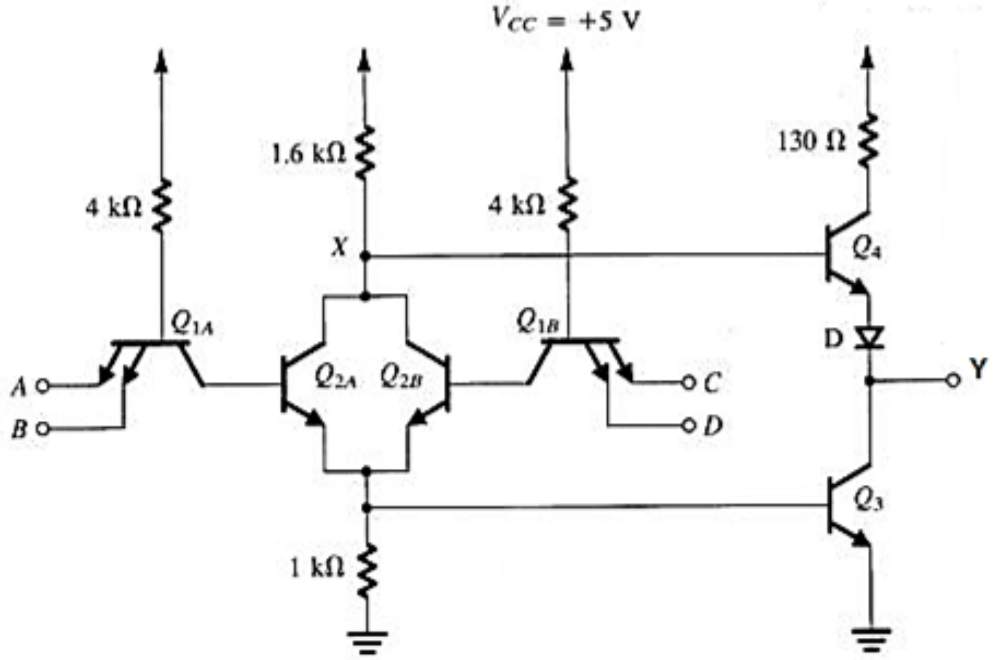
Time limit (10 min.)

Questions

1. (a) Find the minimum number of 2-input NOR gates required to realize the following expression: $A'.B' + X.Y$

   (b) Find the minimum number of 2-input NAND gates required to realize the following expression: $(W' + X')(Y + Z)$

2. The following is an internal schematic of a TTL logic gate. Based on your analysis of the transistor circuit determine the truth table for output Y and obtain the minimized expression for Y using DeMorgan's Theorem.

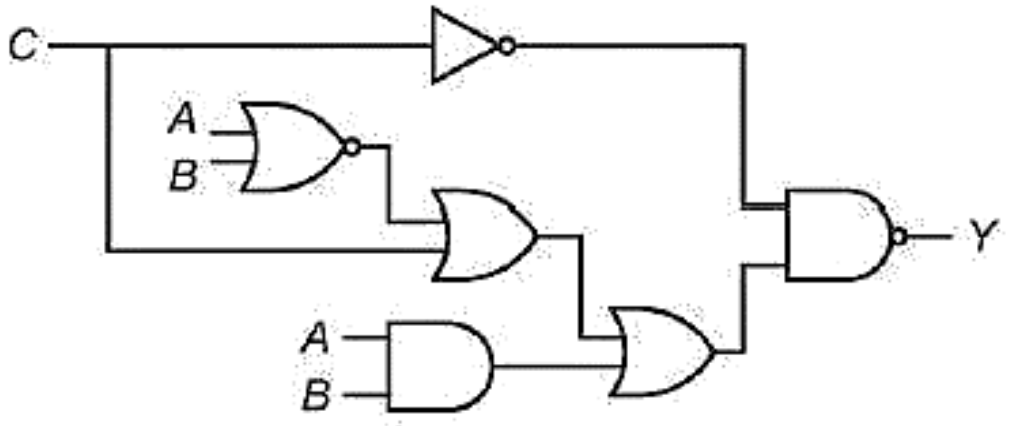


Time limit (10 min.)

Questions

3. For a given logic family, consider V_{OL} = 0.9 V and V_{OH} = 4.5 V . For a given circuit, V_{IL} = 1.2 V and V_{IH} = 3.2 V. Find the noise margins (NM_L, NM_H), transition width and logic swing. Is it functionally better than a circuit with V_{IL} = 1.5 V and V_{IH} = 3 V ?
4. (a) Reduce the Boolean expression: Y=A'B(D'+C'D)+B(A+A'CD)

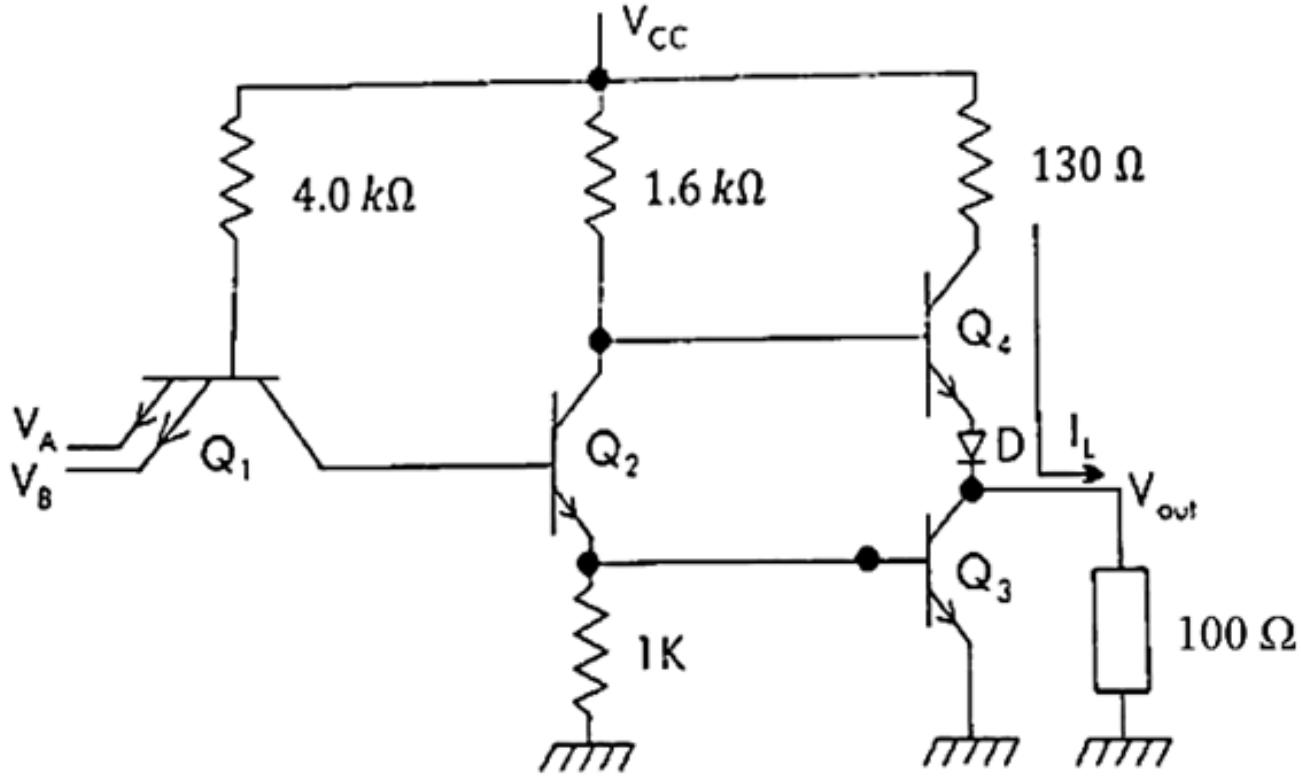
   (b) In the circuit shown in the following figure, if C=0, find the expression for Y?



Time limit (5 min.)

Questions

Q.5. For the 2-input TTL NAND gate, $V_{cc} = 5\,V$ and a $100\,\Omega$ load is connected to its output. Consider $V_{CE(sat)} = 0.3\,V$ and the current gain $h_{FE} = 50$ for any of the transistors. Consider the diode drop in forward bias $V_D = 0.7\,V$. The output voltage when both inputs are 0V is (i)_____ and when both inputs are 5V is (ii) _____ respectively.



Solution 1(a)

- Find the minimum number of 2-input NOR gates required to realize the following expression: A'.B'+X.Y

- A'B' + XY

  = (A'B'+X)(A'B'+Y) (Distributive Property)

  = ((A'B'+X)'+(A'B'+Y)')' (De Morgan's law)

  = (((A+B)'+X)'+((A+B)'+Y)')'

  ⇨ 4 NOR gates required

Solution 1(b)

- Find the minimum number of 2-input NAND gates required to realize the following expression: (W'+X')(Y+Z)

- (W'+X')(Y+Z)

  = (W'+X')Y+(W'+X')Z (Distributive law)

  = [((W'+X')Y+(W'+X')Z)']'

  = [((W'+X')Y)'.((W'+X')Z)']' (De Morgan's theorem)

  = [((WX)'Y)'.((WX)'Z)']'

  ⇨ 4 NAND gates required

Solution 2

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	ϕ	0

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D}$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C} + \bar{A}BC\bar{D} + A\bar{B}\bar{C} + A\bar{B}C\bar{D}$$

$$= \bar{A}\bar{B}(\bar{C} + C\bar{D}) + \bar{A}B(\bar{C} + C\bar{D}) + A\bar{B}(\bar{C} + C\bar{D})$$

$$= (\bar{C} + C\bar{D})(\bar{A}\bar{B} + \bar{A}B + A\bar{B})$$

$$= (\bar{C} + \bar{D})(\bar{A} + A\bar{B})$$

$$= (\bar{C} + \bar{D})(\bar{A} + \bar{B})$$

$$= \overline{CD}\ \overline{AB}$$

Solution 3

Given, V_{OL} = 0.9 V and V_{OH} = 4.5 V

For 1st circuit, V_{IL} = 1.2 V and V_{IH} = 3.2 V

$NM_L = V_{IL} – V_{OL}$ = 1.2 – 0.9 = **0.3** V

$NM_H = V_{OH} – V_{IH}$ = 4.5 – 3.2 = **1.3** V

Transition width = $V_{IH} – V_{IL}$ = 3.2 – 1.2 =**2** V

Logic swing = $V_{OH} – V_{OL}$ = 4.5 – 0.9 = **3.6** V

For 2nd circuit, V_{IL} = 1.5 V and V_{IH} = 3 V

$NM_L = V_{IL} – V_{OL}$ = 1.5 – 0.9 = **0.6** V

$NM_H = V_{OH} – V_{IH}$ = 4.5 – 3 = **1.5** V

No, the 2nd circuit is functionally better than the 1st circuit due to its higher noise margins.

Solution 4 (a)

$$
\begin{aligned}
Y &= A'B(D'+C'D)+B(A+A'CD) \\
&= A'B(D'+C')+B(A+CD) \\
&= B[A'(D'+C')+(A+CD)] \\
&= B[A'D'+(A'C'+A)+CD] \\
&= B[A'D'+(A+C')+CD] \\
&= B[(A'D'+A)+(C'+CD)] \\
&= B[(A+D')+(C'+D)] \\
&= B[A+(D'+D)+C'] \\
&= B[A+1+C'] \\
&= B
\end{aligned}
$$

Solution 4 (b)

$Y = (1.((A+B)'+AB))'$

APPLY DE MORGANS LAW

$Y=(A'B'+AB)'$

$Y=(A \text{ XNOR } B)'$

$Y=(A \text{ XOR } B)$

$Y=AB'+A'B$

Solution 5

When both inputs are LOW, the output is HIGH (Q3 is ON but Q2 and Q4 are OFF).

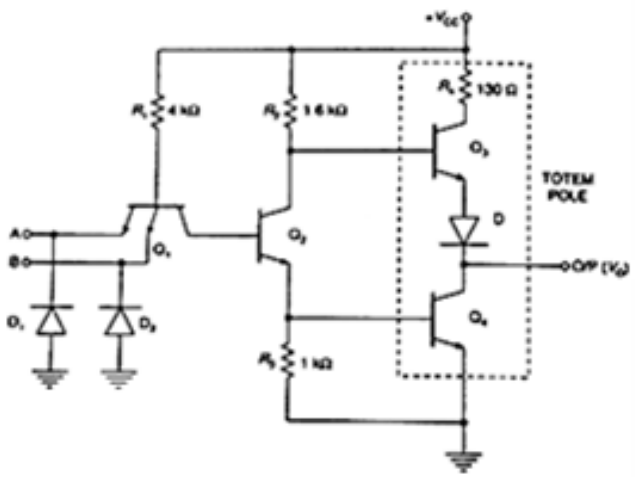
Applying KVL,

$$V_{CC} = I_L R_4 + V_{CE(sat)} + V_D + I_L R_L$$

$$I_L = \frac{V_{CC} - V_{CE(sat)} - V_D}{R_L + R_4}$$

Substituting the values, we get $I_L = \quad 17.39\,mA$

Hence, $V_0 = I_L R_L = \ 1.739\,V$



When both inputs are HIGH, i.e. 5V:

For open load,

Q3 is OFF.Q2 and Q4 in saturation. **For open load, $I_{C4} \approx 0$. That makes Q_4 go deep in saturation i.e. $V_O = V_{CE} \approx 0$.**

For resistive load, R_L

If a voltage drop exists across R_L (i.e. $V_0 > 0$), then a current has to flow through it. This current has to be sourced by the Q4 transistor, i.e. the current has to flow out of the collector terminal through R_L. However, this is not possible since Q4 is an npn transistor and its collector can only sink current. Hence, the output voltage V_0 is maintained at 0, i.e. $V_0 = 0$.