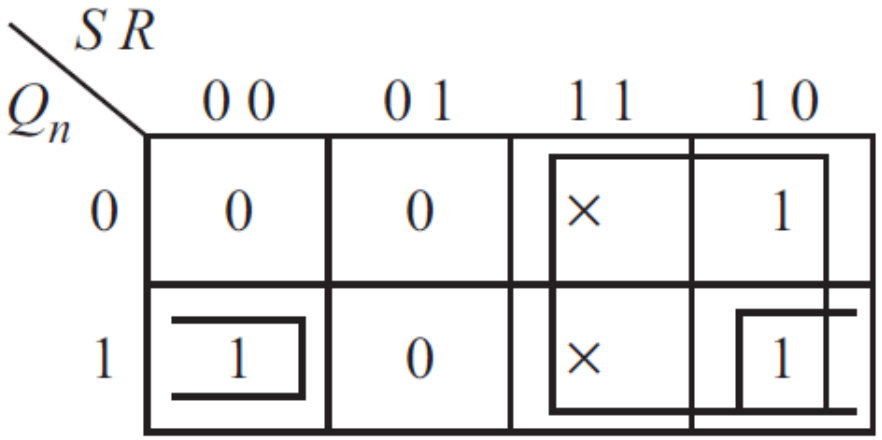
Digital Electronic Circuits
Section 1 (EE, IE)

Lecture 21

Class Test 2:
29-10-2020 (THU): 8:00 – 8:55 AM
Syllabus: Logic families (not covered in CT1) and primarily post CT1, shall include concept dealt in pre-CT1 part which forms the pre-requisite.

Characteristic Equation: *SR*

S	*R*	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	N.A.
1	1	1	N.A.

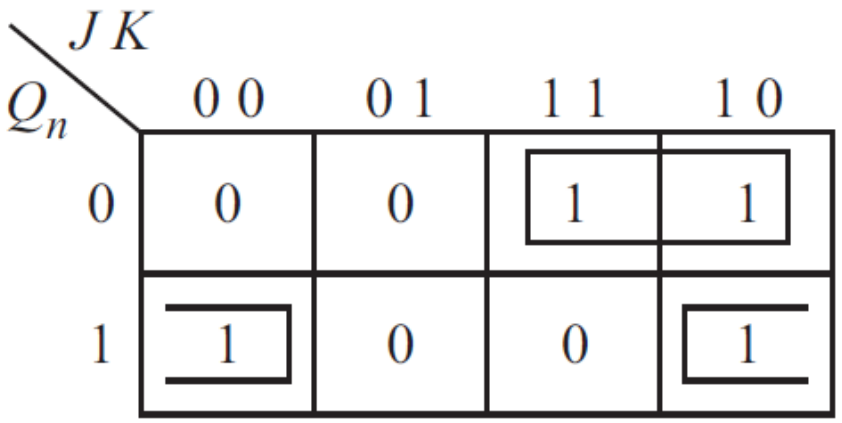


$$Q_{n+1} = S + \overline{R}\,Q_n$$

S	*R*	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	N.A.

Characteristic Equation: *JK*

J	*K*	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

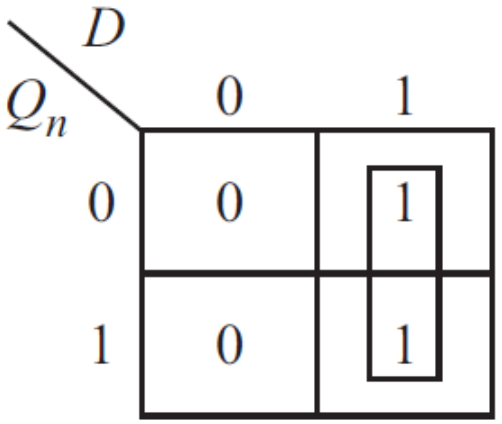


$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

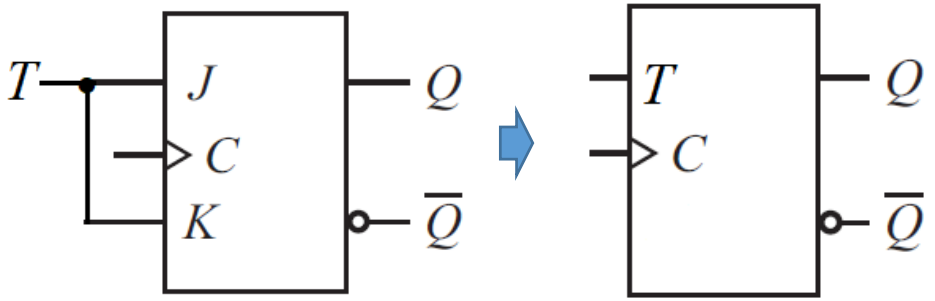
J	*K*	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n'

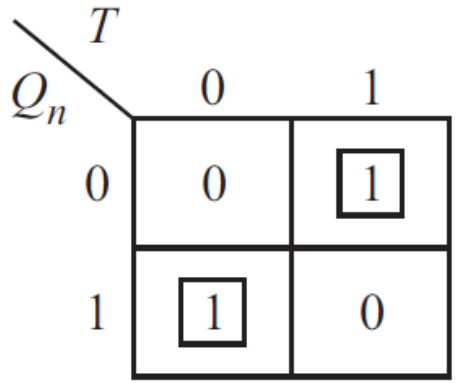
Characteristic Equation: *D* and *T*

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



$$Q_{n+1} = D$$





$$Q_{n+1} = T\overline{Q}_n + \overline{T}Q_n$$

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table: *SR*

- It presents what input should be placed to cause a specific transition of the Flip-Flop when clock triggers.
- It can be obtained from Flip-Flop Truth Table.

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	N.A.

Consider *SR* Flip-Flop with $Q_n = 0$
If $SR = 00$, $Q_{n+1} = 0$
If $SR = 01$, $Q_{n+1} = 0$
i.e. if $SR = 0X$, $Q_{n+1} = 0$

Therefor for *SR* FF,
If $Q_n \rightarrow Q_{n+1} = 0 \rightarrow 0$
then its input *SR* before clock trigger
SR = 00 or 01 i.e. 0X

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Excitation Table of *SR* Flip-Flop

Excitation Table: *JK*, *D* and *T*

$Q_n \rightarrow Q_{n+1}$		J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

$Q_n \rightarrow Q_{n+1}$		D
0	0	0
0	1	1
1	0	0
1	1	1

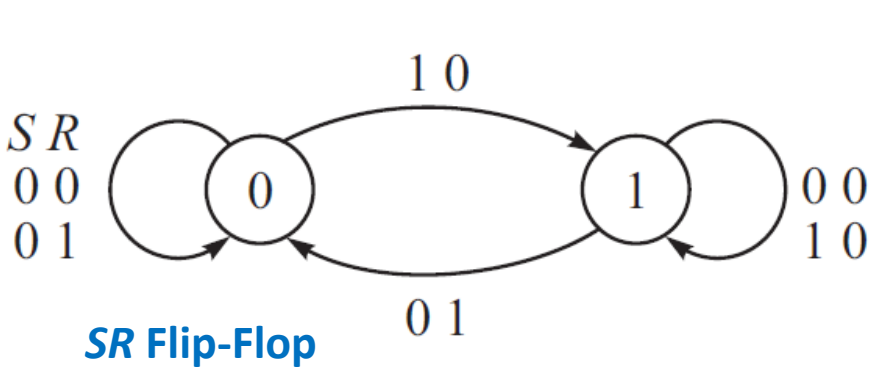
$Q_n \rightarrow Q_{n+1}$		T
0	0	0
0	1	1
1	0	1
1	1	0

J	*K*	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n'

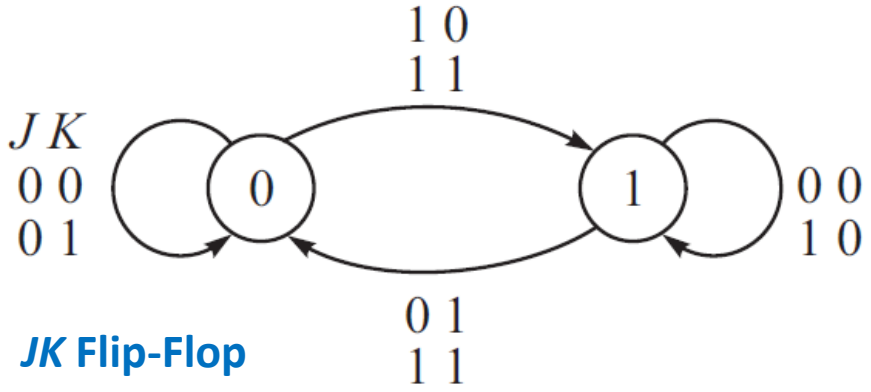
D	Q_{n+1}
0	0
1	1

T	Q_{n+1}
0	Q_n
1	Q_n'

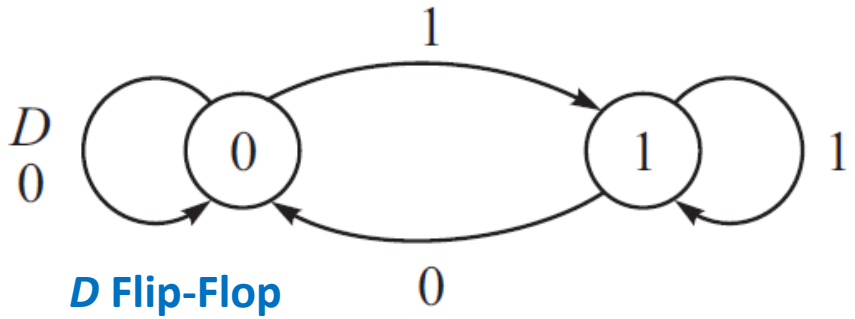
State Transition Diagram



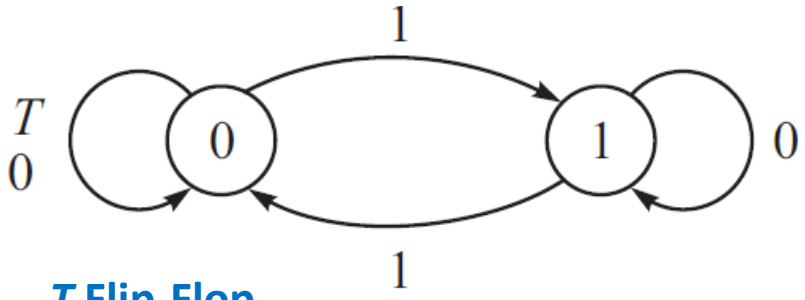
SR Flip-Flop



JK Flip-Flop



D Flip-Flop



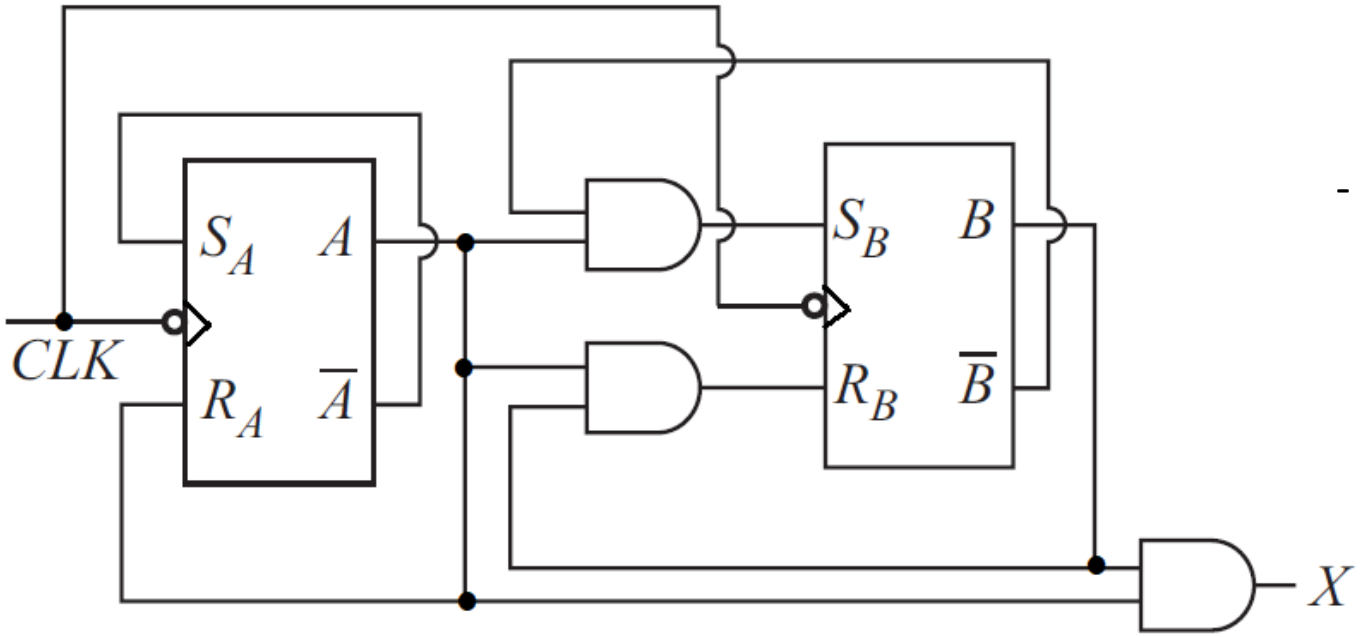
T Flip-Flop

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

It can be directly obtained from excitation table.

An Example

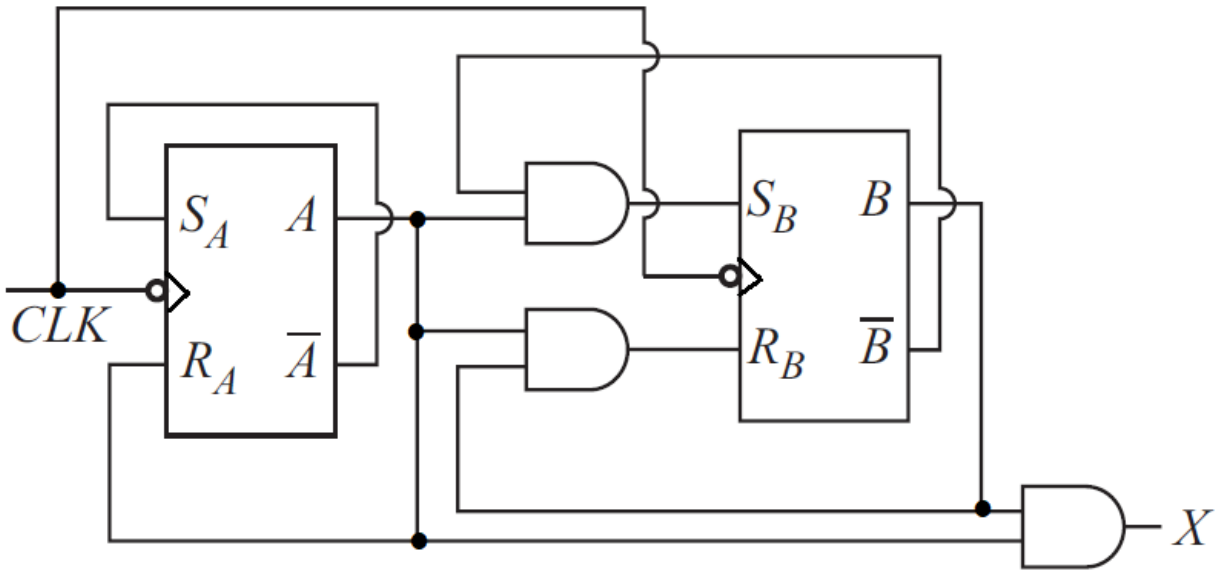
- To analyse the circuit and find how states change with the input clock and how output is generated.



Note that,

- for the basic logic gate part of the circuit, output will be considered as immediately available when input is presented and
- for the flip-flop / memory element part of the circuit, its output change as per **Truth Table / Characteristic Eqn.** waits till the clock trigger.
- Basic gate delay is negligible compared to clock time period. Effect of those delay will be considered later.

Defining Flip-Flop Inputs and Output



For Flip-Flop *A*,

$S_A = A_n'$

$R_A = A_n$

For Flip-Flop *B*,

$S_B = A_n.B_n'$

$R_B = A_n.B_n$

For Output,

$X = A_n.B_n$

State Analysis Table

	Current State		Current Flip-Flop Input				Next State		Output
CLK	B_n	A_n	S_B	R_B	S_A	R_A	B_{n+1}	A_{n+1}	X
0	0	0	0	0	1	0	0	1	0
1	0	1	1	0	0	1	1	0	0
2	1	0	0	0	1	0	1	1	0
3	1	1	0	1	0	1	0	0	1
4	0	0	0	0	1	0	0	1	0
5	0	1			…				

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	N.A.

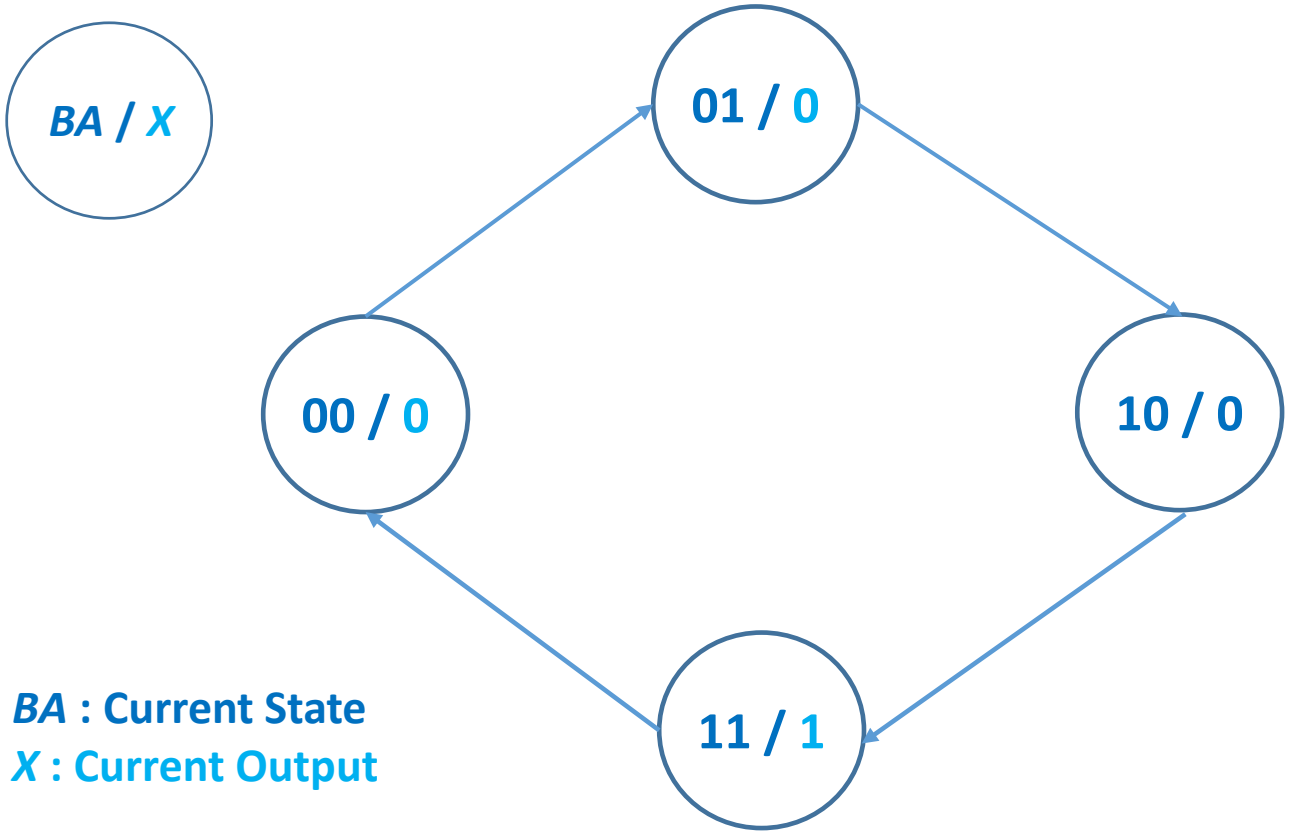
$S_A = A_n'$
$R_A = A_n$

$X = A_n.B_n$

$S_B = A_n.B_n'$
$R_B = A_n.B_n$

- Clock 0: The initial state is assumed to be 0 for each flip-flop.
- Clock *n*: Next state of clock (*n* – 1) is the present state at clock *n* and the circuit evolves.
- State transition as per Flip-Flop Truth Table for the input present.

Analysis Result



***BA* : Current State**
***X* : Current Output**

The circuit generates an **output = 1** at **every 4th clock** trigger when it reaches the state ***BA* = 11** and repeats the state transition
00 → 01 → 10 → 11 → 00 → …

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill