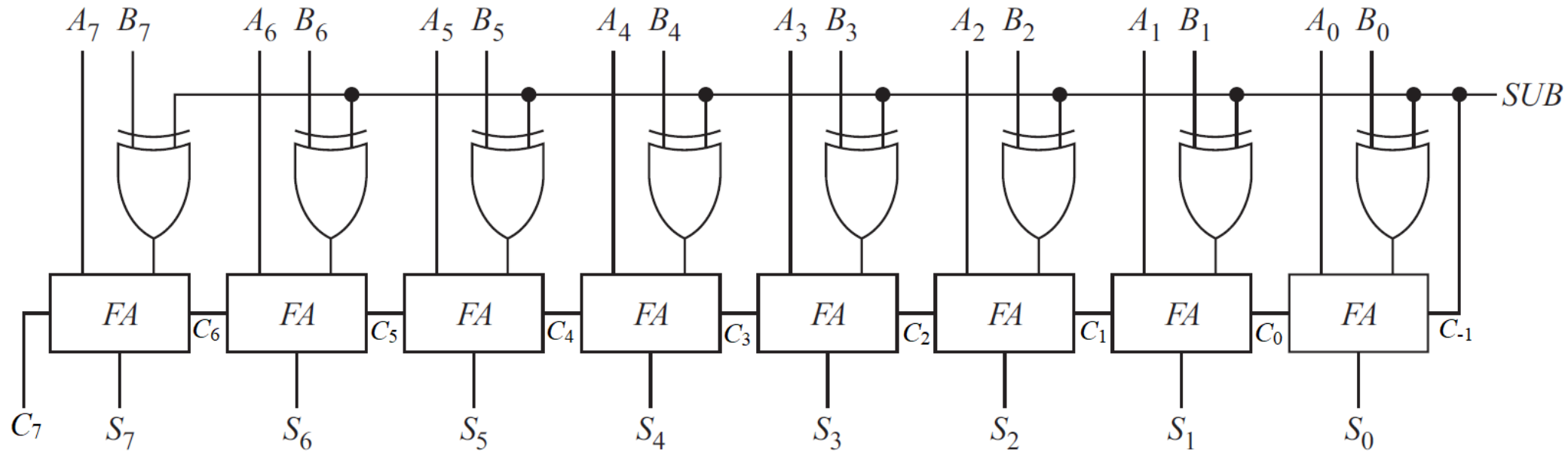


# **Digital Electronic Circuits**

## **Section 1 (EE, IE)**

### **Lecture 16**

# Adder – SubtractOr Circuit



If  $SUB = 0$ , then  $C_{-1} = 0$

Ex-OR gate output =  $B_i \oplus 0 = B_i$

F.A. output =  $A + B$

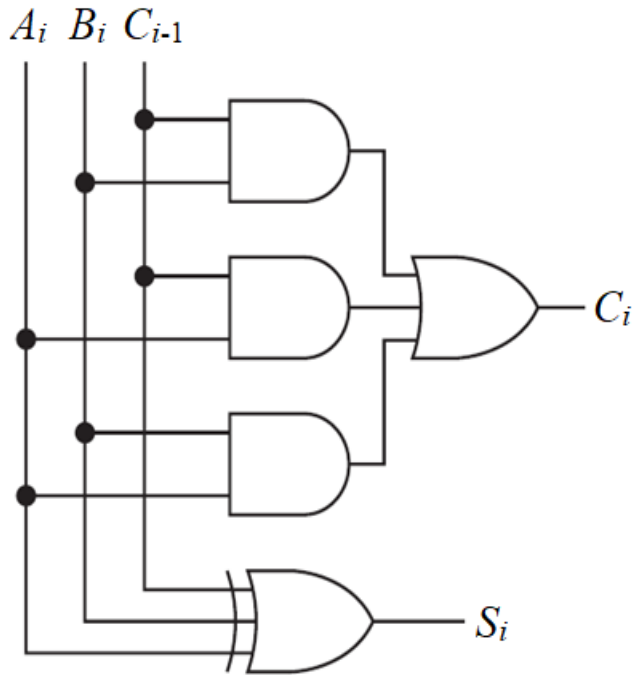
If  $SUB = 1$ , then  $C_{-1} = 1$

Ex-OR gate output =  $B_i \oplus 1 = B_i'$

F.A. output =  $A + (-B) = A - B$

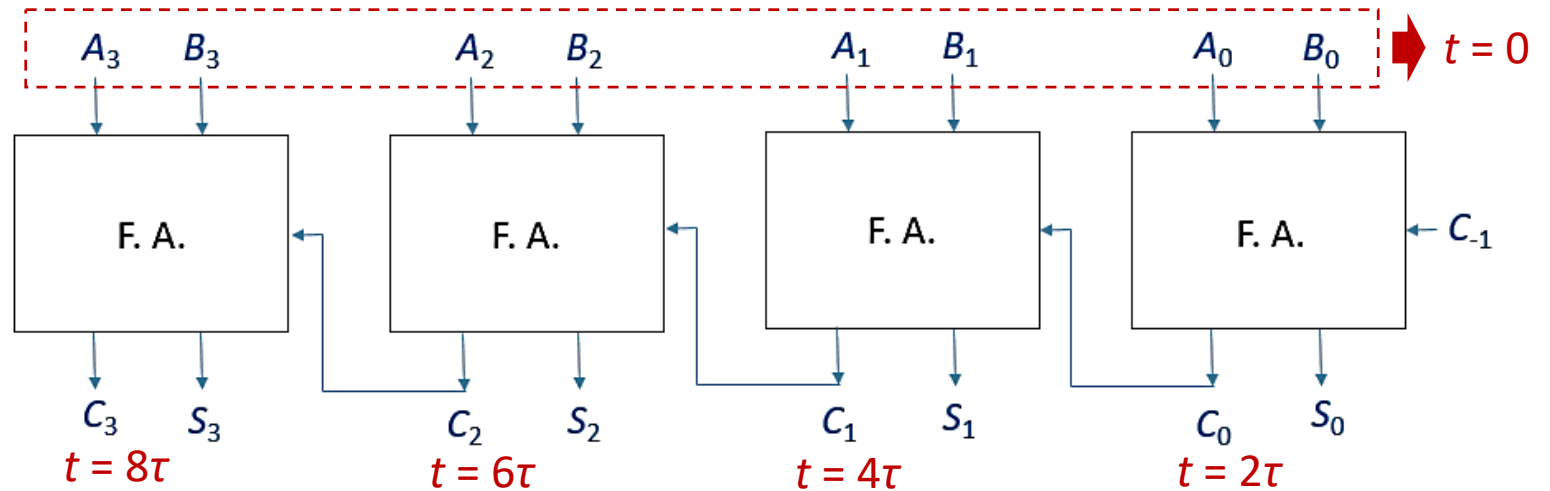
# Delay in Ripple Carry Adder

Propagation delay is cumulative.  
For  $n$ -bit addition,  $2n\tau$  delay.



$$C_i = A_i \cdot B_i + A_i \cdot C_{i-1} + B_i \cdot C_{i-1}$$

$$S_i = A_i \oplus B_i \oplus C_{i-1}$$



Each basic gate delay =  $\tau$   
(AND, OR)

Each Ex-OR gate delay =  $2\tau$

$C_3$  available after  $8\tau$  delay.

For  $S_3$ ,  $A_3 \oplus B_3$  result after  $2\tau$ .

This is Ex-ORed with  $C_2$ .

$C_2$  available after  $6\tau$ .

$S_3$  available after  $8\tau$ .

# Carry: Serial to Parallel

$$C_i = A_i B_i + A_i C_{i-1} + B_i C_{i-1}$$

$$C_i = A_i B_i + C_{i-1}(A_i + B_i)$$

$$C_i = G_i + P_i C_{i-1}$$

Where,  $G_i = A_i B_i$  : **Generation term**  
and  $P_i = A_i + B_i$  : **Propagation term**

$G_i = 1$  : Carry is generated

$P_i = 1$  : Input carry is propagated

$$C_0 = G_0 + P_0 C_{-1} \dots (1)$$

$$C_1 = G_1 + P_1 C_0 \dots (2)$$

Substituting  $C_0$  from Eq.(1) in Eq.(2),

$$C_1 = G_1 + P_1(G_0 + P_0 C_{-1})$$

$$C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{-1} \dots (3)$$

2 parallel AND delay:  $\tau$

1 OR delay :  $\tau$

For  $G_i$  and  $P_i$ , delay :  $\tau$

Total delay :  $3\tau$

# Carry Look Ahead Adder

$$C_2 = G_2 + P_2 C_1 \dots (4)$$

Substituting  $C_1$  from Eq.(3) in Eq.(4),

$$C_2 = G_2 + P_2(G_1 + P_1 G_0 + P_1 P_0 C_{-1})$$

$$C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{-1} \dots (5)$$

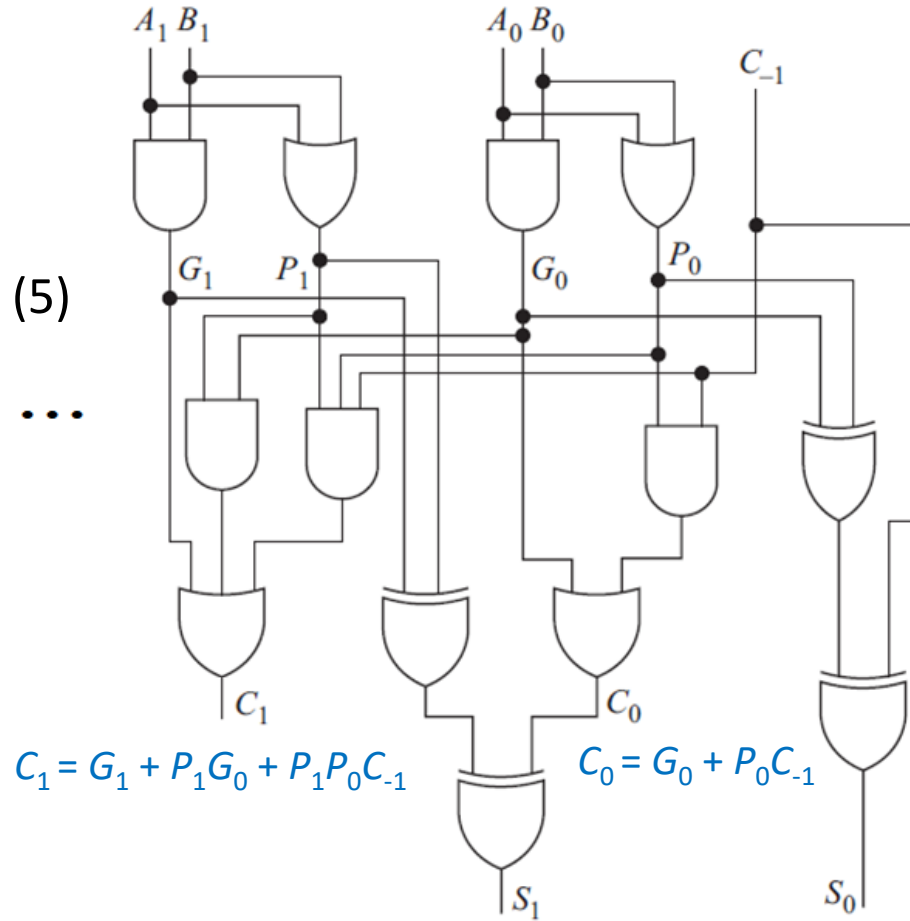
$C_2$  is generated after  $3\tau$  delay, too.

$$C_3 = G_3 + P_3 C_2 \dots (6)$$

From Eq.(5) and Eq.(6)

$$C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{-1} \dots (7)$$

$C_3$  is generated after  $3\tau$  delay, too.



$$S_i = A_i \oplus B_i \oplus C_{i-1}$$

$$S_i = G_i \oplus P_i \oplus C_{i-1}$$

(avoids loading of inputs)

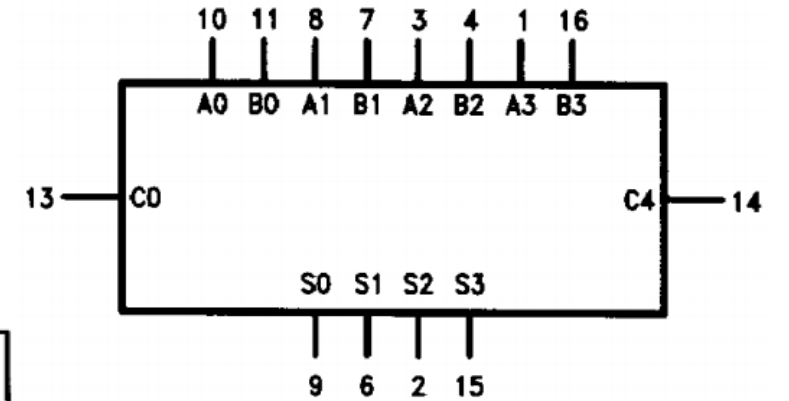
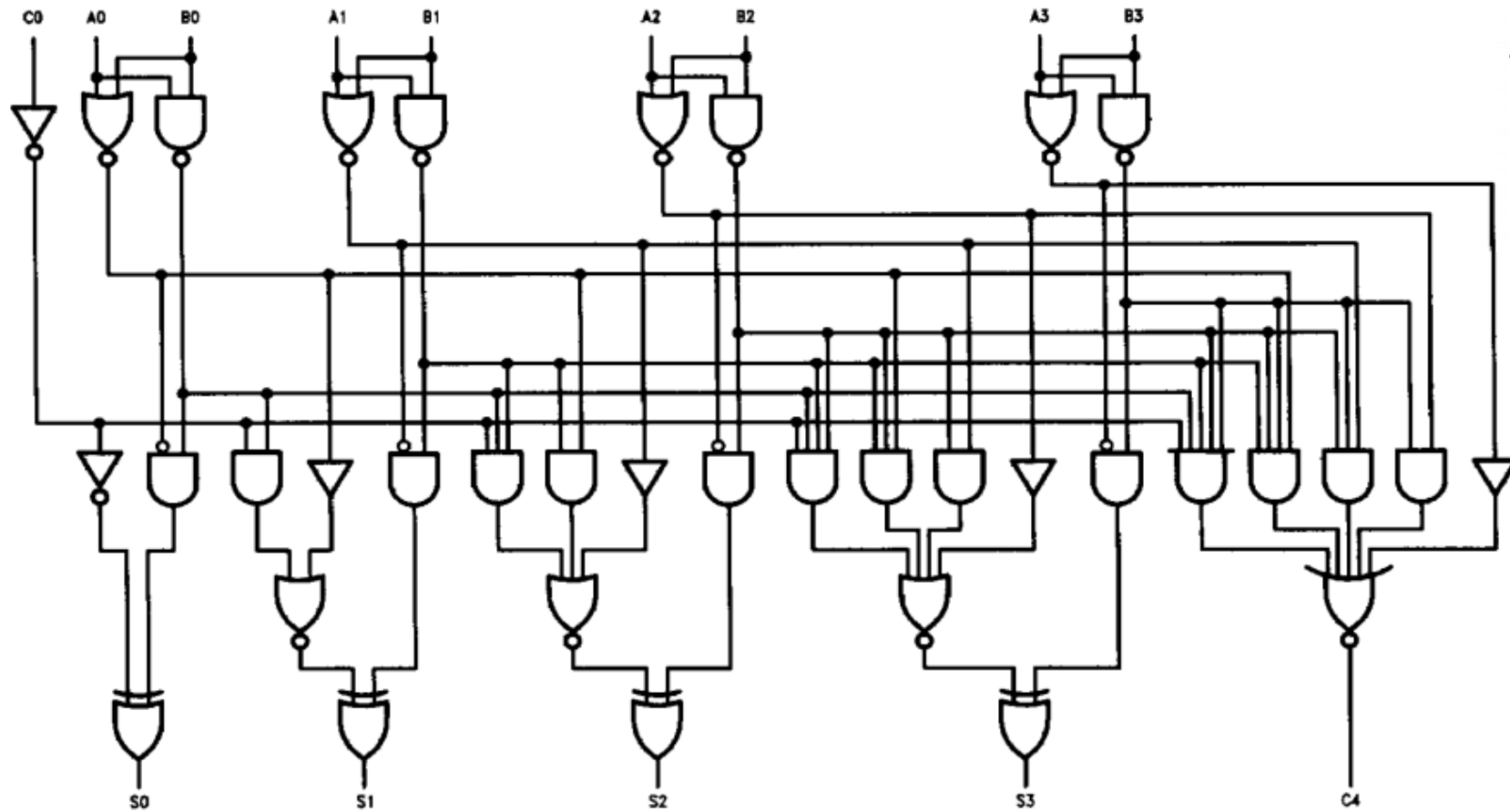
All  $G_i \oplus P_i$  in  $3\tau$

All  $C_{i-1}$  in  $3\tau$

All  $S_i$  in  $3\tau + 2\tau = 5\tau$

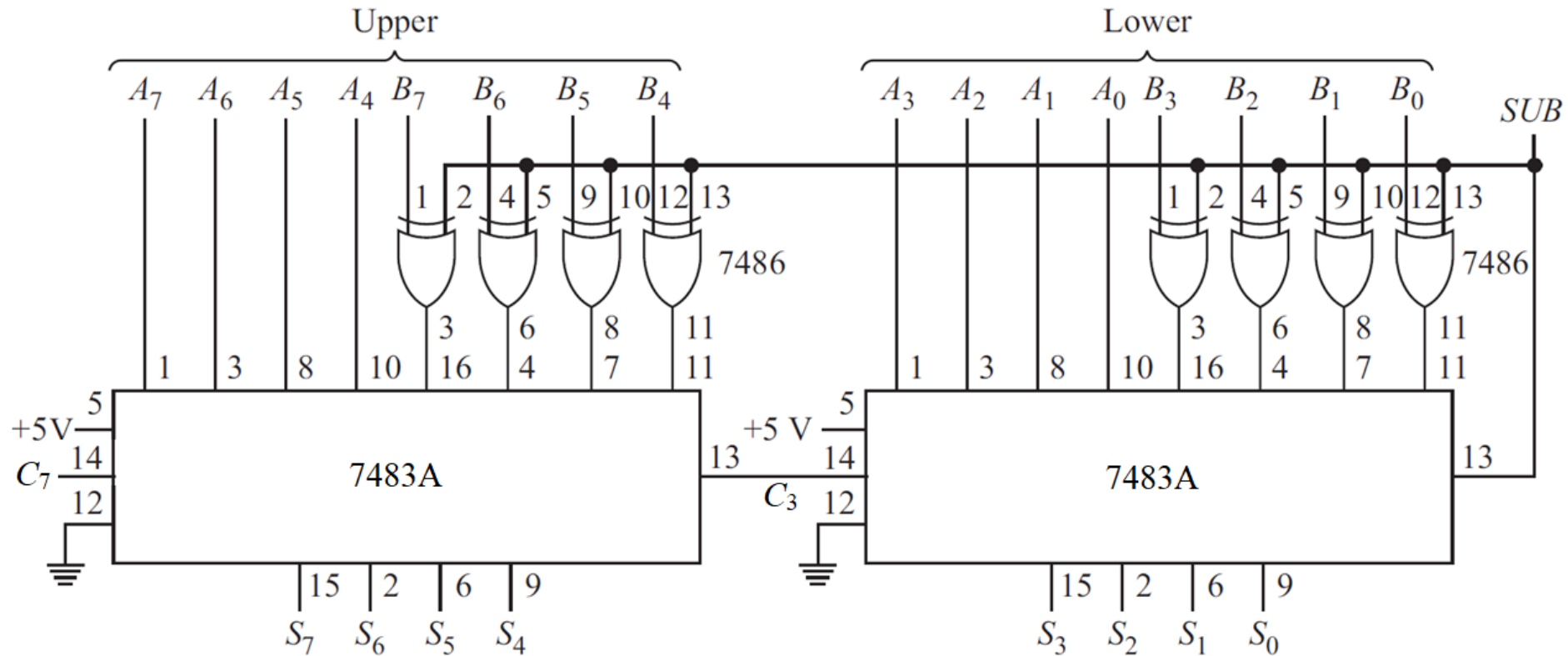
**Delay is not cumulative.**

# IC 7483A



Different manufacturers  
use different notations.

# Addition / Subtraction in Cascade



- Carry ripples from one IC to other.
- Carry look ahead within IC.

# Group Carry Generation and Propagation

$$C_3 = G_3 + P_2G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_{-1}$$

$$G_{3-0} = G_3 + P_2G_2 + P_3P_2G_1 + P_3P_2P_1G_0 : \text{Group Carry Generation term}$$

$$P_{3-0} = P_3P_2P_1P_0 : \text{Group Carry Propagation term}$$

$$C_3 = G_{3-0} + P_{3-0}C_{-1}$$

$$C_7 = G_{7-4} + P_{7-4}C_3$$

$$C_7 = G_{7-4} + P_{7-4}(G_{3-0} + P_{3-0}C_{-1}) = G_{7-4} + P_{7-4}G_{3-0} + P_{7-4}P_{3-0}C_{-1}$$

Similarly,

$$C_{11} = G_{11-8} + P_{11-8}G_{7-4} + P_{11-8}P_{7-4}G_{3-0} + P_{11-8}P_{7-4}P_{3-0}C_{-1}$$

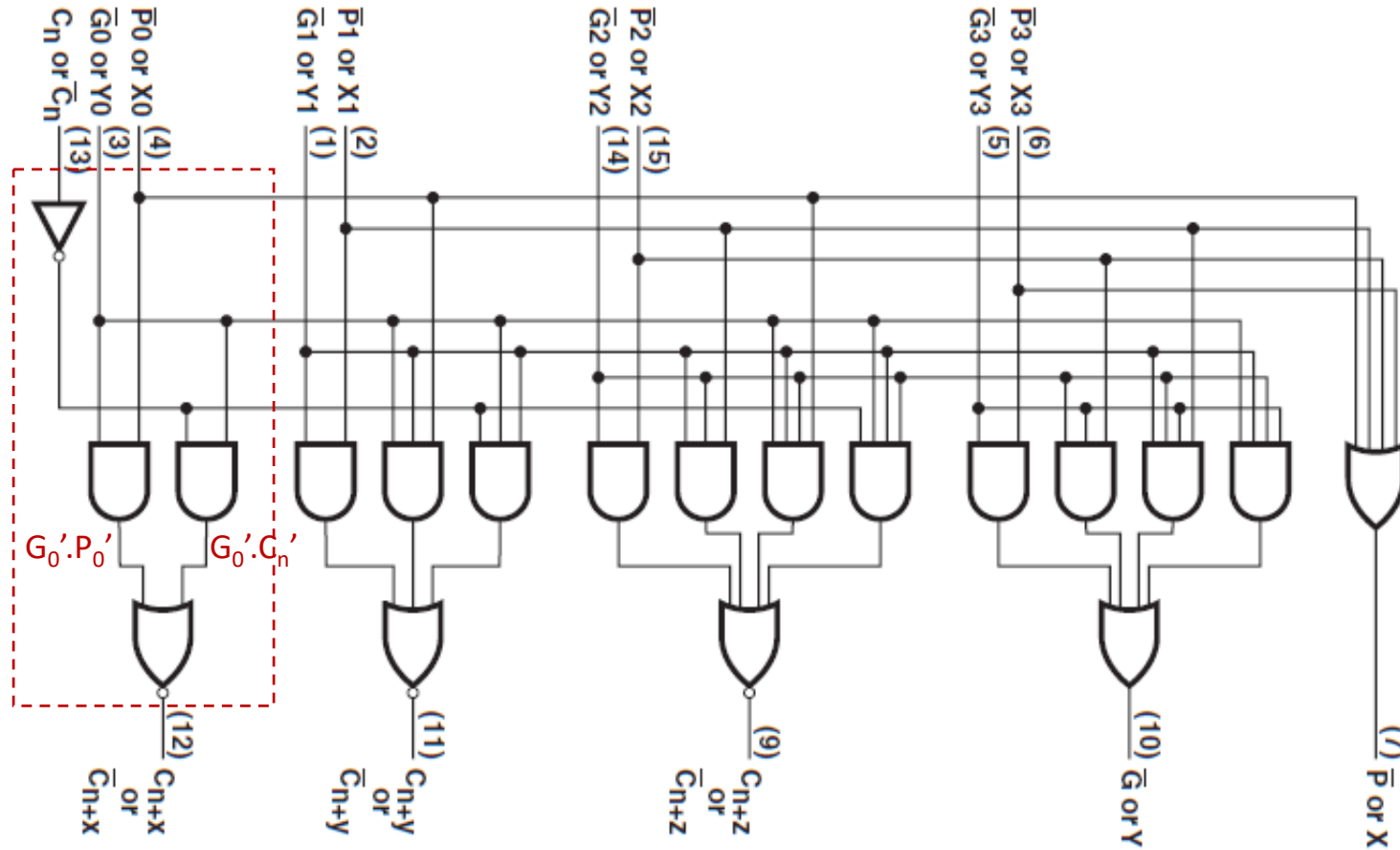
$$C_{15} = G_{15-12} + P_{15-12}G_{11-8} + P_{15-12}P_{11-8}G_{7-4} + P_{15-12}P_{11-8}P_{7-4}G_{3-0} \\ + P_{15-12}P_{11-8}P_{7-4}P_{3-0}C_{-1}$$

$G_{(i+3)-i}$  : in  $3\tau$  and  $P_{(i+3)-i}$  : in  $2\tau$

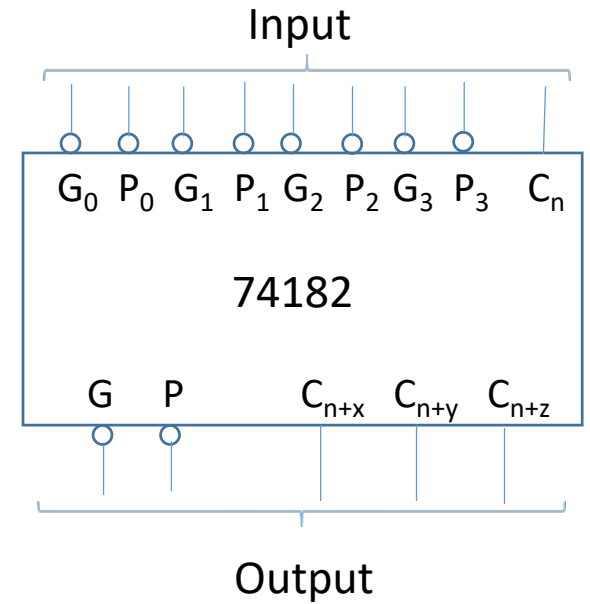
Carry look ahead: in  $5\tau$



# Look Ahead Carry Generator



$$\begin{aligned}
 C_{n+x} &= (G_0' \cdot P_0' + G_0' \cdot C_n')' \\
 &= (G_0' \cdot P_0')' \cdot (G_0' \cdot C_n')' \\
 &= (G_0 + P_0) \cdot (G_0 + C_n) \\
 &= G_0 + G_0 C_n + G_0 P_0 + P_0 C_n \\
 &= G_0 (1 + C_n + P_0) + P_0 C_n \\
 &= G_0 + P_0 C_n
 \end{aligned}$$



# Overflow Detection for Adder

$  \begin{array}{r}  A_3A_2A_1A_0 \\  B_3B_2B_1B_0 \\  \hline  [C_3] \ S_3S_2S_1S_0  \end{array}  $		<div>+ve with +ve :</div> <div> <div>0010 (2)      0010 (2)</div> <div>0011 (3)      0111 (7)</div> <div>-----</div> <div>0101 (5)      1001 (-7)</div> <div>Overflow</div> </div>		<div>Overflow Flag: O</div> <div> <math display="block">  \begin{aligned}  O &amp;= A_3'B_3'S_3 + A_3B_3S_3' \\  &amp;= C_3 \oplus C_2  \end{aligned}  </math> </div>	
<div>0000 : 0      1000 : -8</div> <div>0001 : 1      1001 : -7</div> <div>0010 : 2      1010 : -6</div> <div>0011 : 3      1011 : -5</div> <div>0100 : 4      1100 : -4</div> <div>0101 : 5      1101 : -3</div> <div>0110 : 6      1110 : -2</div> <div>0111 : 7      1111 : -1</div>		<div>-ve with -ve :</div> <div> <div>1110 (-2)      1110 (-2)</div> <div>1101 (-3)      1001 (-7)</div> <div>-----</div> <div>± 1011 (-5)      ± 0111 (7)</div> <div>Overflow</div> </div>		<div>± 0111 (7)</div> <div>1110 (-2)</div> <div>-----</div> <div>± 0101 (5)</div> <div>± 0010 (2)</div> <div>1001 (-7)</div> <div>-----</div> <div>1011 (-5)</div> <div>+ve with -ve :</div>	
<div>Range: -8 to +7</div>					

## References:

- ❑ Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill