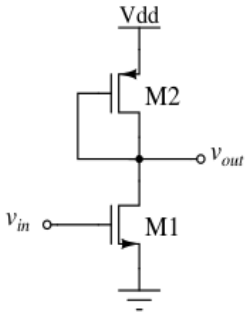
EE 660 VLSI Design Laboratory

Assignment II

Submitted by: L.Sri Sai Swathi (2414202)

1. Design an NMOS common-source amplifier with a PMOS diode-connected load as shown in Fig. 1. The amplifier should have an absolute voltage gain of 3. You can make use of UMC65 models and choose the minimum device size as 2 µm/60 nm. Create a symbol for the amplifier.



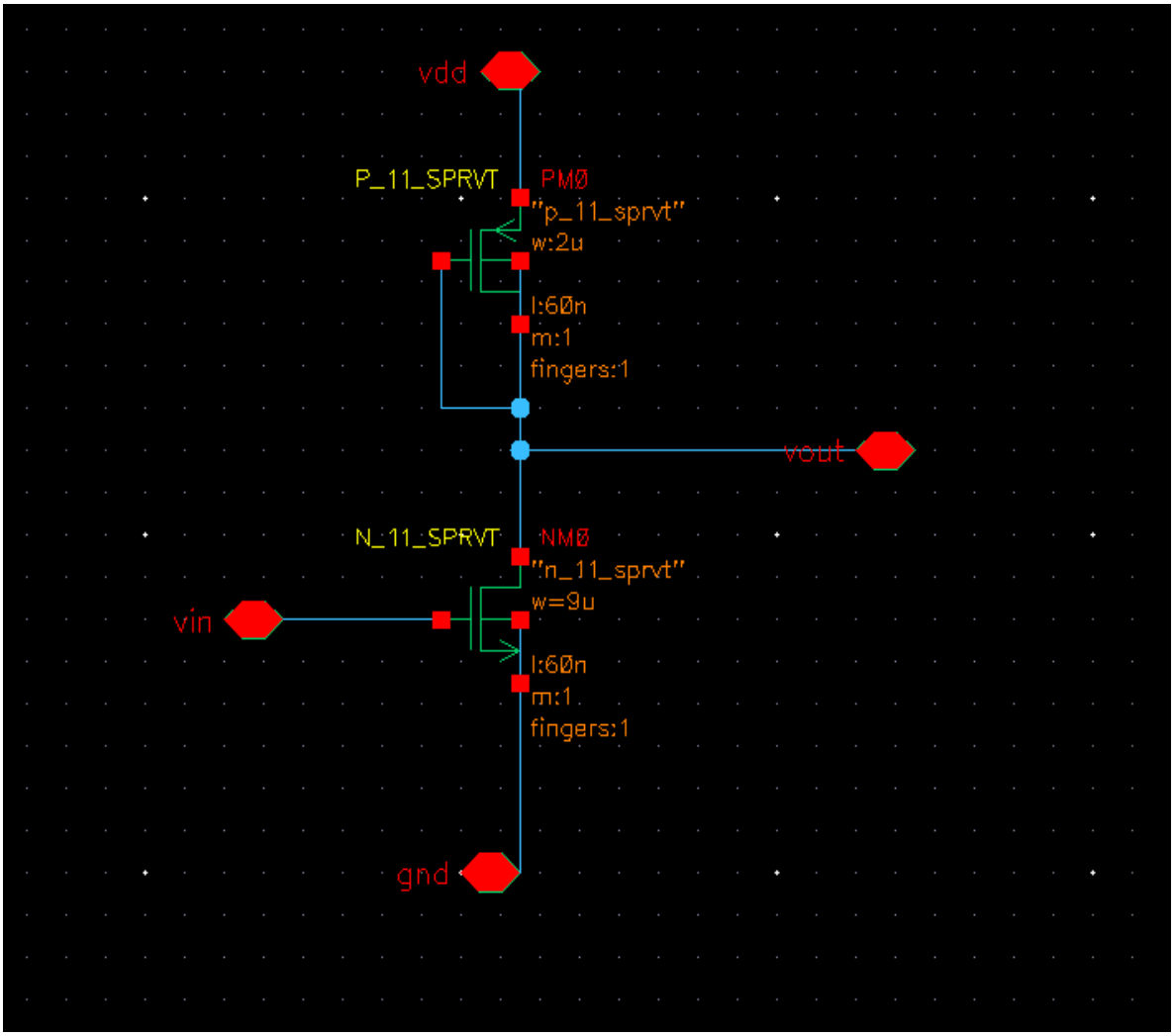


Figure : Schematic of CS Amplifier with PMOS diode connected load

2. Create a test bench and instantiate the amplifier in it. Do a large signal analysis of the circuit by doing a DC sweep of the input voltage from 0 to V DD (1.1 V). Decide the input common-mode voltage at the centre of the region where both M1 and M2 are in saturation.

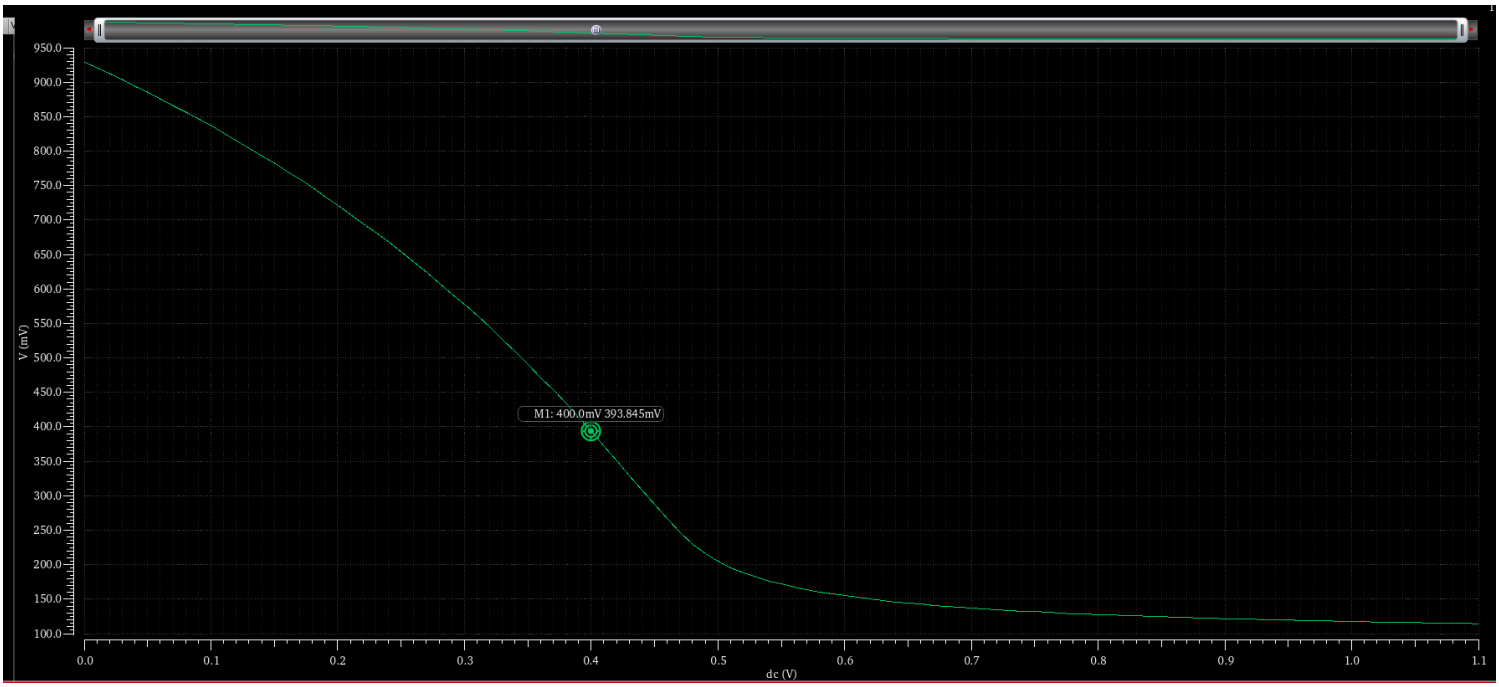
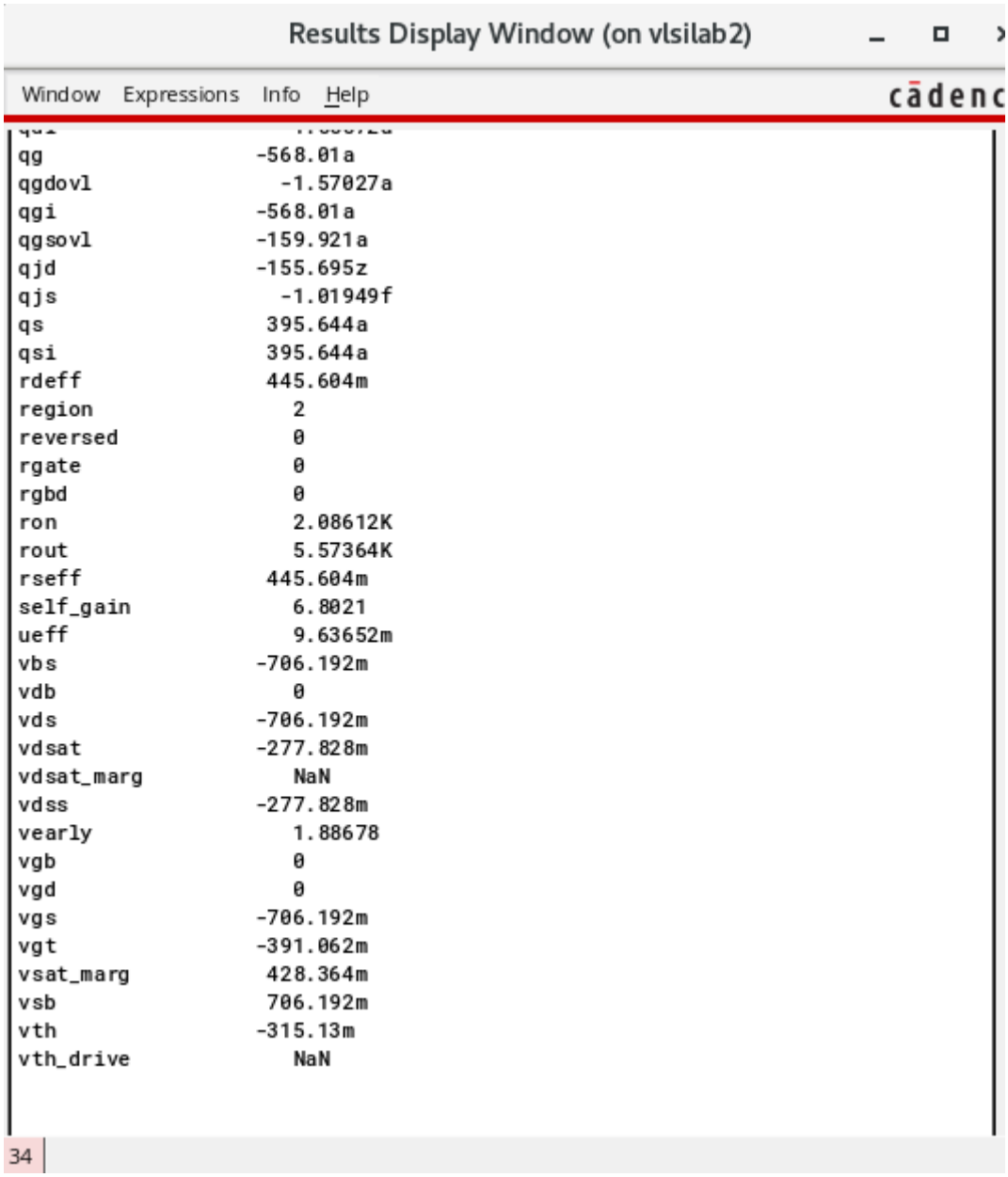


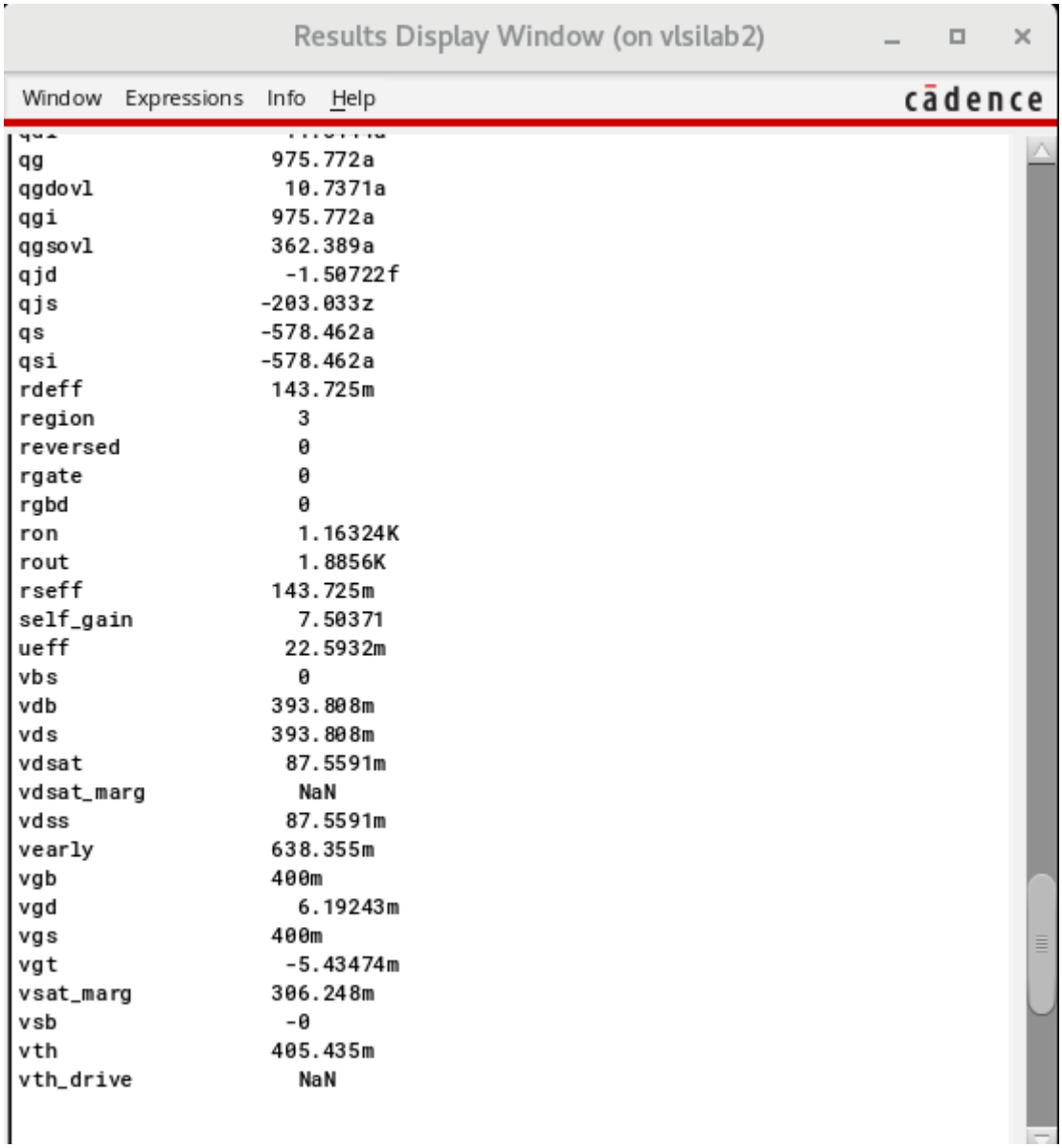
Figure: Plot showing Vout vs Vin

From the plot , Assumed 0.4v as common mode voltage and verified as follows:-

Below is the simulation result of DC operating point analysis. It shows that PMOS is in **region 2** of operation which means “Saturation region”. It is also noted that **|Vtp| =0.315v.**



Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 3 of operation which means “Cuttoff region”. It is also noted that **Vtn =0.405v.**



Observation : Since both transistors are not in saturation when we chose VGS as 400mV , we are choosing another value **420mV** which is greater than both **vtn and vtp**.

3. Connect a sinusoidal source at the input with an amplitude of 10 mV and a 500 fF capacitive load at the output.

(a) Perform a DC operating point analysis to verify that the transistors are in saturation.

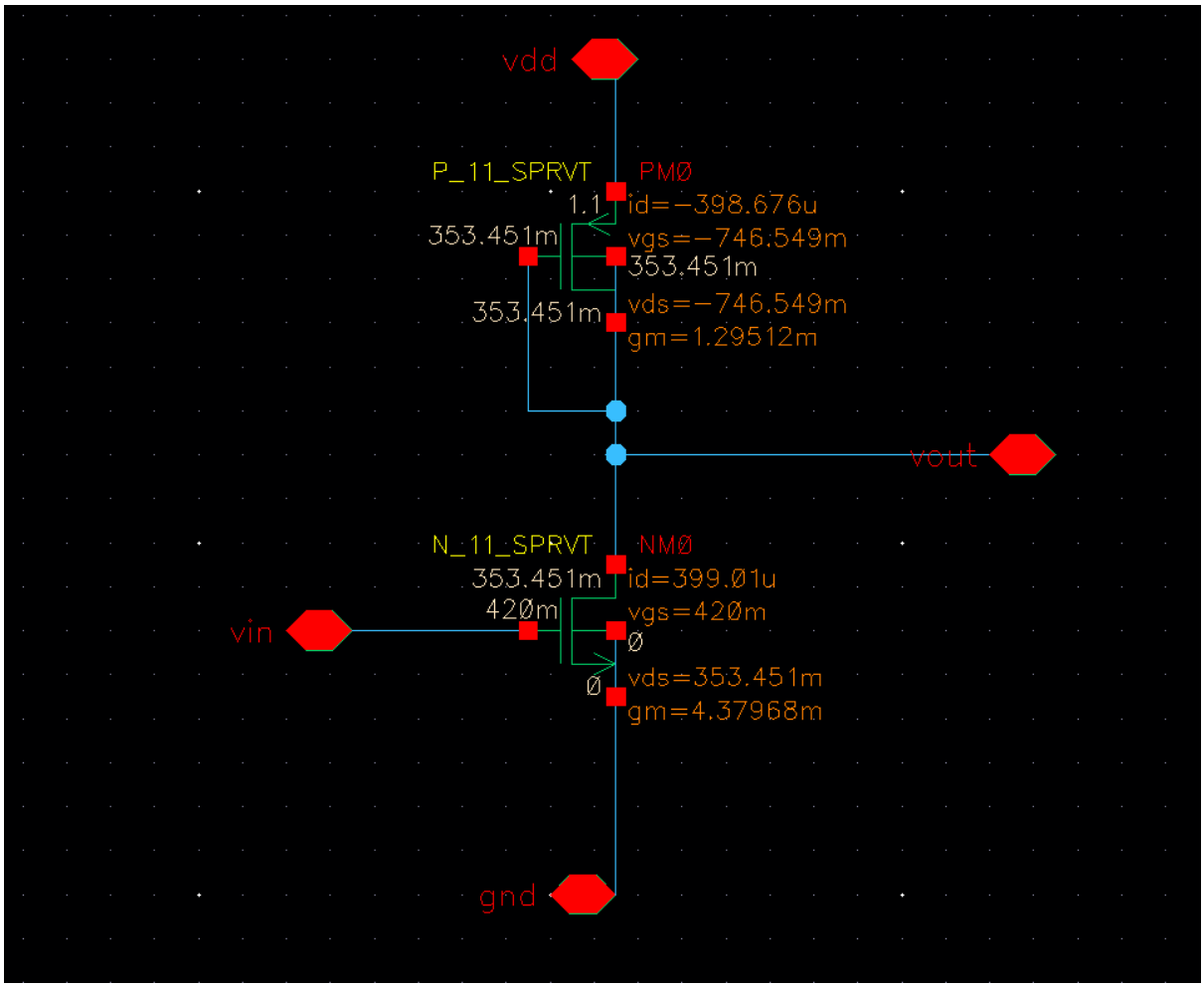
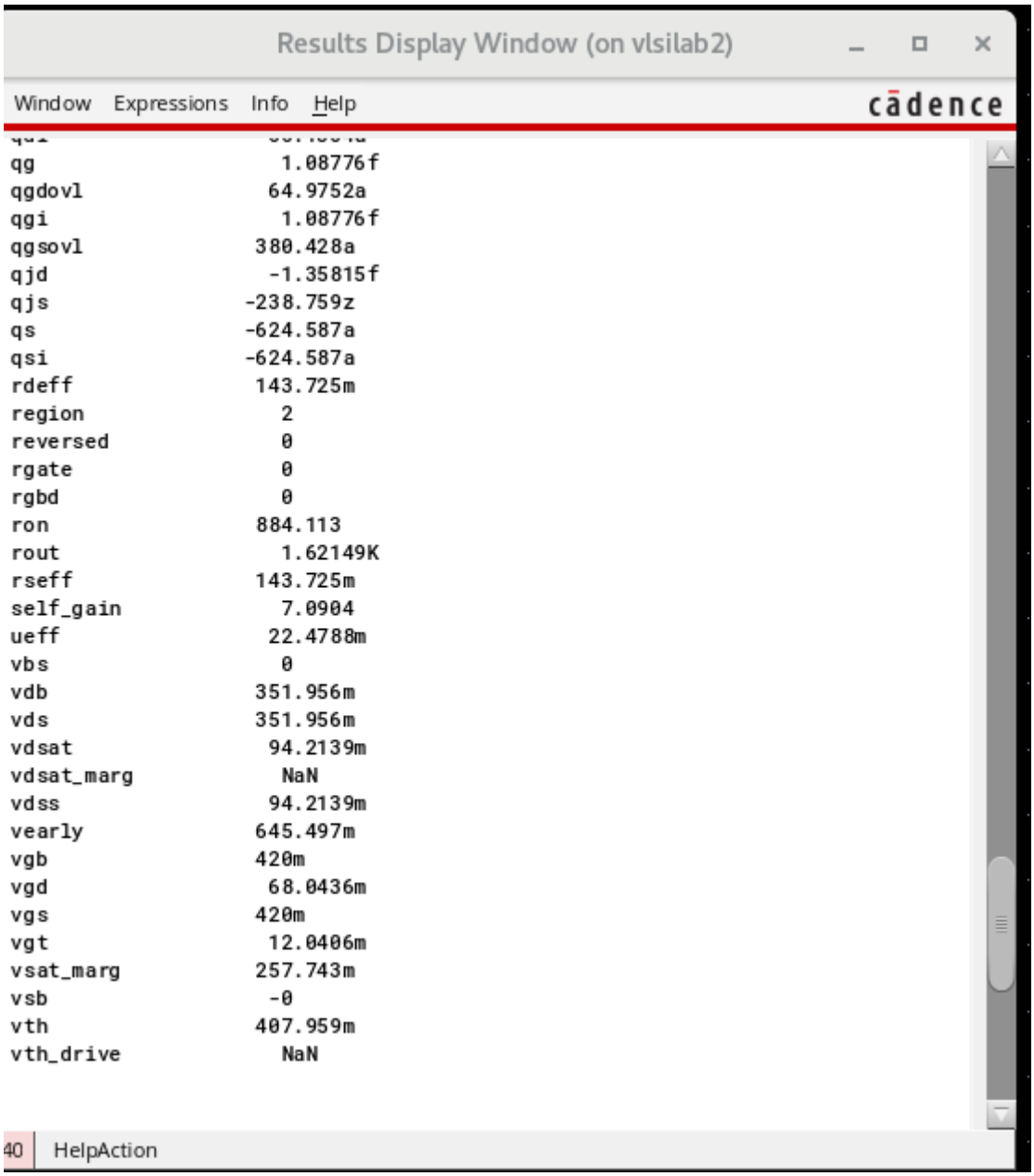


Figure: Schematic showing all the DC operating point voltages and currents

Below is the simulation result of DC operating point analysis. It shows that NMOS is in **region 2** of operation which means “Saturation region”.



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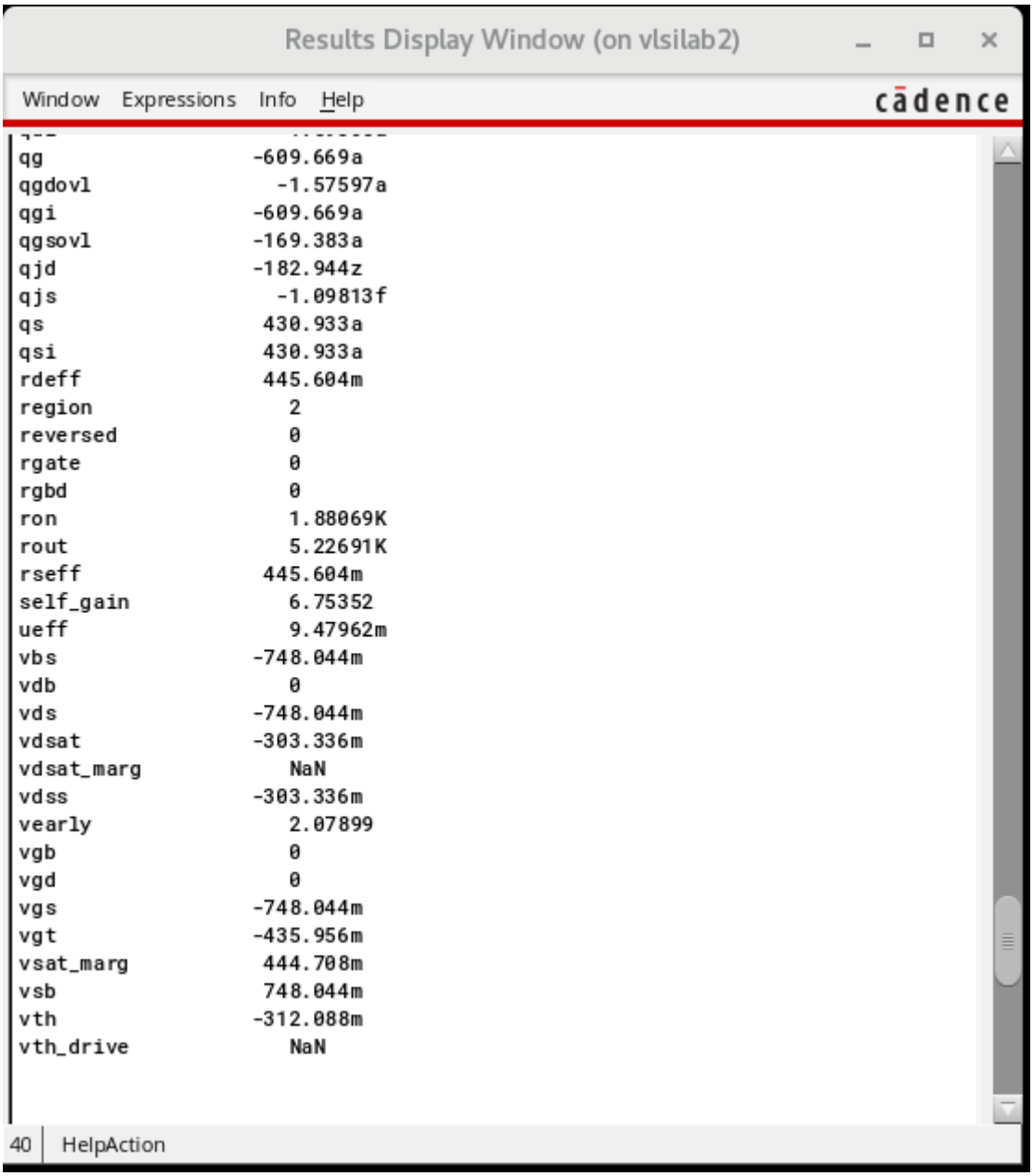


Observation: From the above analysis it’s been verified that 2 transistors are in Saturation region of operation when Vgs=420mV.

b)Perform a transient analysis of the circuit and verify that the input and output waveforms are out of phase.

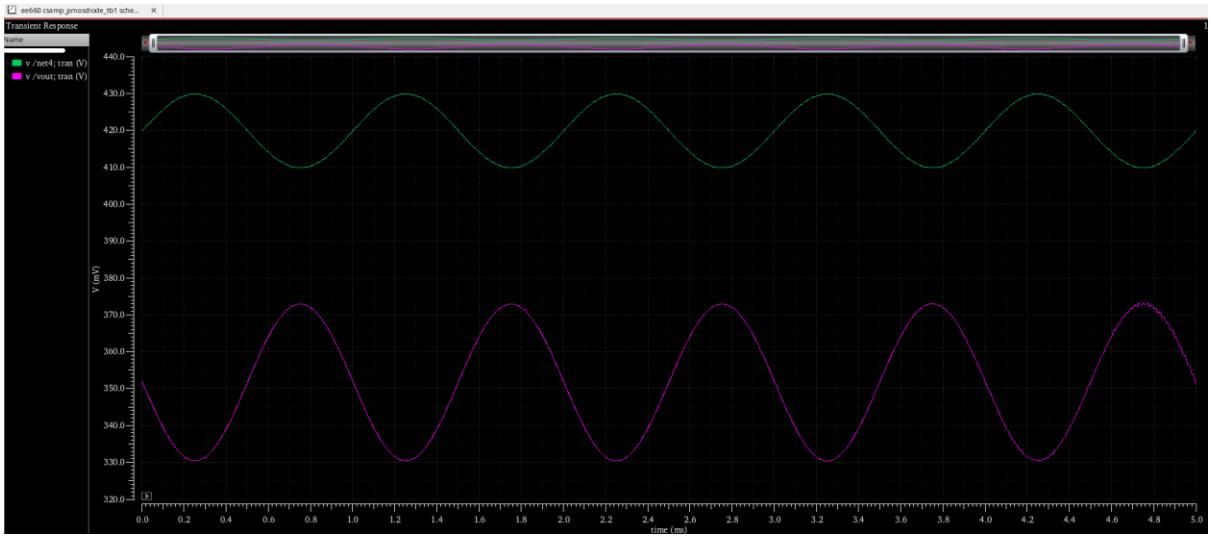


Figure: Plot showing Vin ,Vout waveforms obtained from transient analysis .

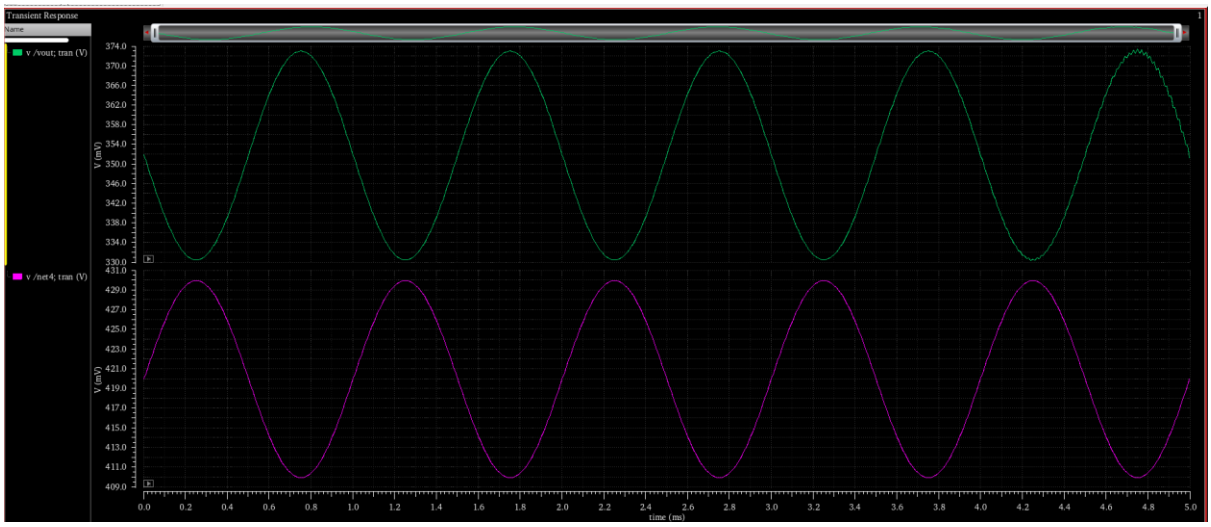


Figure: Plot showing Vin ,Vout waveforms obtained from transient analysis .

Observation: From the above transient analysis graphs it is observed that input and output waveforms are **out of phase**.

(c) Perform an AC analysis of the circuit. Plot the magnitude and phase responses. Note down the low frequency gain and 3 dB frequency of the circuit. Also, check what is the phase difference between the input and output at the 3 dB frequency.

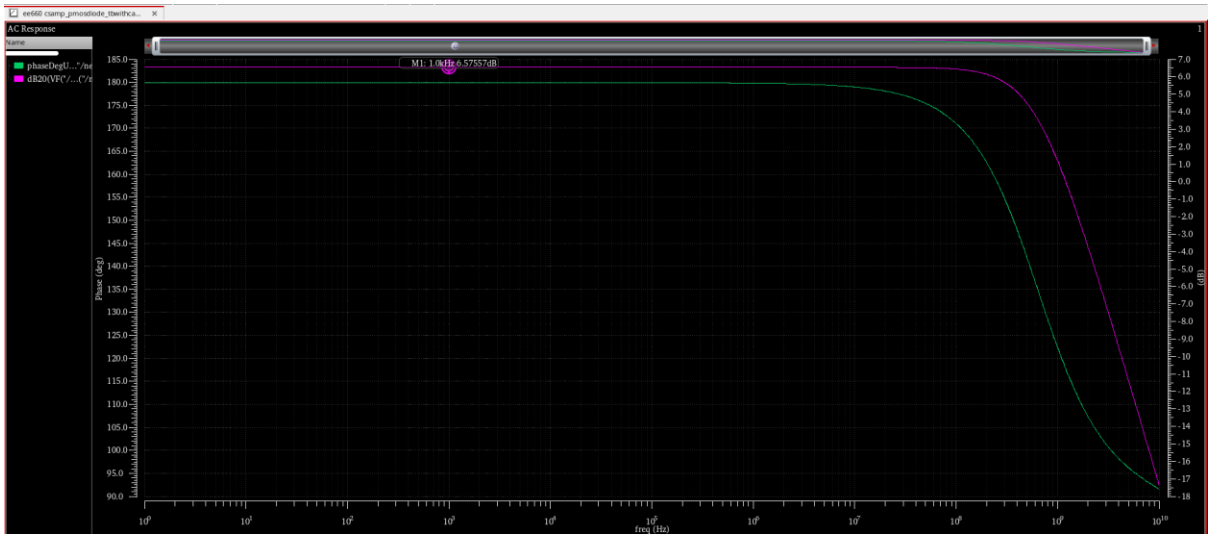


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

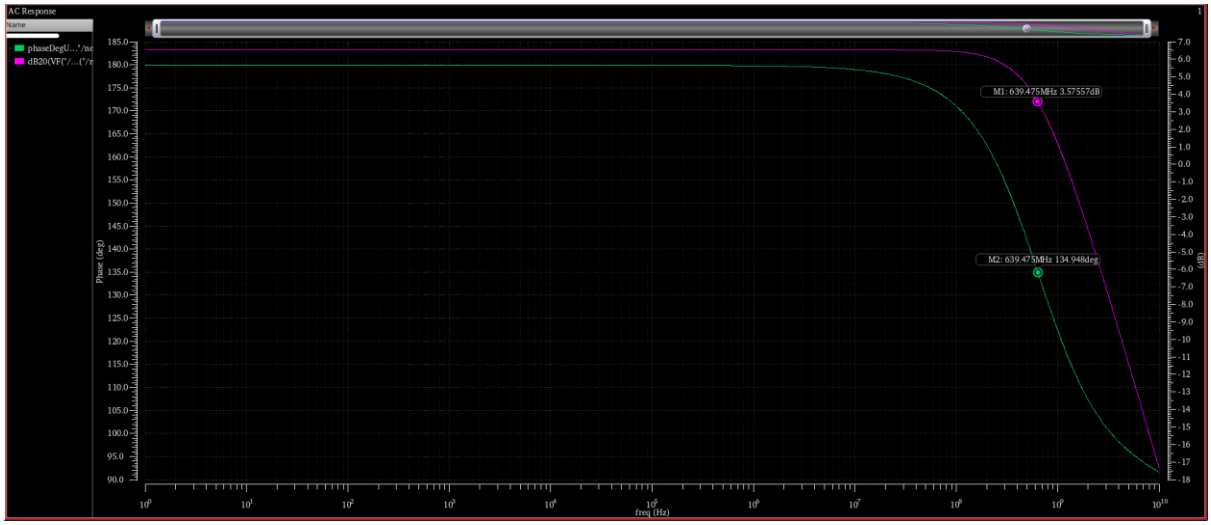


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plots we can say that :

1.Low frequency gain is 6.57dB

2. 3dB cuttoff frequency is 639.475MHz

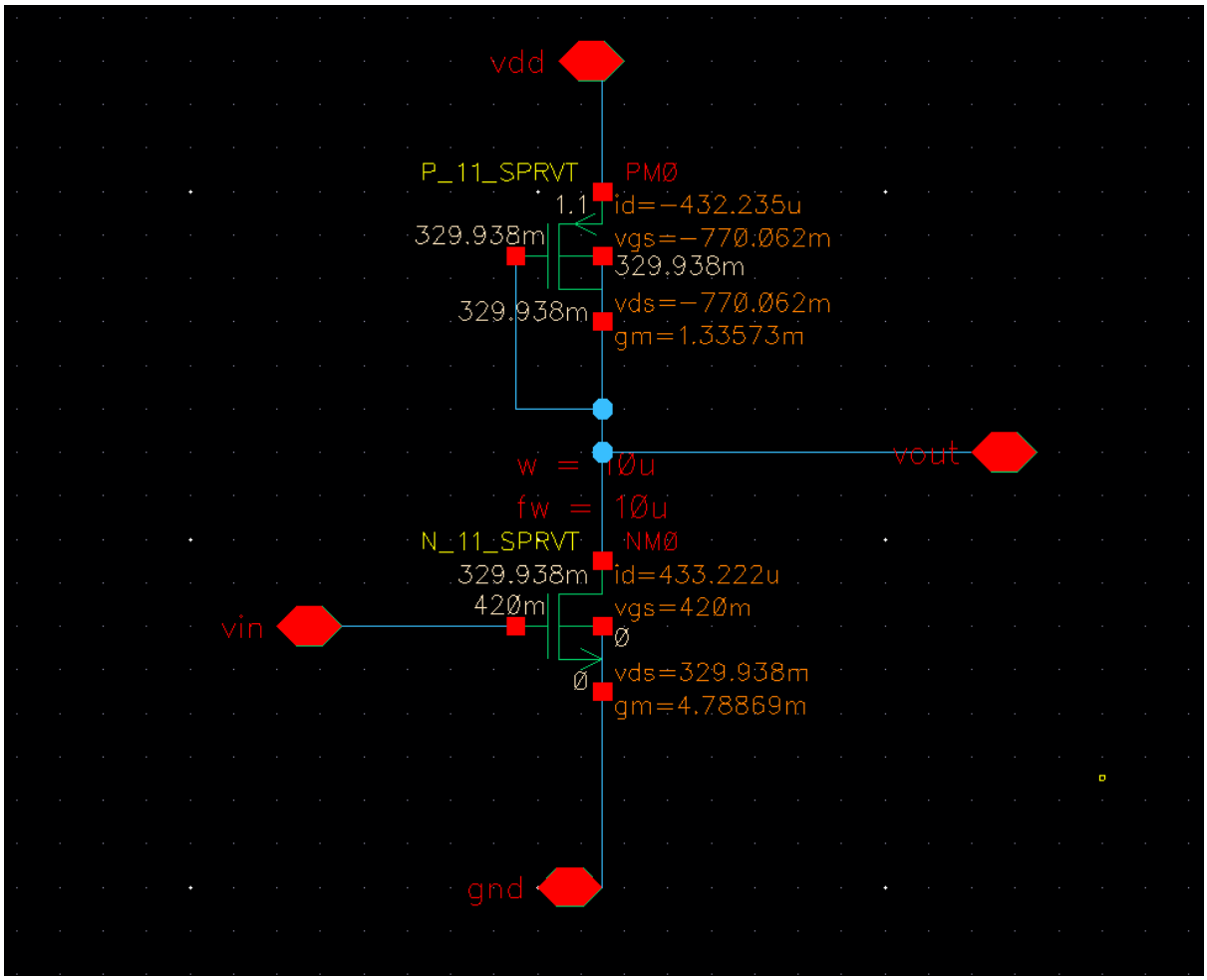
3.Phase difference between the input and output at the 3 dB frequency: 134.94Degrees.

(d) Calculate the power dissipation of the circuit.

Power dissipation of the circuit Id * Vdd = 0.399mA*1.1v =0.4389mW

4. Repeat step 3 by changing the amplitude of the sinusoidal source to 200 mV. Do you see any differences between the results? If yes, justify your observations.

a)DC operating point analysis Results:



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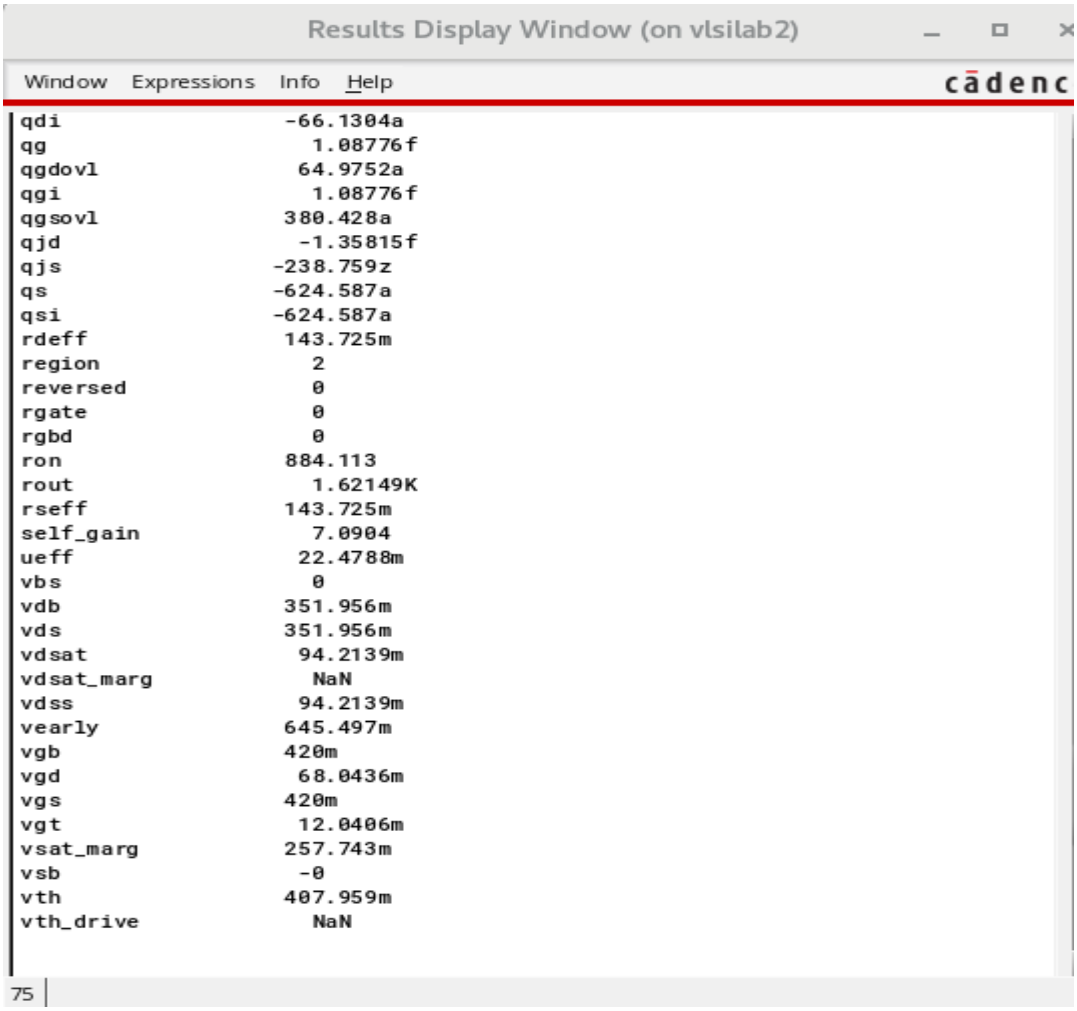

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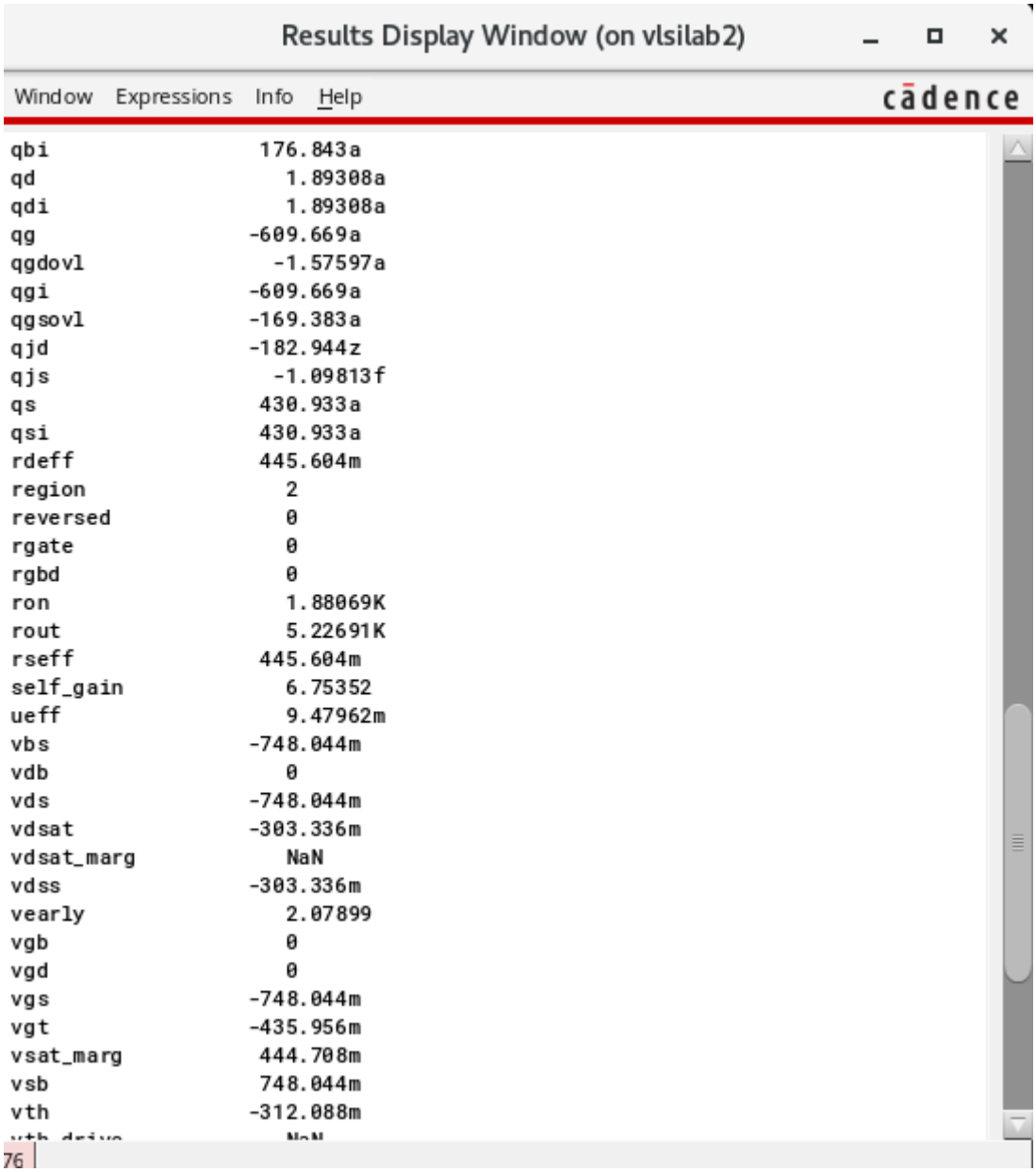
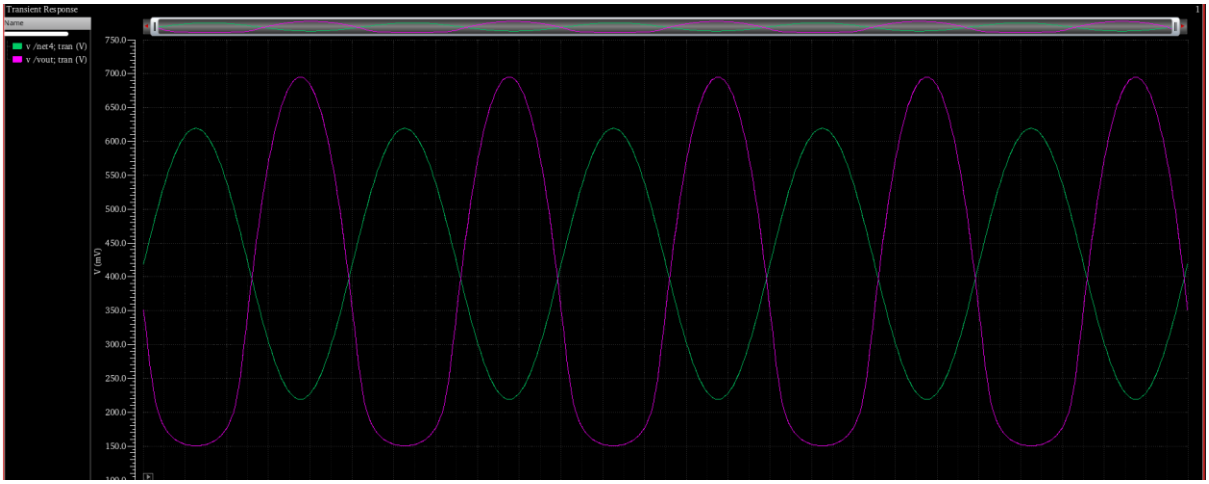


Observation: From the above DC operating point analysis it’s been verified that 2 transistors are in Saturation region of operation when Vgs=420mV.

b)Perform transient analysis of the circuit and verify that the input and output waveforms are out of phase.



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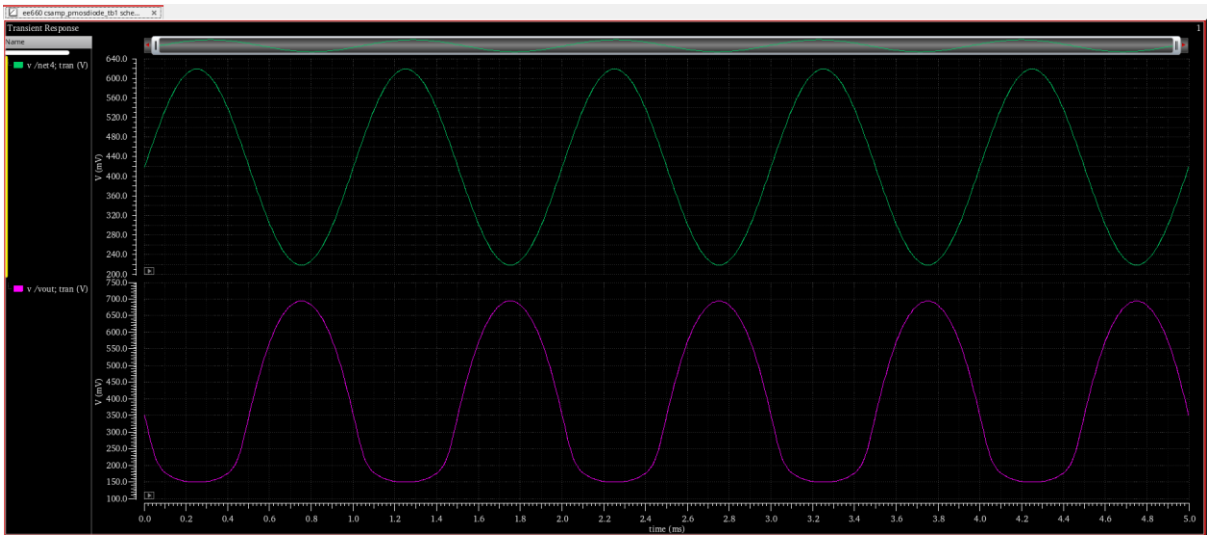
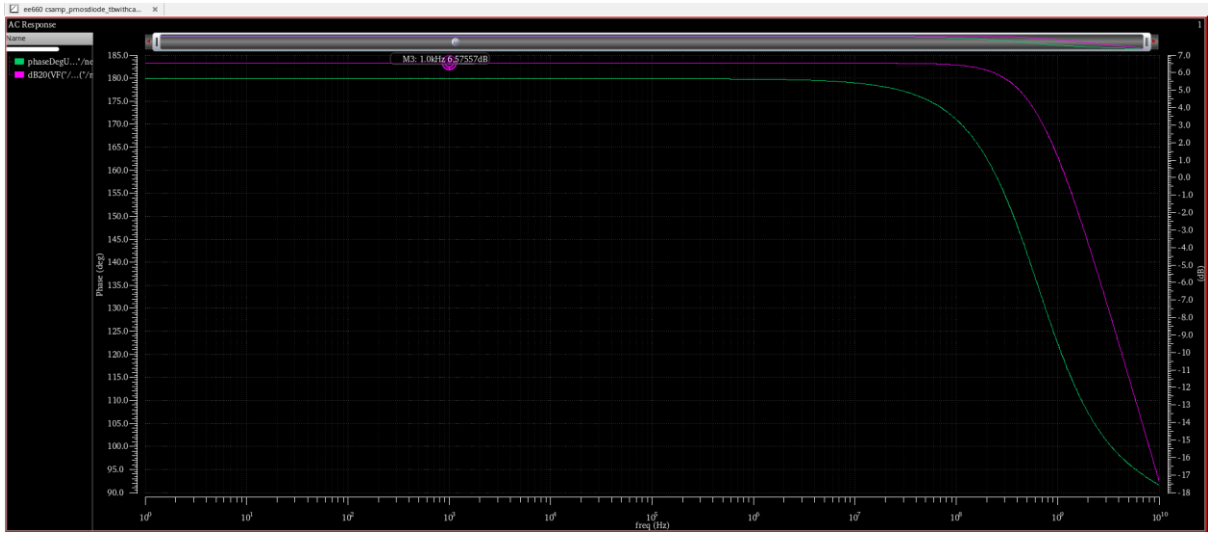


Figure: Plot showing Vin ,Vout waveforms obtained from transient analysis .

Observation: It is Observed that, after changing sinusoidal voltage to 200mV Vout waveform has been changed. This is mainly caused due to the clipping of output voltage caused due to the fact that M1 is in triode region since0.2v is not in the range of saturation Vin . Hence , we could see that Vout got clipped.This is major change that has been observed when we have changed input of sinusoidal voltage to 0.2v

c)Perform AC analysis of the circuit. Plot the magnitude and phase responses.



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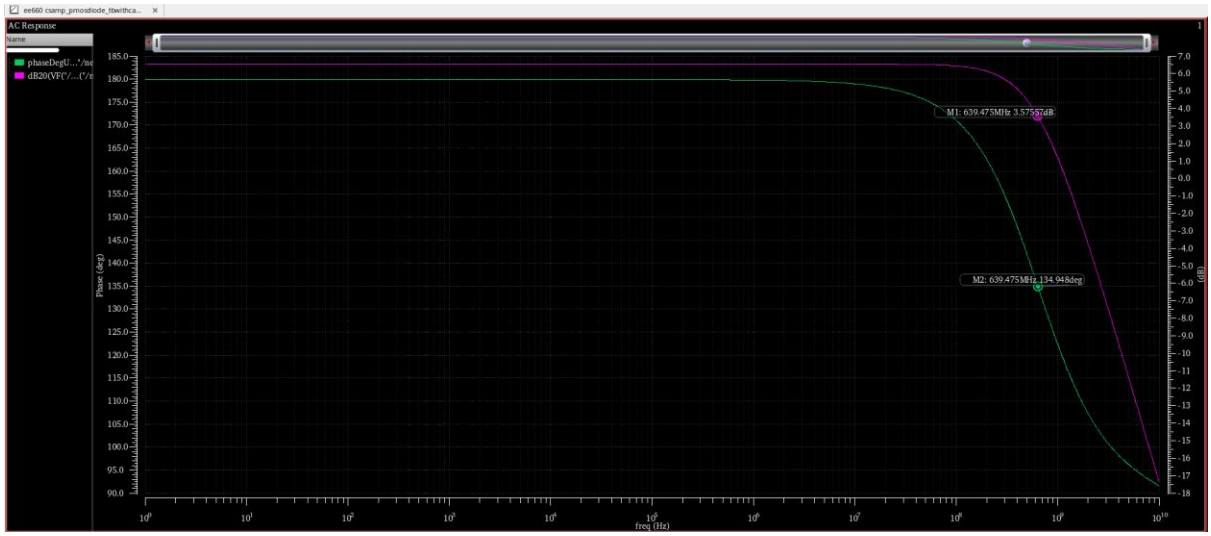

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1.Low frequency gain is 6.57dB

2. 3dB cuttoff frequency is 639.475MHz

3.Phase difference between the input and output at the 3 dB frequency: 134.94Degrees.

(d) Calculate the power dissipation of the circuit.

Power dissipation of the circuit Id * Vdd = 0.433mA*1.1v =0.4763mW

5. Mostly, you would have got a low-frequency gain that is different from the designed value in step 3.Could you change the dimensions of M1 or M2 to get a gain of 3?

Yes , we have got gain less than designed value . To get a gain of 3 (I.e Av in dB= 9.54dB) below modifications are made to the dimensions of M1 and M2

Initially tried reducing width of M2 from 2um to 80nm(least possible) . Below is the magnitude and phase plot :

Figure : Plot showing Magnitude and frequency response

Observed gain =-8.98dB

Now increased width of M1 to 10um(max possible for this technology). Below is the magnitude and phase plot :

Figure : Plot showing Magnitude and frequency response

Observed gain =6.95dB

Since this technology offers maximum width to be 10um , tried placing nmos transistors in parallel .yet maximum gain attained is 6.35 when 3 transistors are used.

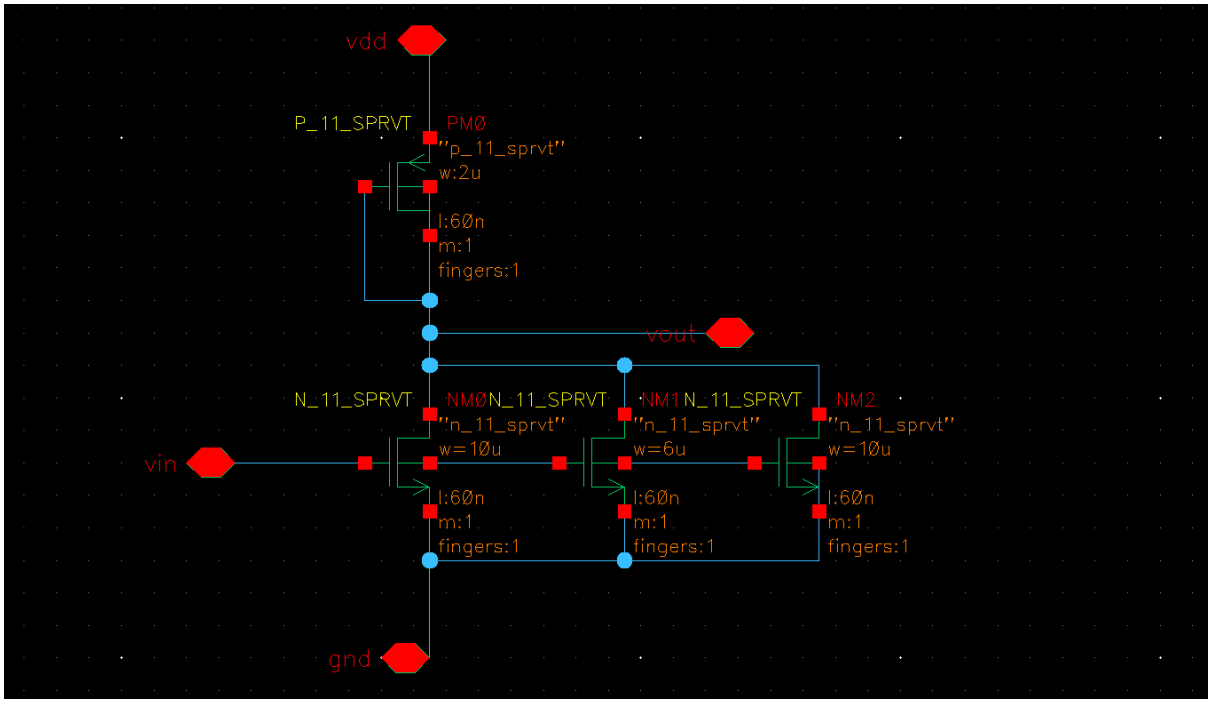

Figure: Schematic showing cs amplifier with 3 nmos transistors in parallel.

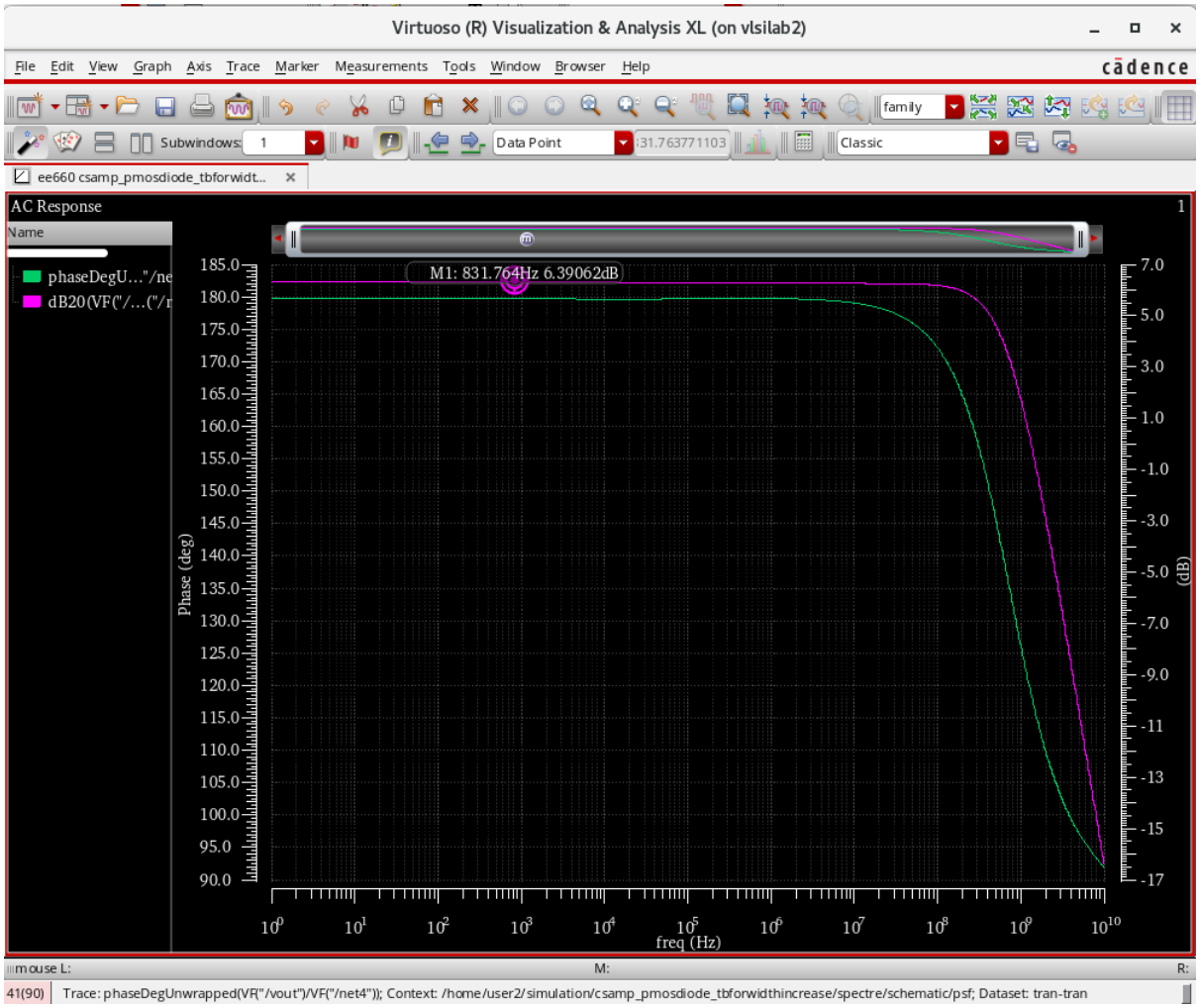

Figure: Plot showing Frequency and magnitude response.

Observed gain is 6.39dB