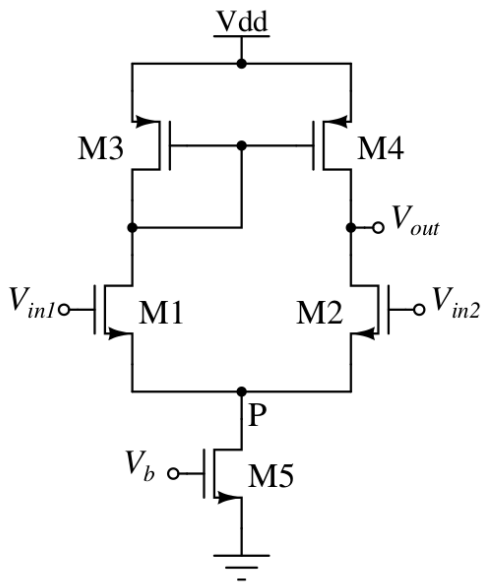
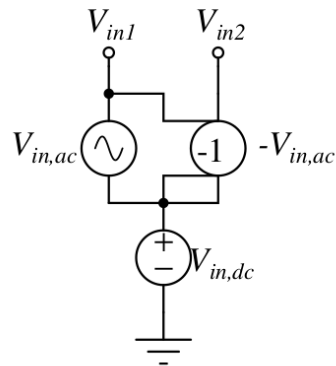


Submitted by: L Sri Sai Swathi (2414202)

1. Design an NMOS common-source differential amplifier with active load as shown in Fig. 1a using UMC65 technology. Given $(W/L)_{1,2,5} = 6\mu/0.06\mu$, $(W/L)_{3,4} = 3\mu/0.06\mu$, $V_b = 0.55$ V, and $V_{in,dc} = 0.7$ V.



(a) Differential amplifier.



(b) Input source.

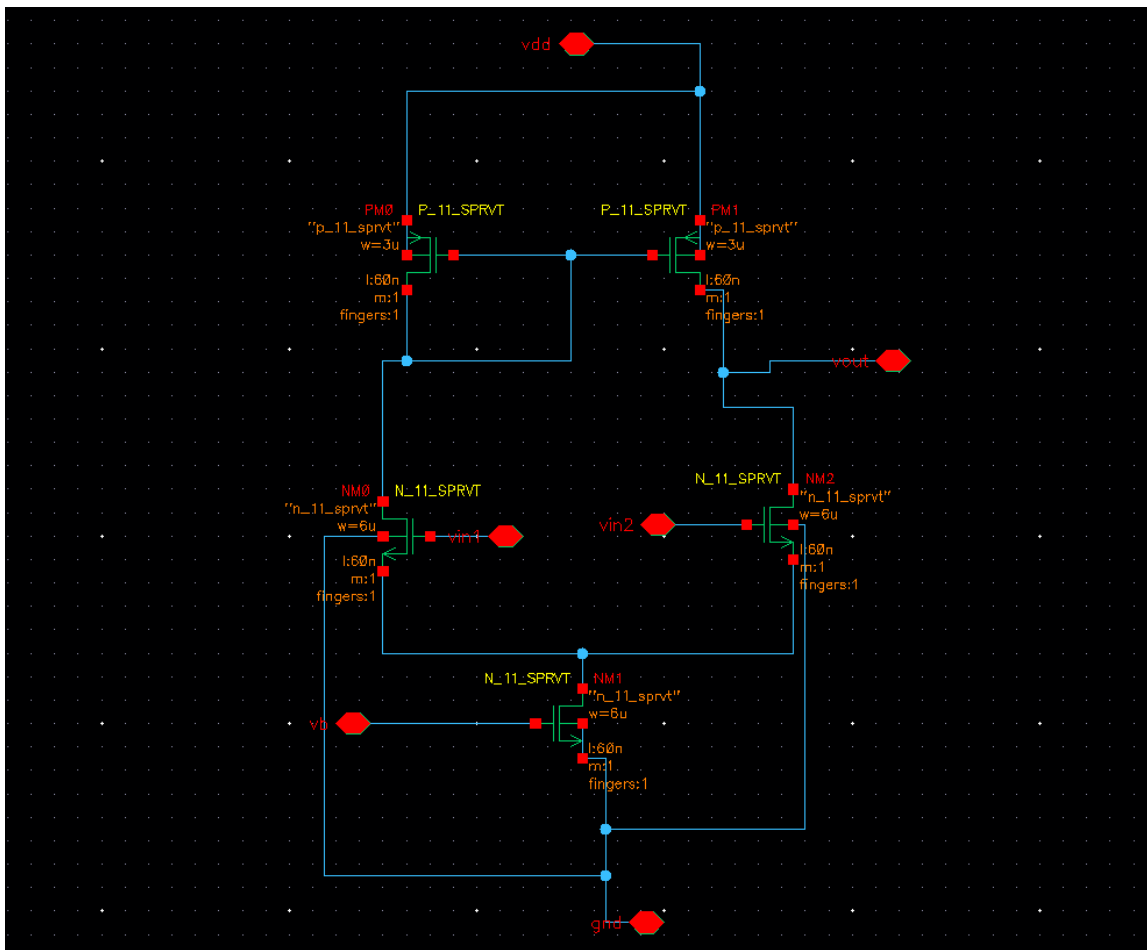


Figure : Schematic of NMOS common-source differential amplifier with active load using 65 nm technology (W/L 1,2,5 = $6\mu/0.06\mu$, (W/L) 3,4 = $3\mu/0.06\mu$, $V_b = 0.55$ V, and $V_{in,dc} = 0.7$ V.

(a) The configuration shown in Fig. 1b is used to generate the input for the amplifier. You can use the small signal amplitude of $V_{in,ac}$ to be 10 mV, and frequency to be 1 kHz. Perform the operating point analysis and check if all the transistors are in saturation region of operation.

Below are the simulation results of DC operating point analysis:

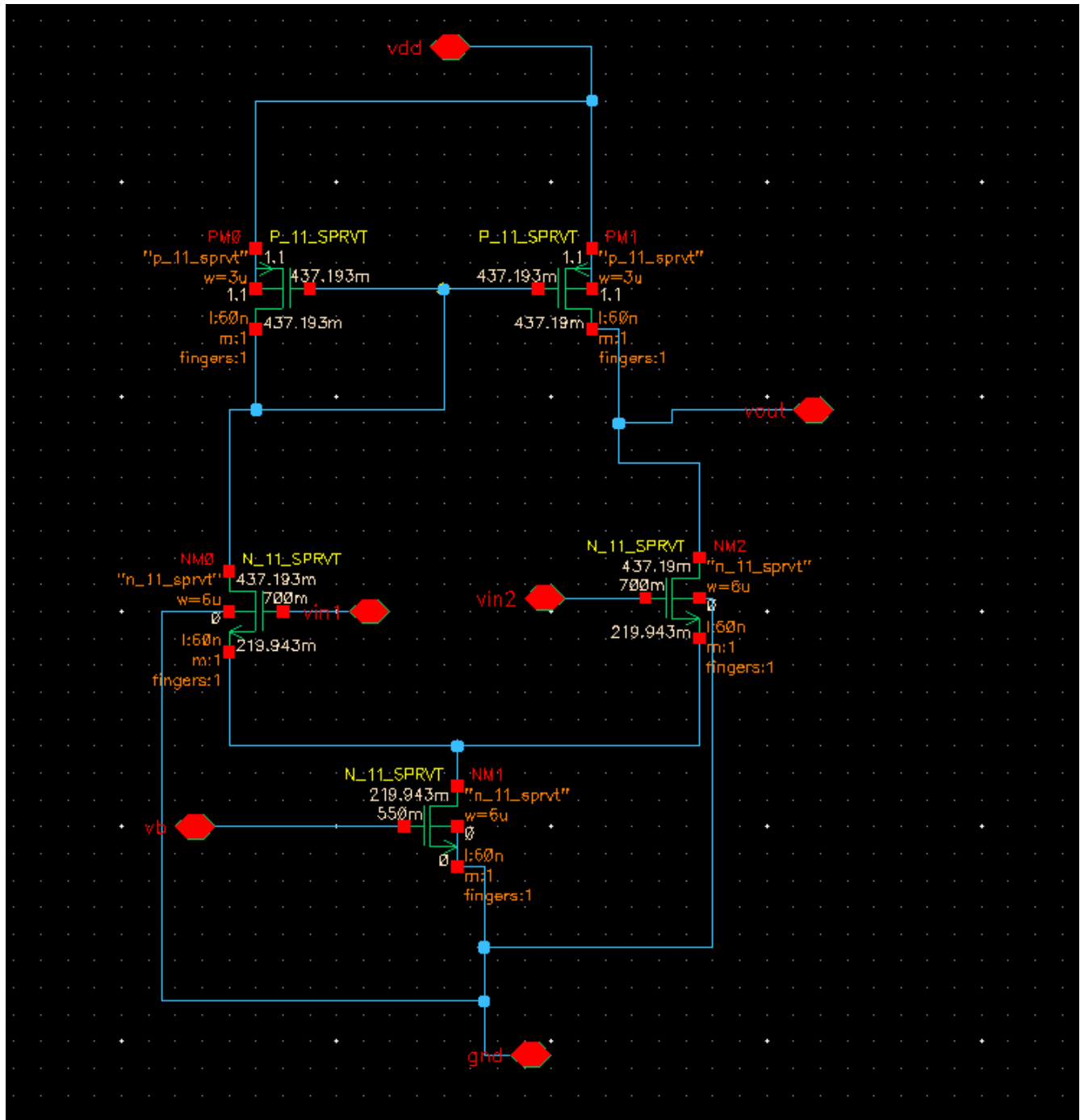
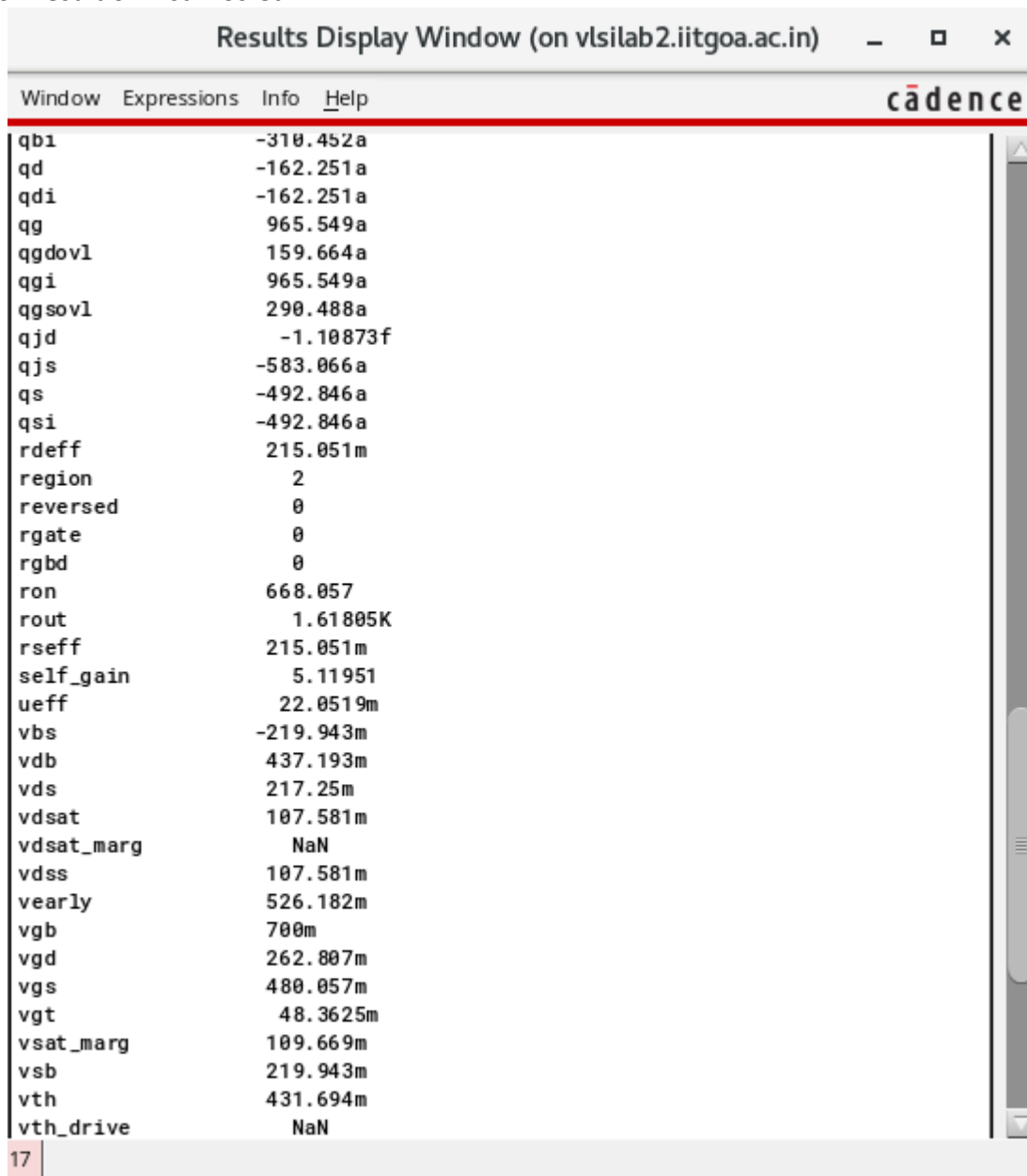


Figure: Schematic with operating point values

Simulation result of first mosfet M1 :



The screenshot shows a 'Results Display Window' from Cadence, titled 'Results Display Window (on vlsilab2.iitgoa.ac.in)'. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation results for MOSFET M1. The results are organized into two columns: the parameter name and its corresponding value. The values are in various units, including amperes (a), milliamperes (mA), millivolts (mV), and milliwatts (mW). The MOSFET is operating in region 2, which is the saturation region. The gate voltage (vgs) is 480.057mV, and the drain current (idd) is -162.251a. The threshold voltage (vth) is 431.694mV, and the overdrive voltage (vov) is 48.3625mV. The transconductance (gm) is 5.11951, and the output resistance (ro) is 1.61805K. The power dissipation (pd) is 26.2807mW. The channel length modulation parameter (lambda) is 0, and the body effect coefficient (gamma) is 0. The channel length (L) is 2, and the channel width (W) is 0. The channel length modulation parameter (lambda) is 0, and the body effect coefficient (gamma) is 0. The channel length (L) is 2, and the channel width (W) is 0.

Parameter	Value
qb1	-310.452a
qd	-162.251a
qdi	-162.251a
qg	965.549a
qgdovl	159.664a
qgi	965.549a
qgsovl	290.488a
qjd	-1.10873f
qjs	-583.066a
qs	-492.846a
qsi	-492.846a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	668.057
rout	1.61805K
rseff	215.051m
self_gain	5.11951
ueff	22.0519m
vbs	-219.943m
vdb	437.193m
vds	217.25m
vdsat	107.581m
vdsat_marg	NaN
vdss	107.581m
vearly	526.182m
vgb	700m
vgd	262.807m
vgs	480.057m
vgt	48.3625m
vsat_marg	109.669m
vsb	219.943m
vth	431.694m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 (Saturation region of operation)

Results Display Window (on vlsilab2.iitgoa.ac.in)		—	□	×
Window	Expressions	Info	Help	cadence
qb	-310.452a			
qbi	-310.452a			
qd	-162.253a			
qdi	-162.253a			
qg	965.55a			
qgdovl	159.666a			
qgi	965.55a			
qgsovl	290.488a			
qjd	-1.10872f			
qjs	-583.066a			
qs	-492.846a			
qsi	-492.846a			
rdeff	215.051m			
region	2			
reversed	0			
rgate	0			
rgb	0			
ron	668.053			
rout	1.61804K			
rseff	215.051m			
self_gain	5.11946			
ueff	22.0519m			
vbs	-219.943m			
vdb	437.19m			
vds	217.247m			
vdsat	107.581m			
vdsat_marg	NaN			
vdss	107.581m			
vearly	526.177m			
vgb	700m			
vgd	262.81m			
vgs	480.057m			
vgt	48.3623m			
vsat_marg	109.666m			
vsb	219.943m			

Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 (Saturation region of operation)

Results Display Window (on vlsilab2.iitgoa.ac.in)

WindowExpressionsInfoHelp

cadence

pwr	142.959u
qb	-320.864a
qbi	-320.864a
qd	-204.672a
qdi	-204.672a
qg	1.1696f
qgdovl	200.167a
qgi	1.1696f
qgsovl	332.67a
qjd	-582.537a
qjs	-389.736z
qs	-644.061a
qsi	-644.061a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	338.383
rout	914.067
rseff	215.051m
self_gain	4.1088
ueff	21.5378m
vbs	0
vdb	219.943m
vds	219.943m
vdsat	144.946m
vdsat_marg	NaN
vdss	144.946m
vearly	594.128m
vgb	550m
vgd	330.057m
vgs	550m
vgt	130.255m
vsat_marg	74.997m
vsb	-0

17

Figure: Simulation result of DC operating point analysis.

Observation: M5 is in region 2 (Saturation region of operation)

Results Display Window (on vlsilab2.iitgoa.ac.in)	
Window	Expressions Info Help
cadence	
qgdovl	-2.32864a
qgi	-800.714a
qgsavl	-224.284a
qjd	786.252a
qjs	149.24z
qs	483.225a
qsi	483.225a
rdeff	298.167m
region	2
reversed	0
rgate	0
rgbd	0
ron	2.03898K
rout	4.48002K
rseff	298.167m
self_gain	7.07539
ueff	9.33764m
vbs	0
vdb	-662.807m
vds	-662.807m
vdsat	-241.903m
vdsat_marg	NaN
vdss	-241.903m
vearly	1.45631
vgb	-662.807m
vgd	0
vgs	-662.807m
vgt	-287.444m
vsat_marg	420.904m
vsb	-0
vth	-375.364m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 (Saturation region of operation)

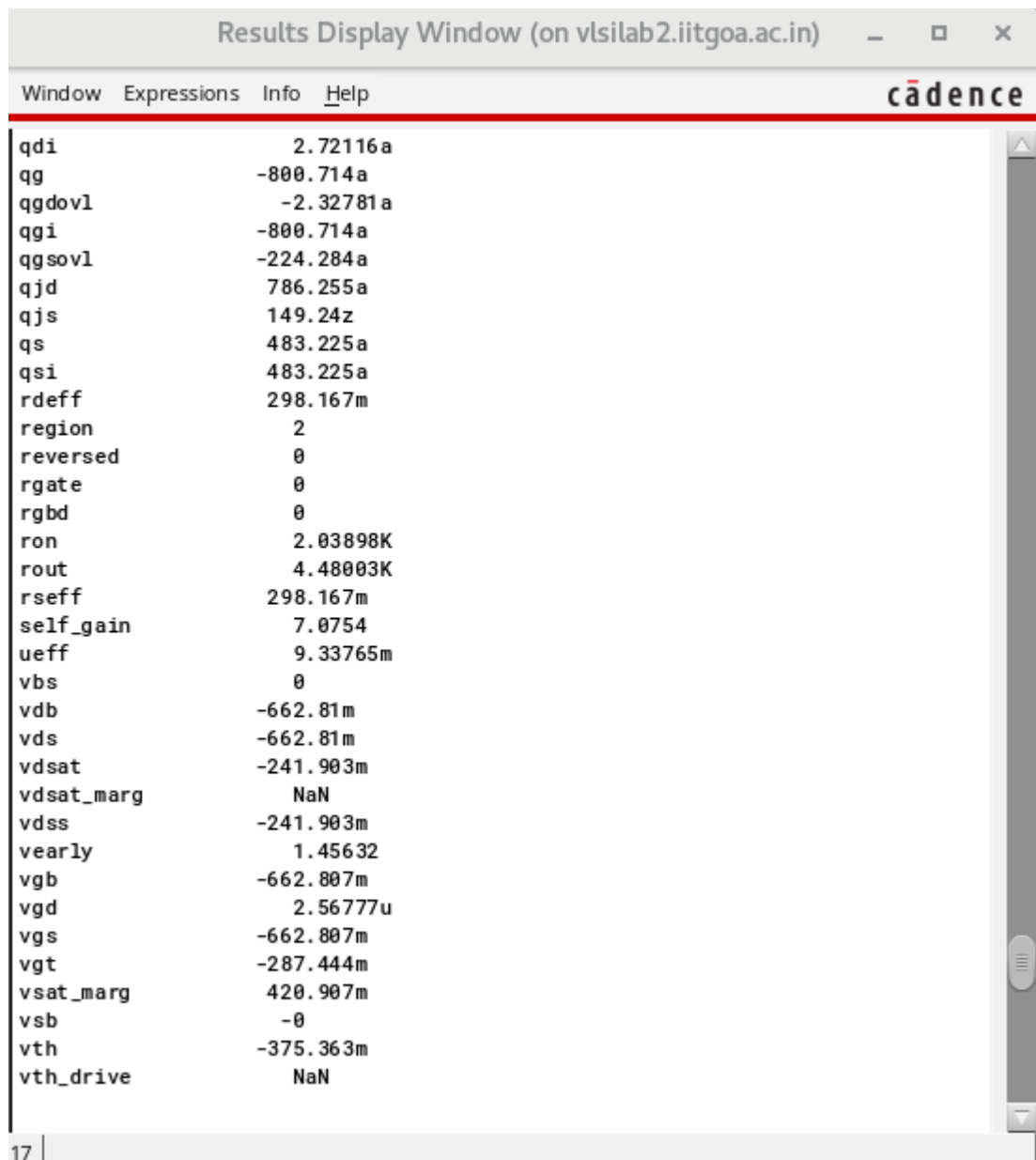


Figure: Simulation result of DC operating point analysis.

Observation: M4 is in region 2 (Saturation region of operation)

It is Verified that all the 5 transistors are in region 2 i.e Saturation region of operation.

(b) Perform the AC analysis of the circuit and find out the differential gain and 3 dB frequency.

Below are simulation results of the AC response analysis :

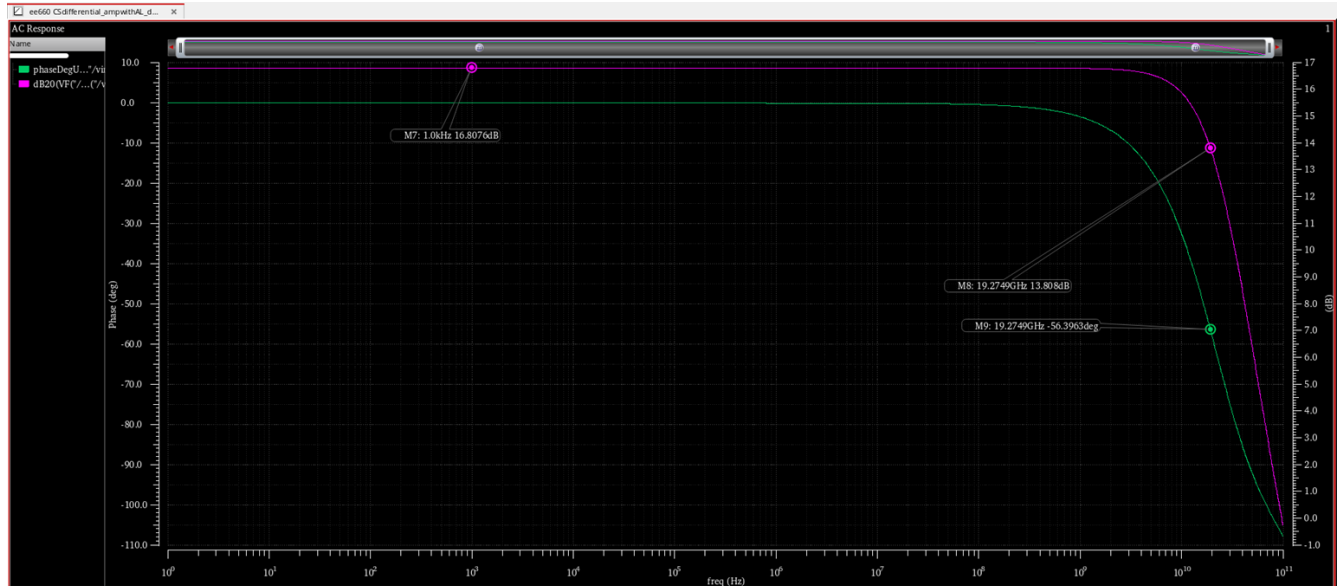


Figure: Plot showing Ac response analysis results (Vout,Vin1 considered)

Observations:From the above Ac Analysis plots we can say that :

- 1.Low frequency gain is **16.807dB**
2. 3dB cutoff frequency is **19.27 GHz**
- 3.Phase difference between the input and output at the 3 dB frequency: **-56.39Degrees.**

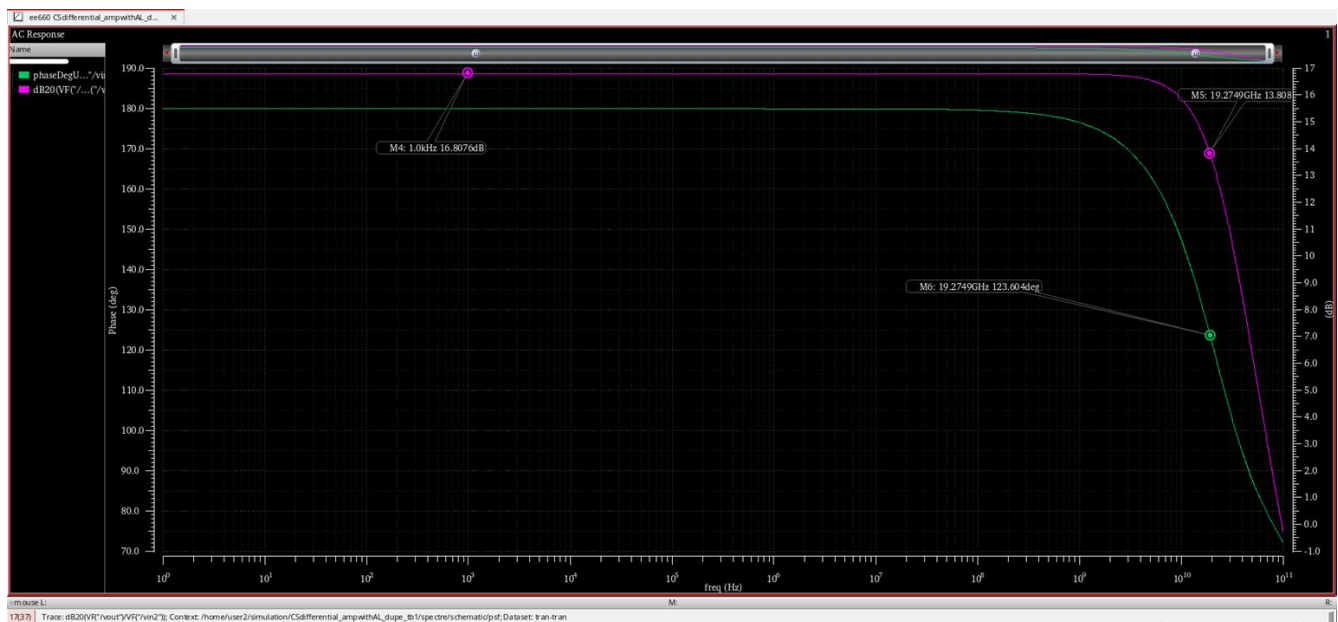


Figure: Plot showing Ac response analysis results (Vout,Vin2 considered)

Observations:From the above Ac Analysis plots we can say that :

- 1.Low frequency gain is **16.807dB**
2. 3dB cutoff frequency is **19.27 GHz**

3. Phase difference between the input and output at the 3 dB frequency: **123.6Degrees**.

(c) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Below are the results of Transient analysis at $v_{in} = 10\text{mV}$:

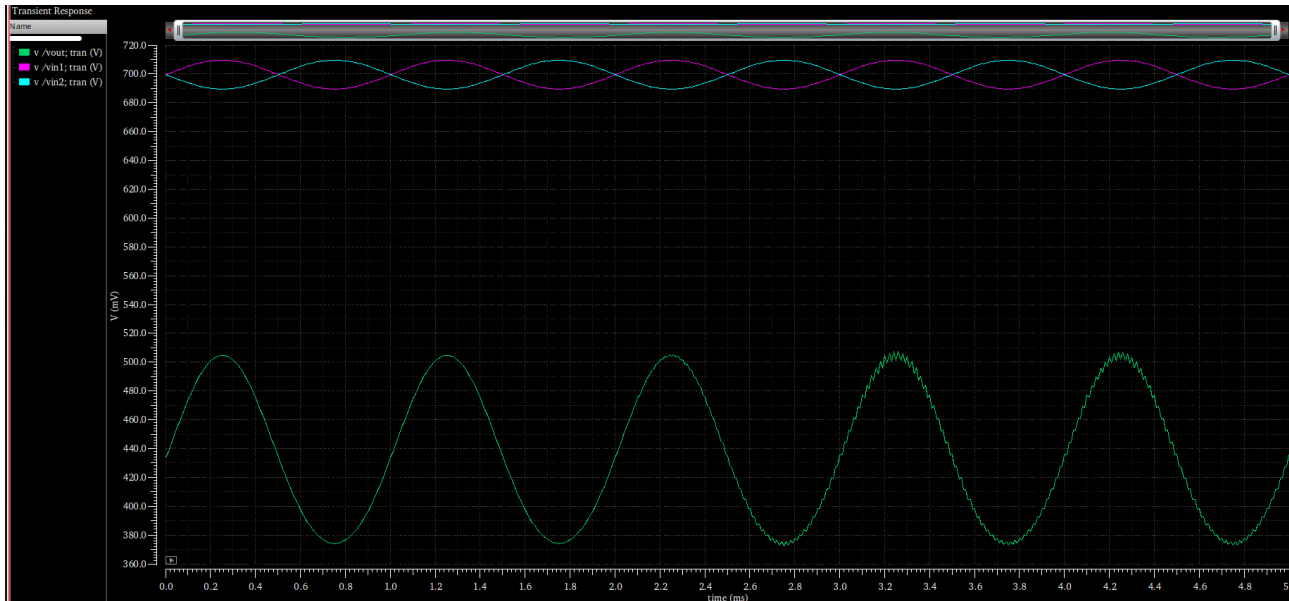


Figure: Plot showing transient analysis simulation result (V_{out} w.r.to V_{in1}, V_{in2})

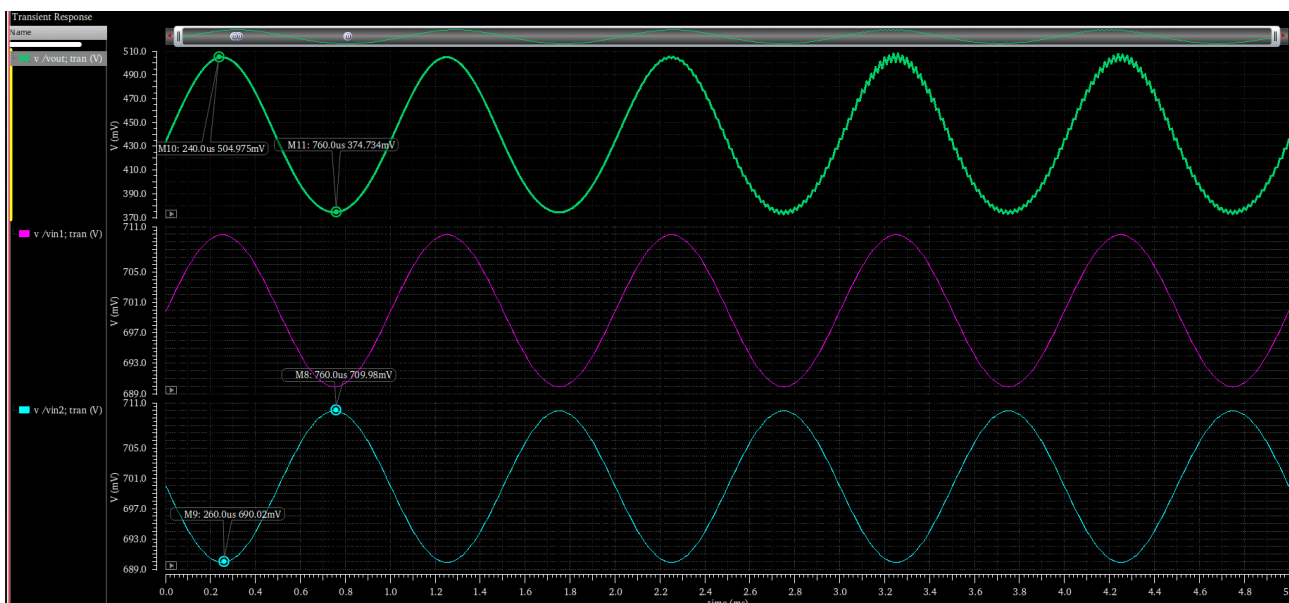


Figure: Plot showing transient analysis simulation result (V_{out} w.r.to V_{in1}, V_{in2})

Below are the results of Transient analysis at $v_{in} = 20\text{mV}$:

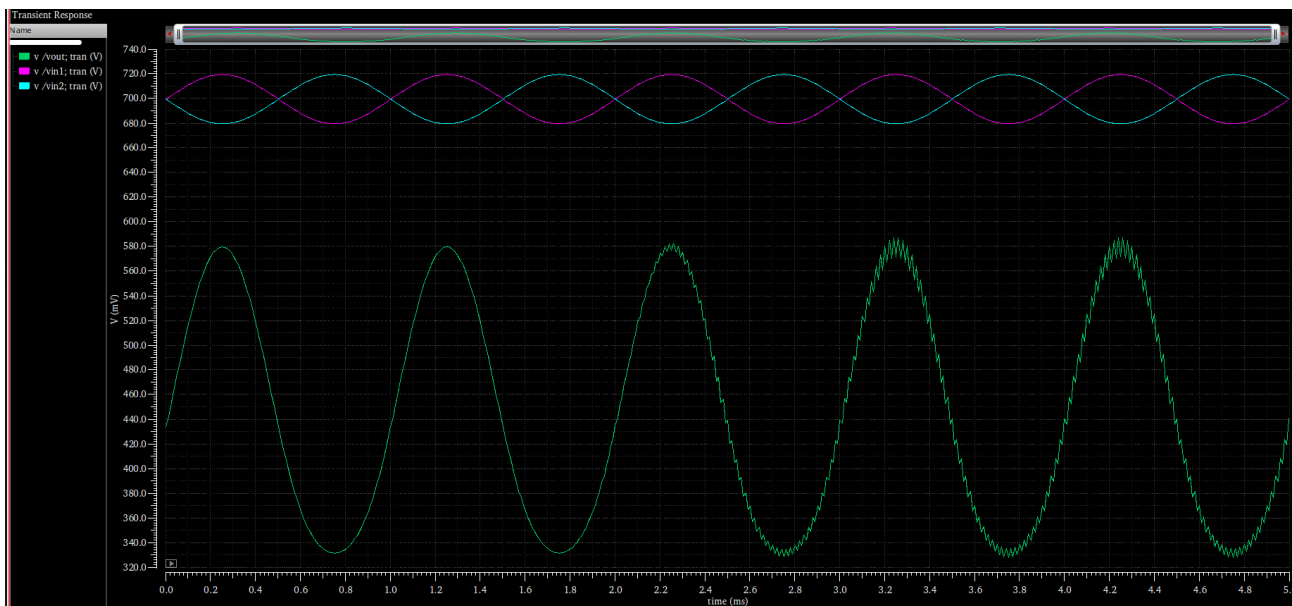


Figure: Plot showing transient analysis simulation result (V_{out} w.r.to V_{in1}, V_{in2})

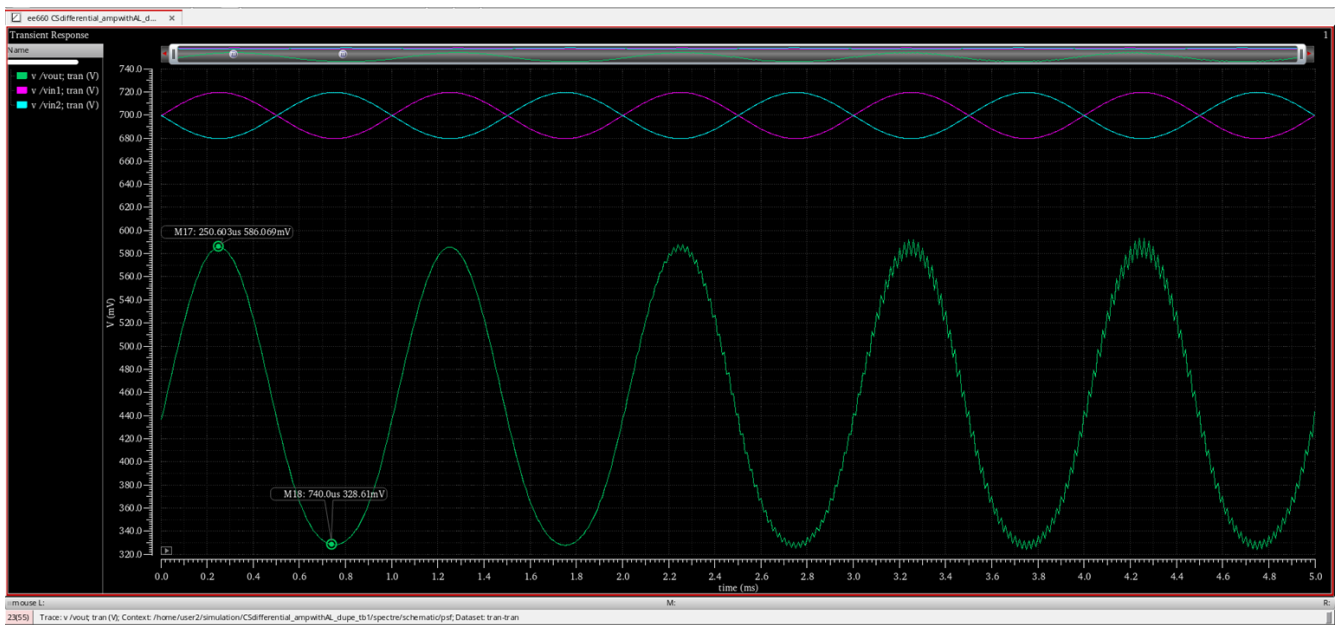


Figure: Plot showing transient analysis simulation result (V_{out} w.r.to V_{in1}, V_{in2})

2. A draw a compact layout of the amplifier by cleaning DRC and LVS. Extract the netlist and do post-layout simulations of the steps mentioned in 1(a) to 1(c). Compare the pre- and post-layout simulation results. (You have to attach the screenshots of RVE indicating clean DRC, LVS, and PEX.)

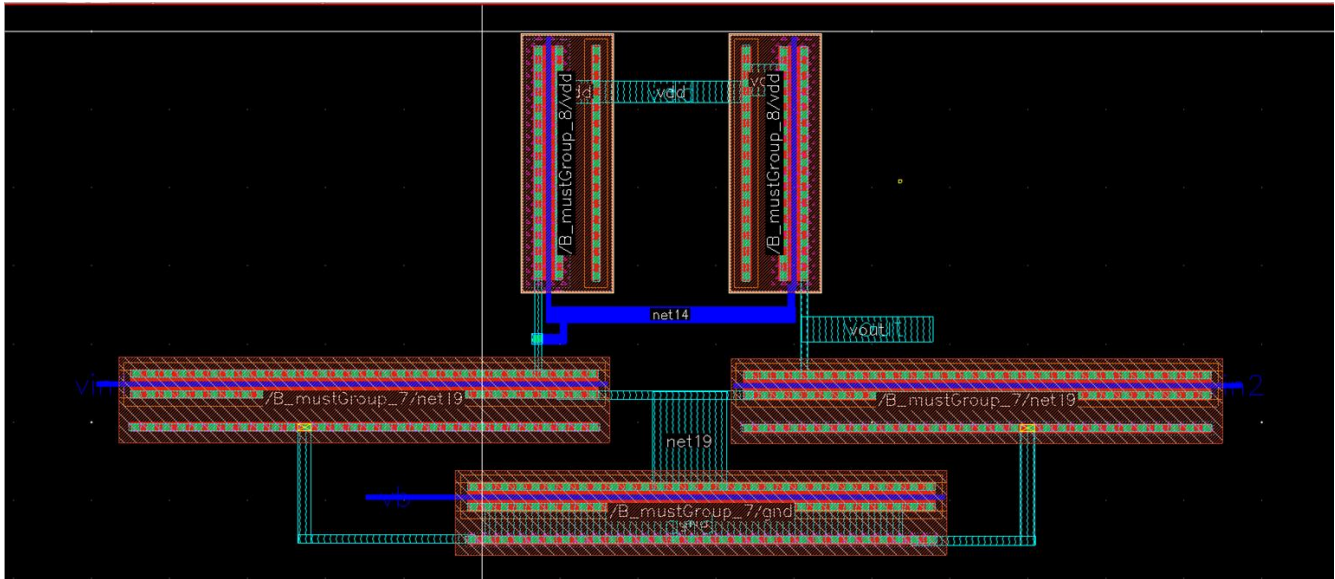
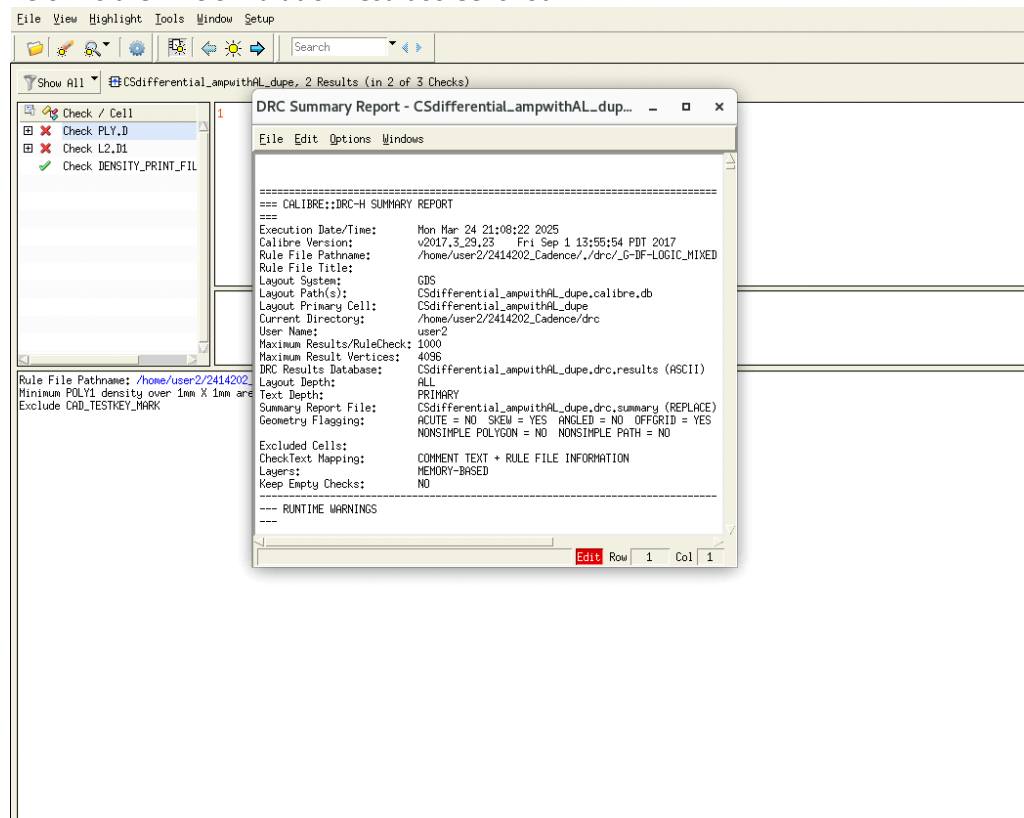
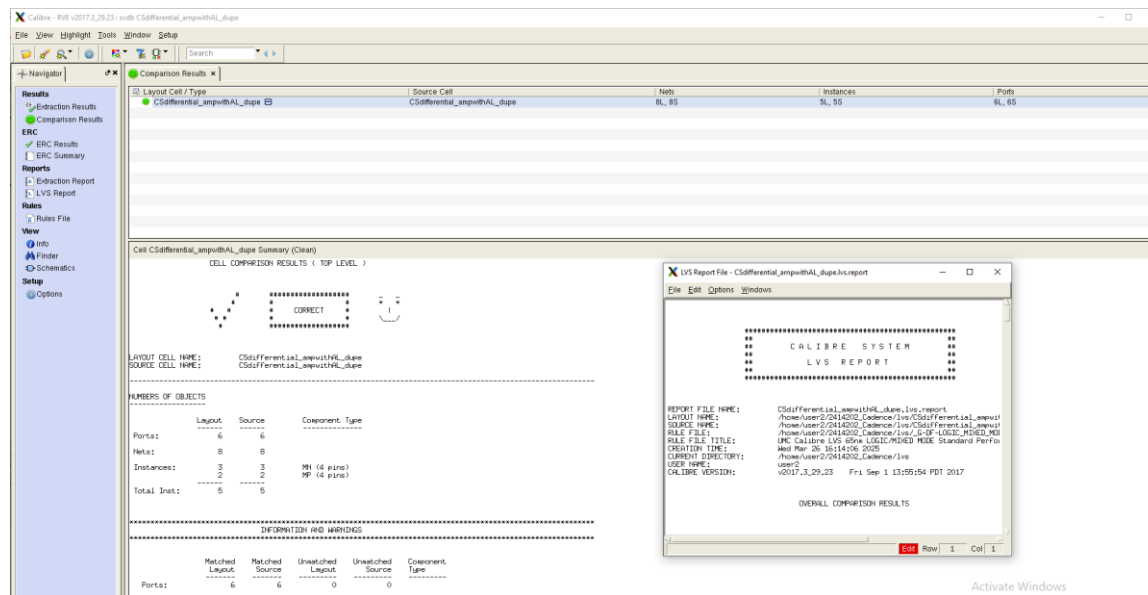


Figure: Layout of NMOS common-source differential amplifier with active load

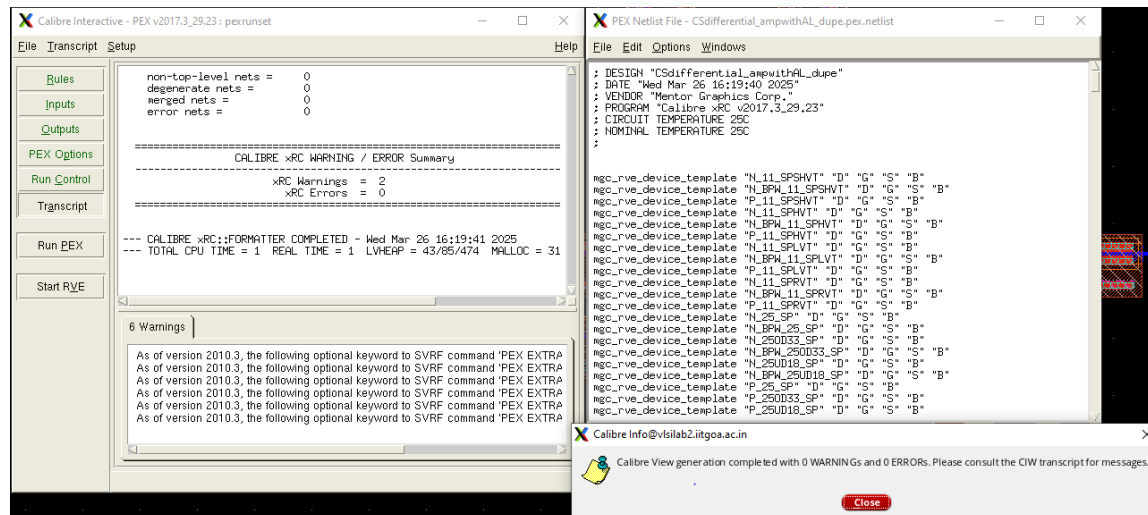
Below is the DRC Simulation result screenshot:



Below is the LVS simulation result screenshot:



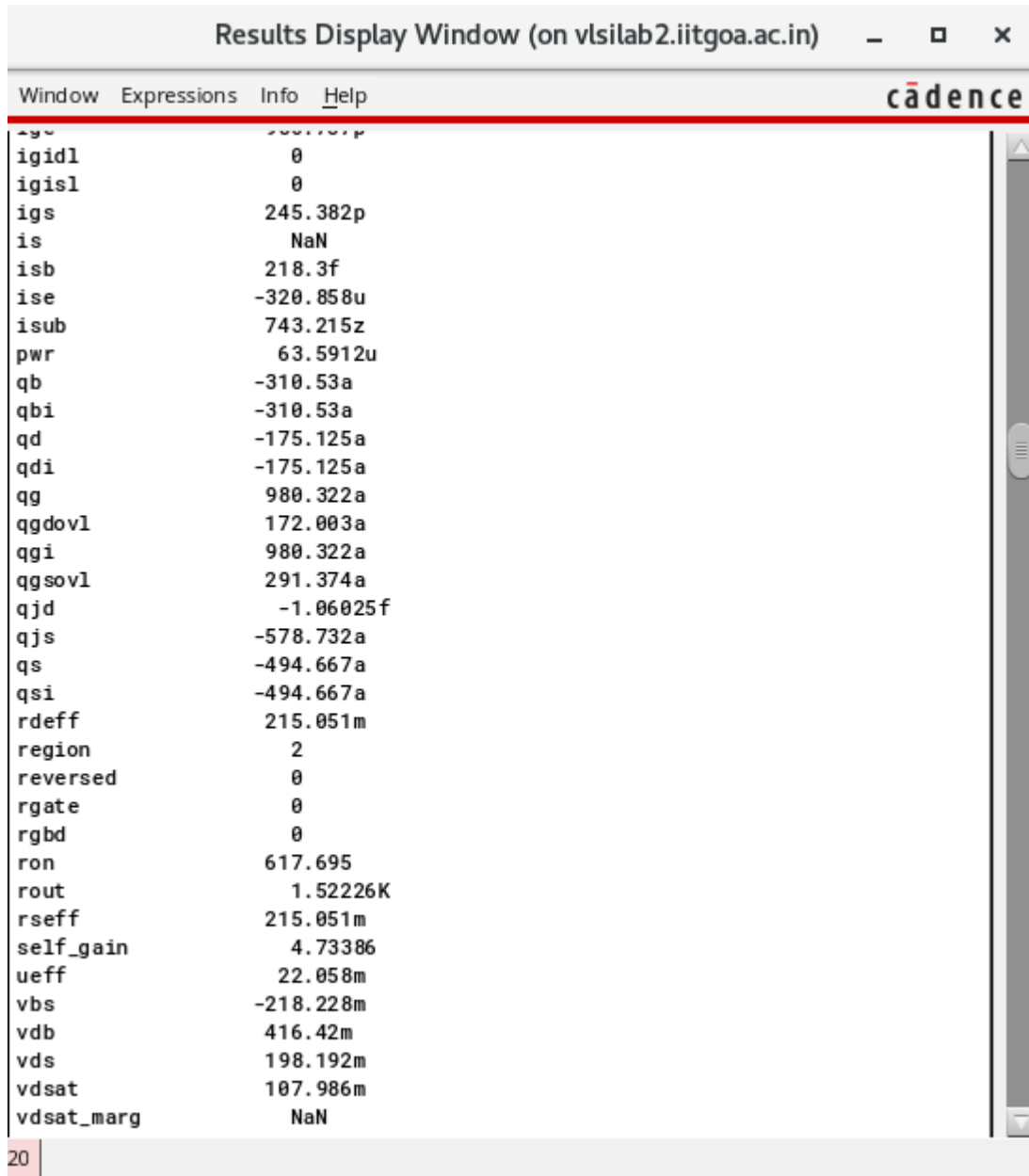
Below is the PEX simulation result screenshot:



Post-layout simulations:

a) Perform the operating point analysis and check if all the transistors are in saturation region of operation.

Simulation result of first mosfet M1 :



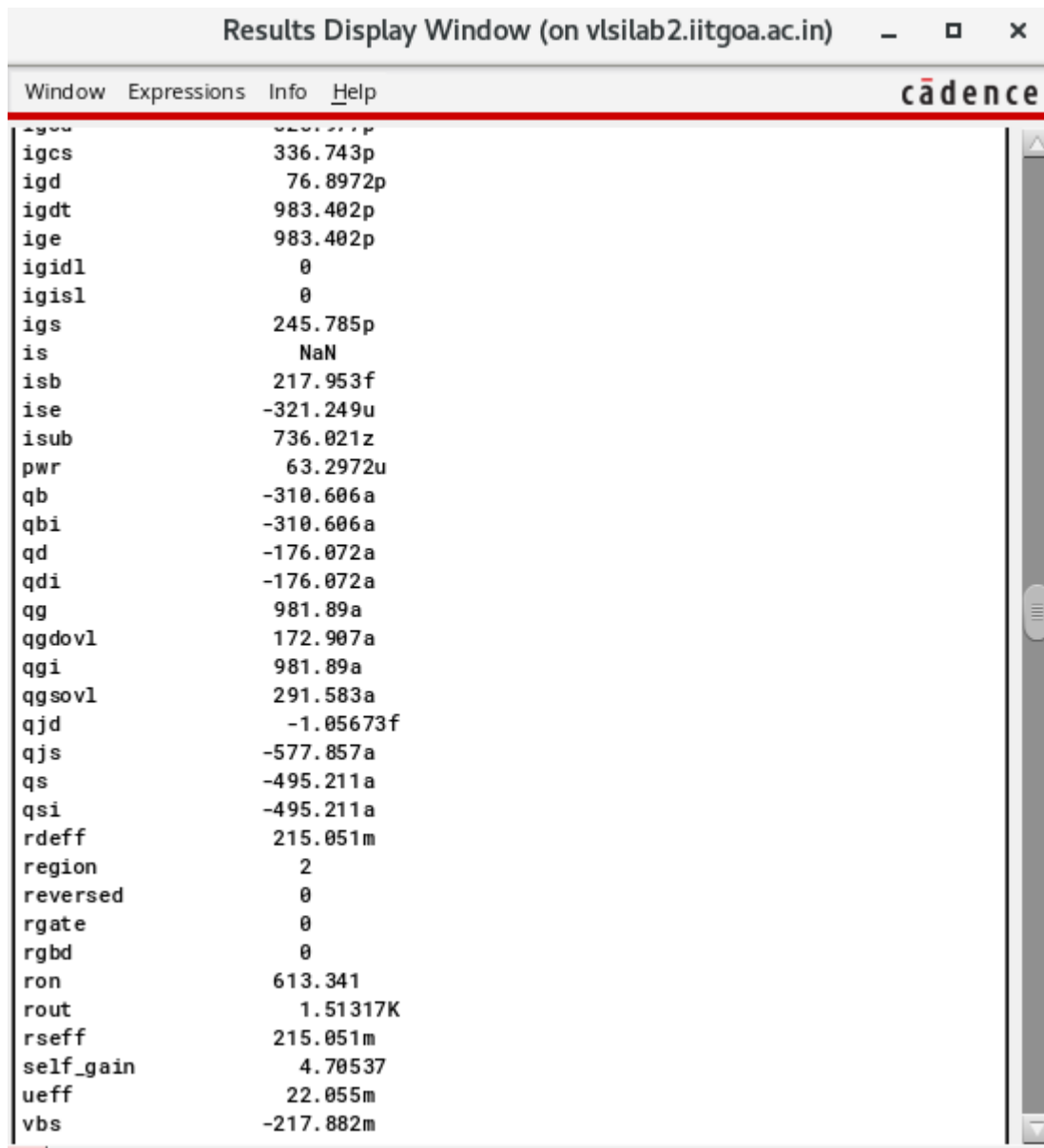
The screenshot shows the 'Results Display Window' from Cadence, displaying the DC operating point analysis results for MOSFET M1. The window has a title bar 'Results Display Window (on vlsilab2.iitgoa.ac.in)' and a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The Cadence logo is in the top right corner. The results are listed in a table with two columns: the parameter name and its value. The parameters include various current and voltage values, as well as region and gain information. The 'region' parameter is highlighted in pink, indicating the transistor is in region 2 (saturation).

Parameter	Value
ig	200.787p
igidl	0
igisl	0
igs	245.382p
is	NaN
isb	218.3f
ise	-320.858u
isub	743.215z
pwr	63.5912u
qb	-310.53a
qbi	-310.53a
qd	-175.125a
qdi	-175.125a
qg	980.322a
qgdovl	172.003a
qgi	980.322a
qgsovl	291.374a
qjd	-1.06025f
qjs	-578.732a
qs	-494.667a
qsi	-494.667a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	617.695
rout	1.52226K
rseff	215.051m
self_gain	4.73386
ueff	22.058m
vbs	-218.228m
vdb	416.42m
vds	198.192m
vdsat	107.986m
vdsat_marg	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 (Saturation region of operation)

Simulation result of mosfet M2:



The image shows a screenshot of the 'Results Display Window' from Cadence, titled 'Results Display Window (on vlsilab2.iitgoa.ac.in)'. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation results for a MOSFET model. The results are organized into two columns: the parameter name and its corresponding value. The 'region' parameter is highlighted with a red background, indicating the operating region of the MOSFET. The 'cadence' logo is visible in the top right corner of the window.

Parameter	Value
igcs	336.743p
igd	76.8972p
igdt	983.402p
ige	983.402p
igidl	0
igisl	0
igs	245.785p
is	NaN
isb	217.953f
ise	-321.249u
isub	736.021z
pwr	63.2972u
qb	-310.606a
qbi	-310.606a
qd	-176.072a
qdi	-176.072a
qg	981.89a
qgdovl	172.907a
qgi	981.89a
qgsavl	291.583a
qjd	-1.05673f
qjs	-577.857a
qs	-495.211a
qsi	-495.211a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	613.341
rout	1.51317K
rseff	215.051m
self_gain	4.70537
ueff	22.055m
vbs	-217.882m

Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 (Saturation region of operation)

Simulation result of mosfet M5:

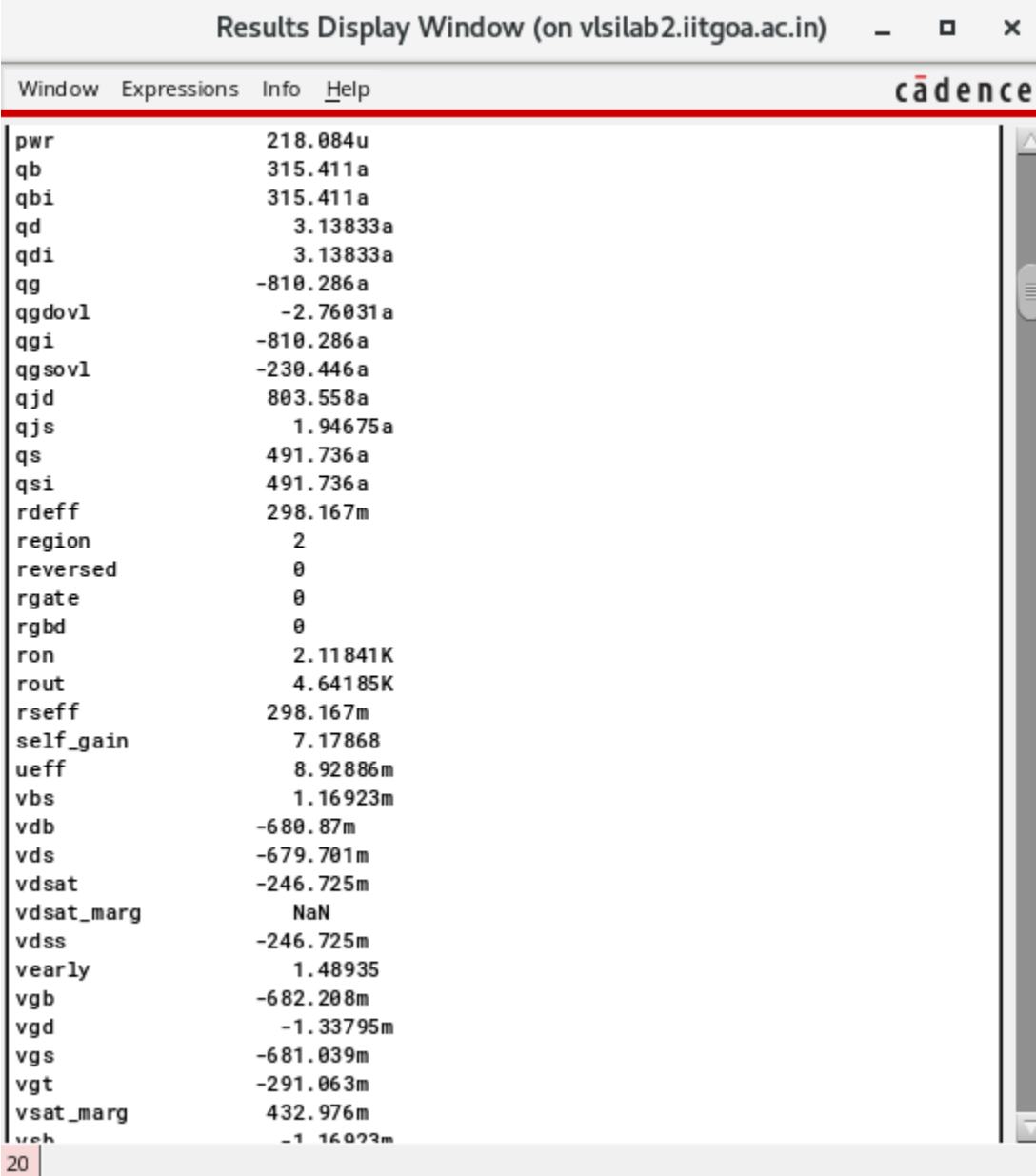
The screenshot shows the 'Results Display Window' from Cadence, titled 'Results Display Window (on vlsilab2.iitgoa.ac.in)'. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of variables and their corresponding values. The variables are listed on the left, and their values are on the right. The values are formatted with scientific notation or standard decimal notation, indicating units like 'a' (atto), 'f' (femto), 'm' (milli), and 'u' (micro). The variables include parameters like 'qb', 'qbi', 'qd', 'qdi', 'qg', 'qgdovl', 'qgi', 'qgsavl', 'qjd', 'qjs', 'qs', 'qsi', 'rdeff', 'region', 'reversed', 'rgate', 'rgbd', 'ron', 'rout', 'rseff', 'self_gain', 'ueff', 'vbs', 'vdb', 'vds', 'vdsat', 'vdsat_marg', 'vdss', 'vearly', 'vgb', 'vgd', 'vgs', 'vgt', 'vsat_marg', and 'vsb'.

Variable	Value
qb	-320.447a
qbi	-320.447a
qd	-207.695a
qdi	-207.695a
qg	1.17009f
qgdovl	202.953a
qgi	1.17009f
qgsavl	331.924a
qjd	-570.212a
qjs	-3.14017a
qs	-641.952a
qsi	-641.952a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	333.398
rout	894.544
rseff	215.051m
self_gain	3.98098
ueff	21.5778m
vbs	-988.457u
vdb	215.066m
vds	214.077m
vdsat	144.507m
vdsat_marg	NaN
vdss	144.507m
vearly	574.393m
vgb	549.751m
vgd	334.686m
vgs	548.763m
vgt	129.389m
vsat_marg	69.5701m
vsb	988.457u

Figure: Simulation result of DC operating point analysis.

Observation: M5 is in region 2 (Saturation region of operation)

Simulation result of mosfet M3:

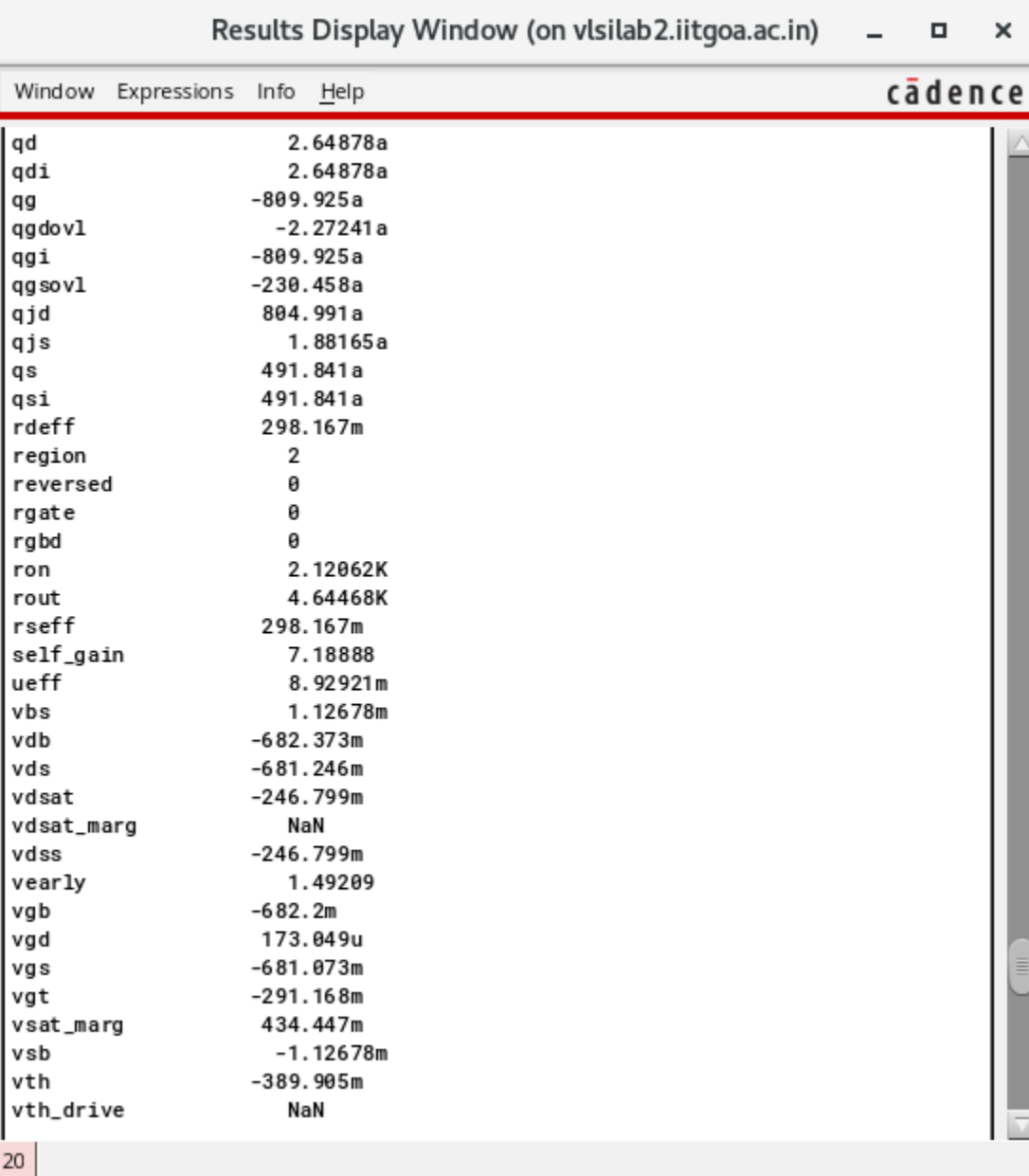


Window	Expressions	Info	Help	
pwr	218.084u			
qb	315.411a			
qbi	315.411a			
qd	3.13833a			
qdi	3.13833a			
qg	-810.286a			
qgdovl	-2.76031a			
qgi	-810.286a			
qgsovl	-230.446a			
qjd	803.558a			
qjs	1.94675a			
qs	491.736a			
qsi	491.736a			
rdeff	298.167m			
region	2			
reversed	0			
rgate	0			
rgbd	0			
ron	2.11841K			
rout	4.64185K			
rseff	298.167m			
self_gain	7.17868			
ueff	8.92886m			
vbs	1.16923m			
vdb	-680.87m			
vds	-679.701m			
vdsat	-246.725m			
vdsat_marg	NaN			
vdss	-246.725m			
vearly	1.48935			
vgb	-682.208m			
vgd	-1.33795m			
vgs	-681.039m			
vgt	-291.063m			
vsat_marg	432.976m			
vsh	-1.16923m			

Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 (Saturation region of operation)

Simulation result of mosfet M4:



Parameter	Value
qd	2.64878a
qdi	2.64878a
qg	-809.925a
qgdovl	-2.27241a
qgi	-809.925a
qgsovl	-230.458a
qjd	804.991a
qjs	1.88165a
qs	491.841a
qsi	491.841a
rdeff	298.167m
region	2
reversed	0
rgate	0
rgbd	0
ron	2.12062K
rout	4.64468K
rseff	298.167m
self_gain	7.18888
ueff	8.92921m
vbs	1.12678m
vdb	-682.373m
vds	-681.246m
vdsat	-246.799m
vdsat_marg	NaN
vdss	-246.799m
vearly	1.49209
vgb	-682.2m
vgd	173.049u
vgs	-681.073m
vgt	-291.168m
vsat_marg	434.447m
vsb	-1.12678m
vth	-389.905m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M4 is in region 2 (Saturation region of operation)

It is Verified that all the 5 transistors are in region 2 i.e Saturation region of operation.

(b) Perform the AC analysis of the circuit and find out the differential gain and 3 dB frequency.

Below are simulation results of the AC response analysis :

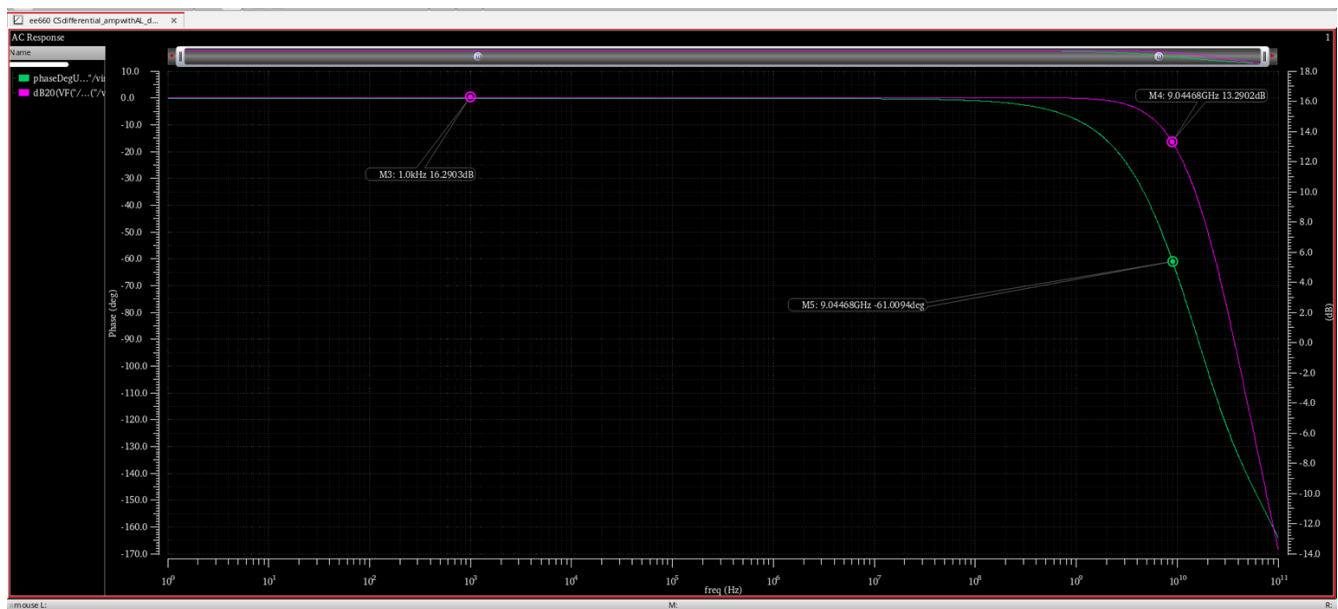


Figure: Plot showing Ac response analysis results (Vout,Vin1 considered)

Observations: From the above Ac Analysis plots we can say that :

1. Low frequency gain is **16.290dB**
2. 3dB cutoff frequency is **9.044 GHz**
3. Phase difference between the input and output at the 3 dB frequency: **-61Degrees.**

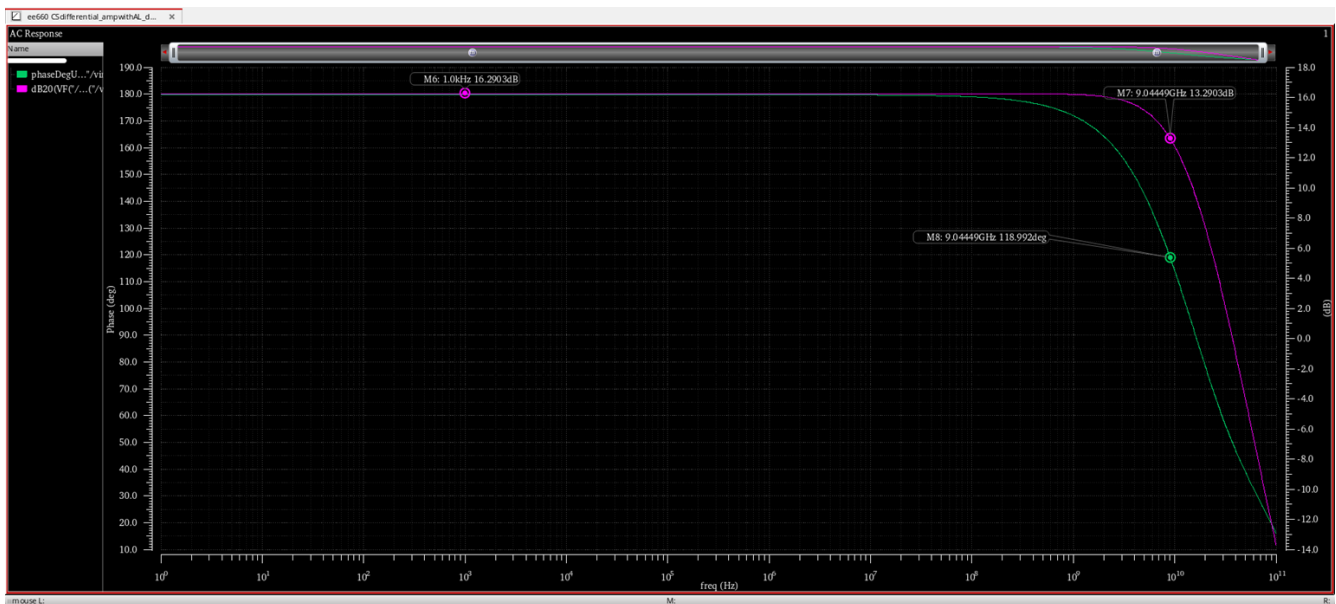


Figure: Plot showing Ac response analysis results (Vout,Vin2 considered)

Observations: From the above Ac Analysis plots we can say that :

1. Low frequency gain is **16.290dB**
2. 3dB cutoff frequency is **9.044 GHz**
3. Phase difference between the input and output at the 3 dB frequency: **118.99 Degrees.**

(c) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Below are the results of Transient analysis at $v_{in} = 10\text{mV}$:

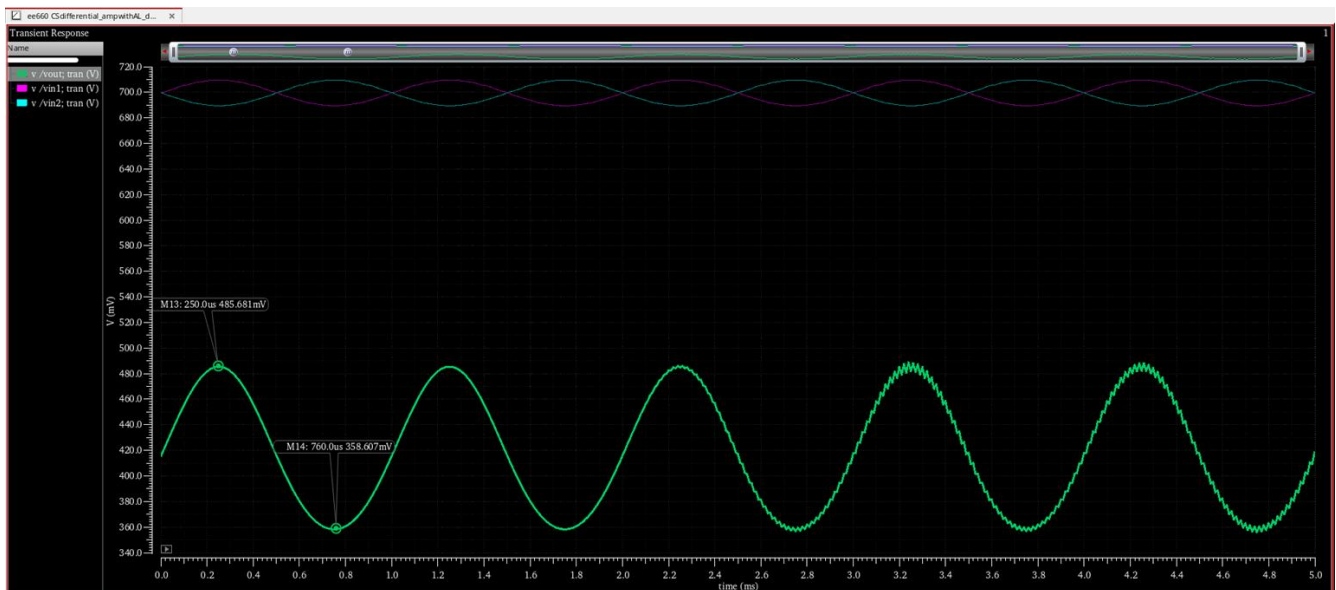


Figure: Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

Below are the results of Transient analysis at $v_{in} = 20\text{mV}$:

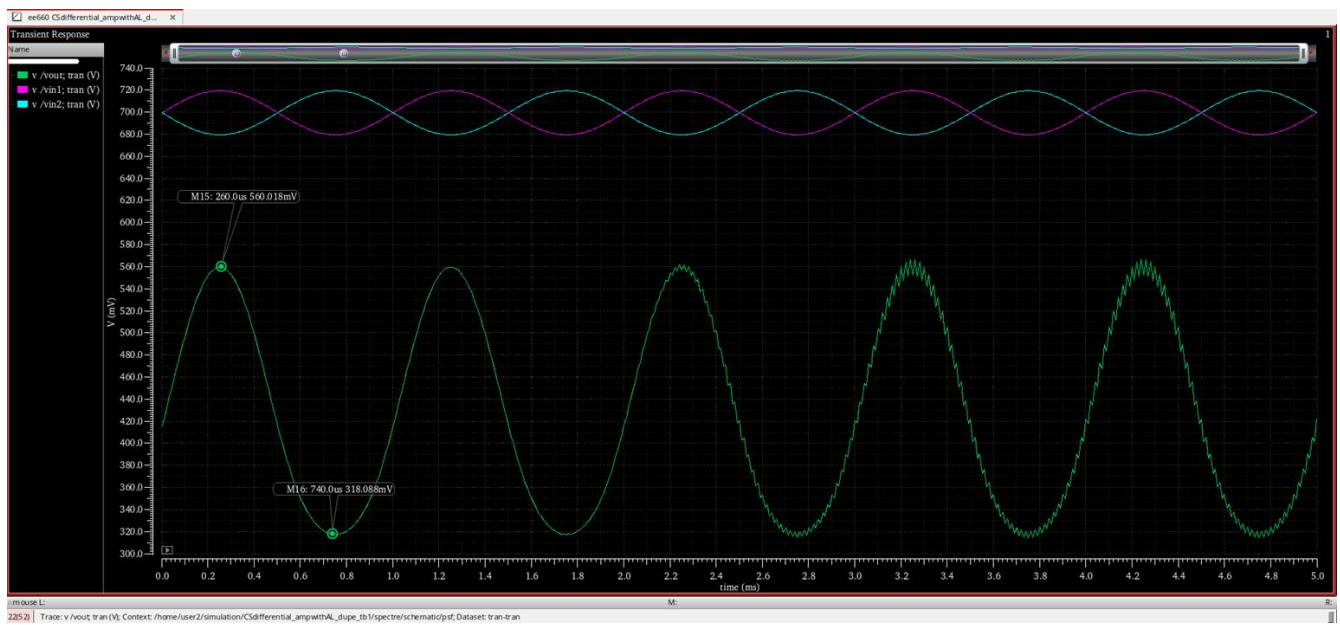


Figure: Plot showing transient analysis simulation result (V_{out} w.r.to V_{in1}, V_{in2})

Comparison between pre- and post-layout simulation results:

1. **DC Analysis:** When $V_b = 0.55\text{ V}$, and $V_{in,dc} = 0.7\text{ V}$ both pre-layout and post-layout results confirm that all transistors (M1, M2, M3, M4, M5) are in the **saturation region**.

2. **AC Analysis:**

- i) **Low frequency gain:**

The pre-layout gain is **16.807 dB**, while the post-layout gain is **16.290 dB** which resulted in **0.517 dB drop in gain**. This is mainly due to the resistance and capacitance developed by metal wires and interconnects in the layout.

- ii) **3dB cutoff frequency:**

3 dB cutoff frequency dropped from **19.27 GHz** (pre-layout) to **9.044 GHz** (post-layout). This is mainly due to the fact that large interconnects are used in layout design due to which parasitic capacitance has increased significantly. Also, contact and via resistances introduced in layout design. All these factors reduced bandwidth since bandwidth is Inversely proportional to RC.

- iii) **Phase difference between the input and output at the 3 dB frequency:**

For pre-layout simulation the phase shift from **Vin1 to Vout** was **-56.39°**, but after for post-layout, it increased to **-61.00°**, adding an extra **-4.61° delay** due to parasitic effects.

For pre-layout simulation the phase shift from **Vin2 to Vout** was **123.60°**, but after for post-layout, it increased to **118.99°**, reducing by **4.61°** because of added resistance and capacitance in the circuit.

3. **Transient Analysis:**

At 10mV : pre –layout simulation has $V_{out,peak} : 504.97\text{mv}$, $V_{out,min} : 374.73\text{ mv}$
Post –layout simulation has $V_{out,peak} : 485\text{mv}$, $V_{out,min} : 358\text{ mv}$

At 20mV : pre –layout simulation has $V_{out,peak} : 586\text{ mv}$, $V_{out,min} : 328\text{ mv}$
Post –layout simulation has $V_{out,peak} : 560\text{mv}$, $V_{out,min} : 318\text{ mv}$

It is observed that there's a slight decrement in V_{out} values of post layout transient simulation. This is mainly due to the **Parasitic resistance in routing**, which causes voltage drops and reduces both peak and minimum output levels for layout.