



EE 660 VLSI Design Laboratory

Instructor: Nandakumar Nambath

Assignment-VIII

Submitted by: (L Sri Sai Swathi (2414202)

1. Design and simulate a two input CMOS NAND gate the circuit diagram of which is given below using 180 nm technology. Choose the aspect ratios of the transistors such that the worst case drive strength of the gate is the same as that of a reference CMOS inverter.

We have chosen W/L ratios of N1,N2,P1,P2 to be 240nm/60nm (Aspect ratio =4) to make sure worst case drive strength matches with that of reference CMOS inverter.

- (a) Using VDD as 1.8 V draw the VTC of the NAND gate using schematic level simulations for the following input patterns
- (b) Using the VTC calculate the values of the switching threshold and noise margins for the different input patterns listed above.

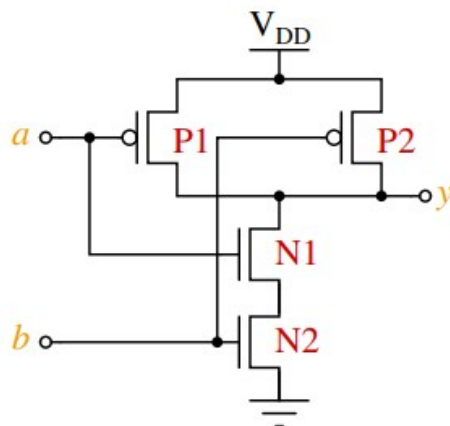


Figure: 2 input CMOS NAND gate circuit diagram

(l) $a = b = 0 \rightarrow 1$

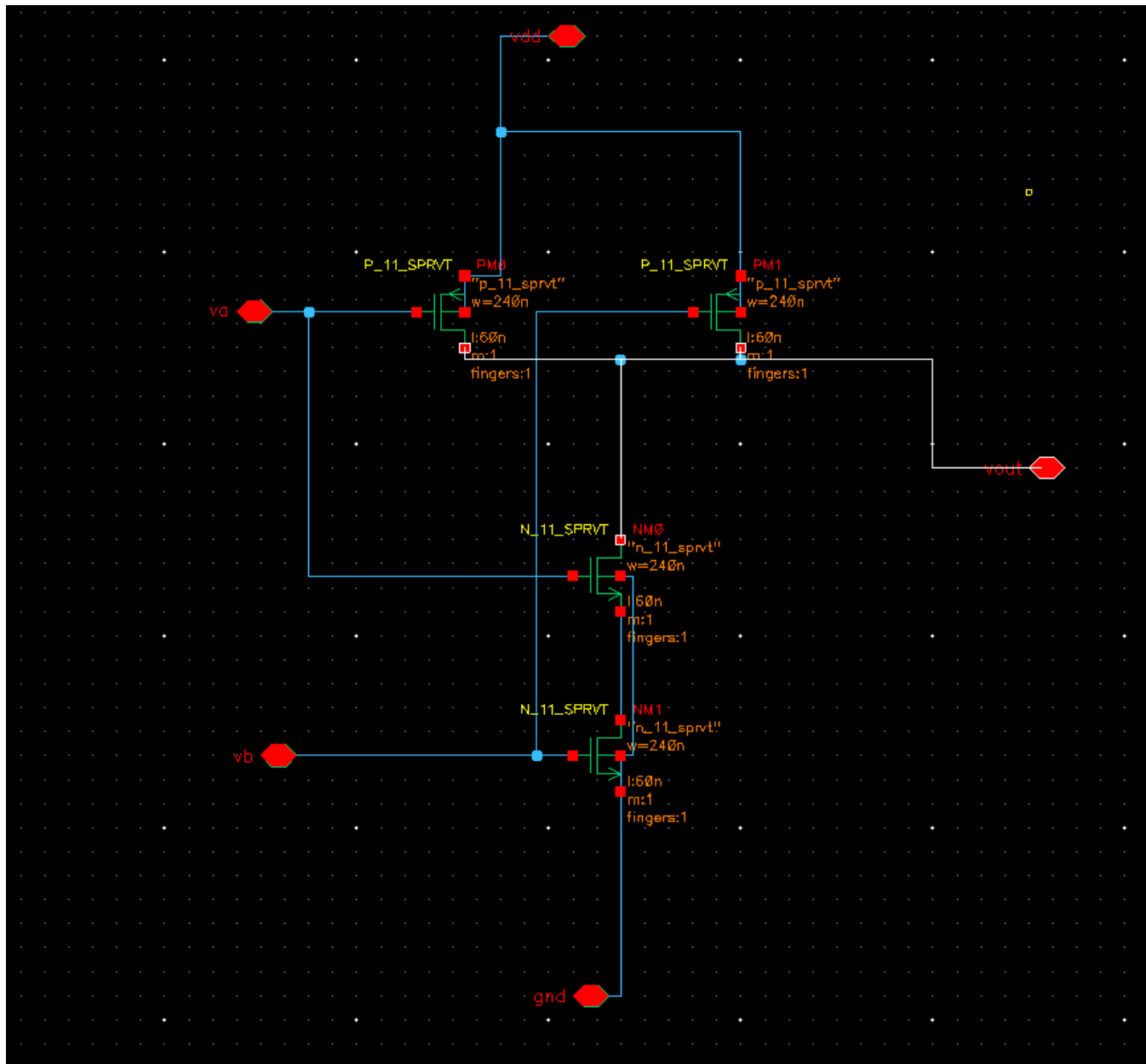


Figure : Schematic of two input CMOS NAND gate

Figure : Schematic of two input CMOS NAND gate

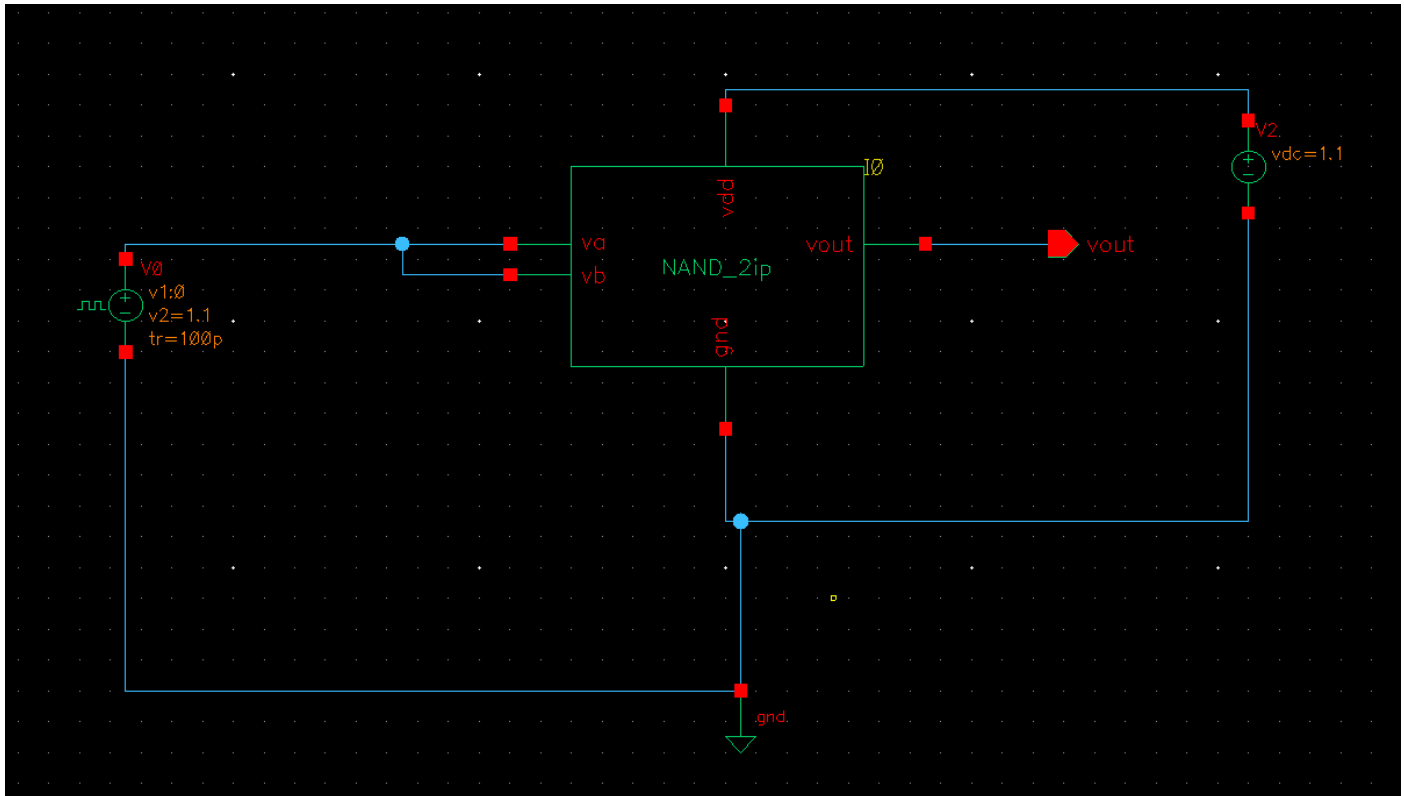


Figure : Schematic of two input CMOS NAND gate used for DC analysis

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with $V_{DD} = 1.1\text{V}$, swept input from 0 to 1.1V in steps of 0.01V.

Below are the simulation results and observations:

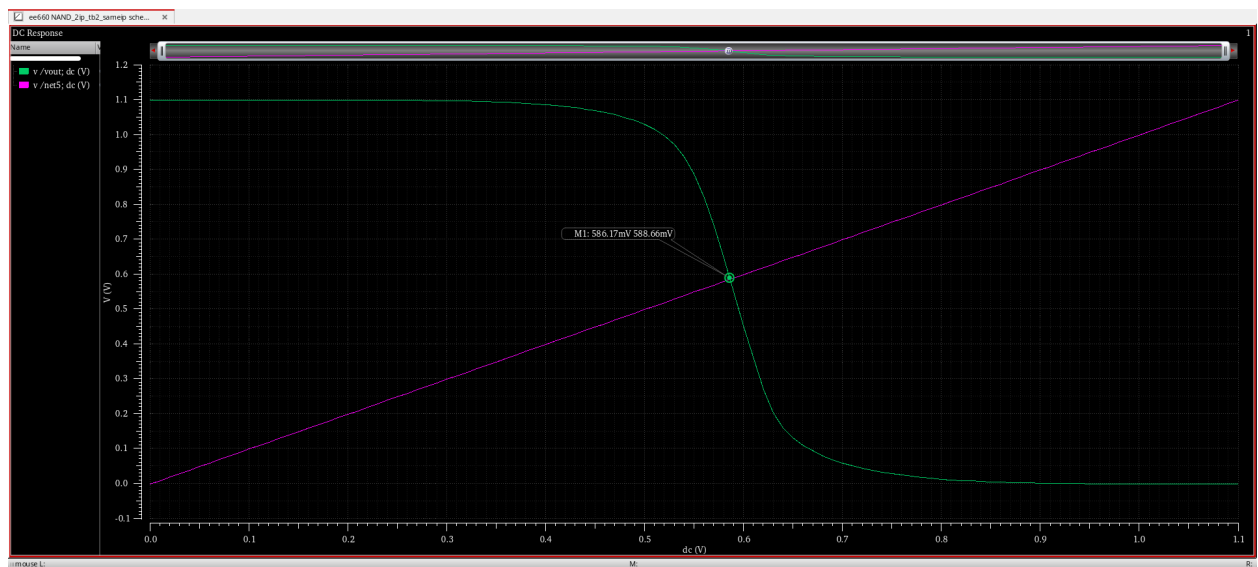


Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as **586.17mV**

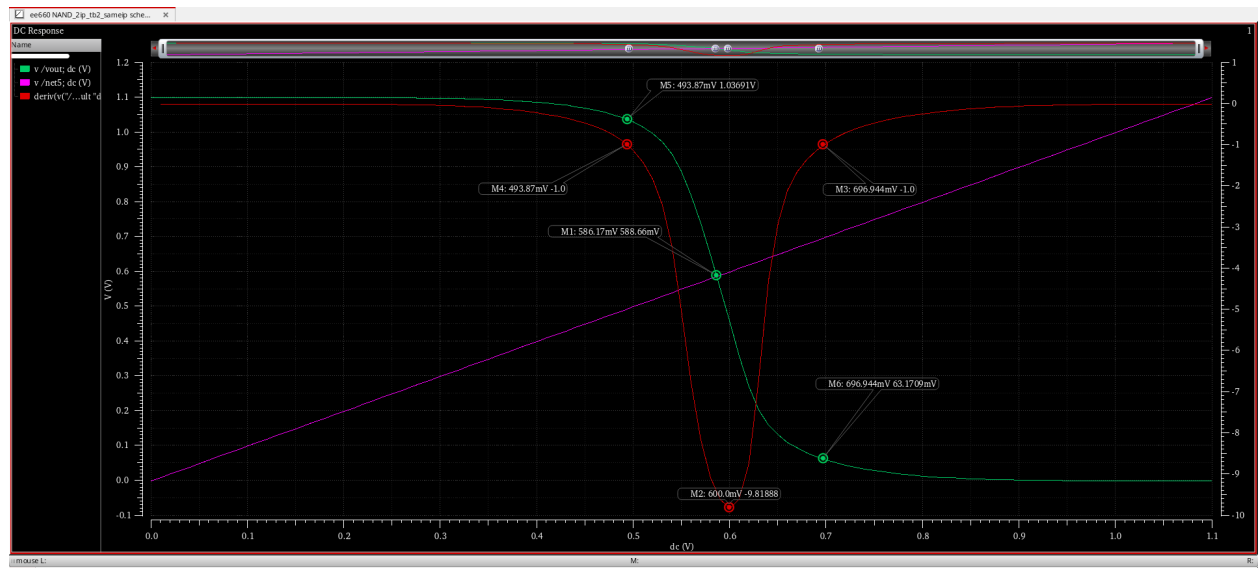


Figure : Plot showing Voltage gain , V_{OH} , V_{IH} , V_{OL} & V_{IL}

From the Plot shown above :

$V_{IL} = 493.87\text{mV}$, $V_{OH} = 1.0369\text{V}$

$V_{IH} = 696.944\text{mV}$

$V_{OL} = 63.17\text{mV}$

NOISE MARGINS:

$NMH = V_{OH} - V_{IH} = 0.339\text{V}$

$NML = V_{IL} - V_{OL} = 0.430\text{V}$

ii. $a = 1, b = 0 \rightarrow 1$

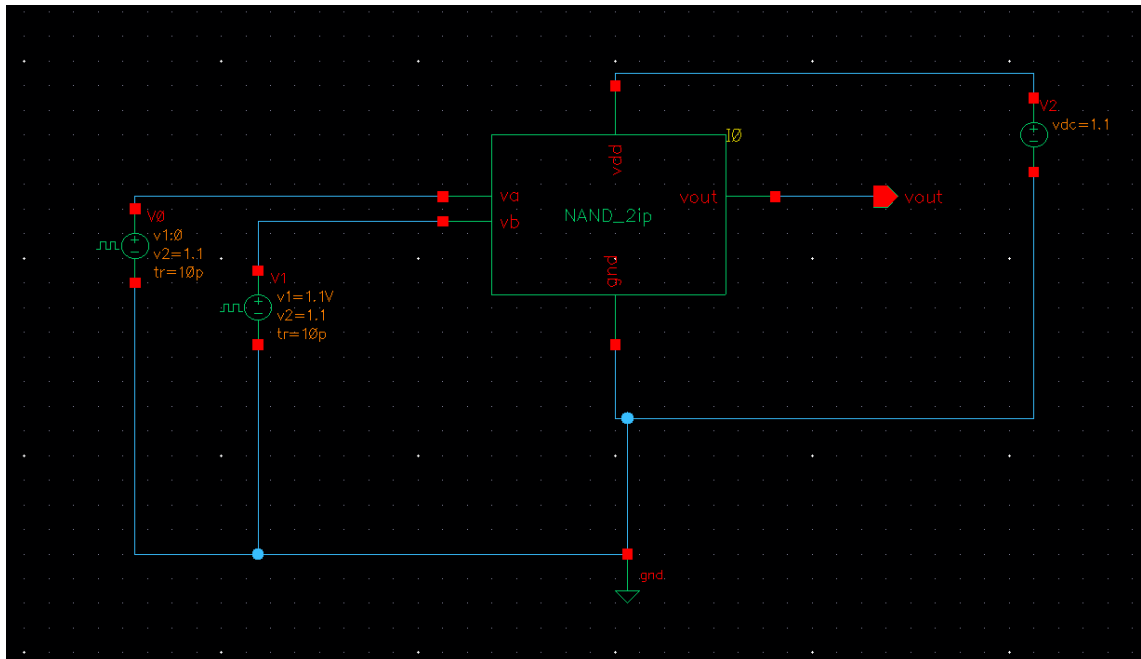


Figure : Schematic of two input CMOS NAND gate used for DC analysis

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with $V_{DD} = 1.1\text{v}$, swept $V_b = 0 \rightarrow 1$ from 0 to 1.1v in steps of 0.01v when $V_a = 1.1\text{V}$.

Below are the simulation results and observations:

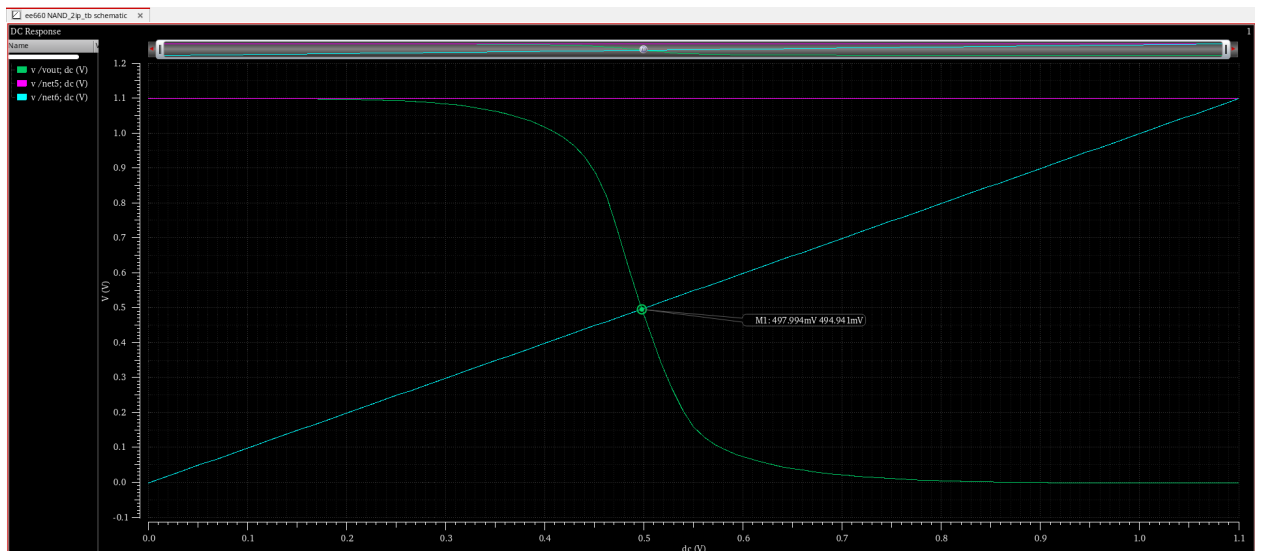


Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as 497.994mV

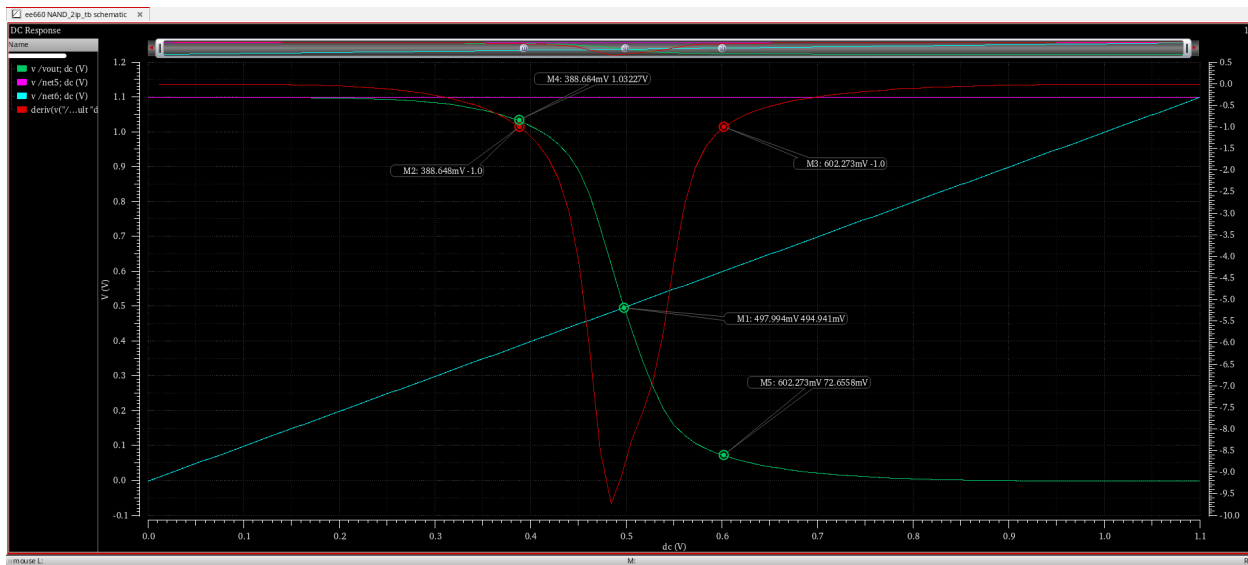


Figure : Plot showing Voltage gain , VOH,VIL ,VIH&VOL

From the Plot shown above :

$V_{IL}=388.684\text{mV}$, $V_{OH}=1.0322\text{V}$

$V_{IH}= 602.273\text{mV}$

$V_{OL}=72.655\text{mV}$

NOISE MARGINS:

$NMH = V_{OH}-V_{IH} = 0.429\text{V}$

$NML = V_{IL}-V_{OL} = 0.316\text{V}$

(III) $b = 1, a = 0 \rightarrow 1$

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with $V_{DD} = 1.1\text{v}$, swept $V_a = 0 \rightarrow 1$ from 0 to 1.1v in steps of 0.01v when $V_b = 1.1\text{V}$.

Below are the simulation results and observations:



Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as 510mV

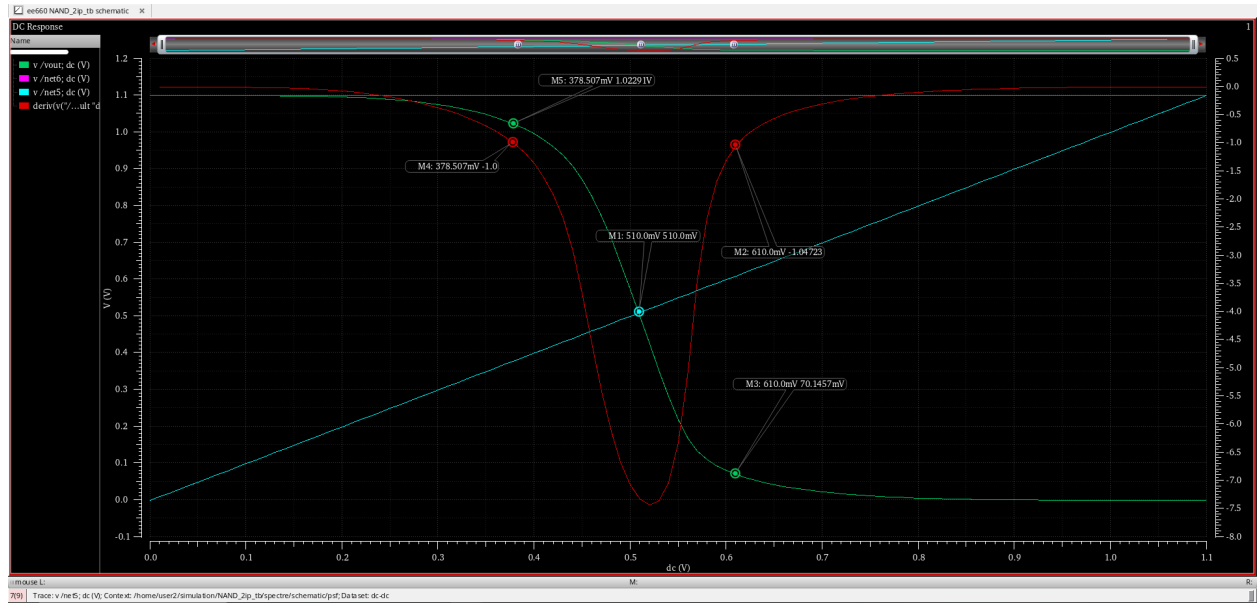


Figure : Plot showing Voltage gain , V_{OH} , V_{IL} , V_{IH} & V_{OL}

From the Plot shown above :

$V_{IL}=378.507\text{mV}$, $V_{OH}=1.022\text{V}$

$V_{IH}= 610.0\text{mV}$ $V_{OL}=70.145\text{mV}$

NOISE MARGINS:

$NMH = V_{OH} - V_{IH} = 0.412\text{V}$

$NML = V_{IL} - V_{OL} = 0.308\text{V}$

2. Connect a 100 fF load to the NAND gate. Tabulate the propagation delays using schematic simulations for the following input patterns:

- (a) $a = b = 0 \rightarrow 1$
- (b) $a = 1, b = 0 \rightarrow 1$
- (c) $a = 0 \rightarrow 1, b = 1$
- (d) $a = b = 1 \rightarrow 0$
- (e) $a = 1, b = 1 \rightarrow 0$
- (f) $a = 1 \rightarrow 0, b = 1$

a) $a = b = 0 \rightarrow 1$

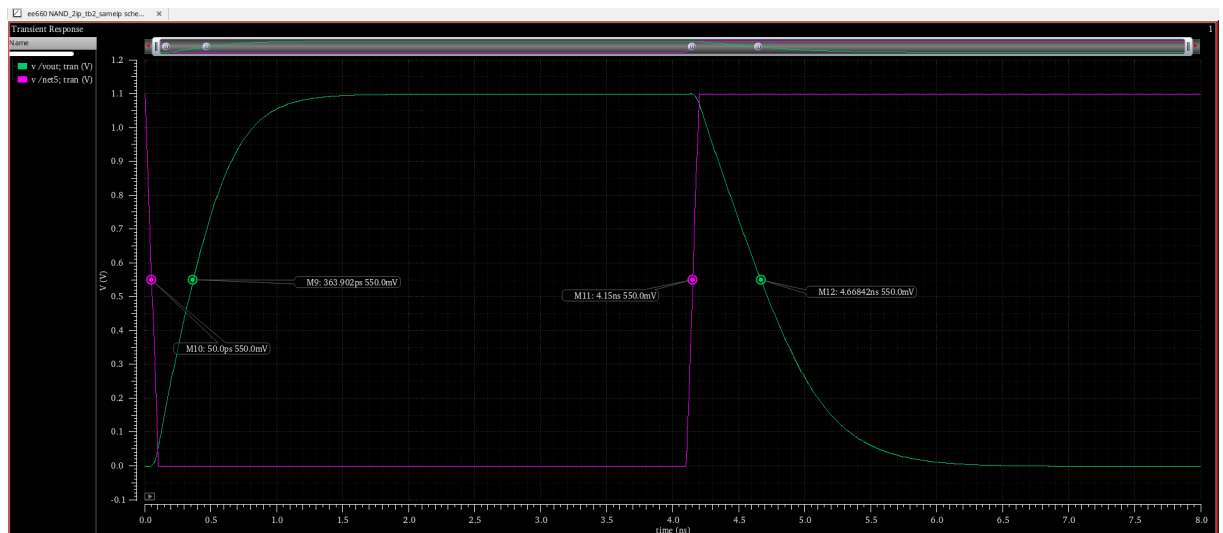


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is **316.16ps**

b) $a = 1, b = 0 \rightarrow 1$

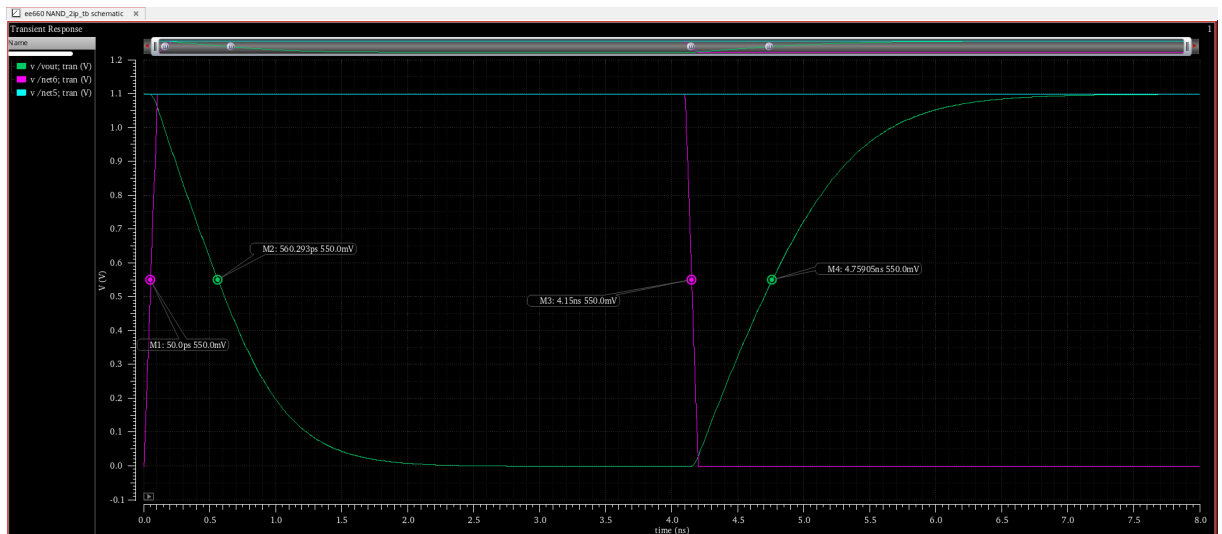


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 559.676ps

c) $b = 1, a = 0 \rightarrow 1$

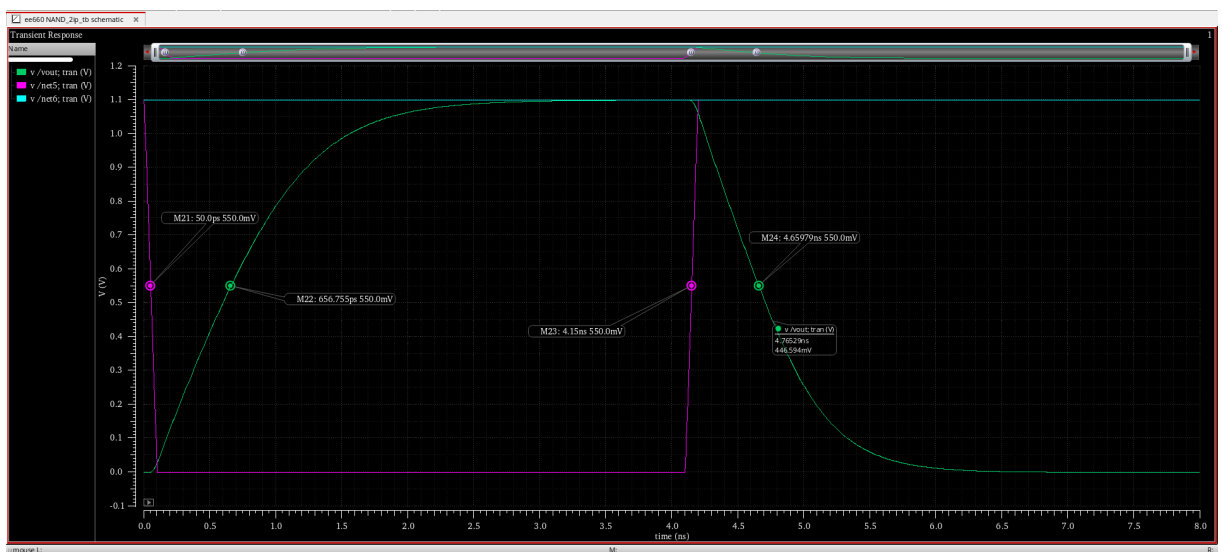


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 557.5ps

d) $a = b = 1 \rightarrow 0$

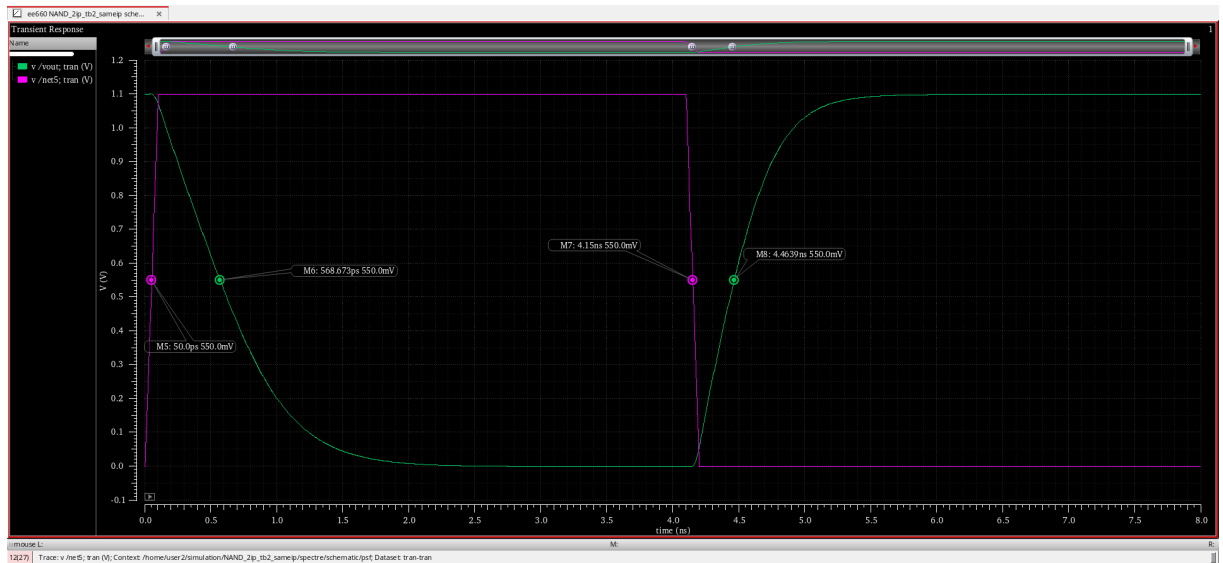


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 416.29ps

e) $a = 1, b = 1 \rightarrow 0$

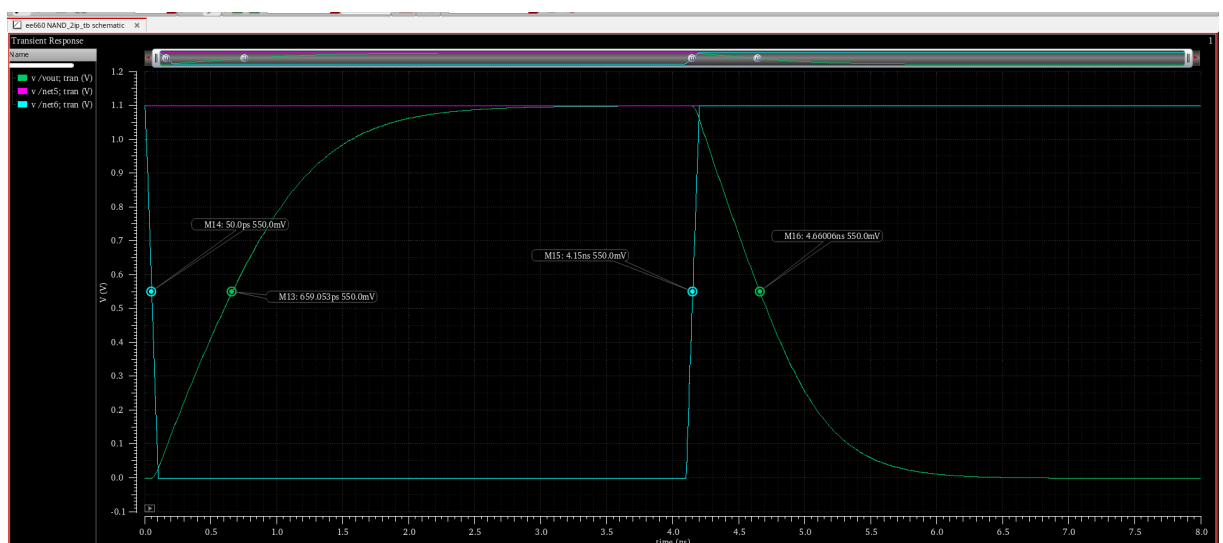


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 559.526 ns

f) $a = 1 \rightarrow 0, b = 1,$

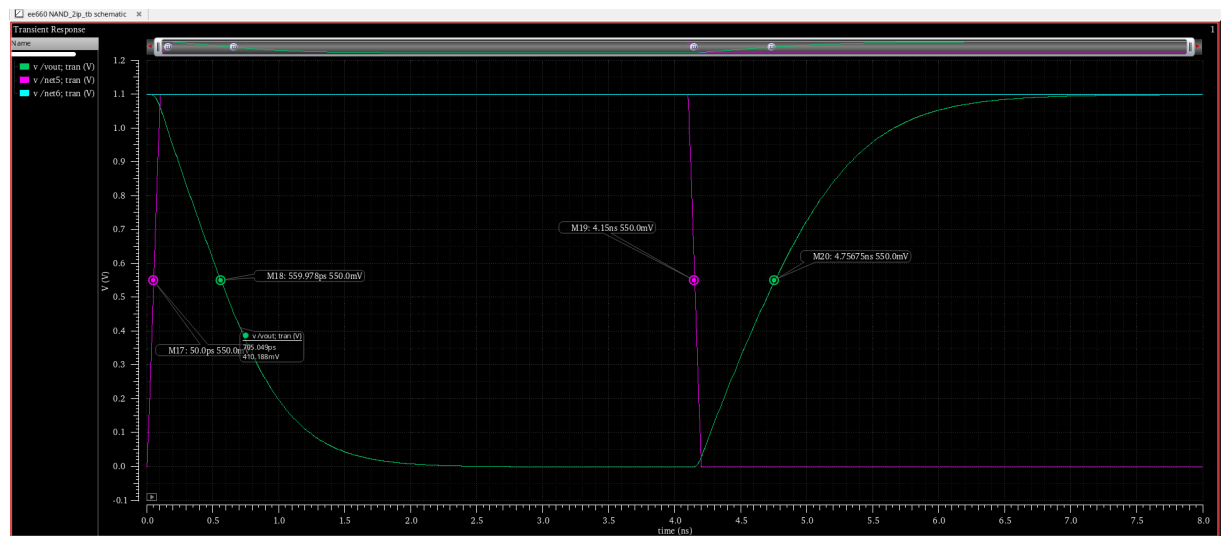


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 558.364 ns

Tabular representation of delay dependence on input patterns:

Input Data Pattern	Delay(ps)
$a = b = 0 \rightarrow 1$	316.16
$a = 1, b = 0 \rightarrow 1$	559.676
$a = 0 \rightarrow 1, b = 1$	557.5
$a = b = 1 \rightarrow 0$	416.29
$a = 1, b = 1 \rightarrow 0$	559.526
$a = 1 \rightarrow 0, b = 1,$	558.364

3. Draw a layout for the NAND gate with minimum area possible. Repeat questions 1 and 2 using post layout simulations and compare the values with the ones obtained through schematic simulations.

i)

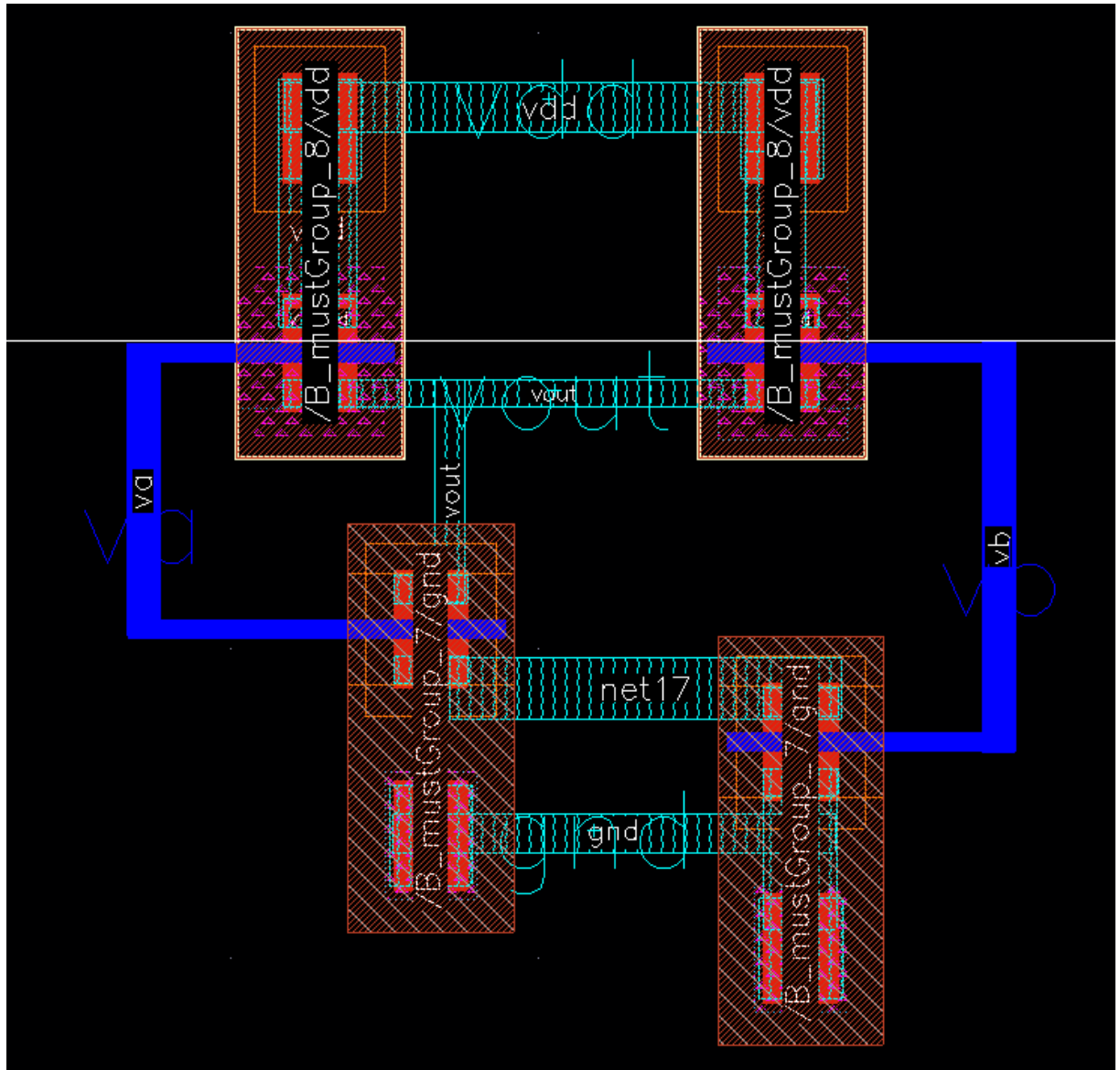


Figure: Layout of 2 input CMOS NAND gate

Below is the DRC Simulation result screenshot:

Calibre - RVE v2017.3.29.23 : NAND_2ip.drc.results

File View Highlight Tools Window Setup

Show All NAND_2ip, 2 Results (in 2 of 3 Checks)

Check / Cell	Results
Check PLY.D	1
Check L2,It1	1
Check DENSITY_PRINT_FILES	0

Rule File Pathname: /home/user2/2414202_Cadence//drc/_G-DF-LOGIC_MIXED_MODE65N-1P8M10F1U-SP-Calibre-drc-1.12.P1
Minimum POLY1 density over 1mm X 1mm area (stepped in 500um increments across the chip) is 15%.
Exclude CAD_TESTKEY_MARK

Check PLY.D

DRC Summary Report - NAND_2ip.drc.summary

File Edit Options Windows

```

===== CALIBRE::DRC-H SUMMARY REPORT =====
Execution Date/Time: Thu Apr 17 11:54:53 2025
Calibre Version: v2017.3.29.23 Fri Sep 1 13:55:54 PDT 2017
Rule File Pathname: /home/user2/2414202_Cadence//drc/_G-DF-LOGIC_MIXED
Rule File Title:
Layout System: GDS
Layout Path(s): NAND_2ip.calibre.db
Layout Primary Cell: NAND_2ip
Current Directory: /home/user2/2414202_Cadence/drc
User Name: user2
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: NAND_2ip.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: NAND_2ip.drc.summary (REPLACE)
Geometry Flaggings: ACUTE = NO SKEW = YES ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: NO
=====
-- RUNTIME WARNINGS
=====

```

Below is the LVS simulation result screenshot:

Calibre - RVE v2017.3.29.23 : NAND_2ip.lvs.results

File View Highlight Tools Window Setup

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
NAND_2ip ED	NAND_2ip	9L, 5S	1L, 1S	5L, 5S

Cell NAND_2ip Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

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*****
***** CORRECT *****
*****

```

LAYOUT CELL NAME: NAND_2ip
SOURCE CELL NAME: NAND_2ip

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	6	6	
Instances:	2	2	NI (4 pins) HP (4 pins)
Total Inst:	4	4	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	5	5	
Instances:	1	1	NAND2 (3 pins)

LVS Report File - NAND_2ip.lvs.report

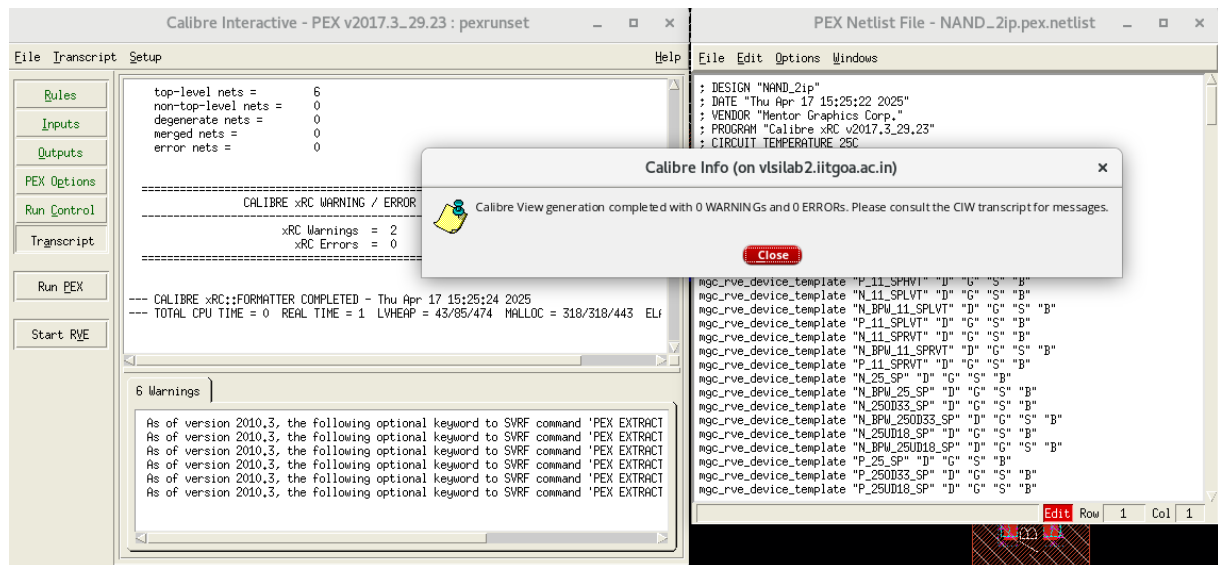
File Edit Options Windows

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*****
***** CALIBRE SYSTEM *****
***** LVS REPORT *****
*****
REPORT FILE NAME: NAND_2ip.lvs.report
LAYOUT NAME: /home/user2/2414202_Cadence/lvs/NAND_2ip.sp
SOURCE NAME: /home/user2/2414202_Cadence/lvs/NAND_2ip.sp.net
RULE FILE: /home/user2/2414202_Cadence/lvs/_G-DF-LOGIC_MIXED.MO
DRC: Calibre LVS 65nm LOGIC/MIXED MODE Standard Ports
CREATION TIME: Thu Apr 17 11:59:44 2025
CURRENT DIRECTORY: /home/user2/2414202_Cadence/lvs
USER NAME: user2
CALIBRE VERSION: v2017.3.29.23 Fri Sep 1 13:55:54 PDT 2017
OVERALL COMPARISON RESULTS

```

Below is the PEX simulation result screenshot:



$$i) a = b = 0 \rightarrow 1$$

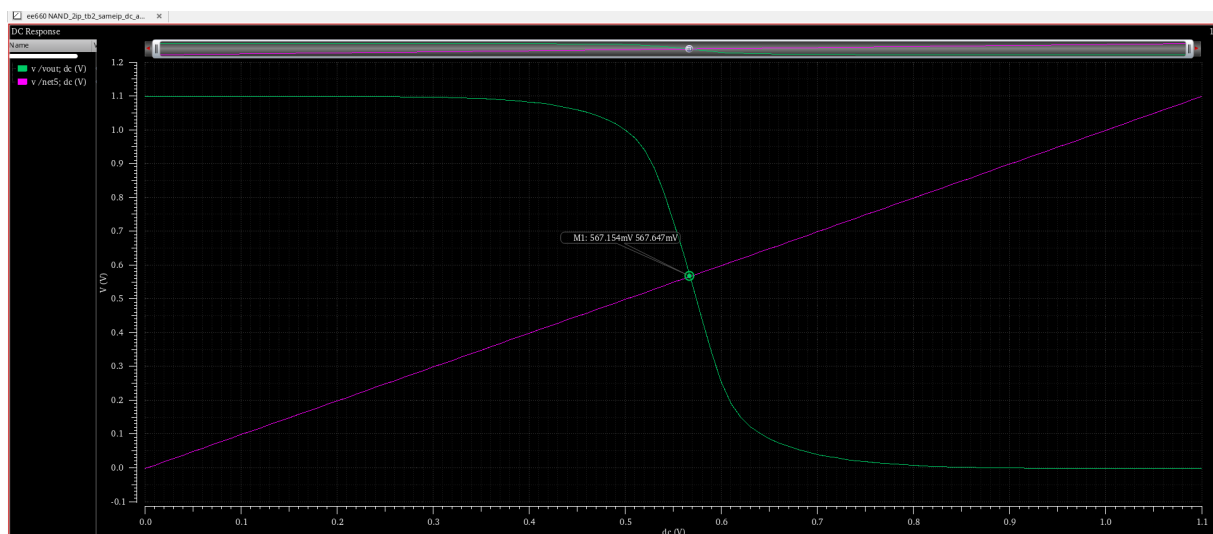


Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as 567.154mV

ii) $a = 1, b = 0 \rightarrow 1$

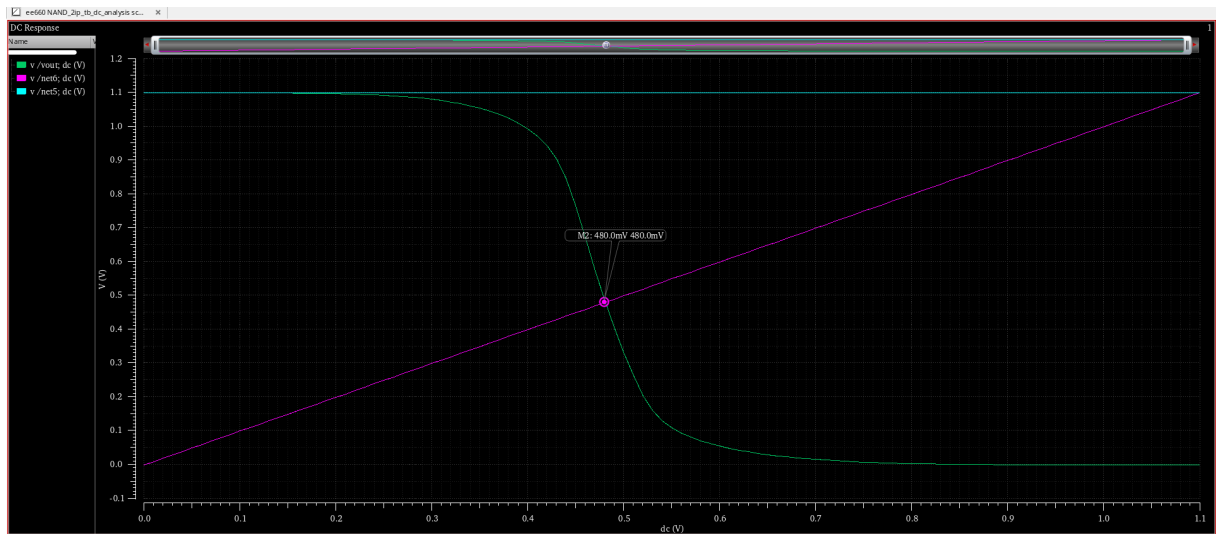


Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as 480mV

iii) $b = 1, a = 0 \rightarrow 1$

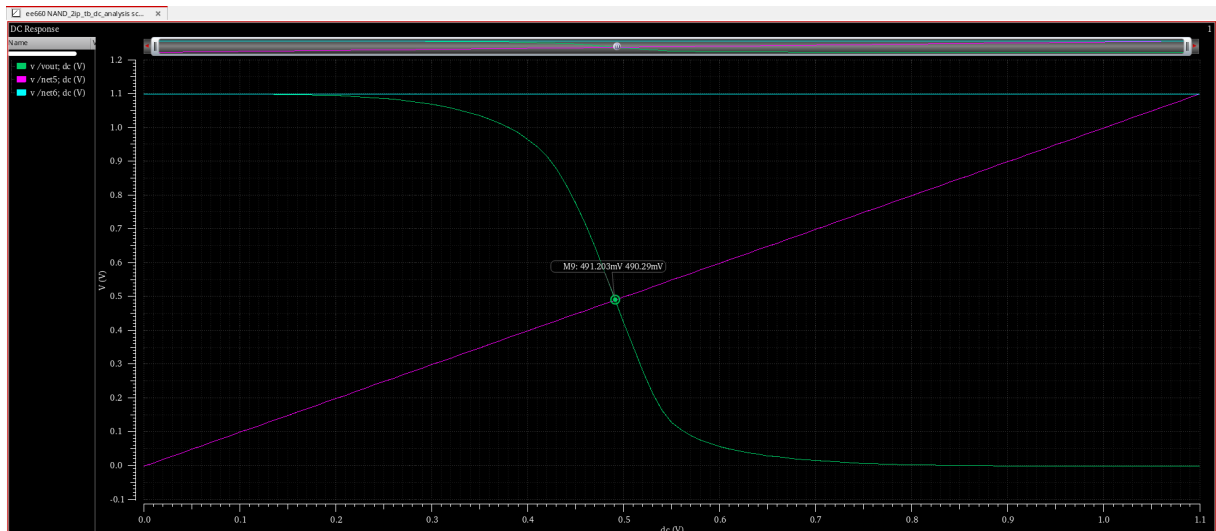


Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as 491.203mV

b) Using the VTC calculate the values of the switching threshold and noise margins for the different input patterns listed above.

i) $a = b = 0 \rightarrow 1$

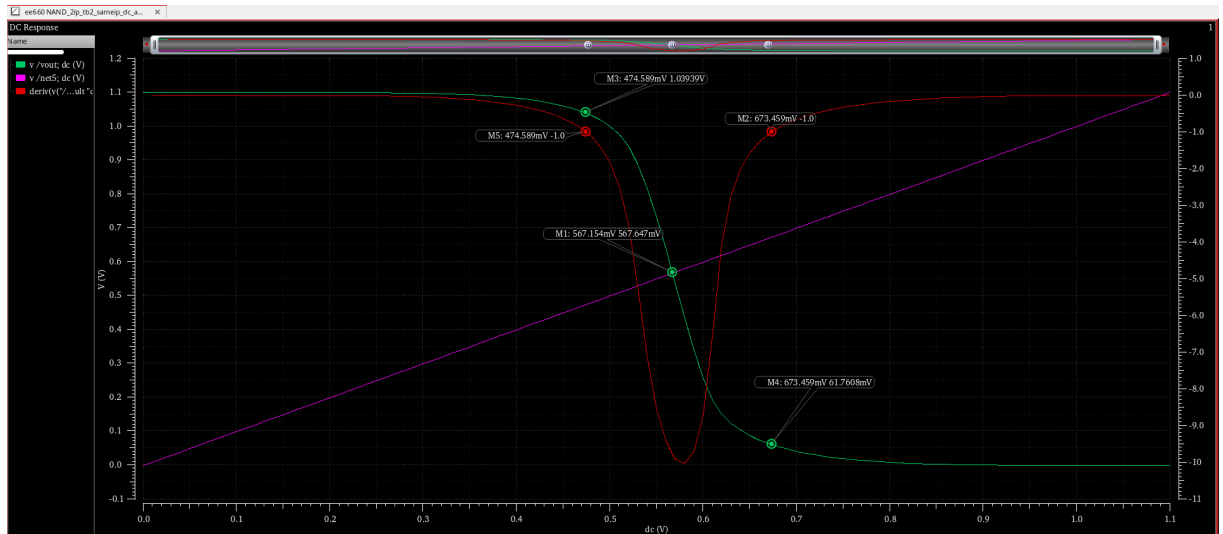


Figure : Plot showing Voltage gain , V_{OH} , V_{IL} , V_{IH} & V_{OL}

From the Plot shown above :

$V_{IL} = 474.589\text{mV}$, $V_{OH} = 1.039\text{V}$

$V_{IH} = 673.459\text{mV}$

$V_{OL} = 61.7609\text{mV}$

NOISE MARGINS:

$NMH = V_{OH} - V_{IH} = 0.365\text{V}$

$NML = V_{IL} - V_{OL} = 0.412\text{V}$

ii) $a = 1, b = 0 \rightarrow 1$

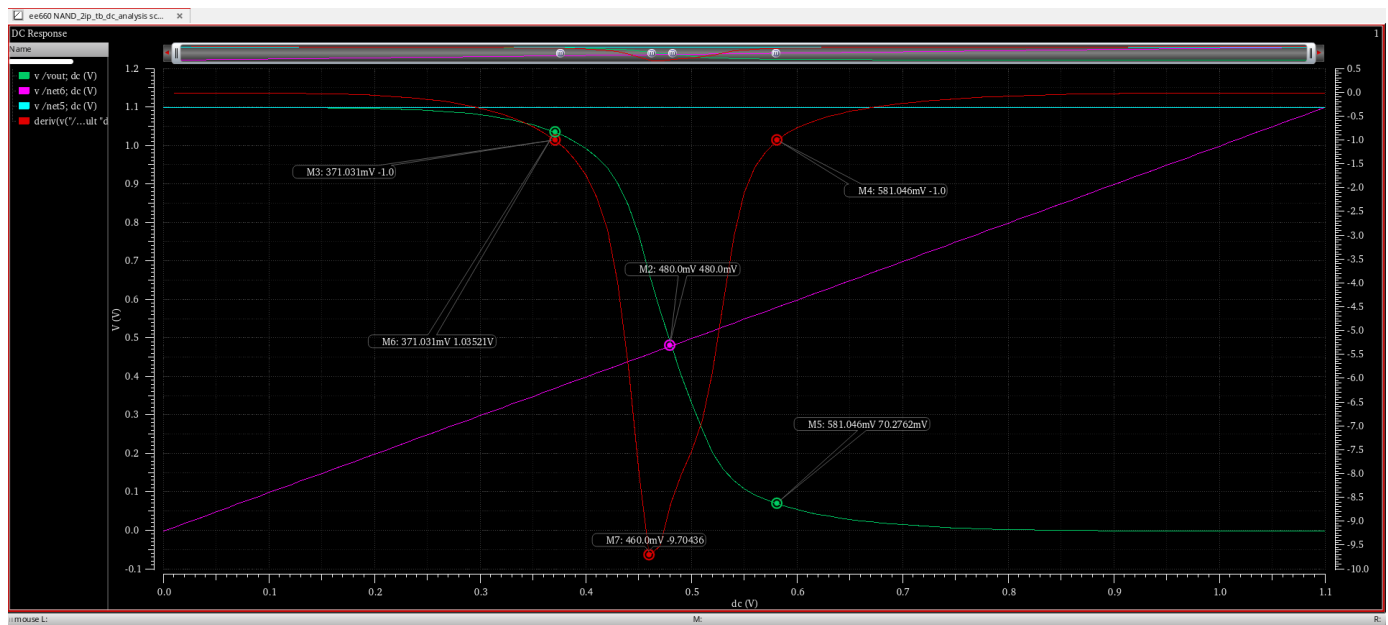


Figure : Plot showing Voltage gain , VOH,VIL,VIH&VOL

From the Plot shown above :

$V_{IL} = 371.031\text{mV}$, $VOH = 1.0352\text{V}$

$VIH = 581.064\text{mV}$

$VOL = 70.2762\text{mV}$

NOISE MARGINS:

$NMH = VOH - VIH = 0.453\text{V}$

$NML = VIL - VOL = 0.300\text{V}$

iii) $b = 1, a = 0 \rightarrow 1$

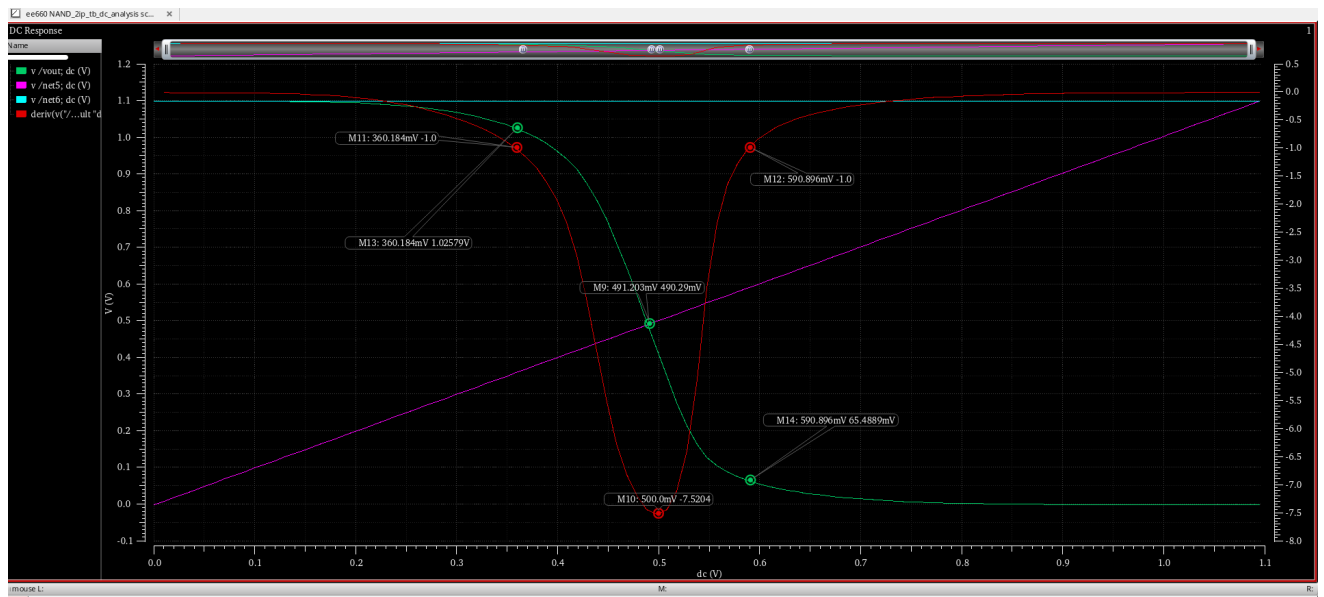


Figure : Plot showing Voltage gain , V_{OH} , V_{IL}

, V_{IH} & V_{OL}

From the Plot shown above :

$V_{IL} = 360.184\text{mV}$,

$V_{OH} = 1.025\text{V}$

$V_{IH} = 590.896\text{mV}$

$V_{OL} = 65.488\text{mV}$

NOISE MARGINS:

$NMH = V_{OH} - V_{IH} = 0.434\text{V}$

$NML = V_{IL} - V_{OL} = 0.294\text{V}$

2. Connect a 100 fF load to the NAND gate. Tabulate the propagation delays using schematic simulations for the following input patterns:

a) $a = b = 0 \rightarrow 1$

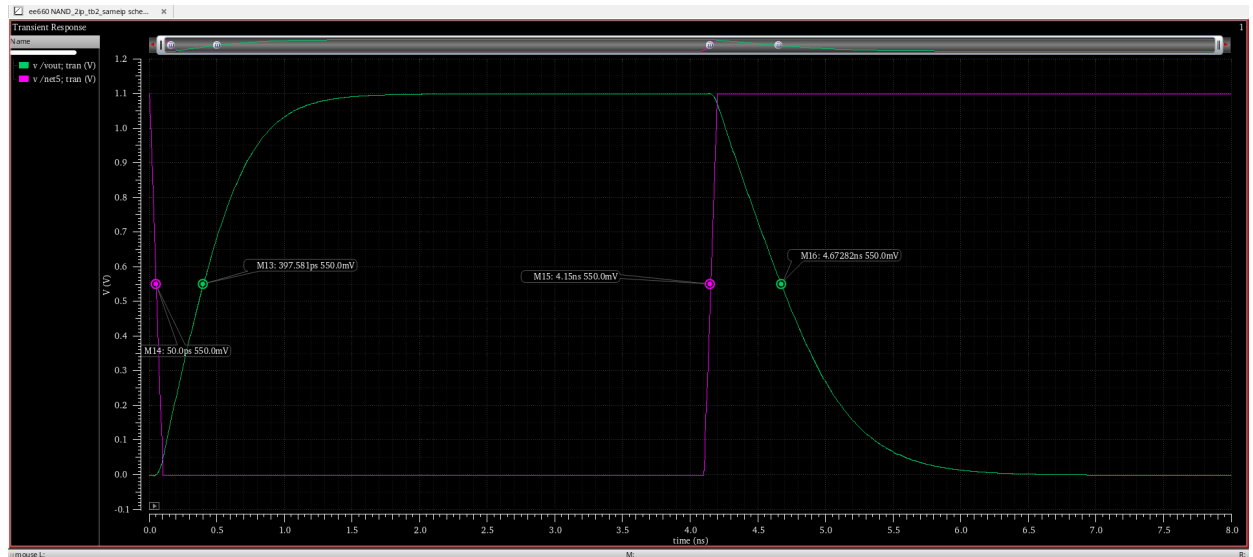


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 432.705 ps

b) $a = 1, b = 0 \rightarrow 1$

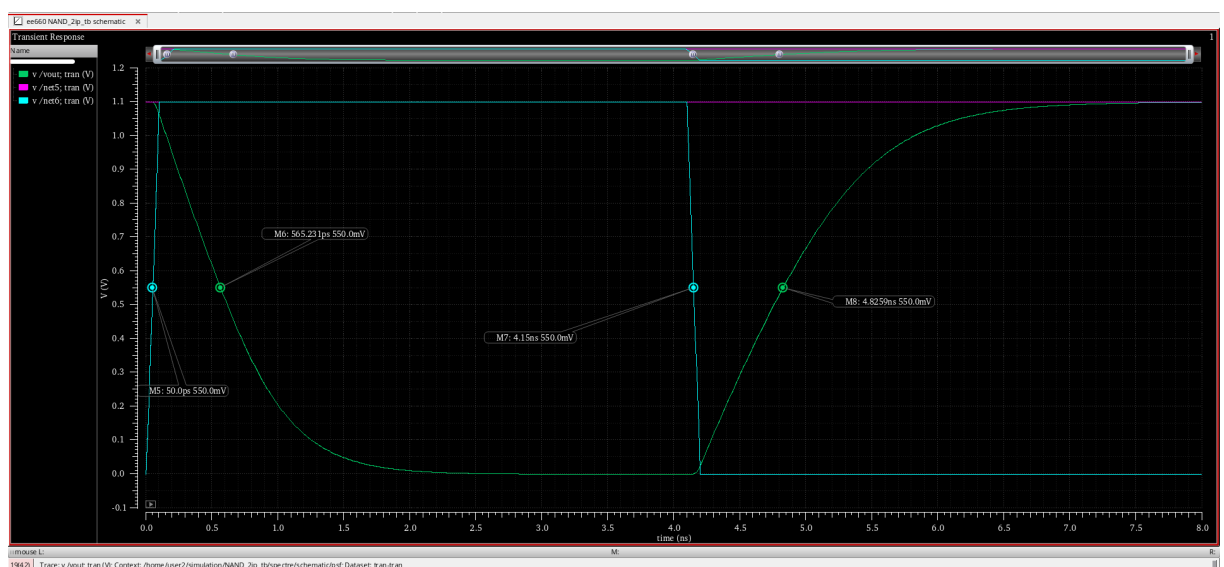


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 595.59 ns

c) $a = 0 \rightarrow 1, b = 1$

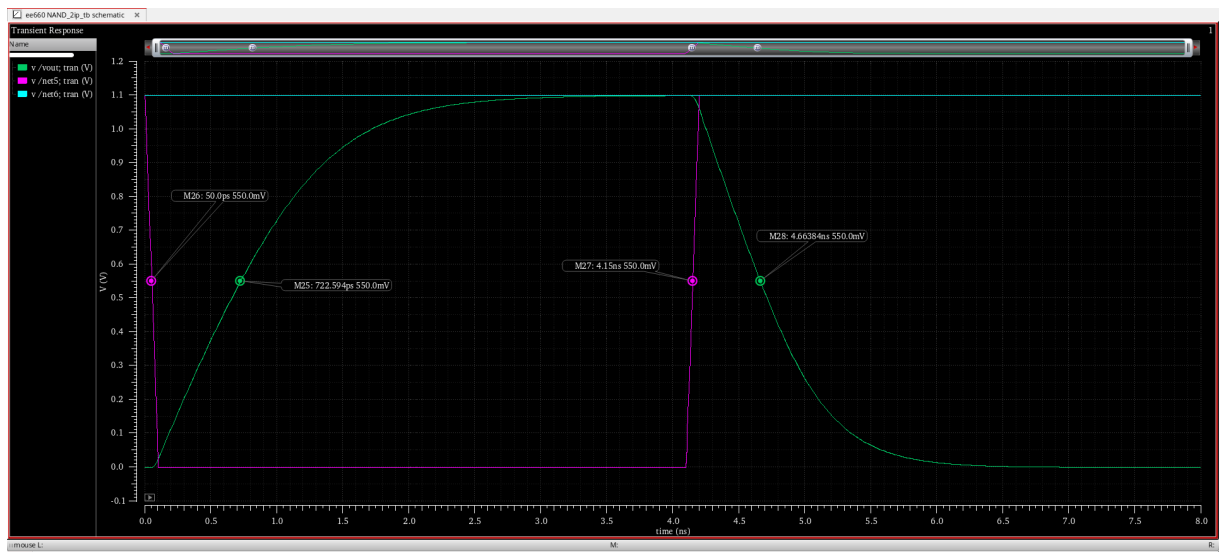


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 592.5ps

d) $a = b = 1 \rightarrow 0$

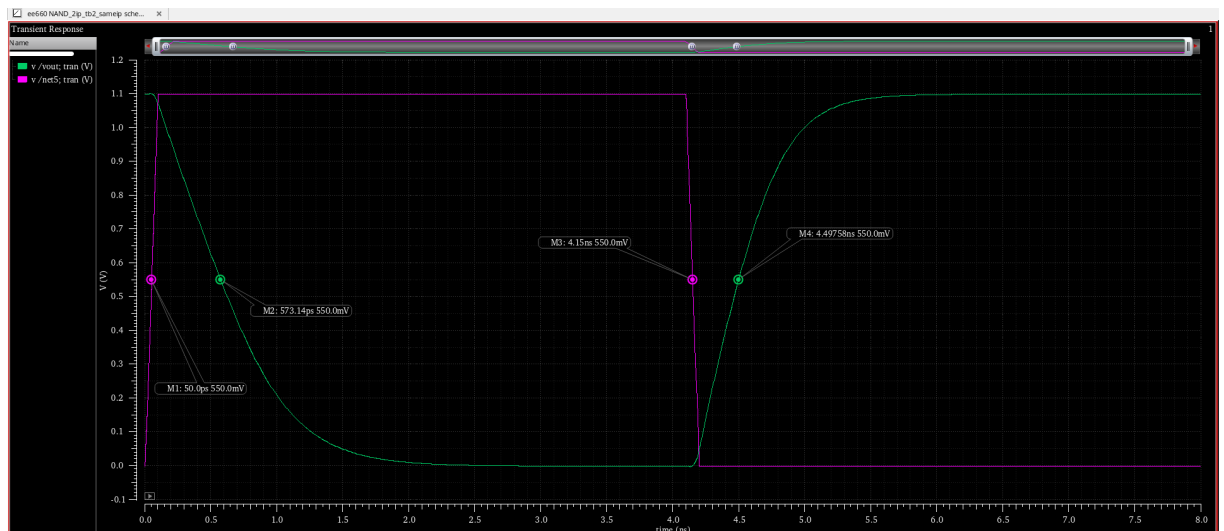


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 435.07 ps

e) $a = 1, b = 1 \rightarrow 0$

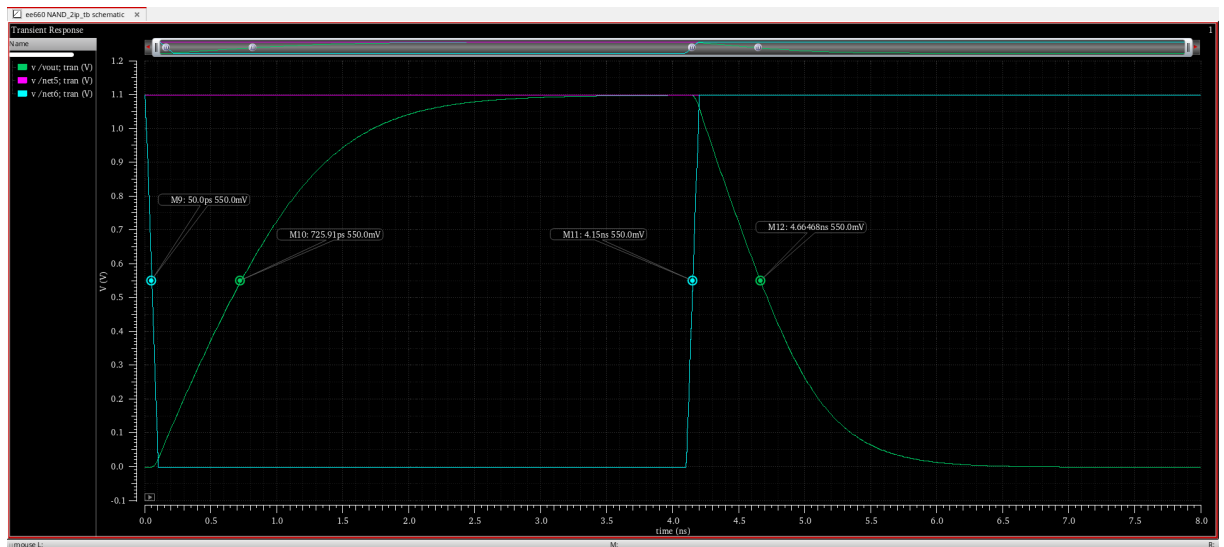


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 595.295 ns

f) $a = 1 \rightarrow 0, b = 1,$

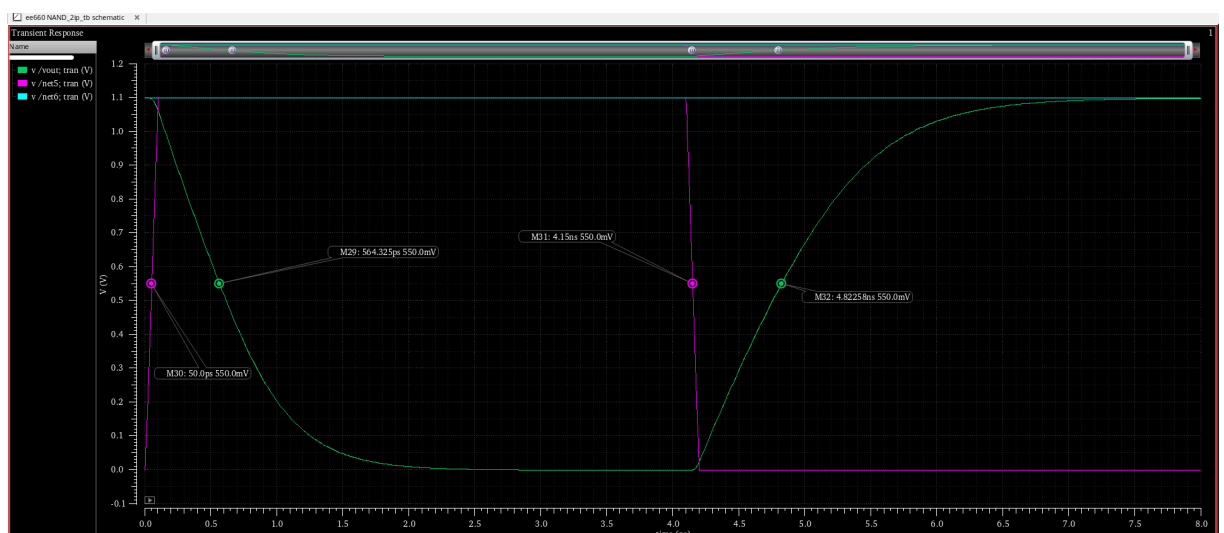


Figure : Simulated transient response of the 2 input CMOS NAND gate

Observation: From the above plot it is observed that the Propagation delay is 593s

Tabular representation of delay dependence on input patterns:

Input Data Pattern	Delay(ps)
a = b = 0 → 1	432.705
a = 1, b = 0 → 1	595.59
a = 0 → 1, b = 1	592.5
a = b = 1 → 0	435.07
a = 1, b = 1 → 0	595.295
a = 1 → 0, b = 1,	593

Comparison between schematic and post layout simulations:

Input Pattern	VM(V)(Schematic Simulation)	VM(V)(Post Layout Simulation)
$a = b = 0 \rightarrow 1$	0.586	0.567
$a = 1, b = 0 \rightarrow 1$	0.497	0.48
$b = 1, a = 0 \rightarrow 1$	0.51	0.491

Table showing VM w.r.to input pattern for schematic and post layout simulations

Observations:

1) When both V_a and V_b are simultaneously transitioning from low to high, both transistors in the pull up network are ON simultaneously for $v_a=v_b=0$, representing strong pull up. Also, **due to balanced drive strengths and transistor sizing** it is observed that switching threshold is symmetrically close to $V_{DD}/2$ (i.e 0.55) for both schematic and post layout simulation.

2) In 2nd and 3rd input patterns only one of pull up devices is on. Hence, the **VTC is shifted to the left as a result of the weaker PUN**. But there's a slight difference between the shift that's happening which is mainly due to the state of internal node between series NMOS devices.

Both schematic and Post -layout exhibiting the same behaviour for all the 3 input patterns but there's a very slight decrement in VM value for post layout simulation mainly due to the fact that nmos transistors are stacked which would reduce capacitance at the interconnect because of overlapping of source of N1 and Drain of N2.

Input Pattern	NML(V)(Schematic Simulation)	NMH(V)(Schematic Simulation)	NML(V)(Post Layout Simulation)	NMH(V)(Post Layout Simulation)
$a = b = 0 \rightarrow 1$	0.430	0.339	0.412	0.365
$a = 1, b = 0 \rightarrow 1$	0.316	0.429	0.3	0.453
$b = 1, a = 0 \rightarrow 1$	0.308	0.412	0.294	0.434

Table showing Noise margins for schematic and post layout simulations

Observations:

1. It is observed that noise margins in both schematic and post layout simulations are **input/pattern dependant**.

2. In post-layout simulation, extra factors like wiring resistance and capacitance are considered. These make small changes, like slightly improving **NMH** due to better handling of high voltages, and slightly lowering **NML** because of increased voltage drops at low levels.

Input Data Pattern	Delay(ps) (Schematic Simulation)	Delay(ps) (Post Layout Simulation)
a = b = 0 → 1	316.16	432.705
a = 1, b = 0 → 1	559.676	595.59
a = 0 → 1, b = 1	557.5	592.5
a = b = 1 → 0	416.29	435.07
a = 1, b = 1 → 0	559.526	595.295
a = 1 → 0, b = 1,	558.364	593

Table showing delay dependence on input patterns for schematic and post layout simulations

Observations:

1. In both the post layout and schematic simulations input transition (**a = b = 1 → 0**) results in a smaller delay, compared with case in which only one input is driven low.
2. In Post Layout Simulations, Delay Increment has been observed for all the input patterns. This is mainly due to fact that the parasitic resistance and capacitance from the interconnects, which can **slow down** certain transitions and **increase delay**.