# EE 660 VLSI Design Laboratory

Instructor: **Nandakumar Nambath**

***Assignment-VIII***

Submitted by: **( L Sri Sai Swathi (2414202)**

**1. Design and simulate a two input CMOS NAND gate the circuit diagram of which is given below using 180 nm technology. Choose the aspect ratios of the transistors such that the worst case drive strength of the gate is the same as that of a reference CMOS inverter.**

We have chosen W/L ratios of N1,N2,P1,P2 to be 240nm/60nm (Aspect ratio =4) to make sure worst case drive strength matches with that of reference CMOS inverter.

**(a) Using VDD as 1.8 V draw the VTC of the NAND gate using schematic level simulations for the following input patterns**

**(b) Using the VTC calculate the values of the switching threshold and noise margins for the different input patterns listed above.**

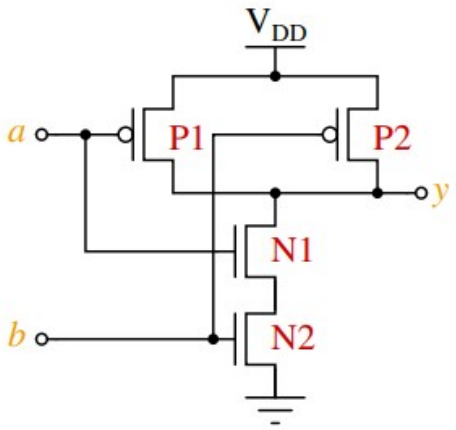


*Figure: 2 input CMOS NAND gate circuit diagram*

**(I) a = b = 0 → 1**

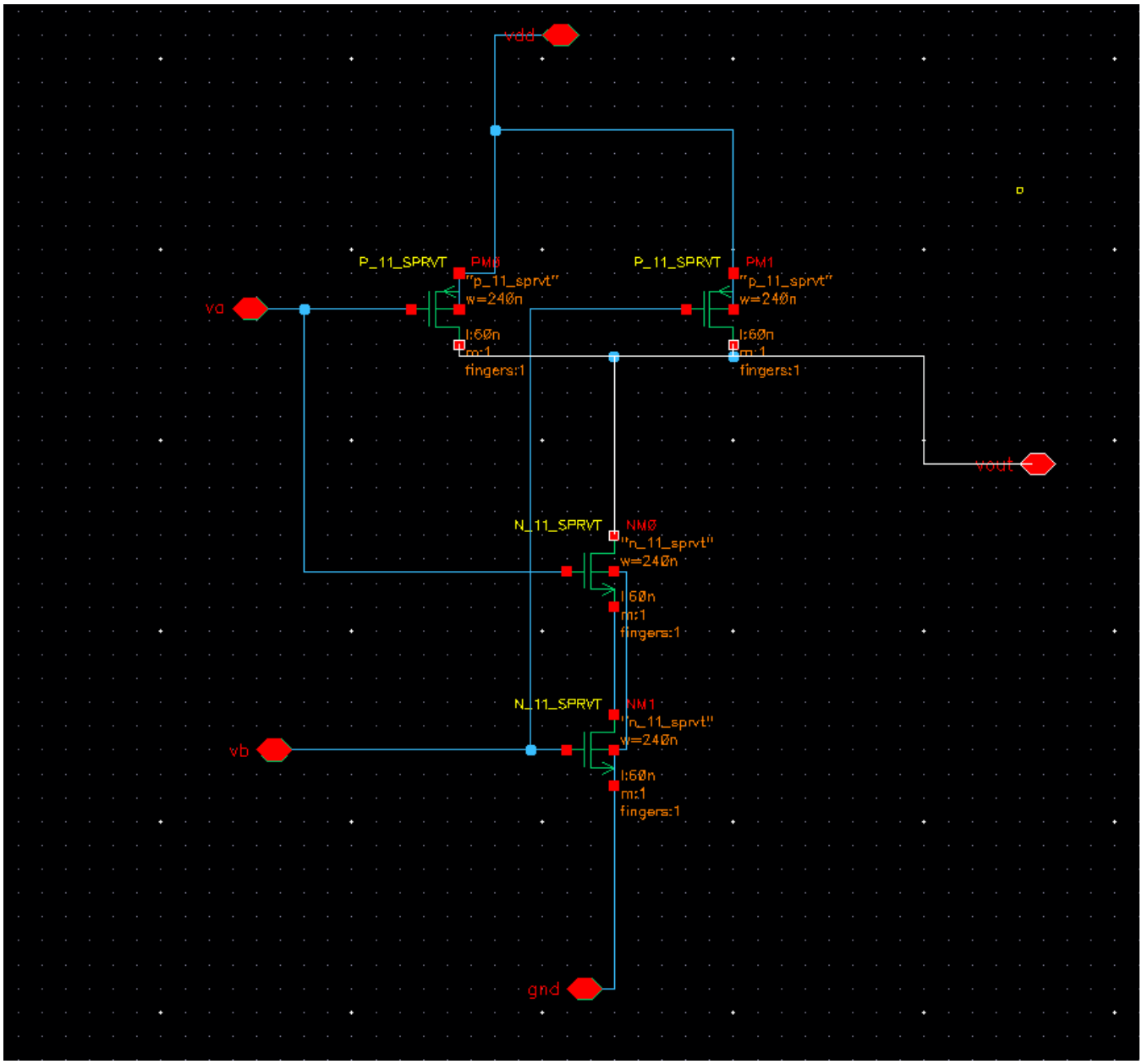


*Figure : Schematic of two input CMOS NAND gate*

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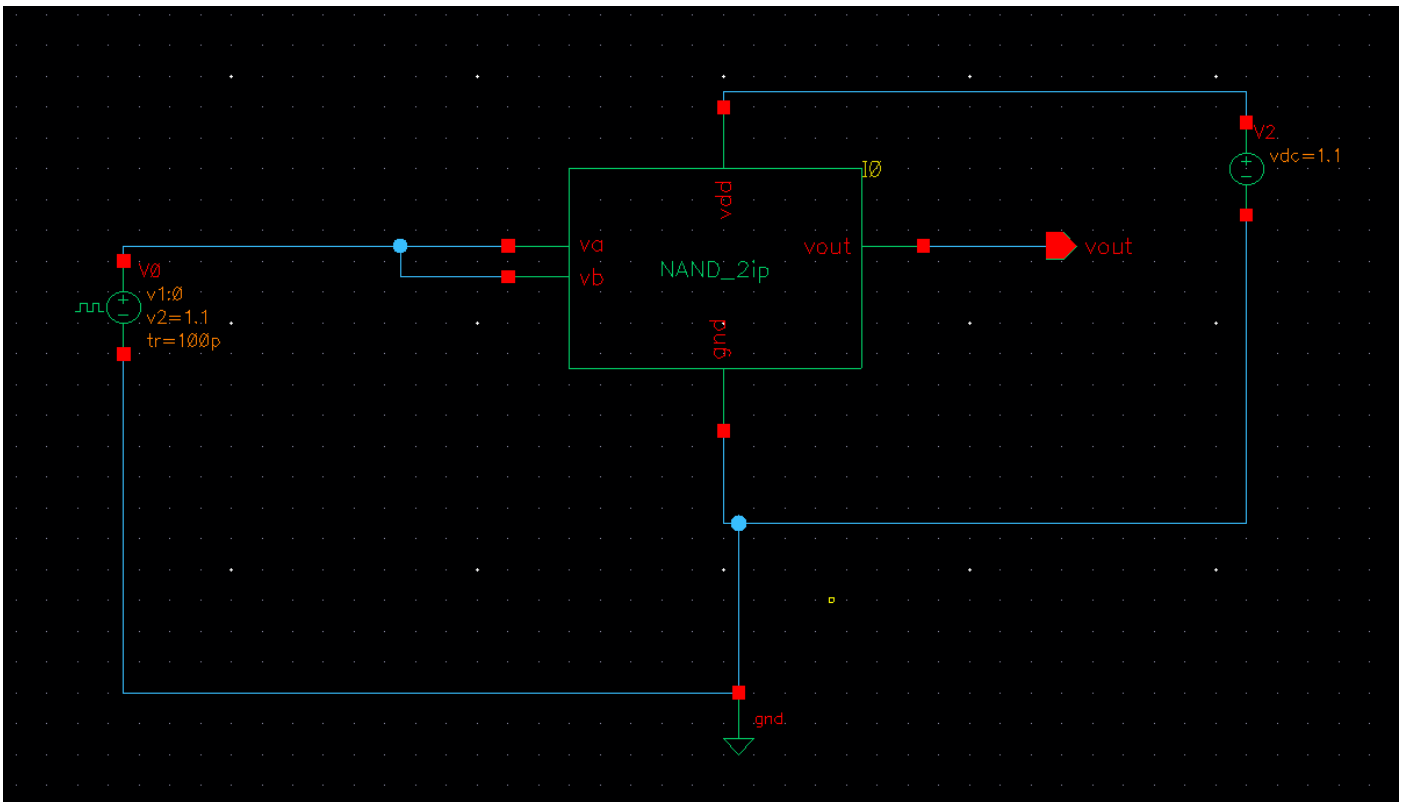



*Figure : Schematic of two input CMOS NAND gate used for DC analysis*

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with VDD =1.1v ,sweeped input from 0 to 1.1v in steps of 0.01v.

**Below are the simulation results and observations:**

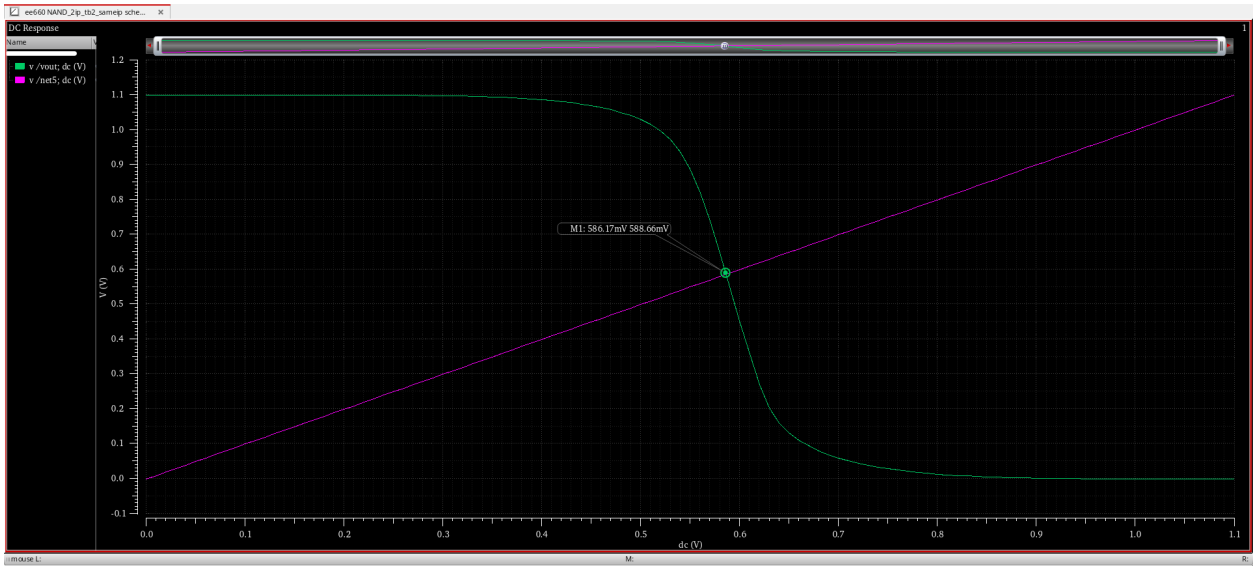



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as **586.17mV**

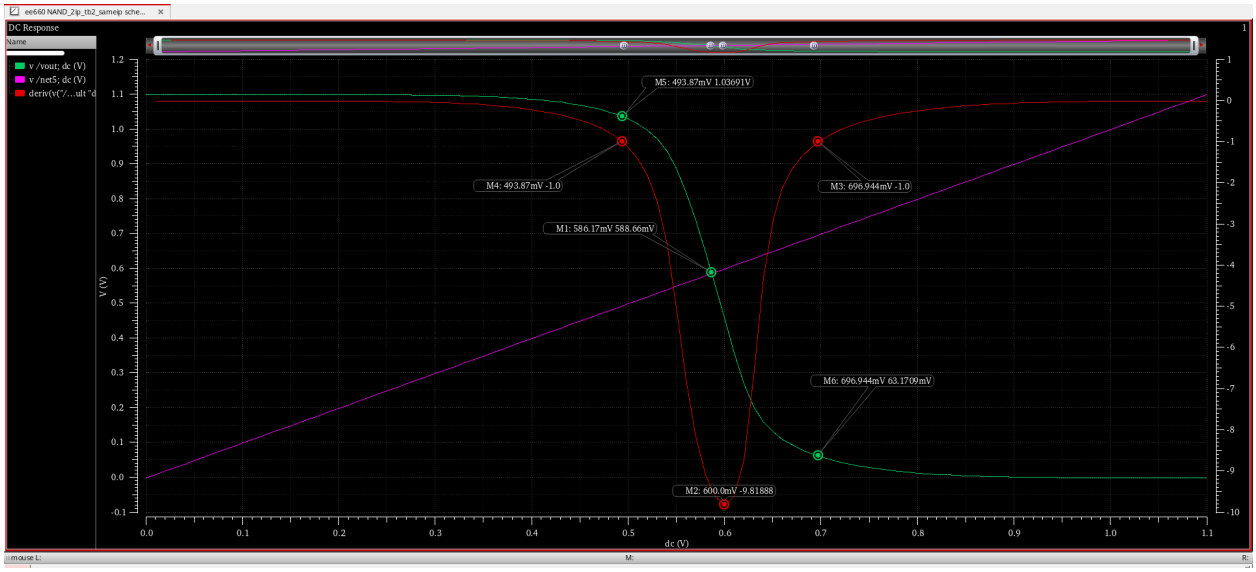



*Figure : Plot showing Voltage gain , VOH,VIH,VOL&VIL*

**From the Plot shown above :**

VIL=493.87mV , VOH=1.0369V

VIH= 696.944mV

VOL=63.17mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.339V

NML = VIL-VOL = 0.430V

**ii. a = 1, b = 0 → 1**

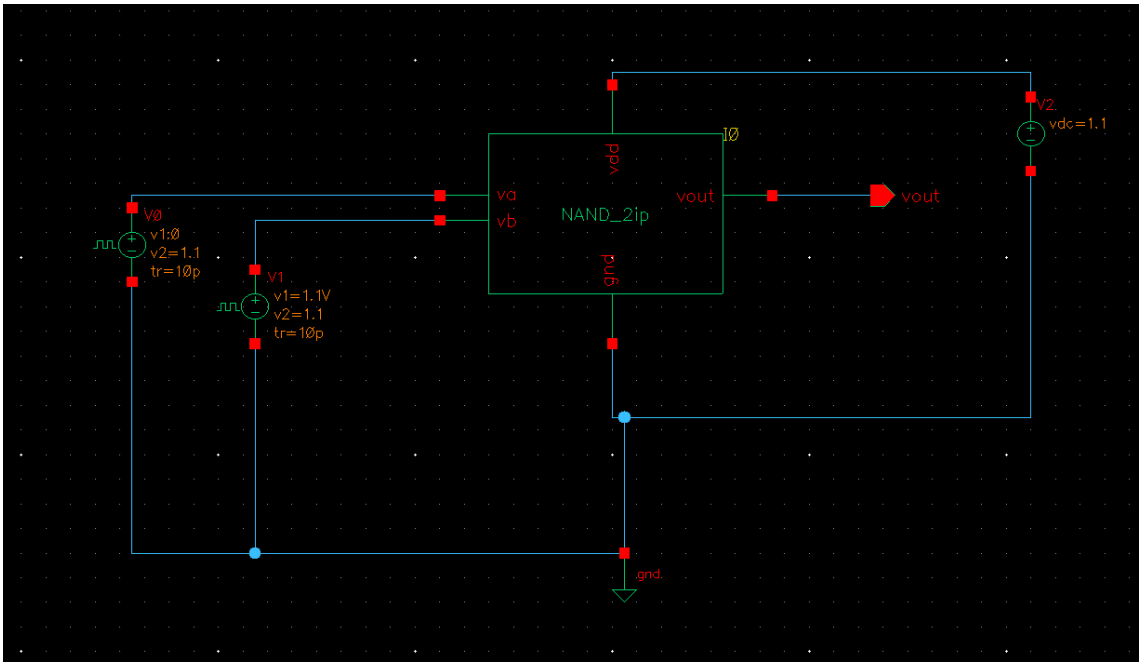



*Figure : Schematic of two input CMOS NAND gate used for DC analysis*

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with VDD =1.1v ,sweeped **Vb = 0 → 1** from 0 to 1.1v in steps of 0.01v when Va=1.1V.

Below are the simulation results and observations:

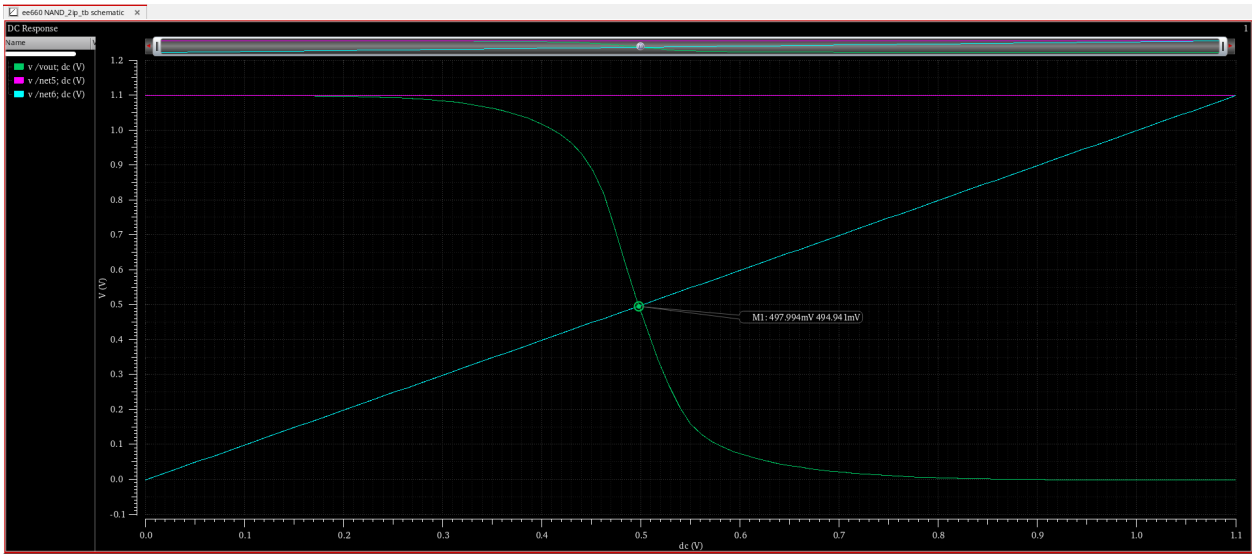



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as 497.994**mV**

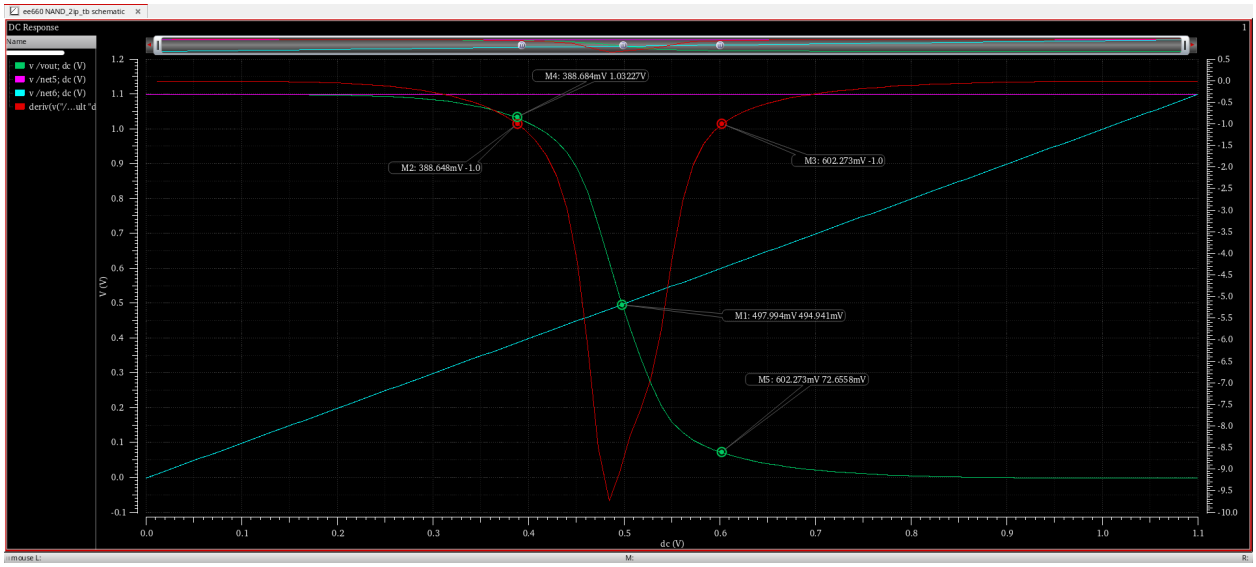



*Figure : Plot showing Voltage gain , VOH,VIL ,VIH&VOL*

**From the Plot shown above :**

*VIL=388.684mV , VOH=1.0322V*

VIH= 602.273mV

VOL=72.655mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.429V

NML = VIL-VOL = 0.316V

**(III) b = 1, a = 0 → 1**

Performed DC analysis for 2 input CMOS NAND gate schematic circuit with VDD =1.1v ,sweeped **Va = 0 → 1** from 0 to 1.1v in steps of 0.01v when **Vb=1.1V.**

Below are the simulation results and observations:

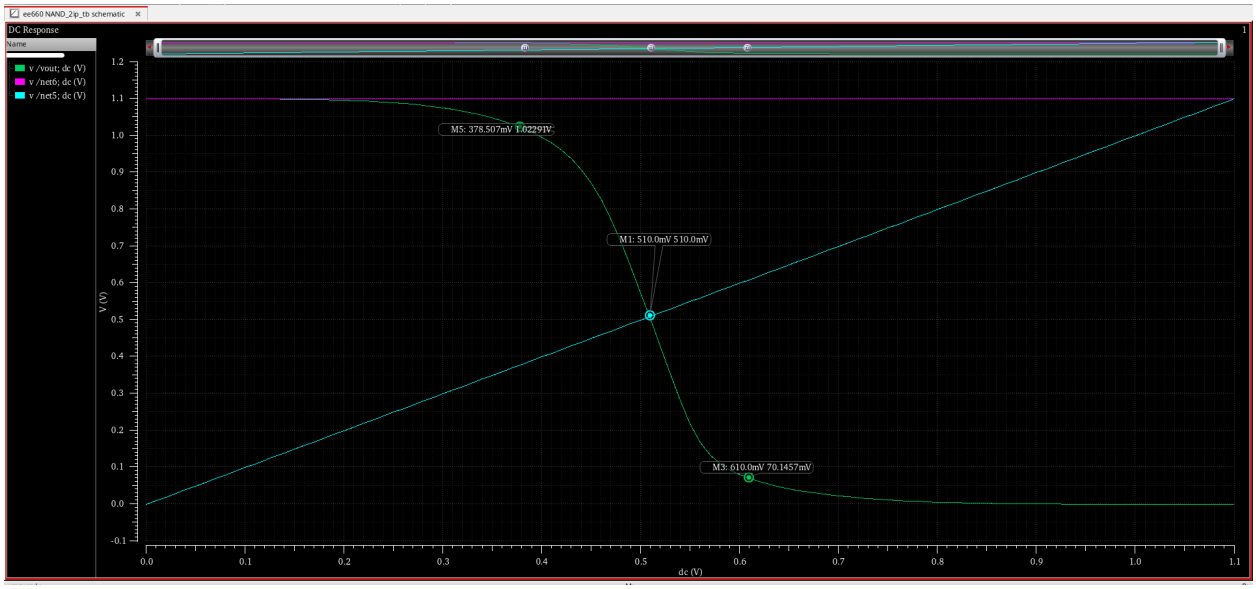



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as 510**mV**

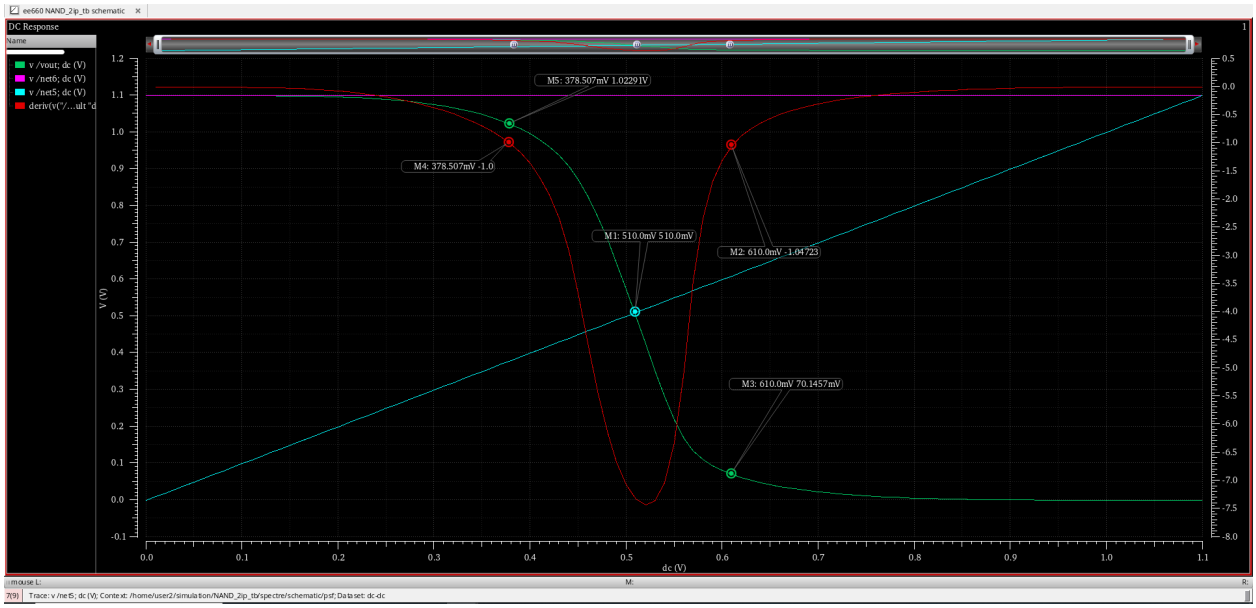



*Figure : Plot showing Voltage gain ,VOH,VIL, VIH&VOL*

**From the Plot shown above :**

**VIL=378.507mV , VOH=1.022V**

VIH= 610.0mV VOL=70.145mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.412V

NML = VIL-VOL = 0.308V

**2. Connect a 100 fF load to the NAND gate. Tabulate the propagation delays using schematic simulations for the following input patterns:**

**(a) a = b = 0 → 1**

**(b) a = 1, b = 0 → 1**

**(c) a = 0 → 1, b = 1**

**(d) a = b = 1 → 0**

**(e) a = 1, b = 1 → 0**

**(f) a = 1 → 0, b = 1**

*a) a = b = 0 → 1*

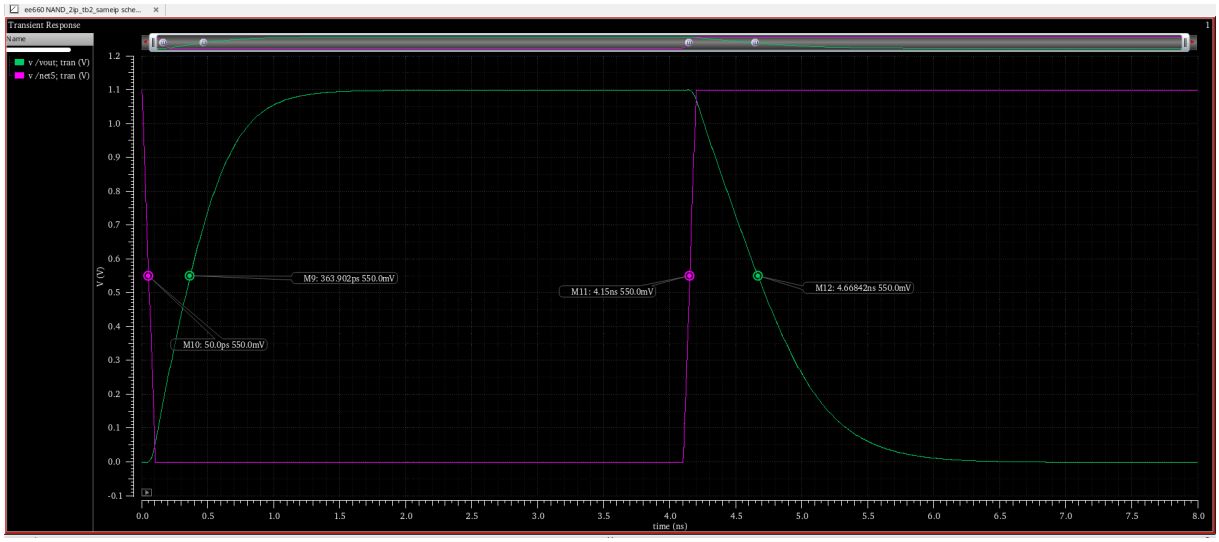



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is **316.16ps**

*b)* $a = 1, b = 0 \rightarrow 1$

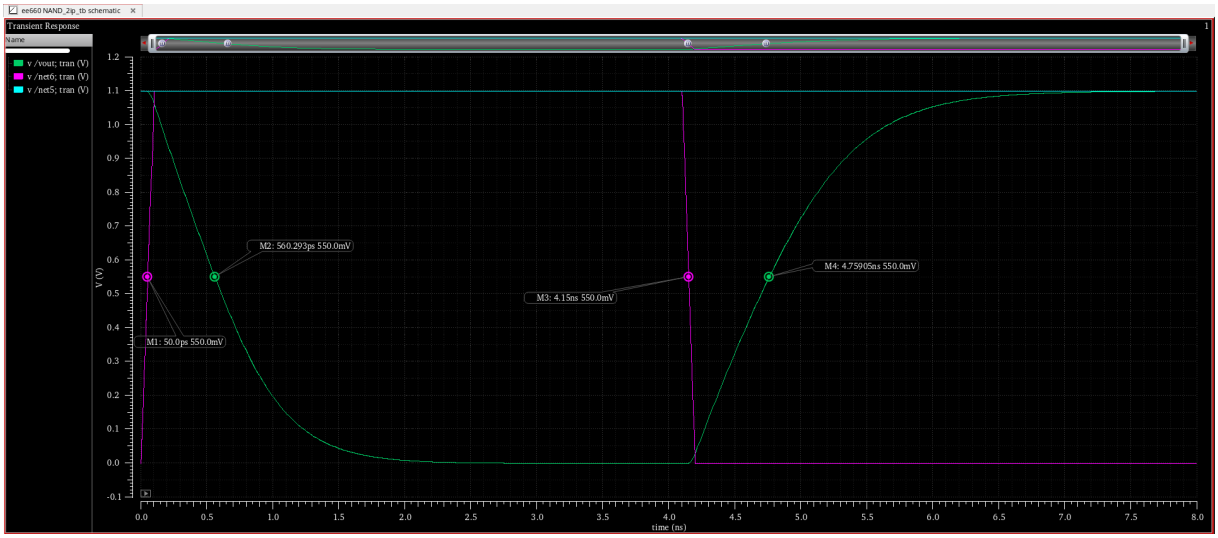



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 559.676p**s**

*c)b*= 1,*a*= 0 → 1

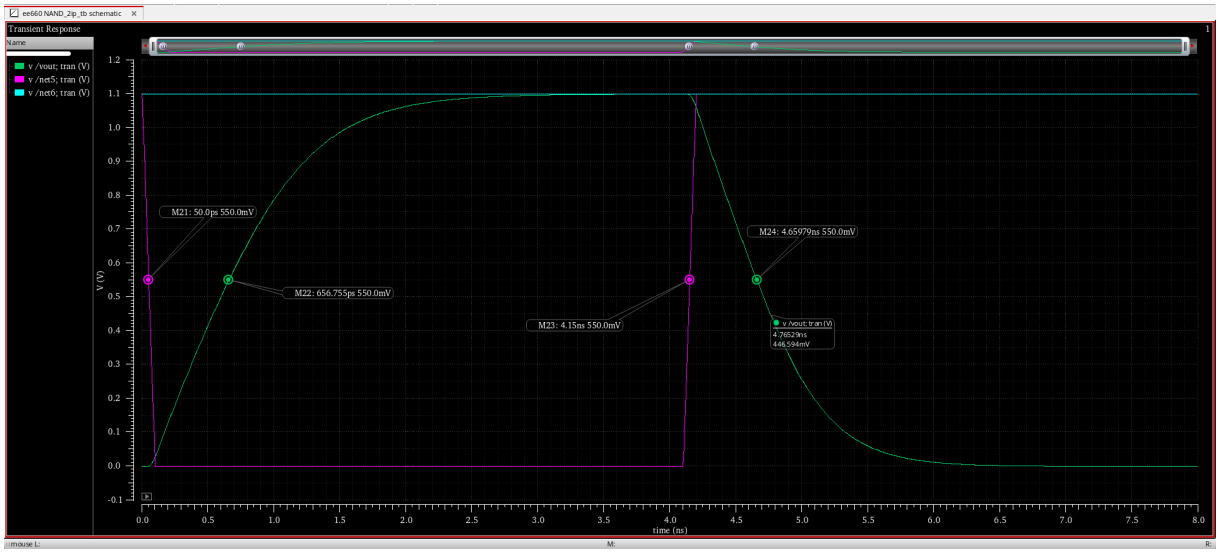



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 557.5p**s**

d)a = b = 1 → 0

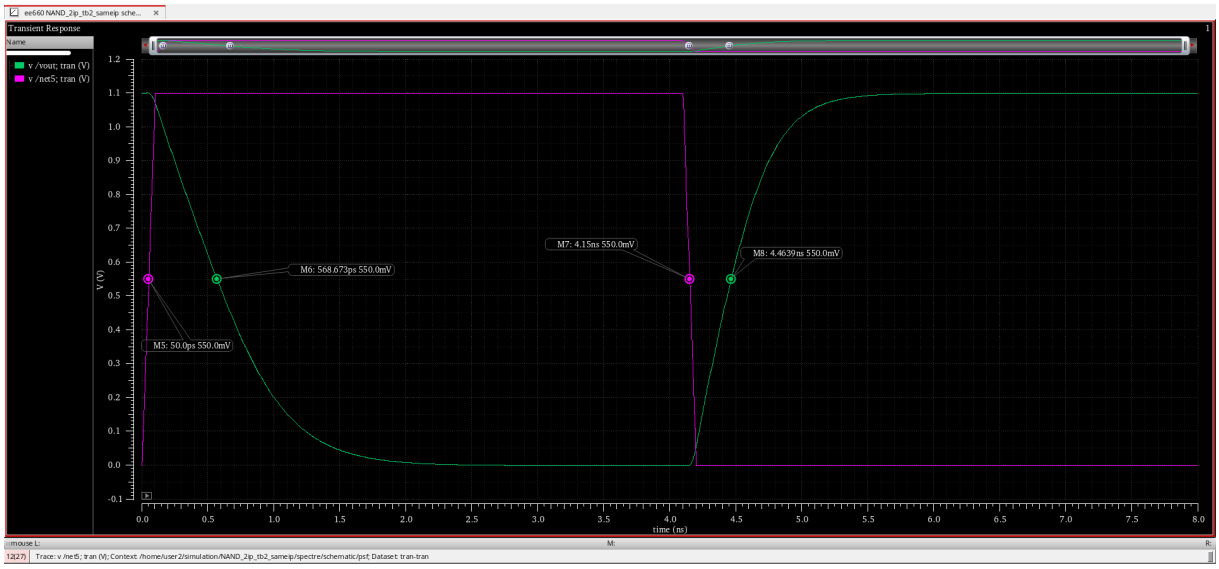



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 416.29p**s**

**e)a = 1, b = 1 → 0**

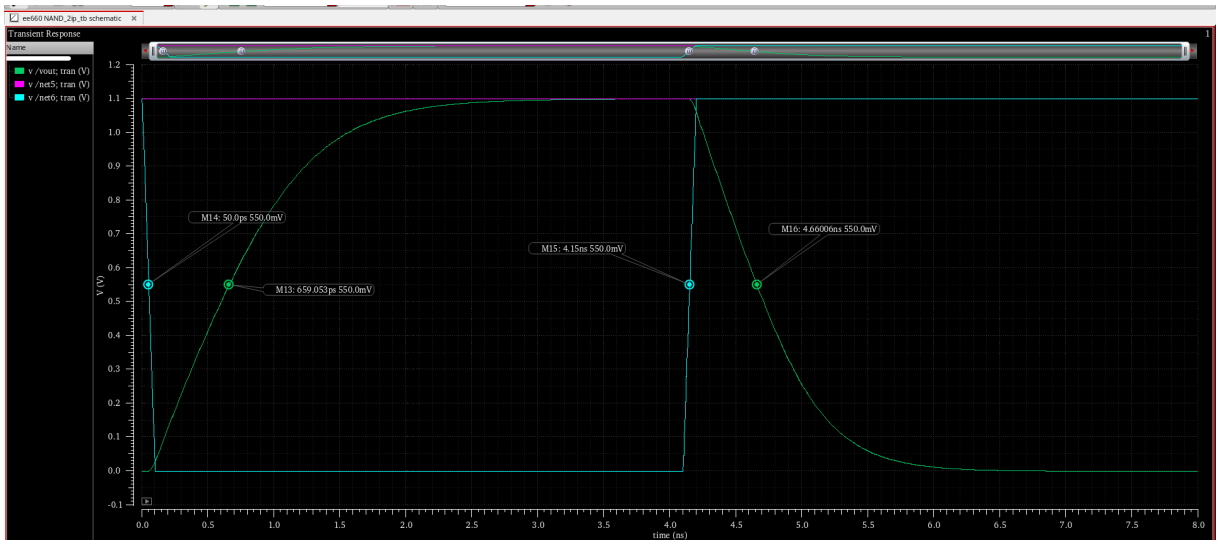



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 559.526 **ns**

**f)a = 1 → 0, b = 1,**

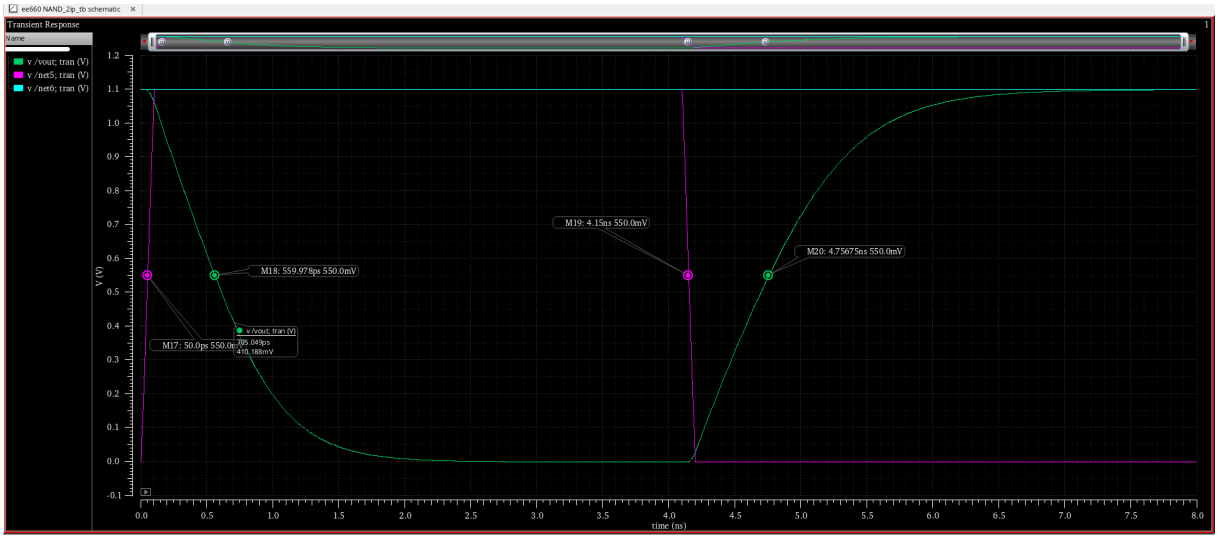



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is **558.364 ns**

**Tabular representation of delay dependence on input patterns:**

| Input Data Pattern | Delay(ps) |
|---|---|
| **a = b = 0 → 1** | 316.16 |
| **a = 1, b = 0 → 1** | 559.676 |
| **a = 0 → 1, b = 1** | 557.5 |
| **a = b = 1 → 0** | 416.29 |
| **a = 1, b = 1 → 0** | 559.526 |
| **a = 1 → 0, b = 1,** | 558.364 |

**3.Draw a layout for the NAND gate with minimum area possible. Repeat questions 1 and 2 using post layout simulations and compare the values withe the ones obtained through schematicsimulations.**

***i)***

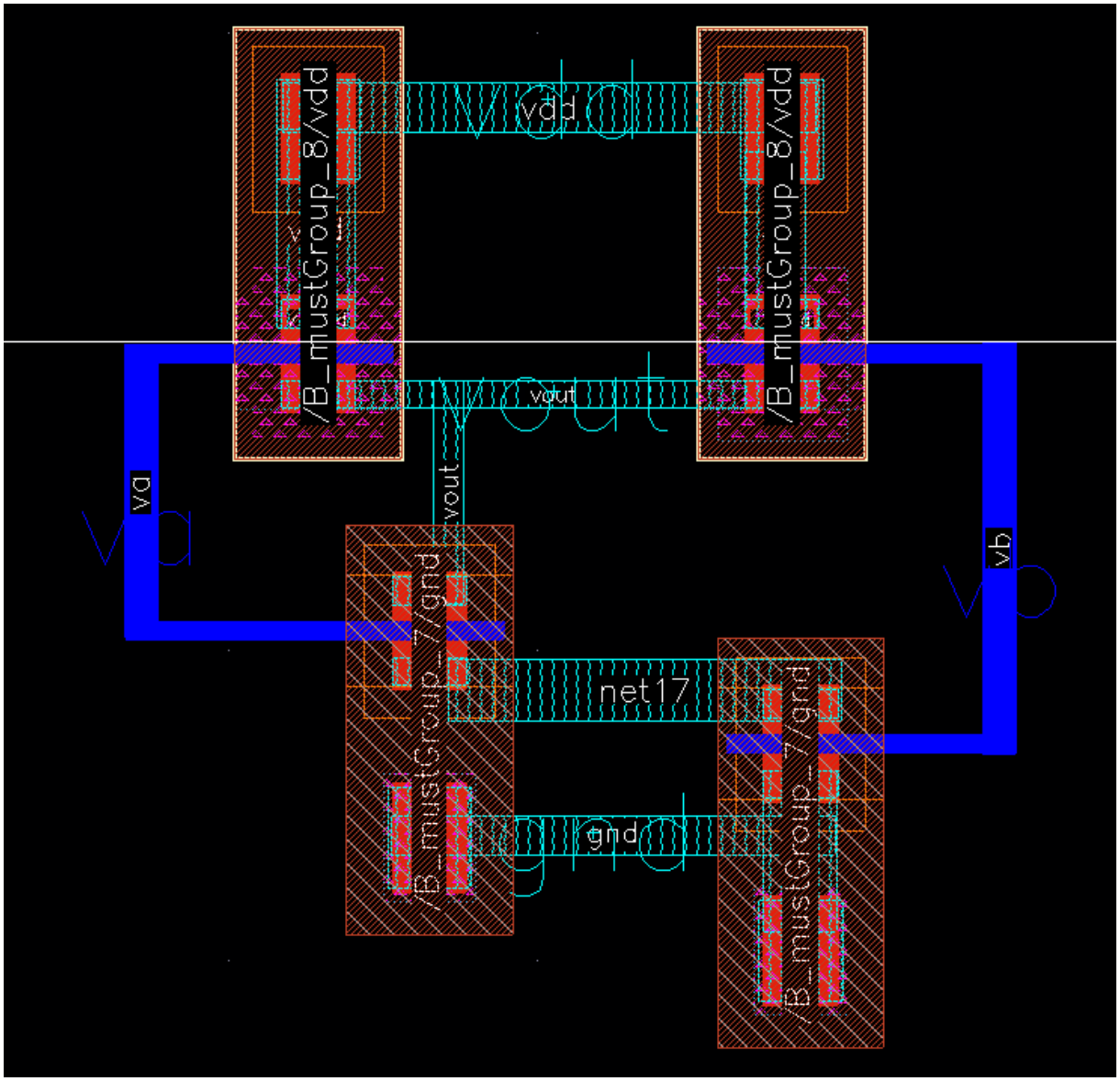
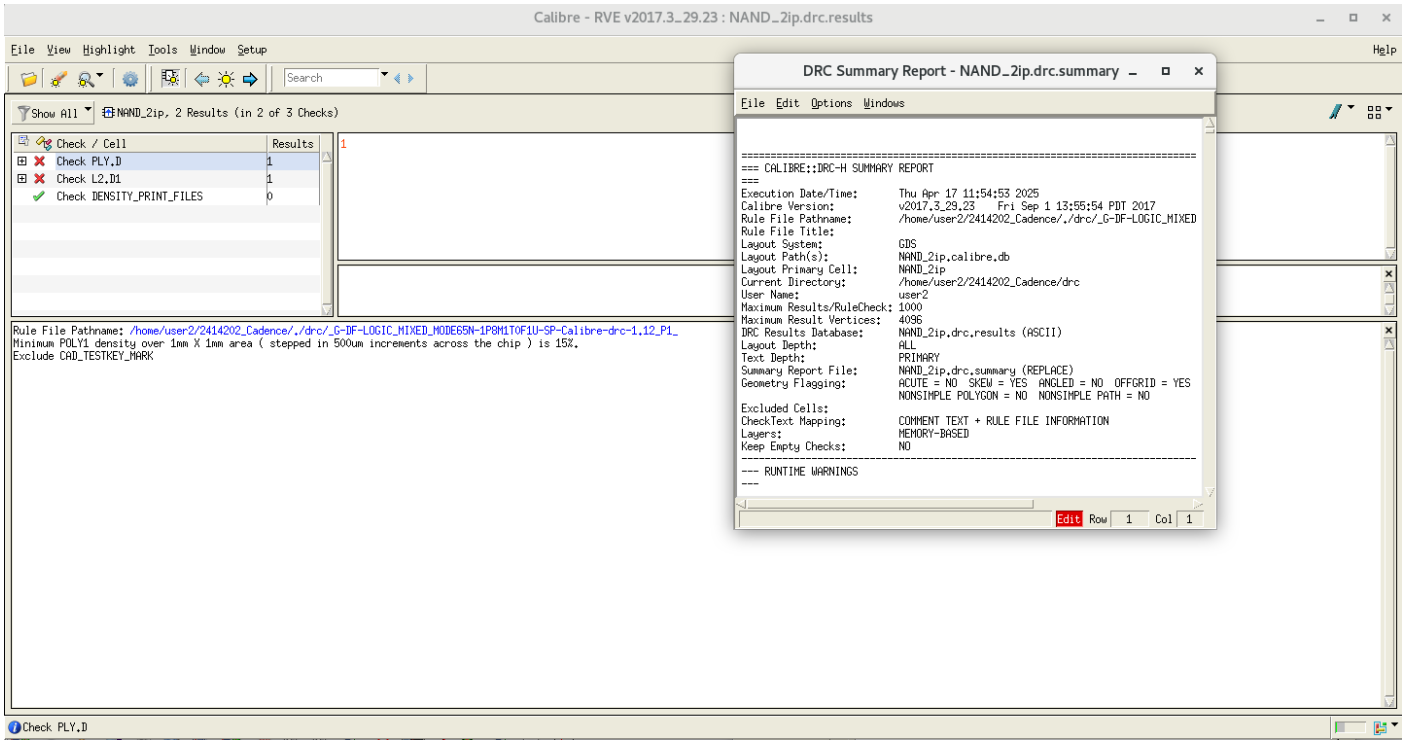
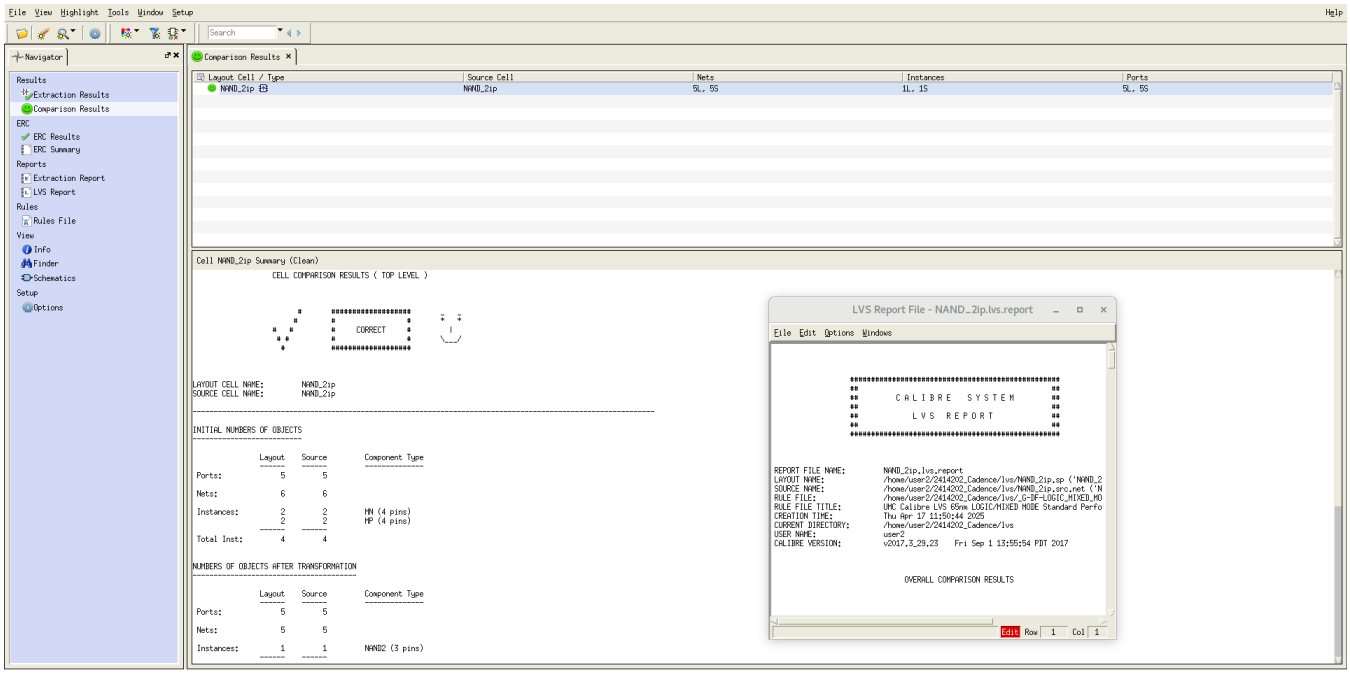



*Figure: Layout of 2 input CMOS NAND gate*

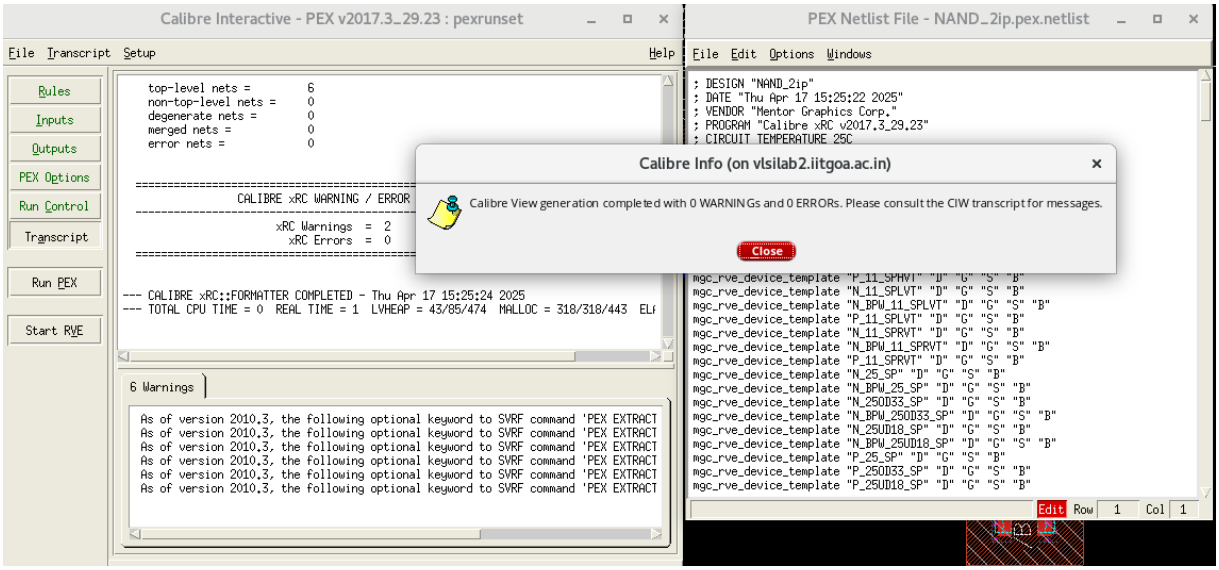
*Below is the DRC Simulation result screenshot:*




*Below is the LVS simulation result screenshot:*



Below is the PEX simulation result screenshot:




***i)a = b = 0 → 1***

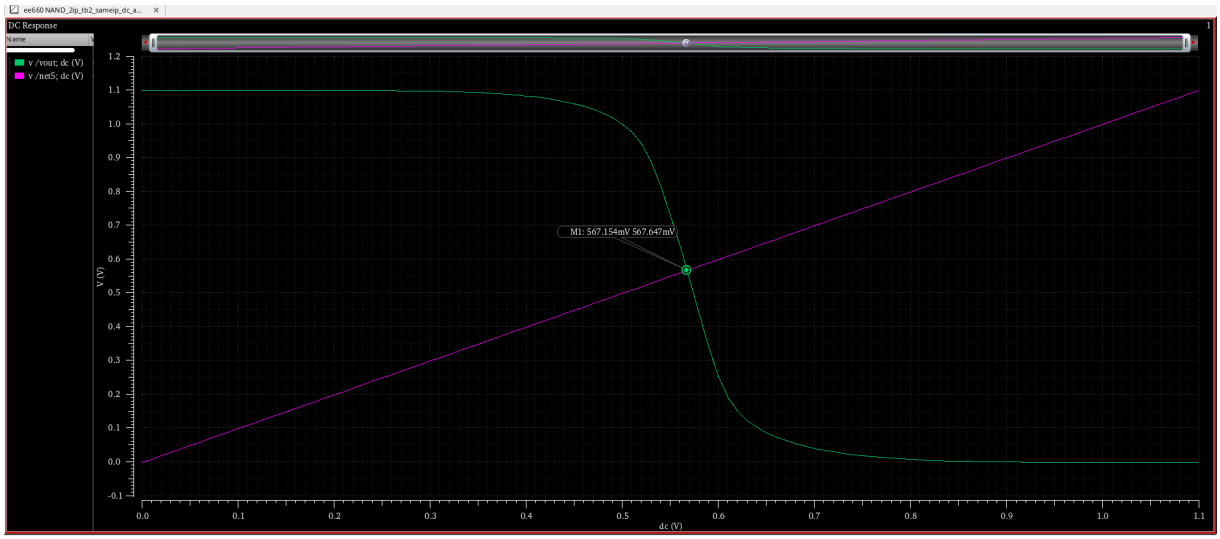



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as 567**.154mV**

***ii) a* = 1,*b* = 0 → 1**

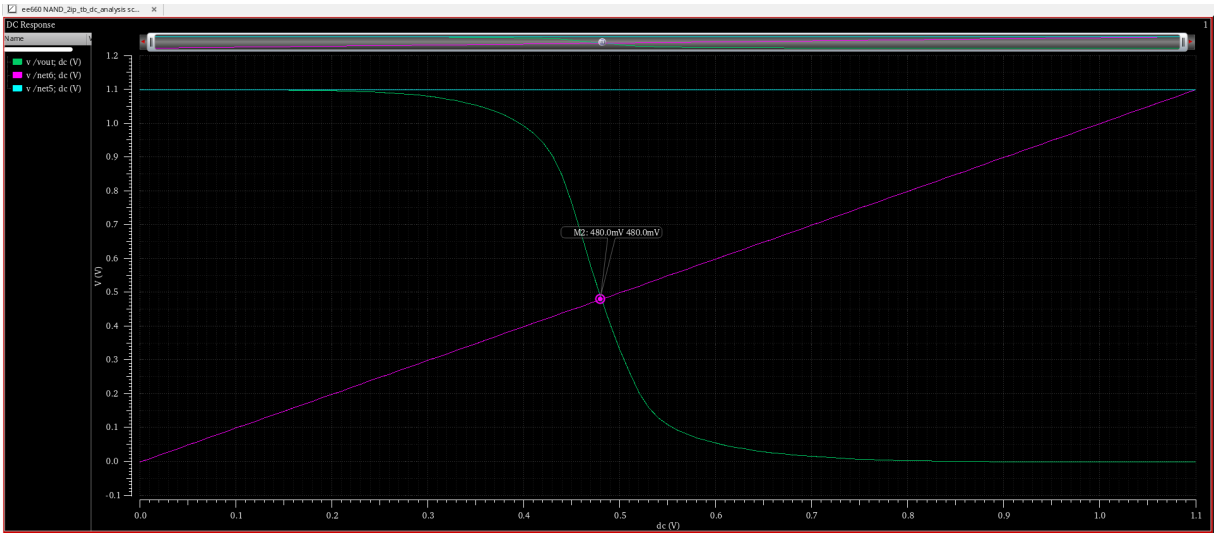



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as 480**mV**

***iii)b* = 1,*a* = 0 → 1**

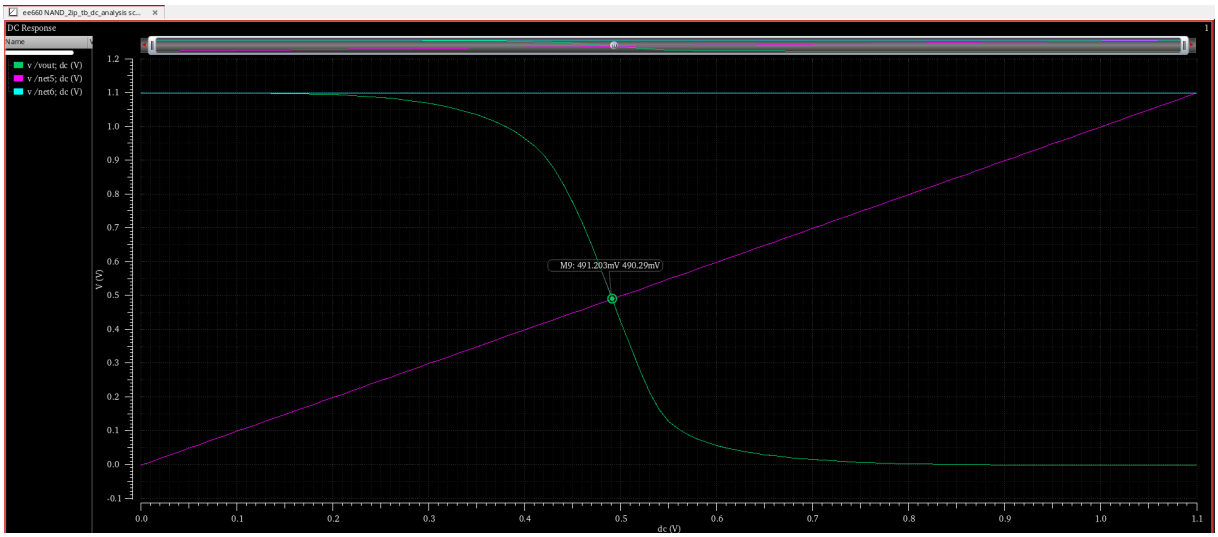



*Figure :Plot showing Simulated voltage transfer characteristics of 2 input CMOS NAND gate*

**Observation:** From the Simulated Voltage transfer characteristics, Switching threshold is identified as 491.203**mV**

**b)Using the VTC calculate the values of the switching threshold and noise margins for the different input patterns listed above.**

***i)*** ***a*** **=** ***b*** **= 0 → 1**

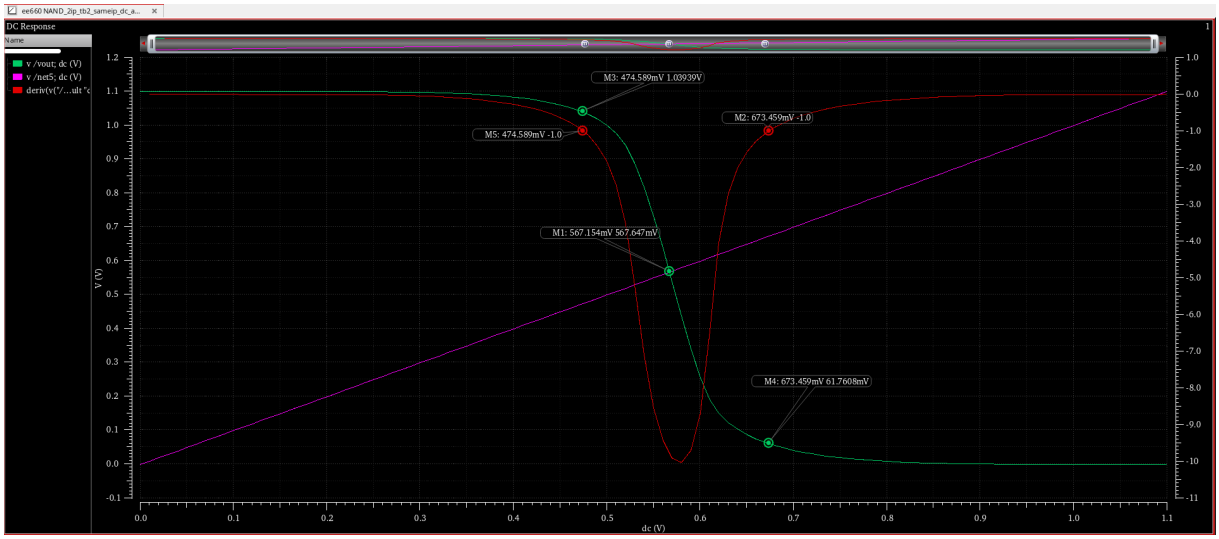



*Figure : Plot showing Voltage gain , VOH,VIL ,VIH&VOL*

**From the Plot shown above :**

VIL=474.589mV , VOH=1.039V

VIH= 673.459mV

VOL=61.7609mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.365V

NML = VIL-VOL = 0.412V

***ii) a* = 1,*b* = 0 → 1**

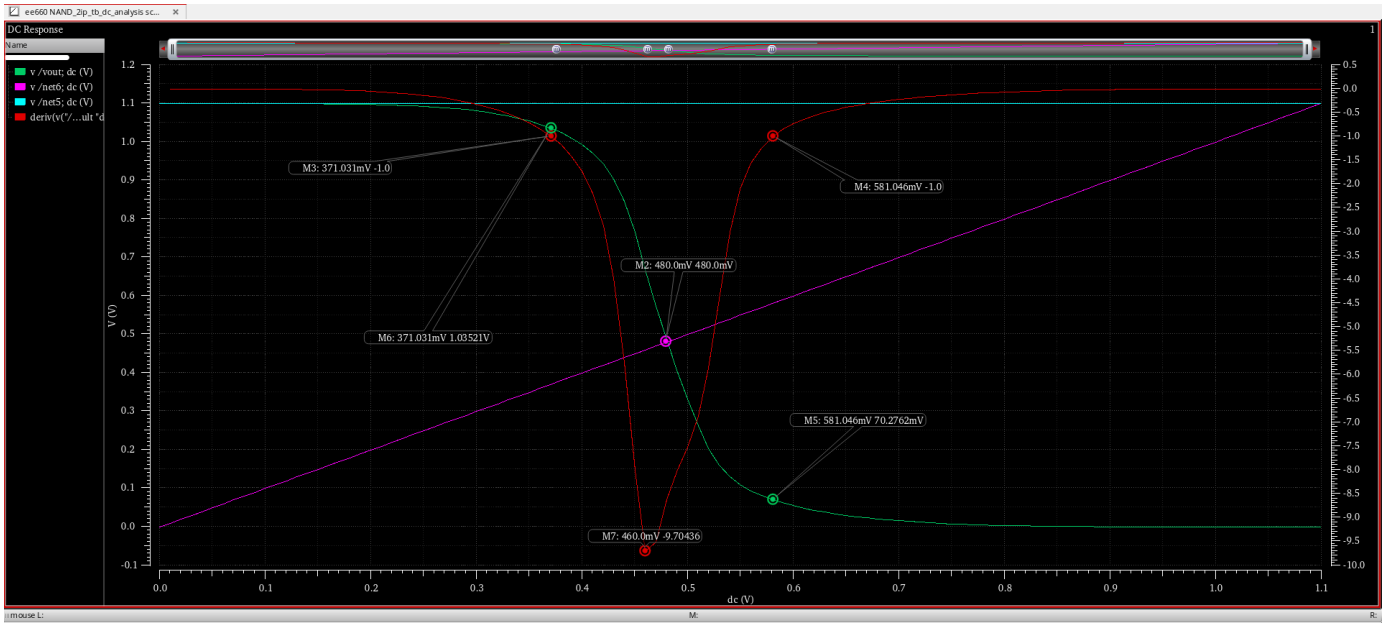



*Figure : Plot showing Voltage gain , VOH,VIL,VIH&VOL*

**From the Plot shown above :**

VIL=371.031mV , VOH=1.0352V

VIH= 581.064mV

VOL=70.2762mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.453V

NML = VIL-VOL = 0.300V

***iii)b* = 1,*a* = 0 → 1**

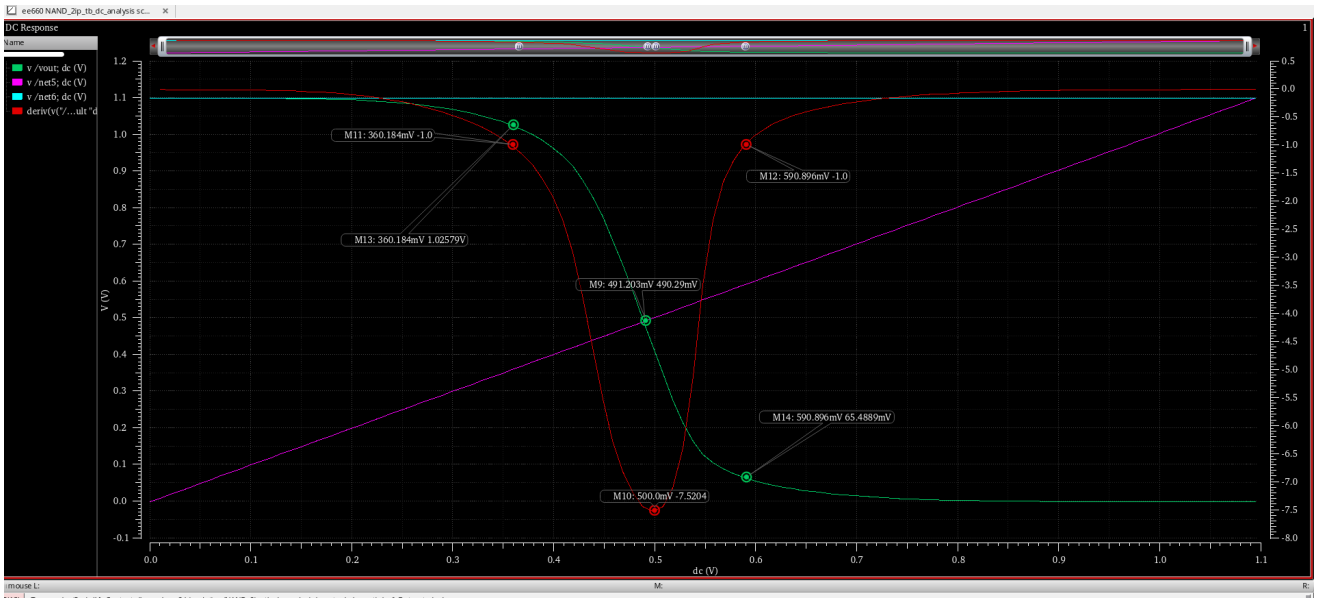



*Figure : Plot showing Voltage gain , VOH,VIL ,VIH&VOL*

**From the Plot shown above :**

VIL=360.184mV ,

VOH=1.025V

VIH= 590.896mV

VOL=65.488mV

**NOISE MARGINS:**

NMH =VOH-VIH = 0.434V

NML = VIL-VOL = 0.294V

**2. Connect a 100 fF load to the NAND gate. Tabulate the propagation delays using schematic simulations for the following input patterns:**

**a) a = b = 0 → 1**

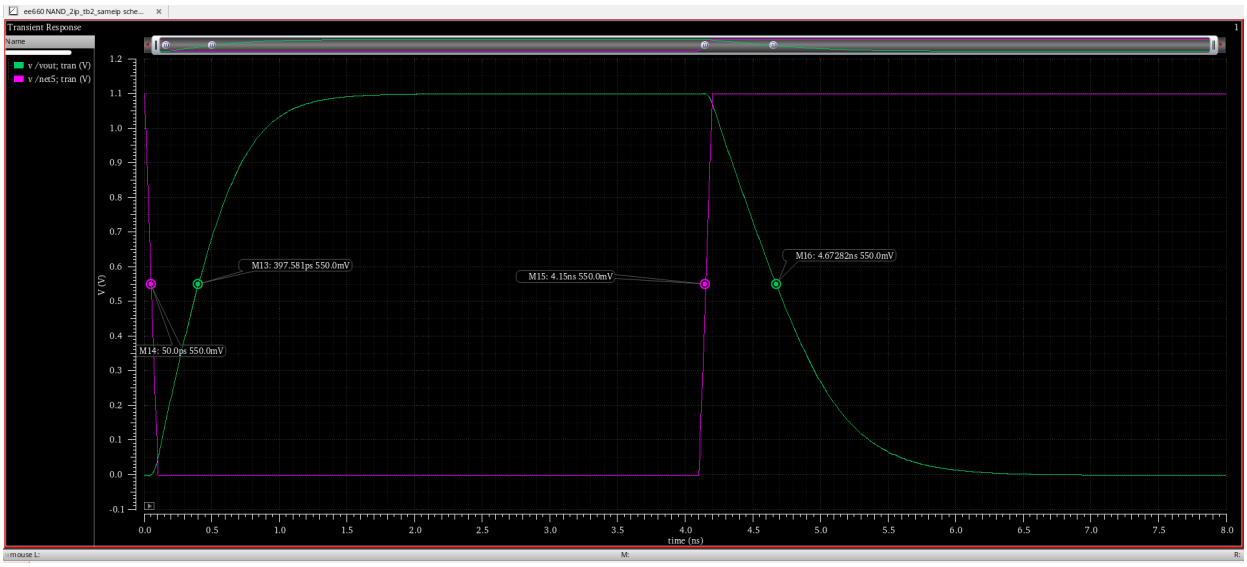



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 432.705 **ps**

**b) a = 1, b = 0 → 1**

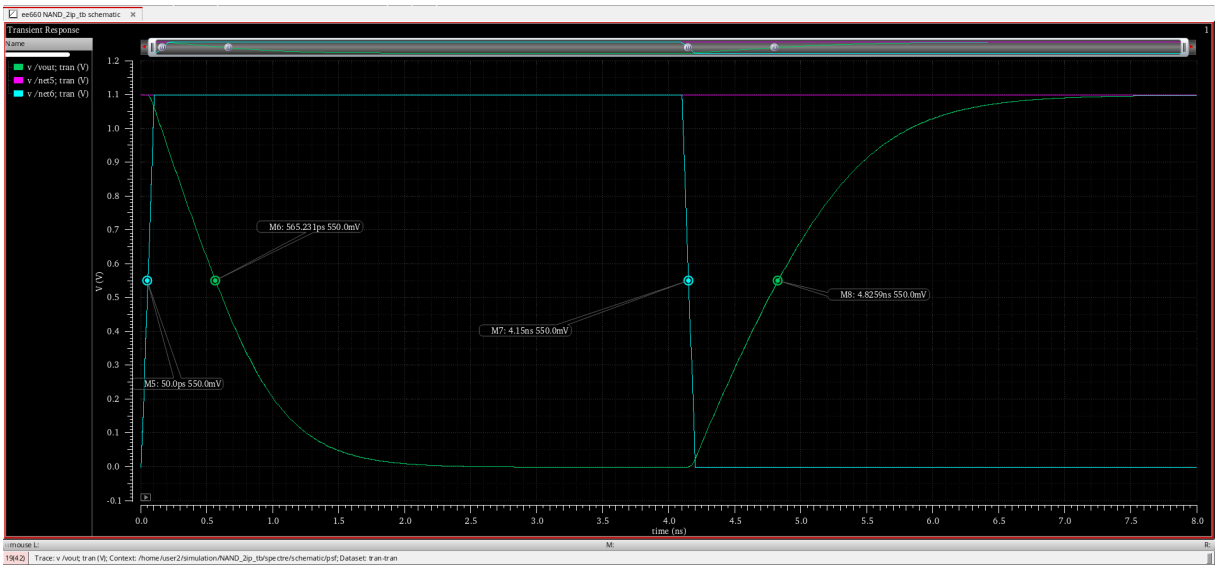



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 595.59 **ns**

**c) a = 0 → 1, b = 1**

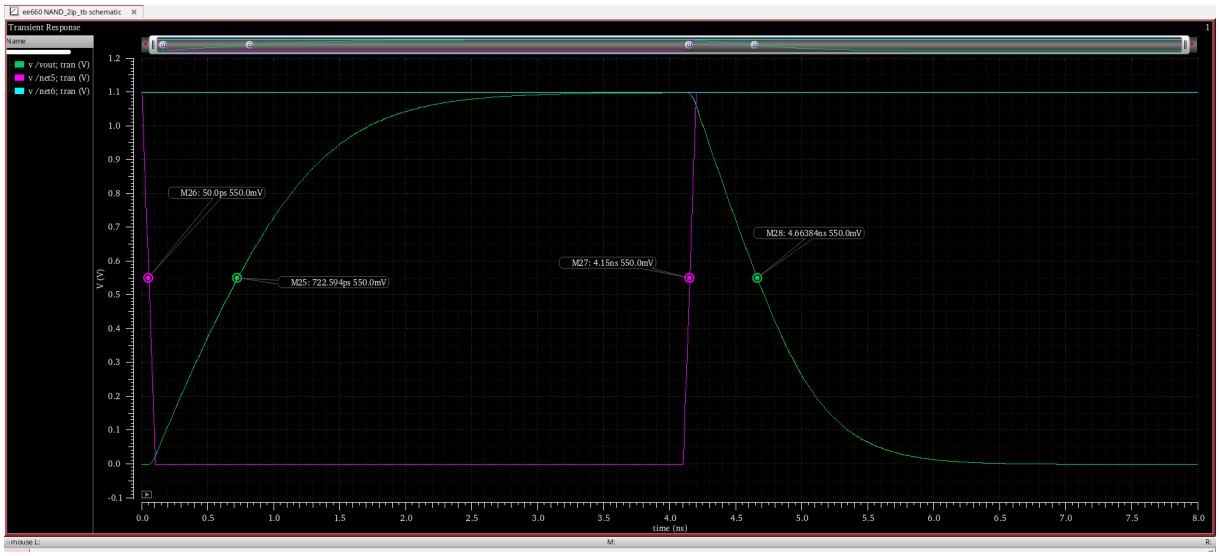



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 592.5p**s**

**d) a = b = 1 → 0**

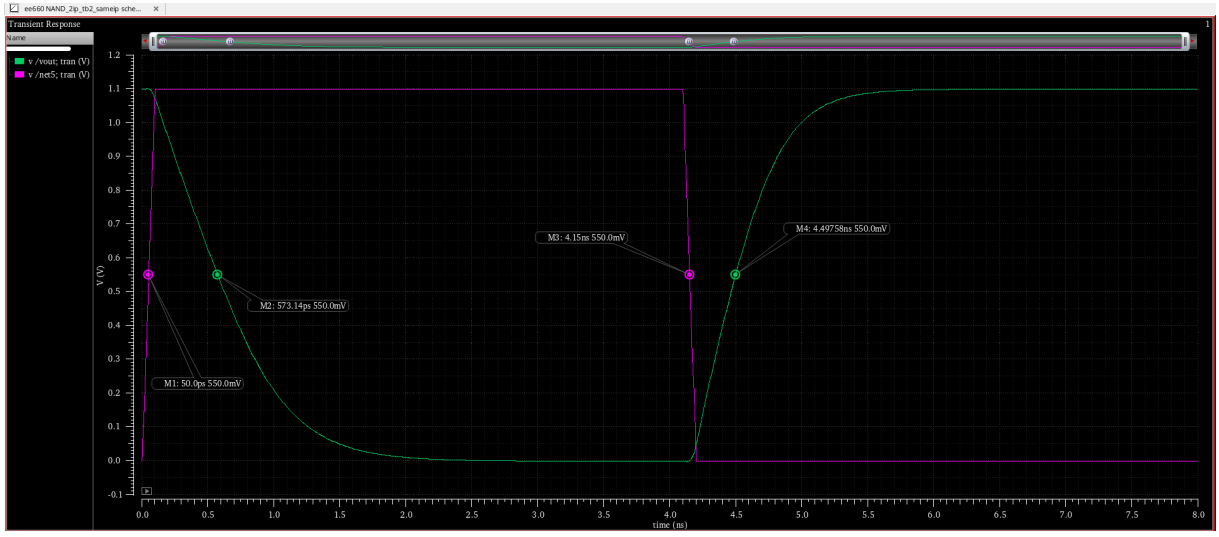



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 435.07 **ps**

**e)a = 1, b = 1 → 0**

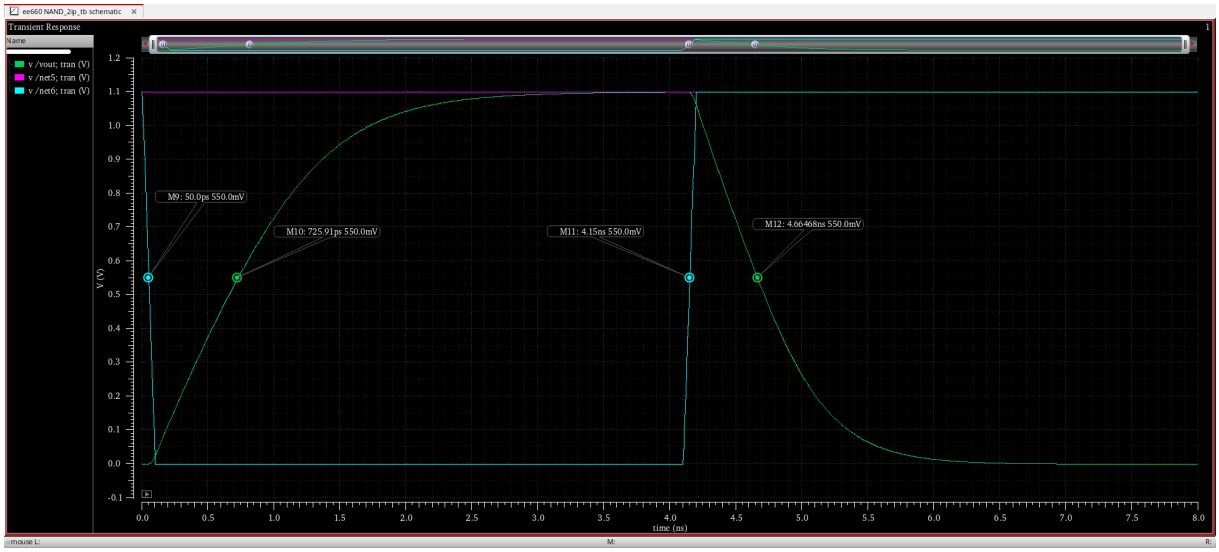



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 595.295 **ns**

**f) a = 1 → 0, b = 1,**

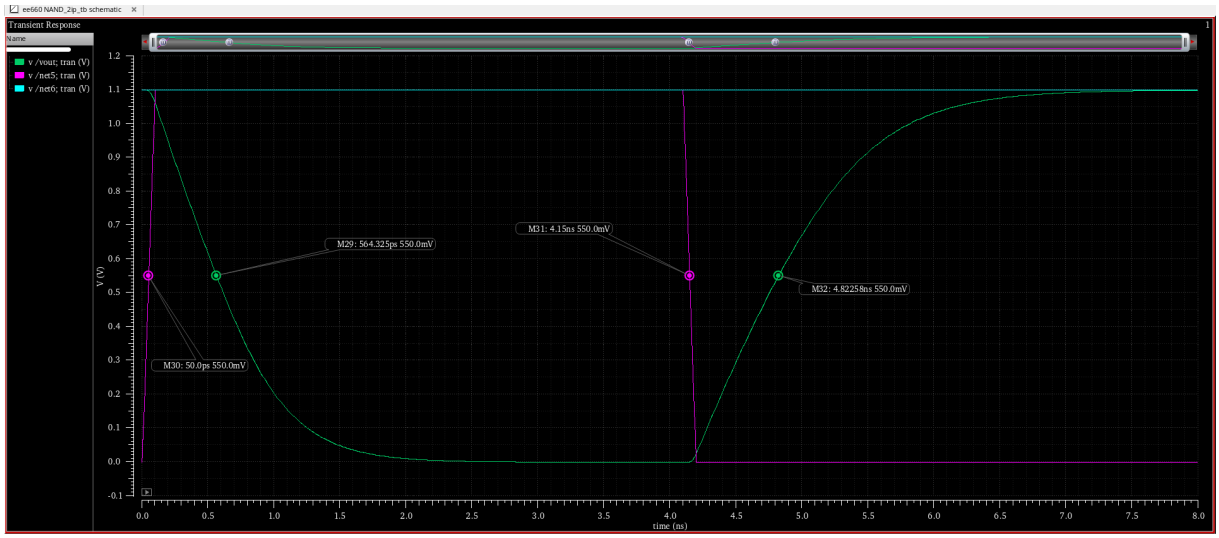



*Figure : Simulated transient response of the 2 input CMOS NAND gate*

**Observation:** From the above plot it is observed that the Propagation delay is 593**s**

**Tabular representation of delay dependence on input patterns:**

| **Input Data Pattern** | **Delay(ps)** |
|---|---|
| **a = b = 0 → 1** | 432.705 |
| **a = 1, b = 0 → 1** | 595.59 |
| **a = 0 → 1, b = 1** | 592.5 |
| **a = b = 1 → 0** | 435.07 |
| **a = 1, b = 1 → 0** | 595.295 |
| **a = 1 → 0, b = 1,** | 593 |

## Comparison between schematic and post layout simulations:

| Input Pattern | VM(V)(Schematic Simulation) | VM(V)(Post Layout Simulation) |
|---|---|---|
| ***a = b =0→1*** | 0.586 | 0.567 |
| ***a = 1,b = 0 → 1*** | 0.497 | 0.48 |
| ***b = 1,a = 0 → 1*** | 0.51 | 0.491 |

*Table showing VM w.r.to input pattern for schematic and post layout simulations*

**Observations:**

***1)*** *When both Va and Vb are simultaneously transitioning from low to high ,both transistors in the pull up network are ON simultaneously for va=vb=0 , representing strong pull up. Also ,****due to balanced drive strengths and transistor sizing*** *it is observed that switching threshold is symmetrically close to VDD/2 (i.e 0.55) for both schematic and post layout simulation.*

***2)****In 2nd and 3rd input patterns only one of pull up devices is on.Hence,the* ***VTC is shifted to the left as a result of the weaker PUN****. But there's a slight difference between the shift that's happening which is mainly due to the state of internal node between series NMOS devices.*

***Both schematic and Post -layout exhibiting the same behaviour for all the 3 input patterns but there's a very slight decrement in VM value for post layout simulation mainly due to the fact that nmos transitors are stacked which would reduce capacitance at the interconnect because of overlapping of source of N1 and Drain of N2.***

| Input Pattern | NML**(V)( (Schematic Simulation)** | NMH**(V)( (Schematic Simulation)** | NML**(V)( (Post Layout Simulation)** | NMH**(V)( (Post Layout Simulation)** |
|---|---|---|---|---|
| ***a = b =0→1*** | 0.430 | 0.339 | 0.412 | 0.365 |
| ***a = 1,b = 0 → 1*** | 0.316 | 0.429 | 0.3 | 0.453 |
| ***b = 1,a = 0 → 1*** | 0.308 | 0.412 | 0.294 | 0.434 |

*Table showing Noise margins for schematic and post layout simulations*

**Observations**:

*1.It is observed that noise margins in both schematic and post layout simulations are* ***input/pattern dependant****.*

*2. In post-layout simulation, extra factors like wiring resistance and capacitance are considered. These make small changes, like slightly improving* ***NMH*** *due to better handling of high voltages, and slightly lowering* ***NML*** *because of increased voltage drops at low levels.*

| **Input Data Pattern** | **Delay(ps)** (Schematic Simulation) | **Delay(ps)** (Post Layout Simulation) |
|---|---|---|
| **a = b = 0 → 1** | 316.16 | 432.705 |
| **a = 1, b = 0 → 1** | 559.676 | 595.59 |
| **a = 0 → 1, b = 1** | 557.5 | 592.5 |
| **a = b = 1 → 0** | 416.29 | 435.07 |
| **a = 1, b = 1 → 0** | 559.526 | 595.295 |
| **a = 1 → 0, b = 1,** | 558.364 | 593 |

*Table showing delay dependence on input patterns for schematic and post layout simulations*

**Observations**:

*1.In both the post layout and schematic simulations input transition* ***(a = b = 1 → 0)*** *results in a smaller delay , compared with case in which only one input is driven low.*

*2. In Post Layout Simulations, Delay Increment has been observed for all the input patterns. This is mainly due to fact that the parasitic resistance and capacitance from the interconnects, which can* ***slow down*** *certain transitions and* ***increase delay*** *.*