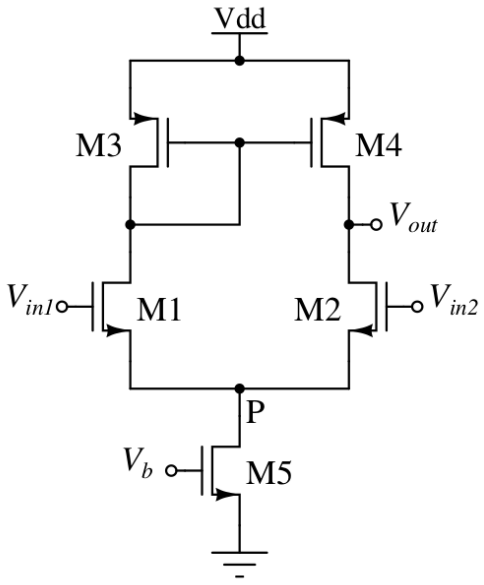
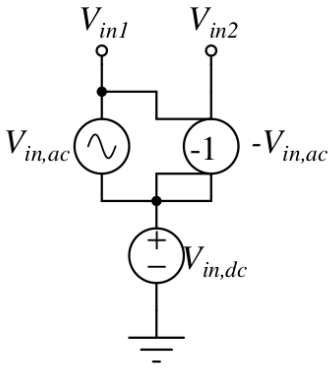
EE 660 VLSI Design Laboratory
Assignment VI
Submitted by: L Sri Sai Swathi (2414202)

1. Design an NMOS common-source differential amplifier with active load as shown in Fig. 1a using UMC65 technology. Given (W/L) 1,2,5 = 6µ/0.06µ, (W/L) 3,4 = 3µ/0.06µ, V b = 0.55 V, and V in,dc =0.7 V.



(a) Differential amplifier.



(b) Input source.

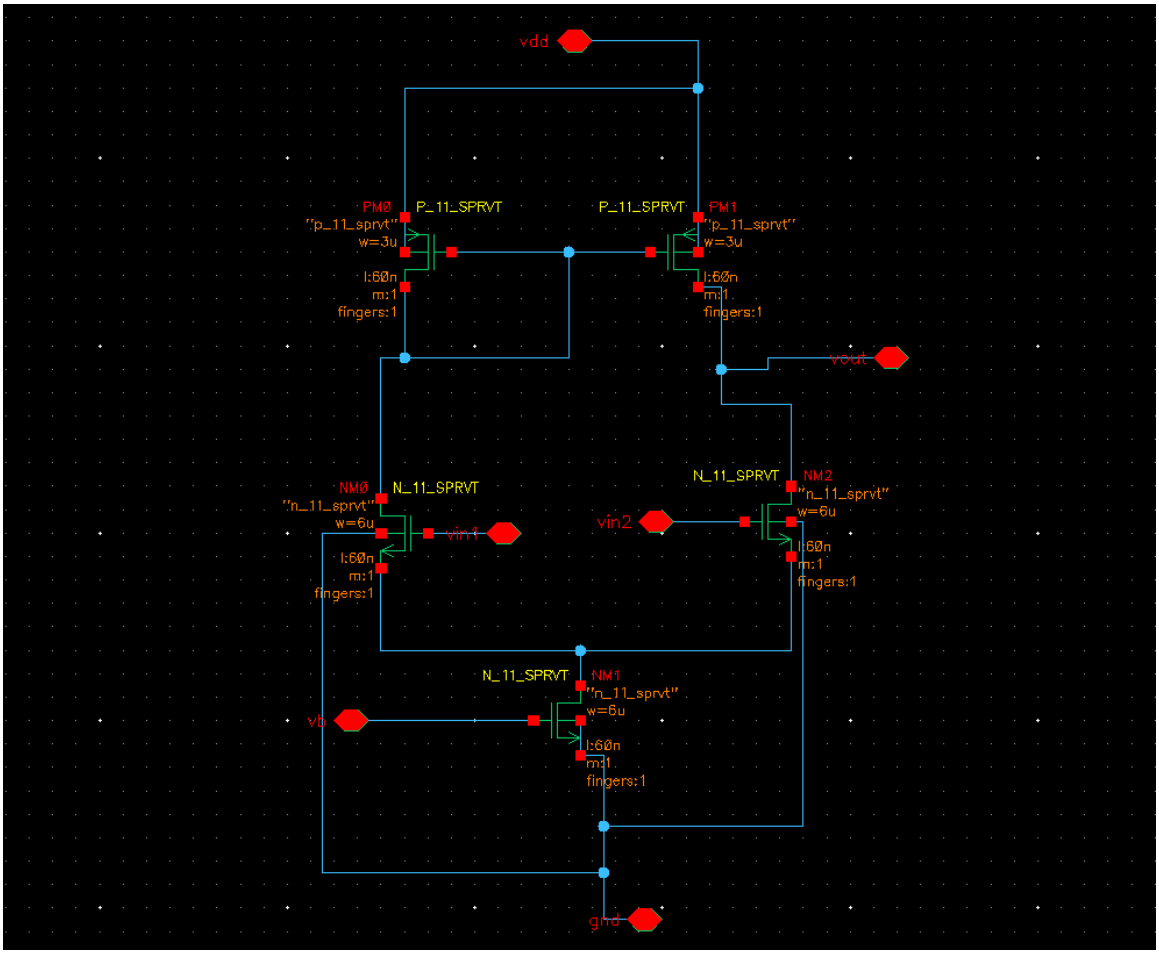


Figure : Schematic of NMOS common-source differential amplifier with active load using 65 nm technology (
W/L) 1,2,5 = 6µ/0.06µ, (W/L) 3,4 = 3µ/0.06µ, V b = 0.55 V, and V in,dc =0.7 V.

(a) The configuration shown in Fig. 1b is used to generate the input for the amplifier. You can use the small signal amplitude of V in,ac to be 10 mV, and frequency to be 1 kHz. Perform the operating point analysis and check if all the transistors are in saturation region of operation.

Below are the simulation results of DC operating point analysis:

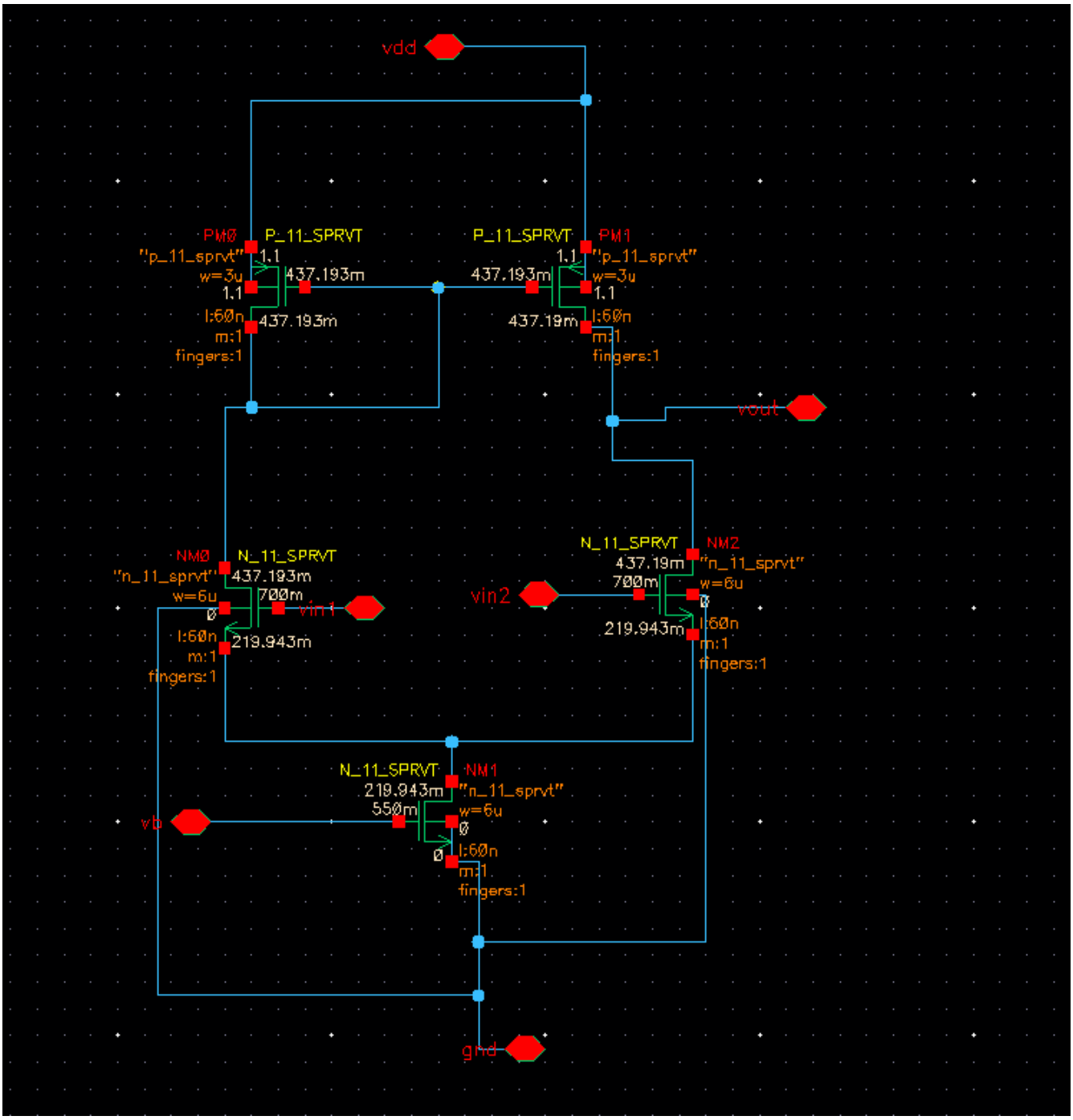


Figure: Schematic with operating point values

Simulation result of first mosfet M1 :

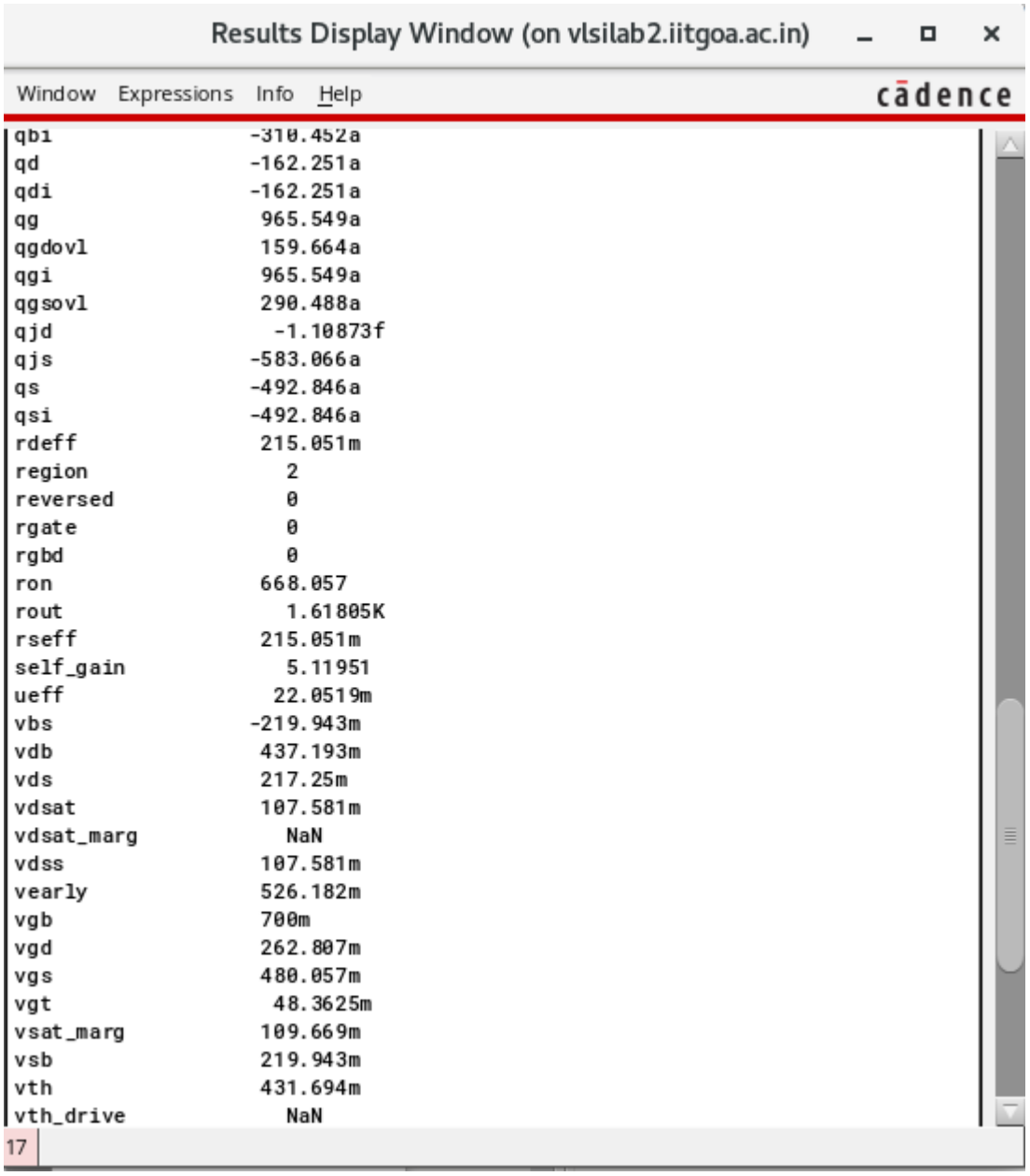


Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 (Saturation region of operation)

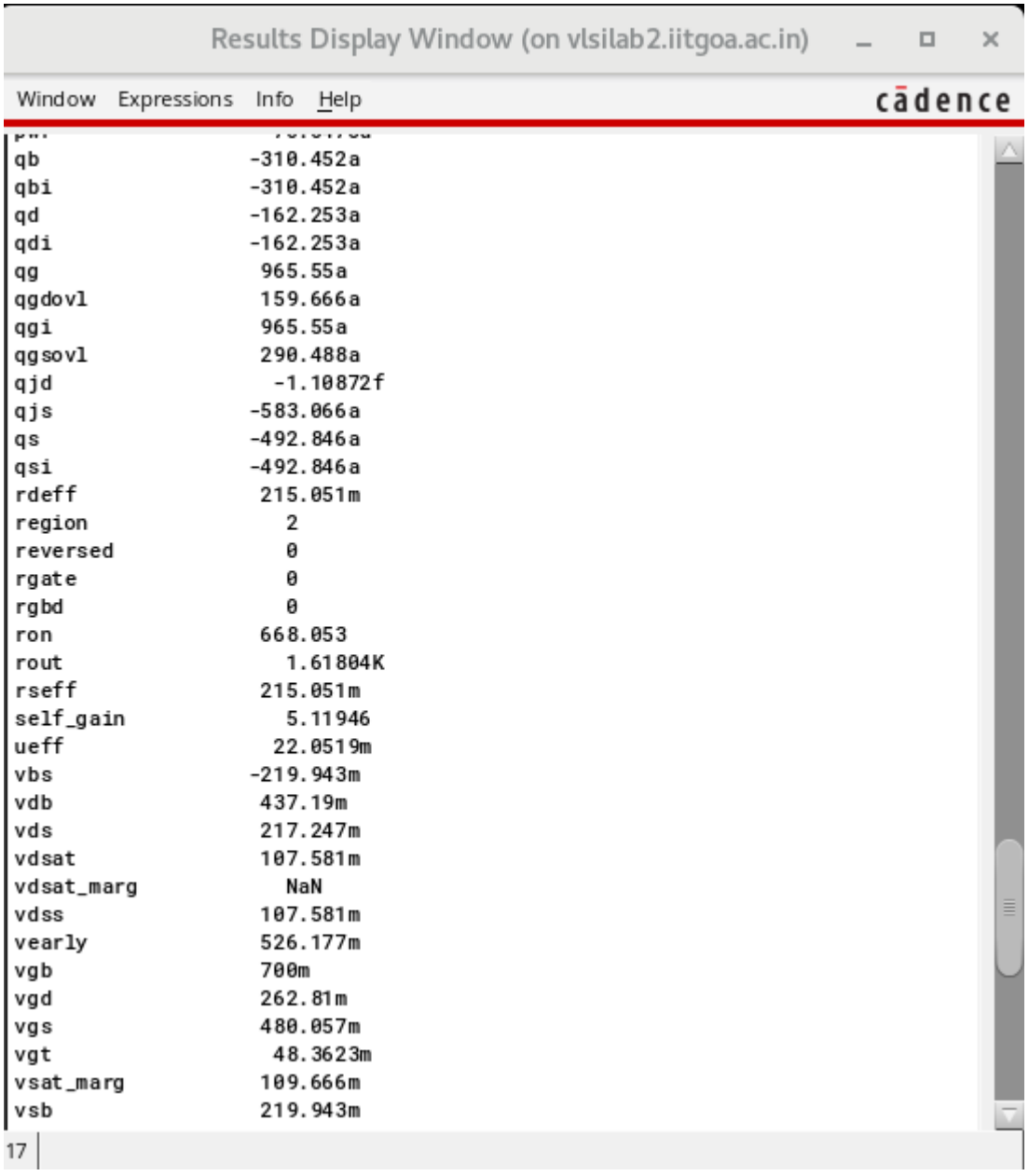


Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 (Saturation region of operation)

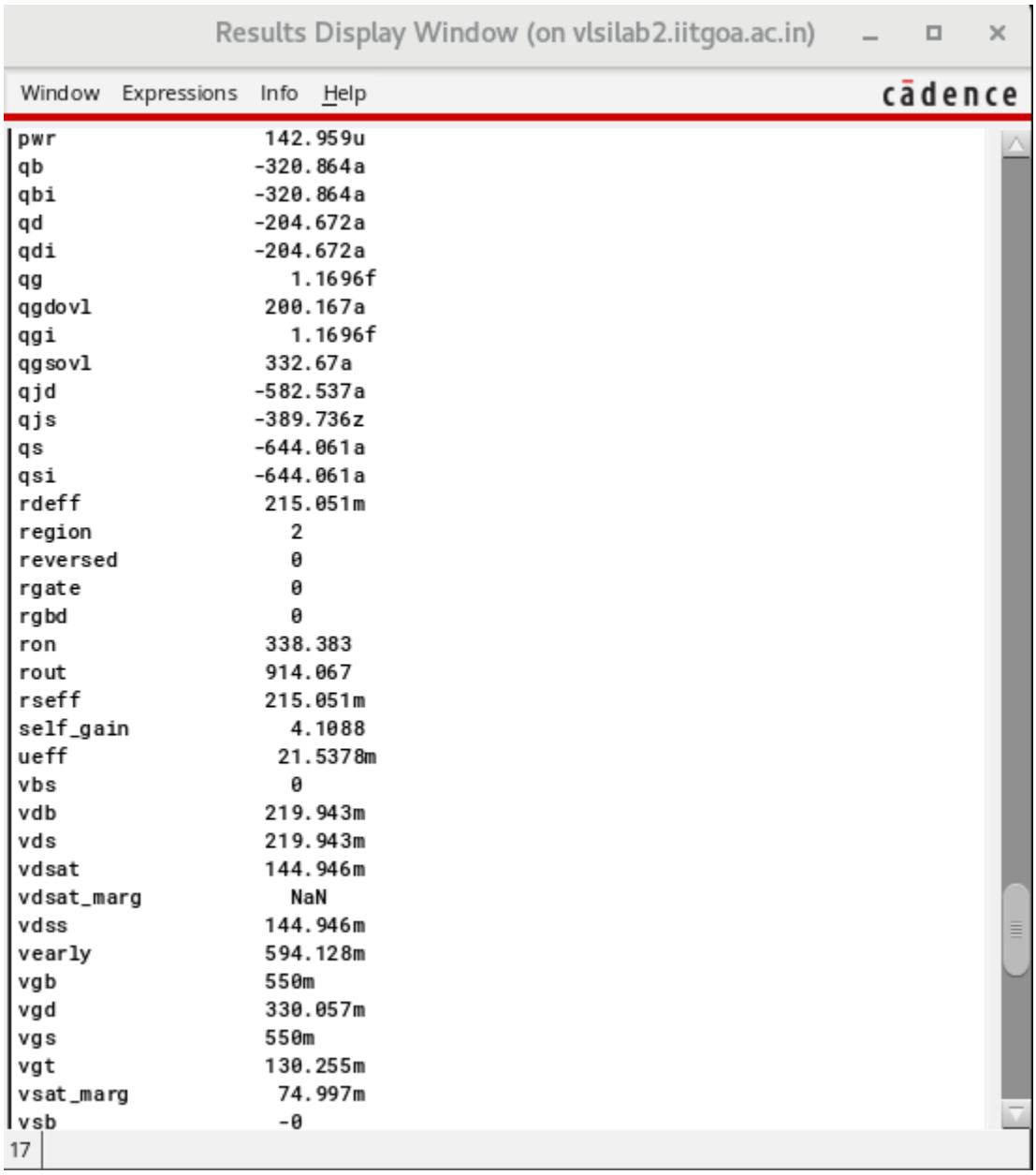


Figure: Simulation result of DC operating point analysis.

Observation: M5 is in region 2 (Saturation region of operation)

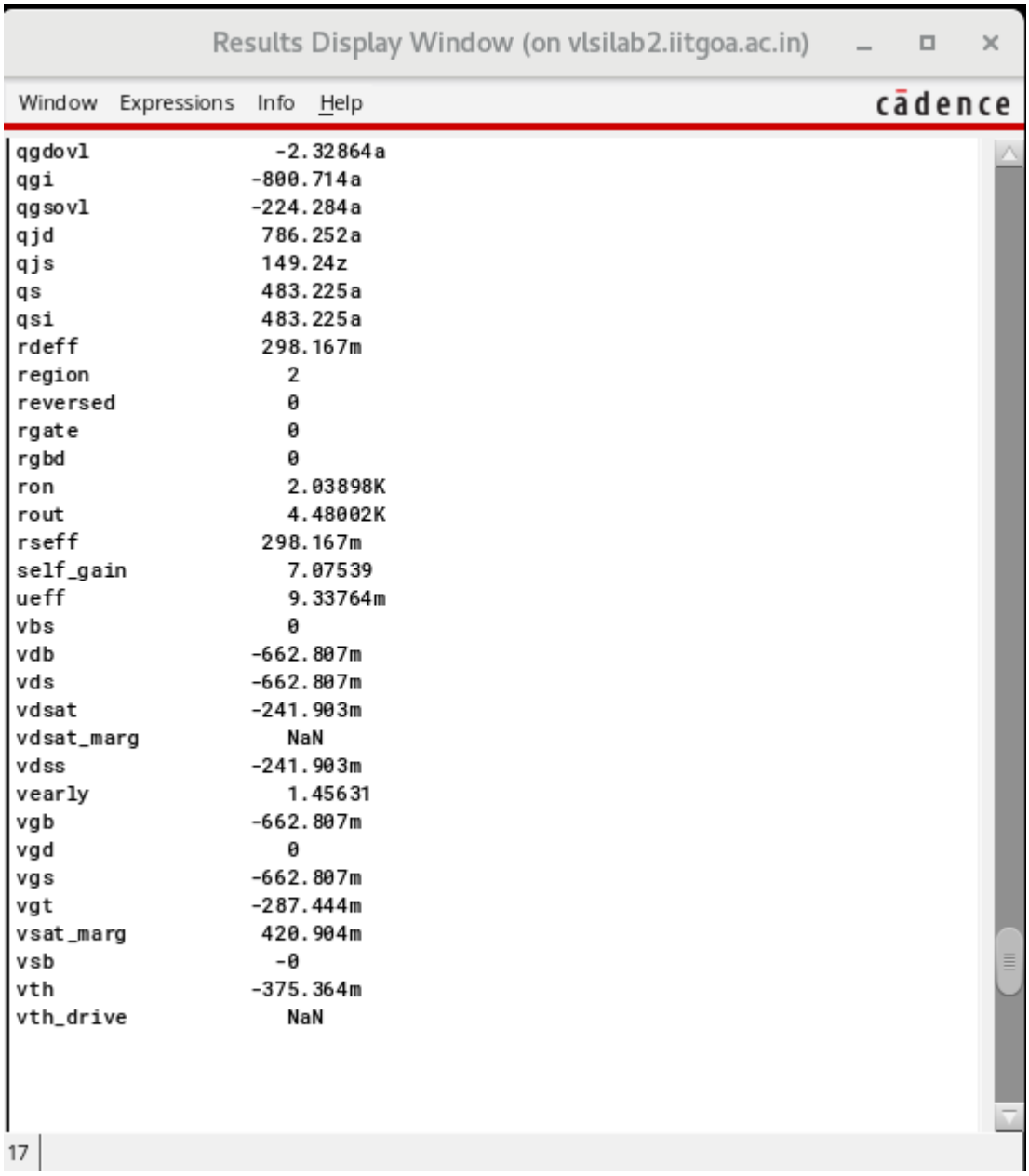


Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 (Saturation region of operation)

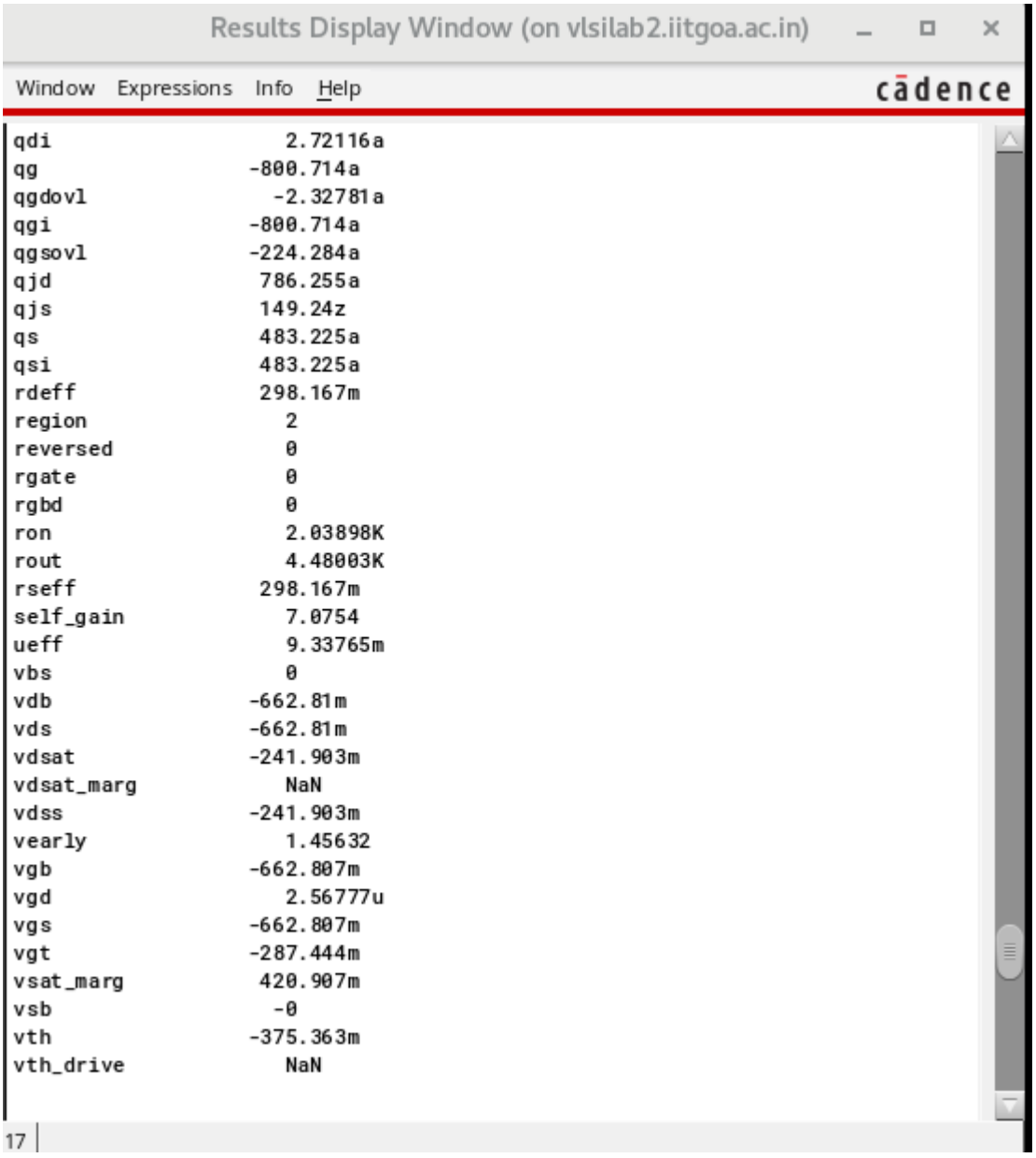


Figure: Simulation result of DC operating point analysis.

Observation: M4 is in region 2 (Saturation region of operation)

It is Verified that all the 5 transistors are in region 2 i.e Saturation region of operation.

(b) Perform the AC analysis of the circuit and find out the differential gain and 3 dB frequency.

Below are simulation results of the AC response analysis :

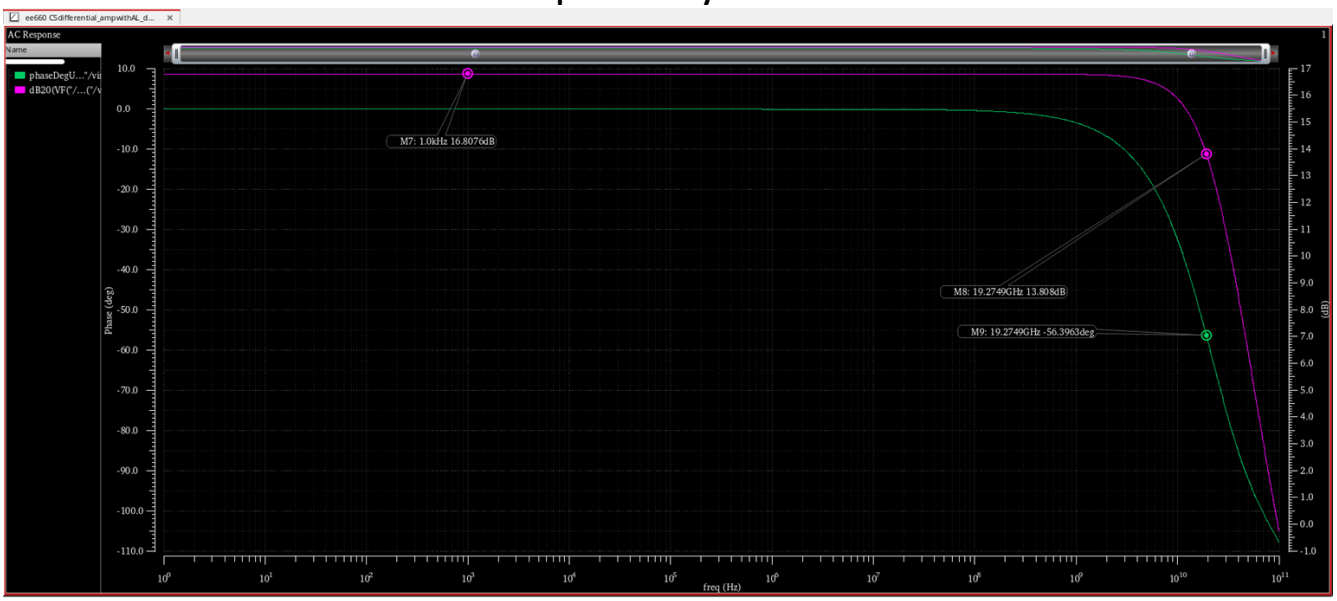


Figure: Plot showing Ac response analysis results (Vout,Vin1 considered)

Observations:From the above Ac Analysis plots we can say that :
1.Low frequency gain is **16.807dB**
2. 3dB cuttoff frequency is **19.27 GHz**
3.Phase difference between the input and output at the 3 dB frequency: -**56.39Degrees.**

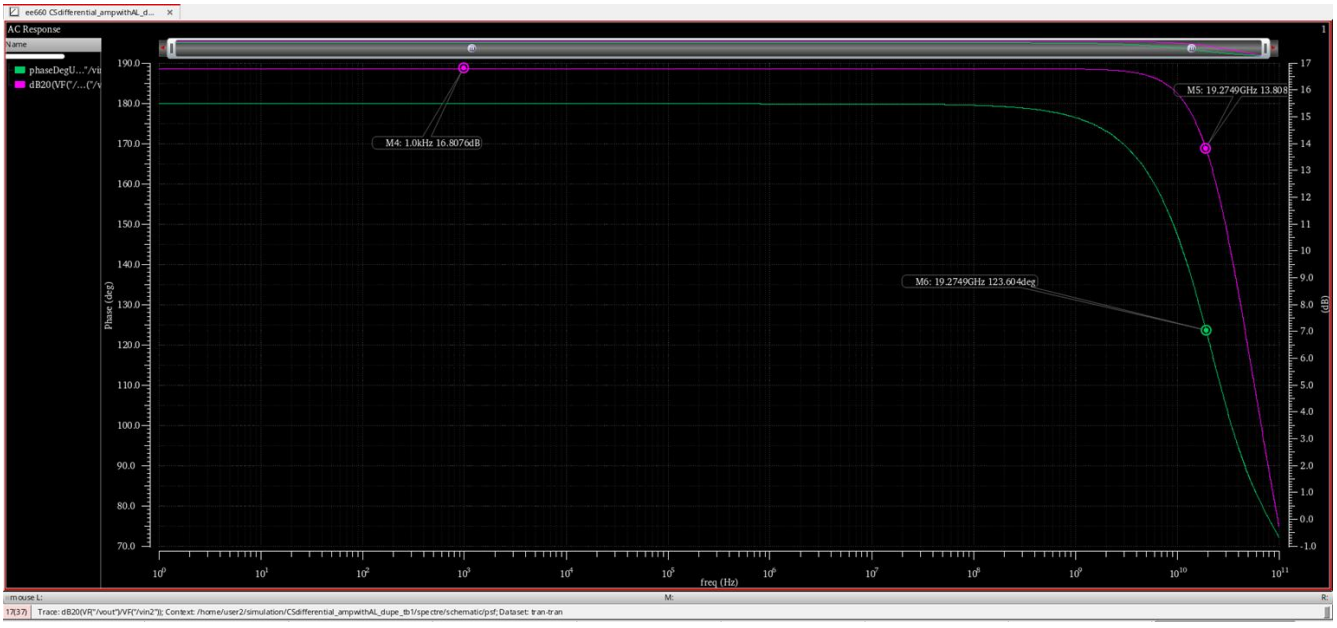


Figure: Plot showing Ac response analysis results (Vout,Vin2 considered)

Observations:From the above Ac Analysis plots we can say that :
1.Low frequency gain is **16.807dB**
2. 3dB cuttoff frequency is **19.27 GHz**

3.Phase difference between the input and output at the 3 dB frequency: **123.6Degrees.**

(c) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Below are the results of Transient analysis at vin =10mv:

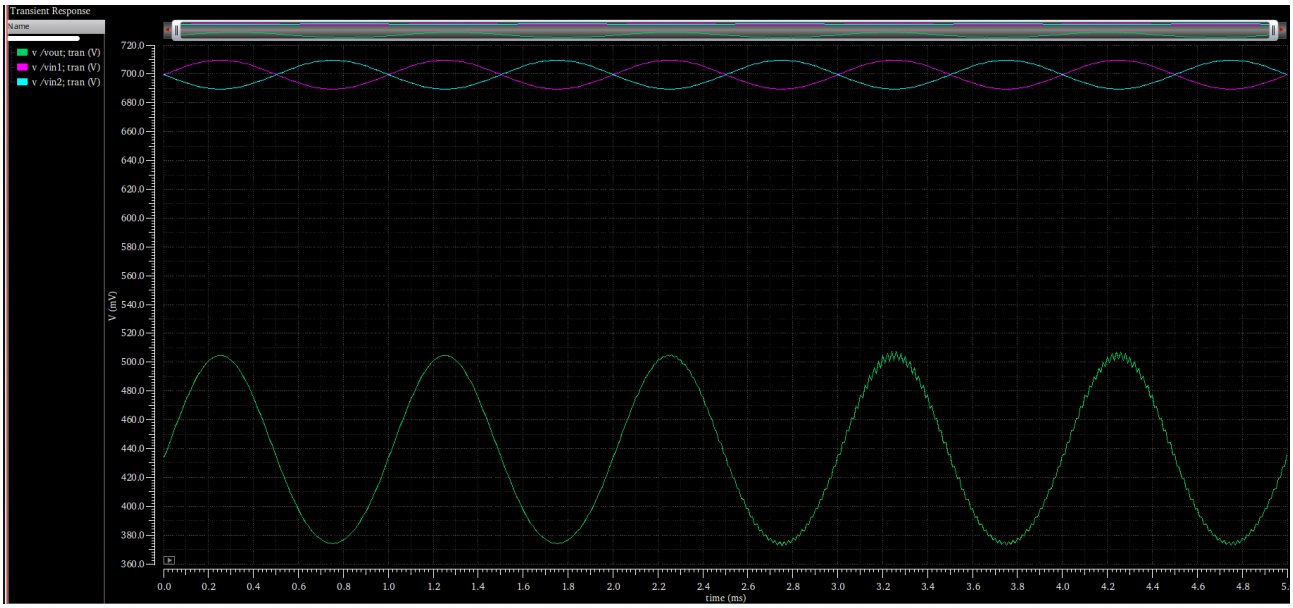


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

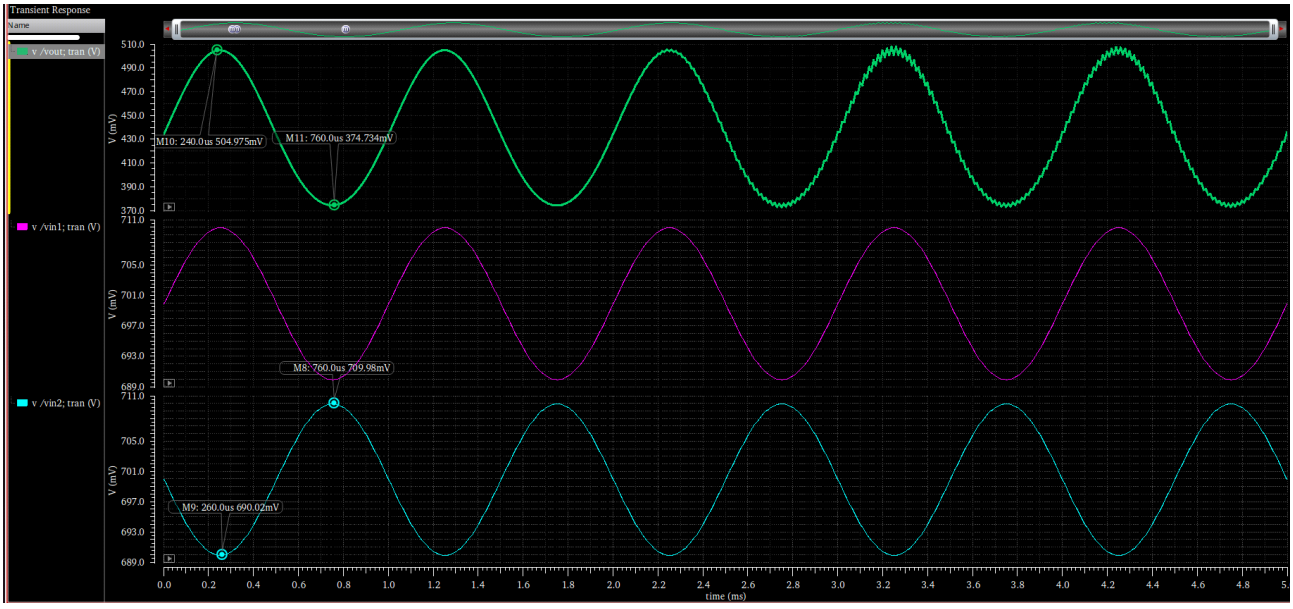


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

Below are the results of Transient analysis at vin =20mv:

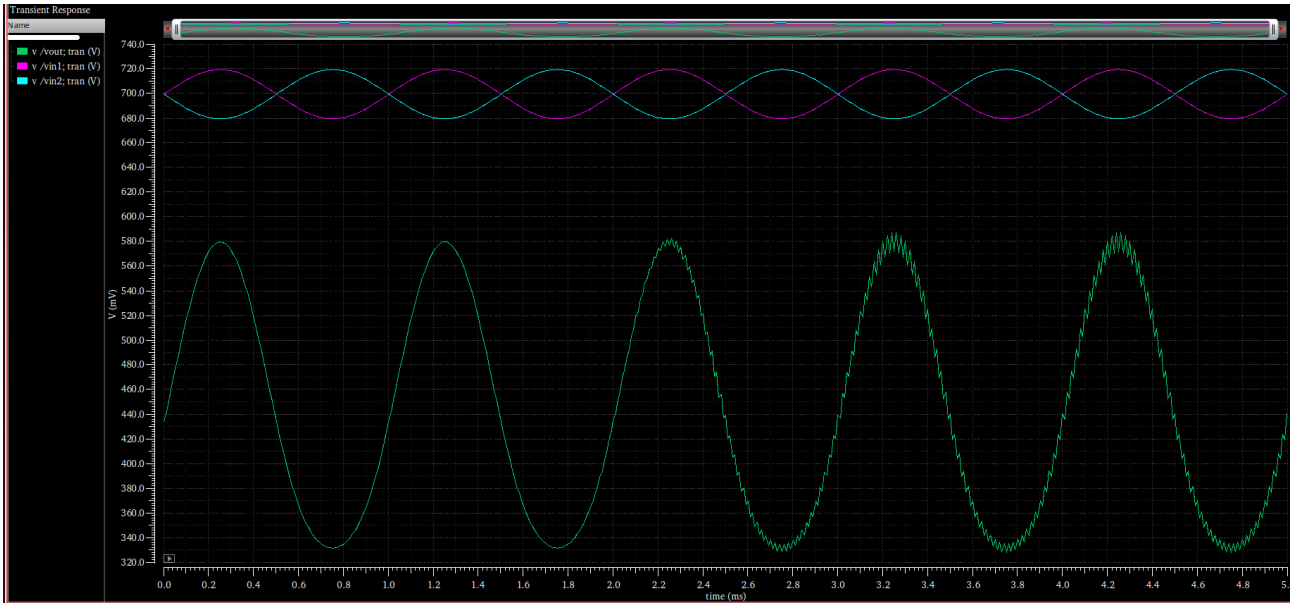


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

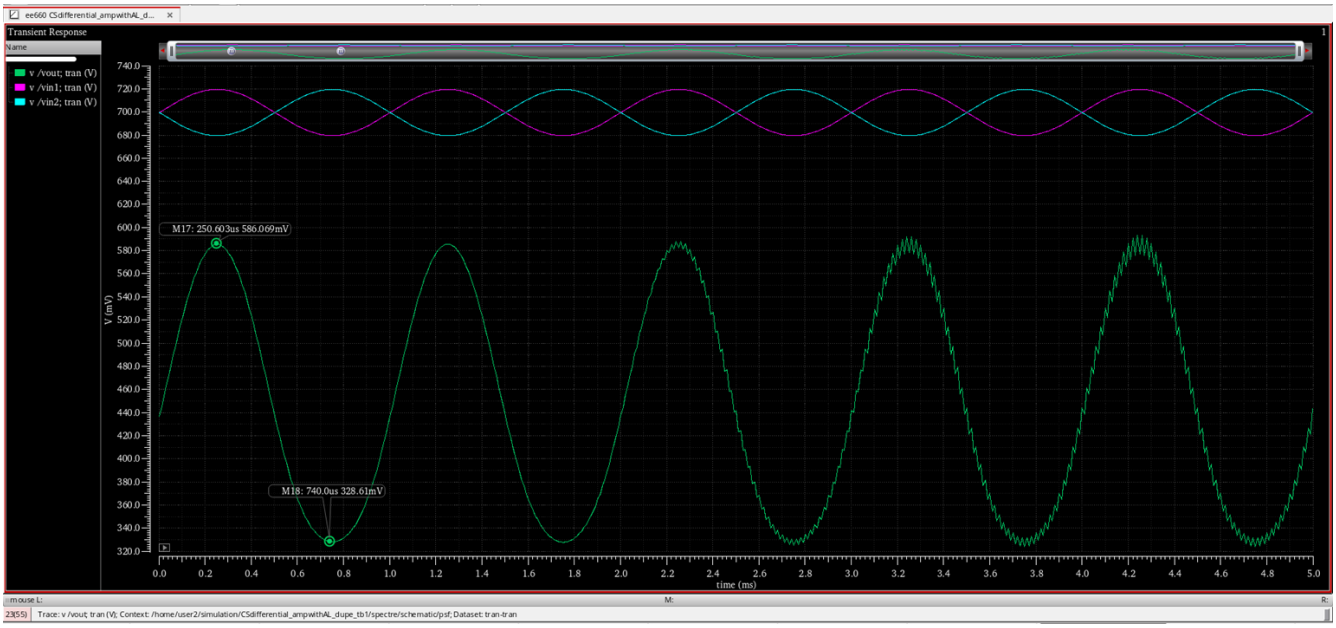


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

2. A draw a compact layout of the amplifier by cleaning DRC and LVS. Extract the netlist and do post-layout simulations of the steps mentioned in 1(a) to 1(c). Compare the pre- and post-layout simulation results. (You have to attach the screenshots of RVE indicating clean DRC, LVS, and PEX.)

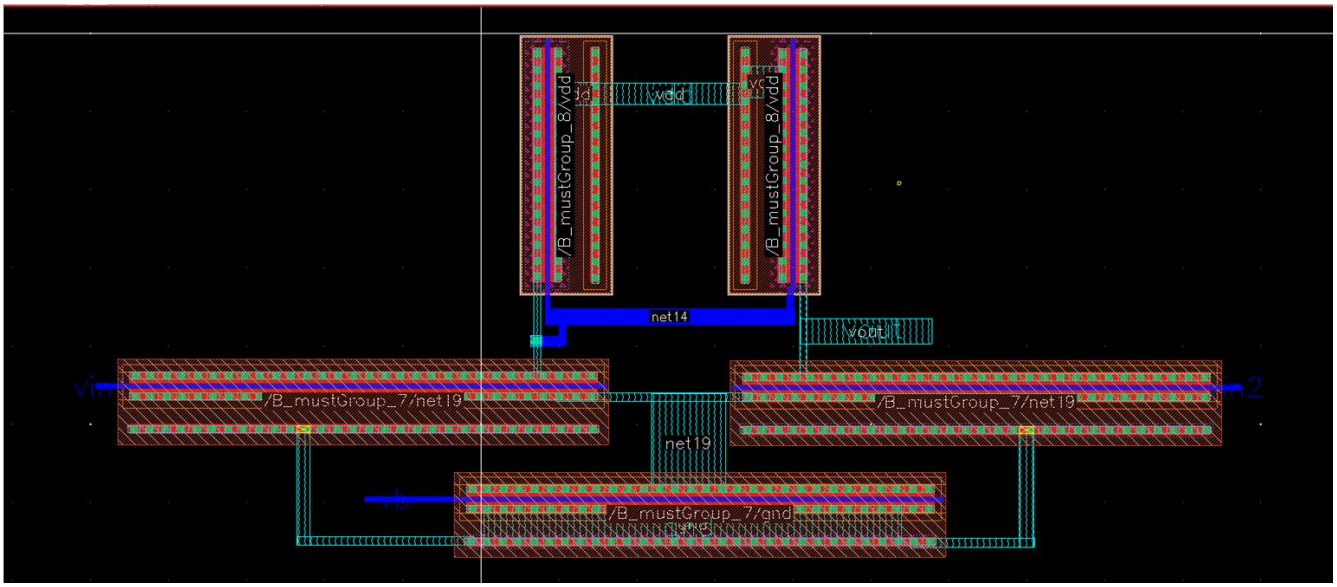
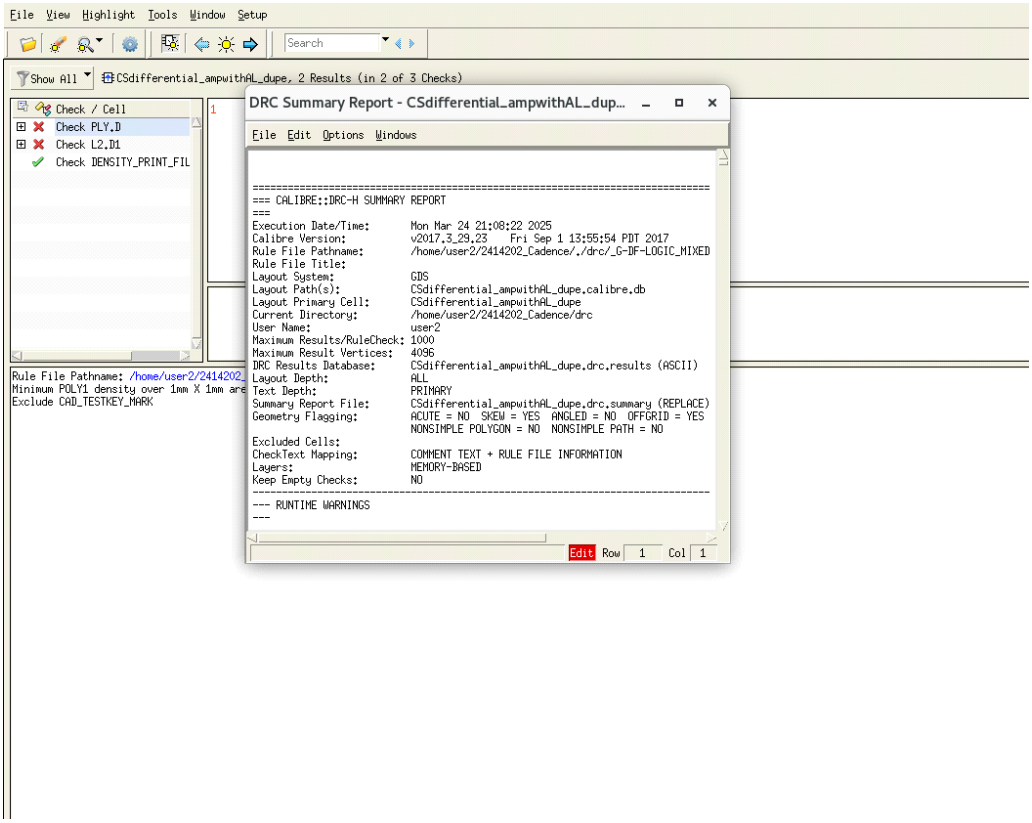
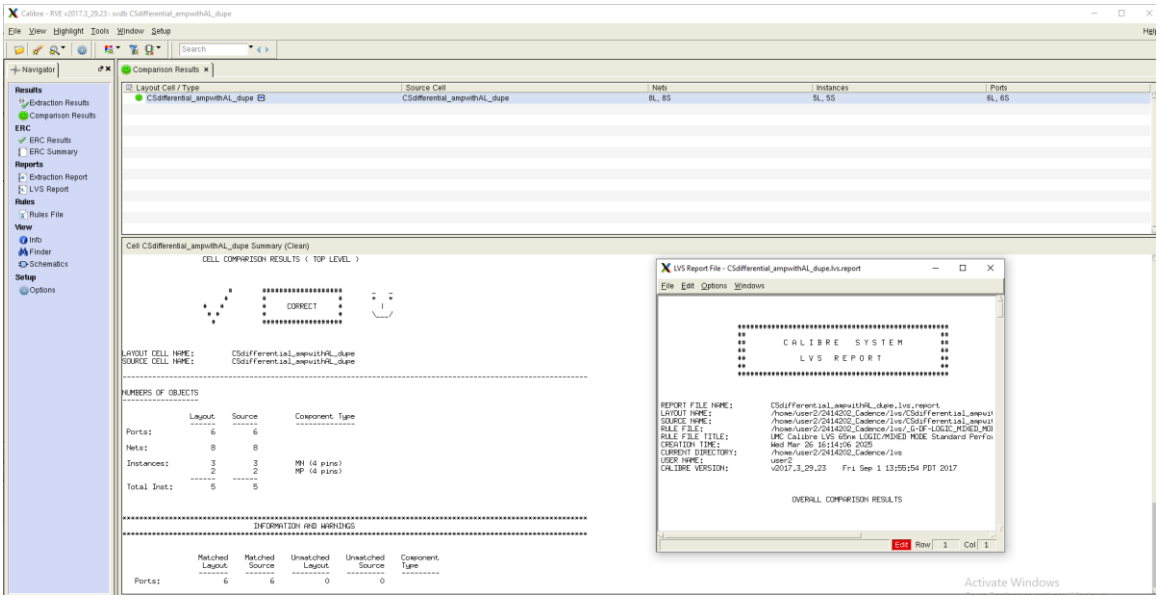


Figure: Layout of NMOS common-source differential amplifier with active load

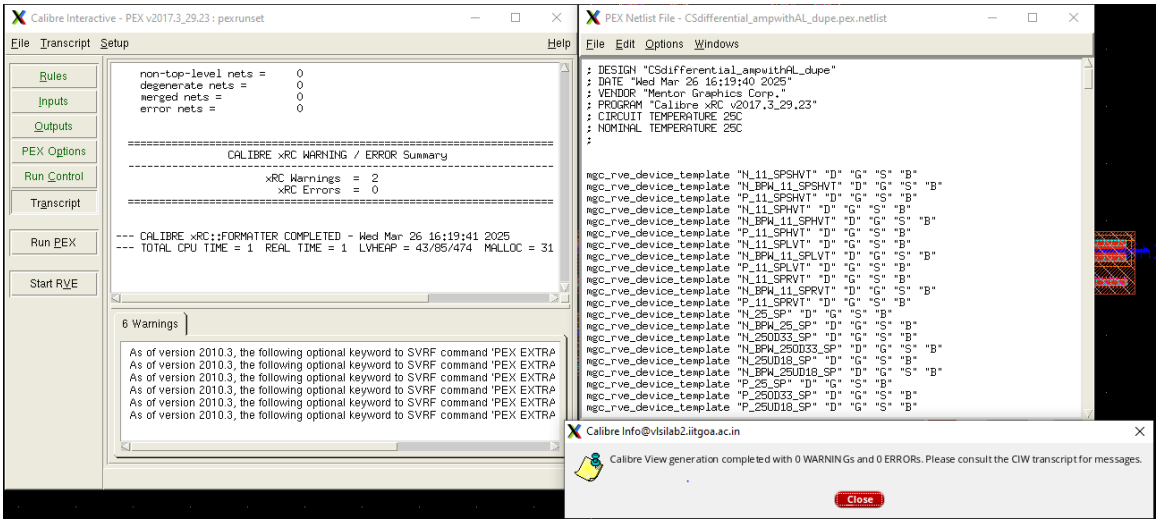
Below is the DRC Simulation result screenshot:



Below is the LVS simulation result screenshot:



Below is the PEX simulation result screenshot:



Post-layout simulations:

a)Perform the operating point analysis and check if all the transistors are in saturation region of operation.

Simulation result of first mosfet M1 :

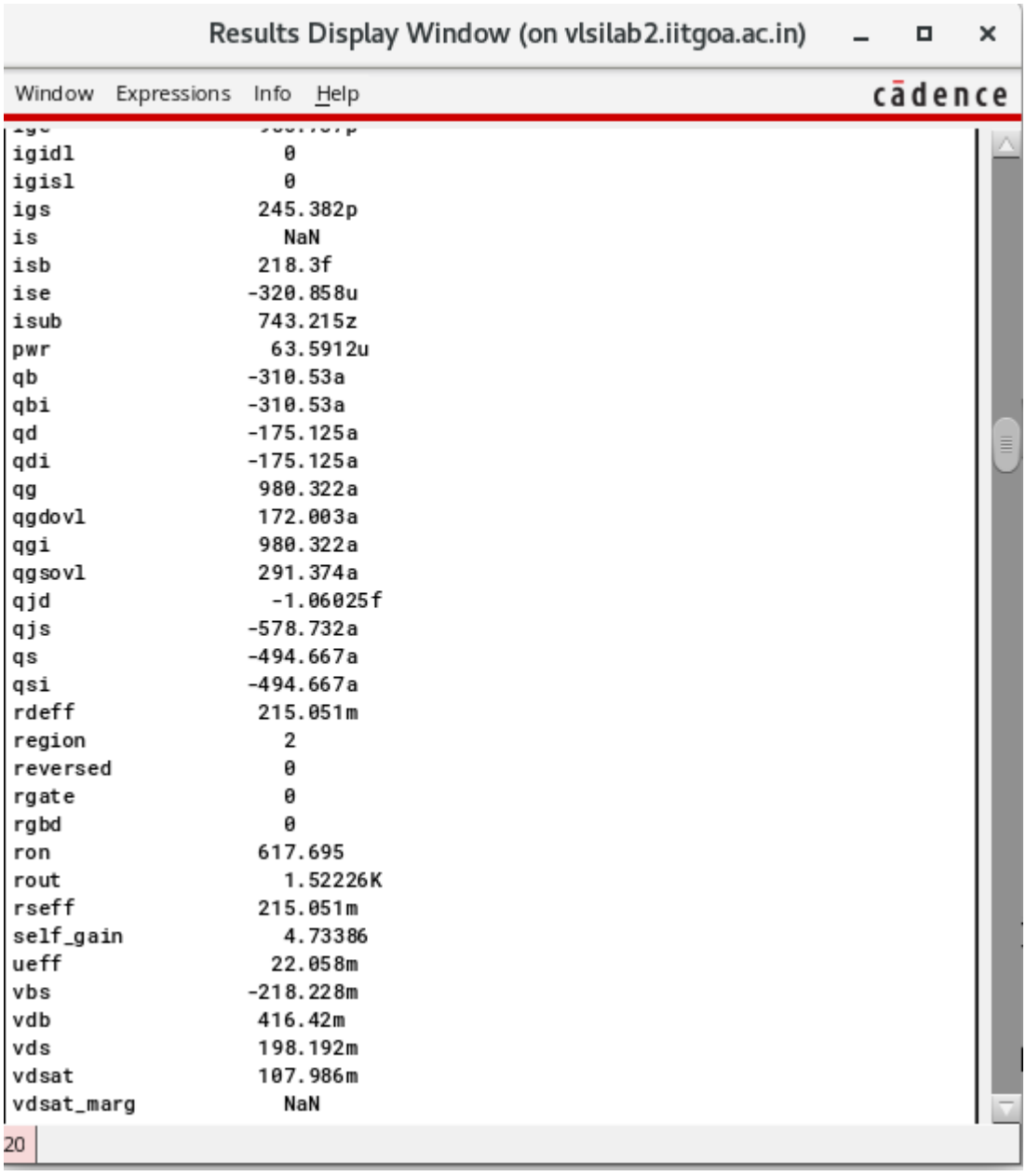


Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 (Saturation region of operation)

Simulation result of mosfet M2:

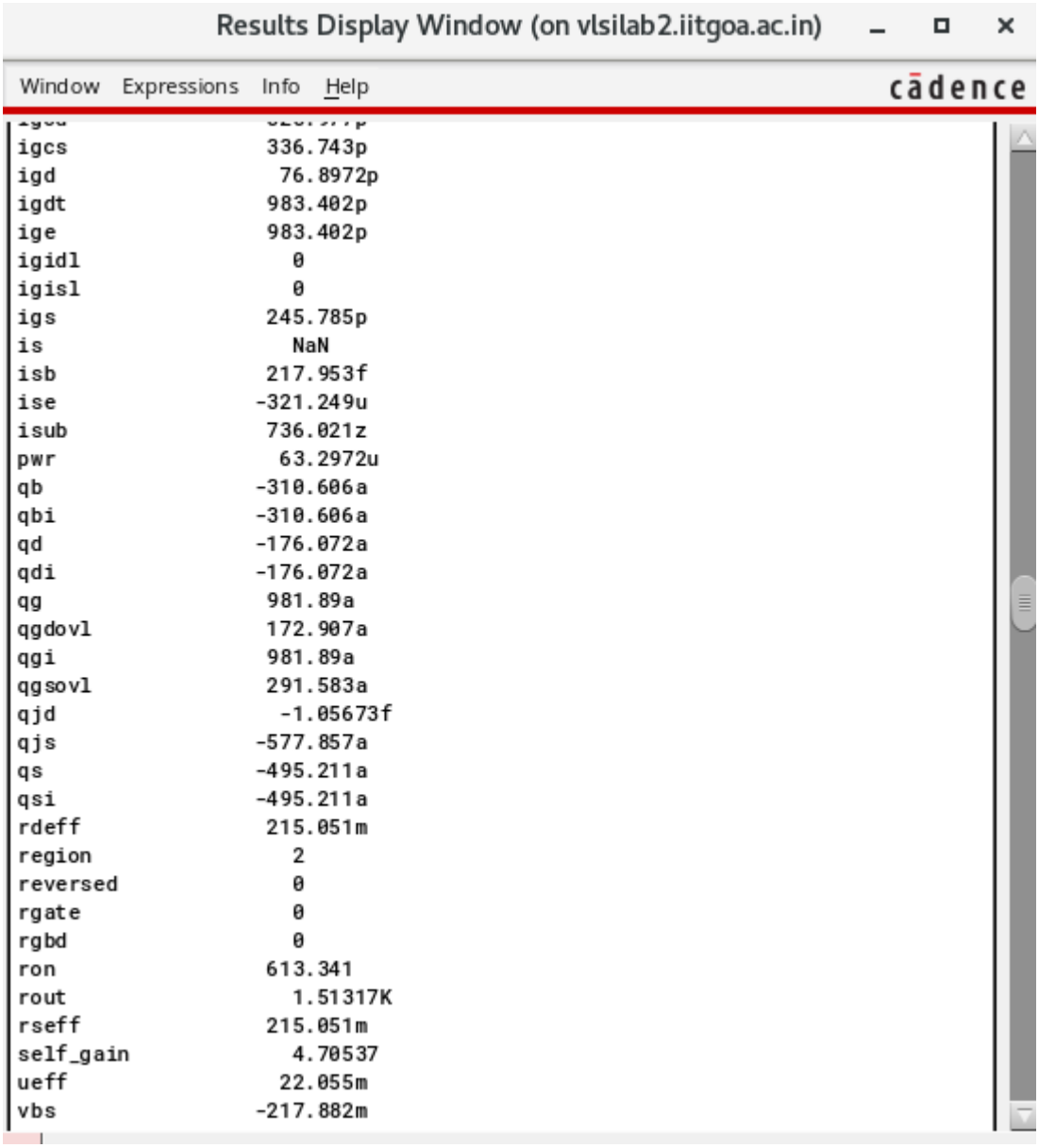


Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 (Saturation region of operation)

Simulation result of mosfet M5:

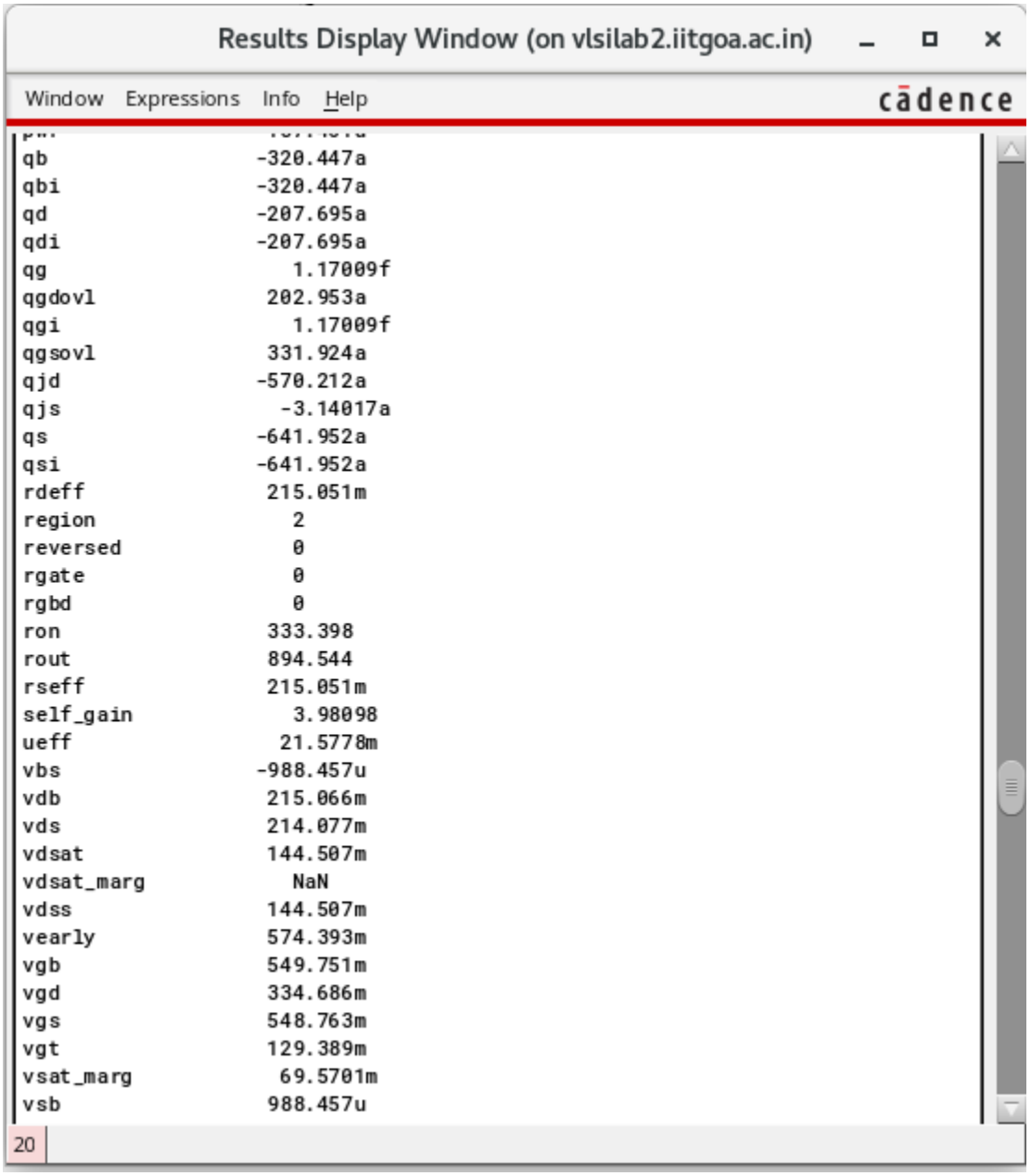


Figure: Simulation result of DC operating point analysis.

Observation: M5 is in region 2 (Saturation region of operation)

Simulation result of mosfet M3:

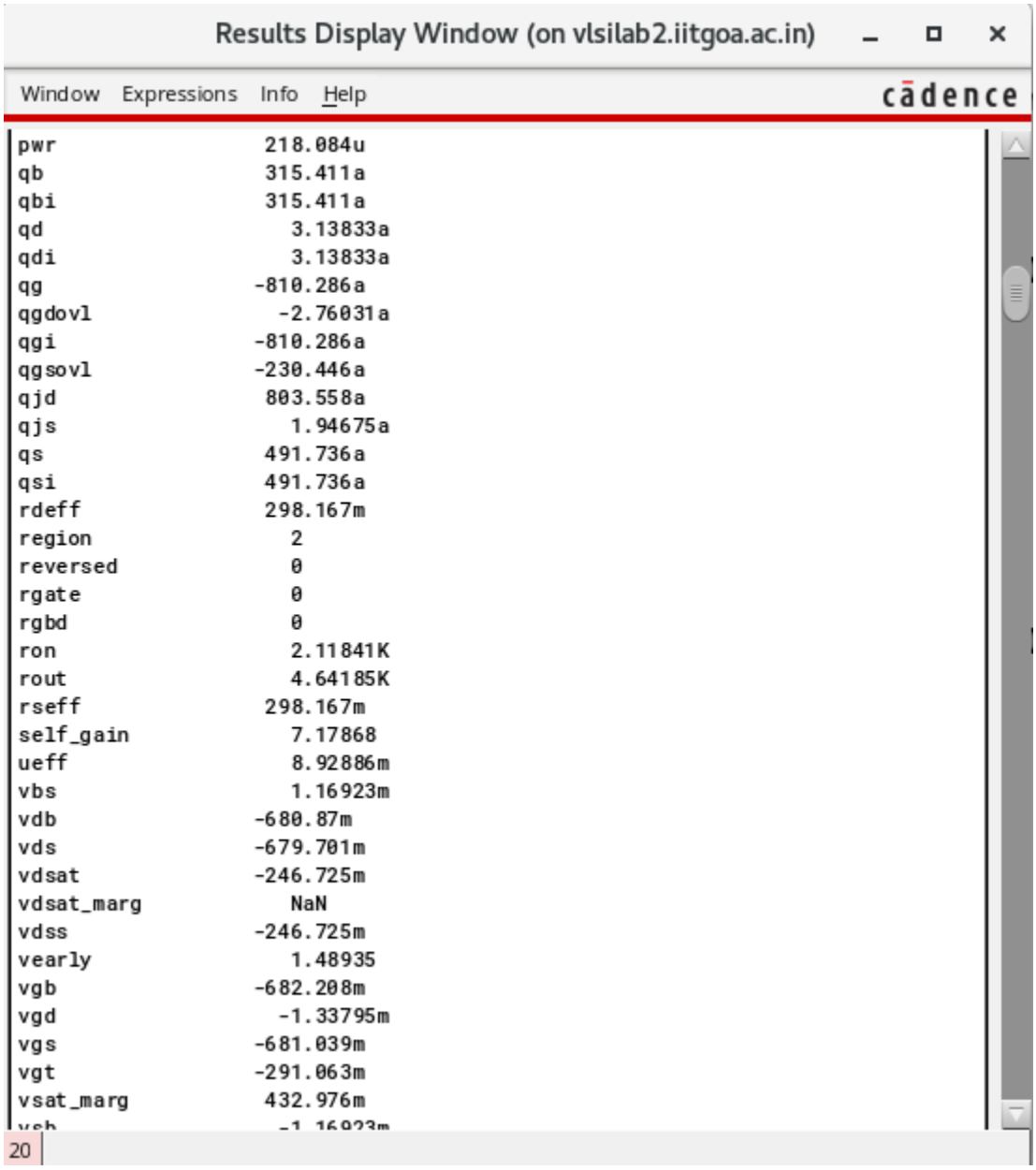


Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 (Saturation region of operation)

Simulation result of mosfet M4:

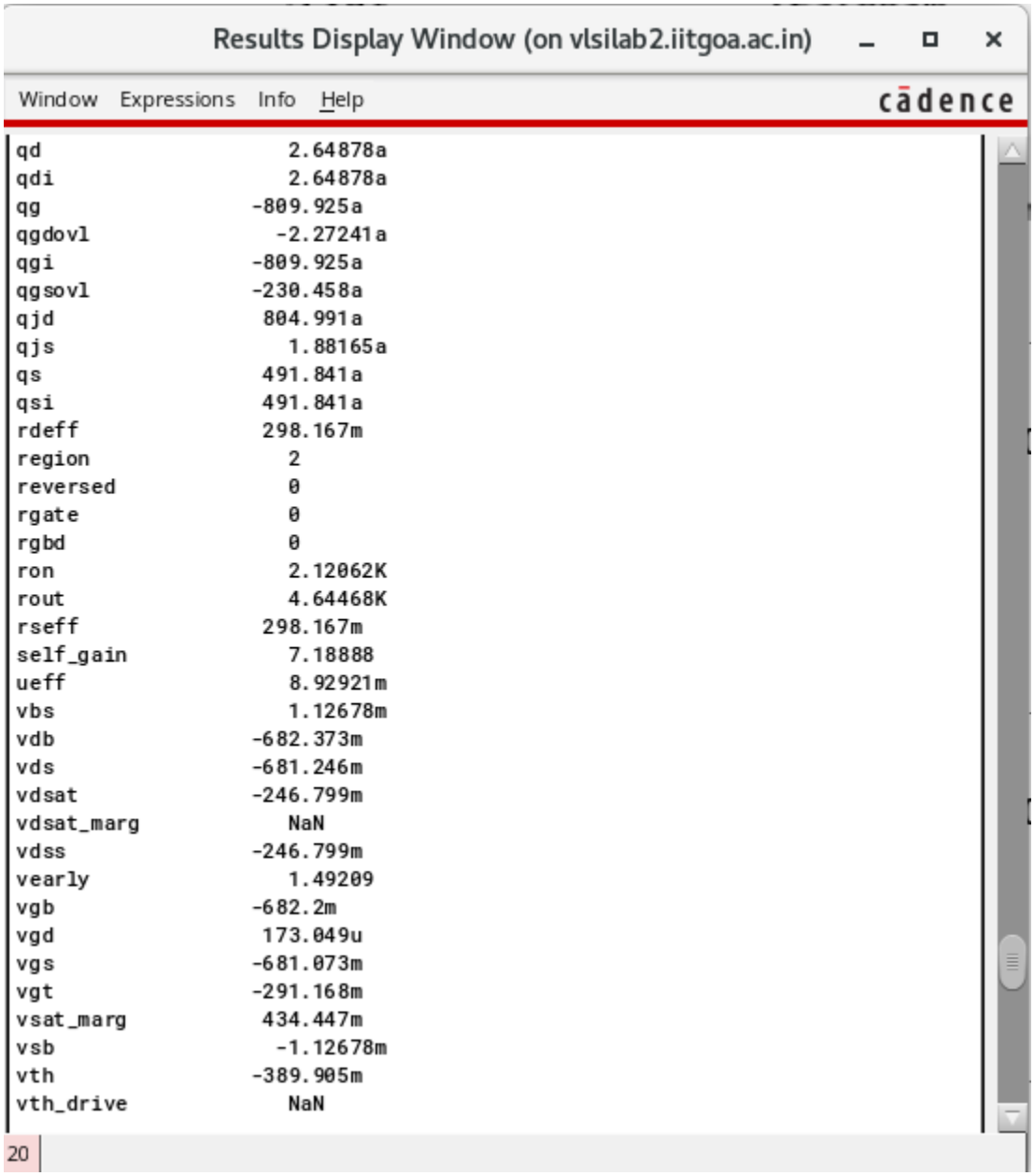


Figure: Simulation result of DC operating point analysis.

Observation: M4 is in region 2 (Saturation region of operation)

It is Verified that all the 5 transistors are in region 2 i.e Saturation region of operation.

(b) Perform the AC analysis of the circuit and find out the differential gain and 3 dB frequency.

Below are simulation results of the AC response analysis :

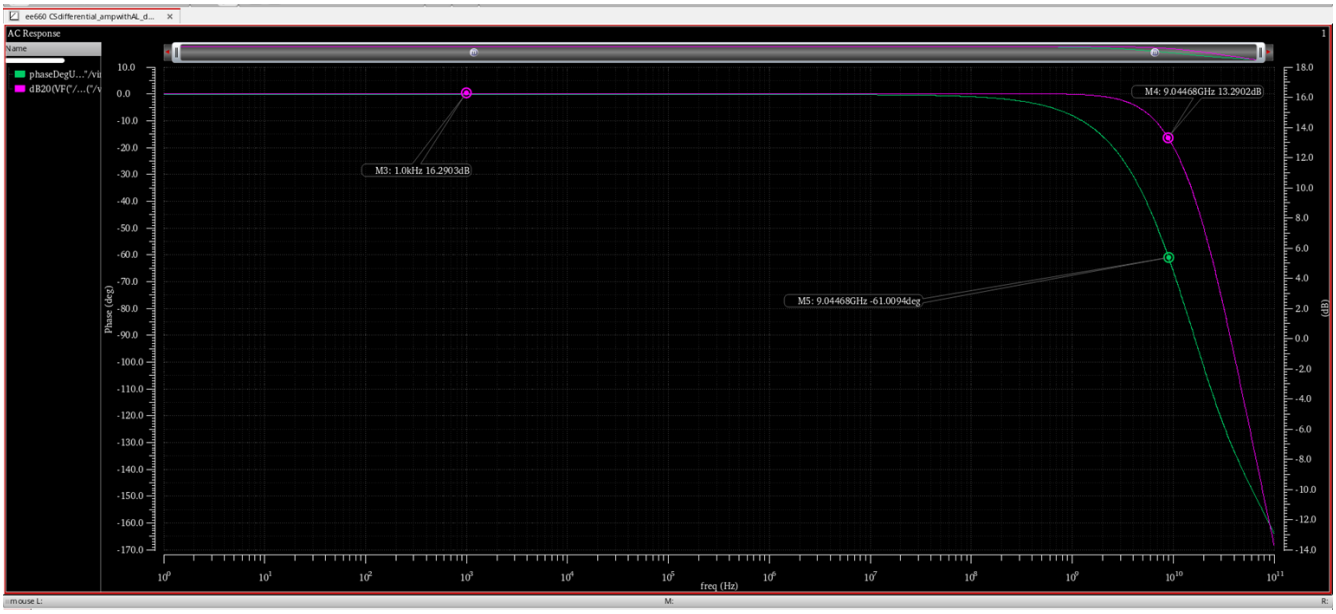


Figure: Plot showing Ac response analysis results (Vout,Vin1 considered)

Observations:From the above Ac Analysis plots we can say that :

1.Low frequency gain is **16.290dB**

2. 3dB cuttoff frequency is **9.044 GHz**

3.Phase difference between the input and output at the 3 dB frequency: **-61Degrees.**

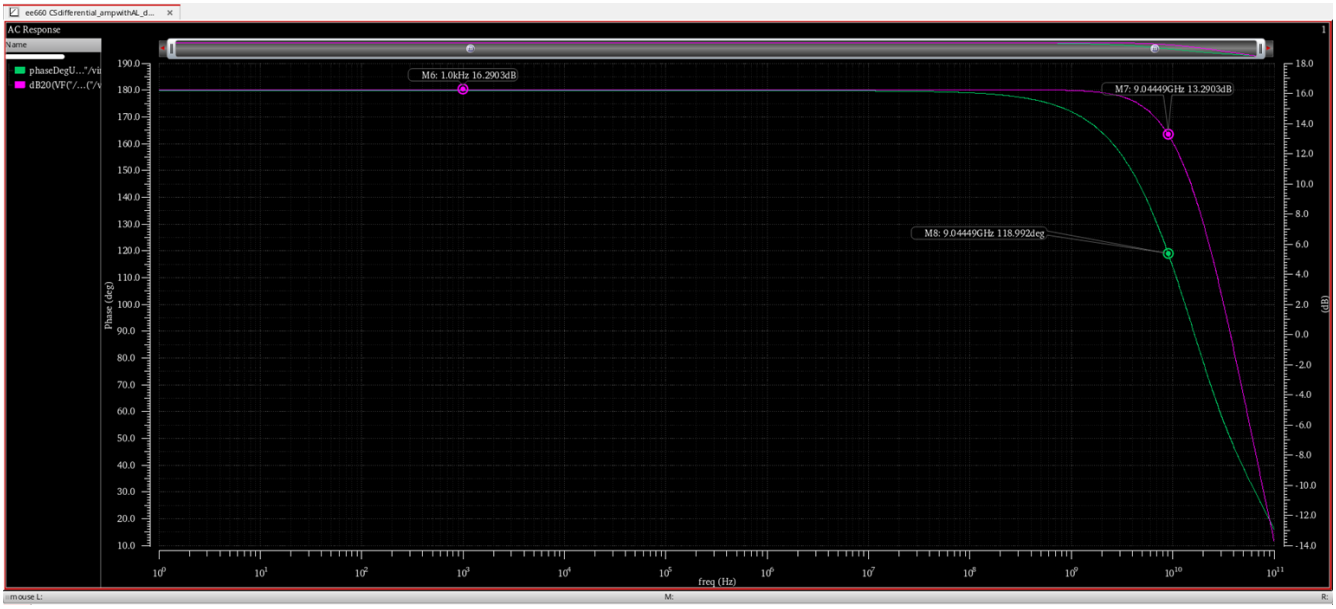


Figure: Plot showing Ac response analysis results (Vout,Vin2 considered)

Observations:From the above Ac Analysis plots we can say that :

1.Low frequency gain is **16.290dB**

2. 3dB cuttoff frequency is **9.044 GHz**

3.Phase difference between the input and output at the 3 dB frequency: **118.99 Degrees.**

(c) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Below are the results of Transient analysis at vin =10mv:

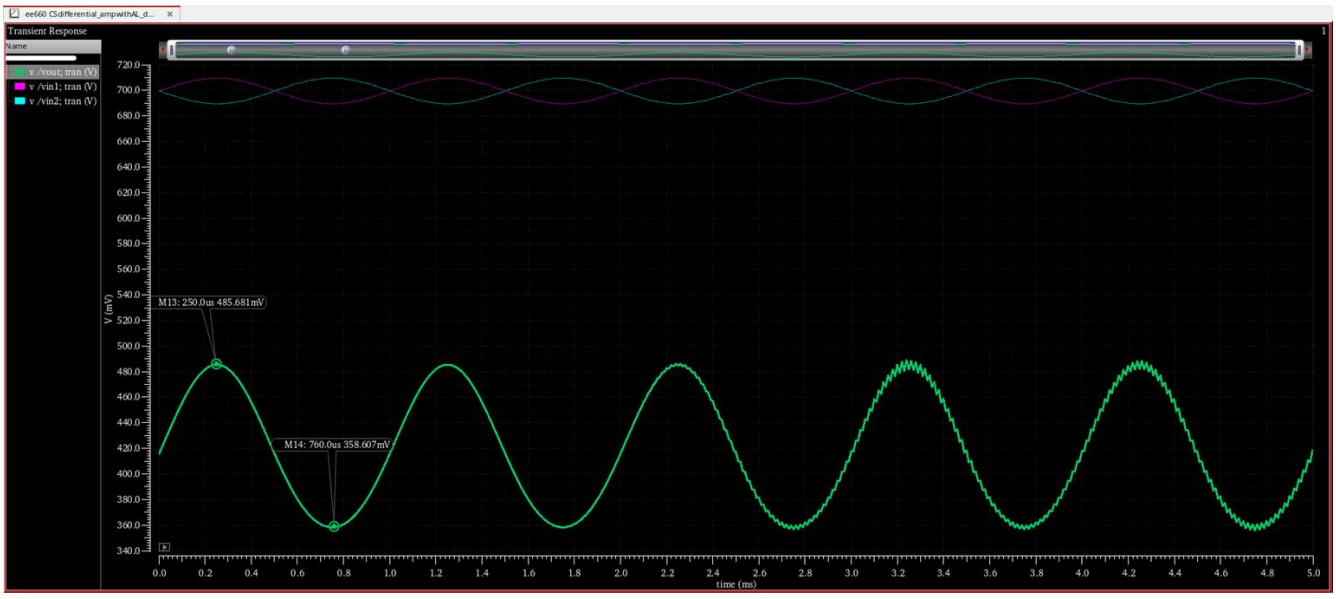


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

Below are the results of Transient analysis at vin =20mv:

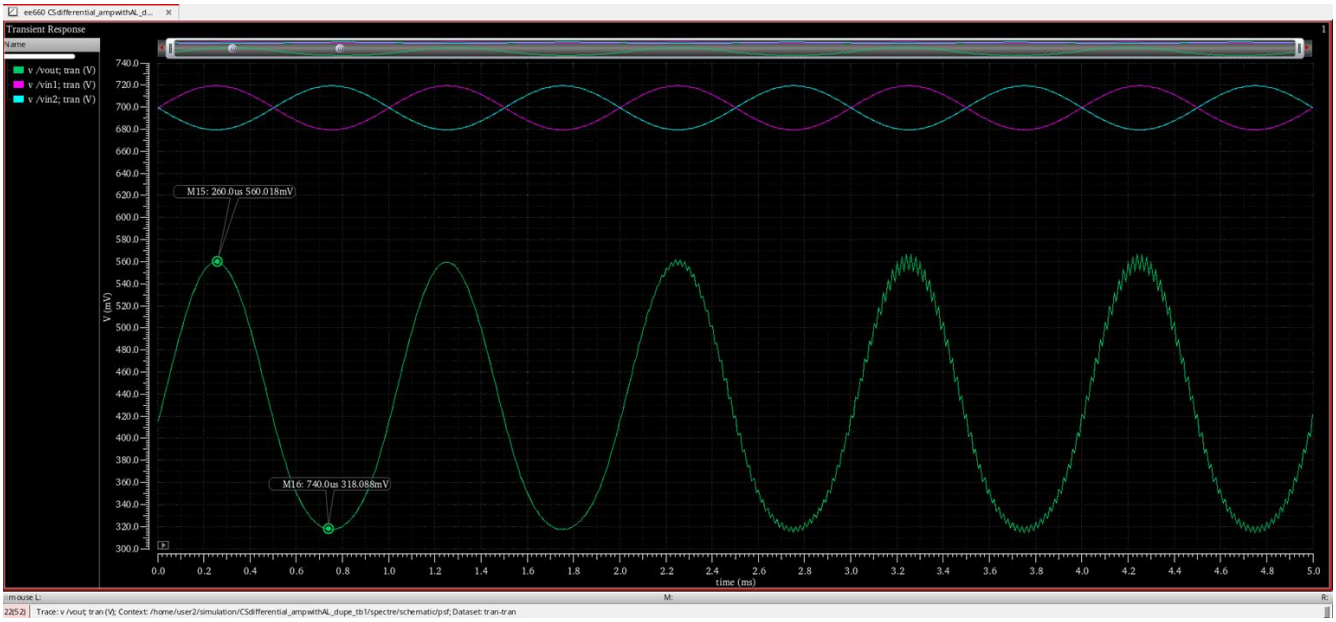


Figure:Plot showing transient analysis simulation result (Vout w.r.to Vin1,Vin2)

Comparison between pre- and post-layout simulation results:

1. **DC Analysis**: When Vb = 0.55 V, and Vin,dc = 0.7 V both pre-layout and post-layout results confirm that all transistors (M1, M2, M3, M4, M5) are in the **saturation region**.

2. **AC Analysis**:

   i)Low frequency gain:
   The pre-layout gain is **16.807 dB**, while the post-layout gain is **16.290 dB** which resulted in **0.517 dB drop in gain**.This is mainly due to the resistance and capacitance developed by metal wires and interconnects in the layout.

   ii) **3dB cuttoff frequency:**
   3 dB cutoff frequency dropped from **19.27 GHz** (pre-layout) to **9.044 GHz** (post-layout).This is mainly due to the fact that large interconnects are used in layout design due to which parasitic capacitance has increased significantly. Also,contact and via resistances introduced in layout design.All these factors reduced bandwidth since bandwidth is Inversely proportional to RC .

   iii) Phase difference between the input and output at the 3 dB frequency:
   For pre-layout simulation the phase shift from **Vin1 to Vout** was **-56.39°**, but after for post-layout , it increased to **-61.00°**, adding an extra **-4.61° delay** due to parasitic effects.

   For pre-layout simulation the phase shift from **Vin2 to Vout** was **123.60°**, but after for post-layout , it increased to **118.99°**, reducing by **4.61°** because of added resistance and capacitance in the circuit.

3. **Transient Analysis:**

   At 10mV : pre –layout simulation has Vout,peak : 504.97mv, Vout,min :374.73 mv
   Post –layout simulation has Vout,peak : 485mv, Vout,min :358 mv

   At 20mV : pre –layout simulation has Vout,peak : 586 mv, Vout,min :328 mv
   Post –layout simulation has Vout,peak : 560mv, Vout,min :318 mv

   It is observed that there's a slight decrement in Vout values of post layout transient simulation . This is mainly due to the **Parasitic resistance in routing**, which causes voltage drops and reduces both peak and minimum output levels for layout.