

EE 660 VLSI Design Laboratory

Assignment IV

Submitted by: L Sri Sai Swathi (2414202)

1. You have done the schematic level simulations of a CS amplifier as shown in Fig. 1 in Assignment
2. Taking the same cell as the schematic, complete its layout

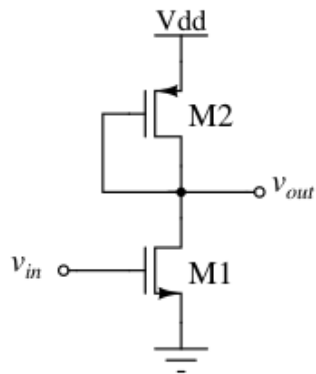


Figure 1: Common-source amplifier with diode connected load.

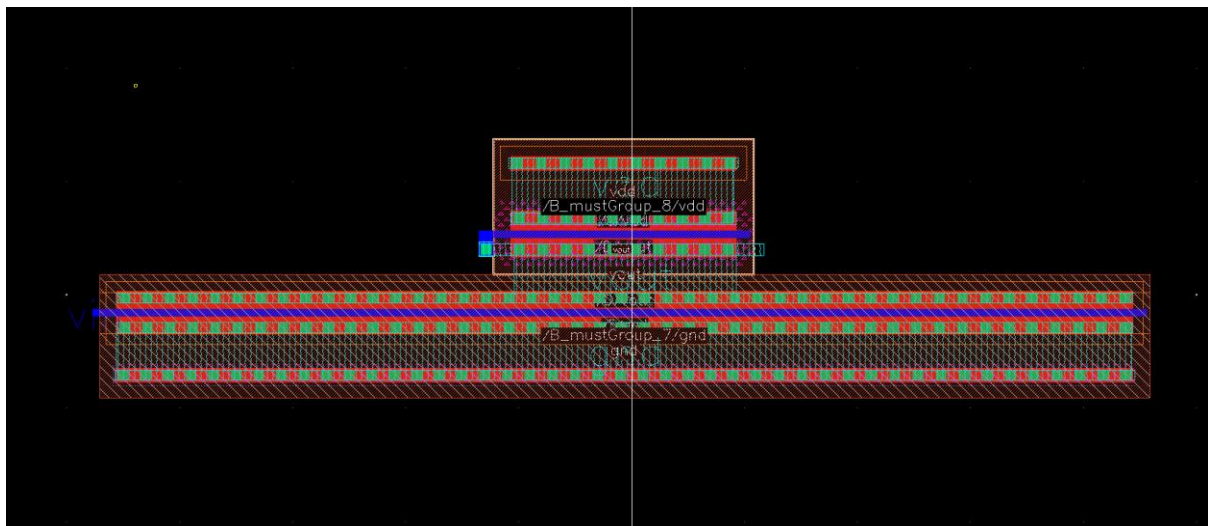


Figure : Layout of CS Amplifier with PMOS diode connected load

2. Using the same test bench do a post-layout large signal analysis of the circuit by doing a DC sweep of the input voltage from 0 to V_{DD} (1.1 V). Decide the input common-mode voltage at the centre of the region where both M1 and M2 are in saturation. Mention if you see any difference in the large signal transfer characteristics between pre- and post-layout simulations.

Results of Post-layout large signal analysis when V_{in} dc is swepted from 0 to 1.1v(V_{DD})

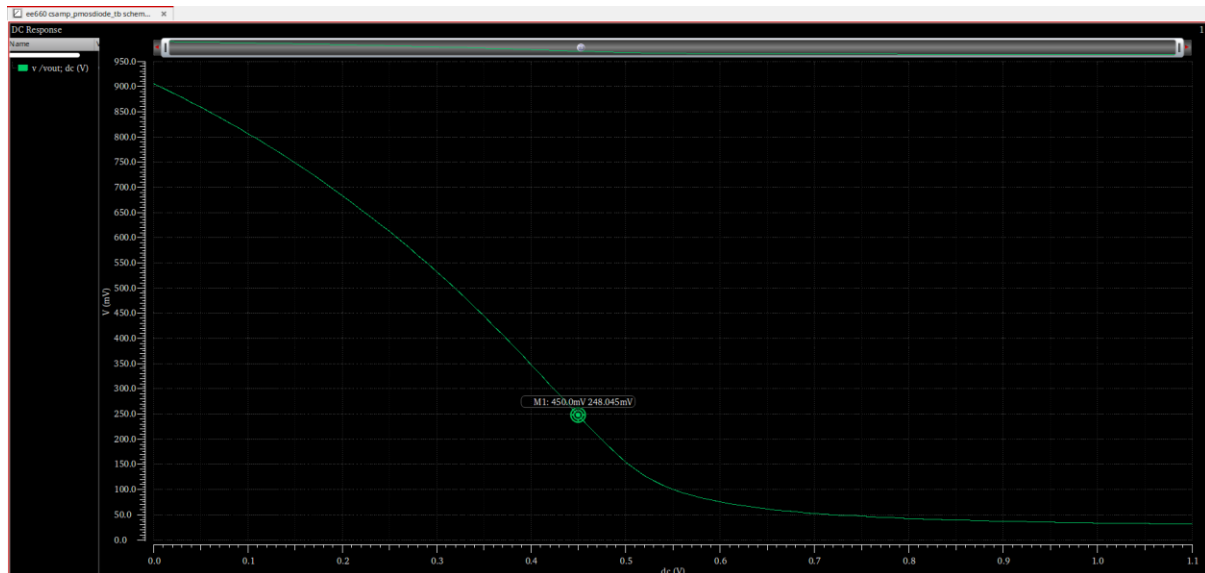
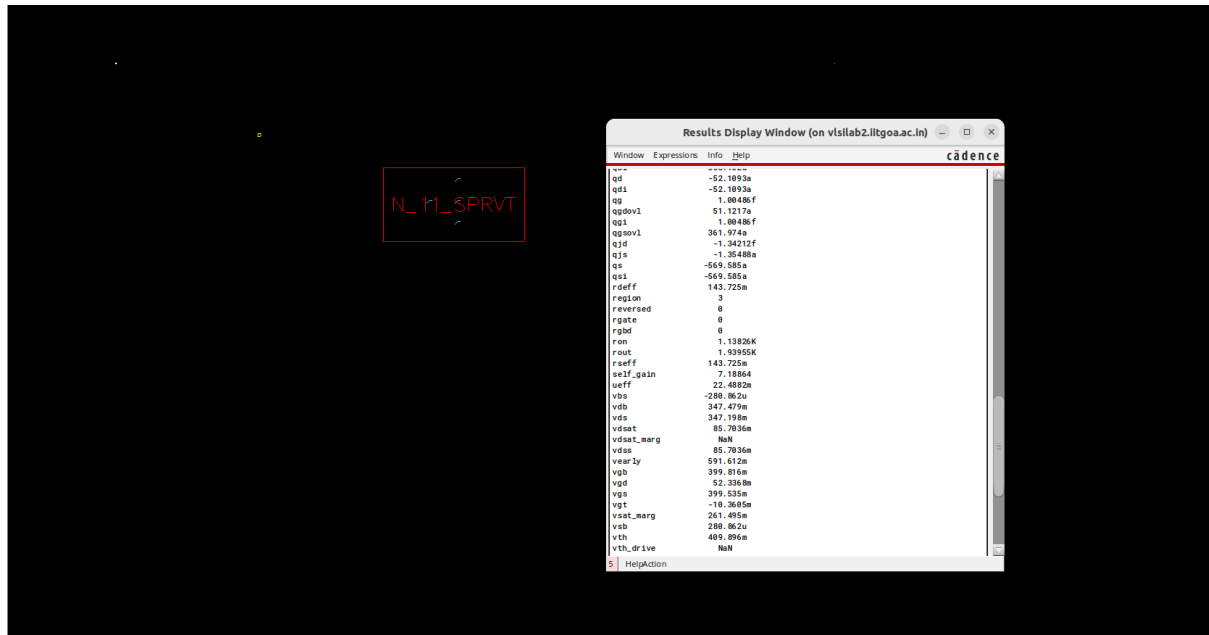


Figure: Plot showing V_{out} vs V_{in}

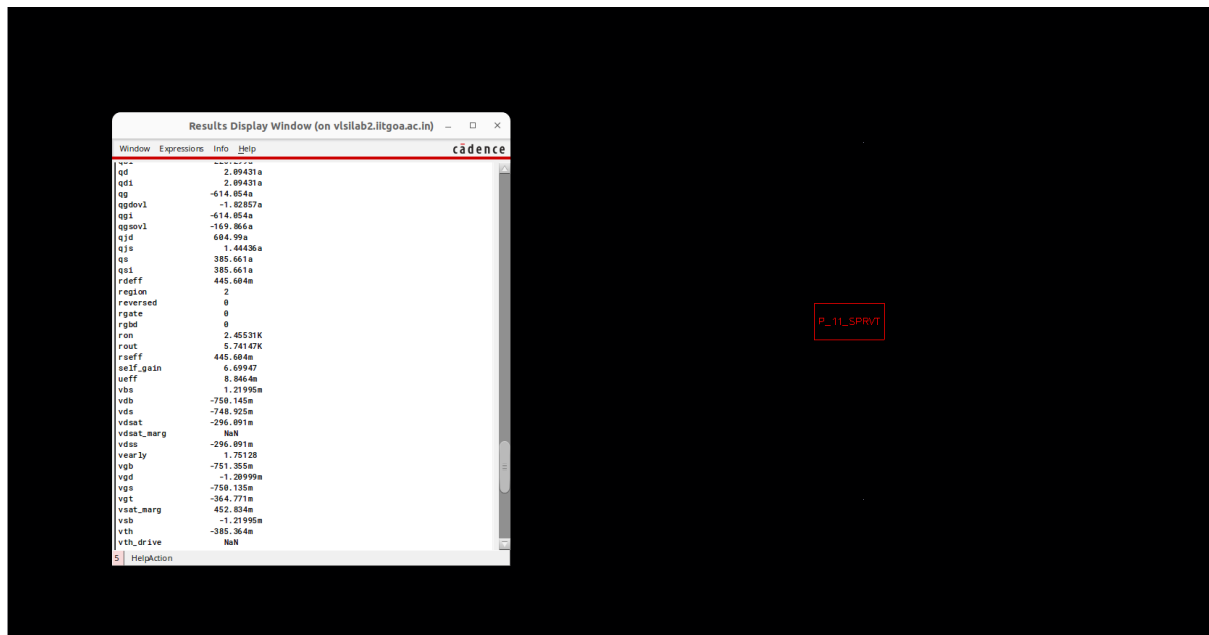
From the plot , Assumed **0.4v** as common mode voltage and verified as follows:-

Below are the simulation results of Analysis done at **400mv**

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 3 of Operation, which means “Cuttoff region”. It is also noted that $V_{tn} = 0.409v$.



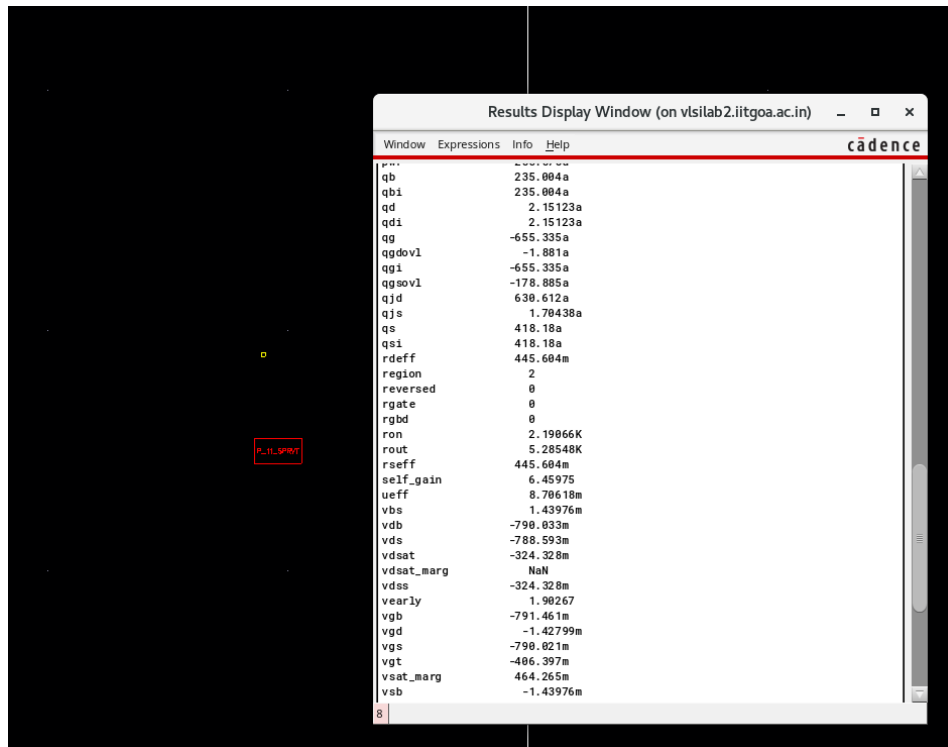
Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “Saturation region”. It is also noted that $|V_{tp}| = 0.385v$.



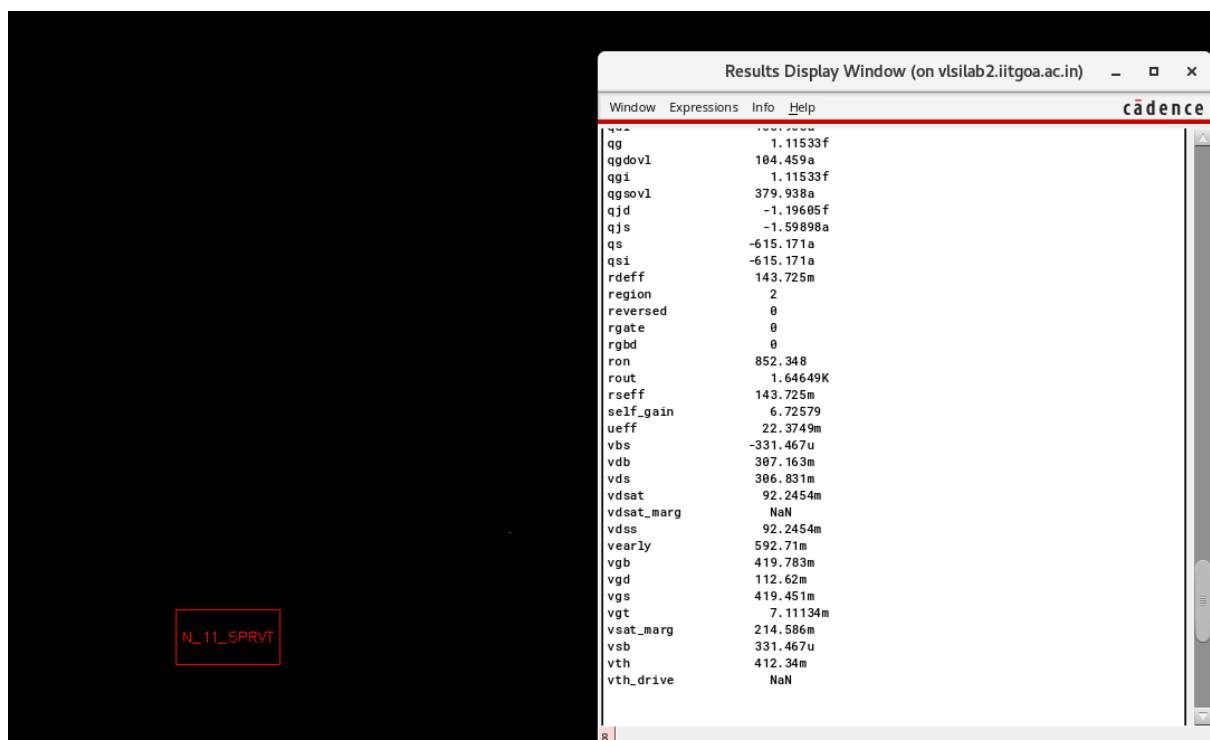
Observation : Since both transistors are **not in saturation** when we chose VGS as 400mV , we are choosing another value 420mV which is greater than both vtn and vtp.

Below are the simulation results at 420mv:

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means **“Saturation region”**



Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of operation which means **“Saturation region”**

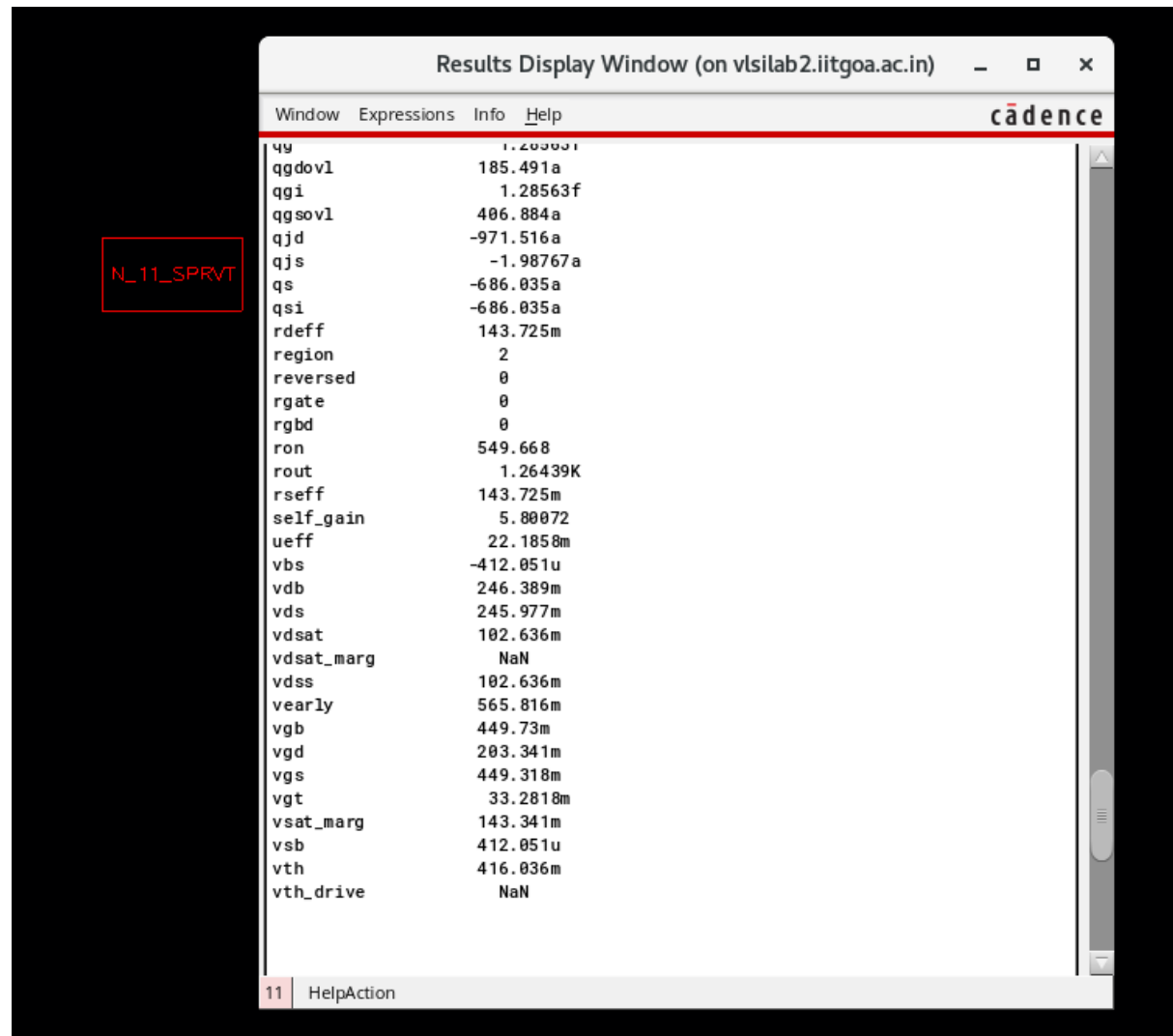


Observation: From the above analysis, it has been verified that 2 transistors are in Saturation region of

operation when **Vgs=420mV**.

Below are the simulation results of Analysis done at vgs=450mv:

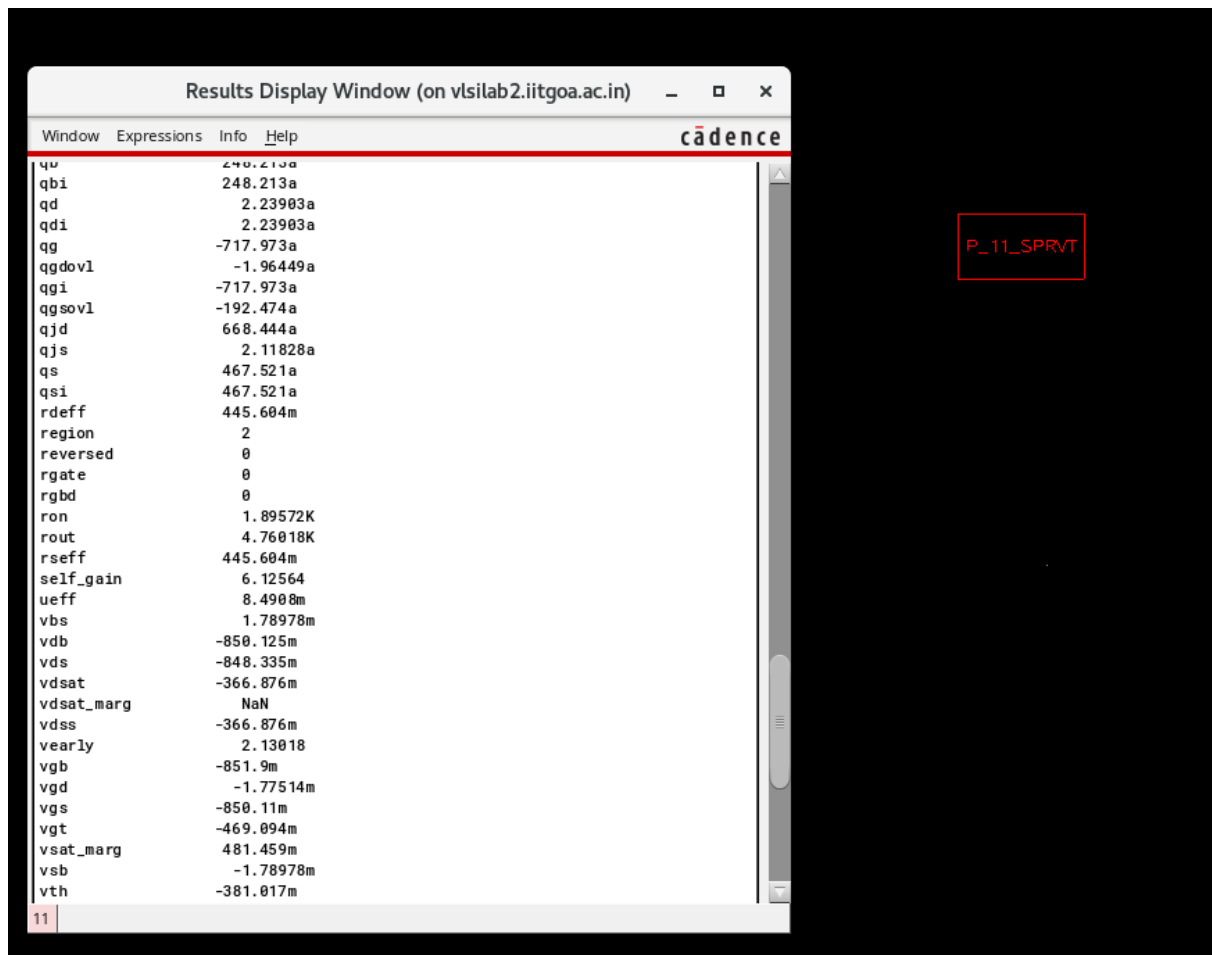
Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of operation which means “**Saturation region**”



The screenshot shows a Cadence Results Display Window titled "Results Display Window (on vlsilab2.iitgoa.ac.in)". The window contains a table of simulation results for the device N_11_SPRVT. The table lists various parameters and their values, including gate-source voltage (vgs), drain-source voltage (vds), and the operating region (region 2, indicating saturation).

Parameter	Value
qy	1.205031
qgdov1	185.491a
qgi	1.28563f
qgsolv1	406.884a
qjd	-971.516a
qjs	-1.98767a
qs	-686.035a
qsi	-686.035a
rdeff	143.725m
region	2
reversed	0
rgate	0
rgbd	0
ron	549.668
rout	1.26439K
rseff	143.725m
self_gain	5.80072
ueff	22.1858m
vbs	-412.051u
vdb	246.389m
vds	245.977m
vdsat	102.636m
vdsat_marg	NaN
vdss	102.636m
vearly	565.816m
vgb	449.73m
vgd	203.341m
vgs	449.318m
vgt	33.2818m
vsat_marg	143.341m
vsb	412.051u
vth	416.036m
vth_drive	NaN

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “**Saturation region**”



Observation: From the above analysis it's been verified that 2 transistors are in Saturation region of operation when **Vgs=450mV**.



Figure : Layout containing all the parasitic capacitances and resistances .

Finally choosing **420mv** as common mode voltage from all the above simulation data.

Difference in the large signal transfer characteristics between pre- and post-layout simulations:

* The main difference is that pre layout VTC has comparatively sharper transition than post layout VTC. It is mainly due to the additional parasitic effects included in the layout(i.e Schematic is quickly responding to changes in input). Also it is observed that when $v_{in} = 0.01v$ v_{out} (pre-layout)=930mV and v_{out} (post-layout)=900mV.

3. Connect a sinusoidal source at the input with an amplitude of 10 mV and a 500 fF capacitive load at the output. In all the following simulations, compare the results of pre- and post-layout simulations.

(a) Perform a post-layout DC operating point analysis to verify that the transistors are in saturation. You may not be able to print the operating point as you did in schematic simulations. You will have to decide the operating region using the terminal voltages.

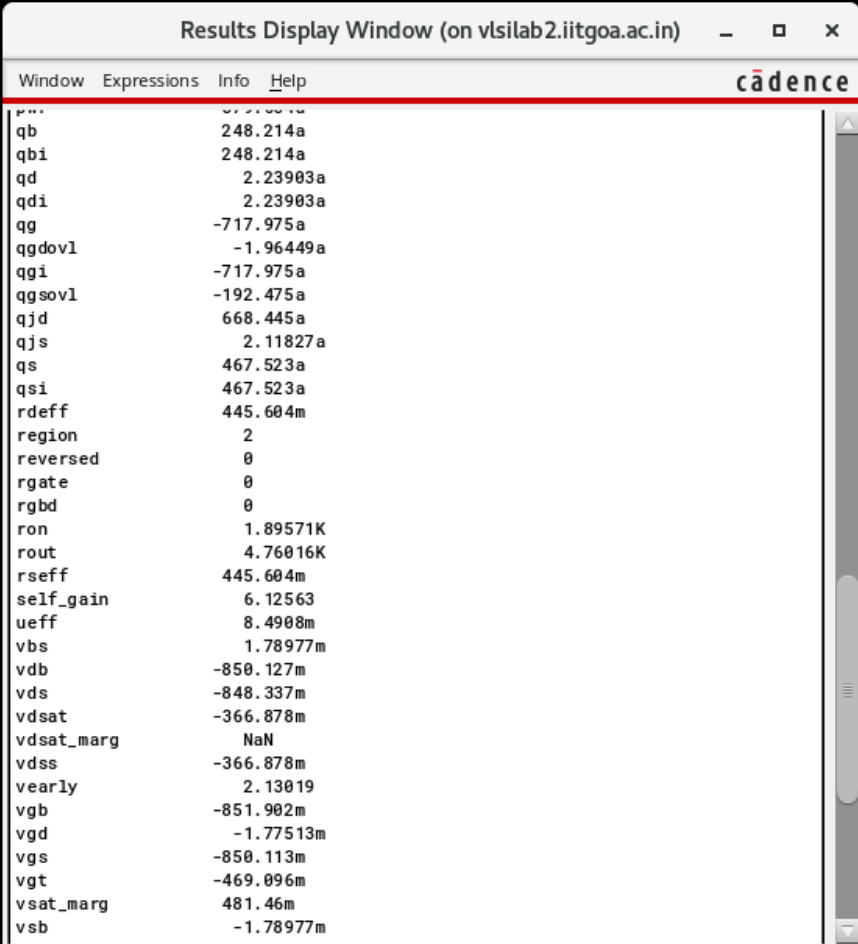
Have Chosen **Vdc as 450mV** , AC amp as 10mV and a 500fF capacitive load .

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means "Saturation region".

Results Display Window (on vlsilab2.iitgoa.ac.in)	
Window Expressions Info Help	cadence
qg	1.28563f
qgdovl	185.494a
qgi	1.28563f
qgsovl	406.884a
qjd	-971.507a
qjs	-1.98766a
qs	-686.034a
qsi	-686.034a
rdeff	143.725m
region	2
reversed	0
rgate	0
rgbd	0
ron	549.665
rout	1.26439K
rseff	143.725m
self_gain	5.80069
ueff	22.1858m
vbs	-412.049u
vdb	246.387m
vds	245.975m
vdsat	102.636m
vdsat_marg	NaN
vdss	102.636m
vearly	565.812m
vgb	449.73m
vgd	203.343m
vgs	449.318m
vgt	33.2816m
vsat_marg	143.339m
vsb	412.049u
vth	416.036m
vth_drive	NaN

7 HelpAction

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “**Saturation region**”.



Parameter	Value
qb	248.214a
qbi	248.214a
qd	2.23903a
qdi	2.23903a
qg	-717.975a
qgdovl	-1.96449a
qgi	-717.975a
qgsov1	-192.475a
qjd	668.445a
qjs	2.11827a
qs	467.523a
qsi	467.523a
rdeff	445.604m
region	2
reversed	0
rgate	0
rgbd	0
ron	1.89571K
rout	4.76016K
rseff	445.604m
self_gain	6.12563
ueff	8.4908m
vbs	1.78977m
vdb	-850.127m
vds	-848.337m
vdsat	-366.878m
vdsat_marg	NaN
vdss	-366.878m
vearly	2.13019
vgb	-851.902m
vgd	-1.77513m
vgs	-850.113m
vgt	-469.096m
vsat_marg	481.46m
vsb	-1.78977m

Observation: Verified that both M1 and M2 are in saturation region of operation when we have connected AC source .

Below are the transient analysis results:

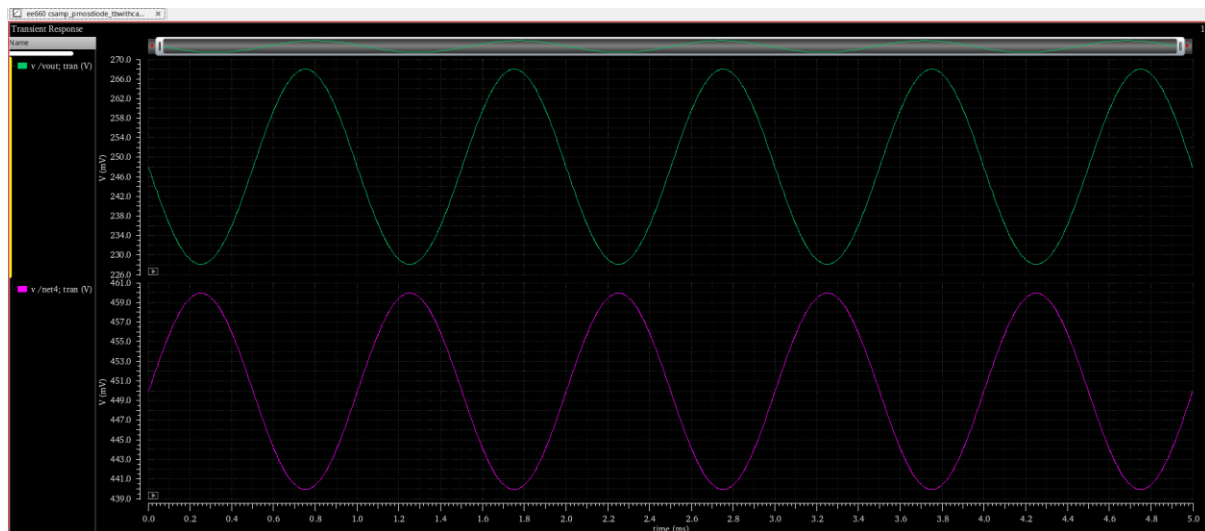


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis.

Observation: From the above transient analysis graphs it is observed that input and output waveforms are **out of phase**.

(c) Perform an AC analysis of the circuit. Plot the magnitude and phase responses. Note down the low frequency gain and 3 dB frequency of the circuit. Also, check what is the phase difference between the input and output at the 3 dB frequency.

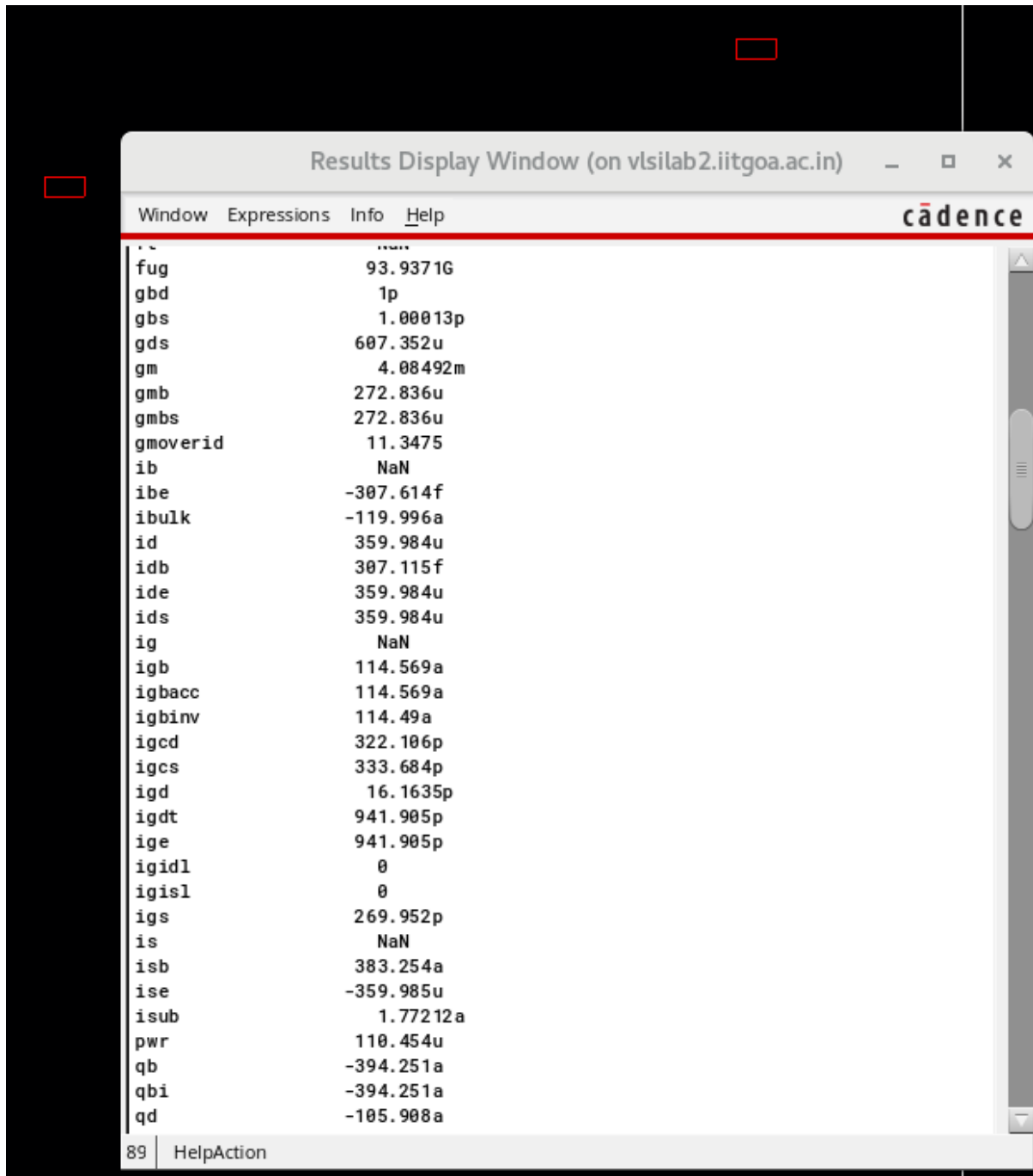


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plot we can say that :

- 1.Low frequency gain is **6.1071dB**
2. 3dB cutoff frequency is **609.576MHz**
- 3.Phase difference between the input and output at the 3 dB frequency: **133 Degrees**.

(d) Calculate the power dissipation of the circuit.



Window	Expressions	Info	Help
fug	93.9371G		
gbd	1p		
gbs	1.00013p		
gds	607.352u		
gm	4.08492m		
gmb	272.836u		
gmbs	272.836u		
gmoverid	11.3475		
ib	NaN		
ibe	-307.614f		
ibulk	-119.996a		
id	359.984u		
idb	307.115f		
ide	359.984u		
ids	359.984u		
ig	NaN		
igb	114.569a		
igbacc	114.569a		
igbinv	114.49a		
igcd	322.106p		
igcs	333.684p		
igd	16.1635p		
igdt	941.905p		
ige	941.905p		
igidl	0		
igisl	0		
igs	269.952p		
is	NaN		
isb	383.254a		
ise	-359.985u		
isub	1.77212a		
pwr	110.454u		
qb	-394.251a		
qbi	-394.251a		
qd	-105.908a		

Screenshot showing all the DC operating point values .

From the DC operating point analysis it is found that $id=359.98\mu A$

Power dissipation of the circuit = $Id * V_{dd} = 359.98\mu A * 1.1v = 0.395mW$

Difference in the large signal transfer characteristics between pre- and post-layout simulations:

a) At $V_{indc}=420\text{mV}$, $V_{in,ac}=10\text{mV}$, both pre and post layout dc operating point analysis have M1,M2 in saturation region of operation. But it is observed that V_{tn} and V_{tp} increased during post layout simulation.

For pre layout DC operating point analysis: $V_{tn}=408\text{mV}$, $|v_{tp}|=312\text{mV}$

For post layout DC operating point analysis: $V_{tn}=416\text{mV}$, $|v_{tp}|=381\text{mV}$

b) Transient Analysis simulation results are similar for pre and post-layout simulation.

c) AC Analysis simulation results comparison: Gain and 3 db cutoff frequency reduced in case of post -layout simulation.

For pre layout simulation:Low frequency gain is **6.57dB**,3dB cutoff frequency is **639.475MHz**

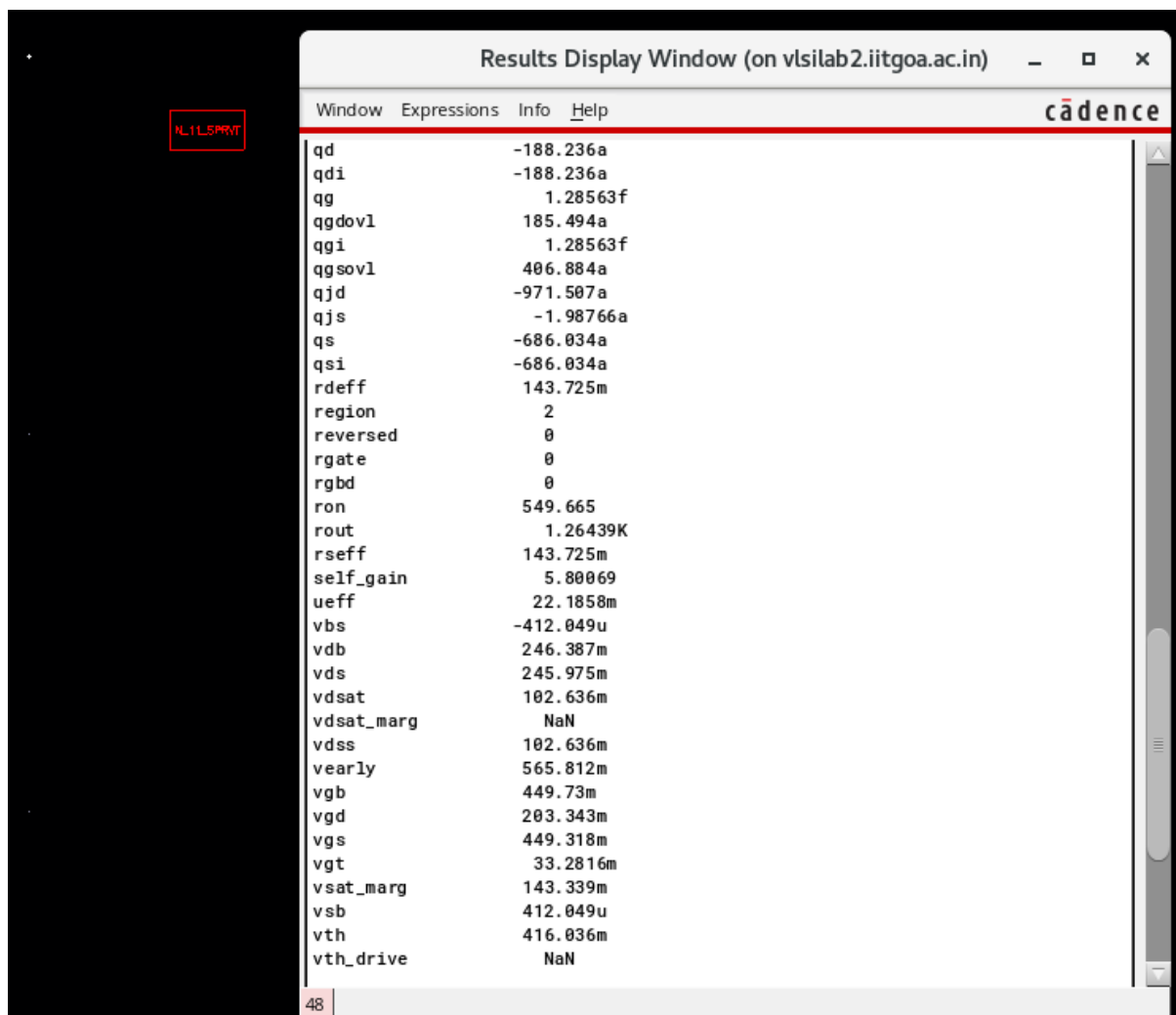
For post layout simulation:Low frequency gain is **6.1071dB**,3dB cutoff frequency is **609.576MHz**

d)Power Dissipation: Power dissipation in the circuit is slightly lesser in case of post-layout simulation. i.e **0.4763mW** for pre-layout and **0.395mW**

4. Repeat step 3 by changing the amplitude of the sinusoidal source to 200 mV. Do you see any differences between the results? If yes, justify your observations. Compare the results of pre- and post-layout simulations.

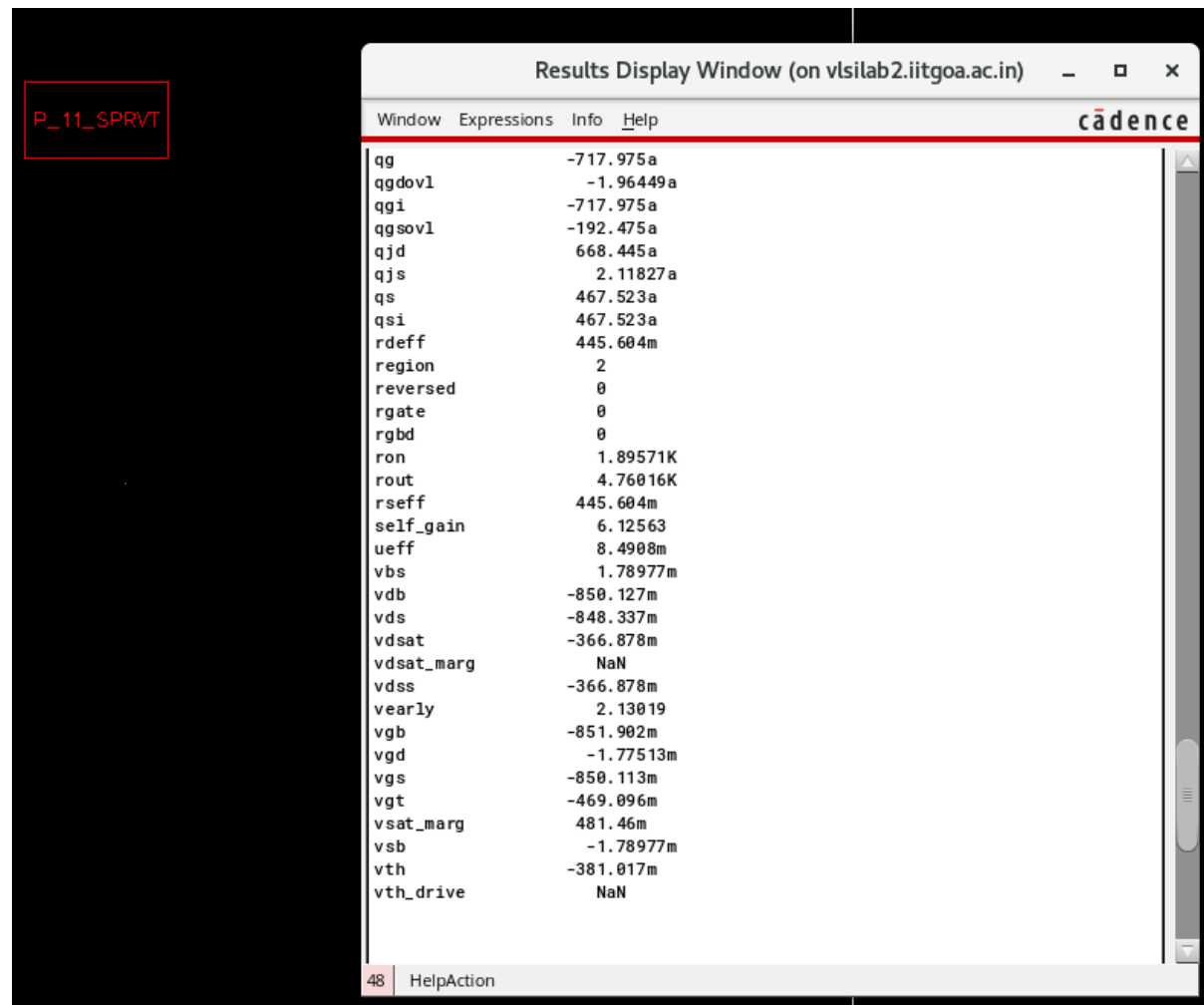
(a) Perform a post-layout DC operating point analysis to verify that the transistors are in saturation. You may not be able to print the operating point as you did in schematic simulations. You will have to decide the operating region using the terminal voltages.

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of operation which means “Saturation region”.



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cadence			
qd	-188.236a		
qdi	-188.236a		
qg	1.28563f		
qgdov1	185.494a		
qgi	1.28563f		
qgsov1	406.884a		
qjd	-971.507a		
qjs	-1.98766a		
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vdsat	102.636m		
vdsat_marg	NaN		
vdss	102.636m		
vearly	565.812m		
vgb	449.73m		
vgd	203.343m		
vgs	449.318m		
vgt	33.2816m		
vsat_marg	143.339m		
vsb	412.049u		
vth	416.036m		
vth_drive	NaN		

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “**Saturation region**”.



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qg	-717.975a
qgdov1	-1.96449a
qgi	-717.975a
qgsov1	-192.475a
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qjs	2.11827a
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vds	-848.337m
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vdsat_marg	NaN
vdss	-366.878m
vearly	2.13019
vgb	-851.902m
vgd	-1.77513m
vgs	-850.113m
vgt	-469.096m
vsat_marg	481.46m
vsb	-1.78977m
vth	-381.017m
vth_drive	NaN

Observation: From the above DC operating point analysis it's been verified that 2 transistors are in Saturation region of operation

(b) Perform a post-layout transient analysis of the circuit and verify that the input and output waveforms are out of phase.

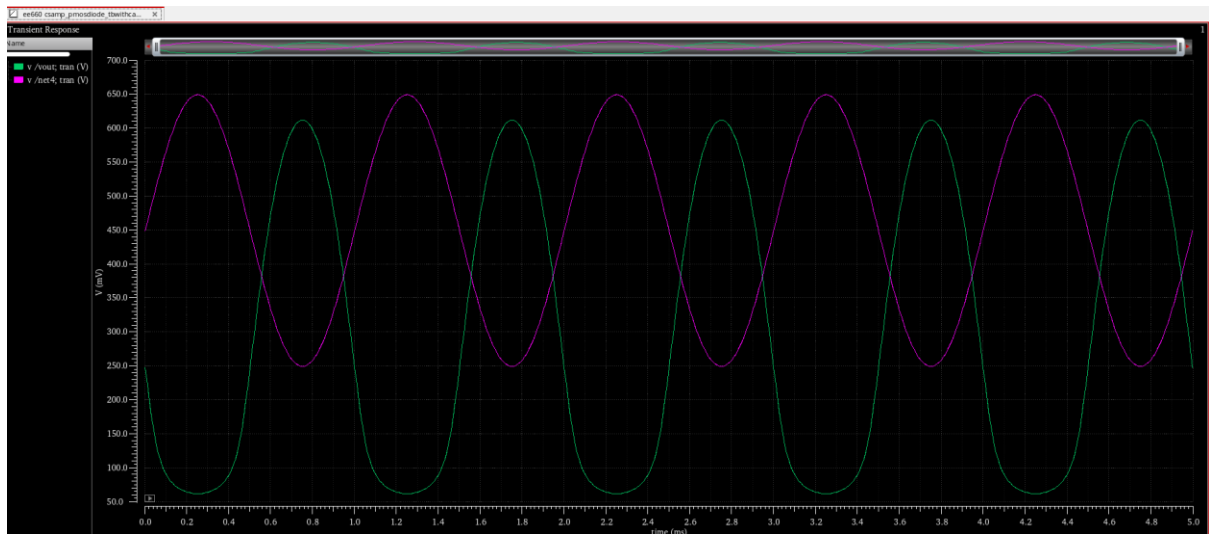


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

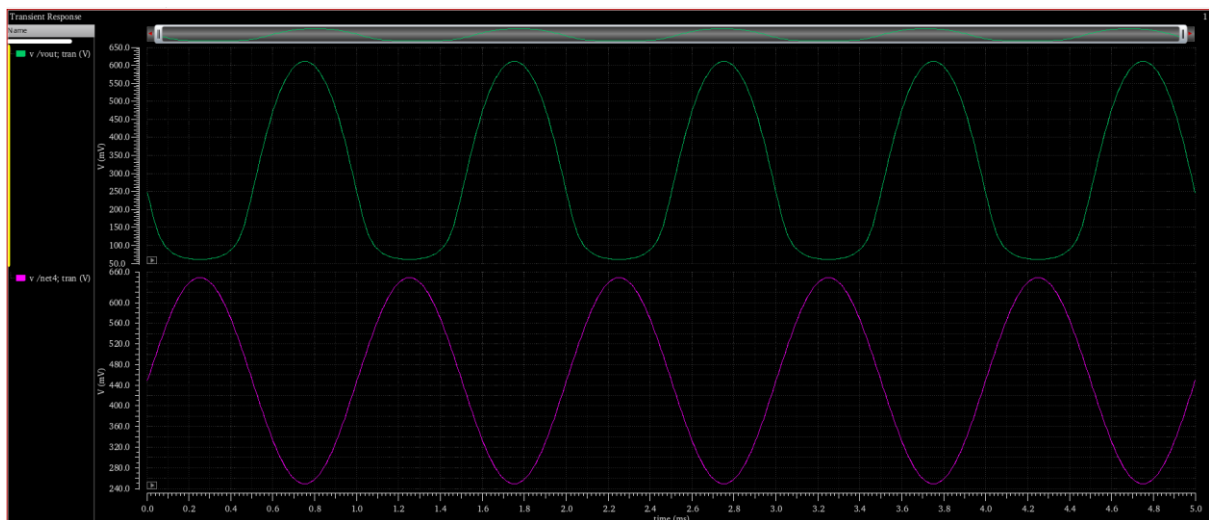


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

Observation: It is Observed that, after changing sinusoidal voltage to 200mV V_{out} waveform has been changed. This is mainly caused due to the clipping of output voltage caused due to the fact that M1 is in triode region since 0.2v is not in the range of saturation V_{in} . Hence , we could see that V_{out} got clipped. This is major change that has been observed when we have changed input of sinusoidal voltage to 0.2v

(c) Perform an AC analysis of the circuit. Plot the magnitude and phase responses. Note down the low frequency gain and 3 dB frequency of the circuit. Also, check what is the phase difference between the input and output at the 3 dB frequency.

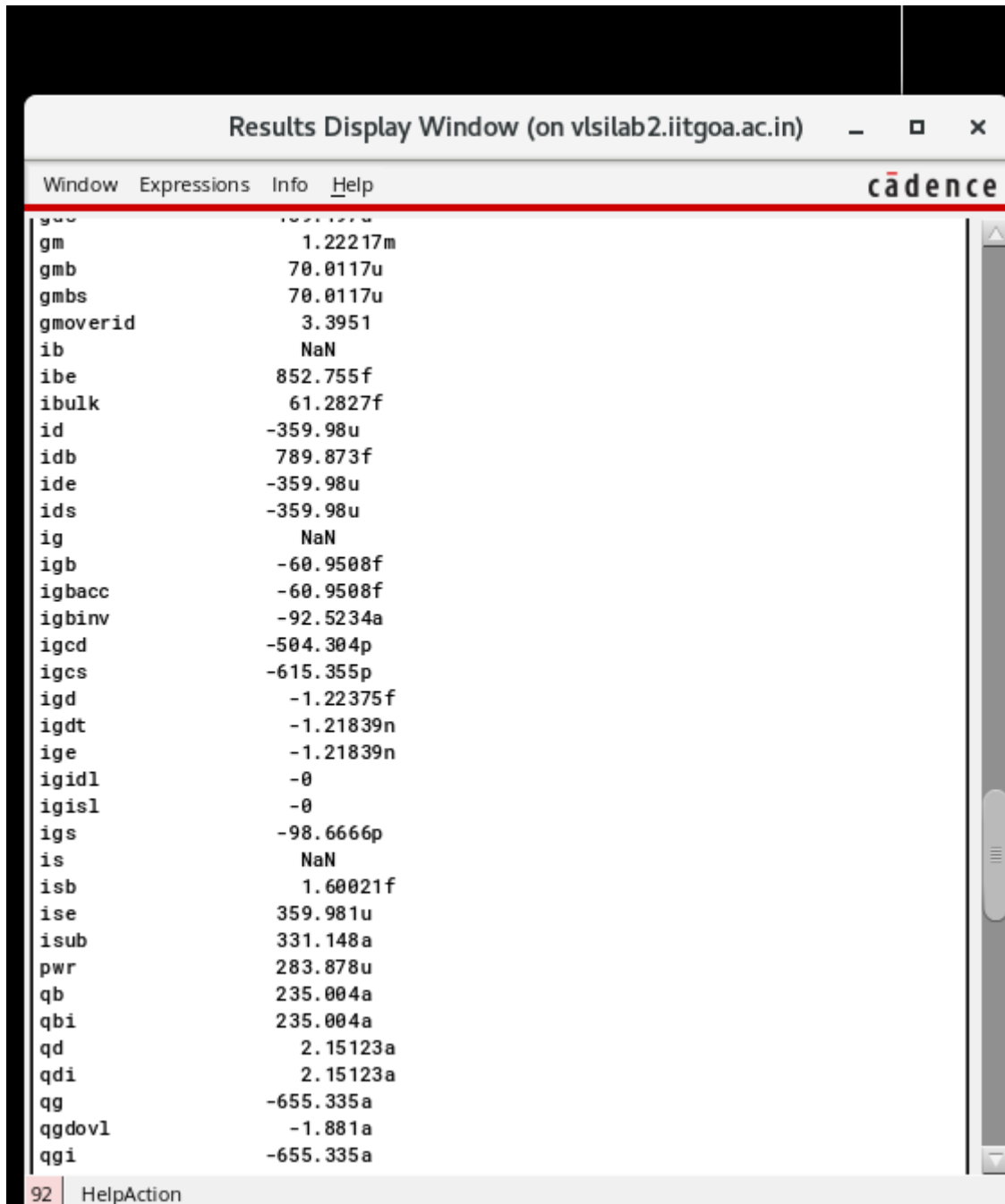


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plot we can say that :

- 1.Low frequency gain is **6.1071dB**
2. 3dB cutoff frequency is **609.576MHz**
- 3.Phase difference between the input and output at the 3 dB frequency: **133 Degrees.**

(d) Calculate the power dissipation of the circuit.



The screenshot shows a 'Results Display Window' from Cadence, titled 'Results Display Window (on vlsilab2.iitgoa.ac.in)'. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help', and a 'cadence' logo. The main area displays a list of circuit parameters and their values. The status bar at the bottom shows '92' and 'HelpAction'.

Parameter	Value
gm	1.22217m
gmb	70.0117u
gmbs	70.0117u
gmoverid	3.3951
ib	NaN
ibe	852.755f
ibulk	61.2827f
id	-359.98u
idb	789.873f
ide	-359.98u
ids	-359.98u
ig	NaN
igb	-60.9508f
igbacc	-60.9508f
igbinv	-92.5234a
igcd	-504.304p
igcs	-615.355p
igd	-1.22375f
igdt	-1.21839n
ige	-1.21839n
igidl	-0
igisl	-0
igs	-98.6666p
is	NaN
isb	1.60021f
ise	359.981u
isub	331.148a
pwr	283.878u
qb	235.004a
qbi	235.004a
qd	2.15123a
qdi	2.15123a
qg	-655.335a
qgdovl	-1.881a
qgi	-655.335a

From the DC operating point analysis it is found that $i_d = 359.98 \mu A$

Power dissipation of the circuit = $I_d \cdot V_{dd} = 359.98 \mu A \cdot 1.1V = 0.395mW$

Difference in the large signal transfer characteristics between pre- and post-layout simulations

a) At $V_{indc}=420\text{mV}$, $V_{in,ac}=200\text{mV}$ both pre and post layout dc operating point analysis have M1,M2 in saturation region of operation. But it is observed that V_{tn} and V_{tp} increased during post layout simulation.

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C) AC Analysis simulation results comparison: Gain and 3 db cutoff frequency reduced in case of post -layout simulation.

For pre layout simulation:Low frequency gain is **6.57dB**,3dB cutoff frequency is **639.475MHz**

For post layout simulation:Low frequency gain is **6.1071dB**,3dB cutoff frequency is **609.576MHz**

d)Power Dissipation: Power dissipation in the circuit is slightly lesser in case of post-layout simulation when compared with pre-layout simulation. i.e **0.4763mW** for pre-layout and **0.395mW** for post-layout simulation.