

EE 660 VLSI Design Laboratory

Assignment II

Submitted by: L.Sri Sai Swathi (2414202)

1. Design an NMOS common-source amplifier with a PMOS diode-connected load as shown in Fig. 1. The amplifier should have an absolute voltage gain of 3. You can make use of UMC65 models and choose the minimum device size as $2\text{ }\mu\text{m}/60\text{ nm}$. Create a symbol for the amplifier.

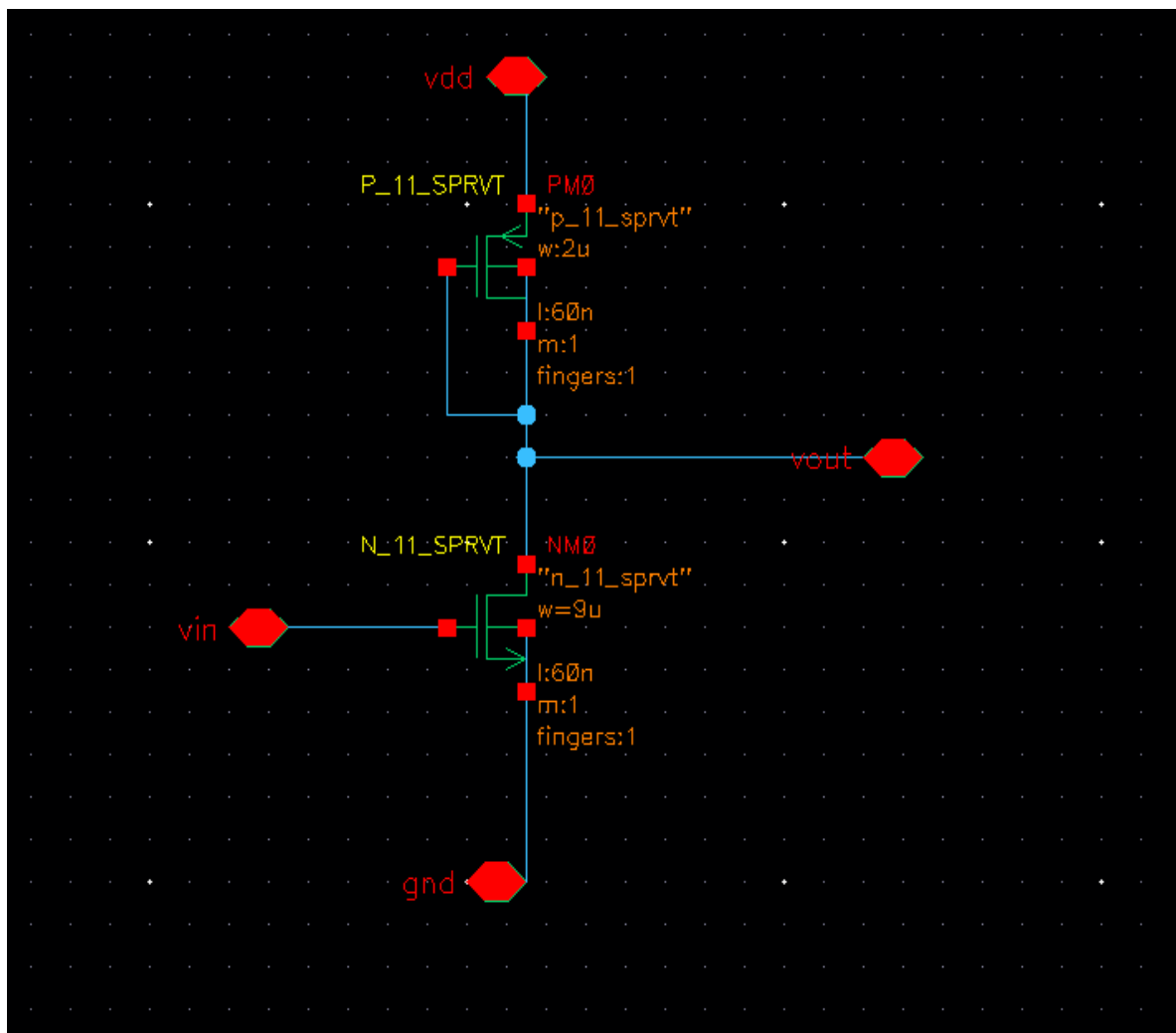
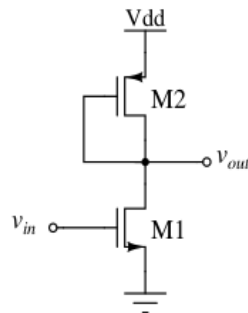


Figure : Schematic of CS Amplifier with PMOS diode connected load

2. Create a test bench and instantiate the amplifier in it. Do a large signal analysis of the circuit by doing a DC sweep of the input voltage from 0 to V_{DD} (1.1 V). Decide the input common-mode voltage at the centre of the region where both M1 and M2 are in saturation.

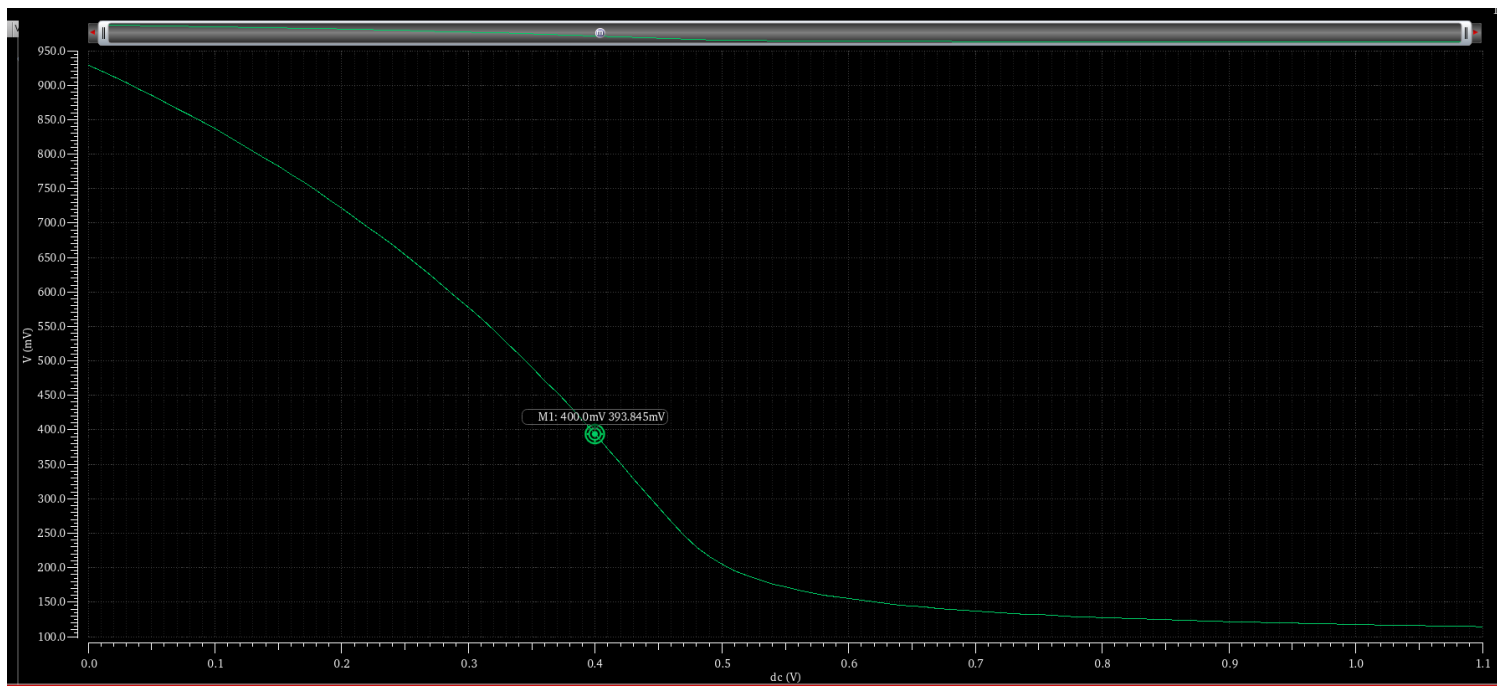


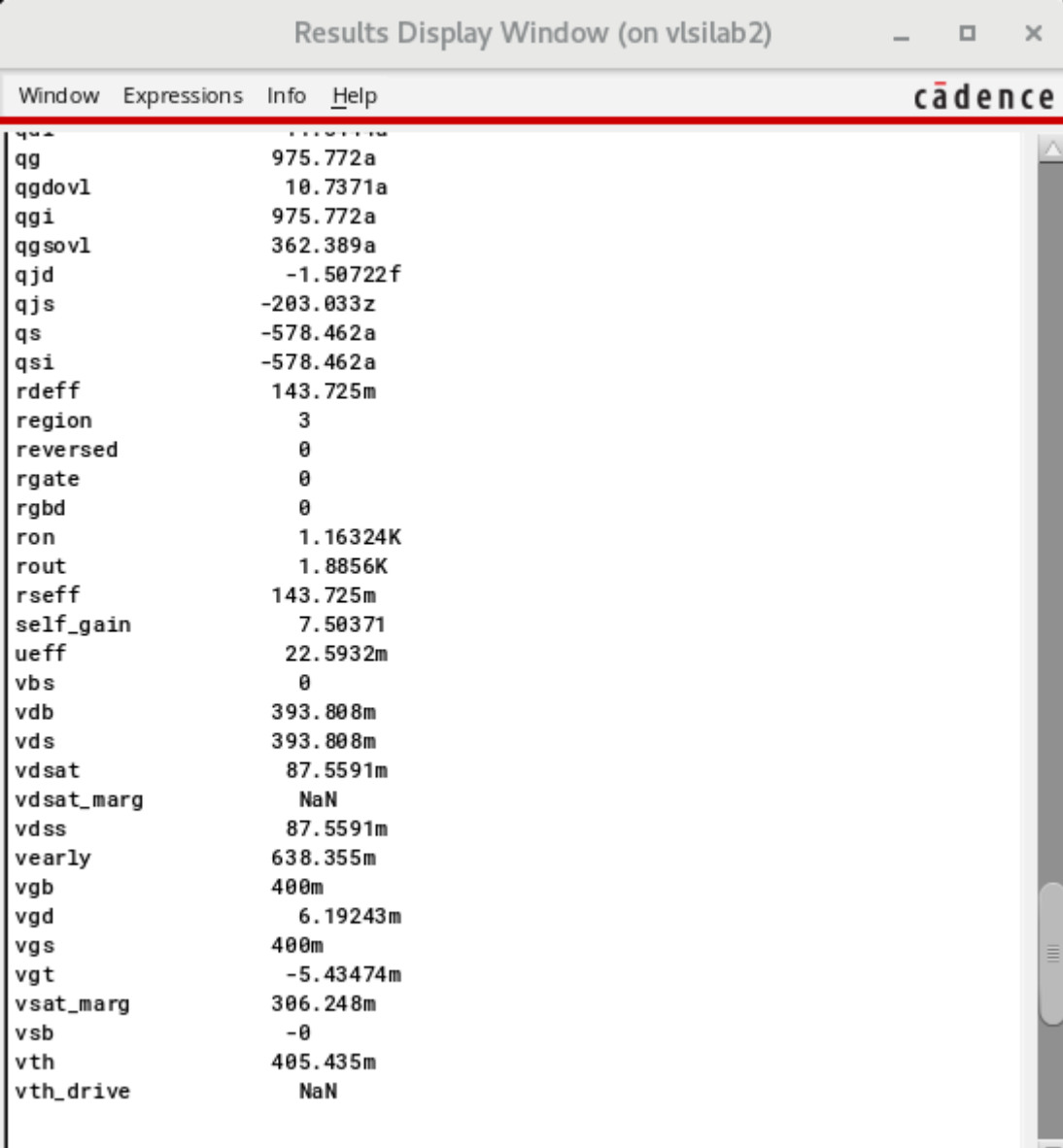
Figure: Plot showing V_{out} vs V_{in}

From the plot, Assumed 0.4V as common mode voltage and verified as follows:-

Below is the simulation result of DC operating point analysis. It shows that PMOS is in **region 2** of operation which means “Saturation region”. It is also noted that $|V_{tp}| = 0.315v$.

Results Display Window (on vlsilab2)	
Window	Expressions Info Help
qg	-568.01a
qgdovl	-1.57027a
qgi	-568.01a
qgsovl	-159.921a
qjd	-155.695z
qjs	-1.01949f
qs	395.644a
qsi	395.644a
rdeff	445.604m
region	2
reversed	0
rgate	0
rgbd	0
ron	2.08612K
rout	5.57364K
rseff	445.604m
self_gain	6.8021
ueff	9.63652m
vbs	-706.192m
vdb	0
vds	-706.192m
vdsat	-277.828m
vdsat_marg	NaN
vdss	-277.828m
vearly	1.88678
vgb	0
vgd	0
vgs	-706.192m
vgt	-391.062m
vsat_marg	428.364m
vsb	706.192m
vth	-315.13m
vth_drive	NaN

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 3 of operation which means “Cuttoff region”. It is also noted that $V_{tn} = 0.405V$.



Parameter	Value
qg	975.772a
qgdovl	10.7371a
qgi	975.772a
qgsovl	362.389a
qjd	-1.50722f
qjs	-203.033z
qs	-578.462a
qsi	-578.462a
rdeff	143.725m
region	3
reversed	0
rgate	0
rgbd	0
ron	1.16324K
rout	1.8856K
rseff	143.725m
self_gain	7.50371
ueff	22.5932m
vbs	0
vdb	393.808m
vds	393.808m
vdsat	87.5591m
vdsat_marg	NaN
vdss	87.5591m
vearly	638.355m
vgb	400m
vgd	6.19243m
vgs	400m
vgt	-5.43474m
vsat_marg	306.248m
vsb	-0
vth	405.435m
vth_drive	NaN

Observation : Since both transistors are not in saturation when we chose VGS as 400mV , we are choosing another value **420mV** which is greater than both **vtn** and **vtp**.

3. Connect a sinusoidal source at the input with an amplitude of 10 mV and a 500 fF capacitive load at the output.

(a) Perform a DC operating point analysis to verify that the transistors are in saturation.

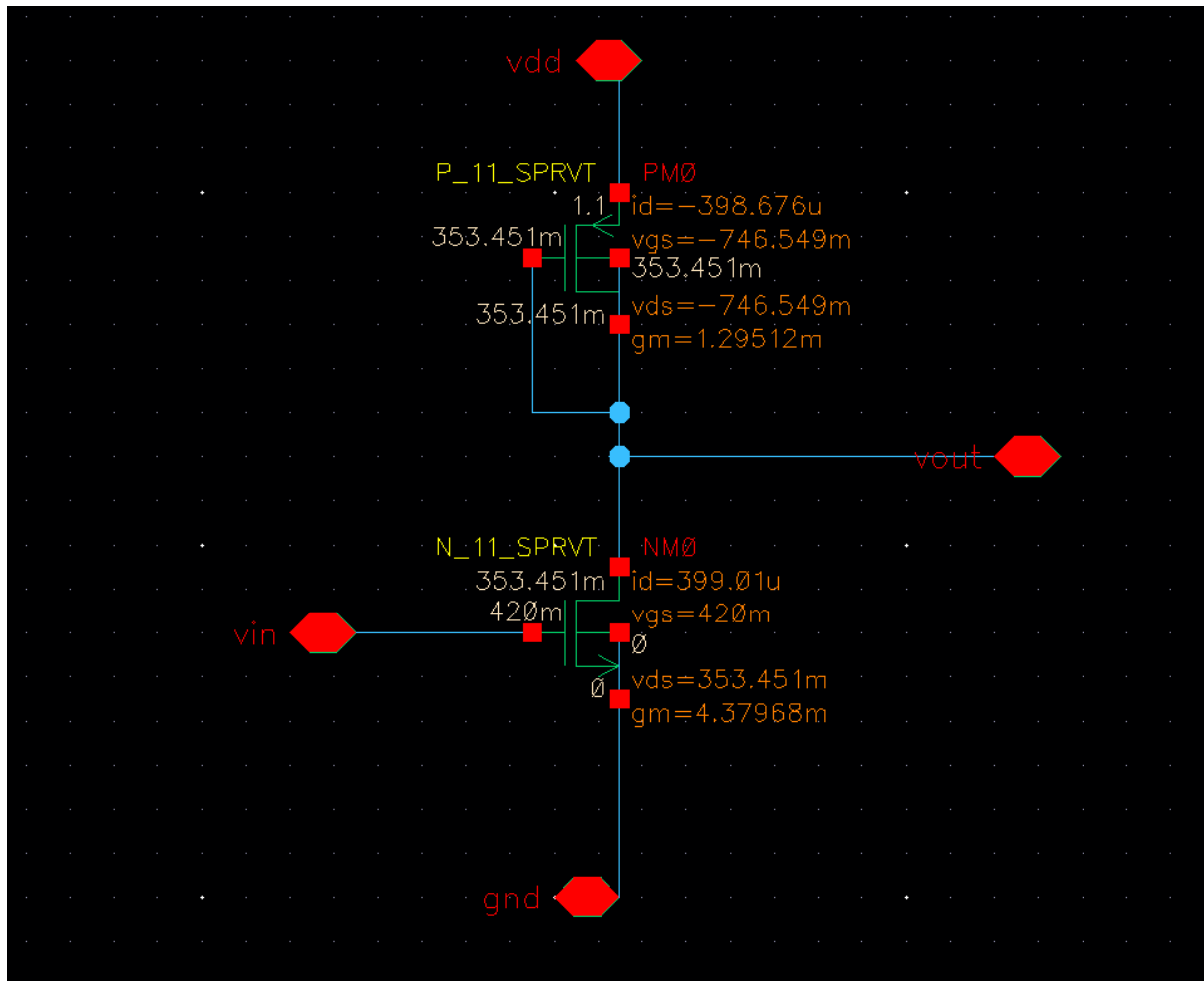
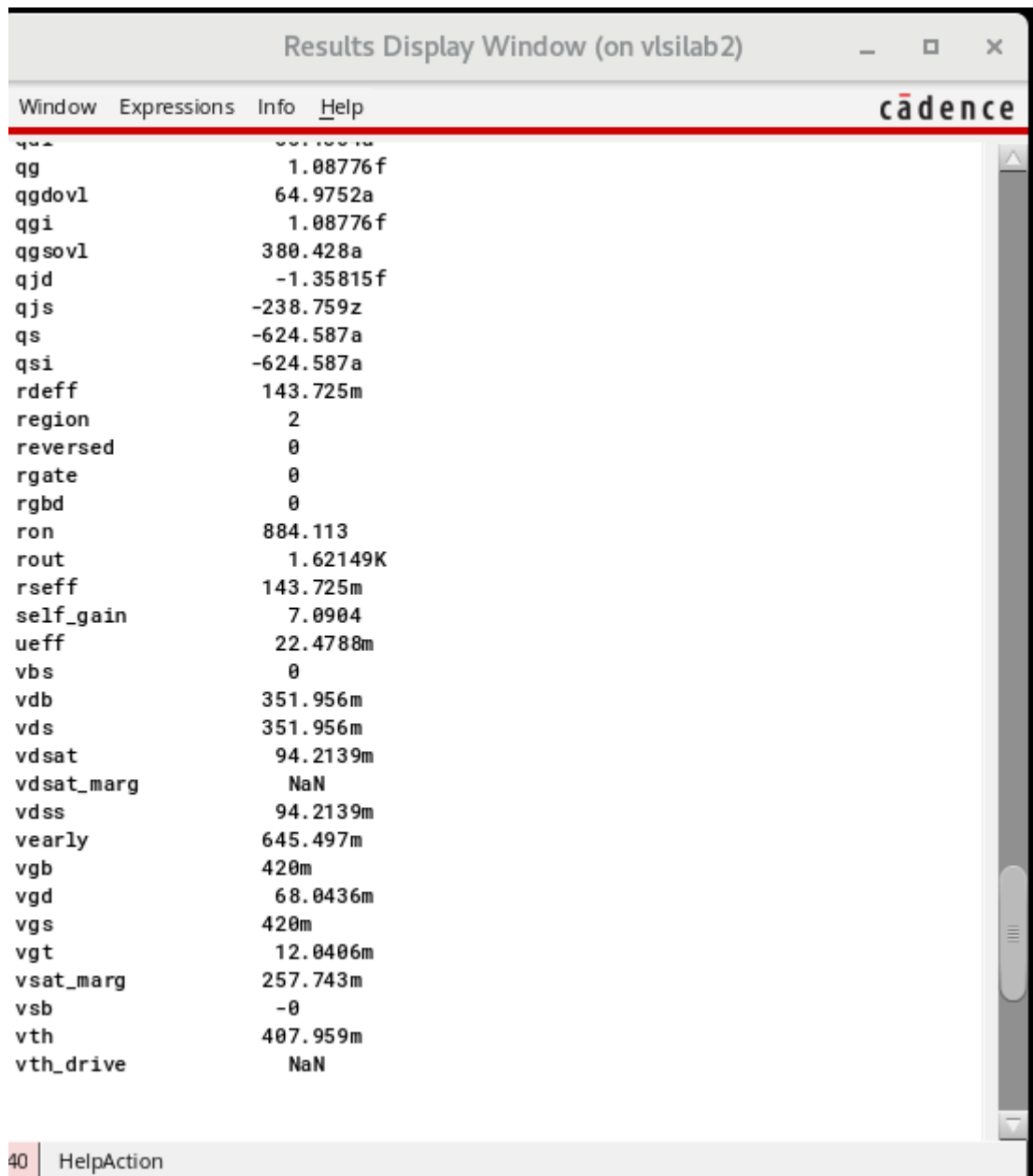


Figure: Schematic showing all the DC operating point voltages and currents

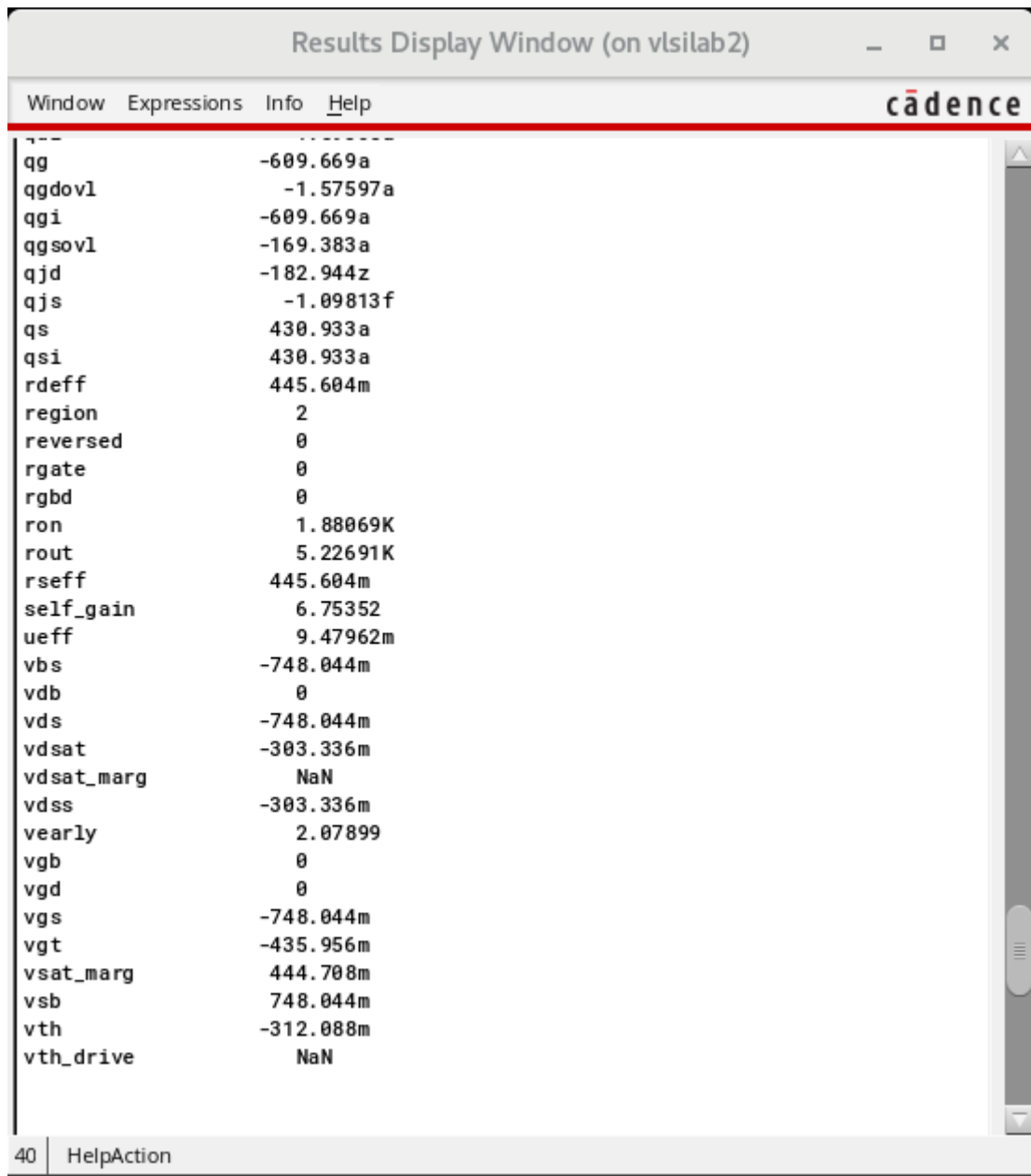
Below is the simulation result of DC operating point analysis. It shows that NMOS is in **region 2** of operation which means “Saturation region”.



Window	Expressions	Info	Help
qg		1.08776 f	
qgdovl		64.9752a	
qgi		1.08776 f	
qgsavl		380.428a	
qjd		-1.35815 f	
qjs		-238.759z	
qs		-624.587a	
qsi		-624.587a	
rdeff		143.725m	
region		2	
reversed		0	
rgate		0	
rgbd		0	
ron		884.113	
rout		1.62149K	
rseff		143.725m	
self_gain		7.0904	
ueff		22.4788m	
vbs		0	
vdb		351.956m	
vds		351.956m	
vdsat		94.2139m	
vdsat_marg		NaN	
vdss		94.2139m	
vearly		645.497m	
vgb		420m	
vgd		68.0436m	
vgs		420m	
vgt		12.0406m	
vsat_marg		257.743m	
vsb		-0	
vth		407.959m	
vth_drive		NaN	

40 | HelpAction

Below is the simulation result of DC operating point analysis. It shows that PMOS is in **region 2** of operation which means “Saturation region”.



Parameter	Value
qg	-609.669a
qgdovl	-1.57597a
qgi	-609.669a
qgsovl	-169.383a
qjd	-182.944z
qjs	-1.09813f
qs	430.933a
qsi	430.933a
rdeff	445.604m
region	2
reversed	0
rgate	0
rgbd	0
ron	1.88069K
rout	5.22691K
rseff	445.604m
self_gain	6.75352
ueff	9.47962m
vbs	-748.044m
vdb	0
vds	-748.044m
vdsat	-303.336m
vdsat_marg	NaN
vdss	-303.336m
vearly	2.07899
vgb	0
vgd	0
vgs	-748.044m
vgt	-435.956m
vsat_marg	444.708m
vsb	748.044m
vth	-312.088m
vth_drive	NaN

Observation: From the above analysis it's been verified that 2 transistors are in Saturation region of operation when $V_{gs}=420\text{mV}$.

b)Perform a transient analysis of the circuit and verify that the input and output waveforms are out of phase.

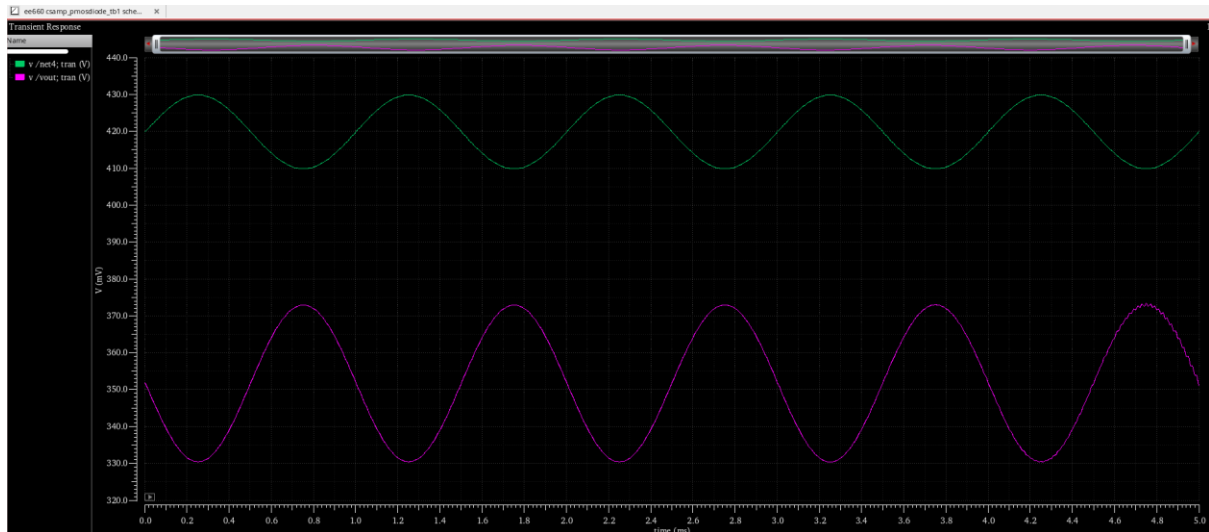


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

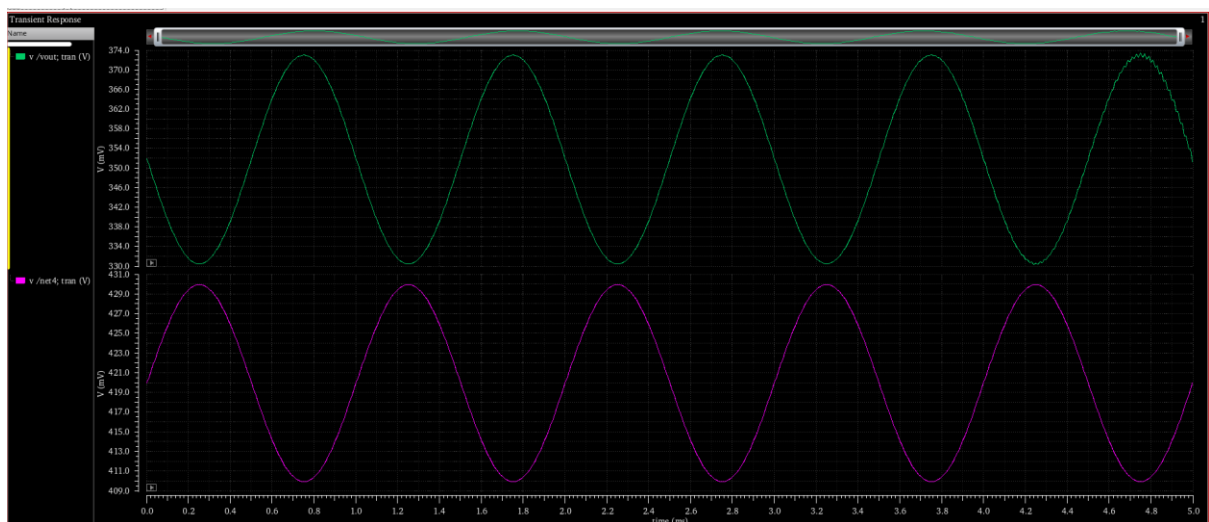


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

Observation: From the above transient analysis graphs it is observed that input and output waveforms are out of phase.

(c) Perform an AC analysis of the circuit. Plot the magnitude and phase responses. Note down the low frequency gain and 3 dB frequency of the circuit. Also, check what is the phase difference between the input and output at the 3 dB frequency.

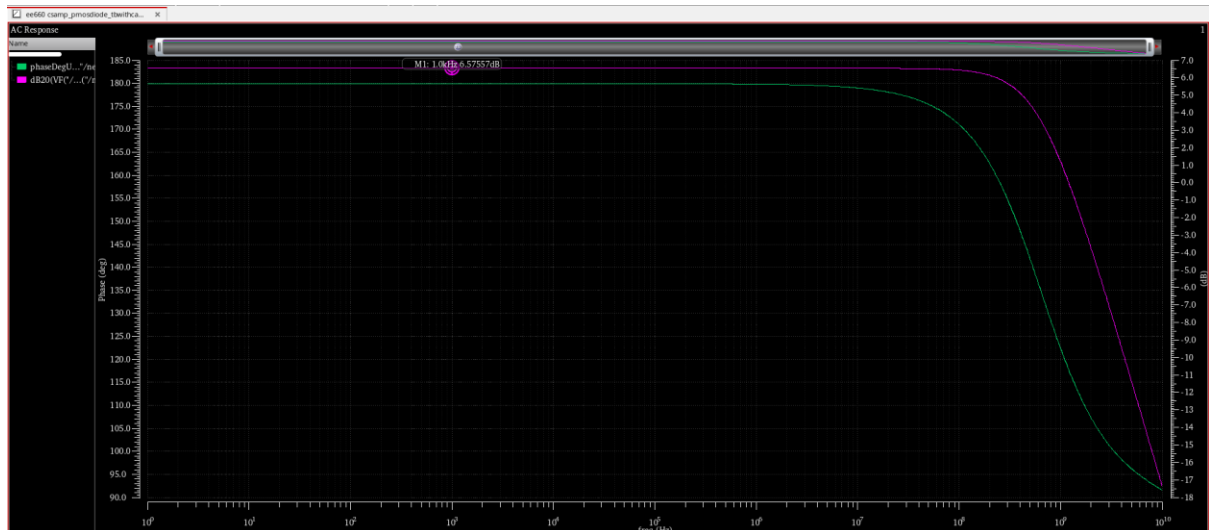


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.



Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations: From the above AC Analysis plots we can say that :

1. Low frequency gain is 6.57dB
2. 3dB cutoff frequency is 639.475MHz
3. Phase difference between the input and output at the 3 dB frequency: 134.94Degrees.

(d) Calculate the power dissipation of the circuit.

Power dissipation of the circuit $I_d * V_{dd} = 0.399\text{mA} * 1.1\text{V} = 0.4389\text{mW}$

4. Repeat step 3 by changing the amplitude of the sinusoidal source to 200 mV. Do you see any differences between the results? If yes, justify your observations.

a)DC operating point analysis Results:

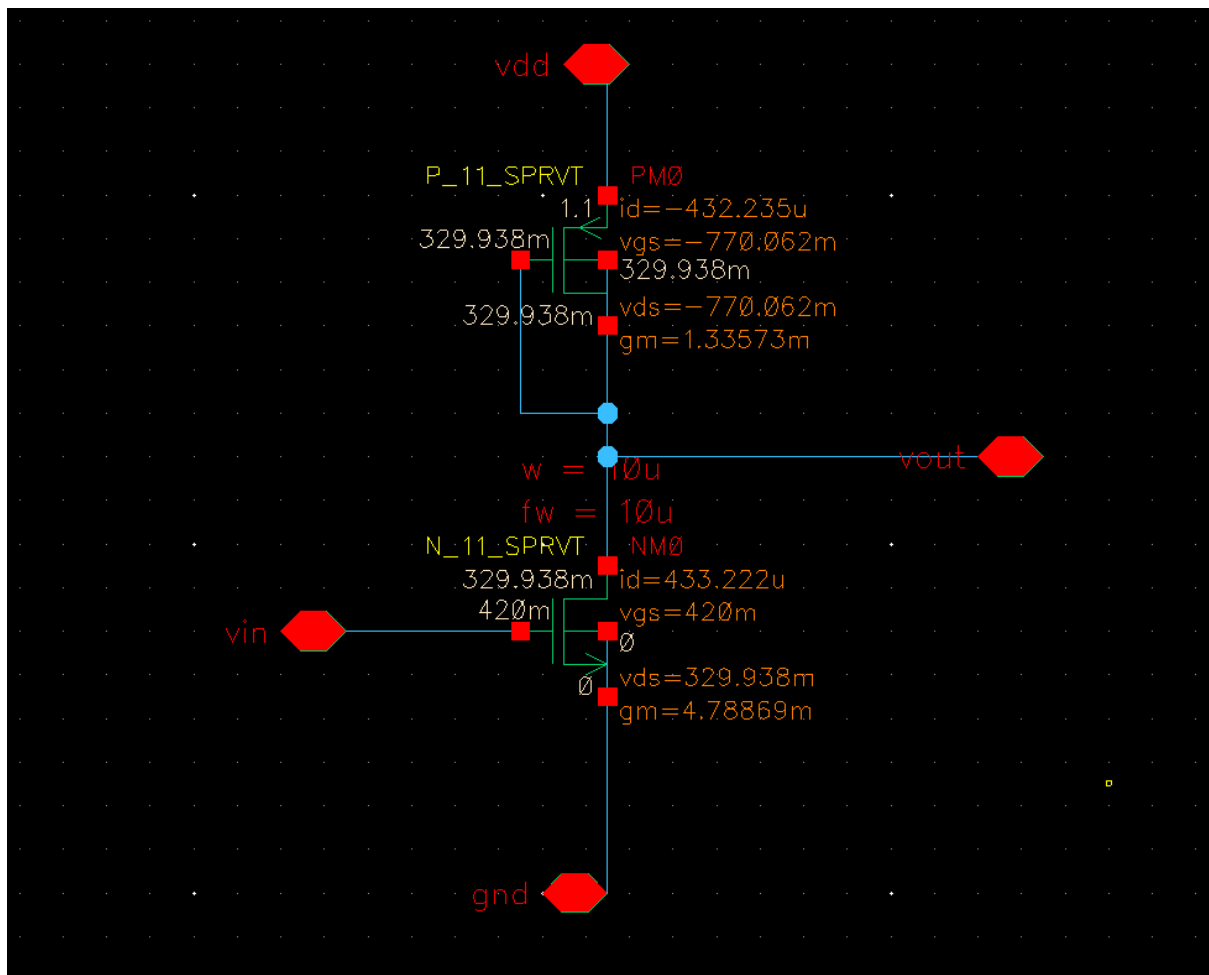


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Below is the simulation result of DC operating point analysis. It shows that NMOS is in **region 2** of operation which means “Saturation region”.

Results Display Window (on vlsilab2)	
Window Expressions Info Help	cadence
qdi	-66.1304a
qg	1.08776f
qgdovl	64.9752a
qgi	1.08776f
qgsovl	380.428a
qjd	-1.35815f
qjs	-238.759z
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qsi	-624.587a
rdeff	143.725m
region	2
reversed	0
rgate	0
rgbd	0
ron	884.113
rout	1.62149K
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self_gain	7.0904
ueff	22.4788m
vbs	0
vdb	351.956m
vds	351.956m
vdsat	94.2139m
vdsat_marg	NaN
vdss	94.2139m
vearly	645.497m
vgb	420m
vgd	68.0436m
vgs	420m
vgt	12.0406m
vsat_marg	257.743m
vsb	-0
vth	407.959m
vth_drive	NaN

75

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Results Display Window (on vlsilab2)	
Window	Expressions Info Help
cadence	
qbi	176.843a
qd	1.89308a
qdi	1.89308a
qg	-609.669a
qgdovl	-1.57597a
qgi	-609.669a
qgsavl	-169.383a
qjd	-182.944z
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vdsat_marg	NaN
vdss	-303.336m
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vgd	0
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Observation: From the above DC operating point analysis it's been verified that 2 transistors are in Saturation region of operation when $V_{gs}=420mV$.

b)Perform transient analysis of the circuit and verify that the input and output waveforms are out of phase.

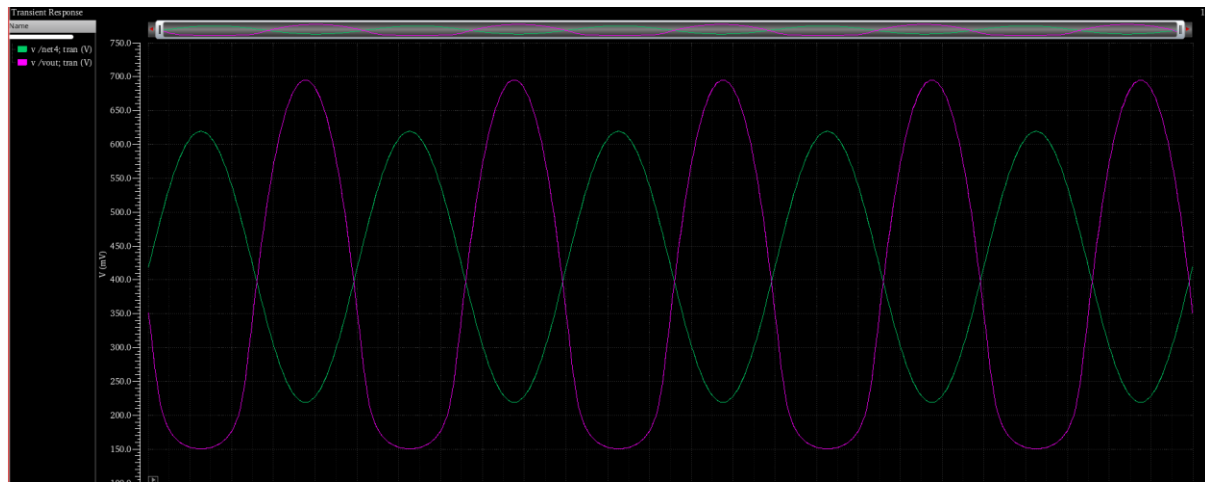


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

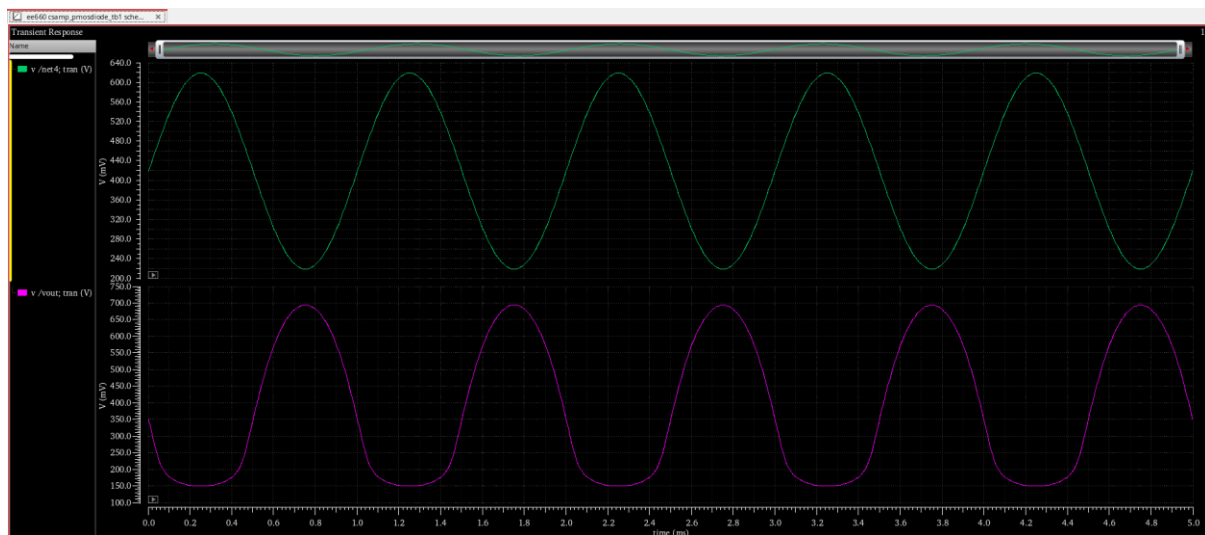


Figure: Plot showing V_{in} , V_{out} waveforms obtained from transient analysis .

Observation: It is Observed that, after changing sinusoidal voltage to 200mV V_{out} waveform has been changed. This is mainly caused due to the clipping of output voltage caused due to the fact that M1 is in triode region since 0.2v is not in the range of saturation V_{in} . Hence , we could see that V_{out} got clipped. This is major change that has been observed when we have changed input of sinusoidal voltage to 0.2v

c) Perform AC analysis of the circuit. Plot the magnitude and phase responses.

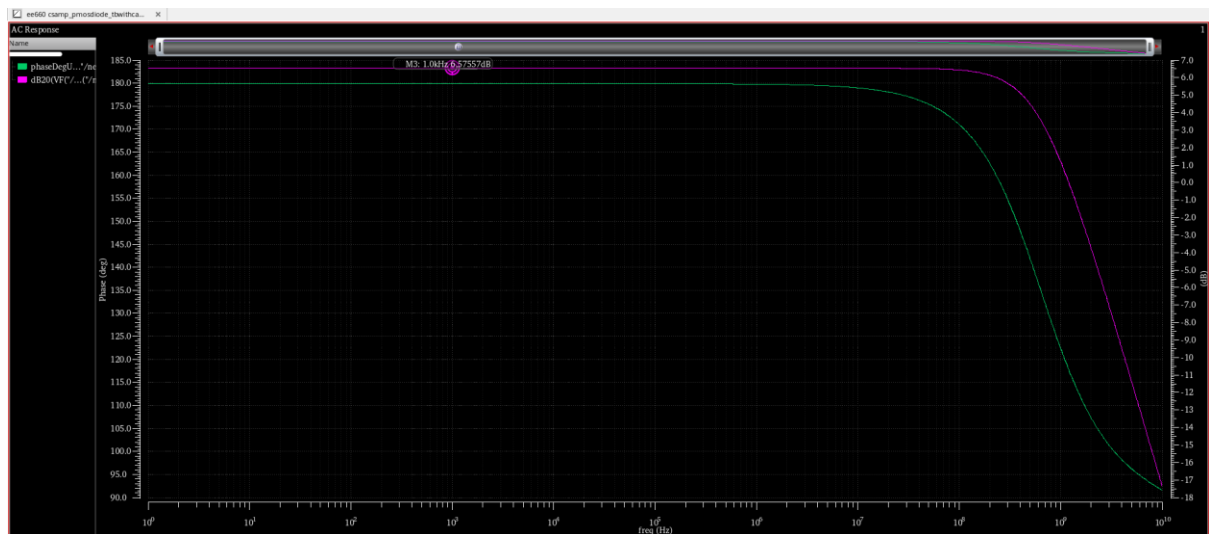


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

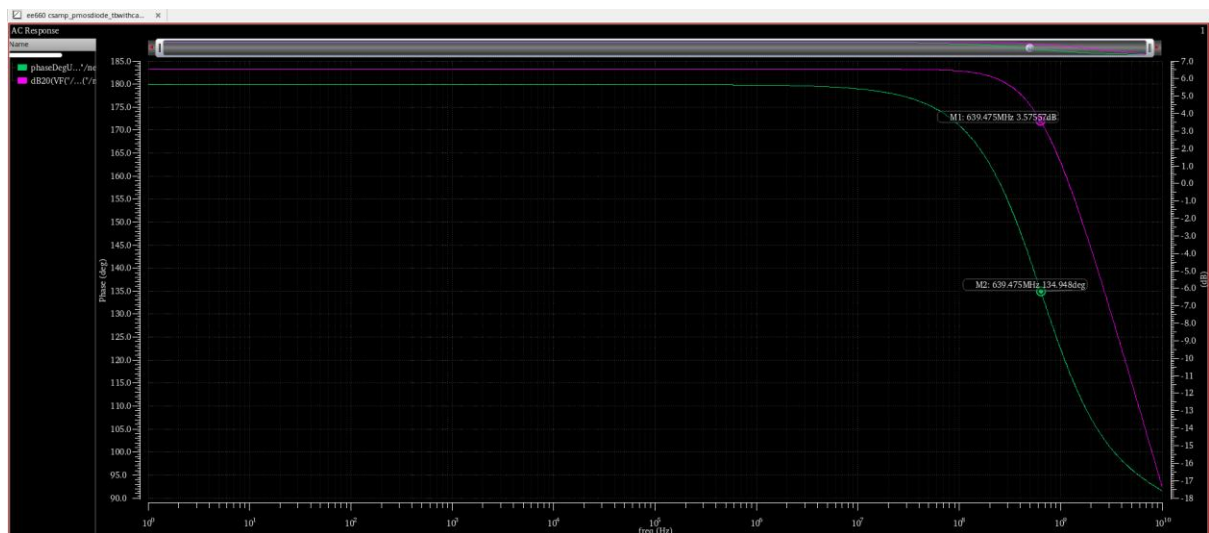


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Observations: From the above Ac Analysis plots we can say that :

1. Low frequency gain is 6.57dB
2. 3dB cutoff frequency is 639.475MHz
3. Phase difference between the input and output at the 3 dB frequency: 134.94Degrees.

(d) Calculate the power dissipation of the circuit.

$$\text{Power dissipation of the circuit } I_d * V_{dd} = 0.433\text{mA} * 1.1\text{v} = 0.4763\text{mW}$$

5. Mostly, you would have got a low-frequency gain that is different from the designed value in step 3. Could you change the dimensions of M1 or M2 to get a gain of 3?

Yes, we have got gain less than designed value. To get a gain of 3 (i.e. A_v in dB = 9.54dB) below modifications are made to the dimensions of M1 and M2

Initially tried reducing width of M2 from 2 μ m to 80nm (least possible). Below is the magnitude and phase plot:



Figure : Plot showing Magnitude and frequency response

Observed gain = -8.98dB

Now increased width of M1 to 10 μ m (max possible for this technology). Below is the magnitude and phase plot:



Figure : Plot showing Magnitude and frequency response

Observed gain = 6.95dB

Since this technology offers maximum width to be 10um , tried placing nmos transistors in parallel .yet maximum gain attained is 6.35 when 3 transistors are used.

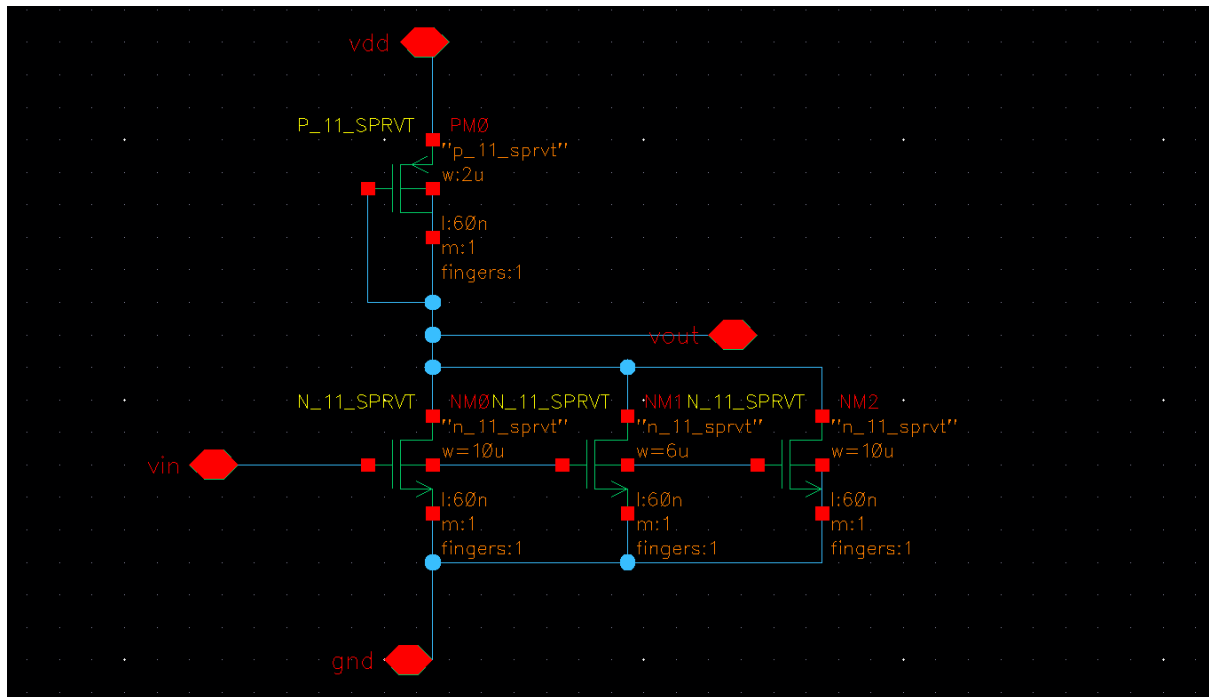


Figure: Schematic showing cs amplifier with 3 nmos transistors in parallel.

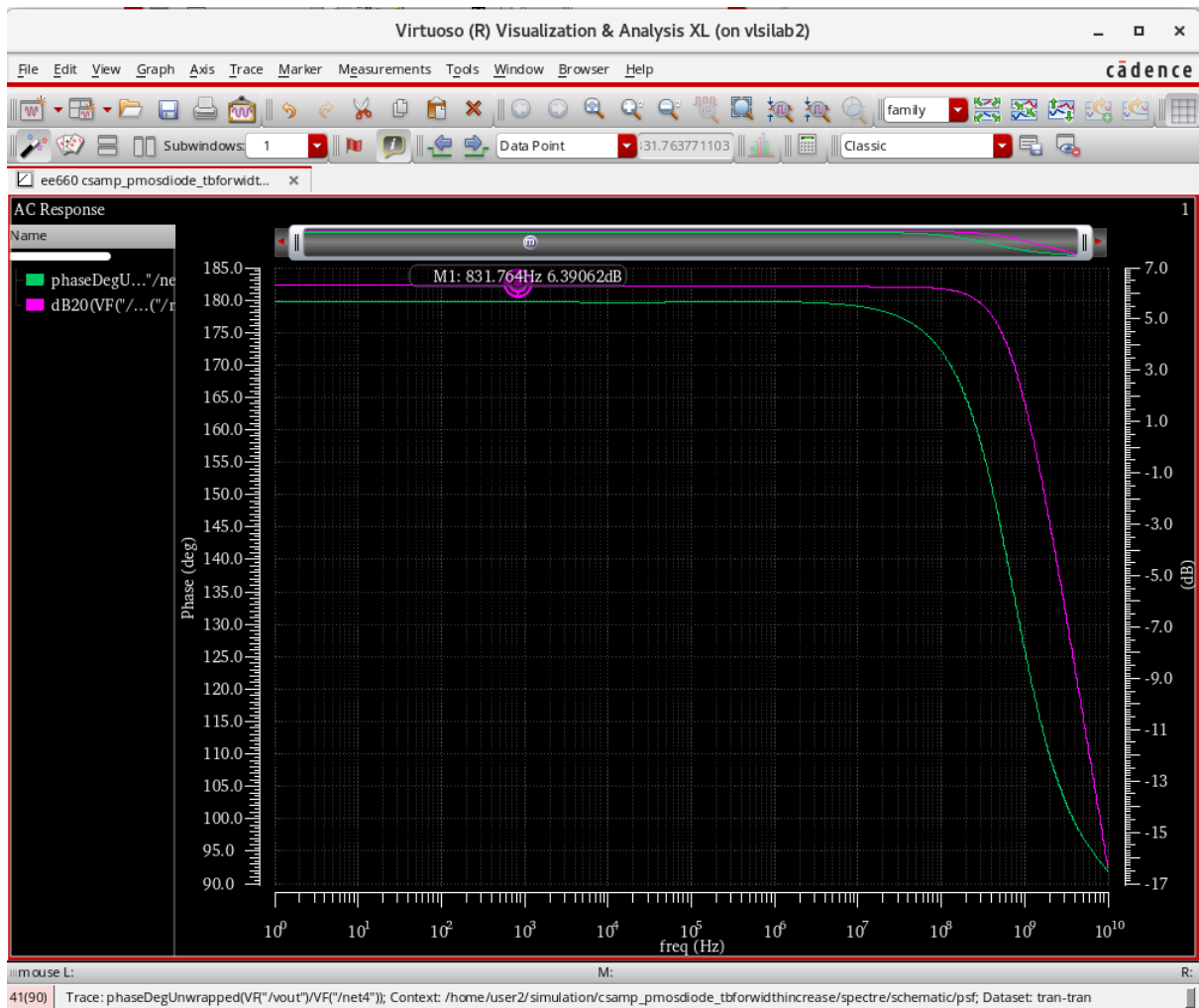


Figure: Plot showing Frequency and magnitude response.

Observed gain is 6.39dB