EE 660 VLSI Design Laboratory

Assignment V

Submitted by: L Sri Sai Swathi (2414202)

1. Design and simulate a CMOS inverter, the circuit diagram of which is given below using UMC 65 nm technology. You have to choose the minimum size NMOS and PMOS devices such that the switching threshold is V DD /2.

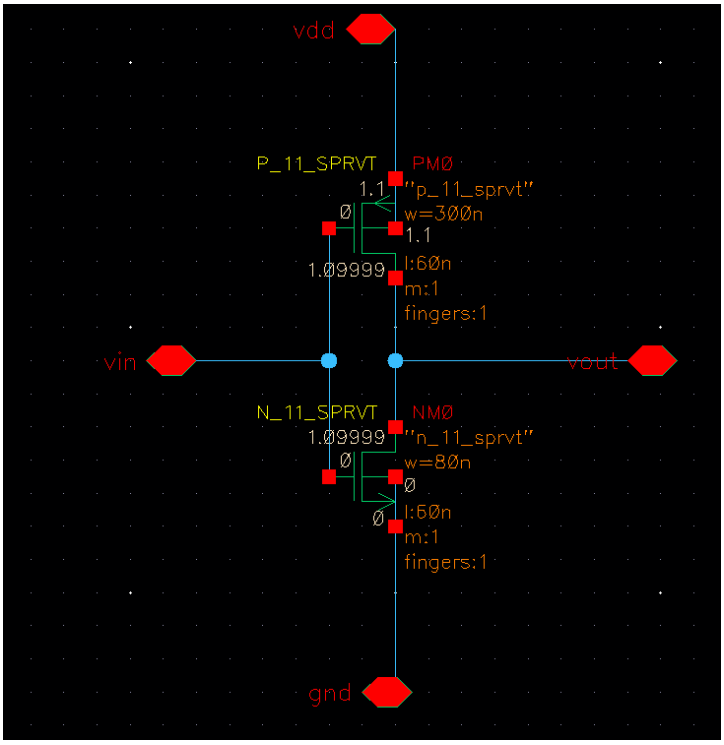


Figure : Schematic of CMOS inverter using 65 nm technology

It is given that VM should be VDD/2 . Also ,nmos has to be of minimum size . Choosing wn to be 80nm which is the minimum possible size in 65nm technology that's been used.

For VM=VDD/2 ; (wn/wp)= (up/un) .

We get wp= 200nm. Hence starting analysis with wp =200nm ,wn=80nm.

Performed DC analysis for CMOS inverter(***wn=80nm,wp=200nm***) schematic circuit with VDD =1.1v ,sweeped input from 0 to 1.1v in steps of 0.01v. Below are the simulation results and observations:

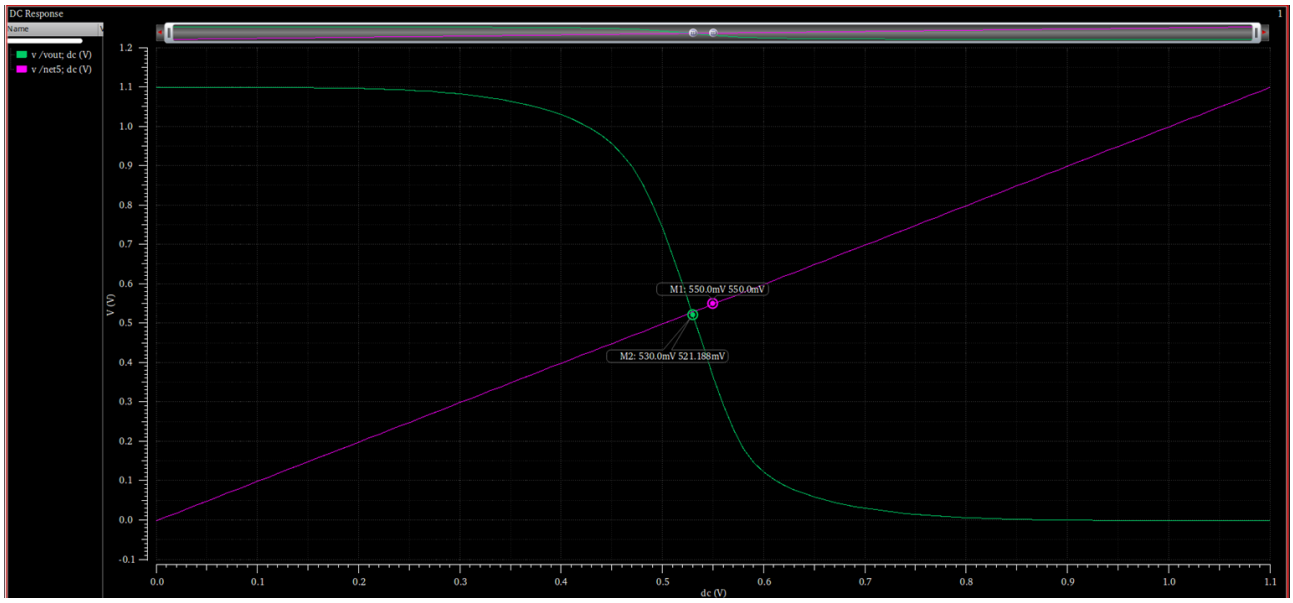


Figure :Plot showing Voltage Transfer Characteristics of CMOS inverter

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as **0.53mv**. Since it is not VDD/2 (i.e 0.55V), increasing wp to 250nm.

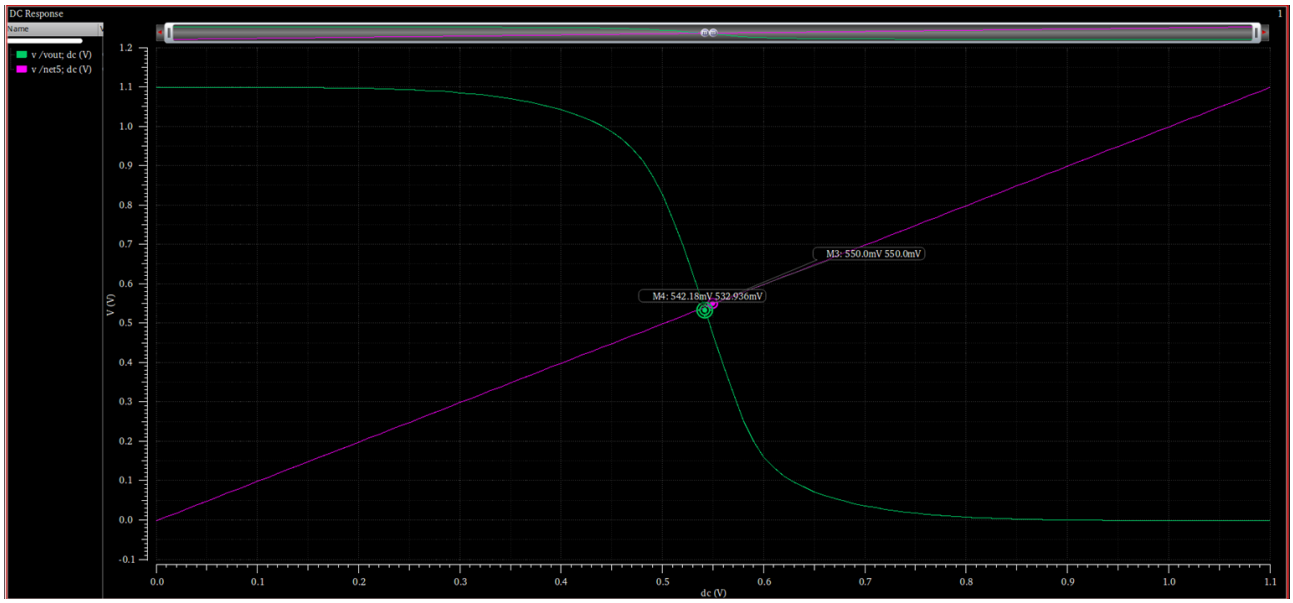


Figure: Plot showing Voltage Transfer Characteristics of CMOS inverter(when wp=250mv)

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as **0.542mv**. Since it is not VDD/2 (i.e 0.55V), increasing wp to 300nm.

Performed DC analysis for CMOS inverter(***wn=80nm,wp=300nm***) schematic circuit with VDD =1.1v ,sweeped input from 0 to 1.1v in steps of 0.01v. Below are the simulation results and observations:

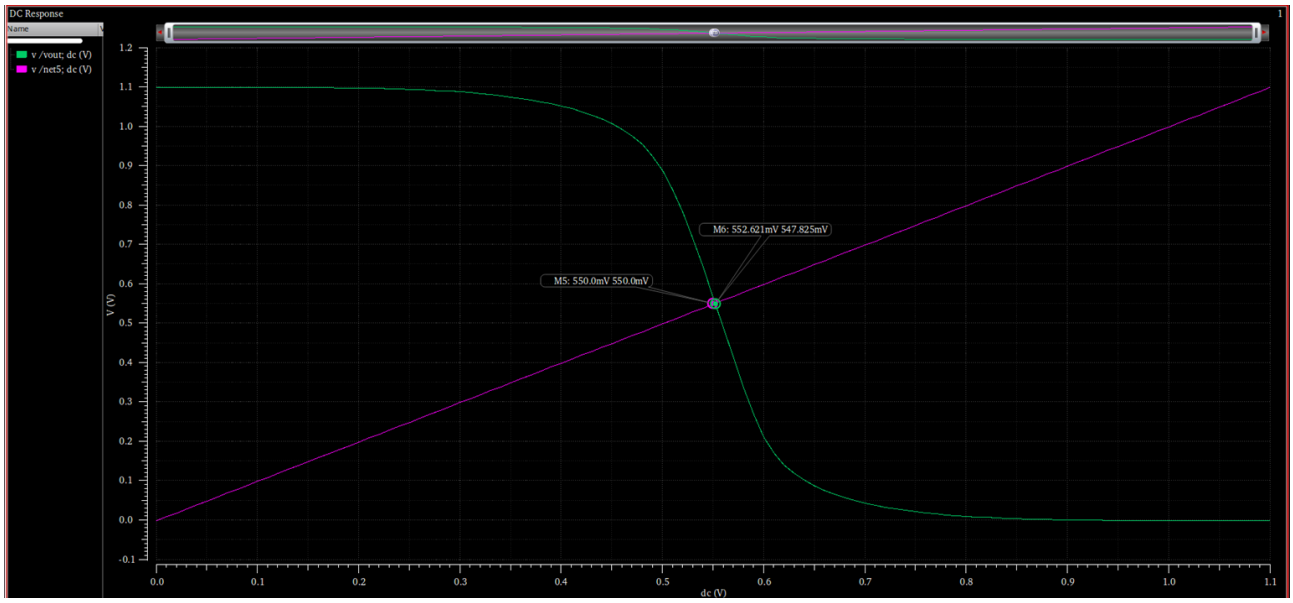


Figure: Plot showing Voltage Transfer Characteristics of CMOS inverter

Observation: From the Simulated Voltage transfer characteristics, Switching threshold is identified as **0.552mV.**

b) Using the VTC calculate the values of the switching threshold and noise margins.

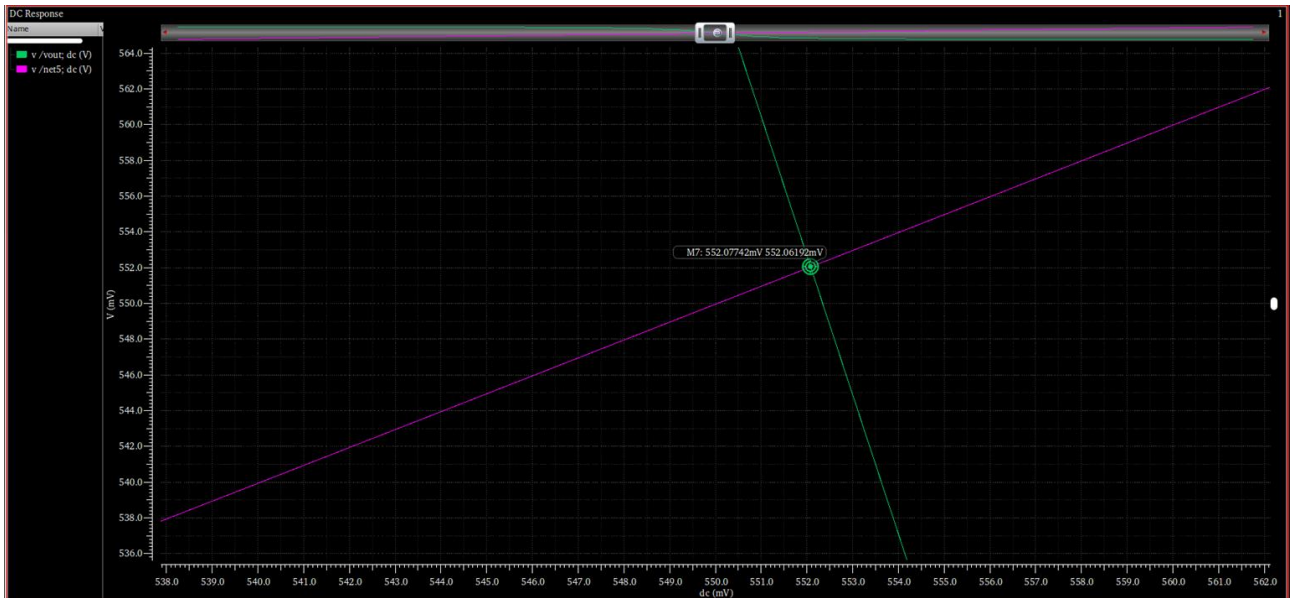


Figure: Plot showing Voltage Transfer Characteristics of CMOS inverter

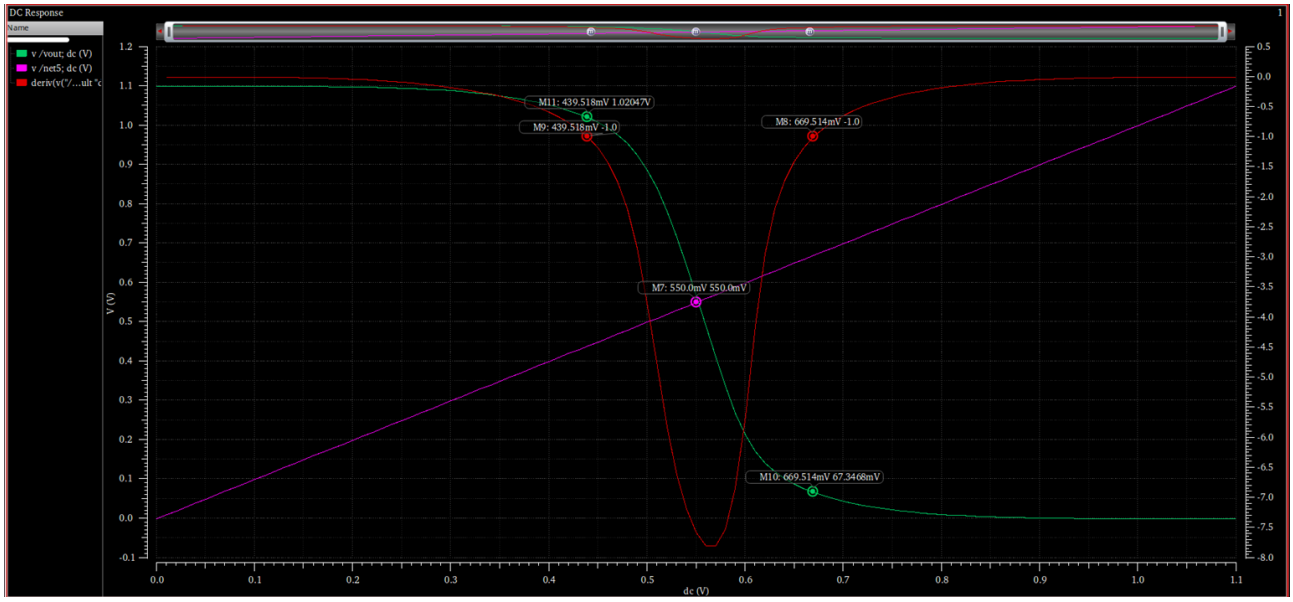


Figure : Plot showing Voltage Gain of CMOS inverter

From the Plot shown above :

VIL=439.518mV ,VIH= 669.514mV
VOH=1.0204V, VOL=67.346mV

NOISE MARGINS:

NMH =VOH-VIH = **0.35V**
NML = VIL-VOL = **0.37V**

(c) From the VTC estimate the gain of the inverter at V M and calculate the noise margins using the piecewise linear approximation of VTC.

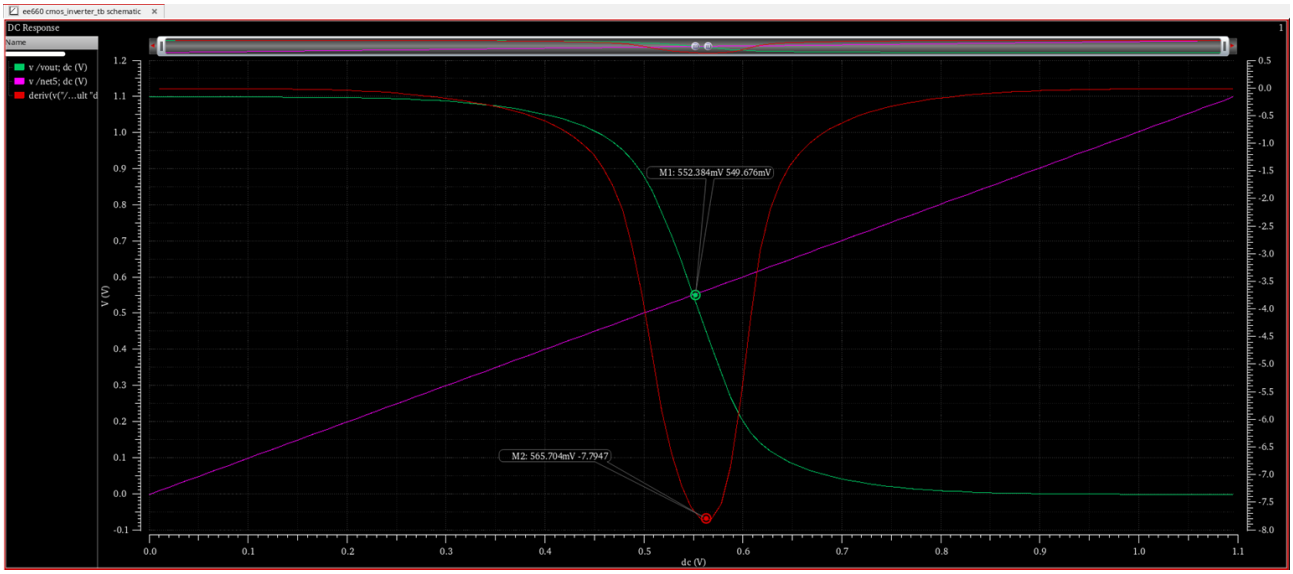


Figure : Plot showing piecewise linear approximation of VTC

From the plot :

Gain(g) =-7.79
Vm=0.552V

Noise Margins Calculation using piecewise linear approximation :

$$V_{IL} = V_M - \frac{(V_M - V_{DD})}{g}$$

$$V_{IH} = V_M - (\frac{V_M}{g})$$

$$NM_H = V_{DD} - V_{IH}$$

$$NM_L = V_{IL}$$

NM_H=1.029V
NM_L=0.4816V

(d) Calculate the values of t pLH and t pHL by doing a schematic transient simulation of the inverter driving a copy of it.

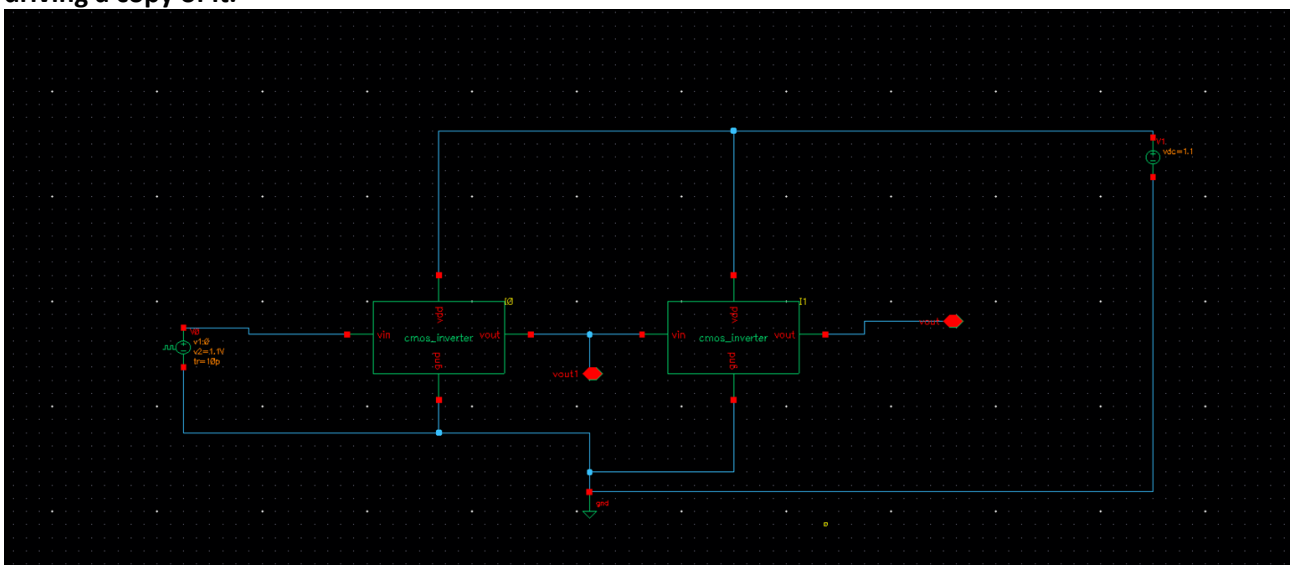


Figure: Schematic of CMOS cascaded inverter pair

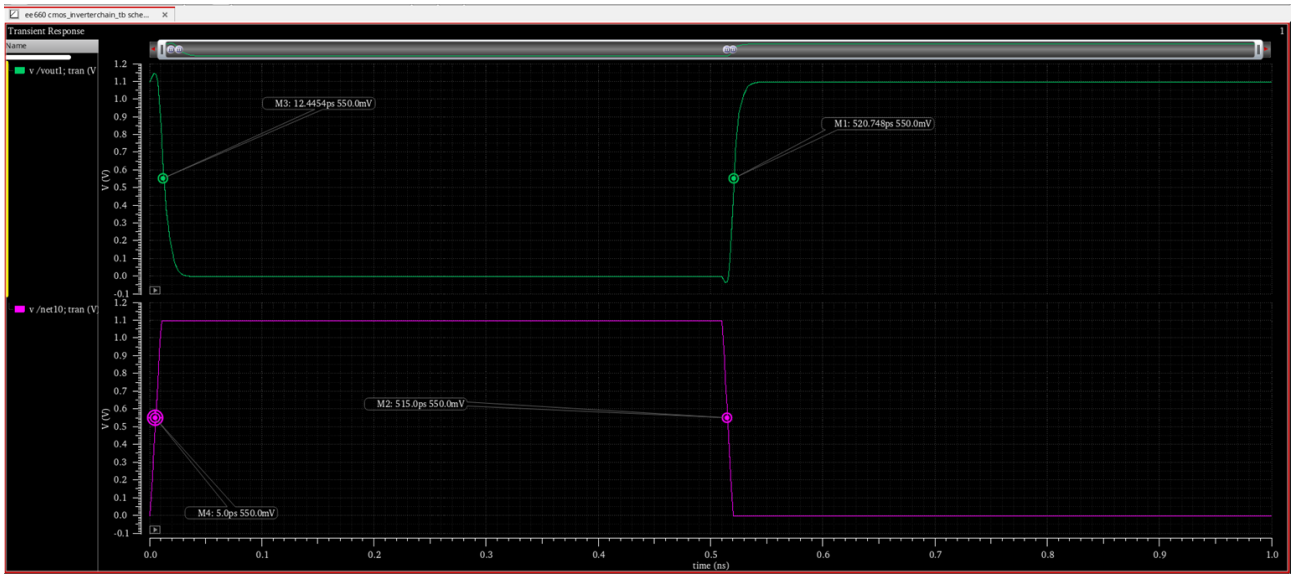


Figure : Simulated transient response of the inverter.

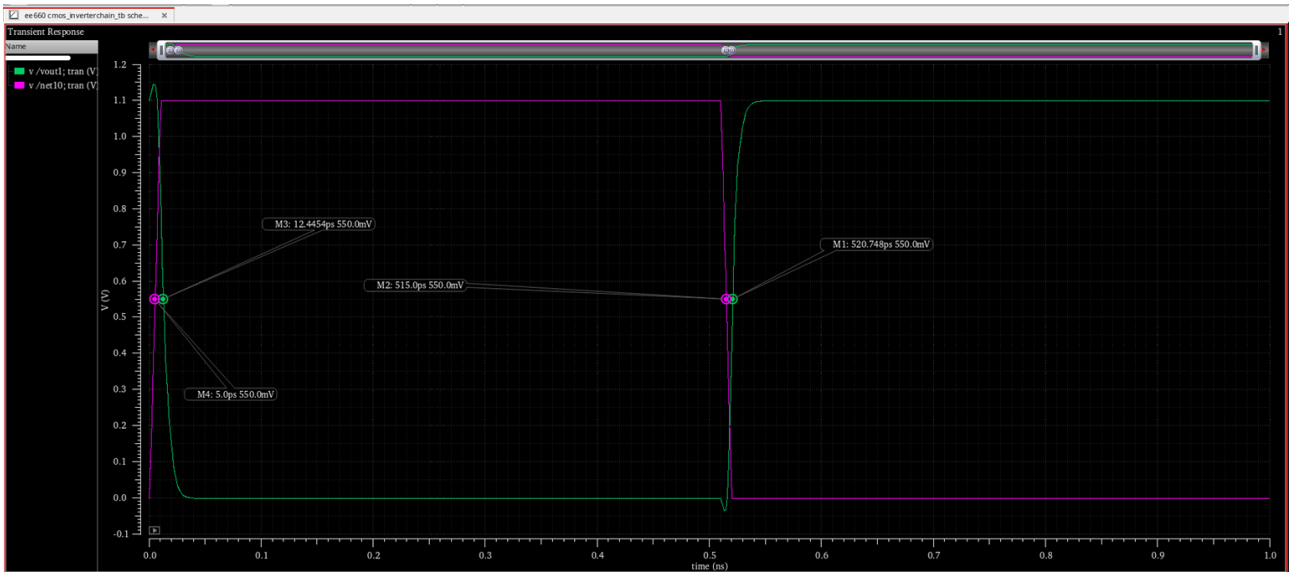


Figure : Simulated transient response of the inverter.

Observation: From the above plot it is observed that **tpHL= 7.44psec** and **tpLH= 5.74psec**

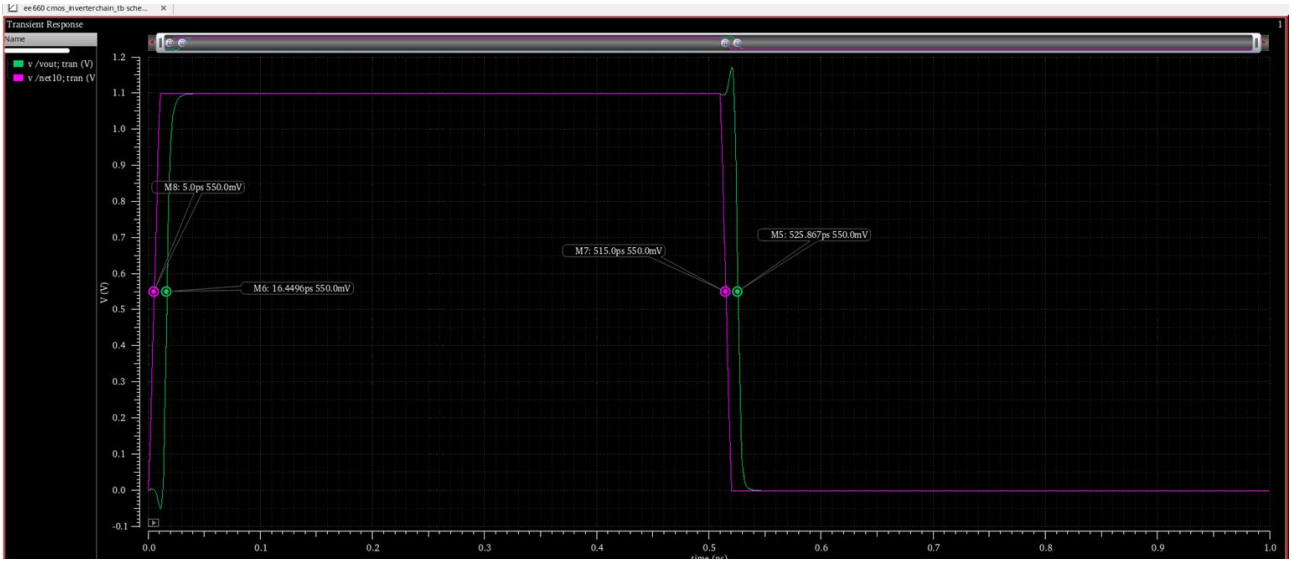


Figure : Simulated transient response of the inverter pair .

Observation: From the above plot it is observed that **tpHL= 10.867psec** and **tpLH= 11.44psec**

(e) Calculate the static, dynamic, and switching power consumptions of the inverter.

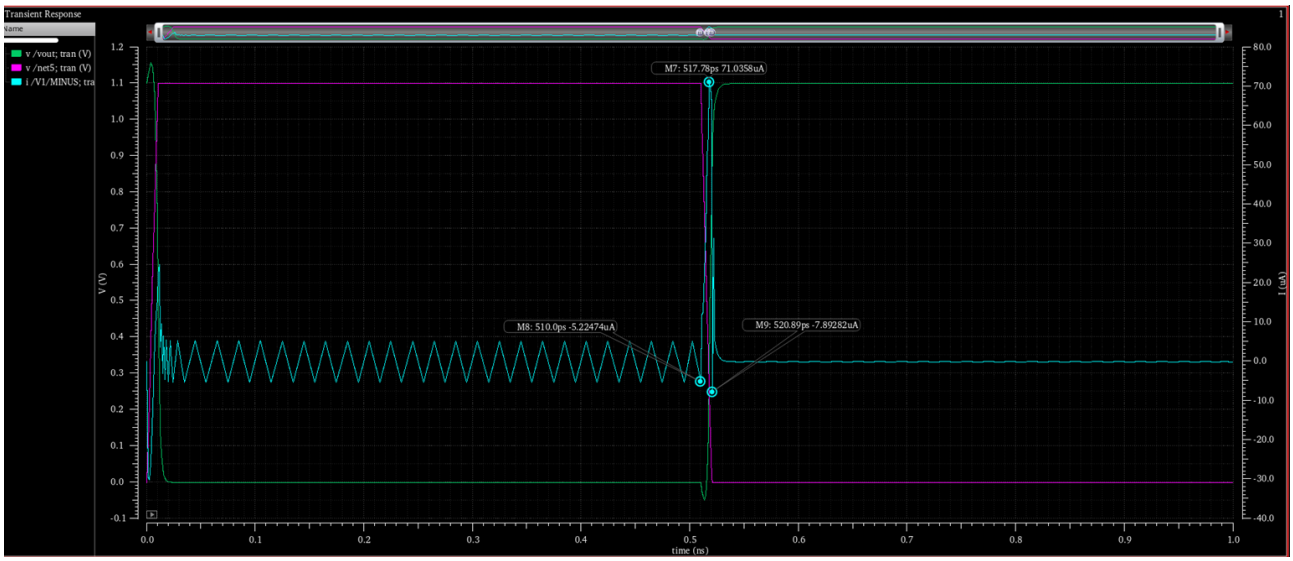


Figure : Plot showing short circuit current during transient analysis.

Switching Power Calculation:
From the above plot :
tsc= 10.89ps
Ipeak = 71uAmps
fclk= 1GHZ since t=1ns
Switching Power = tsc*Ipeak * fclk*Vdd = 10.89ps * 71uA * 1 GHz * 1.1v =0.850 **uW**

Static Power Calculation:

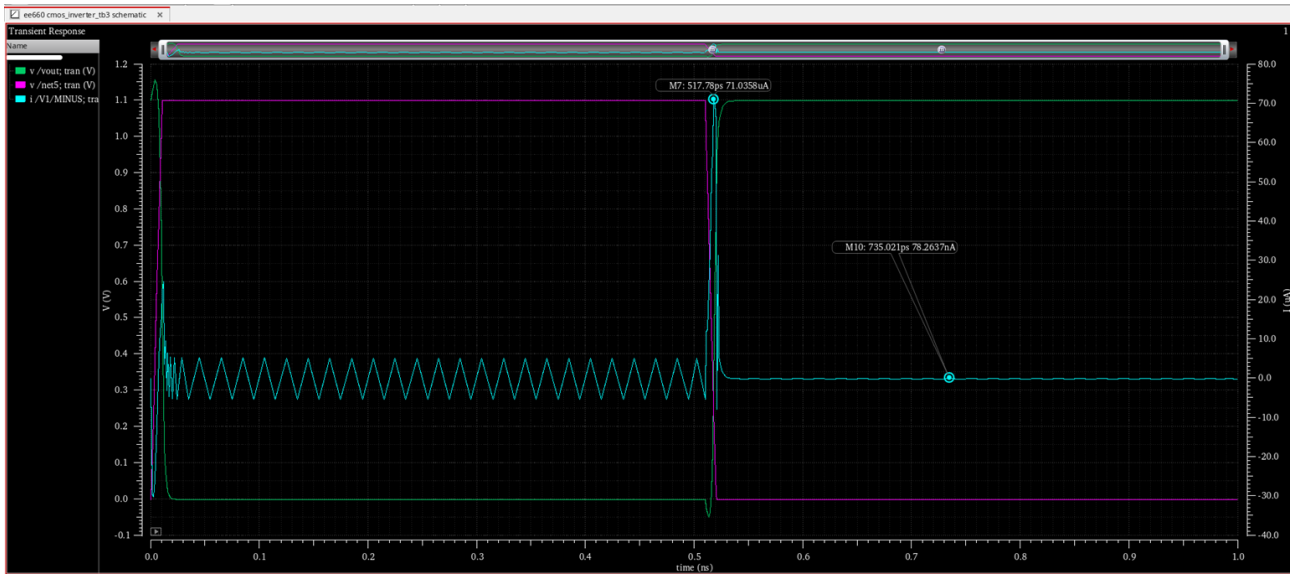
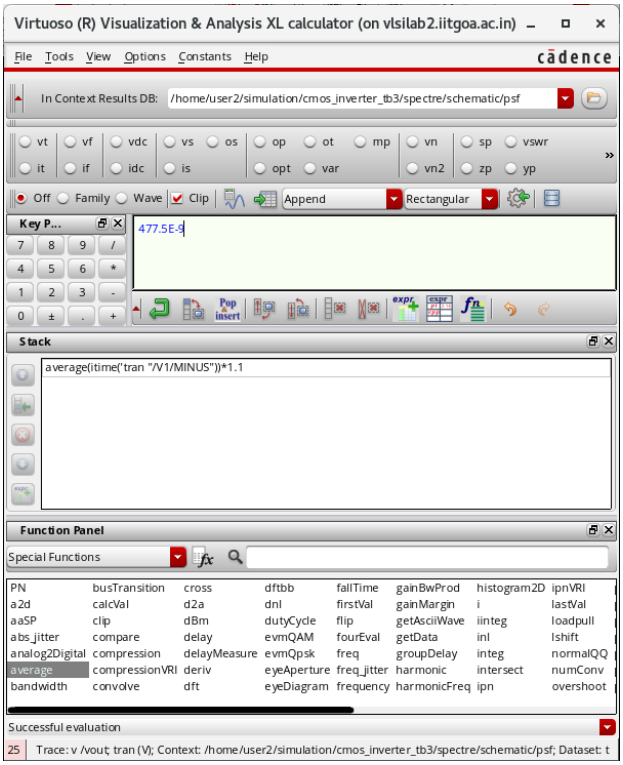


Figure : Plot showing short circuit current during transient analysis.

Pstatic= Vdd*I leakage
From the above plot its observed that I leakage = 78.26nA
P static= 1.1v*78.26nA =86 nW.

Dynamic Power Consumption:



Dynamic power has been calculated using built-in functions that helps to measure the average value of I of a circuit signal and then multiplied the result with vdd(1.1v).

Pdynamic =0.477 uW

2. A draw a compact layout of the inverter by cleaning DRC and LVS. Extract the netlist and do post-layout simulations of the steps mentioned in 1(a) to 1(e). Compare the pre- and post-layout simulation results. (You have to attach the screenshots of RVE indicating clean DRC, LVS, and PEX.)

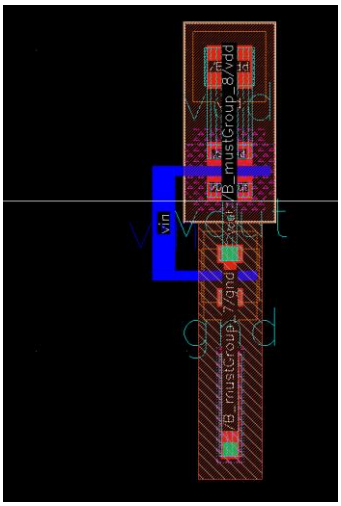
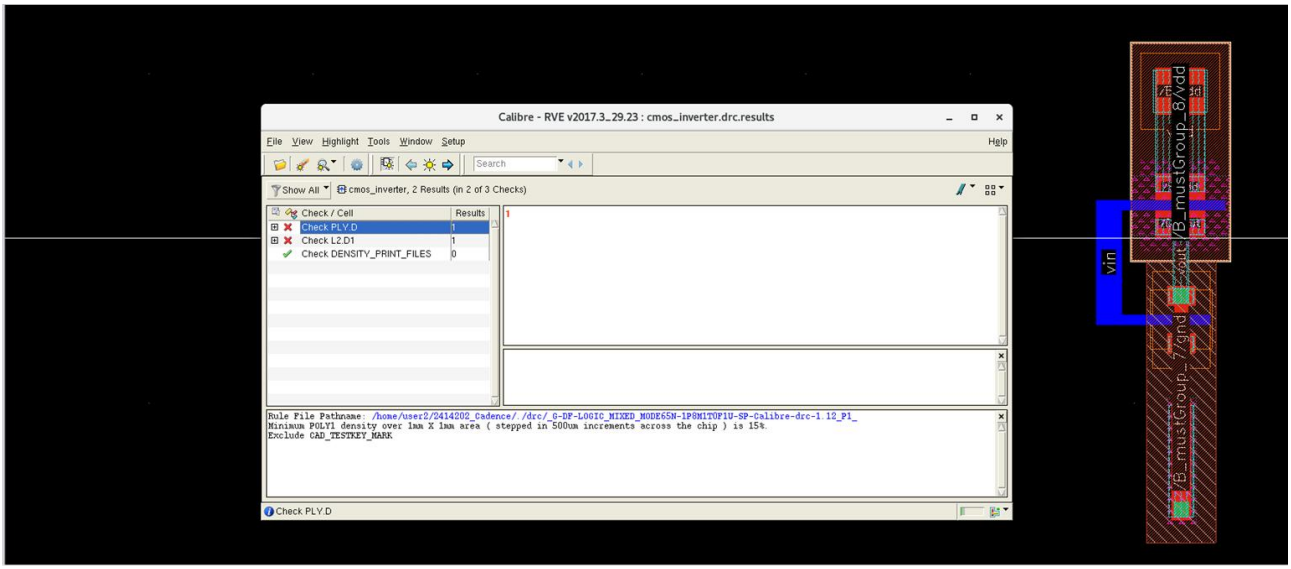
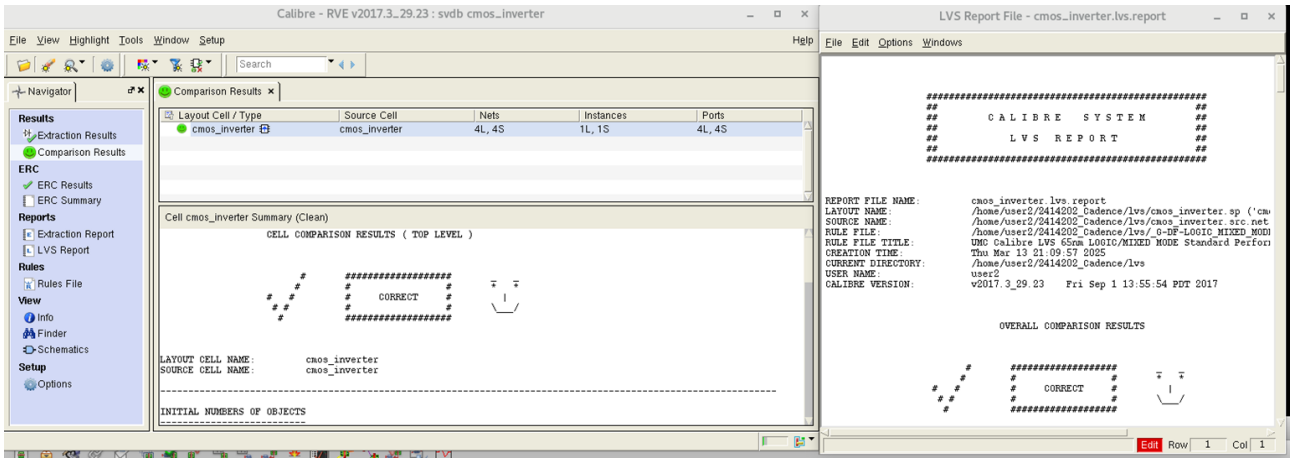


Figure: Layout of CMOS inverter

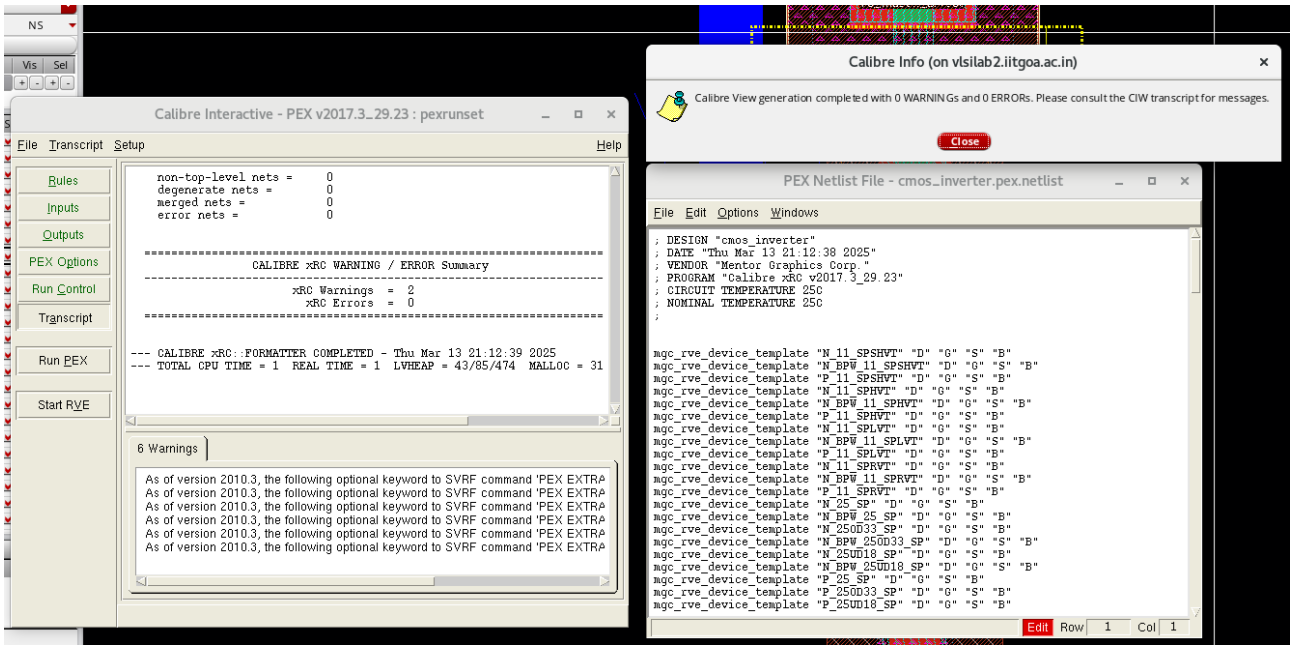
Below is the DRC Simulation result screenshot:

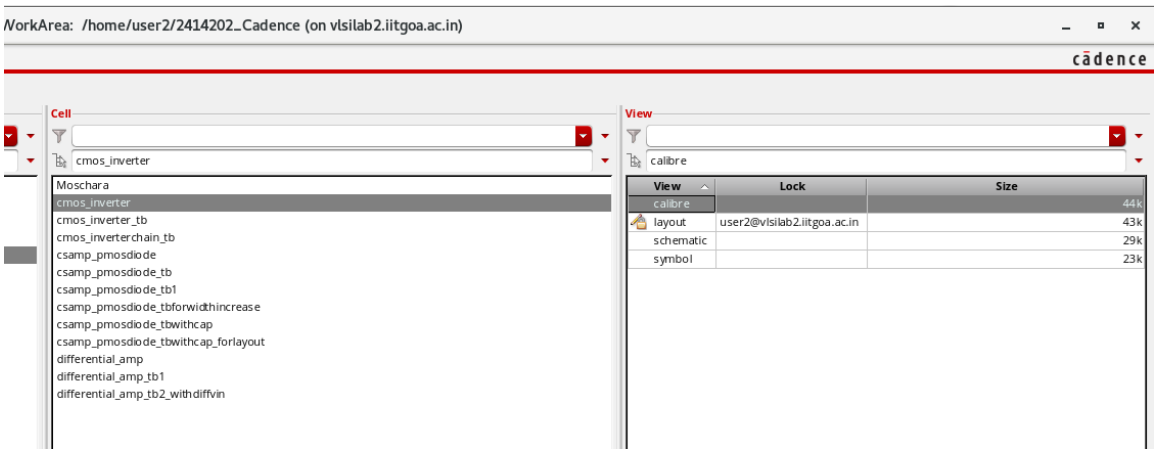


Below is the LVS simulation result screenshot:



Below is the PEX Simulation result screenshot:





Below are the Simulation results of post-layout dc and transient analysis:

(a) Using V DD as 1.1 V, draw the VTC of the inverter using schematic-level simulations.

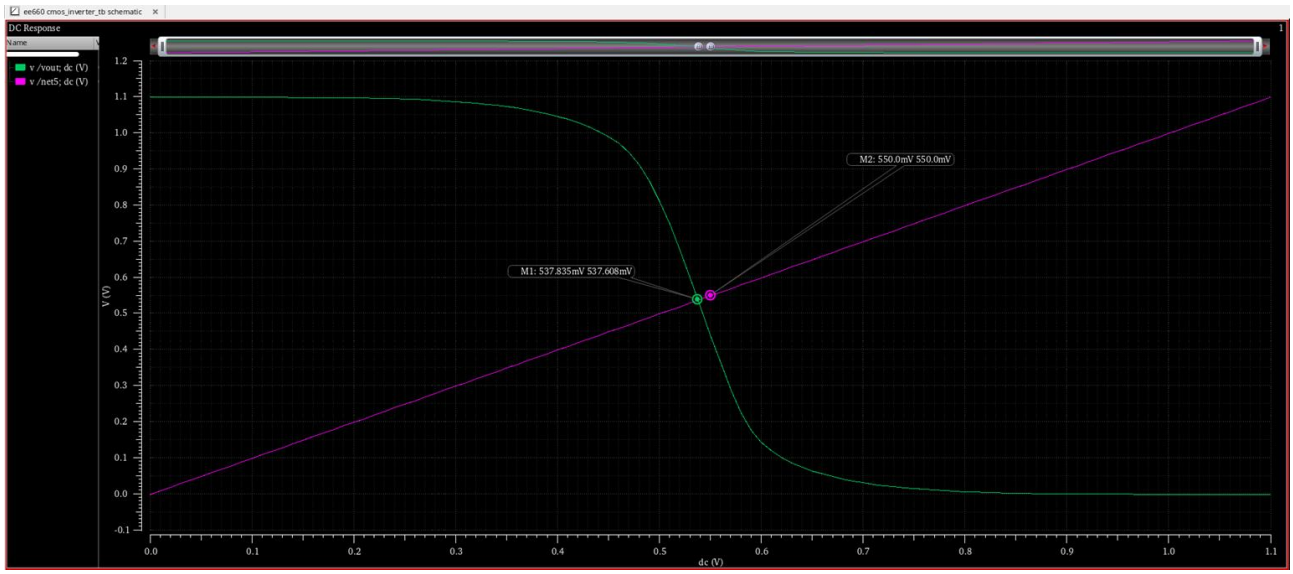


Fig: Plot showing VTC of inverter for post layout dc simulation

From the figure :
Switching threshold is identified as **VM =537.835mV**

(b) Using the VTC calculate the values of the switching threshold and noise margins.

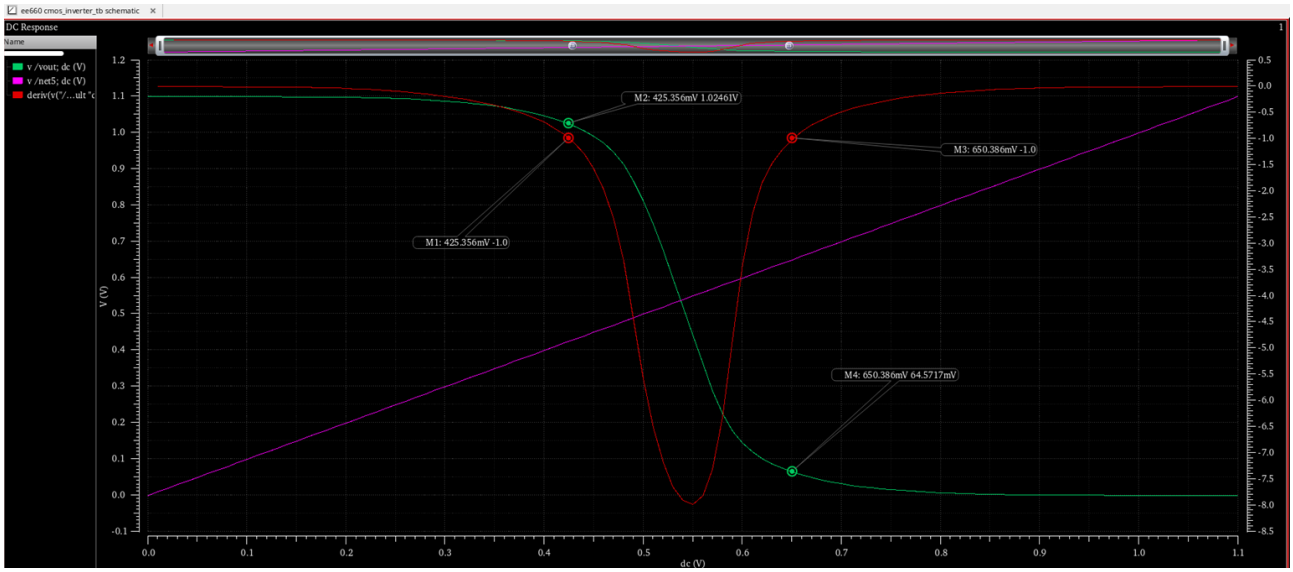


Figure : Plot showing VTC of CMOS inverter with gain

From the figure :

VIL=425.356mV ,VIH= 650.386mV
VOH=1.024V, VOL=64.571mV

NOISE MARGINS:

NMH =VOH-VIH = **0.374V**
NML = VIL-VOL = **0.36V**

(c) From the VTC estimate the gain of the inverter at V M and calculate the noise margins using the piecewise linear approximation of VTC.

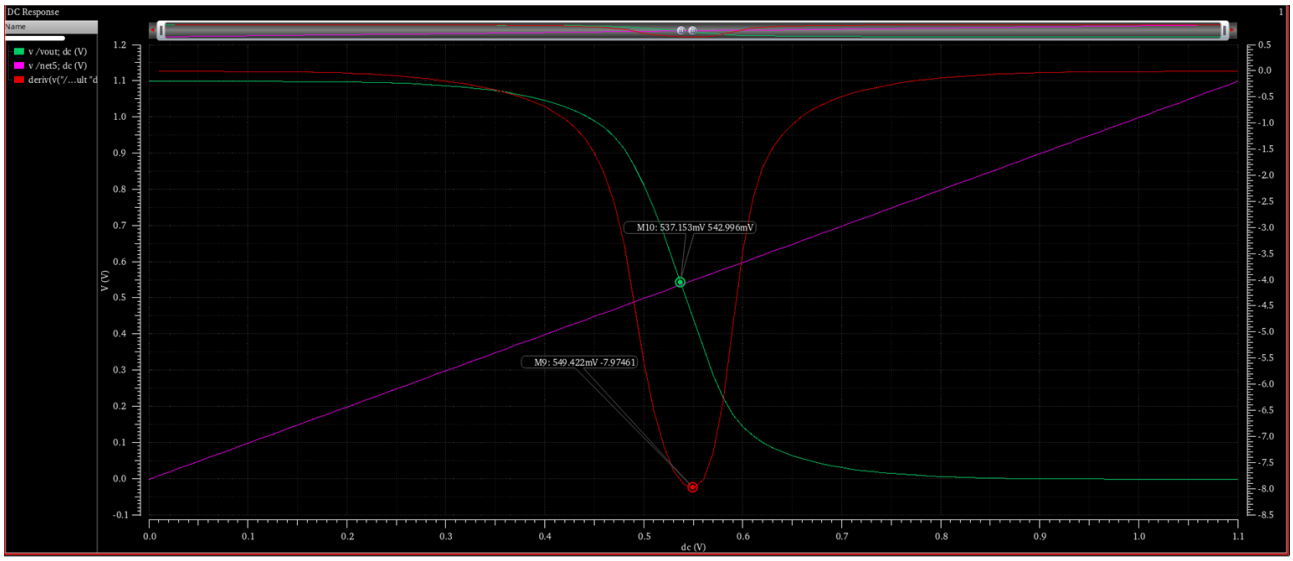


Figure : Plot showing piecewise linear approximation of VTC

From the plot :

g=-7.974
Vm=0.537V

Noise Margins Calculation using piecewise linear approximation :

$$V_{IL} = V_M - \frac{(V_M - V_{DD})}{g}$$

$$V_{IH} = V_M - (\frac{V_M}{g})$$

$$NM_H = V_{DD} - V_{IH}$$

$$NM_L = V_{IL}$$

NM_H=1.02V
NM_L=0.466V

(d) Calculate the values of t pLH and t pHL by doing a schematic transient simulation of the inverter driving a copy of it.

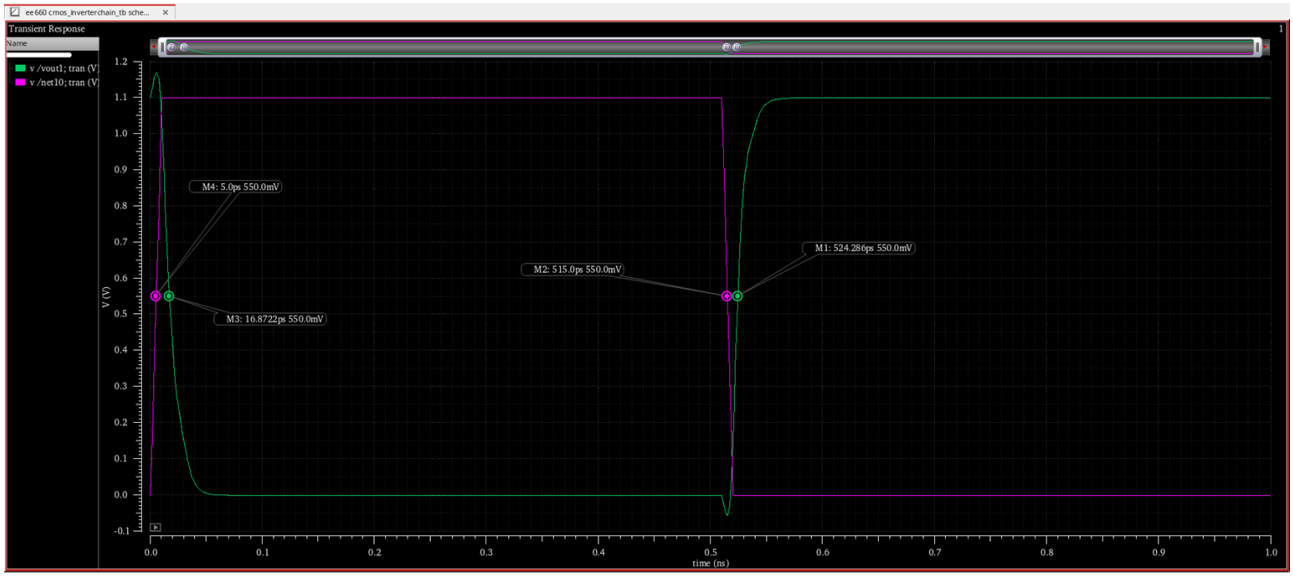


Figure : Simulated transient response of the inverter.

From the plot :

tpHL = 16.872ps-5ps =11.872ps
tpLH = 524.286ps-515ps = 9.286ps

(e) Calculate the static, dynamic, and switching power consumptions of the inverter.

Switching Power Calculation:

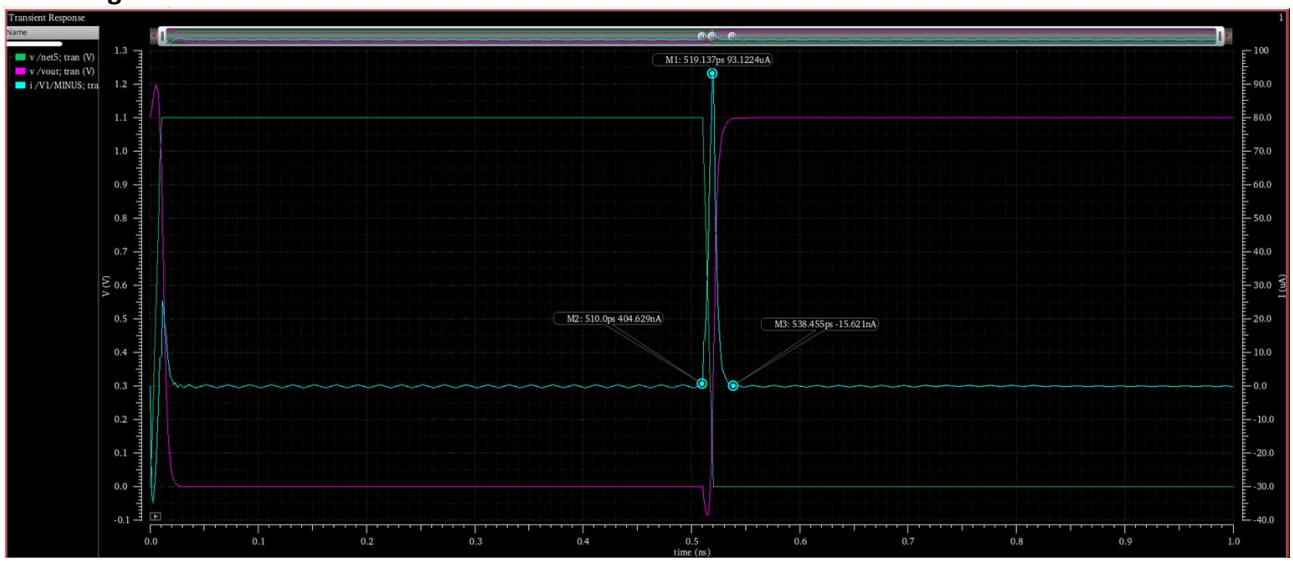


Figure : Plot showing short circuit current during transient.

From the above plot :

tsc= 38.45ps
Ipeak = 93.12uAmps
fclk= 1GHZ since t=1ns
Switching Power = tsc*Ipeak * fclk*Vdd = 38.45ps * 93.12uA * 1 GHz * 1.1v =**3.938 uW**

Static Power Calculation:

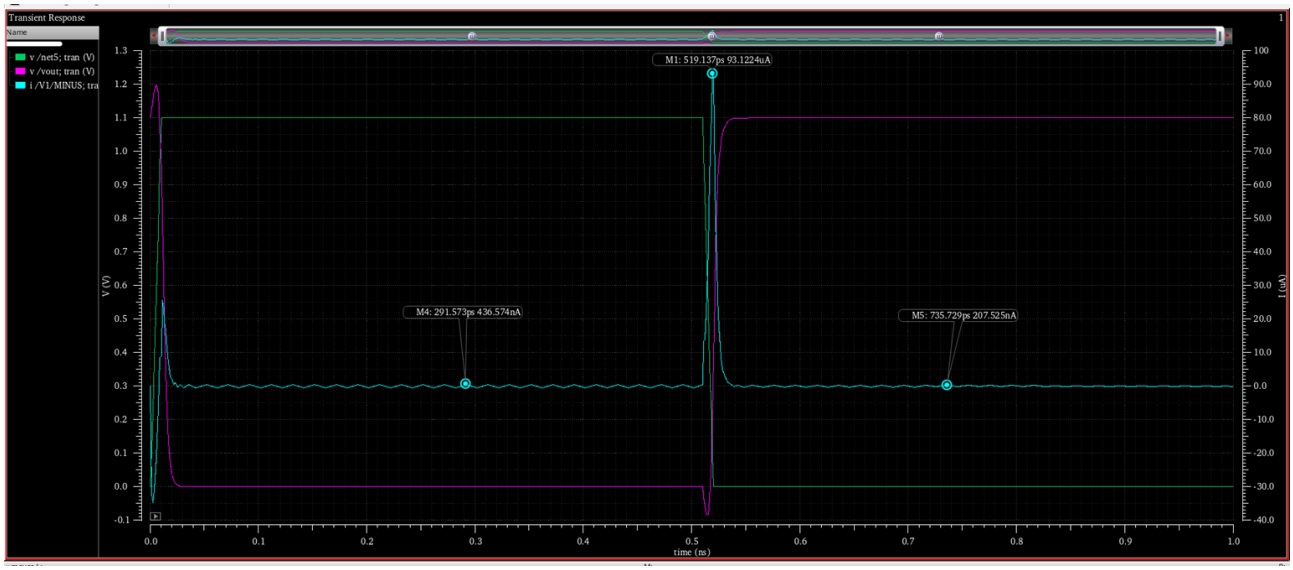


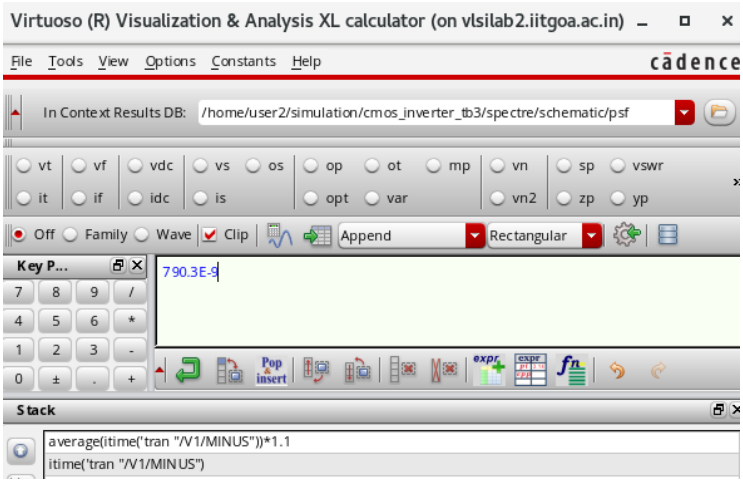
Figure : Plot showing leakage current during transient.

From the plot, It is observed that I leakage = 436.574nAmps

Pstatic= Vdd*I leakage

P static= 1.1v*436.574nA =0.48 pW.

Dynamic Power Calculation:



Dynamic power has been calculated using built-in functions that helps to measure the average value of I of a circuit signal and then multiplied the result with vdd(1.1v).

Pdynamic =0.790 uW