EE 660 VLSI Design Laboratory

Assignment IV

Submitted by: L Sri Sai Swathi (2414202)

1. You have done the schematic level simulations of a CS amplifier as shown in Fig. 1 in Assignment
2. Taking the same cell as the schematic, complete its layout

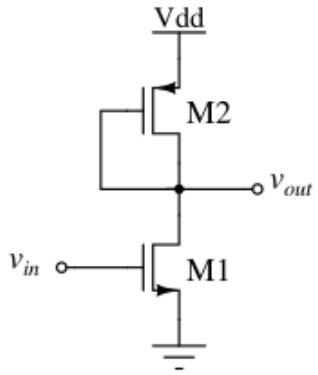


Figure 1: Common-source amplifier with diode connected load.

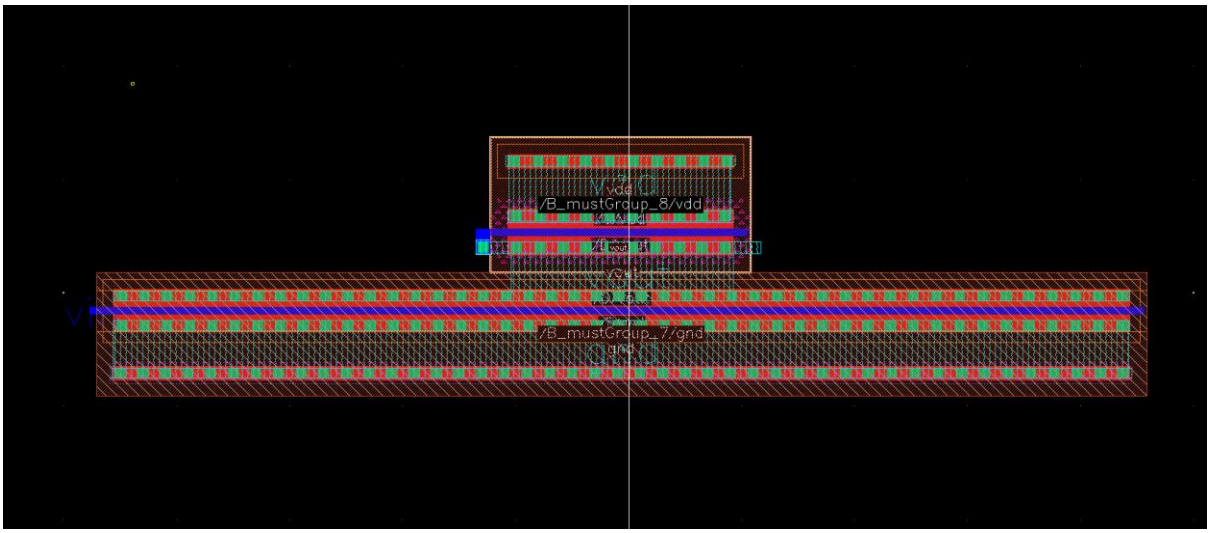


Figure : Layout of CS Amplifier with PMOS diode connected load

2. Using the same test bench do a post-layout large signal analysis of the circuit by doing a DC sweep of the input voltage from 0 to V DD (1.1 V). Decide the input common-mode voltage at the centre of the region where both M1 and M2 are in saturation. Mention if you see any difference in the large signal transfer characteristics between pre- and post-layout simulations.

Results of Post-layout large signal analysis when Vin dc is sweeped from 0 to 1.1v(VDD)

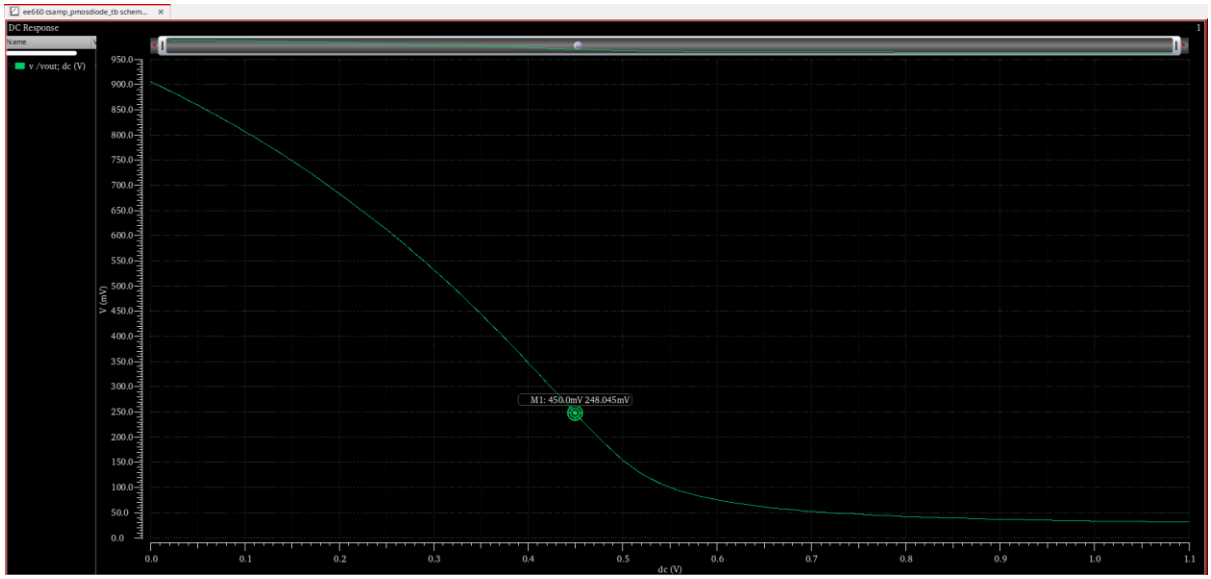
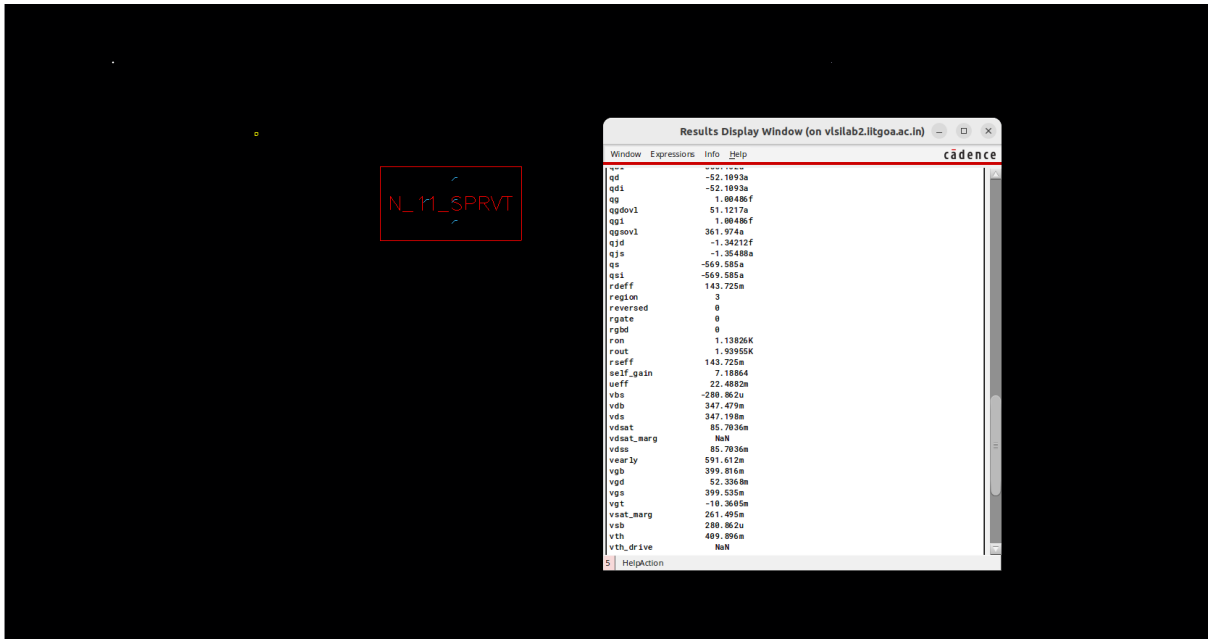


Figure: Plot showing Vout vs Vin

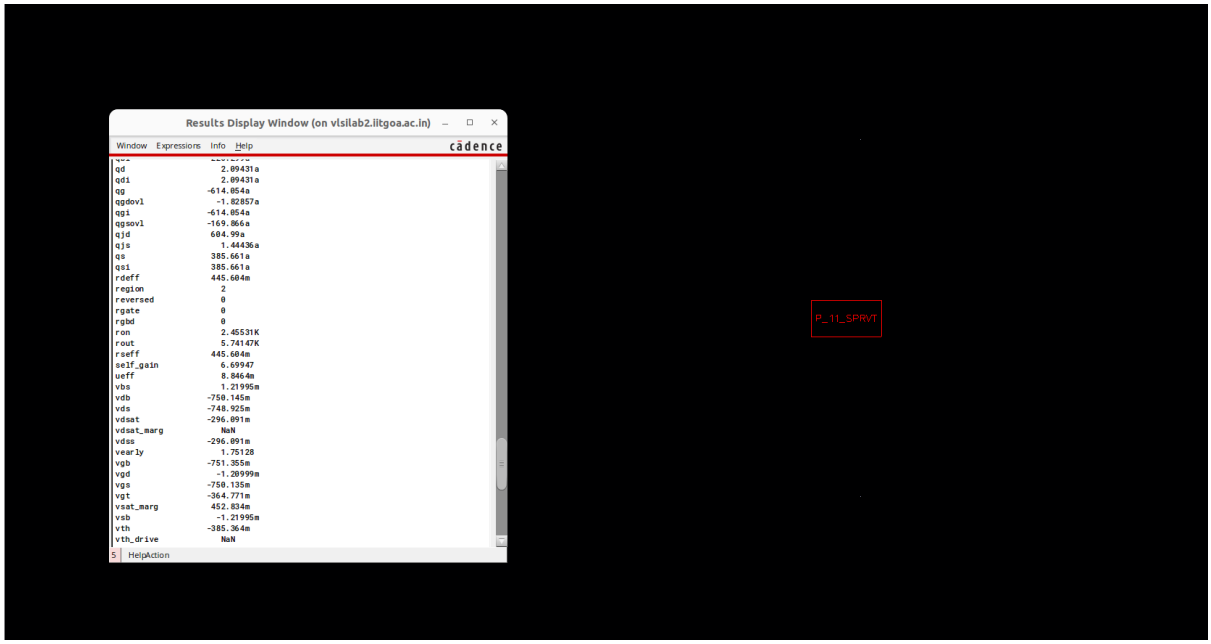
From the plot , Assumed **0.4v** as common mode voltage and verified as follows:-

Below are the simulation results of Analysis done at **400mv**

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 3 of Operation, which means “Cuttoff region”. It is also noted that Vtn =0.409v.



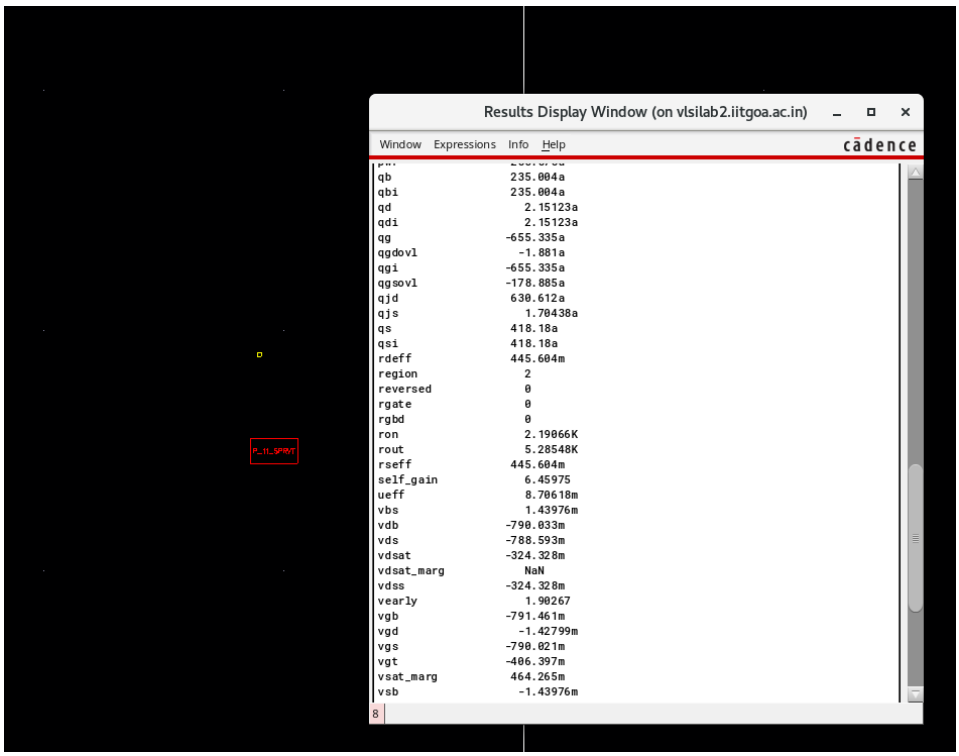
Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “Saturation region”. It is also noted that |Vtp| =0.385v.



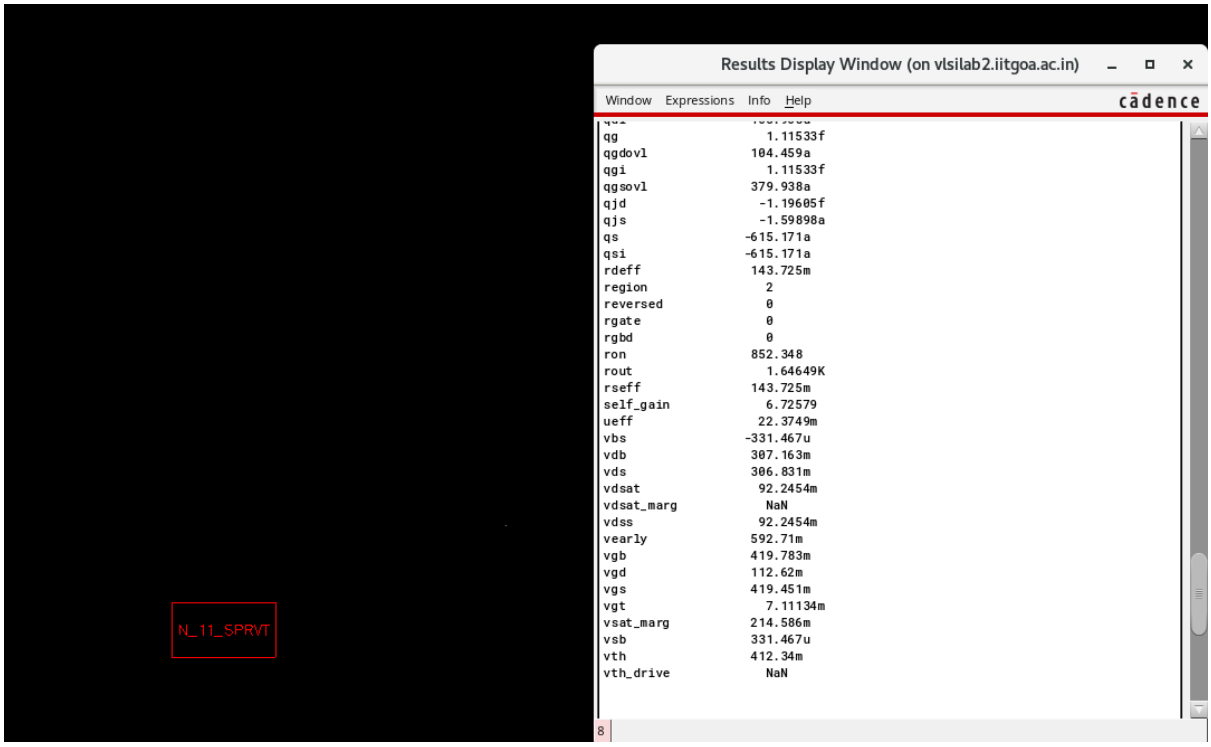
Observation : Since both transistors are **not in saturation** when we chose VGS as 400mV , we are choosing another value 420mV which is greater than both vtn and vtp.

Below are the simulation results at 420mv:

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means "**Saturation region**"



Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of operation which means "**Saturation region**"



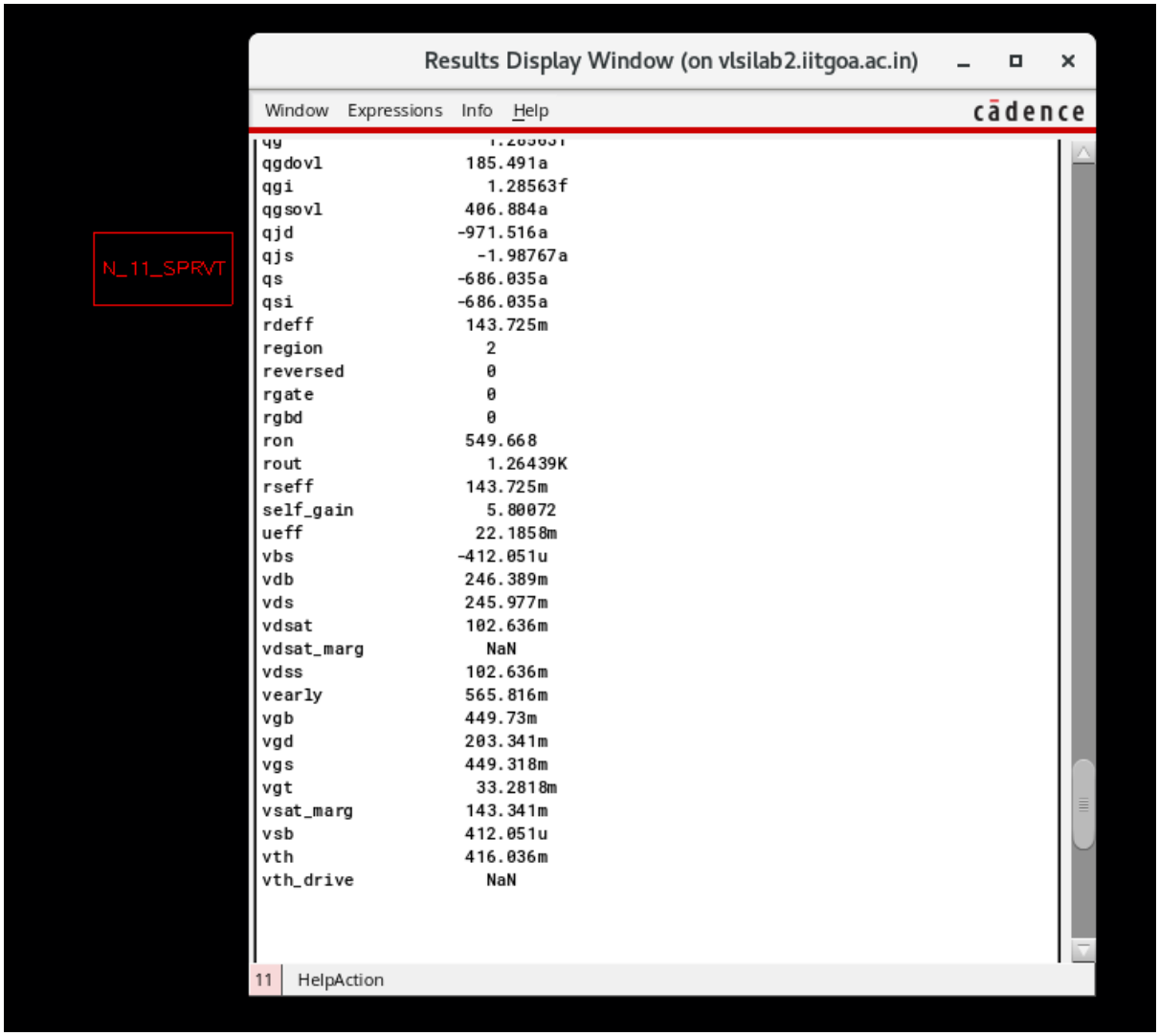
Observation: From the above analysis, it has been verified that 2 transistors are in Saturation region of

operation when **Vgs=420mV.**

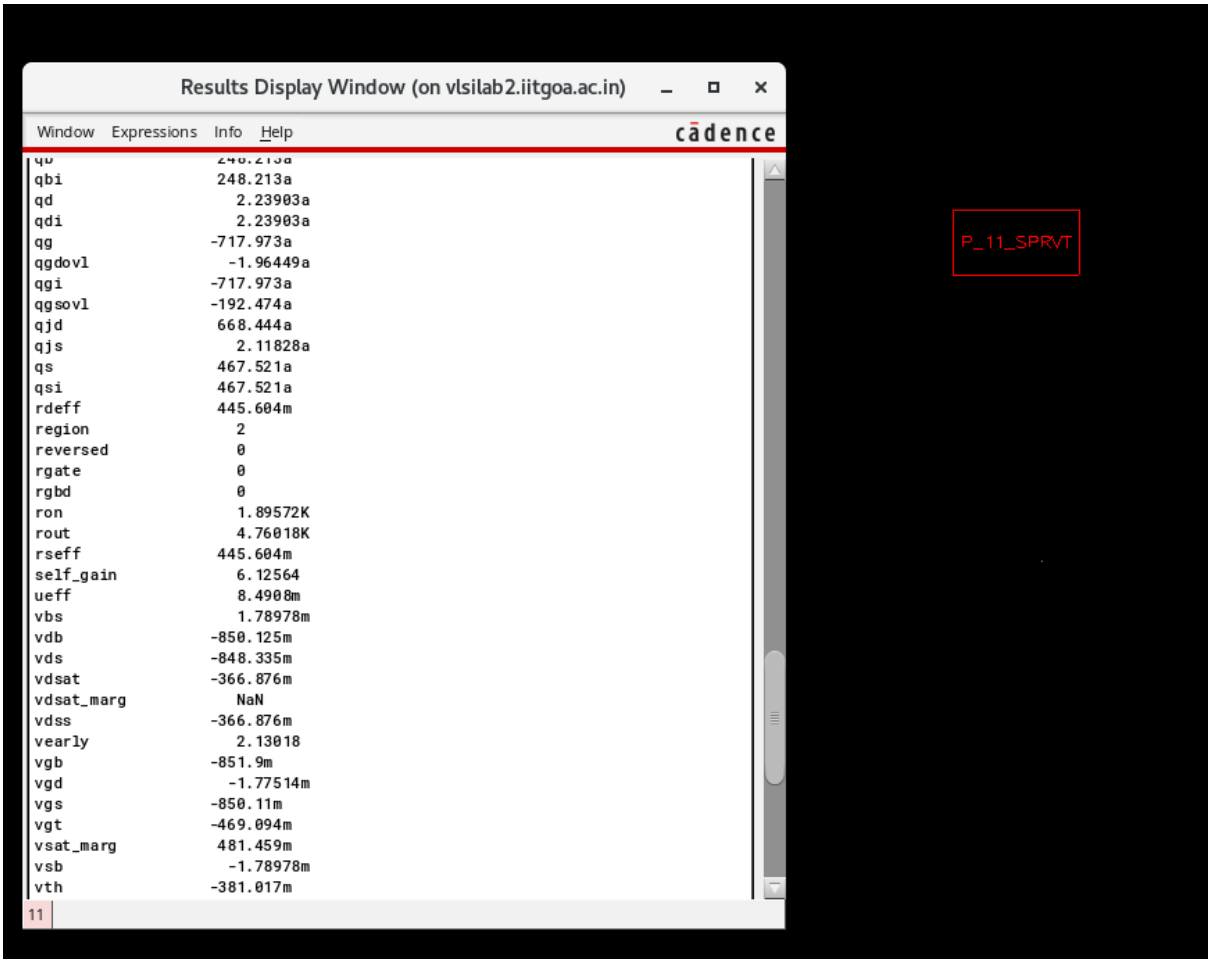
Below are the simulation results of Analysis done at vgs=450mv:

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of

operation which means "**Saturation region**"



Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means "**Saturation region**"



Observation: From the above analysis it's been verified that 2 transistors are in Saturation region of operation when **Vgs=450mV.**

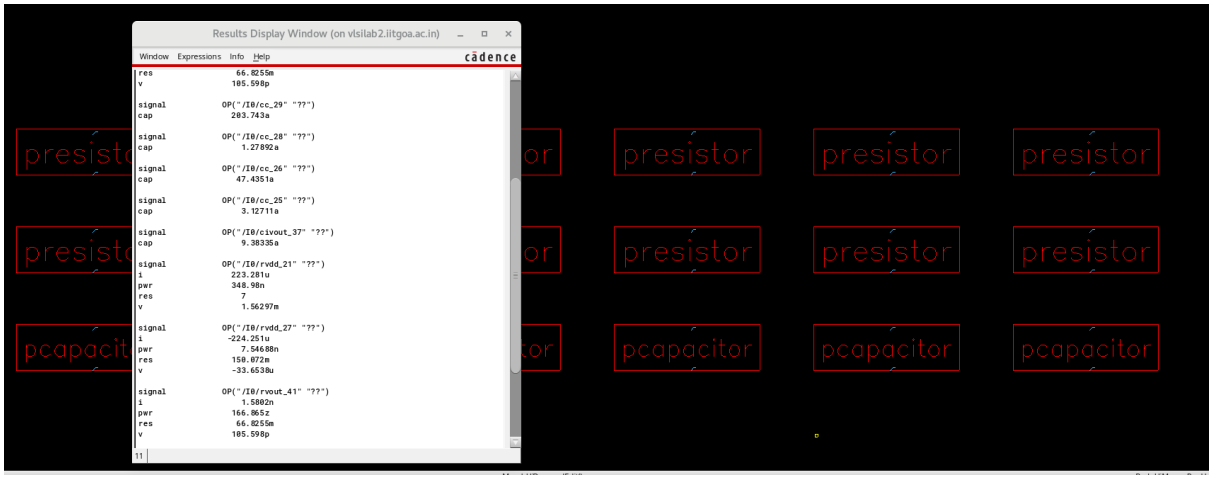


Figure : Layout containing all the parasitic capacitances and resistances .

Finally choosing **420mv** as common mode voltage from all the above simulation data.

Difference in the large signal transfer characteristics between pre- and post-layout simulations:

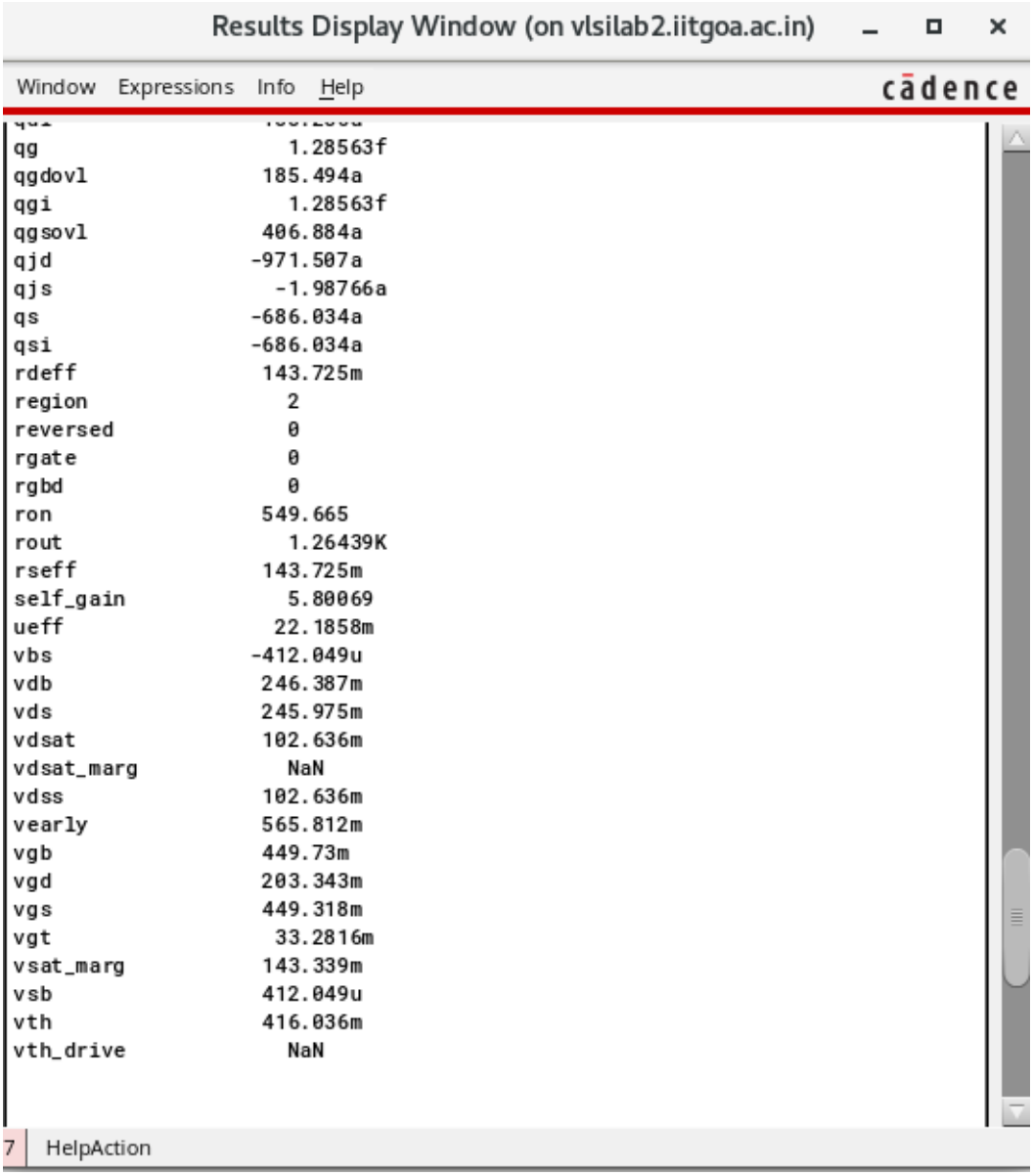
***** The main difference is that pre layout VTC has comparatively sharper transition than post layout VTC. It is mainly due to the additional parasitic effects included in the layout(i.e Schematic is quickly responding to changes in input). Also it is observed that when vin =0.01v vout (pre-layout)=930mV and vout(post-layout)=900mV.

3. Connect a sinusoidal source at the input with an amplitude of 10 mV and a 500 fF capacitive load at the output. In all the following simulations, compare the results of pre- and post-layout simulations.

(a) Perform a post-layout DC operating point analysis to verify that the transistors are in saturation. You may not be able to print the operating point as you did in schematic simulations. You will have to decide the operating region using the terminal voltages.

Have Chosen **Vdc as 450mV** , AC amp as 10mV and a 500fF capacitive load .

Below is the simulation result of DC operating point analysis. It shows that PMOS is in region 2 of operation which means “Saturation region”.



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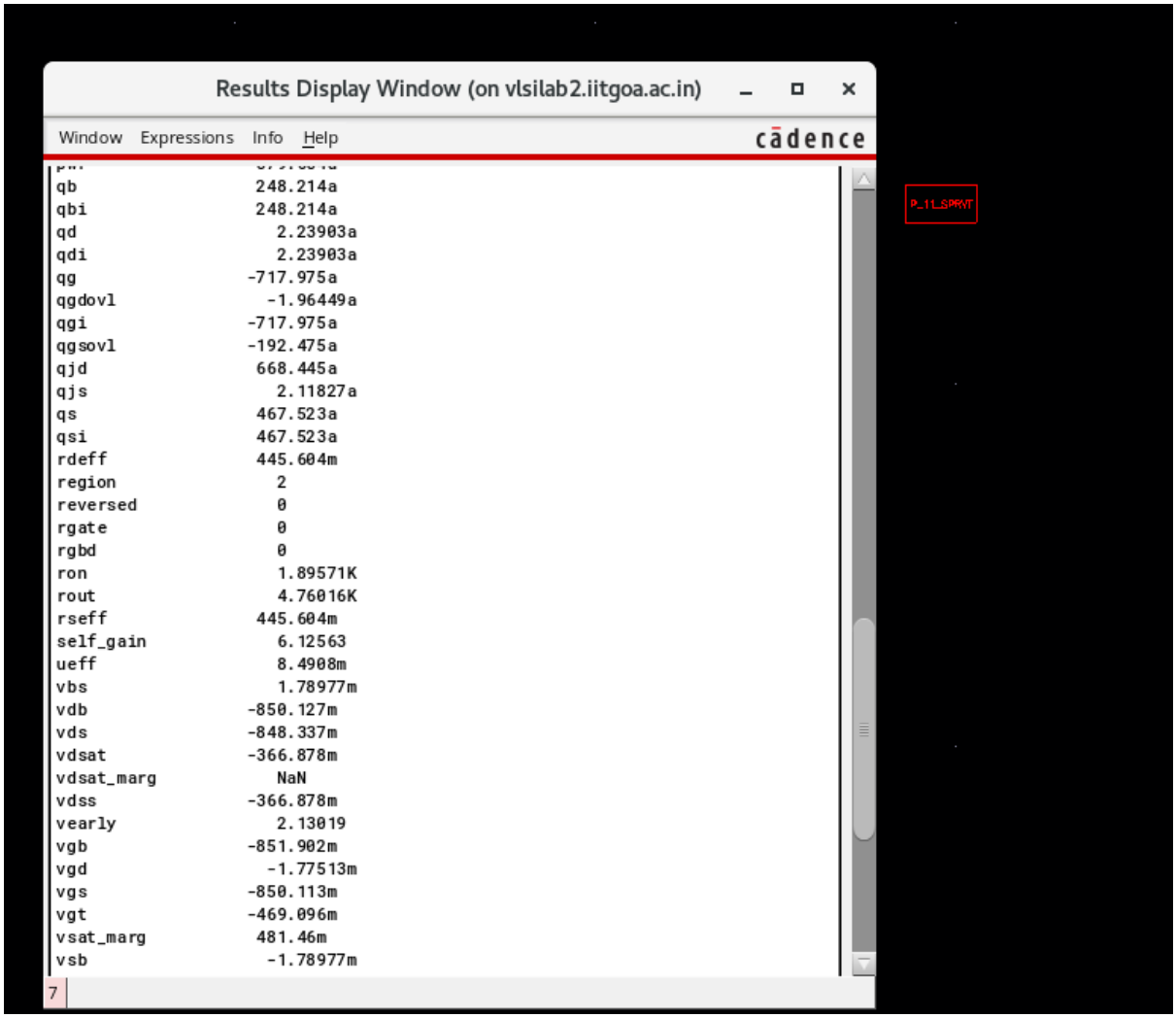


Observation:Verified that both M1 and M2 are in saturation region of operation when we have connected AC source .

Below are the transient analysis results:

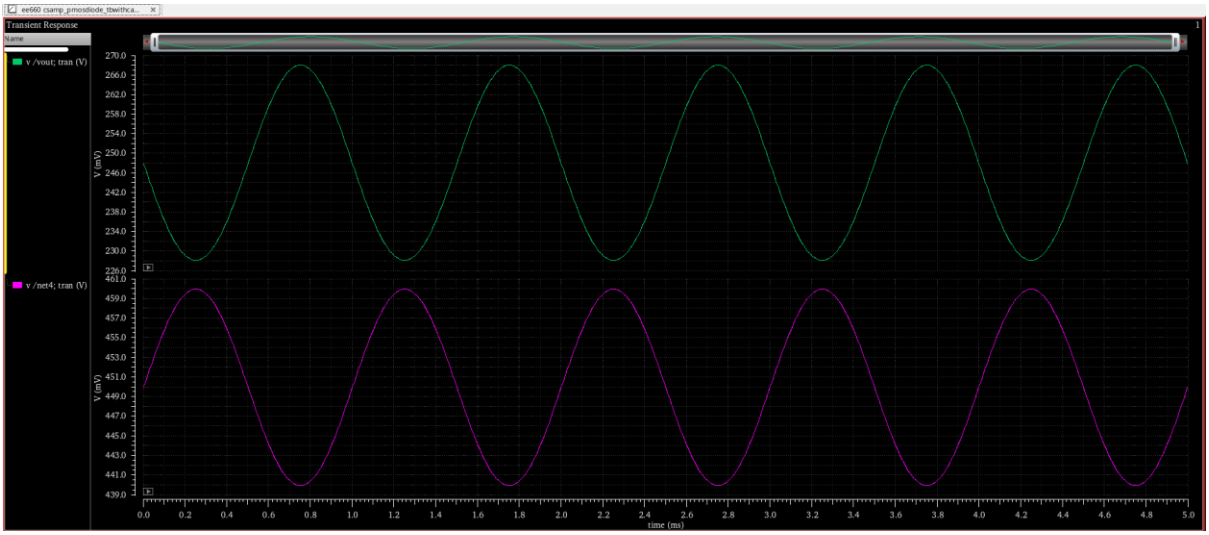


Figure: Plot showing Vin ,Vout waveforms obtained from transient analysis .

Observation: From the above transient analysis graphs it is observed that input and output waveforms are **out of phase**.

(c) Perform an AC analysis of the circuit. Plot the magnitude and phase responses. Note down the low frequency gain and 3 dB frequency of the circuit. Also, check what is the phase difference between the input and output at the 3 dB frequency.

Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

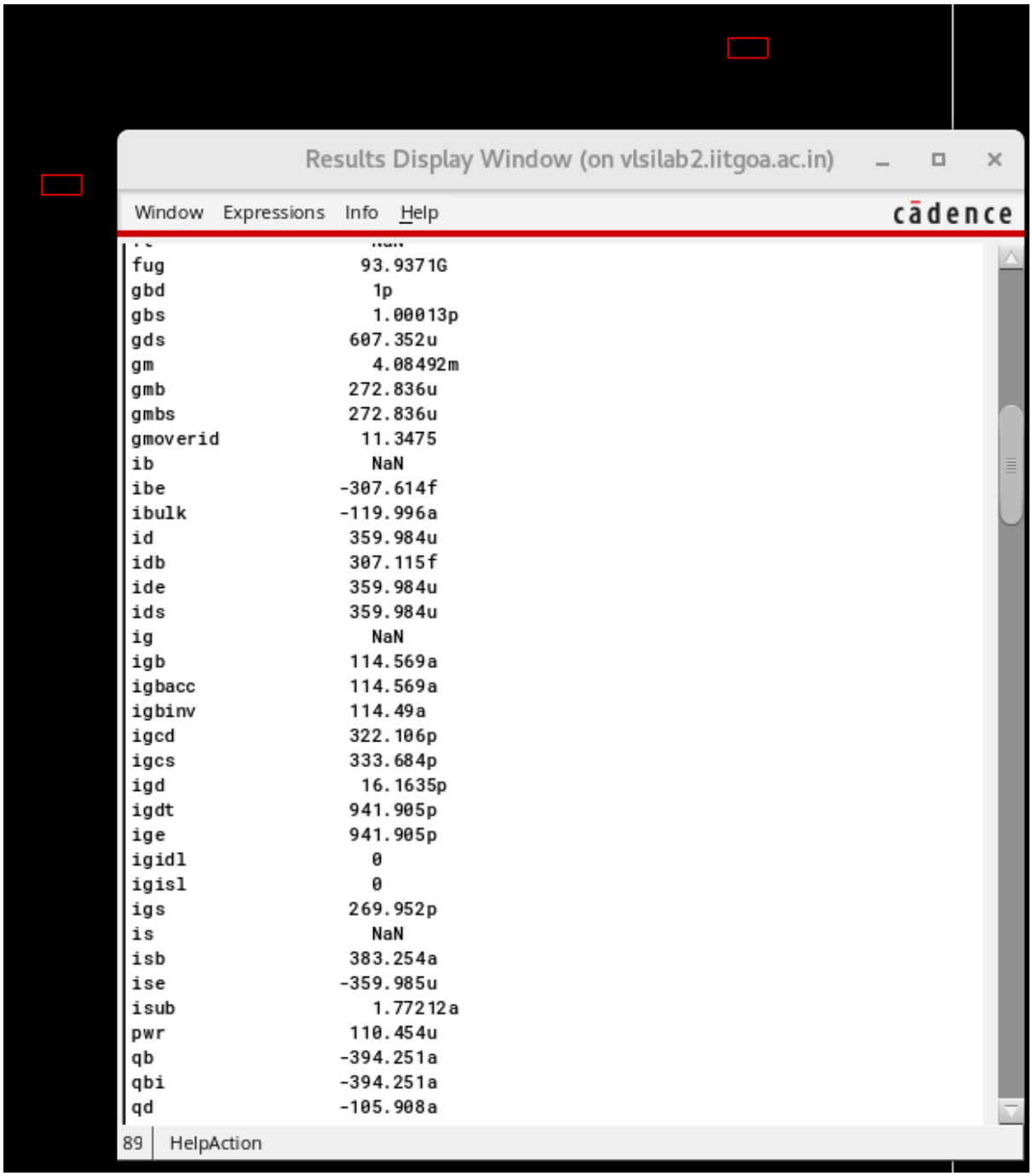
Observations:From the above Ac Analysis plot we can say that :

1.Low frequency gain is **6.1071dB**

2. 3dB cuttoff frequency is **609.576MHz**

3.Phase difference between the input and output at the 3 dB frequency: **133 Degrees.**

(d) Calculate the power dissipation of the circuit.



Screenshot showing all the DC operating point values .

From the DC operating point analysis it is found that id=359.98uA

Power dissipation of the circuit = Id * Vdd = 359.98uA*1.1v =0.395mW

Difference in the large signal transfer characteristics between pre- and post-layout simulations:

a) At Vindc=420mv ,Vin,ac=10mv ,both pre and post layout dc operating point analysis have M1,M2 in saturation region of operation. But it is observed that Vtn and Vtp increased during post layout simulation.

For pre layout DC operating point analysis: Vtn =408mV, |vtp| =312mV

For post layout DC operating point analysis: Vtn =416mV, |vtp| =381mV

b) Transient Analysis simulation results are similar for pre and post-layout simulation.

C) AC Analysis simulation results comparison: Gain and 3 db cuttoff frequency reduced in case of post -layout simulation.

For pre layout simulation:Low frequency gain is **6.57dB,**3dB cuttoff frequency is **639.475MHz**

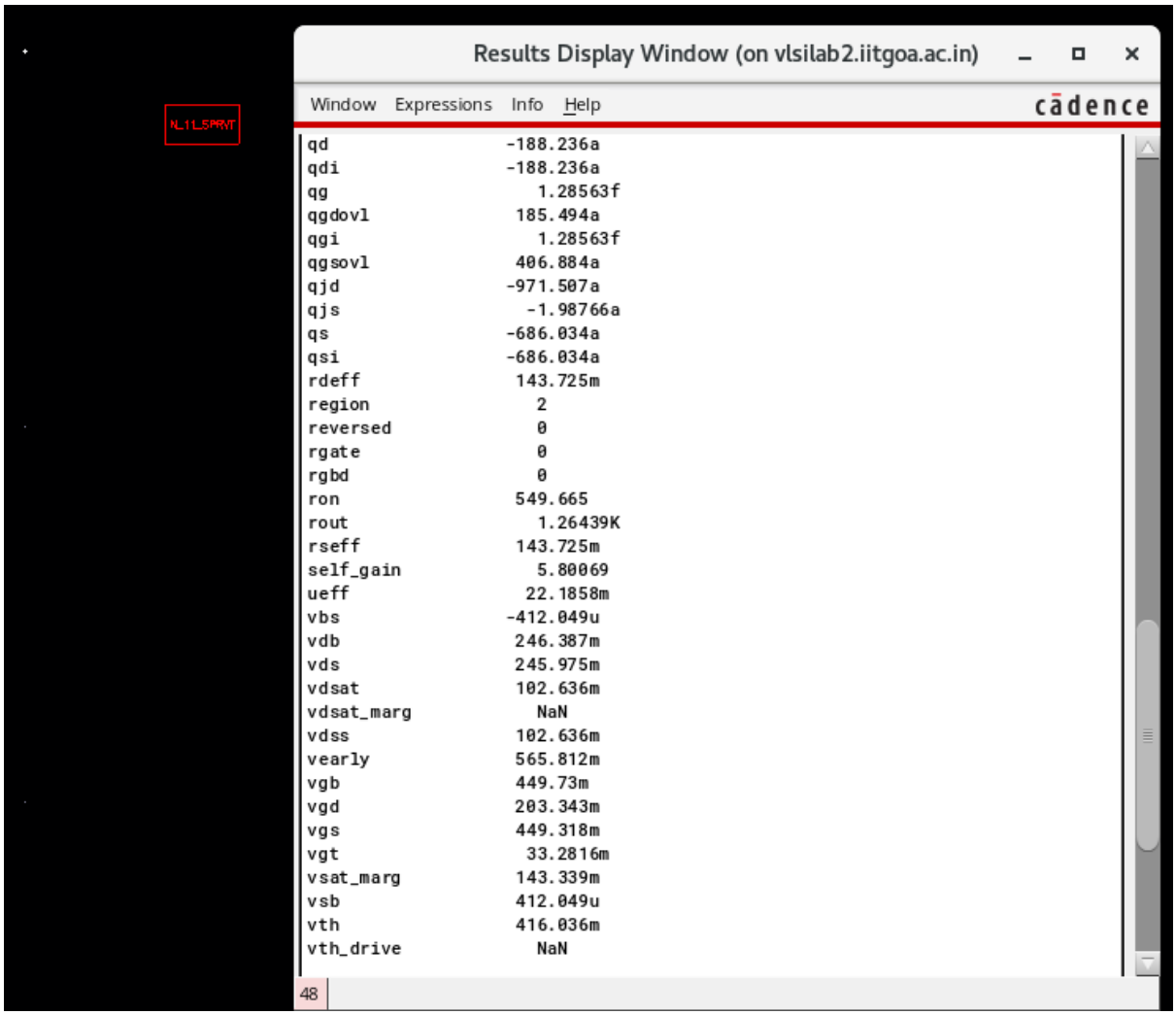
For post layout simulation:Low frequency gain is **6.1071dB,**3dB cuttoff frequency is **609.576MHz**

d)Power Dissipation: Power dissipation in the circuit is slightly lesser in case of post-layout simulation. **i.e 0.4763mW for pre-layout and 0.395mW**

4. Repeat step 3 by changing the amplitude of the sinusoidal source to 200 mV. Do you see any differences between the results? If yes, justify your observations. Compare the results of pre- and post-layout simulations.

(a) Perform a post-layout DC operating point analysis to verify that the transistors are in saturation. You may not be able to print the operating point as you did in schematic simulations. You will have to decide the operating region using the terminal voltages.

Below is the simulation result of DC operating point analysis. It shows that NMOS is in region 2 of operation which means "**Saturation region**".



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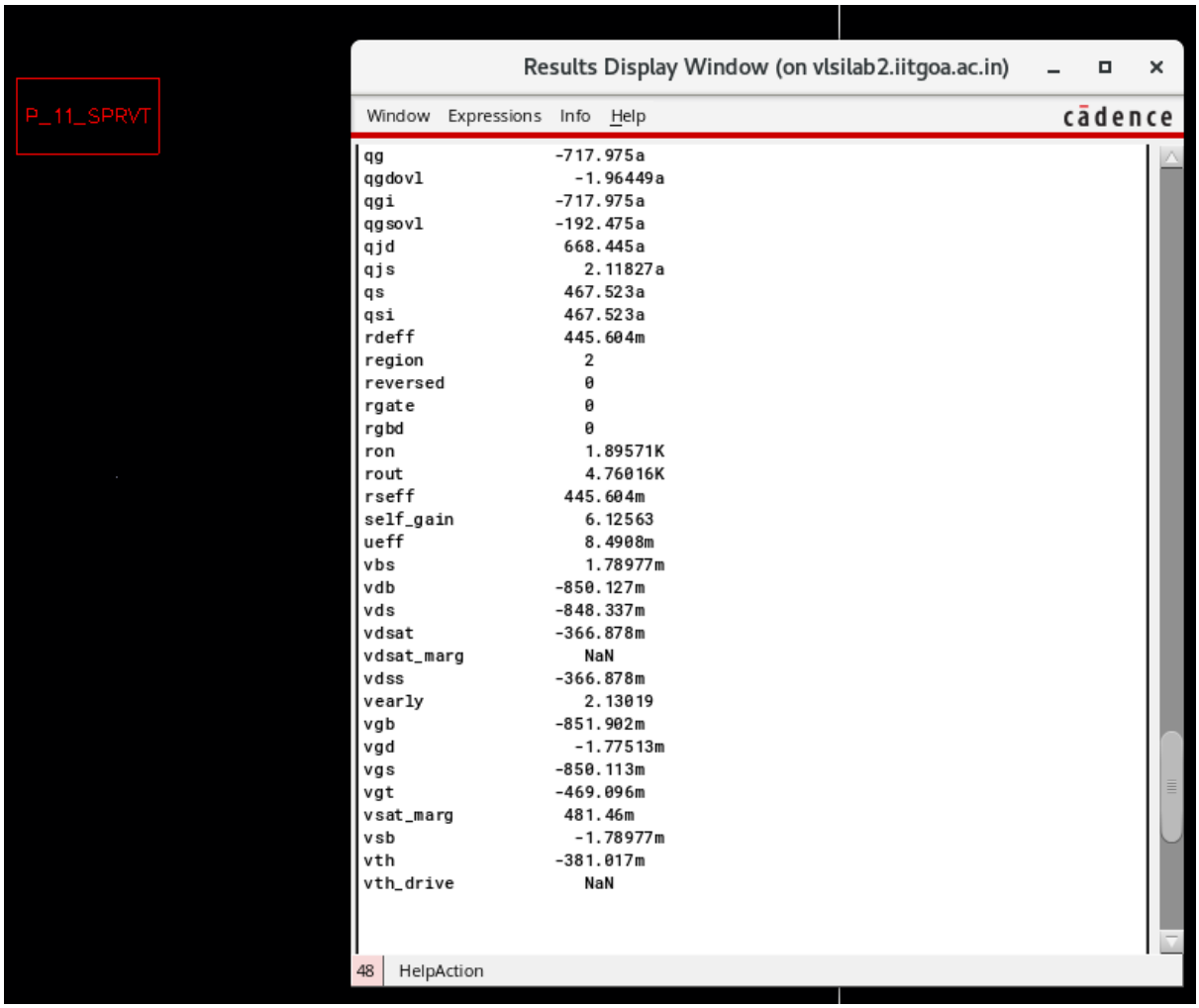
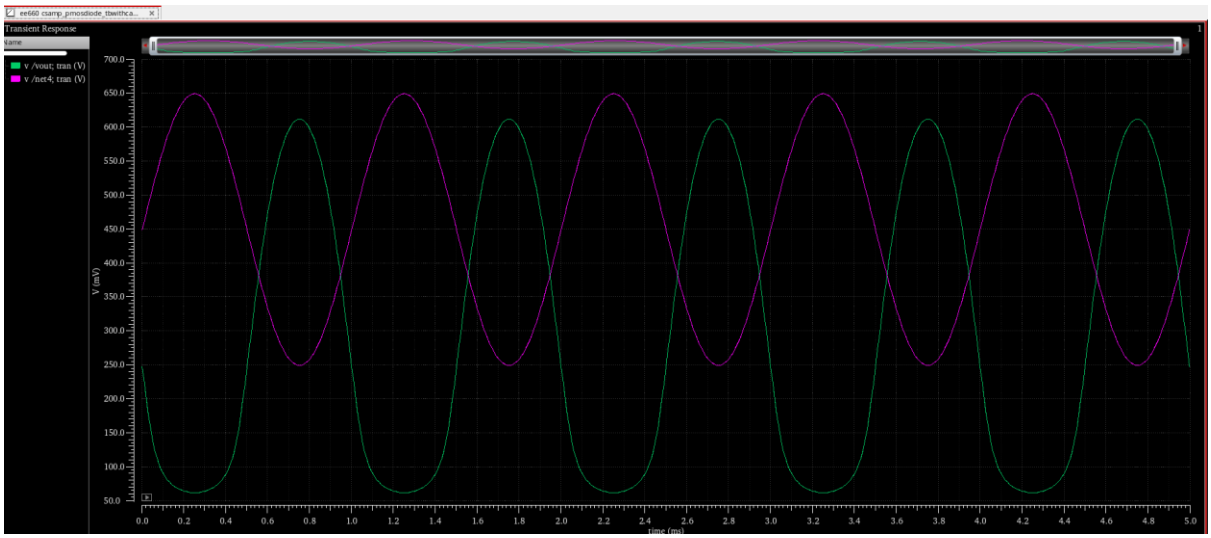


Observation: From the above DC operating point analysis it's been verified that 2 transistors are in Saturation region of operation

(b) Perform a post-layout transient analysis of the circuit and verify that the input and output waveforms are out of phase.



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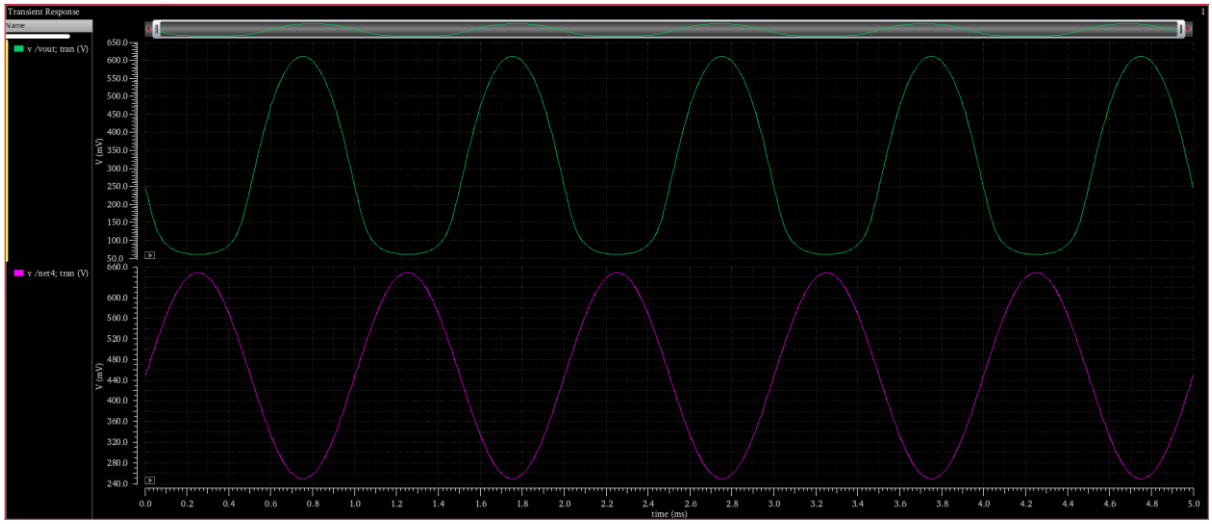

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Observation: *It is Observed that, after changing sinusoidal voltage to 200mV Vout waveform has been changed. This is mainly caused due to the clipping of output voltage caused due to the fact that M1 is in triode region since 0.2v is not in the range of saturation Vin . Hence , we could see that Vout got clipped. This is major change that has been observed when we have changed input of sinusoidal voltage to 0.2v*

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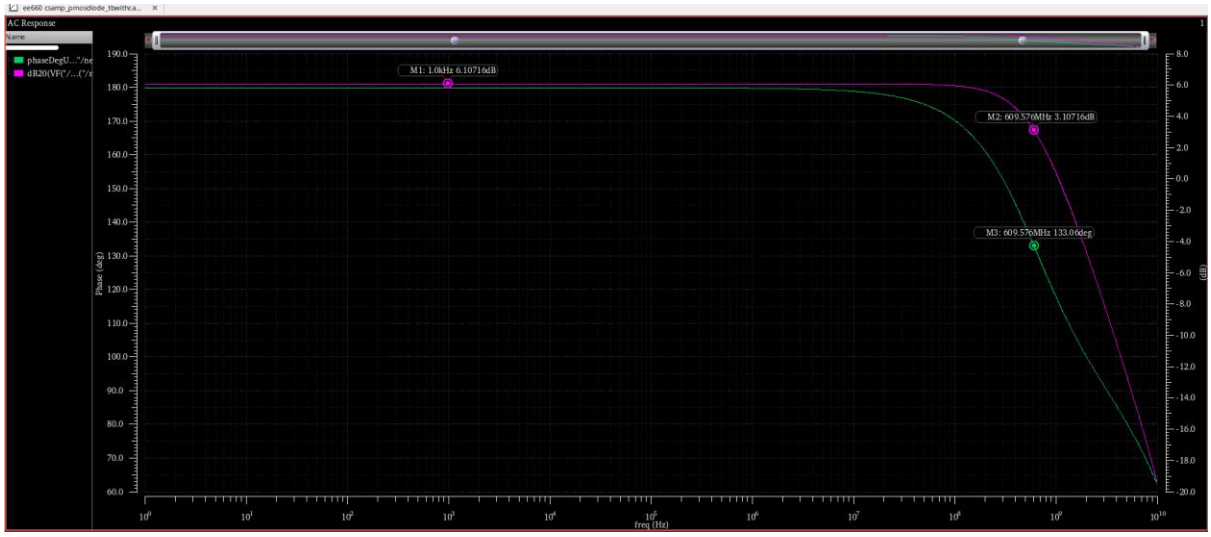

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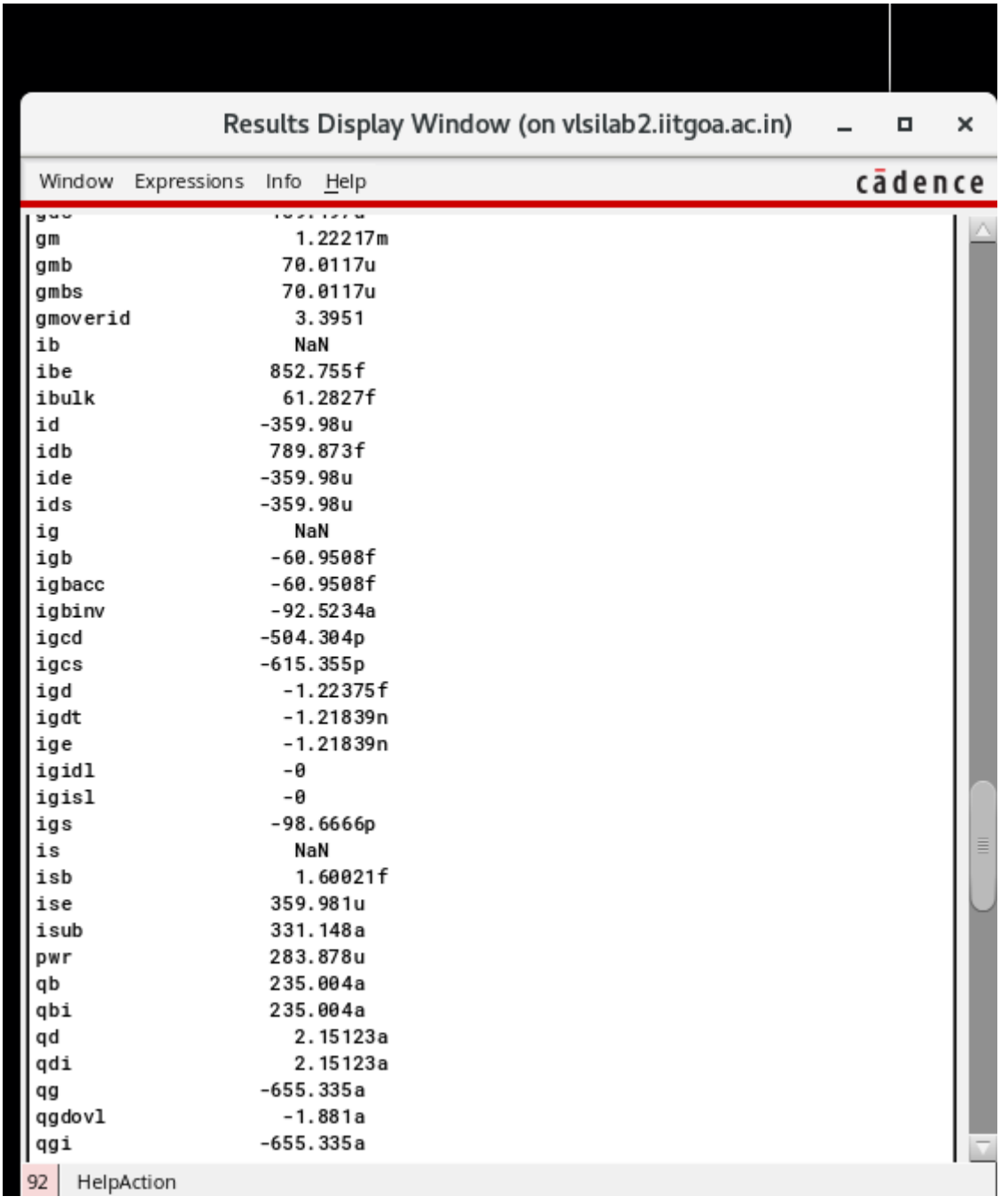

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