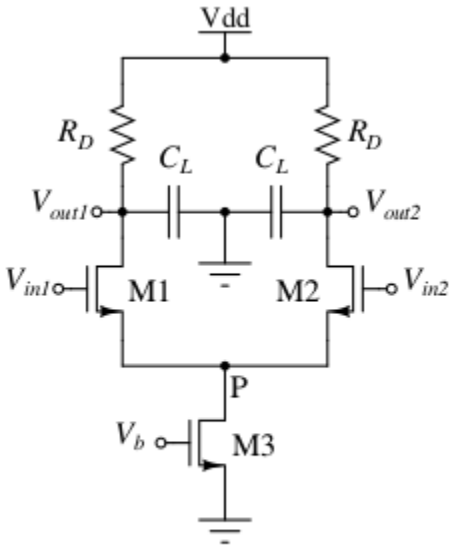
EE 660 VLSI Design Laboratory

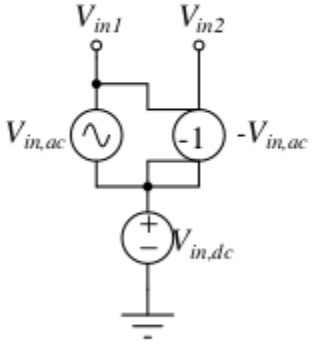
Assignment III

Submitted by: L Sri Sai Swathi (2414202)

1. Design an NMOS common-source differential amplifier with resistive load as shown in Fig. 1a. You can make use of UMC65 models for the transistors. Given (W/L) 1,2,3 = 6μ/0.06μ, R D = 1 kΩ, C L =100 fF, and V b = 0.55 V.



(a) Differential amplifier.



(b) Input source.

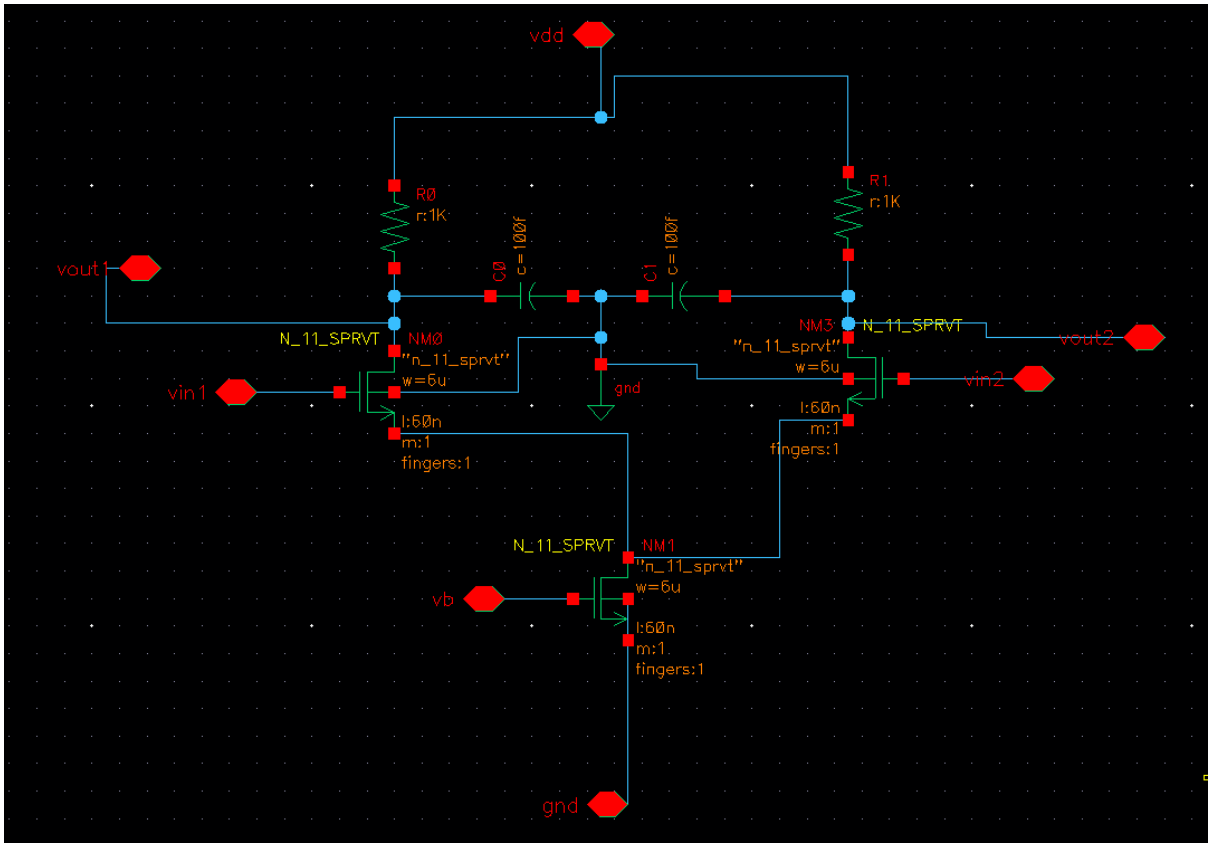


Figure: Schematic showing NMOS common-source differential amplifier with resistive load .

a) The configuration shown in Fig. 1b is used to generate the input for the amplifier. You can use the small signal amplitude of V in,ac to be 10 mV, and frequency to be 1 kHz. Decide the value of V in,dc , say (V b1), such that the differential gain is at least 2. Calculate the value of gm1 from the gain assuming the second order effects are absent.

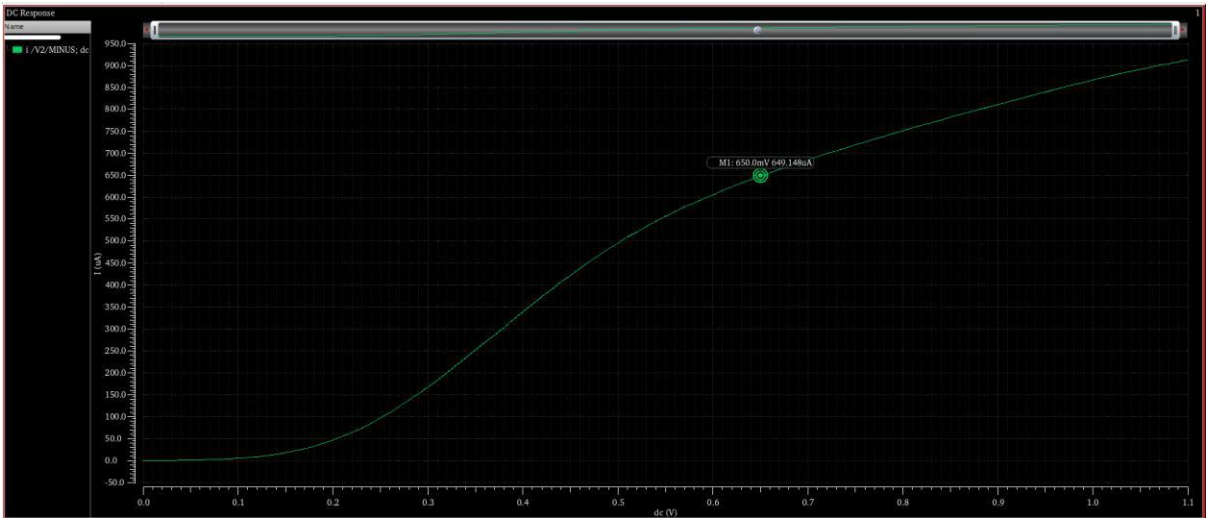


Figure:Plot showing vin dc vs I with vin dc as 500mv

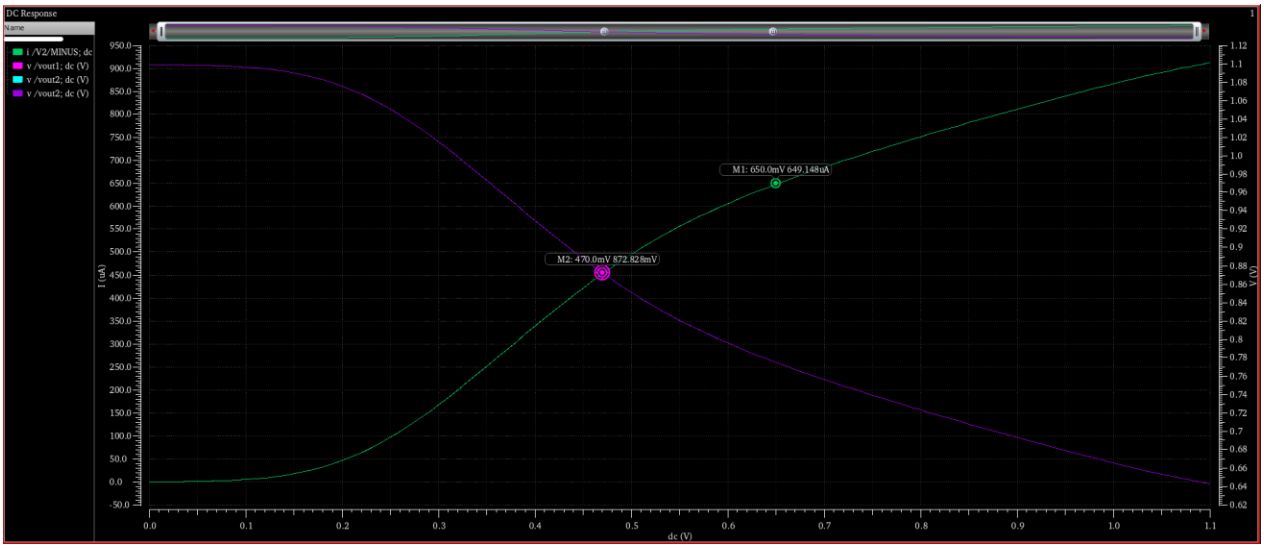


Figure:Plot showing vin dc vs I ,vout1,vout2 with vin dc as 500mv

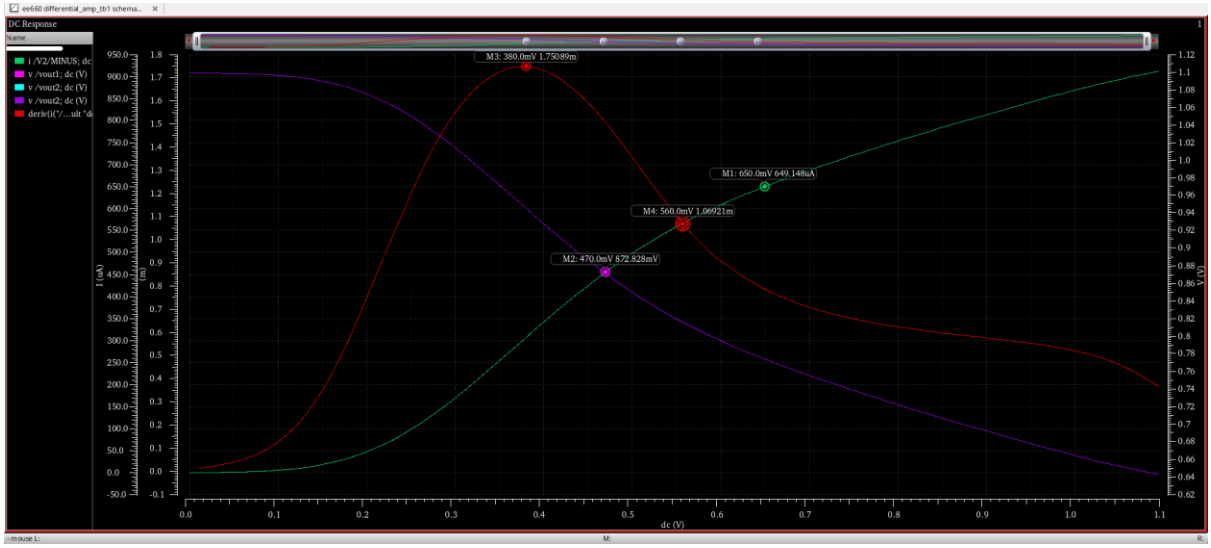


Figure:Plot showing vin dc vs I ,vout1,gm with vin dc as 500mv

Observation : From the plot gm is identified to be 1.75m seimens.

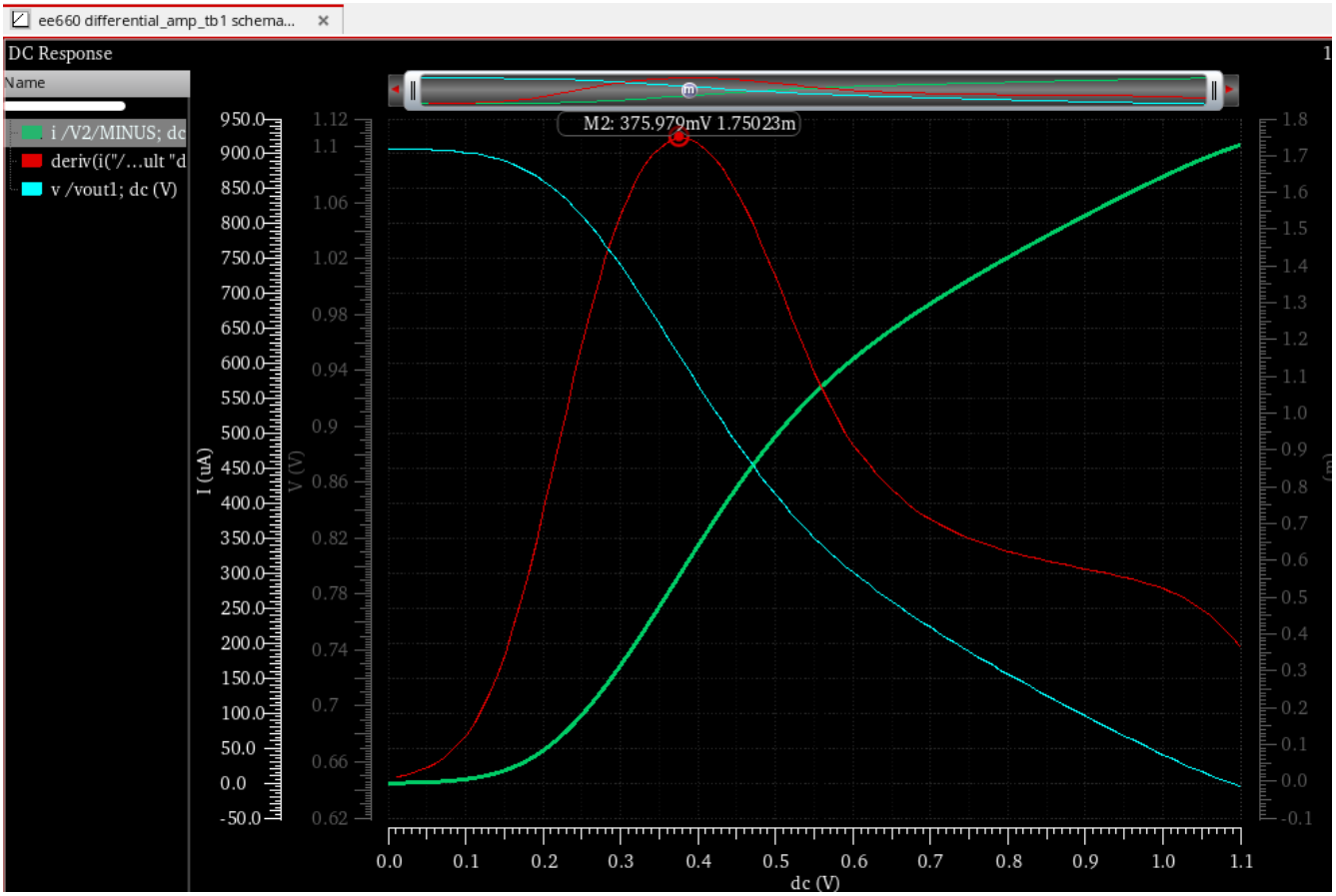


Figure:Plot showing I ,vout1,gm with vin dc as 650mv

We have also tried increasing vindc from 500mV to 750mV and observed gm to be 1.75mS.

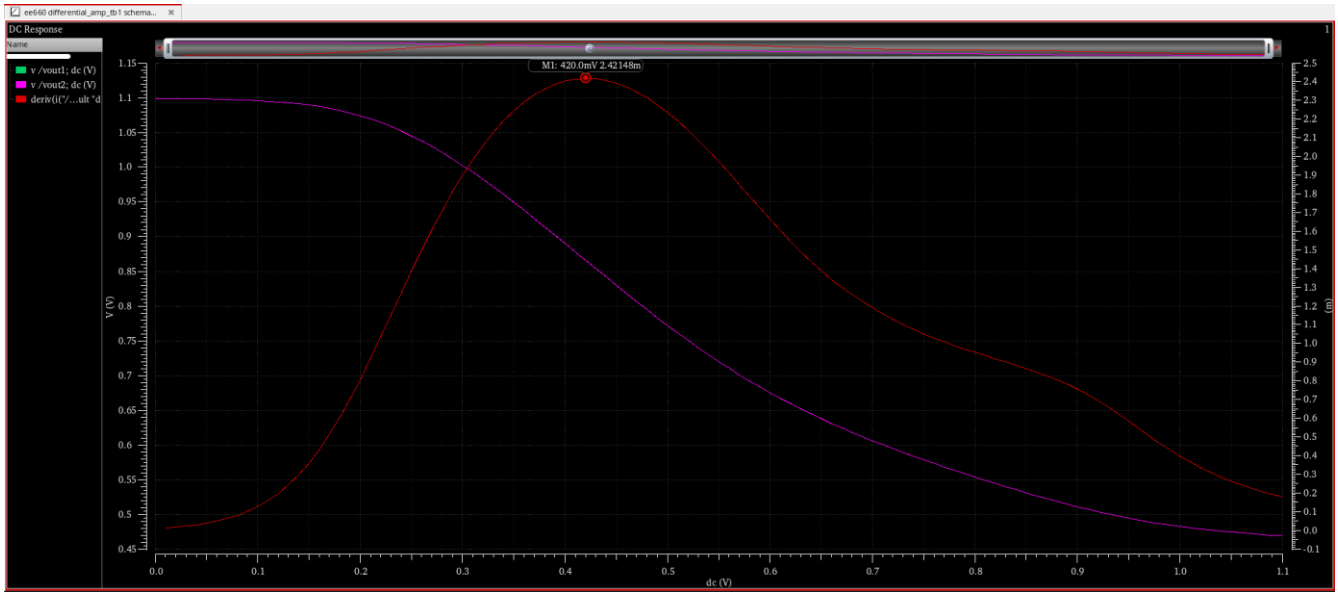


Figure:Plot showing d vout /d vindc .

*Observation: From the above plots , choosing 650mv as dc bias point.We have also observed that gm as **1.75mS**. And dvout/dvin as **2.4***

Below are the simulation results of DC operating point analysis at dc voltage 0.5v

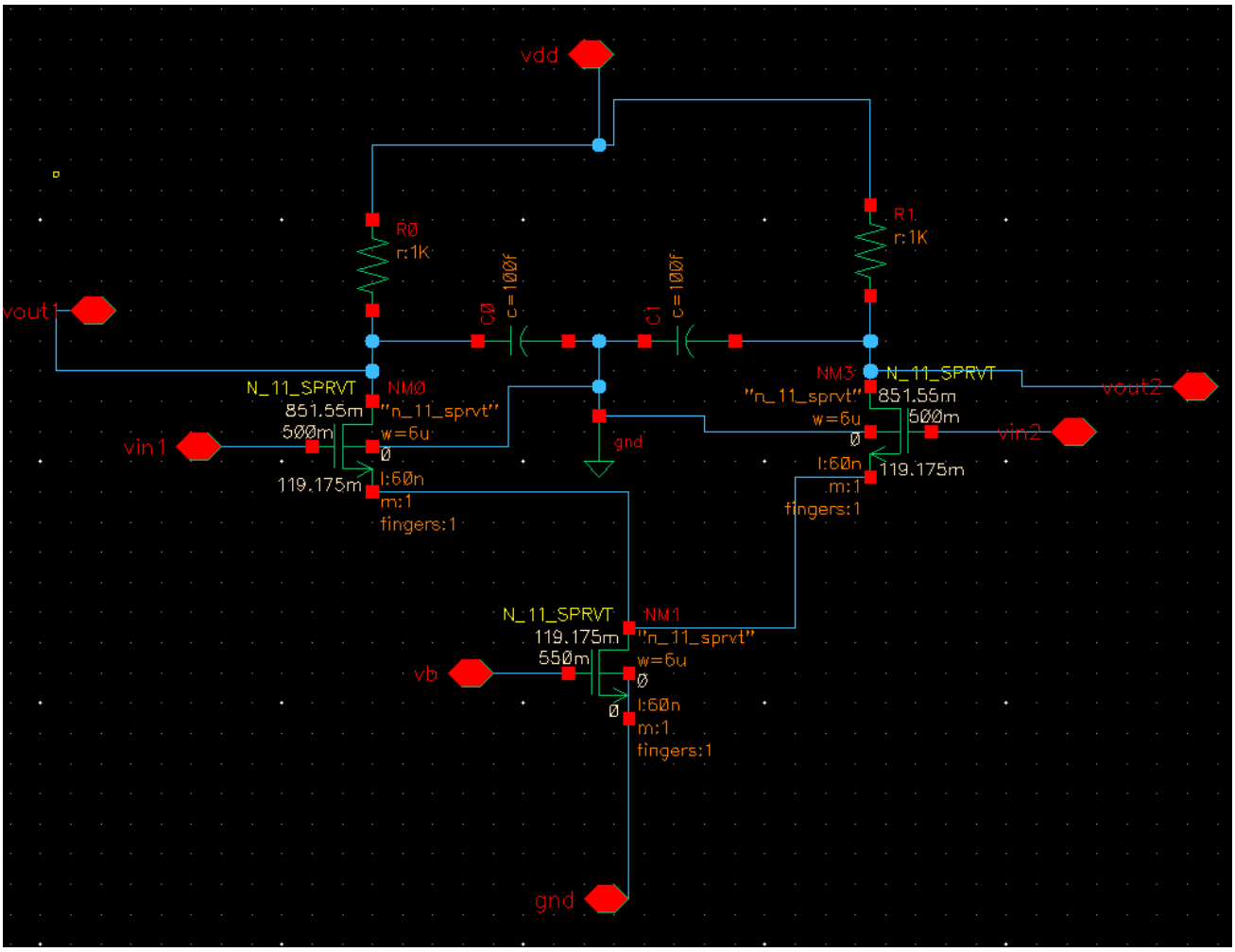


Figure: Schematic showing NMOS common-source differential amplifier with resistive load with all the operating point values.

Simulation result of first mosfet M1 :

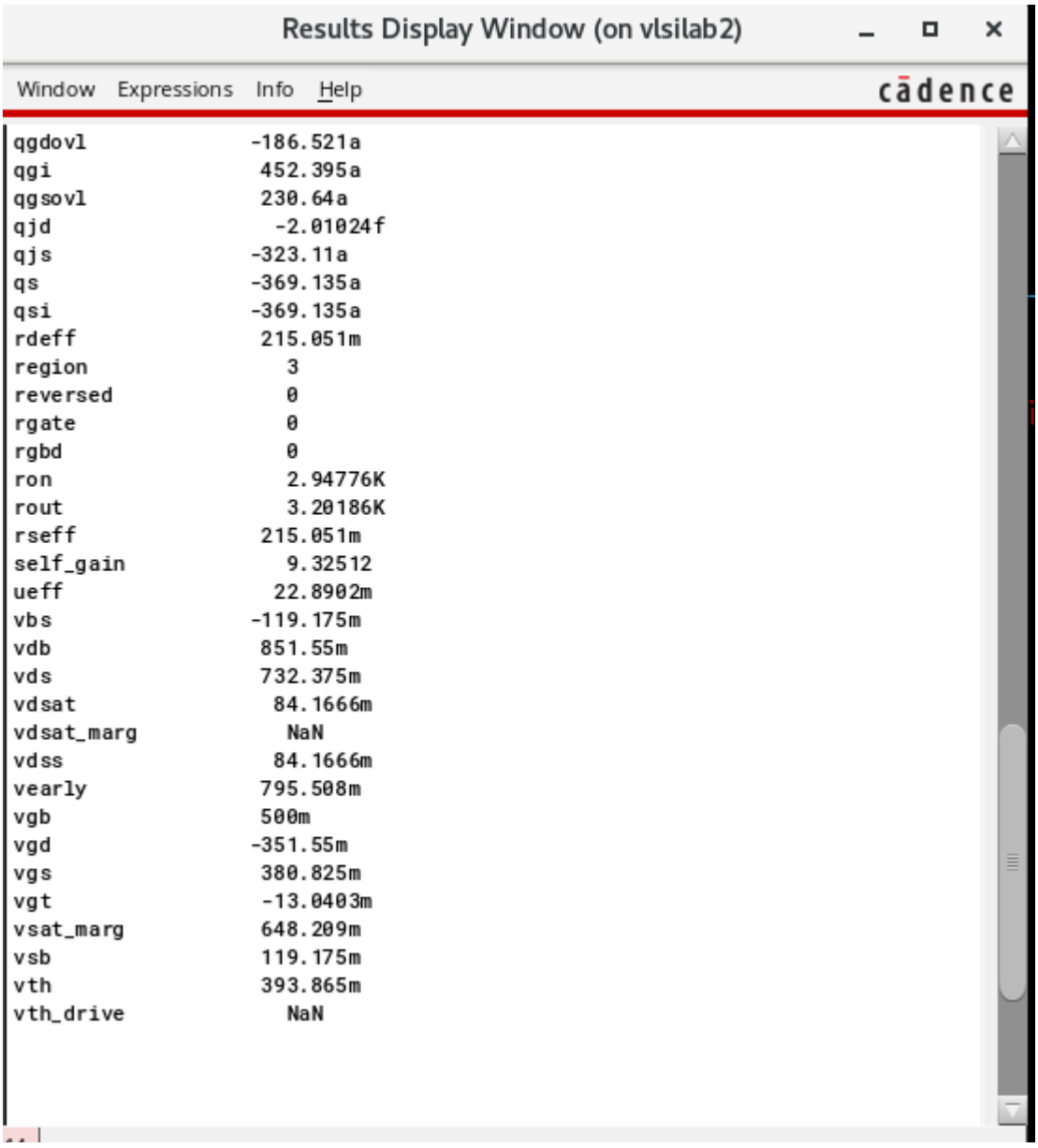


Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 3 at vindc =500mv

Simulation result of mosfet M2 :

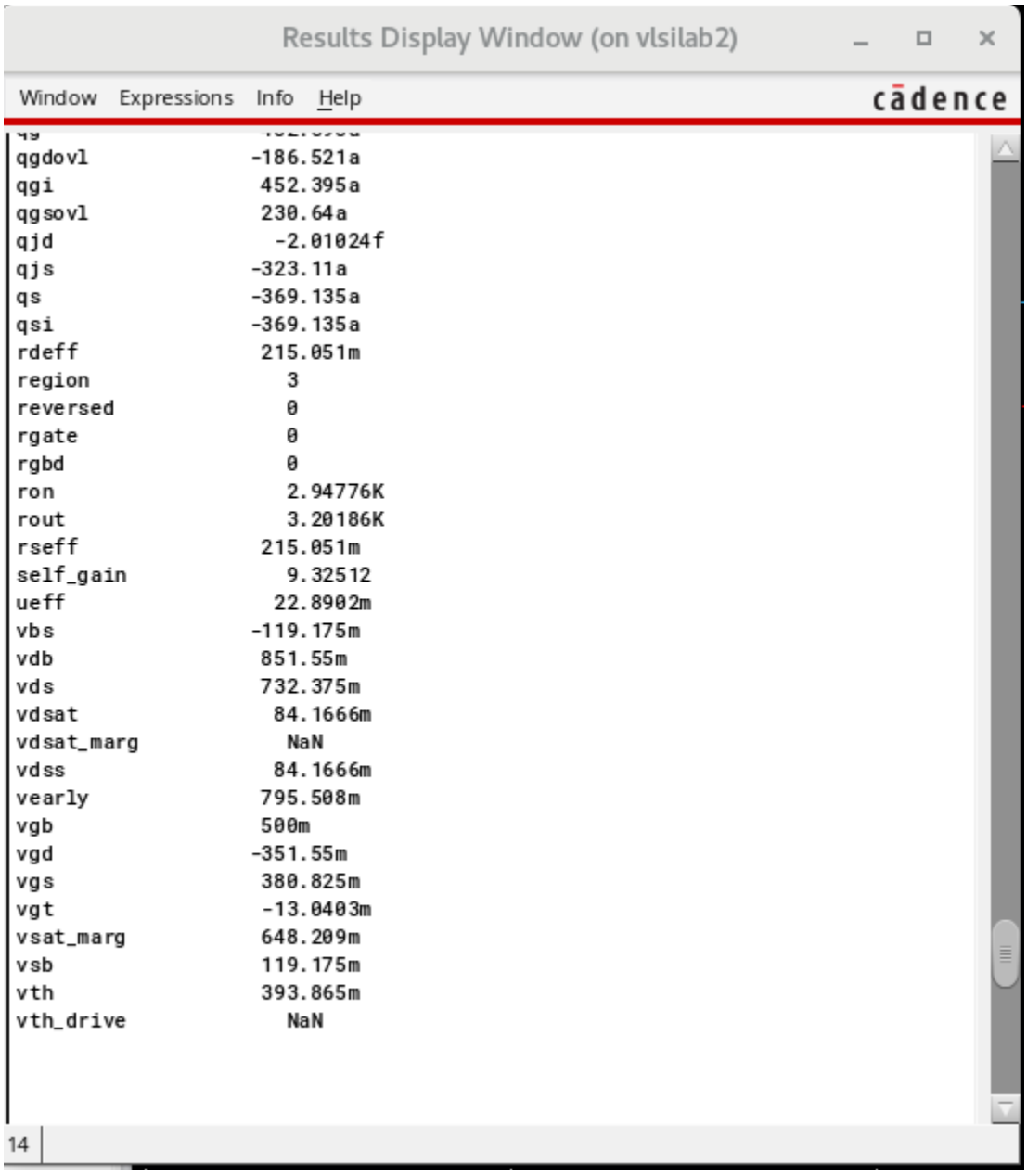


Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 3 at vindc =500mv

Simulation result of mosfet M3 :

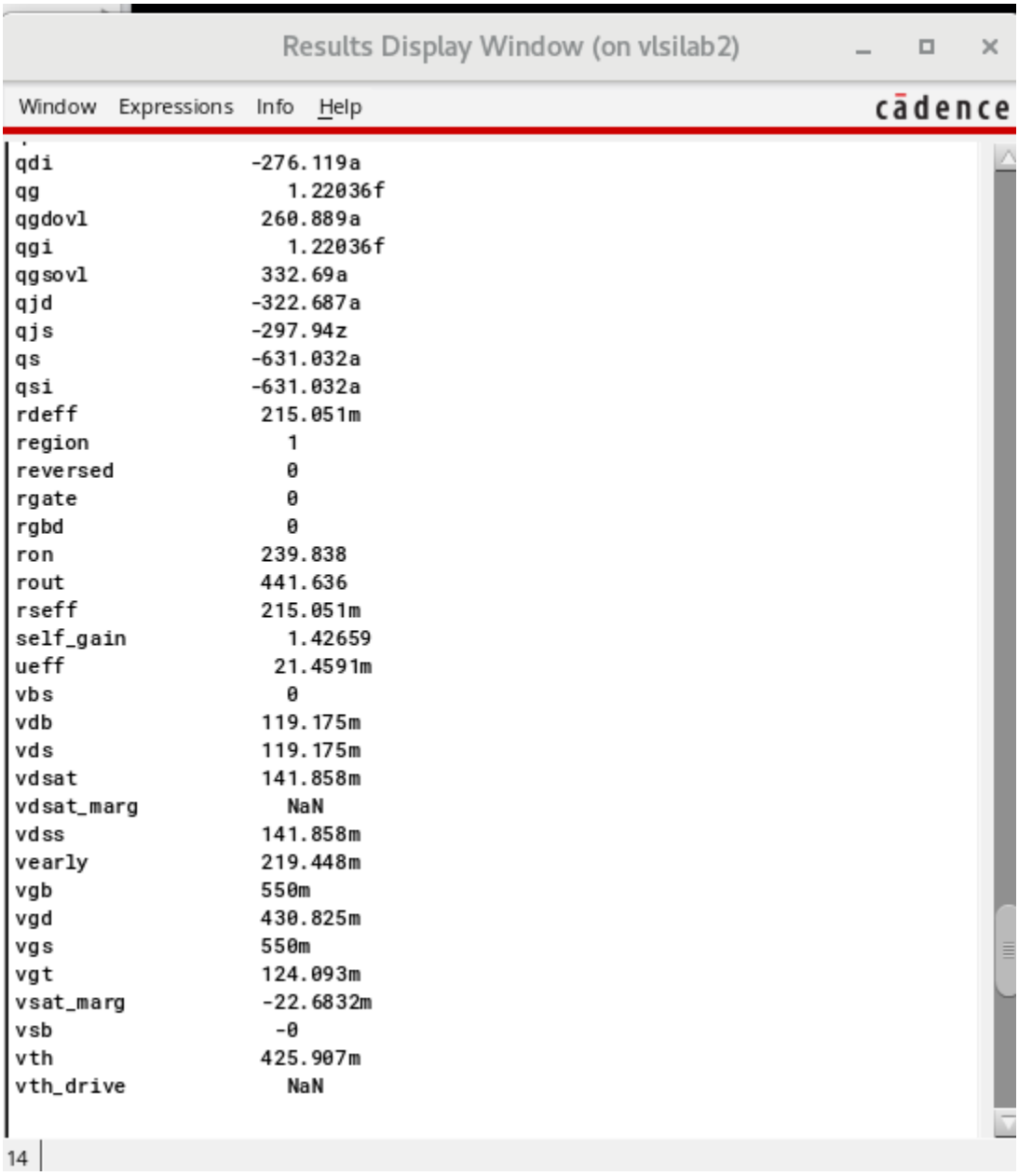


Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 1 at vindc =500mv. Since all 3 are not in saturation increasing vin, dc to 650mv.

Below are the simulation results of DC operating point analysis at dc voltage 650mv:

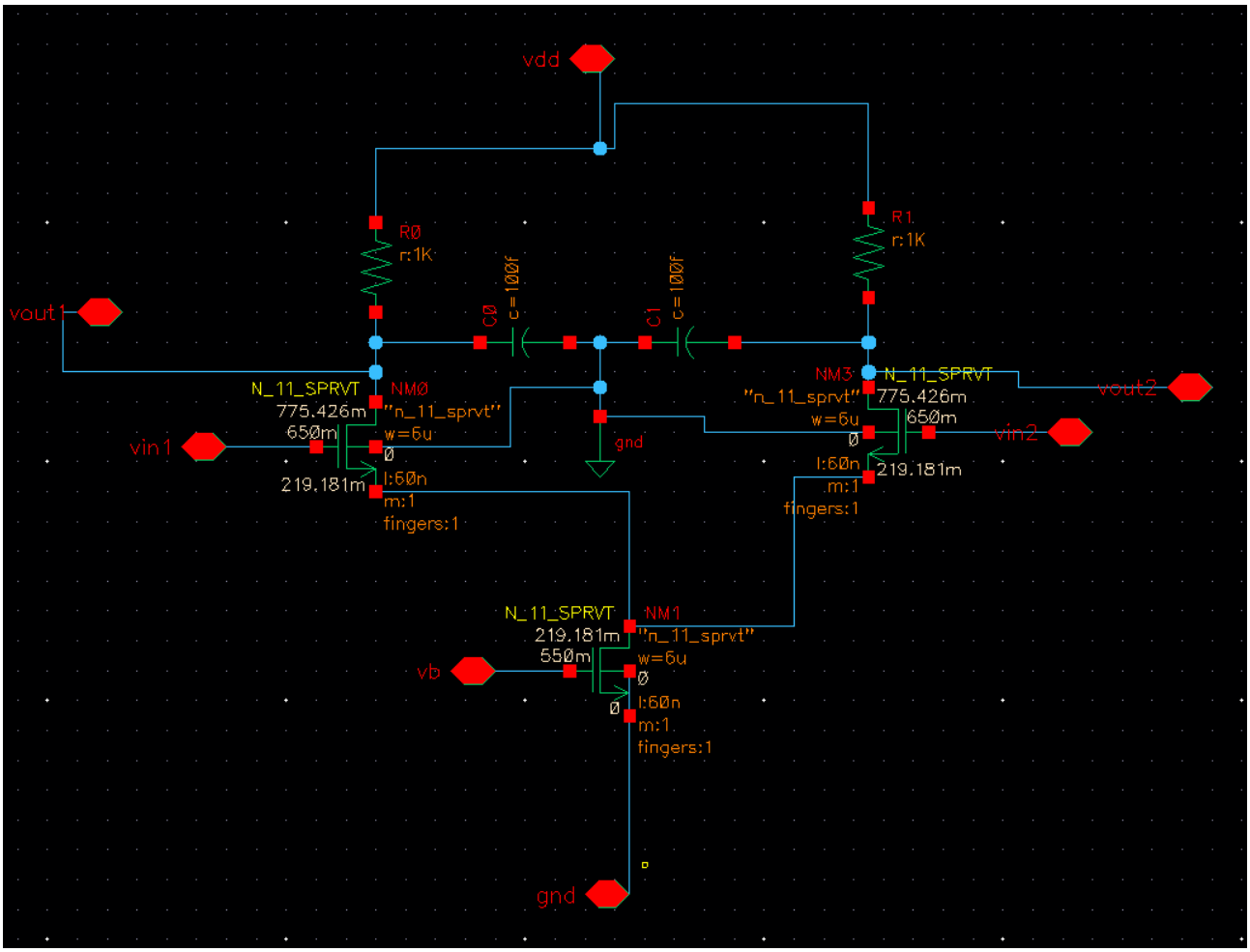


Figure: Schematic showing NMOS common-source differential amplifier with resistive load with all the operating point values.

Simulation result of first mosfet M1 :

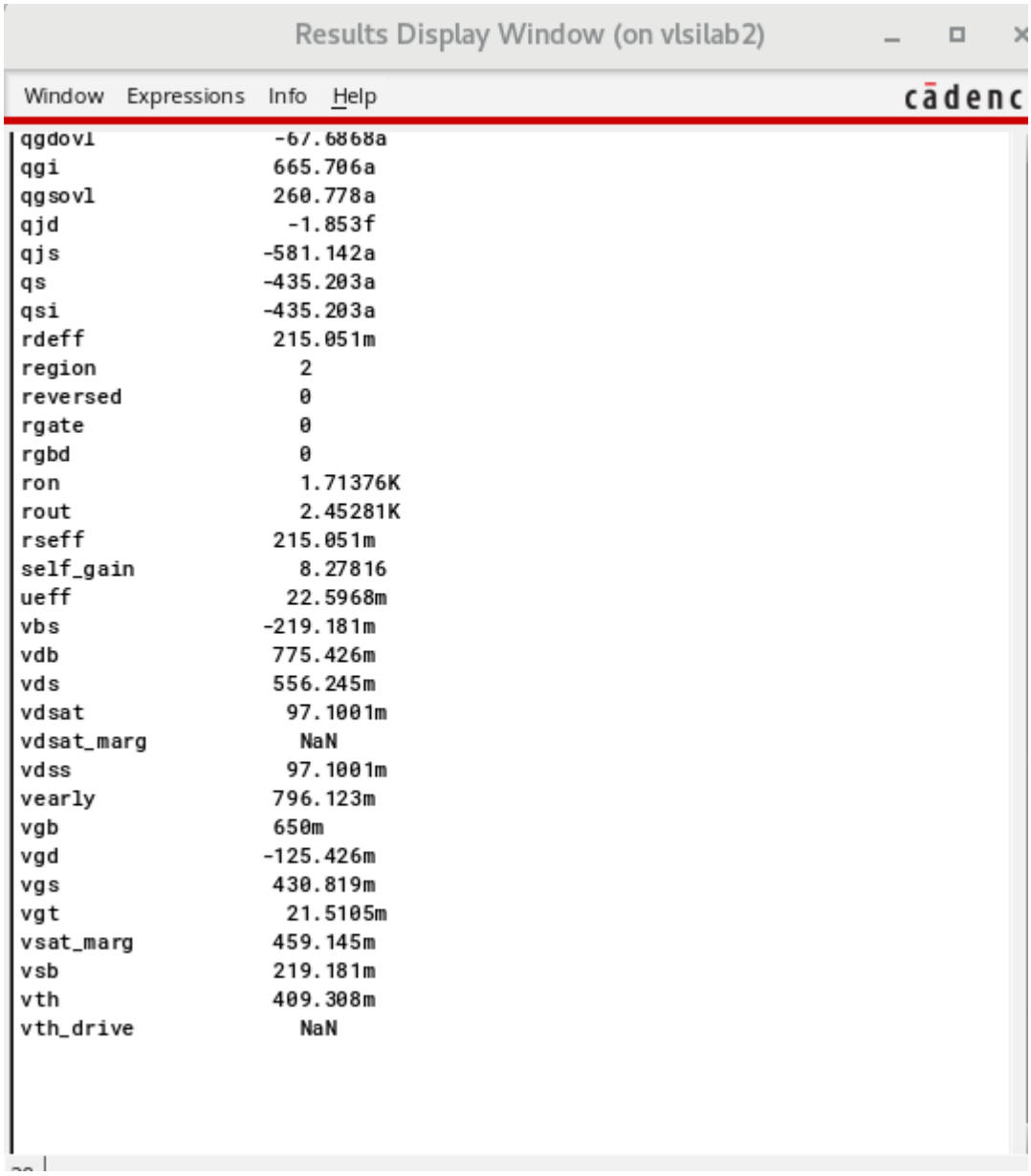


Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 at vindc =650mv

Simulation result of mosfet M2 :

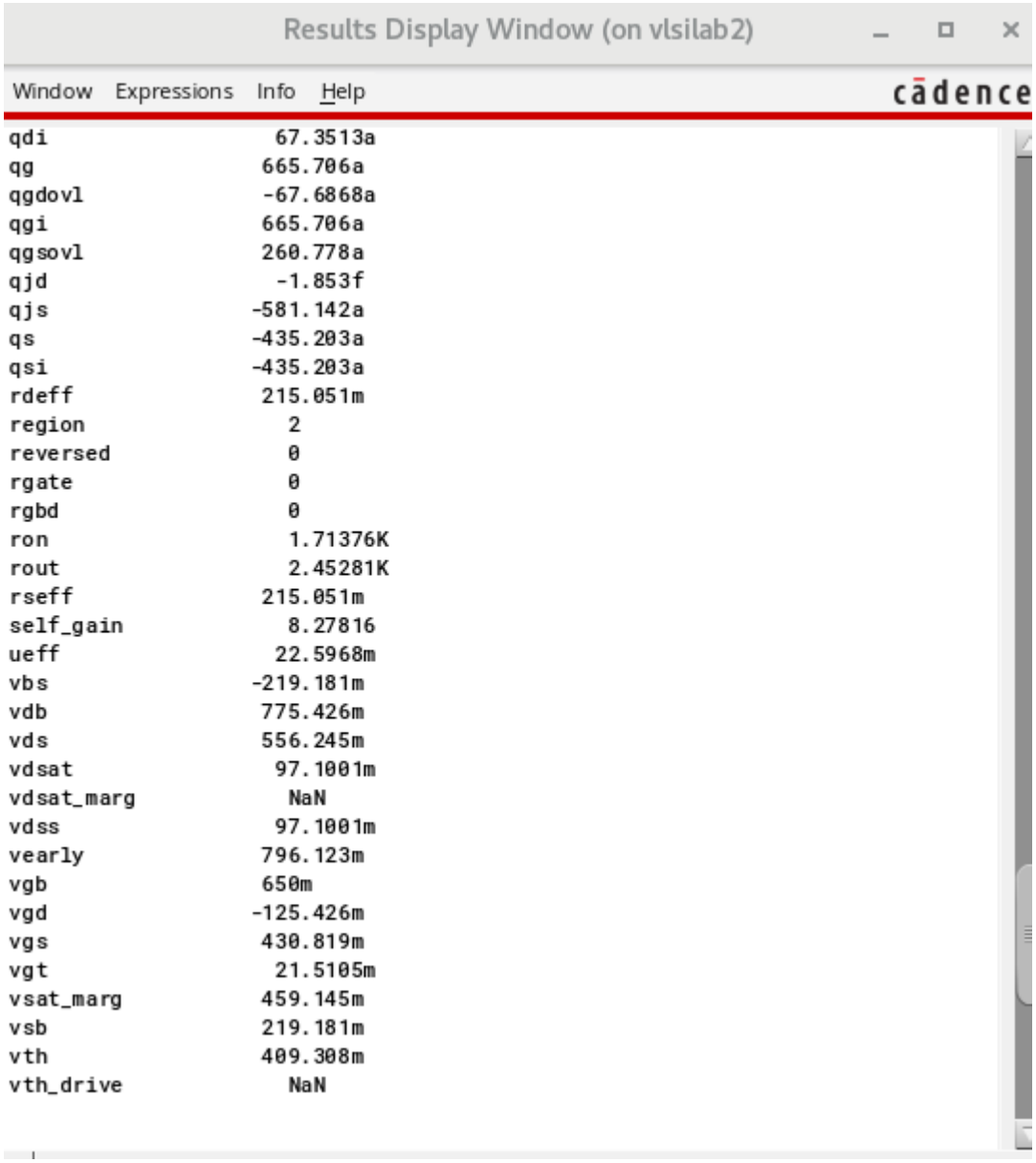


Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 at vindc =650mv

Simulation result of mosfet M3:

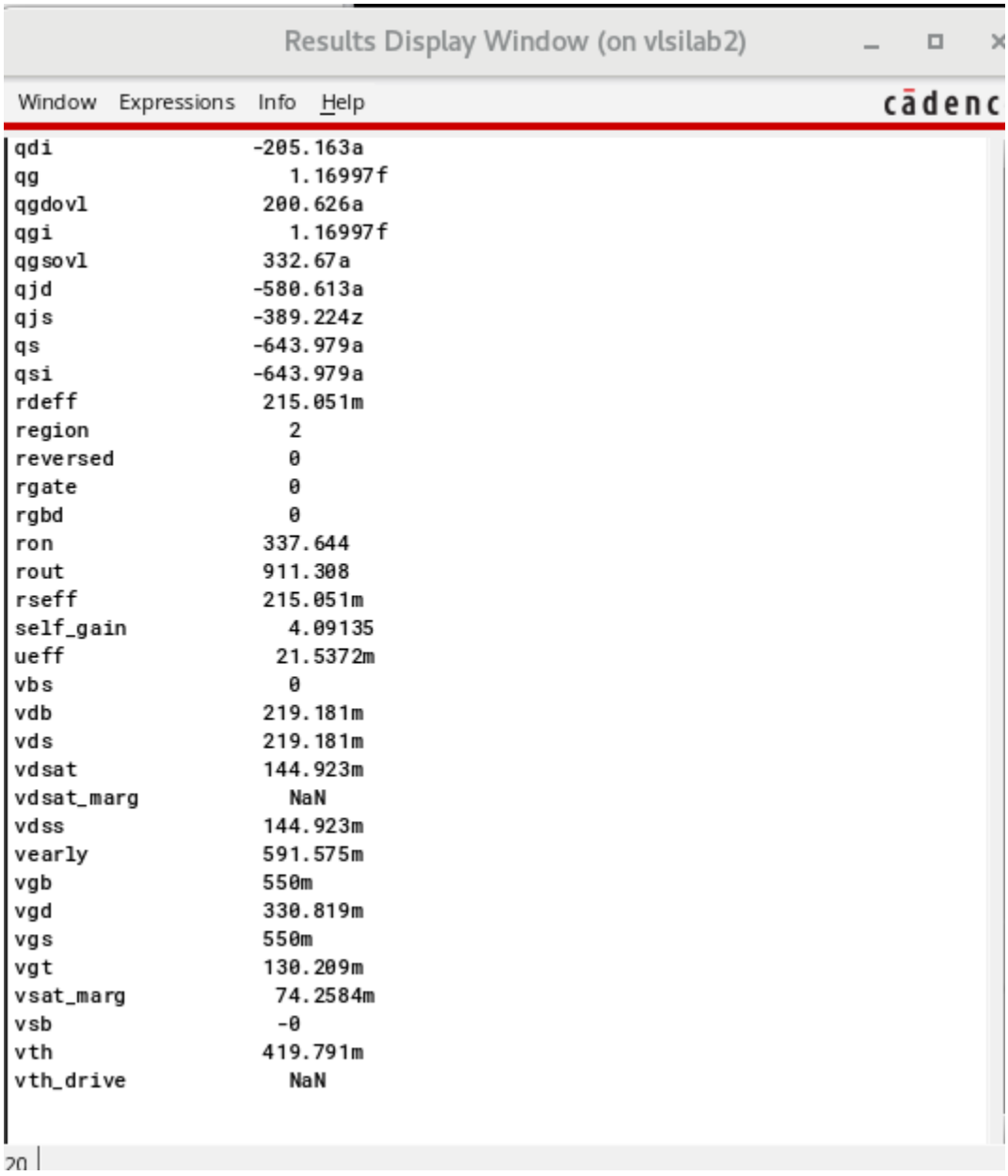


Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 at vindc =650mv. It is observed that all the 3 mosfets are in saturation region .i.e region2

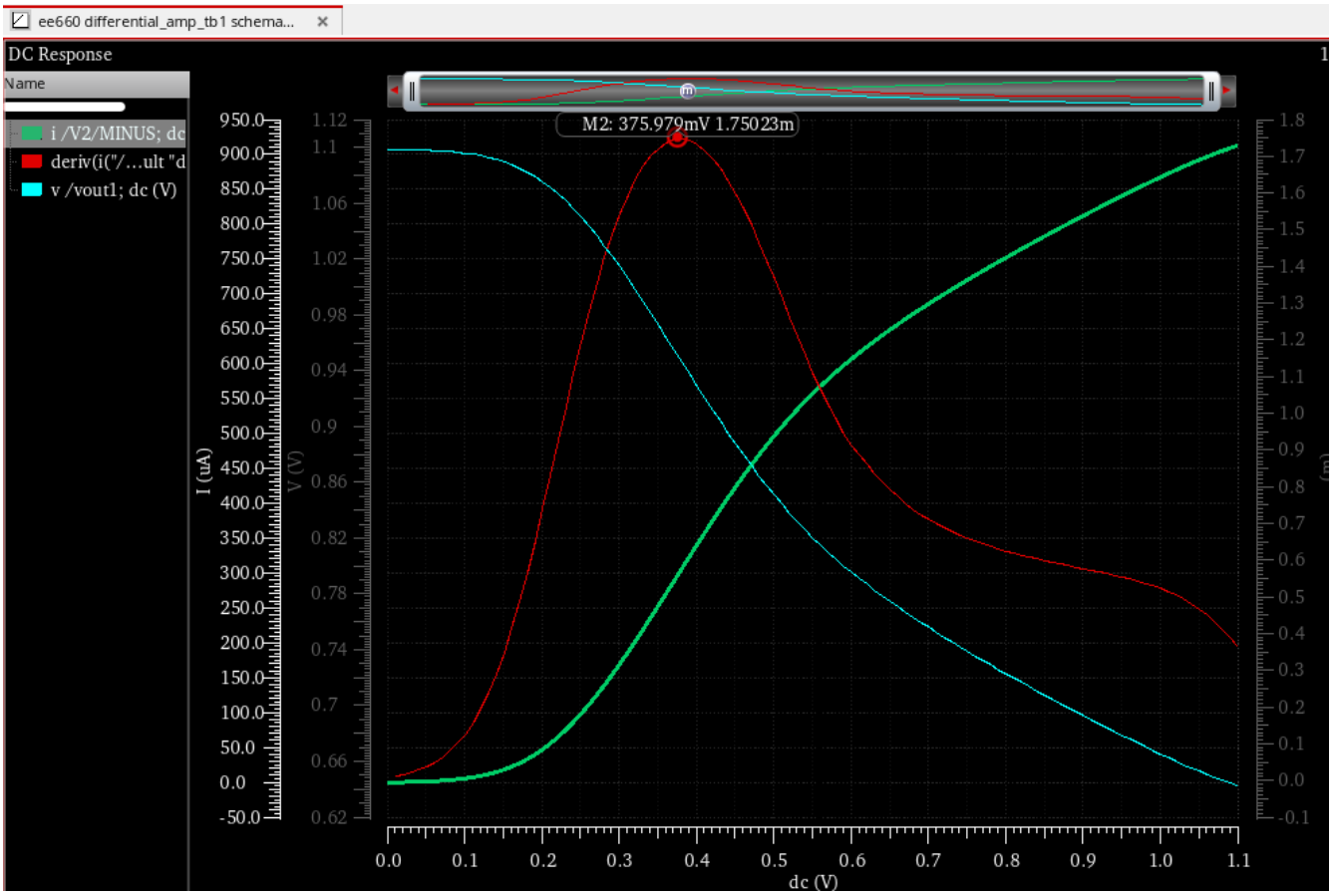


Figure:Plot showing I ,vout1,gm with vin dc as 650mv

(b) Perform the operating point analysis with V in,dc = V b1 and check if all the transistors are in
saturation region of operation. If not, find out another value for V b1 . Calculate V out1,max and V out1,min , and hence the maximum differential output voltage swing. From this calculate the maximum input swing that can be applied to the amplifier

Performed transient analysis at Vin,dc=650mV ,small signal voltage is 10mV,frequency =1KHz

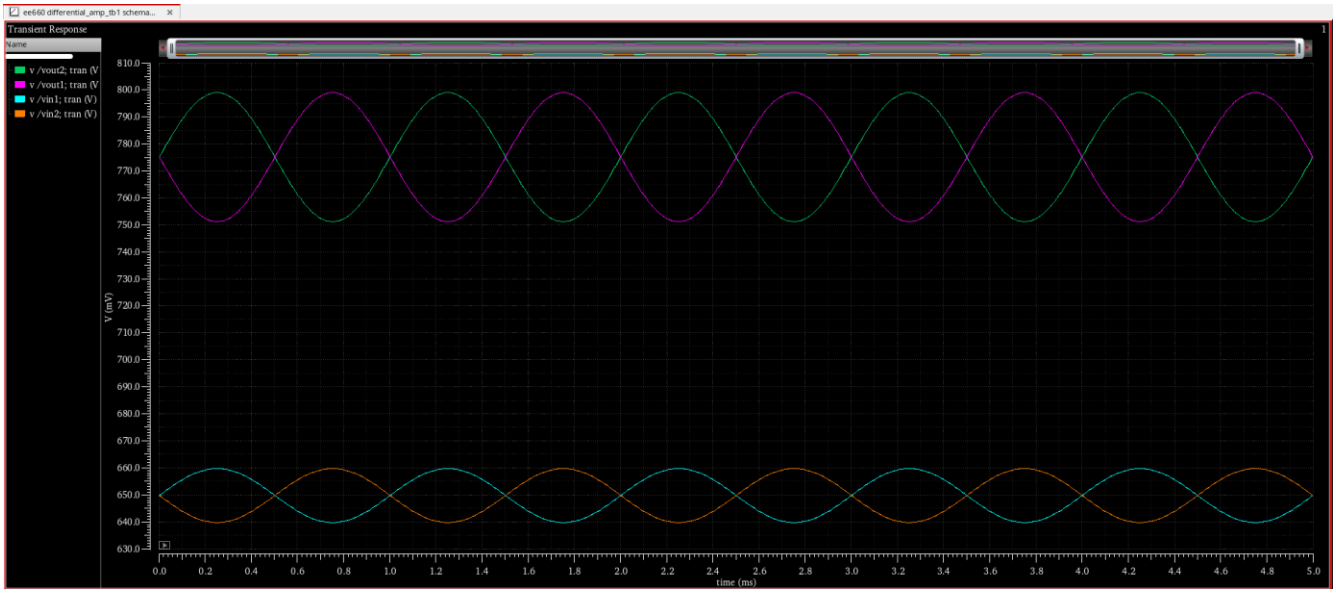


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

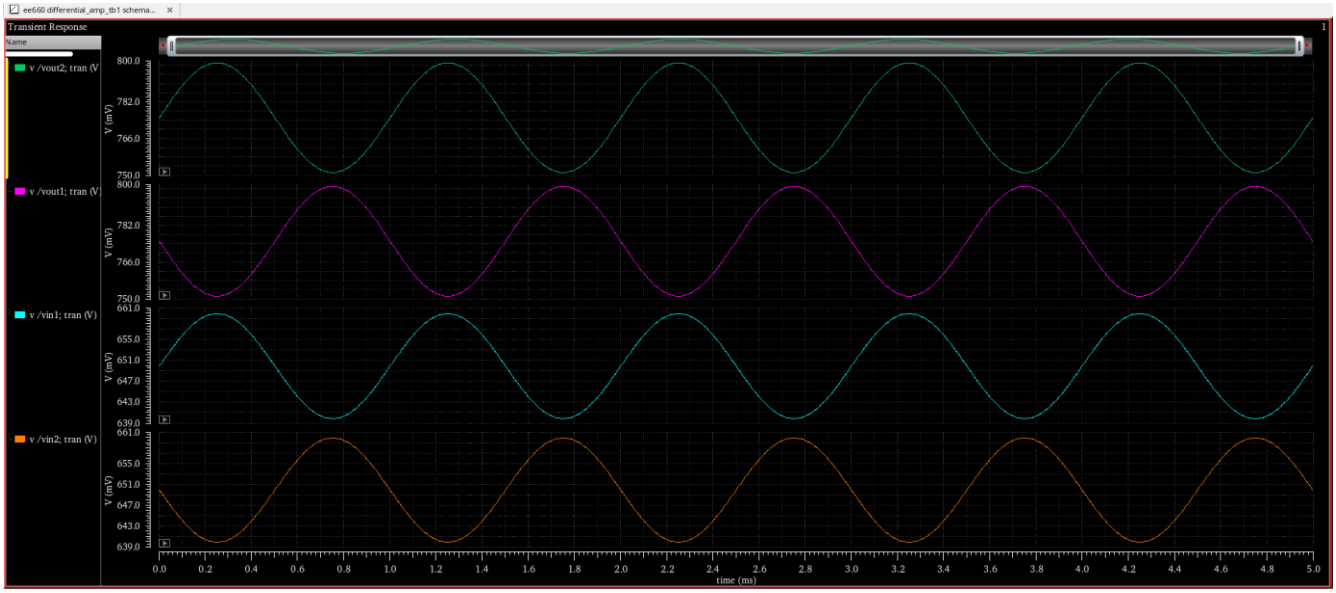


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

***Observation**:From the above plot it is evident that Vin1 ,Vout1 are out of phase and Vin2 ,Vout2 are out of phase.*

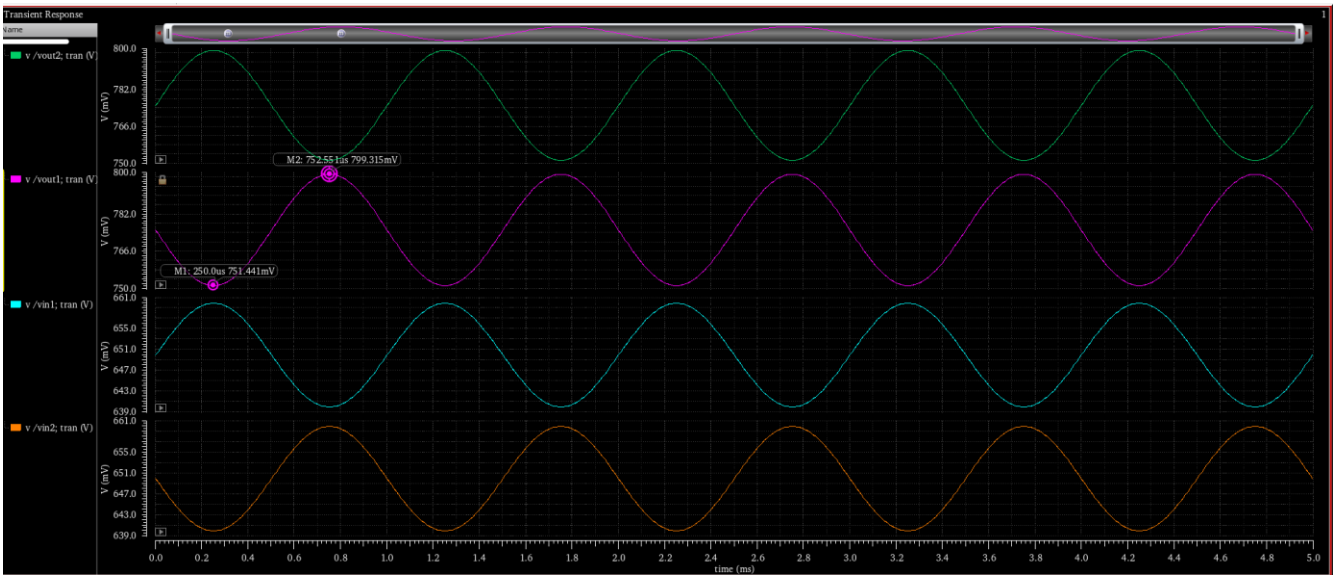


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

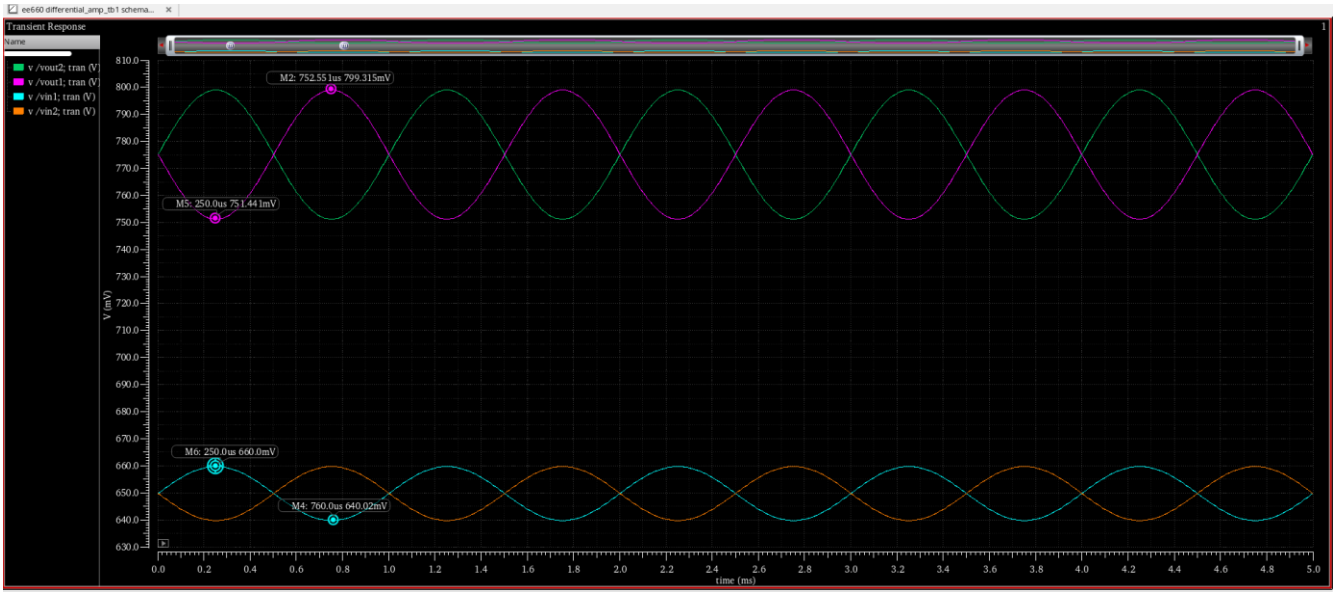


Figure:Plot showing Vin1, Vout1 with min and max points highlighted

Observation:

Vout1max=799.31mV
Vout1min= 751.44mv
Vout,swing=47.87mV
Vdiff swing =2x(Vout1max-vout1min)=2 x47.87=95.74mV
Vin,pp=20mv
Av =Vout1,pp/ Vin,pp = 2.39
Vin,swing =vout,swing /2.39=20mV

(c) Perform the AC analysis of the circuit and find out the 3 dB frequency. What is the phase difference between the input and output at this cut-off frequency? Is it possible for you to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios?

Below are simulation results of the AC response analysis :

Figure: Plot showing Ac response analysis results (Vout1,Vin1 considered)

Observations:From the above Ac Analysis plots we can say that :
1.Low frequency gain is **7.589dB**
2. 3dB cuttoff frequency is **2.157GHz**
3.Phase difference between the input and output at the 3 dB frequency: **134.72Degrees.**

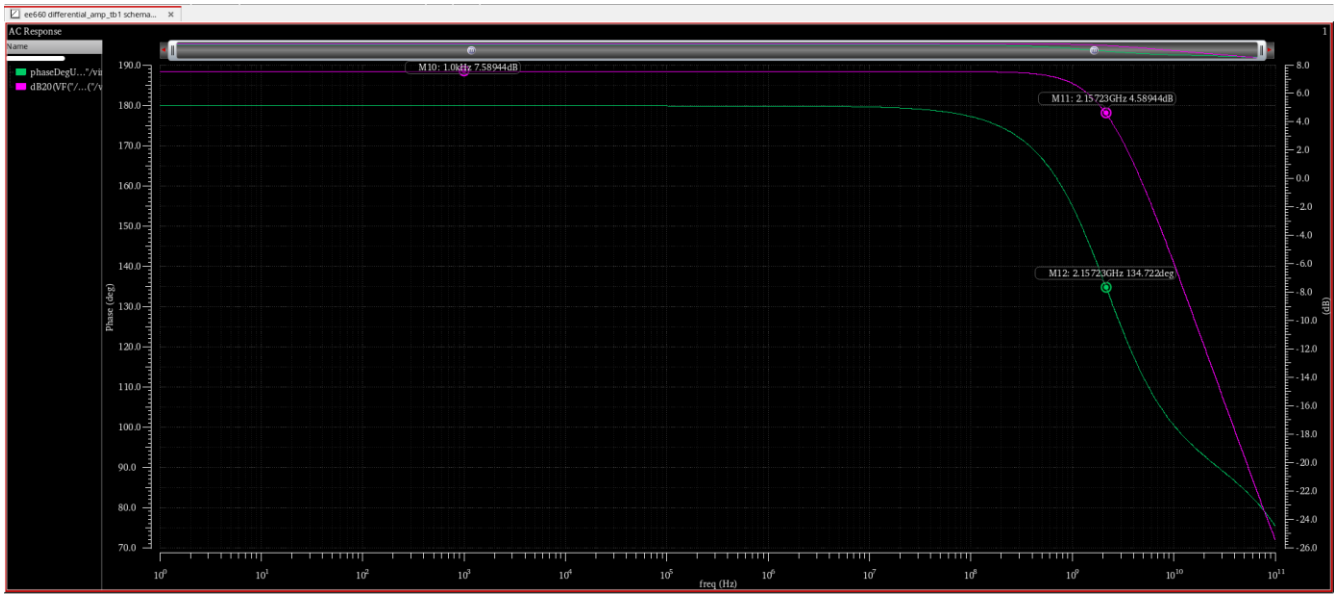


Figure: Plot showing Ac response analysis results (Vout2,Vin2 considered)

AC response Vout2,vin2

Observations:From the above Ac Analysis plots we can say that :

1.Low frequency gain is **7.589dB**

2. 3dB cuttoff frequency is **2.157GHz**

3.Phase difference between the input and output at the 3 dB frequency: **134.72Degrees.**

Is it possible for you to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios?

Trial 1: When RD is increased from 1k to 1.5k

Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plots we can say that :
1.Low frequency gain is **9.424dB**
2. 3dB cuttoff frequency is 1**.689GHz**

Bandwidth got reduced.

Trial 2: Changed Aspect ratios i.e **M1,M2** has width 9um and **M3** has width 8um

Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plots we can say that :
1.Low frequency gain is **9.33dB**
2. 3dB cuttoff frequency is **2.43GHz**

Trial 3:when all three transistors has width as 9um

Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plot we can say that :

1.Low frequency gain is **9.48dB**

2. 3dB cuttoff frequency is **2.53GHz**

Trial4 :when m1 ,m2 has w =6um and m3 has w =9um

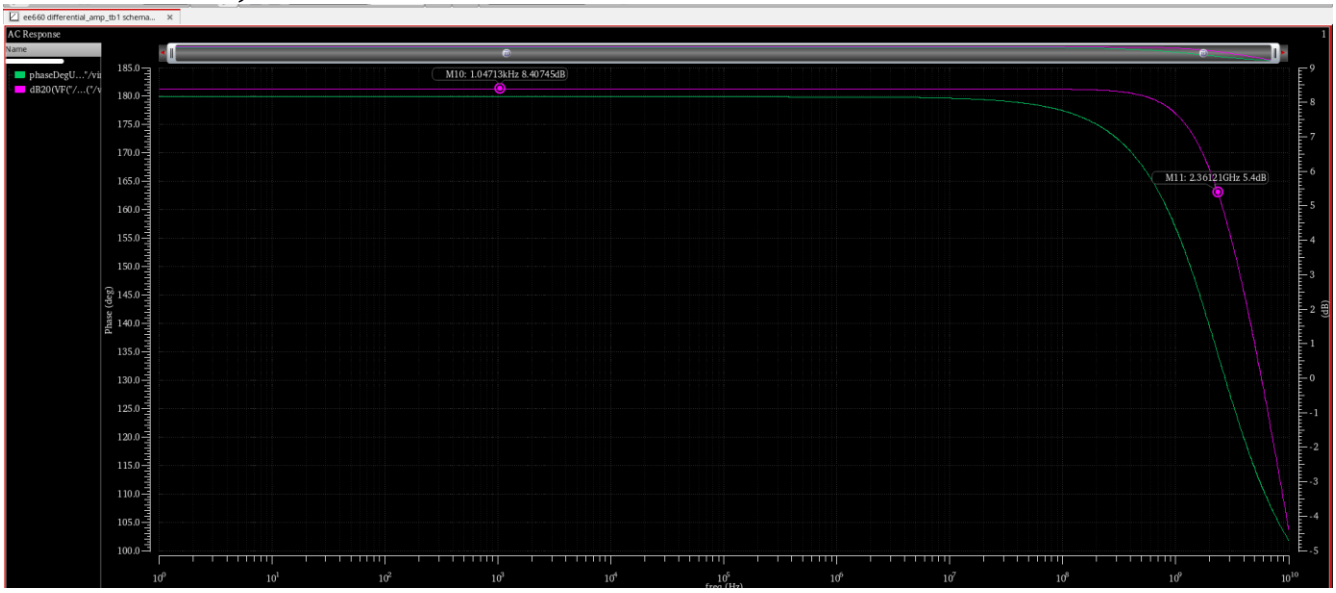


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

1.Low frequency gain is **8.40dB**

2. 3dB cuttoff frequency is 2.36GHz

Trial5 :when m1 ,m2 ,m3 has w =9um and Rd=0.5Kohms

Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observation:

1.Low frequency gain is 6.08**dB**

2. 3dB cuttoff frequency is 3.94GHz

Conclusion: It is not possible for us to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios

(d) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Performed transient analysis at Vin,dc=650mV ,small signal voltage is 10mV,frequency =1KHz

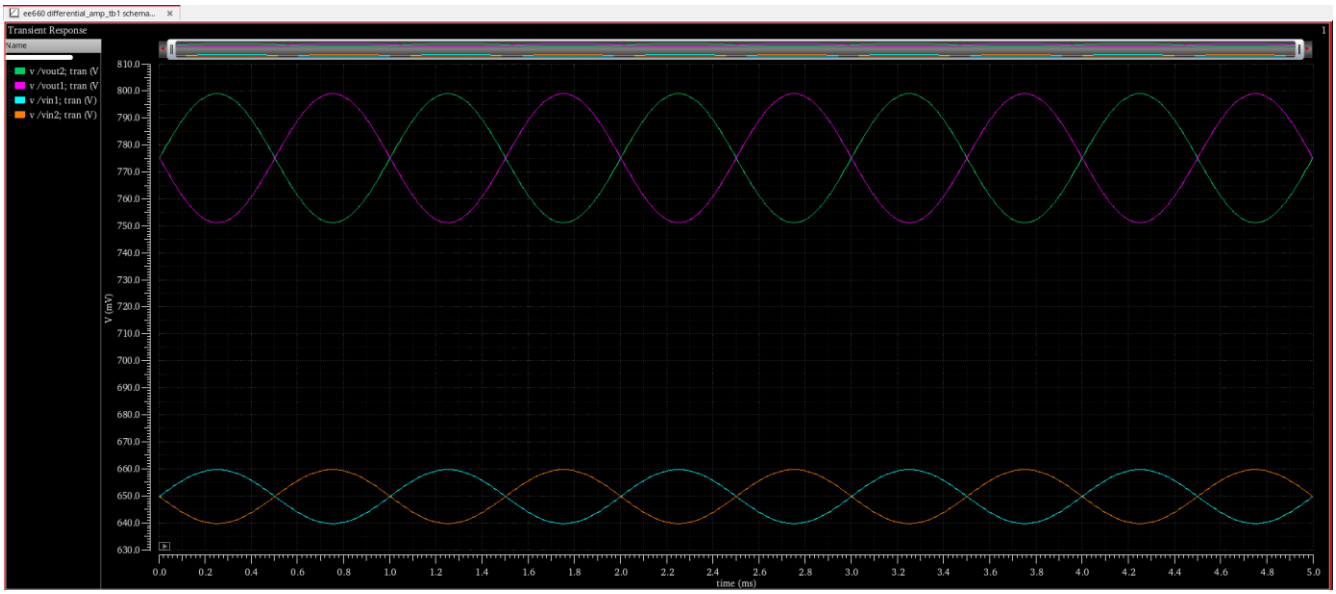


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

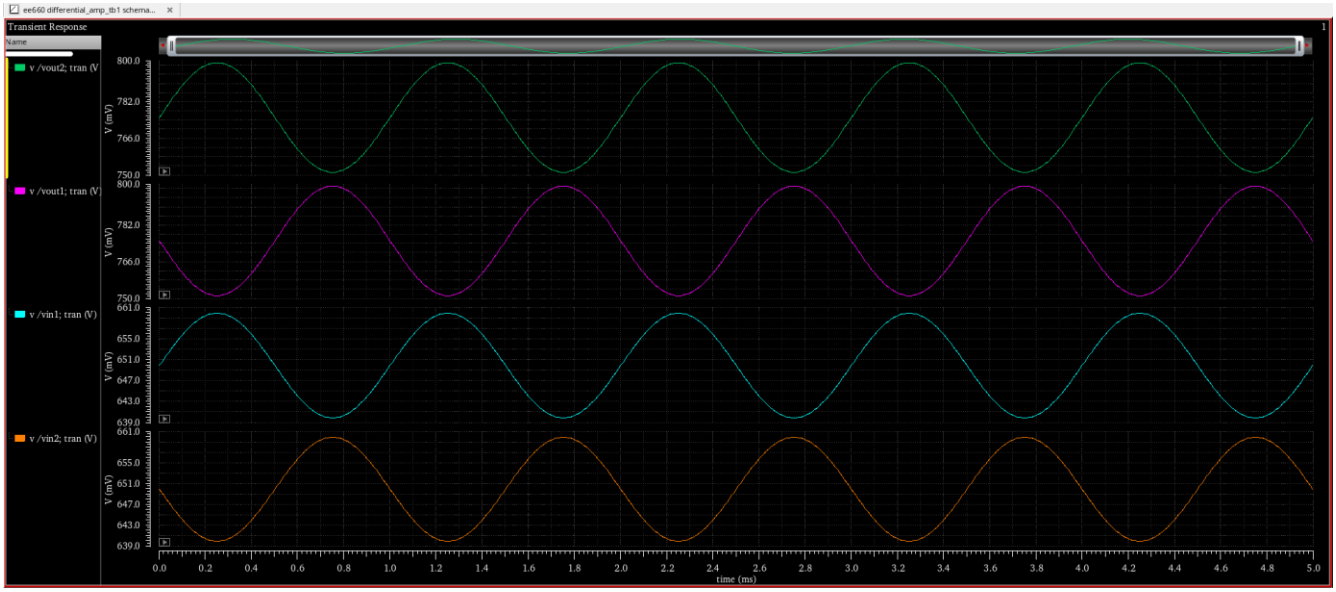


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

***Observation**:From the above plot it is evident that Vin1 ,Vout1 are out of phase and Vin2 ,Vout2 are out of phase.*

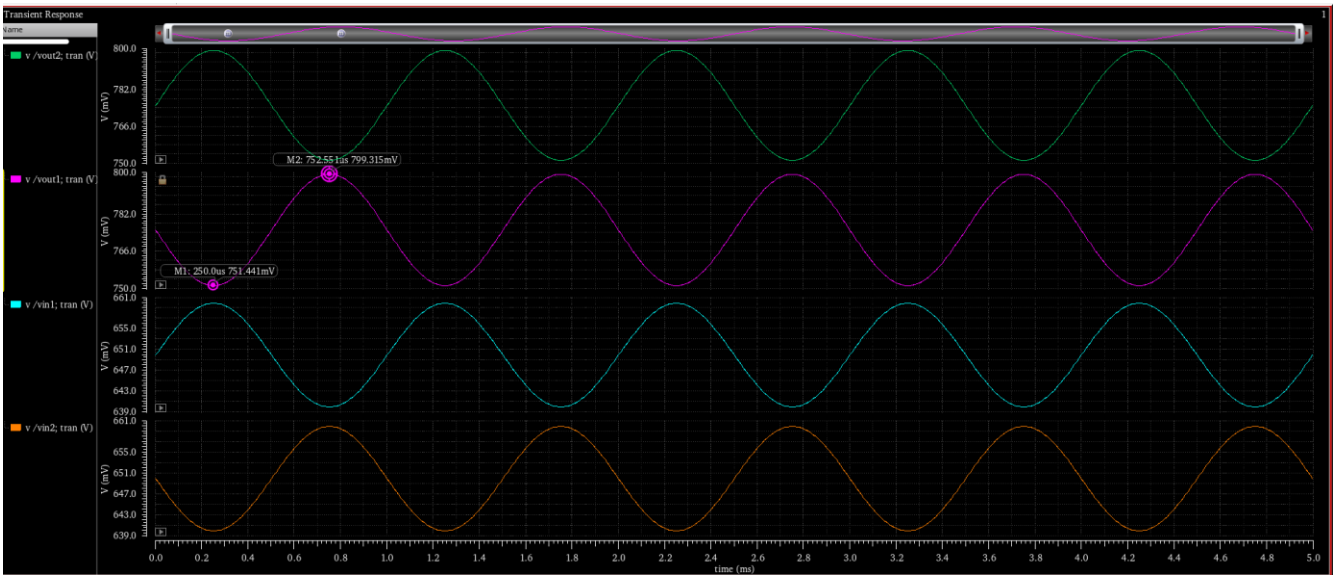


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

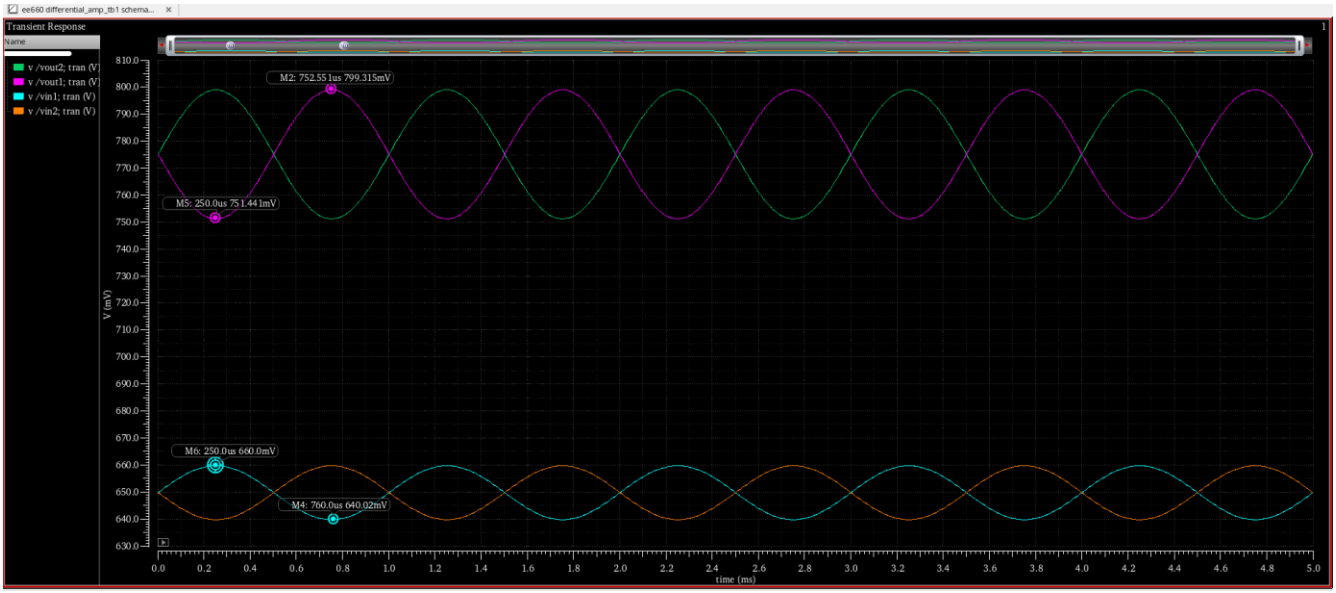


Figure:Plot showing Vin1, Vout1 with min and max points highlighted

Observation:

Vout1max=799.31mV

Vout1min= 751.44mv

Vdiff swing =2x(Vout1max-vout1min)=2 x47.87=95.74mV

Vin,pp=20mv

Av =Vout1,pp/ Vin,pp = 2.39

Below are the results when input small signal input voltage is 20mV:

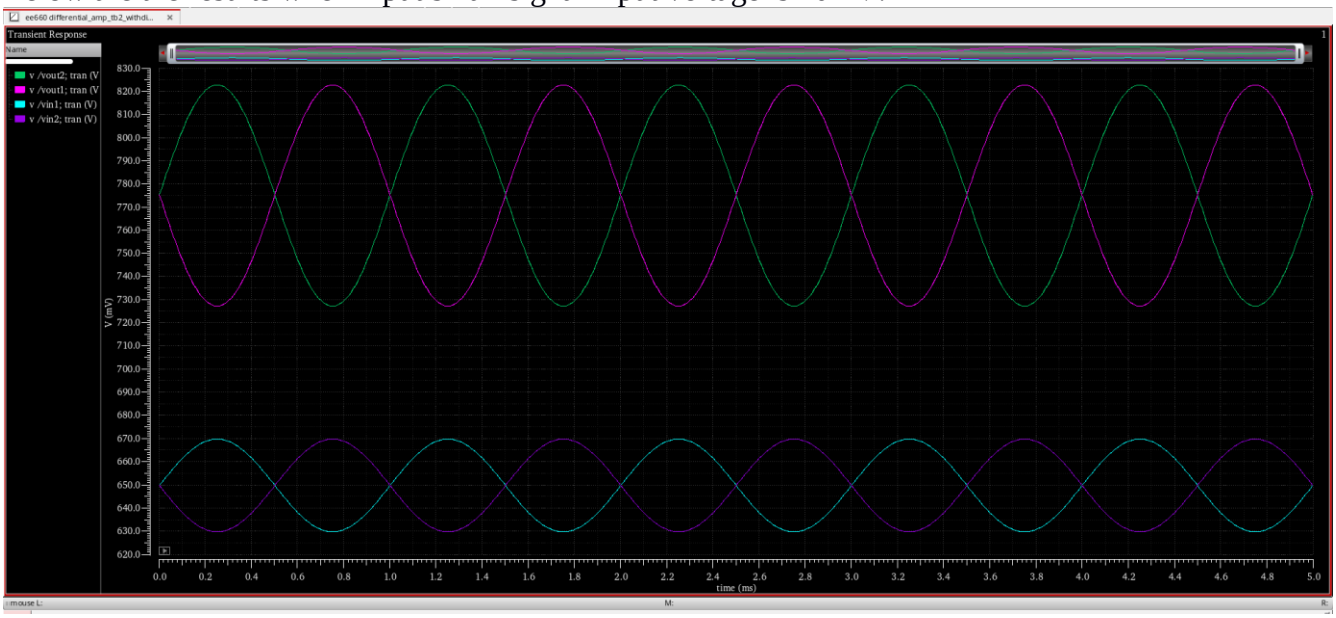


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

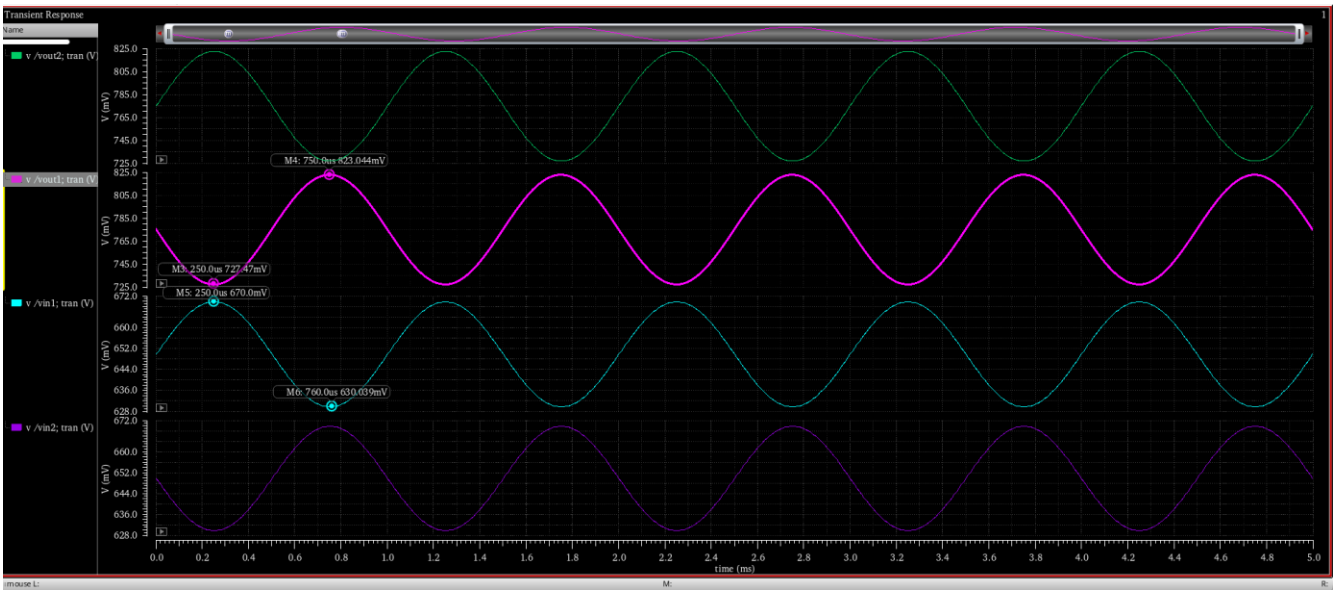


Figure:Plot showing Vin1, Vout1 with min and max points highlighted

Observation:

Vout1max=823mV

Vout1min= 727mv

Vdiff swing =2x(Vout1max-vout1min)=2 x96=192mV

Vin,pp=40mv

Av =Vout1,pp/ Vin,pp = 2.4

e) Remove the VCVS from Fig. 1b and connect V in2 to V in,dc . Perform the transient analysis ofthe circuit with the input small signal voltage assumed to be 10 mV. Plot the waveforms of V out and V out2 , and explain the operation of the circuit.

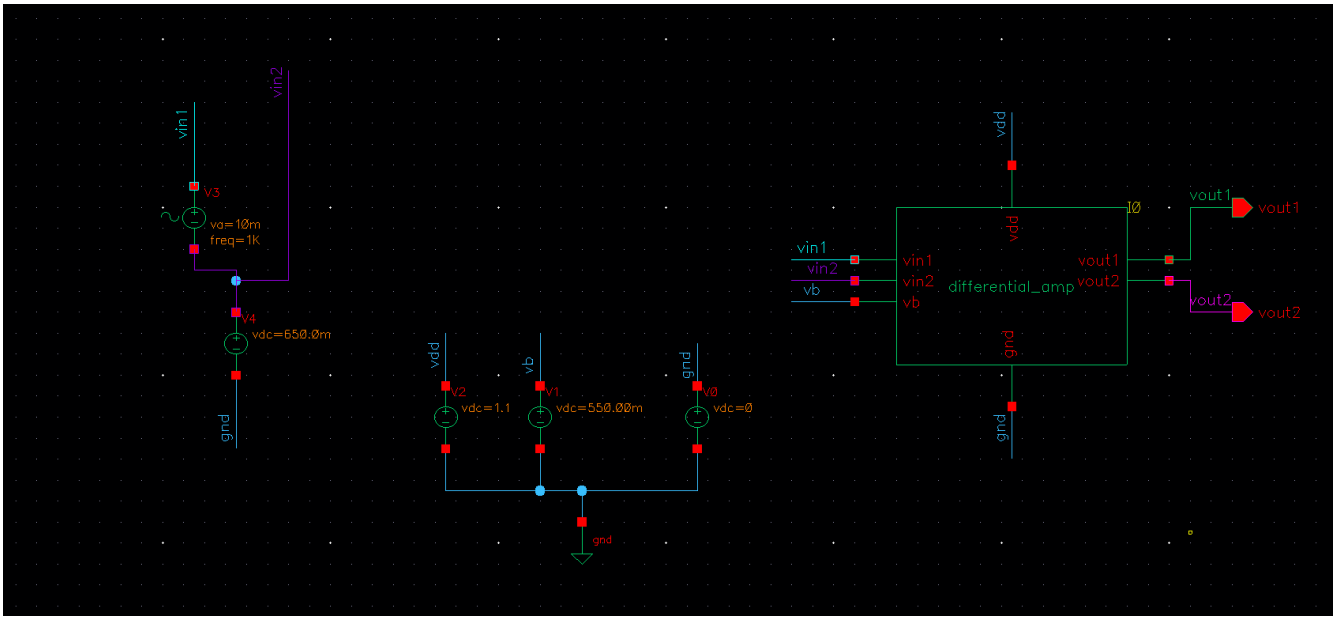


Figure:Schematic showing differential amplifier with vin2 connected to vin,dc and vin1 to ac input

Transient Analysis Simulation Results:

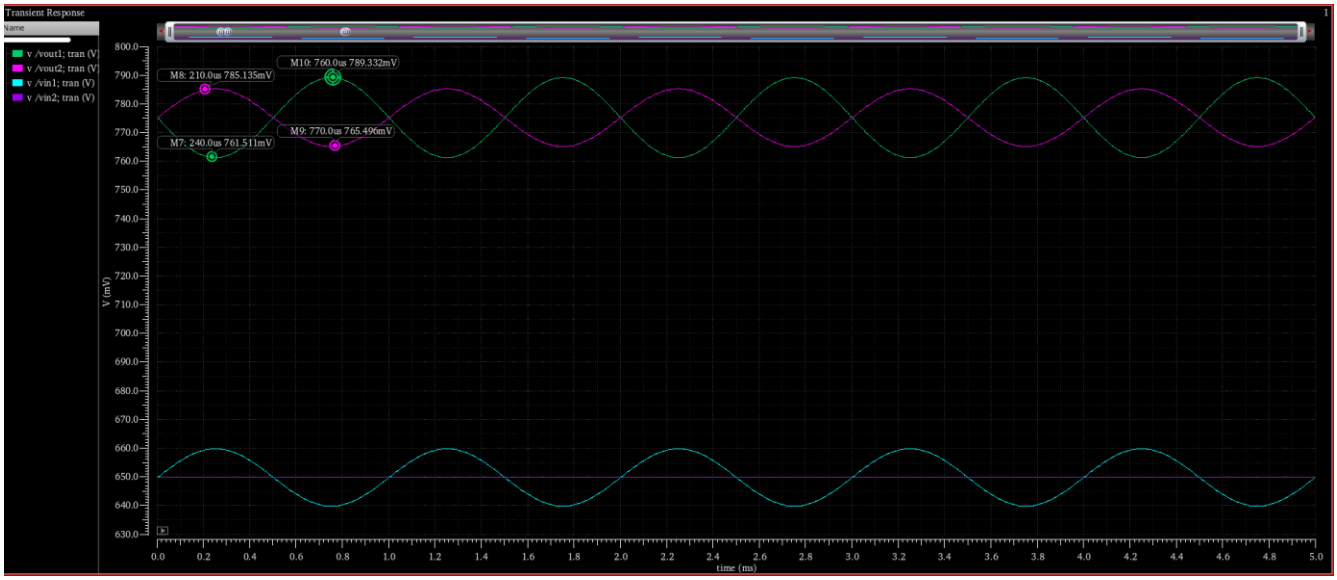


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2 obtained from Transient Analysis

Explanation of above differential Circuit operation:

Here Vin1 is sinusoidal voltage source with 10mv ac amplitude and 0.65v dc voltage, whereas Vin2 has only dc voltage of 0.65V .Since ,vin2 is fixed circuit will respond to the changes in the vin1. The tail current source (M3) provides a fixed total current that is split between M1 and M2.When Vin1 increases above Vin2, M1 draws more current, and M2 draws less. Since the total current remains constant, the current flowing through M1 and M2 adjusts in an opposite manner. This current variation directly affects the drain voltages Vout1 and Vout2.

When Vin1 increases (positive half-cycle of AC input)

M1 draws more current → Voltage drop across RD increases → Vout1 decreases.

M2 draws less current → Voltage drop across RD decreases → Vout2 increases.

When Vin1 decreases (negative half-cycle of AC input)

M1 draws less current → Voltage drop across RD decreases → Vout1 increases.

M2 draws more current → Voltage drop across RD increases → Vout2 decreases.