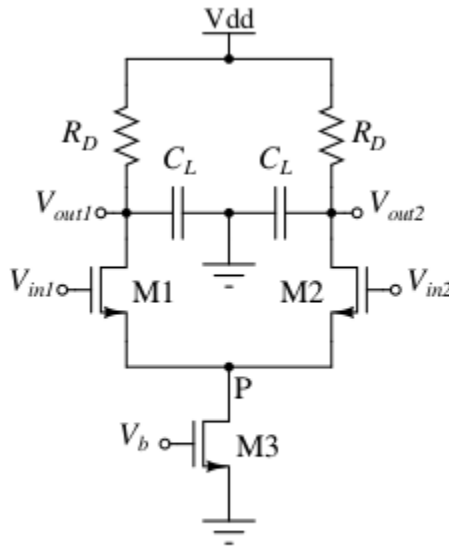


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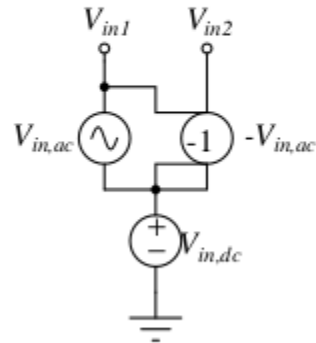
Assignment III

Submitted by: L Sri Sai Swathi (2414202)

1. Design an NMOS common-source differential amplifier with resistive load as shown in Fig. 1a. You can make use of UMC65 models for the transistors. Given $(W/L)_{1,2,3} = 6\mu/0.06\mu$, $R_D = 1\text{ k}\Omega$, $C_L = 100\text{ fF}$, and $V_b = 0.55\text{ V}$.



(a) Differential amplifier.



(b) Input source.

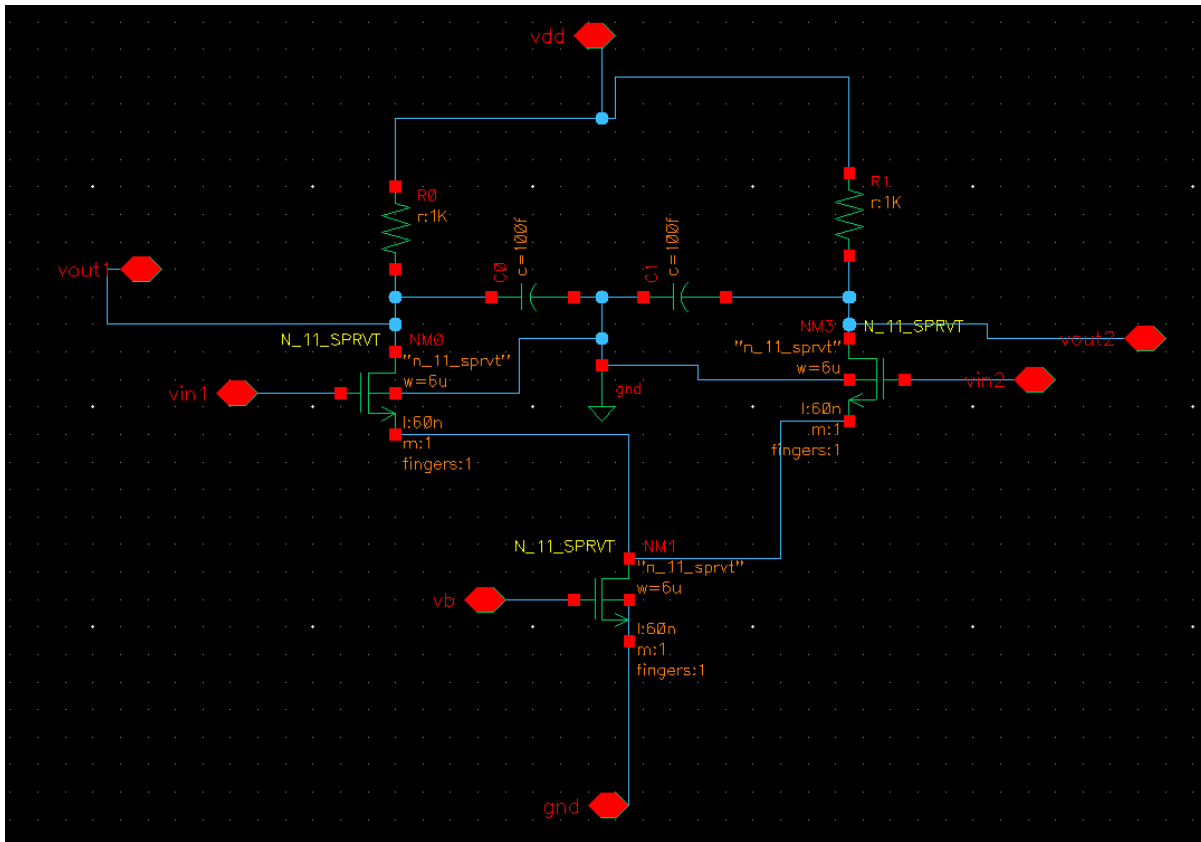


Figure: Schematic showing NMOS common-source differential amplifier with resistive load .

a) The configuration shown in Fig. 1b is used to generate the input for the amplifier. You can use the small signal amplitude of $V_{in,ac}$ to be 10 mV, and frequency to be 1 kHz. Decide the value of $V_{in,dc}$, say (V_{b1}), such that the differential gain is at least 2. Calculate the value of g_{m1} from the gain assuming the second order effects are absent.

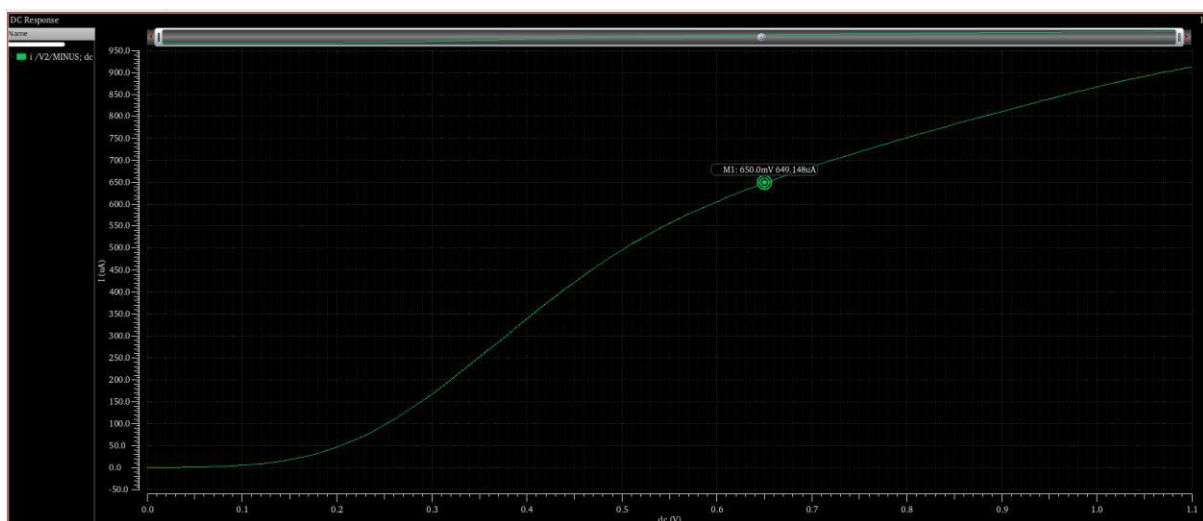


Figure:Plot showing $v_{in\ dc}$ vs I with $v_{in\ dc}$ as 500mv

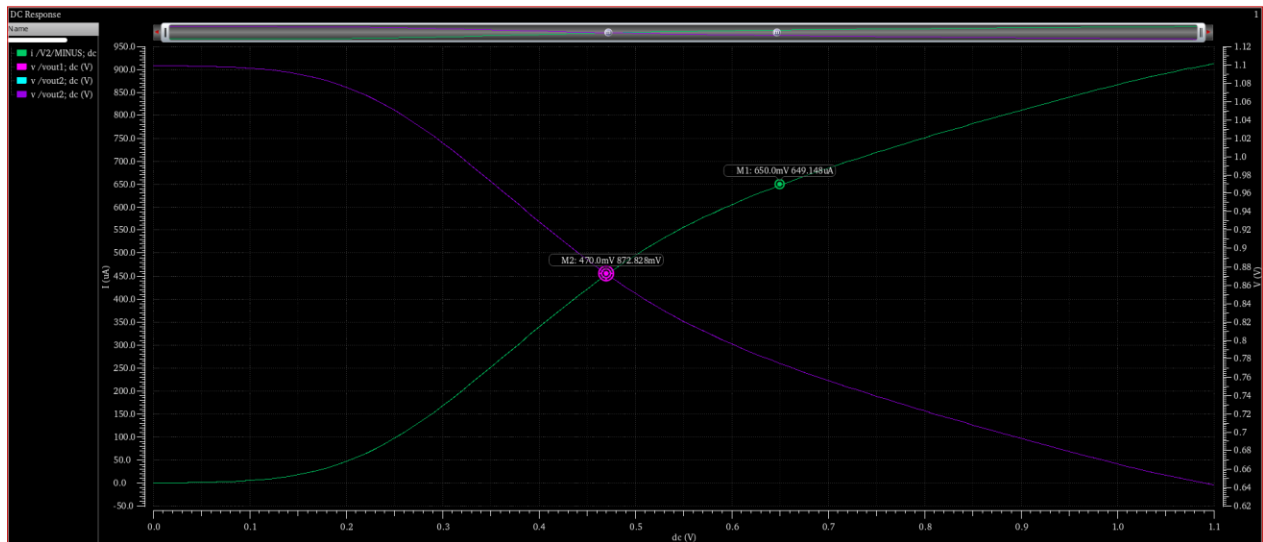


Figure: Plot showing v_{in} dc vs I , v_{out1} , v_{out2} with v_{in} dc as 500mv

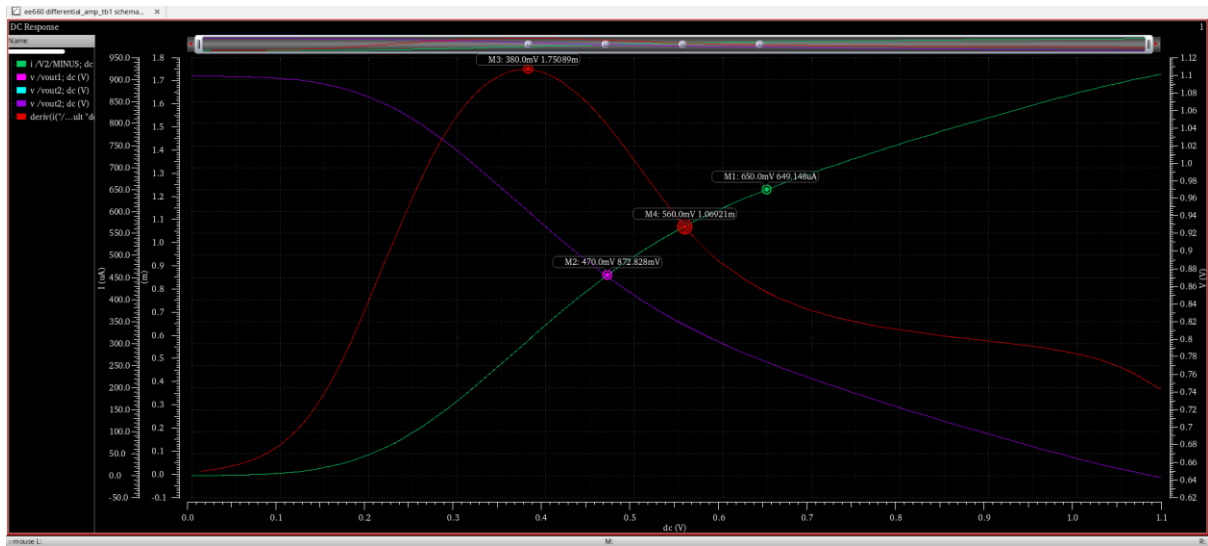


Figure: Plot showing v_{in} dc vs I , v_{out1} , gm with v_{in} dc as 500mv

Observation : From the plot gm is identified to be 1.75m seimens.

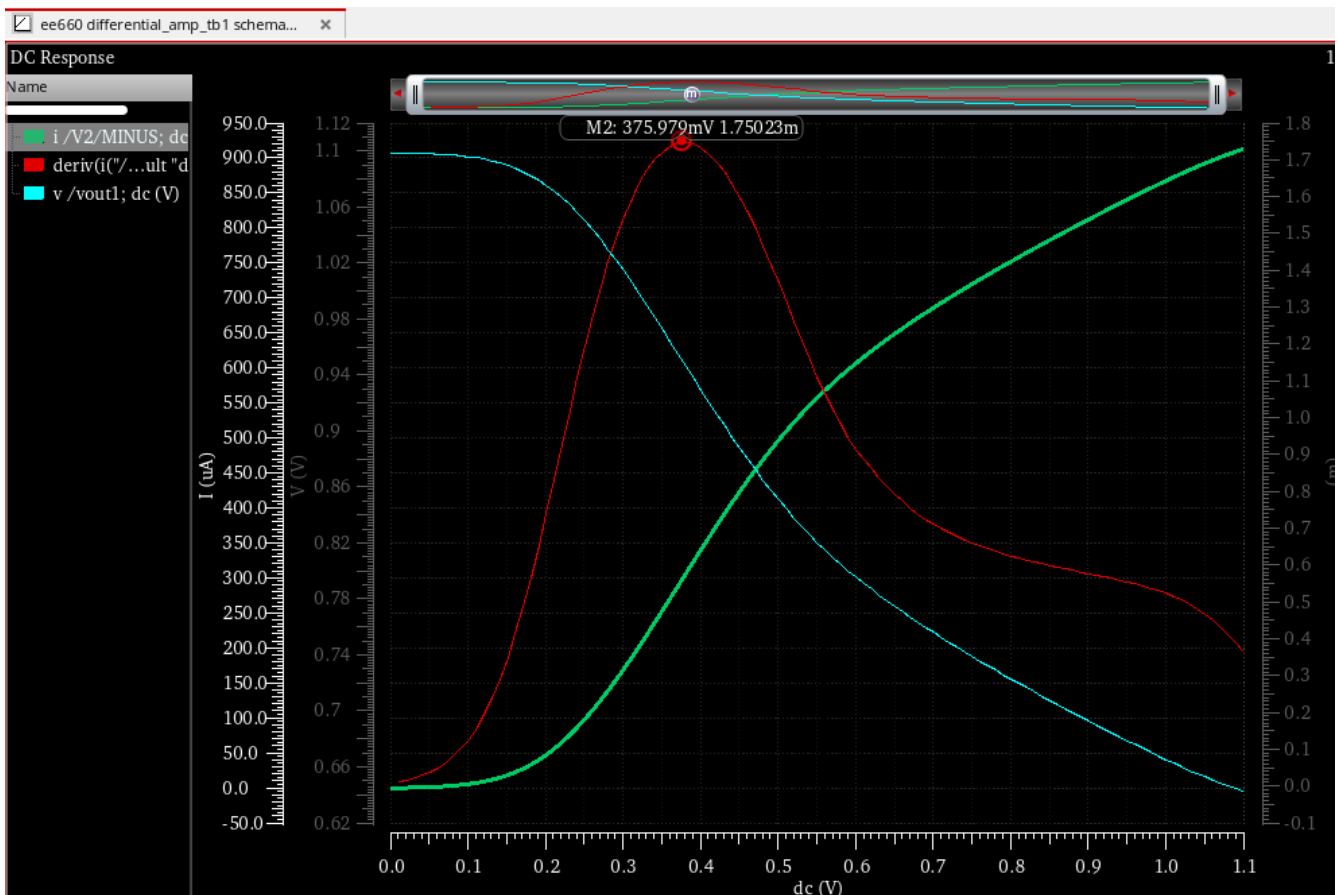


Figure:Plot showing I , v_{out1} , g_m with v_{in} dc as 650mV

We have also tried increasing v_{indc} from 500mV to 750mV and observed g_m to be 1.75mS.

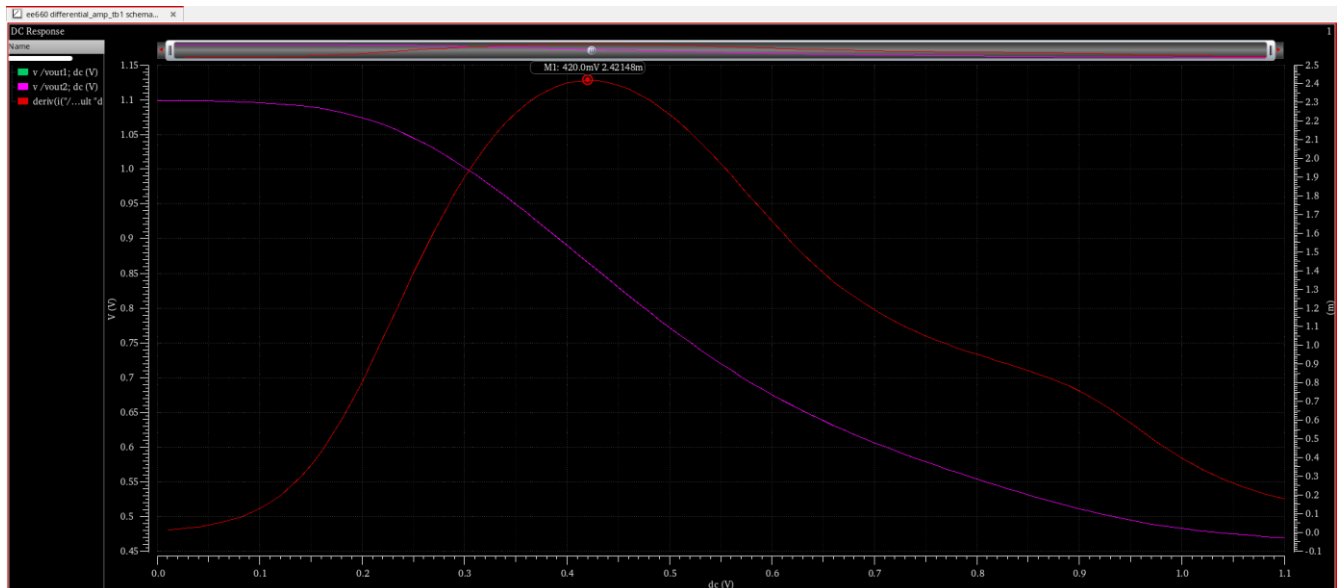


Figure:Plot showing $d v_{out} / d v_{indc}$.

Observation: From the above plots, choosing 650mV as dc bias point. We have also observed that g_m as 1.75mS. And $d v_{out} / d v_{in}$ as 2.4

Below are the simulation results of DC operating point analysis at dc voltage 0.5v

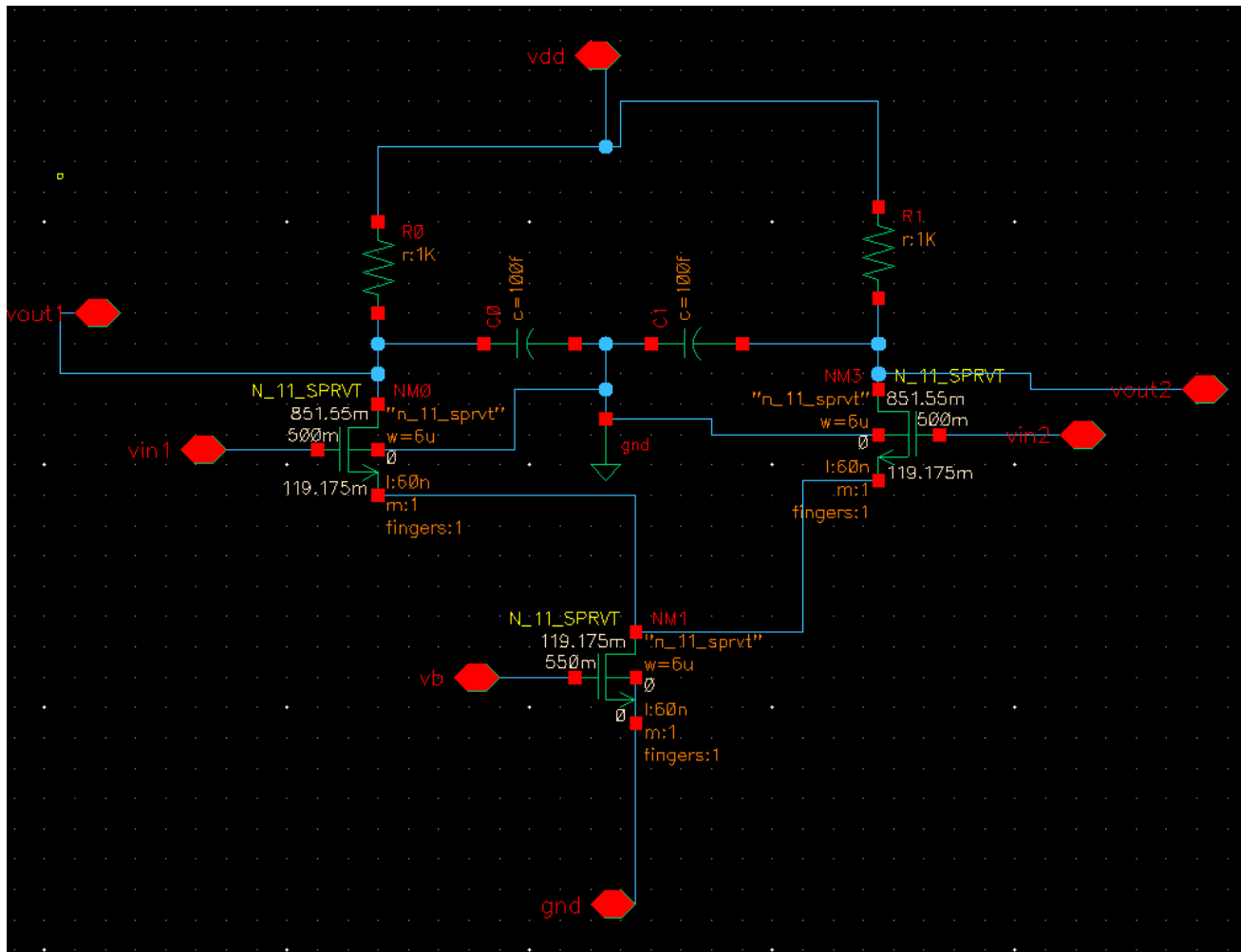
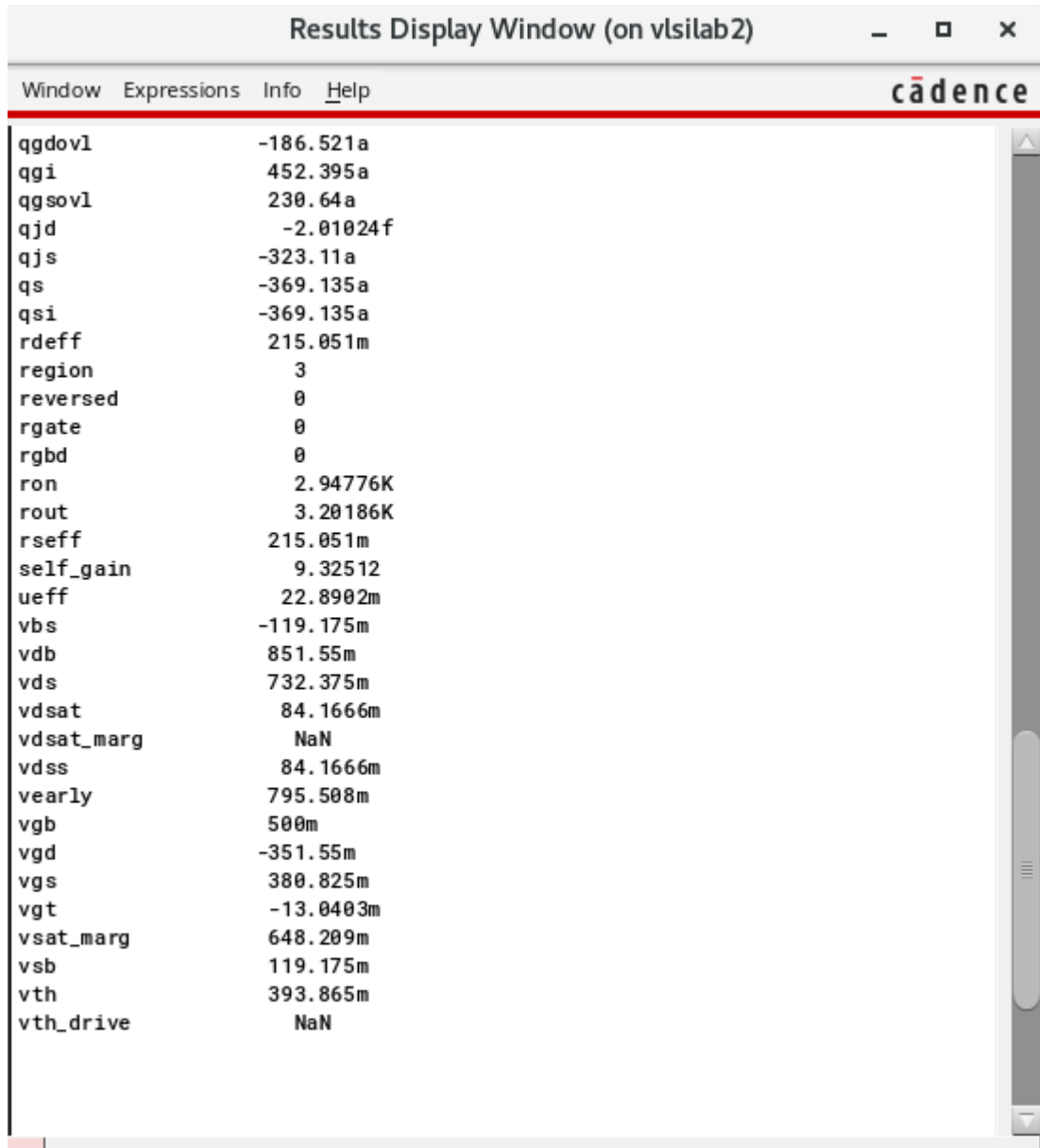


Figure: Schematic showing NMOS common-source differential amplifier with resistive load with all the operating point values.

Simulation result of first mosfet M1 :



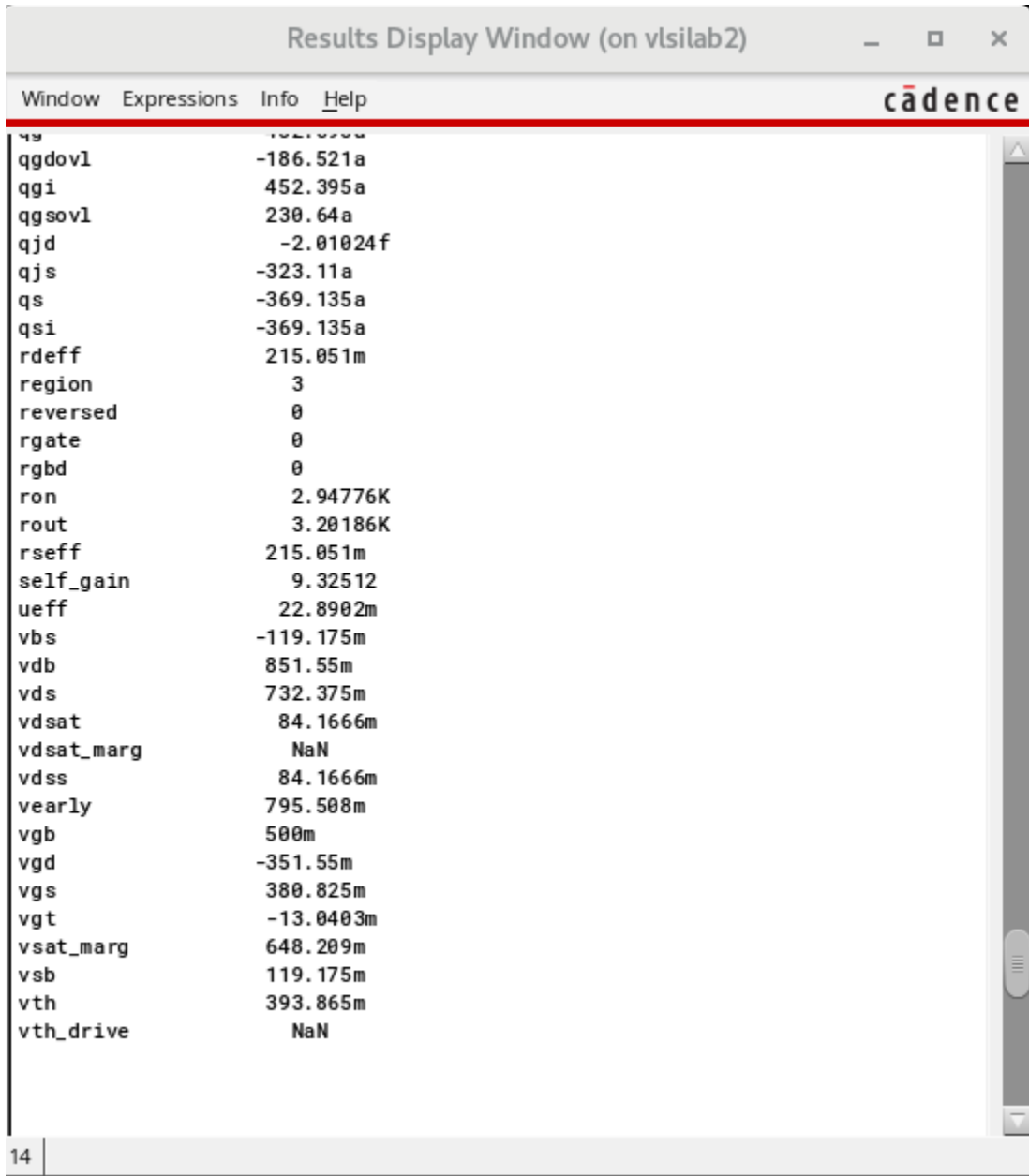
The image shows a screenshot of the 'Results Display Window (on vlsilab2)' in Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation results for MOSFET M1. The results are organized into two columns: the parameter name and its corresponding value. The values include various electrical parameters such as gate voltage (vg), drain voltage (vds), and threshold voltage (vth), along with their units (a, f, m, K, V, mV, etc.). The 'region' parameter is set to 3, indicating the MOSFET is in saturation. The 'vgs' (gate-source voltage) is 380.825mV, and the 'vds' (drain-source voltage) is 732.375mV. The 'vth' (threshold voltage) is 393.865mV. The 'vgs' is also labeled as 'vgs' and 'vgs'.

Parameter	Value
qgdovl	-186.521a
qgi	452.395a
qgsovl	230.64a
qjd	-2.01024f
qjs	-323.11a
qs	-369.135a
qsi	-369.135a
rdeff	215.051m
region	3
reversed	0
rgate	0
rgbd	0
ron	2.94776K
rout	3.20186K
rseff	215.051m
self_gain	9.32512
ueff	22.8902m
vbs	-119.175m
vdb	851.55m
vds	732.375m
vdsat	84.1666m
vdsat_marg	NaN
vdss	84.1666m
vearly	795.508m
vgb	500m
vgd	-351.55m
vgs	380.825m
vgt	-13.0403m
vsat_marg	648.209m
vsb	119.175m
vth	393.865m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 3 at $v_{indc} = 500\text{mV}$

Simulation result of mosfet M2 :



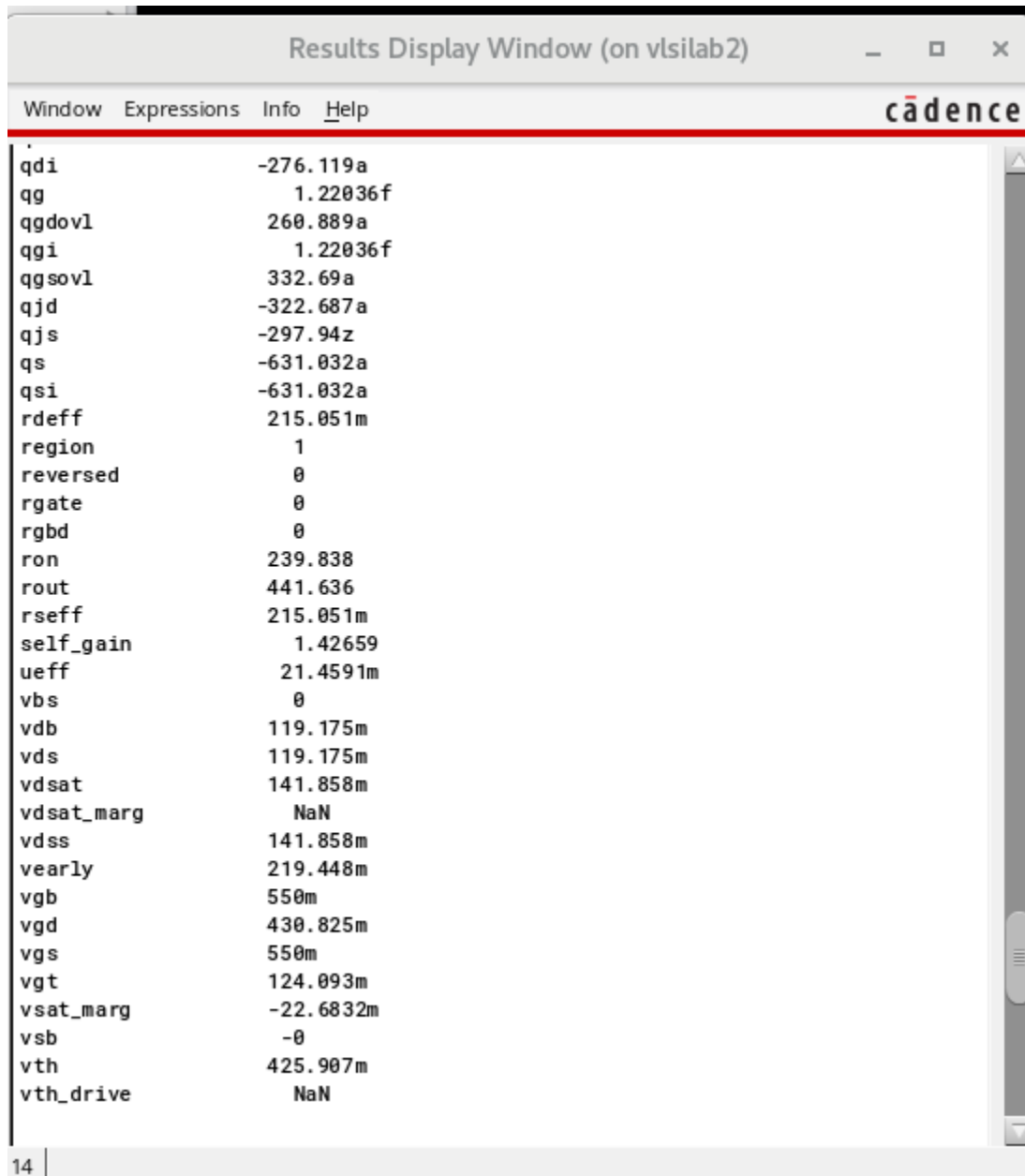
The image shows a screenshot of the 'Results Display Window (on vlsilab2)' in a Cadence environment. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation results for a MOSFET model. The results are organized into two columns: the parameter name and its corresponding value. The values include various electrical parameters such as gate voltage, drain current, threshold voltage, and transconductance, along with physical parameters like region, reversed, gate, and body. The bottom of the window shows a status bar with the number '14'.

Parameter	Value
qgdovl	-186.521a
qgi	452.395a
qgsovl	230.64a
qjd	-2.01024f
qjs	-323.11a
qs	-369.135a
qsi	-369.135a
rdeff	215.051m
region	3
reversed	0
rgate	0
rgbd	0
ron	2.94776K
rout	3.20186K
rseff	215.051m
self_gain	9.32512
ueff	22.8902m
vbs	-119.175m
vdb	851.55m
vds	732.375m
vdsat	84.1666m
vdsat_marg	NaN
vdss	84.1666m
vearly	795.508m
vgb	500m
vgd	-351.55m
vgs	380.825m
vgt	-13.0403m
vsat_marg	648.209m
vsb	119.175m
vth	393.865m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 3 at $v_{indc} = 500\text{mV}$

Simulation result of mosfet M3 :



The screenshot shows the 'Results Display Window (on vlsilab2)' in Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The 'cadence' logo is in the top right corner. The main area displays a list of parameters and their values for MOSFET M3. The parameters are listed on the left, and their values are on the right. The values are in scientific notation or decimal form, indicating the units (e.g., 'a' for amperes, 'f' for femto, 'm' for milli, 'N' for nano, 'V' for volts).

Parameter	Value
qdi	-276.119a
qg	1.22036f
qgdovl	260.889a
qgi	1.22036f
qgsovl	332.69a
qjd	-322.687a
qjs	-297.94z
qs	-631.032a
qsi	-631.032a
rdeff	215.051m
region	1
reversed	0
rgate	0
rgbd	0
ron	239.838
rout	441.636
rseff	215.051m
self_gain	1.42659
ueff	21.4591m
vbs	0
vdb	119.175m
vds	119.175m
vdsat	141.858m
vdsat_marg	NaN
vdss	141.858m
vearly	219.448m
vgb	550m
vgd	430.825m
vg	550m
vgt	124.093m
vsat_marg	-22.6832m
vsb	-0
vth	425.907m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 1 at $v_{indc} = 500\text{mV}$. Since all 3 are not in saturation increasing $v_{in, dc}$ to 650mV.

Below are the simulation results of DC operating point analysis at dc voltage 650mv:

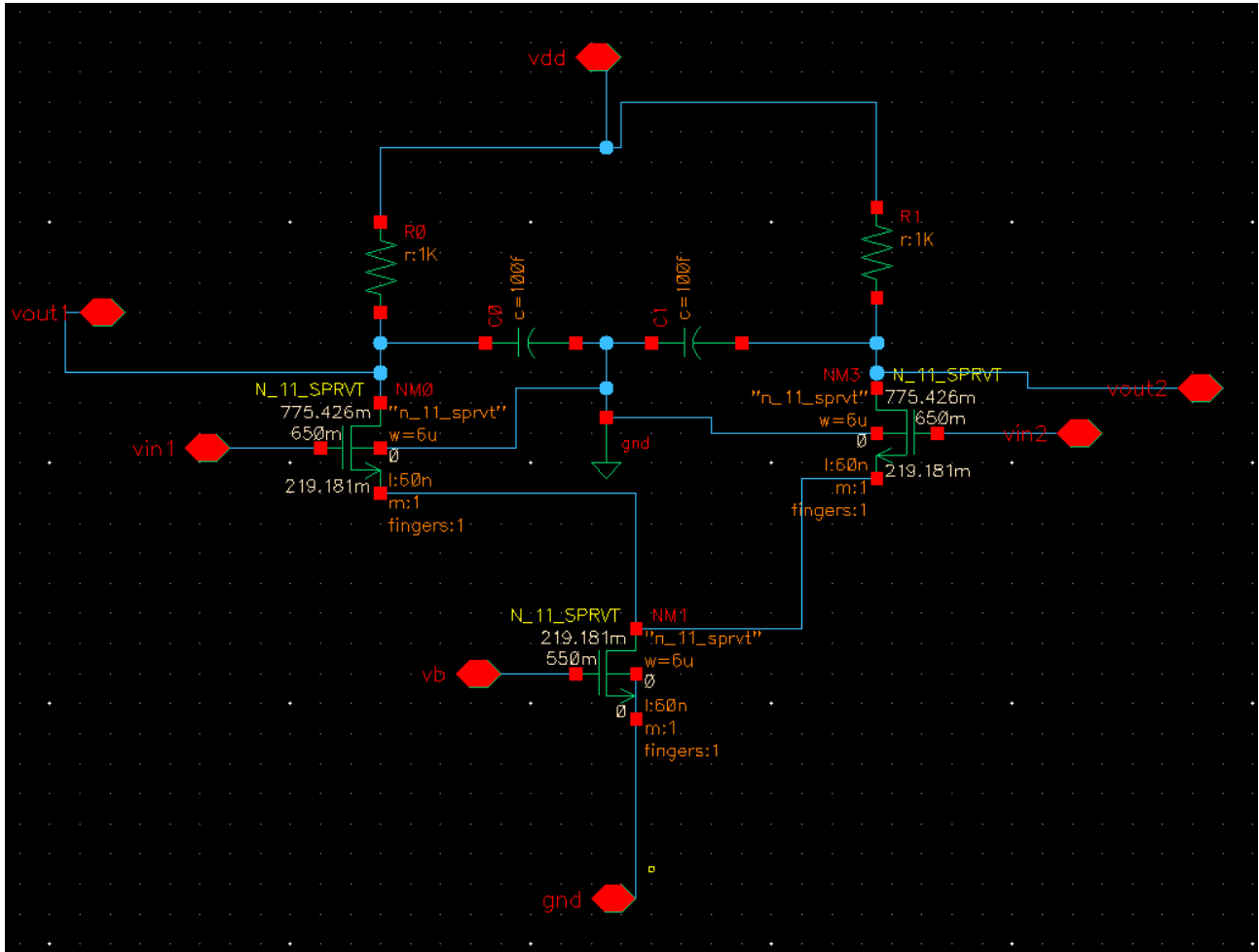
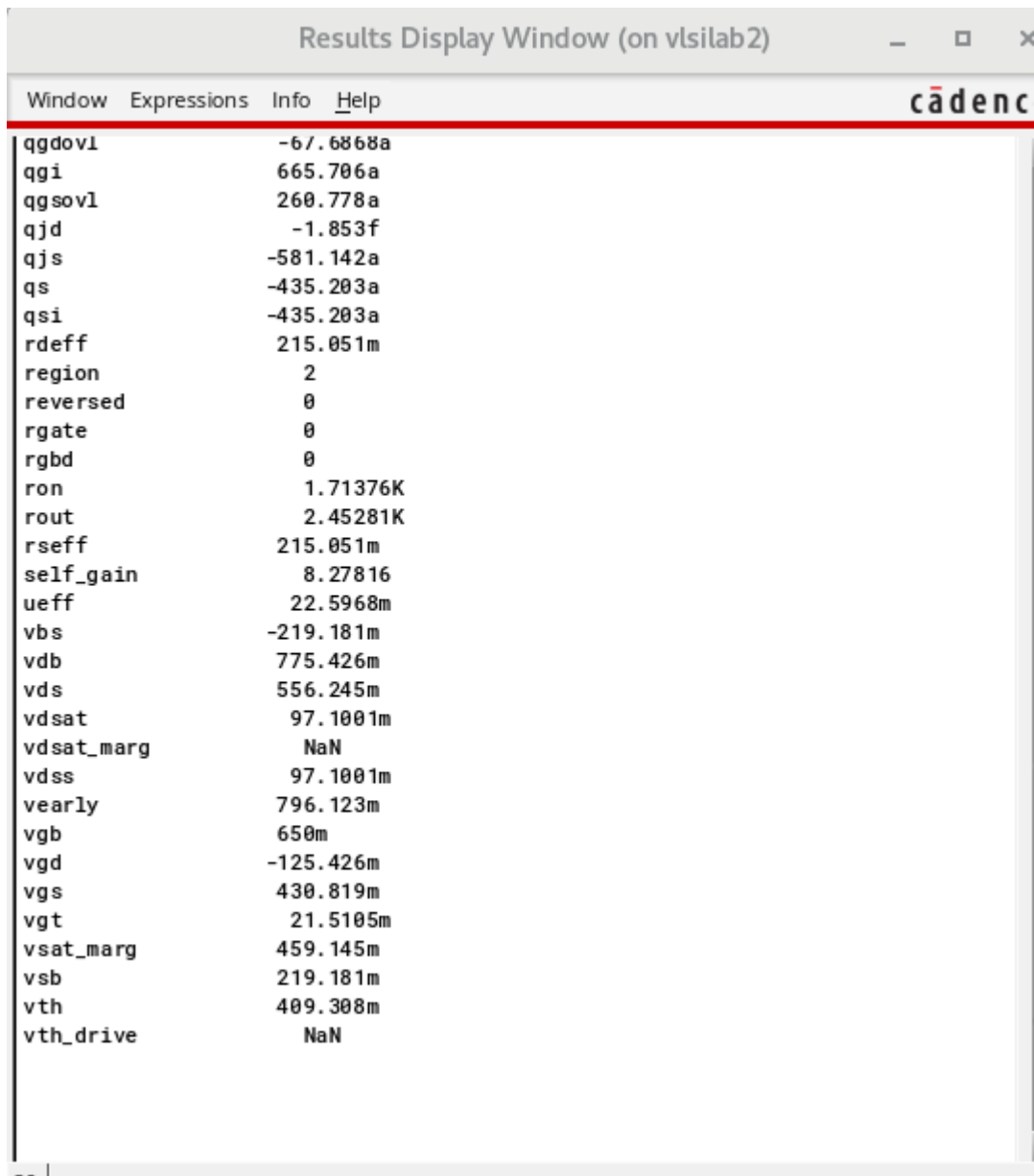


Figure: Schematic showing NMOS common-source differential amplifier with resistive load with all the operating point values.

Simulation result of first mosfet M1 :



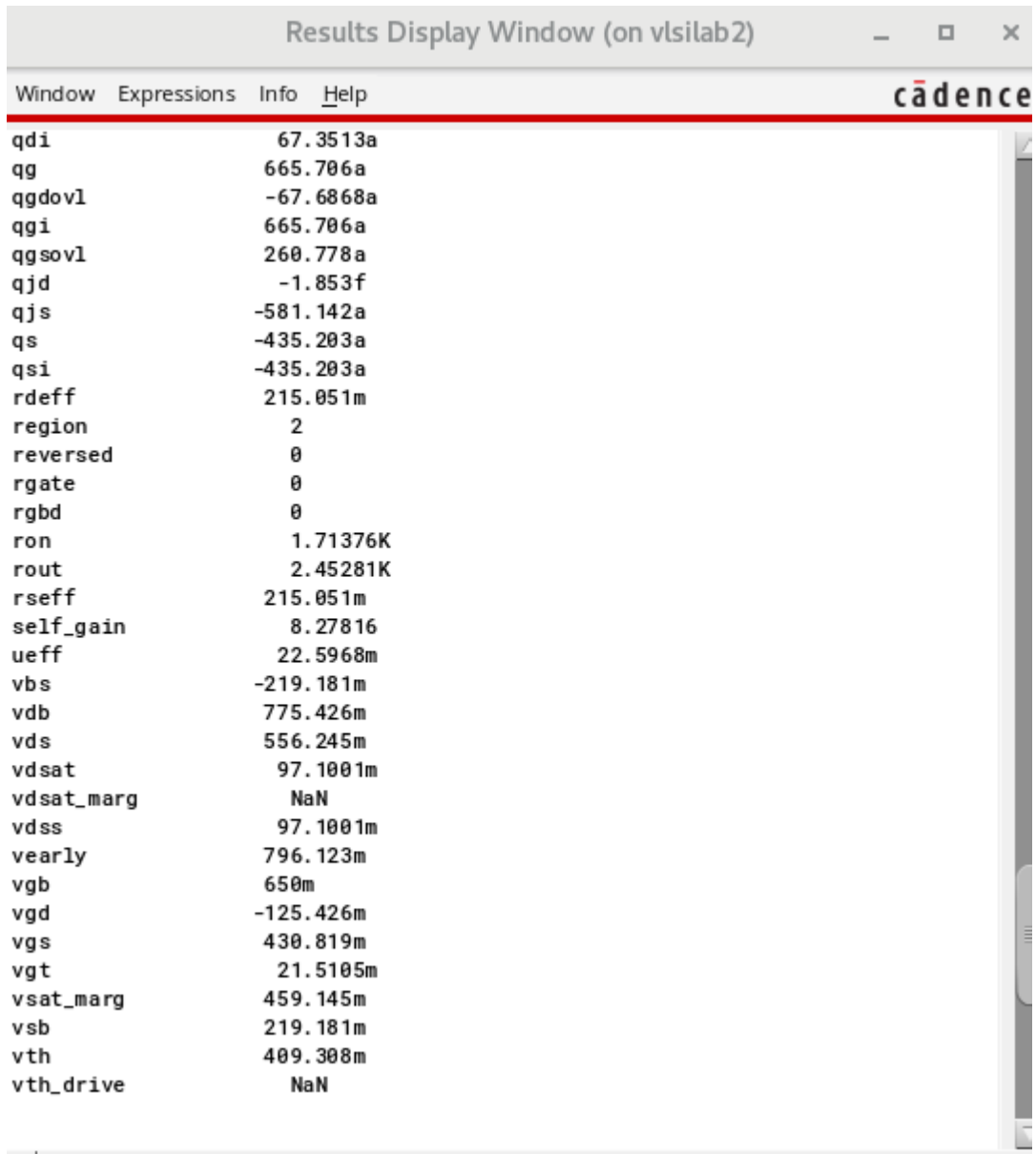
The image shows a screenshot of the 'Results Display Window (on vlsilab2)' in Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation results for MOSFET M1. The results are organized into two columns: the parameter name and its corresponding value. The values are in various units, including amperes (a), milliamperes (m), volts (v), and millivolts (mv). The 'region' parameter is set to 2, indicating the MOSFET is in the saturation region. The 'vth_drive' parameter is set to NaN, indicating that the threshold voltage is not defined for this device.

Parameter	Value
qgdovl	-67.6868a
qgi	665.706a
qgsov1	260.778a
qjd	-1.853f
qjs	-581.142a
qs	-435.203a
qsi	-435.203a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	1.71376K
rout	2.45281K
rseff	215.051m
self_gain	8.27816
ueff	22.5968m
vbs	-219.181m
vdb	775.426m
vds	556.245m
vdsat	97.1001m
vdsat_marg	NaN
vdss	97.1001m
vearly	796.123m
vgb	650m
vgd	-125.426m
vgs	430.819m
vgt	21.5105m
vsat_marg	459.145m
vsb	219.181m
vth	409.308m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M1 is in region 2 at $v_{indc} = 650\text{mv}$

Simulation result of mosfet M2 :



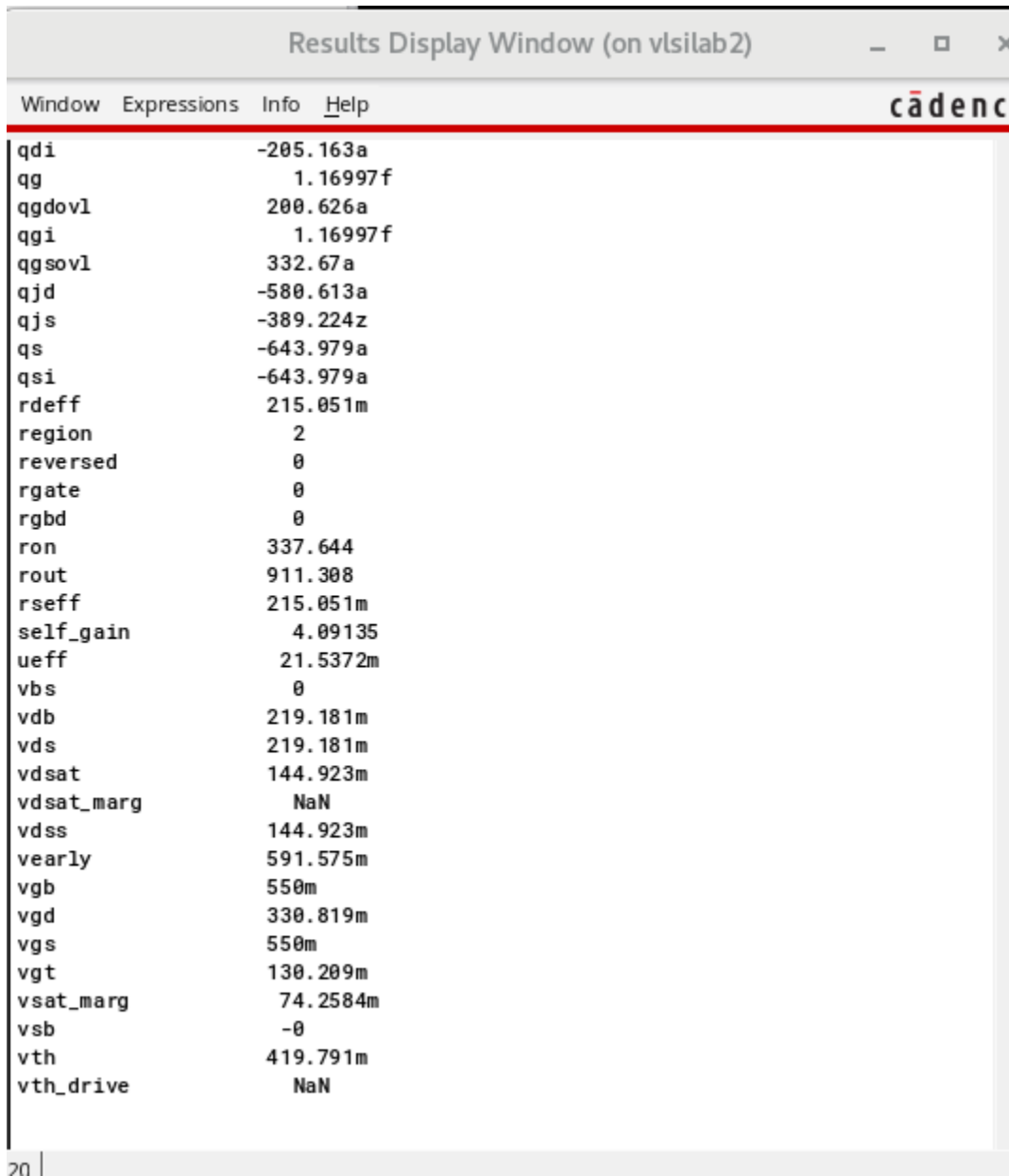
The image shows a screenshot of the 'Results Display Window (on vlsilab2)' in Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The 'cadence' logo is in the top right corner. The main area displays a list of simulation parameters and their values. The parameters are listed on the left, and their corresponding values are on the right. The values are in scientific notation or standard units.

Parameter	Value
qdi	67.3513a
qg	665.706a
qgdovl	-67.6868a
qgi	665.706a
qgsovl	260.778a
qjd	-1.853f
qjs	-581.142a
qs	-435.203a
qsi	-435.203a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	1.71376K
rout	2.45281K
rseff	215.051m
self_gain	8.27816
ueff	22.5968m
vbs	-219.181m
vdb	775.426m
vds	556.245m
vdsat	97.1001m
vdsat_marg	NaN
vdss	97.1001m
vearly	796.123m
vgb	650m
vgd	-125.426m
vgs	430.819m
vgt	21.5105m
vsat_marg	459.145m
vsb	219.181m
vth	409.308m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M2 is in region 2 at $v_{indc} = 650\text{mV}$

Simulation result of mosfet M3:



The screenshot shows a 'Results Display Window (on vlsilab2)' from Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The main area displays a list of simulation parameters and their values. The parameters are listed on the left, and their corresponding values are on the right. The values are in scientific notation or standard decimal form. The 'region' parameter is highlighted with a red background, indicating the operating point of the MOSFET.

Parameter	Value
qdi	-205.163a
qg	1.16997f
qgdovl	200.626a
qgi	1.16997f
qgsovl	332.67a
qjd	-580.613a
qjs	-389.224z
qs	-643.979a
qsi	-643.979a
rdeff	215.051m
region	2
reversed	0
rgate	0
rgbd	0
ron	337.644
rout	911.308
rseff	215.051m
self_gain	4.09135
ueff	21.5372m
vbs	0
vdb	219.181m
vds	219.181m
vdsat	144.923m
vdsat_marg	NaN
vdss	144.923m
vearly	591.575m
vgb	550m
vgd	330.819m
vgs	550m
vgt	130.209m
vsat_marg	74.2584m
vsb	-0
vth	419.791m
vth_drive	NaN

Figure: Simulation result of DC operating point analysis.

Observation: M3 is in region 2 at $v_{indc} = 650\text{mV}$. It is observed that all the 3 mosfets are in saturation region .i.e region2

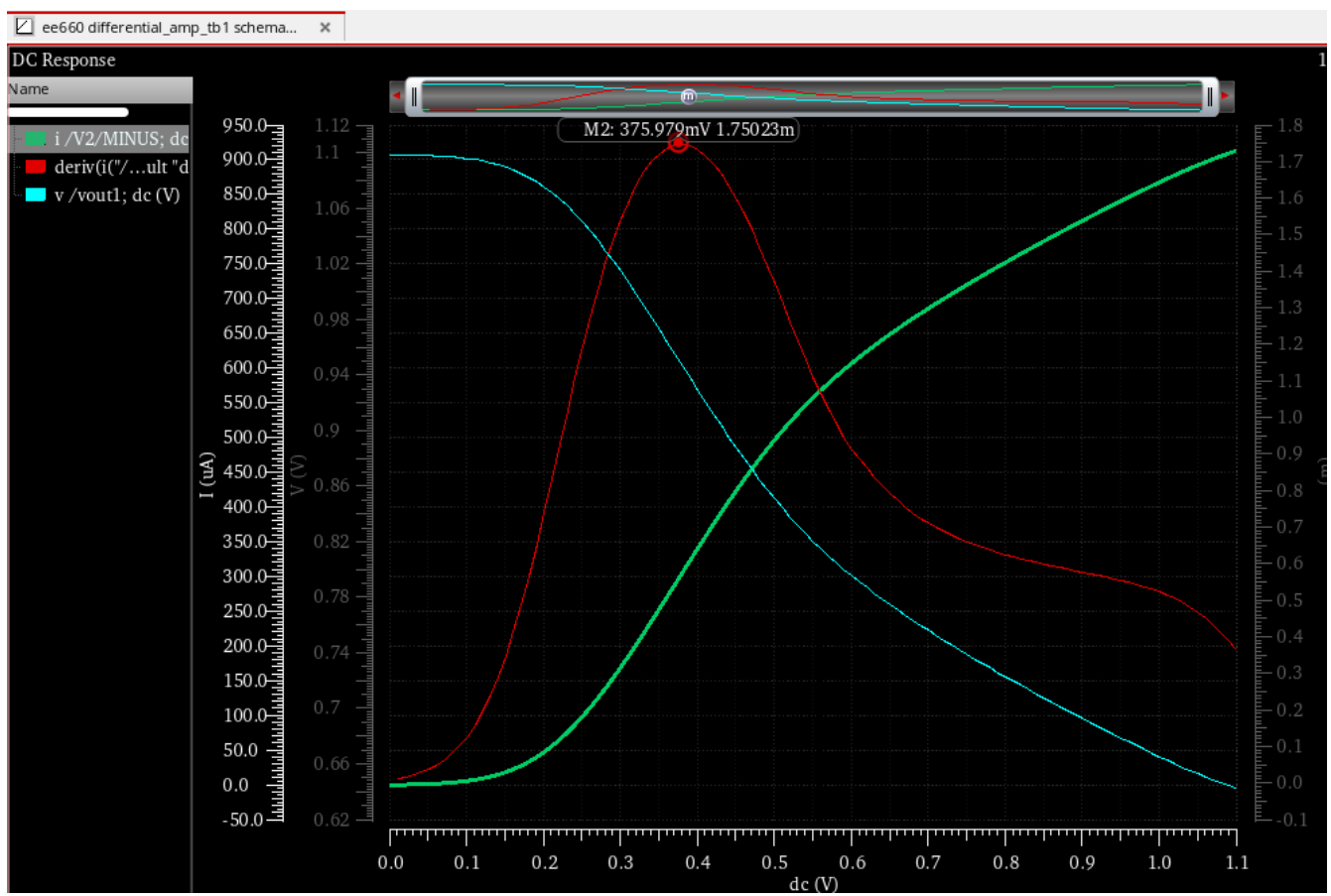


Figure:Plot showing I , v_{out1} , gm with v_{in} dc as 650mv

(b) Perform the operating point analysis with $V_{in,dc} = V_{b1}$ and check if all the transistors are in saturation region of operation. If not, find out another value for V_{b1} . Calculate $V_{out1,max}$ and $V_{out1,min}$, and hence the maximum differential output voltage swing. From this calculate the maximum input swing that can be applied to the amplifier

Performed transient analysis at $V_{in,dc}=650mV$, small signal voltage is $10mV$, frequency $=1KHz$

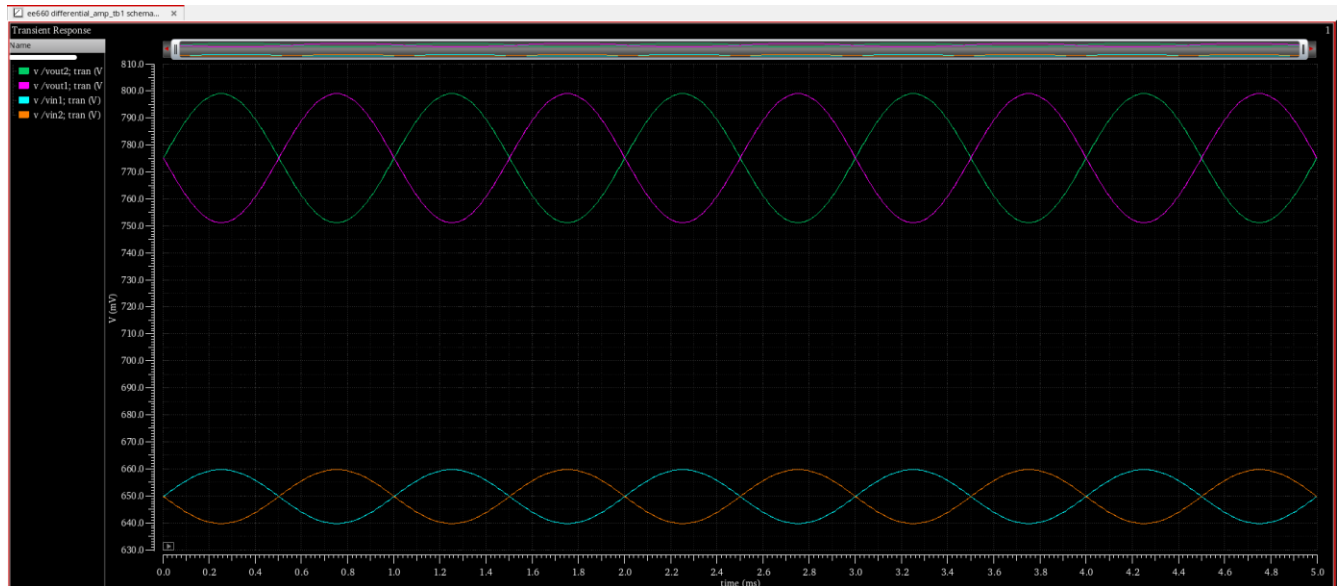


Figure:Plot showing $V_{in1}, V_{in2}, V_{out1}, V_{out2}$

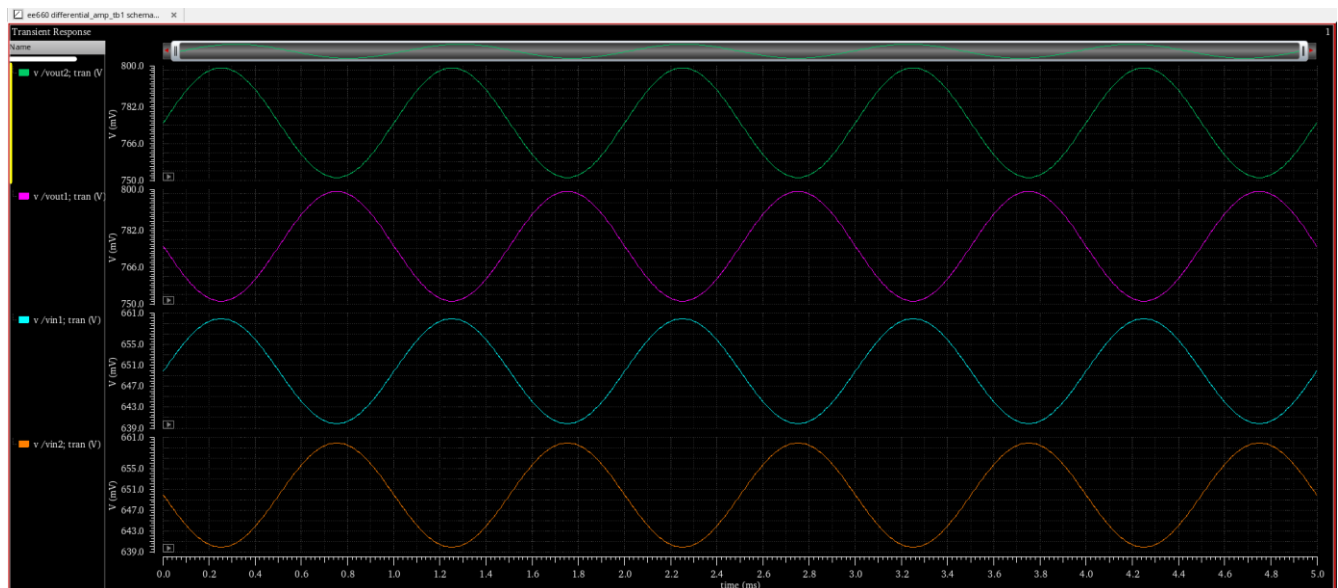


Figure:Plot showing $V_{in1}, V_{in2}, V_{out1}, V_{out2}$

Observation: From the above plot it is evident that V_{in1}, V_{out1} are out of phase and V_{in2}, V_{out2} are out of phase.

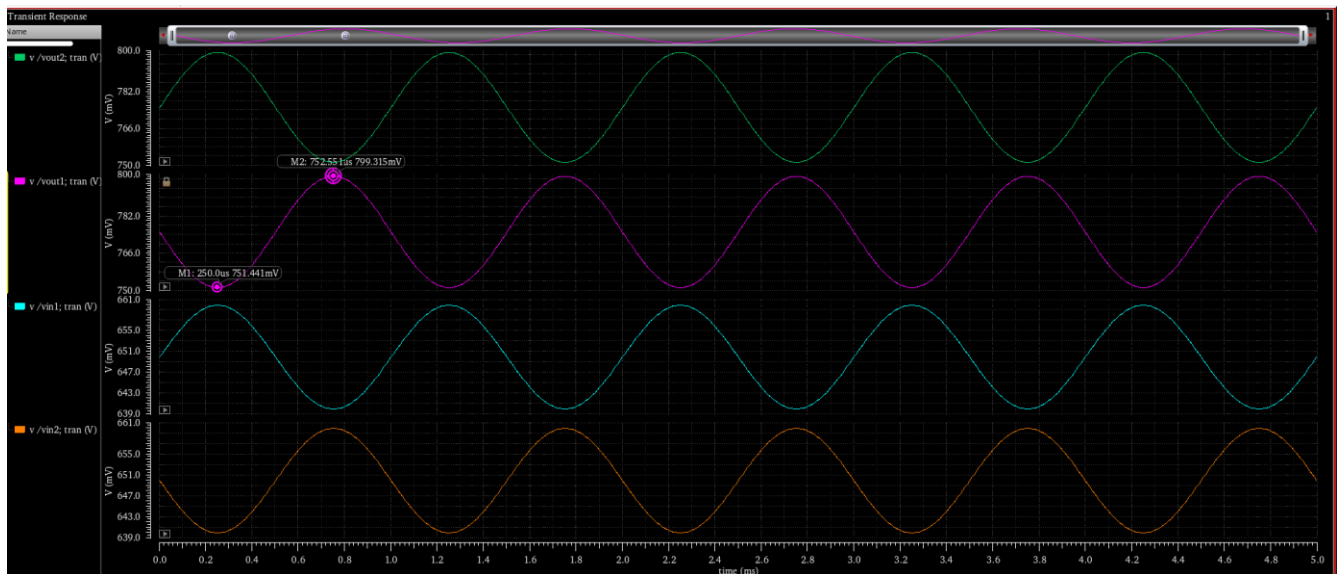


Figure: Plot showing V_{in1} , V_{in2} , V_{out1} , V_{out2}

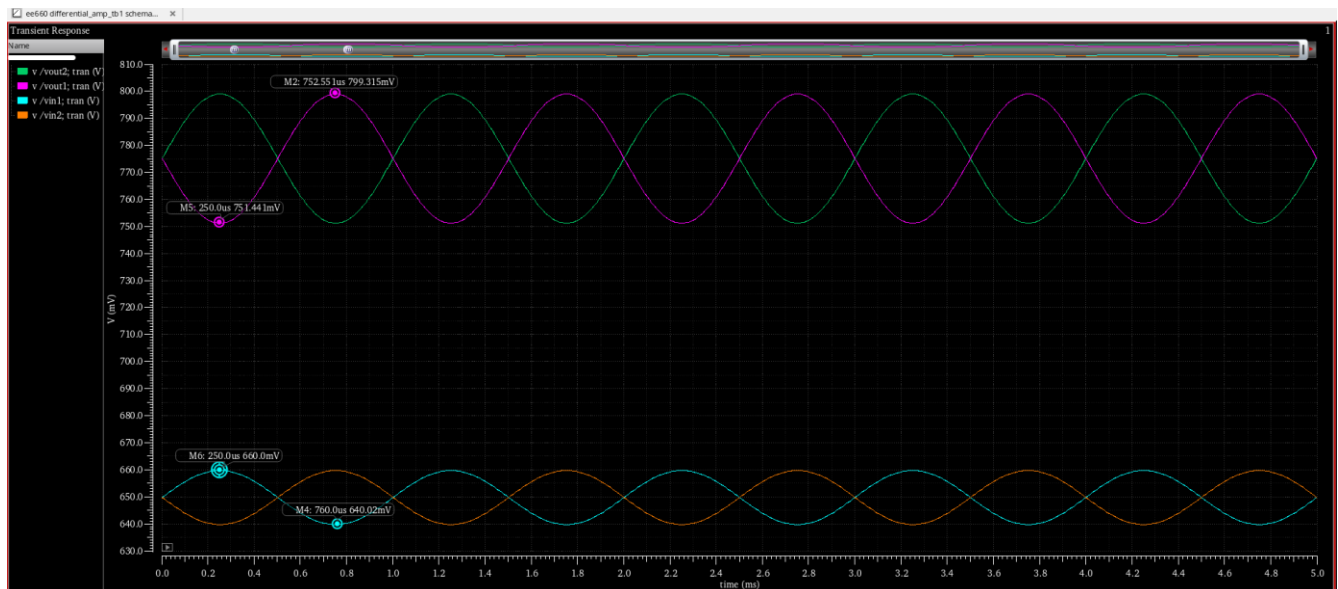


Figure: Plot showing V_{in1} , V_{out1} with min and max points highlighted

Observation:

$V_{out1max} = 799.31\text{mV}$

$V_{out1min} = 751.44\text{mV}$

$V_{out,swing} = 47.87\text{mV}$

$V_{diff\ swing} = 2 \times (V_{out1max} - V_{out1min}) = 2 \times 47.87 = 95.74\text{mV}$

$V_{in,pp} = 20\text{mV}$

$A_v = V_{out1,pp} / V_{in,pp} = 2.39$

$V_{in,swing} = V_{out,swing} / 2.39 = 20\text{mV}$

(c) Perform the AC analysis of the circuit and find out the 3 dB frequency. What is the phase difference between the input and output at this cut-off frequency? Is it possible for you to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios?

Below are simulation results of the AC response analysis :



Figure: Plot showing Ac response analysis results (Vout1,Vin1 considered)

Observations: From the above Ac Analysis plots we can say that :

1. Low frequency gain is **7.589dB**
2. 3dB cutoff frequency is **2.157GHz**
3. Phase difference between the input and output at the 3 dB frequency: **134.72Degrees**.

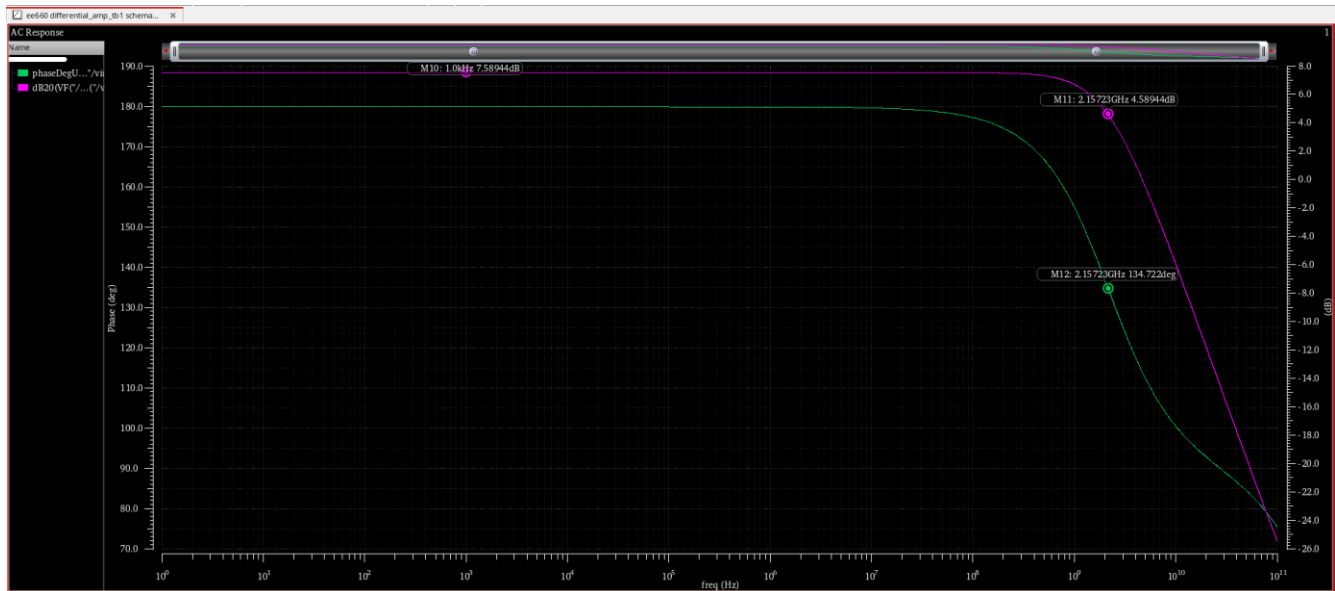


Figure: Plot showing Ac response analysis results (Vout2,Vin2 considered)

AC response Vout2,vin2

Observations:From the above Ac Analysis plots we can say that :

- 1.Low frequency gain is **7.589dB**
2. 3dB cutoff frequency is **2.157GHz**
- 3.Phase difference between the input and output at the 3 dB frequency: **134.72Degrees**.

Is it possible for you to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios?

Trial 1:When RD is increased from 1k to 1.5k



Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plots we can say that :

- 1.Low frequency gain is **9.424dB**
2. 3dB cutoff frequency is **1.689GHz**

Bandwidth got reduced.

Trial 2: Changed Aspect ratios i.e **M1,M2** has width 9um and **M3** has width 8um



Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plots we can say that :

- 1.Low frequency gain is **9.33dB**
2. 3dB cutoff frequency is **2.43GHz**

Trial 3: when all three transistors has width as 9um



Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observations:From the above Ac Analysis plot we can say that :

- 1.Low frequency gain is **9.48dB**
2. 3dB cutoff frequency is **2.53GHz**

Trial4 : when m1 ,m2 has w =6um and m3 has w =9um



Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

- 1.Low frequency gain is **8.40dB**
2. 3dB cutoff frequency is **2.36GHz**

Trial5 :when m1 ,m2 ,m3 has w =9um and Rd=0.5Kohms

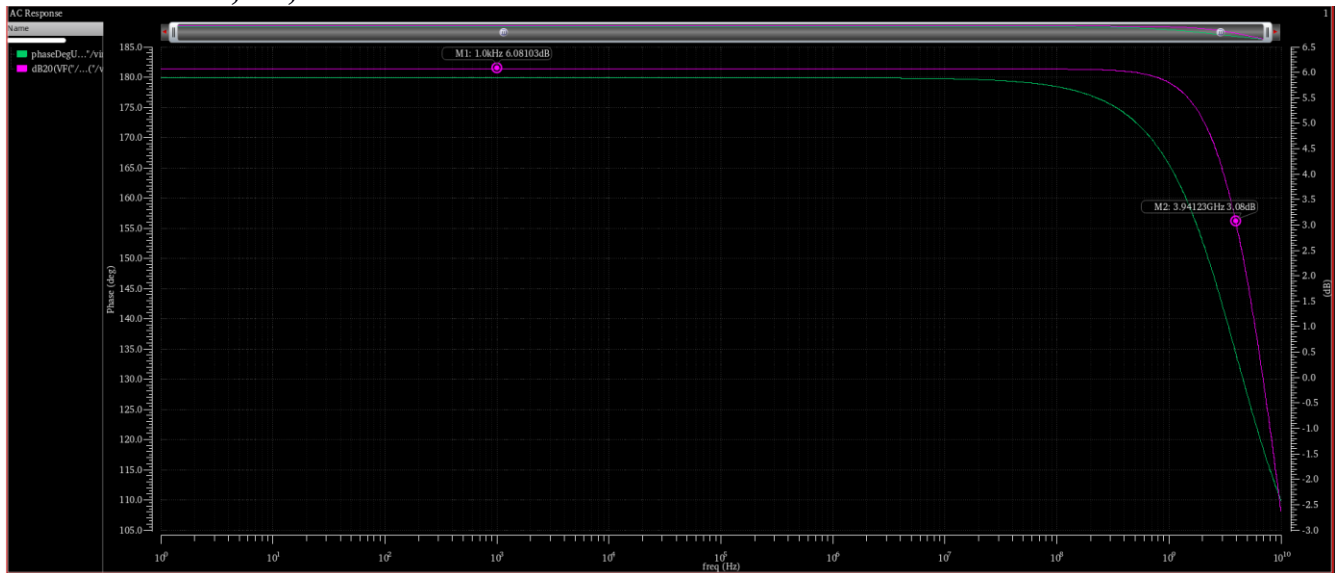


Figure :Plot showing Frequency and Phase response obtained by performing AC analysis.

Observation:

- 1.Low frequency gain is 6.08dB**
- 2. 3dB cutoff frequency is 3.94GHz**

Conclusion: It is not possible for us to increase the bandwidth without reducing the gain by changing R D and/or W/L ratios

(d) Perform the transient analysis of the circuit with the input small signal voltage assumed to be 10 mV and 20 mV, and plot the differential input and output waveforms.

Performed transient analysis at $V_{in,dc}=650\text{mV}$, small signal voltage is 10mV, frequency =1KHz

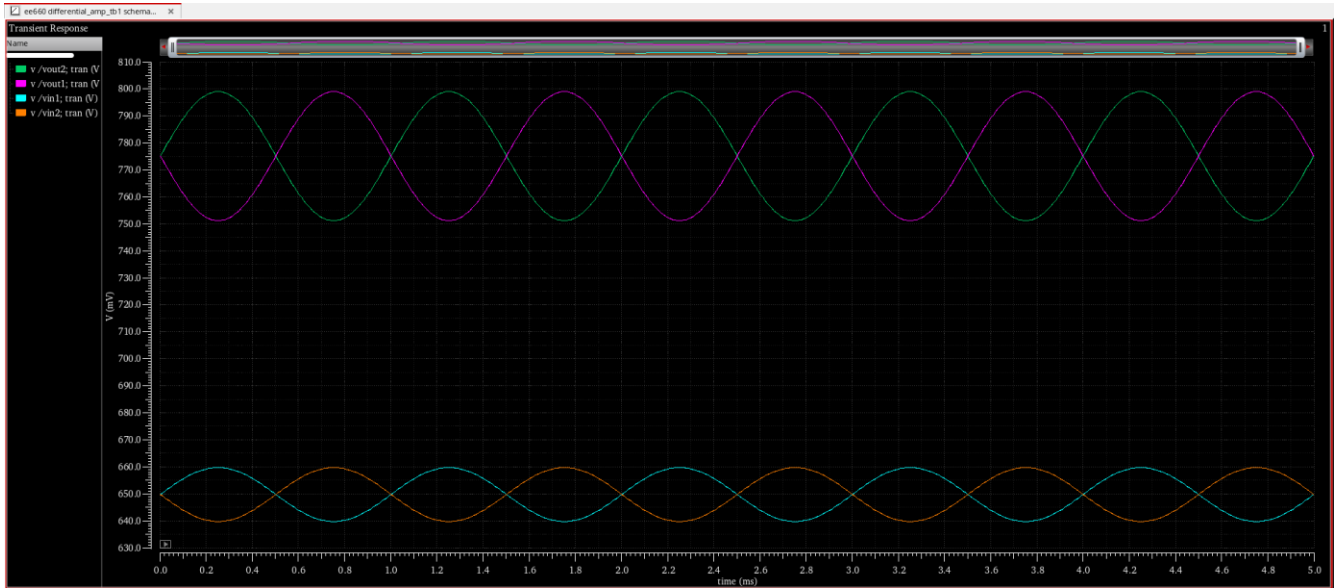


Figure:Plot showing $V_{in1}, V_{in2}, V_{out1}, V_{out2}$

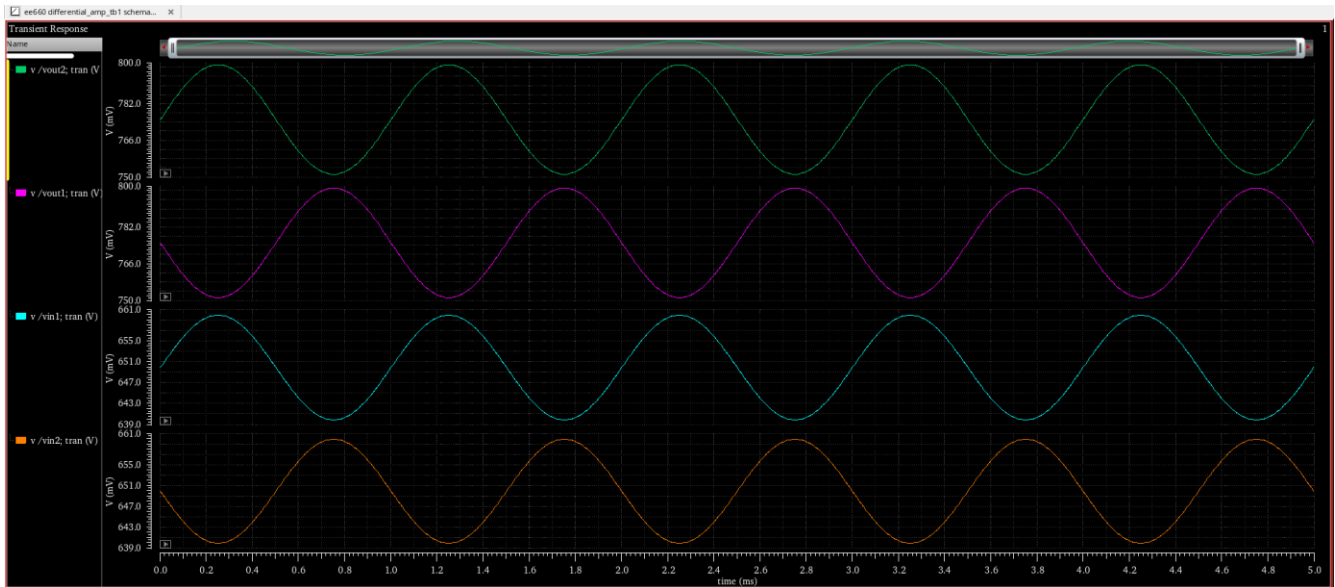


Figure:Plot showing $V_{in1}, V_{in2}, V_{out1}, V_{out2}$

Observation: From the above plot it is evident that V_{in1}, V_{out1} are out of phase and V_{in2}, V_{out2} are out of phase.

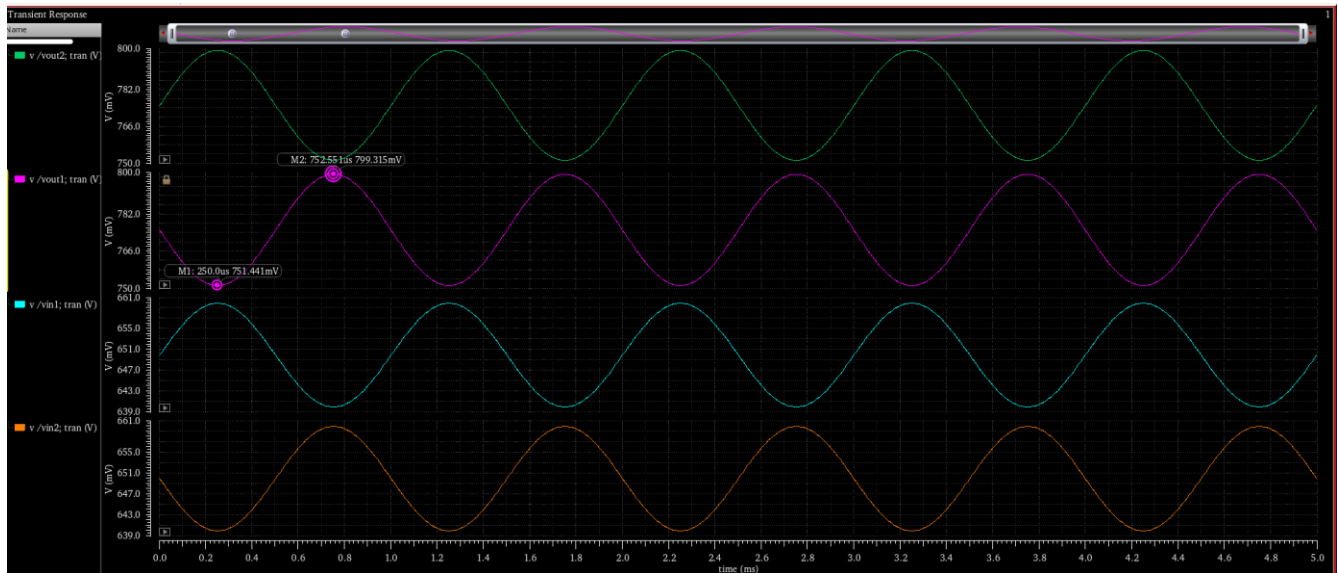


Figure:Plot showing Vin1,Vin2,Vout1 ,Vout2

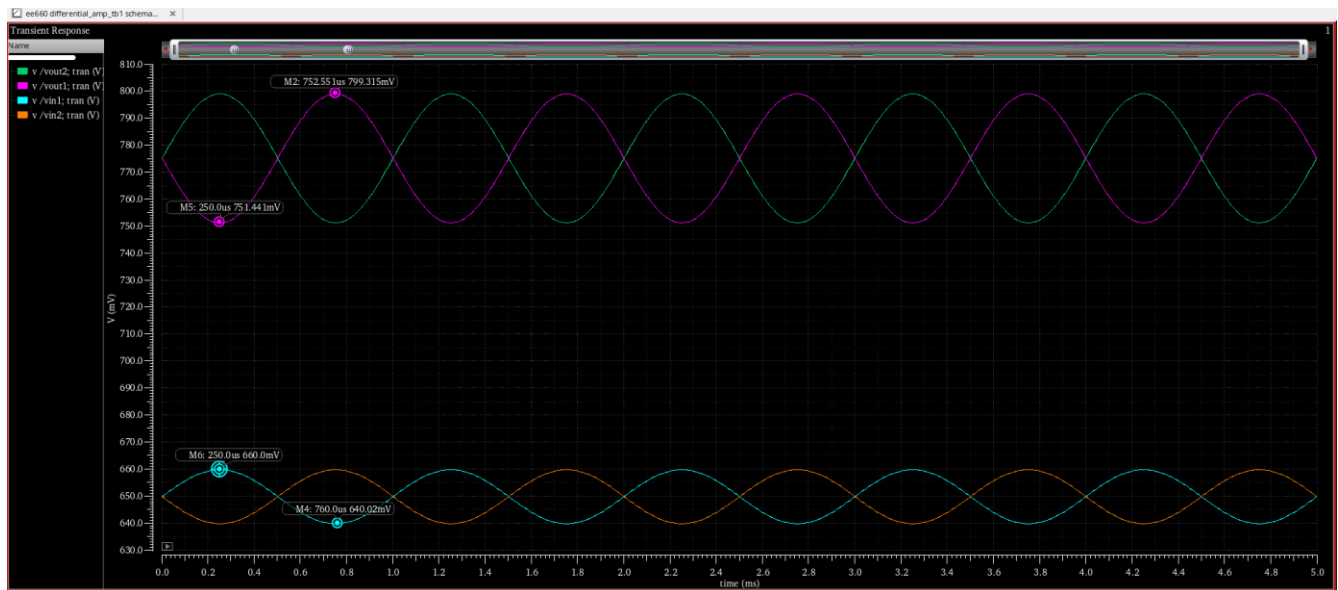


Figure:Plot showing Vin1, Vout1 with min and max points highlighted

Observation:

Vout1max=799.31mV

Vout1min= 751.44mv

Vdiff swing =2x(Vout1max-vout1min)=2 x47.87=95.74mV

Vin,pp=20mv

Av =Vout1,pp/ Vin,pp = 2.39

Below are the results when input small signal input voltage is 20mV:

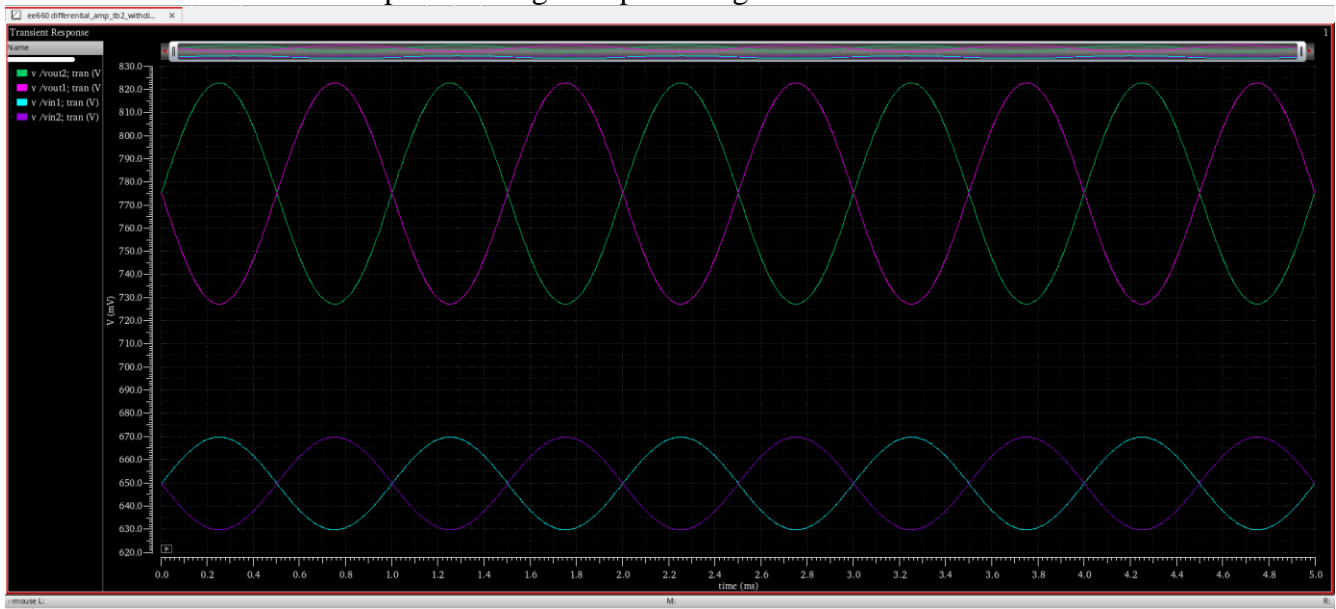


Figure:Plot showing $V_{in1}, V_{in2}, V_{out1}, V_{out2}$

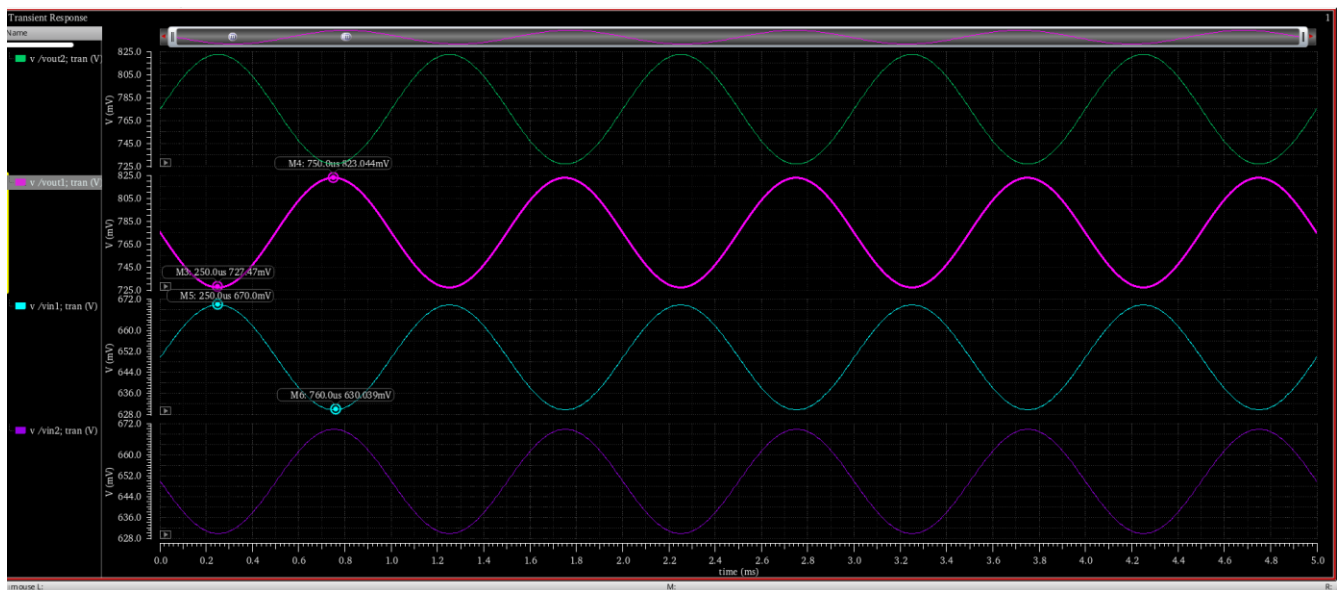


Figure:Plot showing V_{in1}, V_{out1} with min and max points highlighted

Observation:

$V_{out1\text{max}} = 823\text{mV}$

$V_{out1\text{min}} = 727\text{mV}$

$V_{diff \text{ swing}} = 2 \times (V_{out1\text{max}} - v_{out1\text{min}}) = 2 \times 96 = 192\text{mV}$

$V_{in,pp} = 40\text{mV}$

$A_v = V_{out1,pp} / V_{in,pp} = 2.4$

The circuit diagram illustrates a differential amplifier with a common-mode feedback (CMFB) loop. The input stage consists of two NMOS transistors, M_1 and M_2 , whose sources are connected to a common node. This node is biased by a PMOS transistor, M_3 , which is connected to V_{DD} . The gates of M_1 and M_2 are driven by a differential-mode input signal v_{in1} . The gates of M_3 and M_4 are driven by a common-mode input signal v_{in2} . The output of the differential pair is taken from the drains of M_1 and M_2 , which are connected to V_{DD} through load resistors R_1 and R_2 . The common-mode feedback loop is implemented using a PMOS transistor, M_5 , whose gate is connected to the common-mode output v_{out2} and whose source is connected to the common source node of M_1 and M_2 . The drain of M_5 is connected to V_{DD} . The common-mode output v_{out2} is also connected to the gates of M_1 and M_2 through a coupling capacitor C_1 . The differential-mode output v_{out1} is taken from the drain of M_1 . The circuit is simulated using a differential amplifier block, which is configured to have a differential-mode input v_{in1} and a common-mode input v_{in2} . The differential-mode output v_{out1} and common-mode output v_{out2} are shown. The circuit is simulated using a differential amplifier block, which is configured to have a differential-mode input v_{in1} and a common-mode input v_{in2} . The differential-mode output v_{out1} and common-mode output v_{out2} are shown.

Transient Analysis Simulation Results:



Explanation of above differential Circuit operation:

Here V_{in1} is sinusoidal voltage source with 10mv ac amplitude and 0.65v dc voltage, whereas V_{in2} has only dc voltage of 0.65V .Since , v_{in2} is fixed circuit will respond to the changes in the v_{in1} . The tail current source (M3) provides a fixed total current that is split between M1 and M2. When V_{in1} increases above V_{in2} , M1 draws more current, and M2 draws less. Since the total current remains constant, the current flowing through M1 and M2 adjusts in an opposite manner. This current variation directly affects the drain voltages V_{out1} and V_{out2} .

When V_{in1} increases (positive half-cycle of AC input)

M1 draws more current \rightarrow Voltage drop across R_D increases $\rightarrow V_{out1}$ decreases.

M2 draws less current \rightarrow Voltage drop across R_D decreases $\rightarrow V_{out2}$ increases.

When V_{in1} decreases (negative half-cycle of AC input)

M1 draws less current \rightarrow Voltage drop across R_D decreases $\rightarrow V_{out1}$ increases.

M2 draws more current \rightarrow Voltage drop across R_D increases $\rightarrow V_{out2}$ decreases.