

# Report

- Schematics, Layouts, Simulation Results, DRC, LVS and PEX comparison Reports enclosed for Inverter, 2 Input NAND, 3 Input NAND, J-K Flip Flop, and Mod 5 Synchronous Counter.
- Post Layout Simulation Reports included for J-K Flip Flop and Counter.
- **All Layouts have a height (span y axis) = 1407 nm**
- **Mod 5 Counter has a width (span on x axis) = 35287 nm**
- **Area of Counter Layout = 49.65 sq. um**
- All Layouts are made from scratch.
- Target of 1400 nm was not achieved because while cleaning up the DRCs, some layers moved by 2 or 3nm, which became hard to rectify later.
- Only the Counter layout has a screenshot showing scales as while exporting layout as image, scales were omitted from other layouts. All other layouts have the same height (1407 nm)
- For JK Flip Flop Simulation : Clk freq = 250 MHz,  
Input J has frequency = 125 MHz, input K has frequency = 62.5MHz
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- **For Counter Output : QC = MSB, QA = LSB**
- Counter takes 1 clock cycle to reset to 000.
- Counting starts in response to the clock edge at t=4ns. Outputs should be observed from 6ns.
- There is a delay of 1 clock cycle between the input and time at which output should be observed because the J-K flip flop is designed using Master Slave architecture, where the master operates on positive clock edge and slave on negative edge. Hence output at slave is reflected only after 1 clock cycle.
- Counter moves from 000 → 001 → 010 → 011 → 100 → 000 (QC QB QA respectively).
- Counter resets from 100 → 000 at 26ns.
- Operating Frequency ( Frequency range simulated for before excess glitches are introduced : 100 MHz → 2500 MHz
- Counter schematic simulated for frequency from 100 MHz to 2.5 GHz.
- Observed that with increasing frequencies, more glitches are introduced, which make it hard to read the waveform.
- Simulations for different frequencies for both schematic and Post layout analysis attached.

Table below mentions Rise and Fall Time for different gates

Simulation Results		
Freq = 250 MHz	Rise Time	Fall Time
Inverter	0.01ns	0.01ns
2 Input NAND	0.02ns	0.05ns
3 Input NAND	0.02ns	0.05ns
JK Flip Flop (Q)	0.04ns	0.05ns
JK Flip Flop (Q_BAR)	0.04ns	0.05ns

Following table captures Schematic Simulation results for Counter

Counter : Schematic Simulation			
Freq = 250 MHz	QC	QB	QA
Setup Time	3.8ns	3.8ns	3.8ns
Hold Time	0.16ns	0.16ns	0.16ns
Rise Time	0.04ns	0.05ns	0.07ns
Fall Time	0.05ns	0.07ns	0.1ns

Following table captures Post Layout Simulation results for Counter

Counter : Post Layout Simulation			
Freq = 250 MHz	QC	QB	QA
Setup Time	3.84ns	3.84ns	3.84ns
Hold Time	0.16ns	0.16ns	0.16ns
Rise Time	0.04ns	0.04ns	0.07ns
Fall Time	0.05ns	0.07ns	0.1ns