Report

- Schematics, Layouts, Simulation Results, DRC, LVS and PEX comparison Reports enclosed for Inverter, 2 Input NAND, 3 Input NAND, J-K Flip Flop, and Mod 5 Synchronous Counter.
- Post Layout Simulation Reports included for J-K Flip Flop and Counter.

- For JK Flip FLop Simulation **:** Clk freq = 250 MHz,
  Input J has frequency = 125 MHz, input K has frequency = 62.5MHz
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- **For Counter Output : QC = MSB, QA = LSB**

- Counter takes 1 clock cycle to reset to 000.
- Counting starts in response to the clock edge at t=4ns. Outputs should be observed from 6ns.
- There is a delay of 1 clock cycle between the input and time at which output should be observed because the J-K flip flop is designed using Master Slave architecture, where the master operates on positive clock edge and slave on negative edge. Hence output at slave is reflected only after 1 clock cycle.
- Counter moves from 000 → 001 → 010 → 011 → 100 → 000 (QC QB QA respectively).
- Counter resets from 100 → 000 at 26ns.
- Operating Frequency (Frequency range simulated for before excess glitches are introduced : 100 MHz → 2500 MHz

- **All Layouts have a height (span y axis) = 1407 nm**
- **Mod 5 Counter has a width (span on x axis) =35287 nm**
- **Area of Counter Layout = 49.65 sq. um**

- All Layouts are made from scratch.
- Target of 1400 nm was not achieved because while cleaning up the DRCs, some layers moved by 2 or 3nm, which became hard to rectify later.

- Counter schematic simulated for frequency from 100 MHz to 2.5 GHz.
- Observed that with increasing frequencies, more glitches are introduced, which make it hard to read the waveform.
- Simulations for different frequencies for both schematic and Post layout analysis attached.

Following table captures Post Layout Simulation results for Counter

Freq = 250 MHz	**QC**	**QB**	**QA**
Setup Time	1.88ns	1.88ns	1.88ns
Hold Time	0.17ns	0.17ns	0.17ns
Rise Time	0.04ns	0.04ns	0.07ns
Fall Time	0.05ns	0.07ns	0.1ns