ANALOG IC (ELP735)
PROJECT INTERIM REPORT
Date : 30/09/2021

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AIM : Design a 2- stage single ended OTA.
TOOL USED : Cadence Virtuoso
SPECIFICATIONS : FreePDK 45nm Technology

Parameter	Value
Ideal Current Source	10 uA
Power Supply	1.8 V
DC Gain	> 65 dB
UGB	100 MHz
Open Loop Phase Margin	> 60 deg
Open Loop Gain Margin	> 10dB
Input referred Noise (1k - 100 MHz)	70 uVrms
IM3 (2 Vpp differential signal)	> 62 dB
Common Mode Phase Margin	> 60 deg
Common Mode Gain Margin	> 10(dB)

RESULTS:

Note :

- All calculations have been handwritten and attached with this report.
- The hand-drawn schematic has been used as reference for all calculations.
- At the end of this report, snapshots of the amplifier schematic and biasing circuit, simulated in Cadence are also attached at the end. The values of parameters used for exact calculations are obtained from these simulations.

Amplifier Choice :

Folded Cascode single ended OTA is chosen as Stage 1 of the 2-stage op-amp. The reasons behind choosing this architecture are : this architecture is fairly simple to design since the bias voltages are independent of input common mode voltage; due to this simplicity, since, in the first cut trials approximate gain and input referred noise were achieved, hence this architecture was chosen. This does involve 1 extra biasing voltage, but in terms of understanding and calculations, since Vcm is not involved anywhere, the bias voltages and currents were relatively easier to achieve.

Stage 2 of this OTA is a PMOS Common Source Amplifier with NMOS as load. This nmos is biased using current sources such that both the transistors are always in saturation.

The circuit and calculations including all the formulas used are the very basic ones taught during the lectures. Currently, no improvements have been attempted for improving the total DC Gain of the circuit or further reducing the input referred noise. The focus of this report is only on DC biasing. All bias voltages are such that voltage between any 2 nodes of a transistor is less than 1V

For initial calculations, to find approximate bias voltage values, threshold and overdrive voltage values have been assumed based on dc simulation of a simple common source amplifier. The assumed values are :
Vovp = 400mV = 0.4V Vovn = 200mV = 0.2V
Vtp = 300 mV = 0.3V Vtn = 300 mV = 0.3V

Assumed Common Mode signal for simulations is Vcm = 1V (Vcm(max) = 1.3 V from attached calculations).

W/L ratios for each transistor of the amplifier is mentioned in the brackets in the hand-drawn schematic against the transistors.s Due to simulation non-idealities, W/L ratios do not match perfectly for matching the currents.
L is not common for all transistors; it has been modified to attain the required voltage drops.

For calculating values of gain and input referred noise, gm and ro that are used are values obtained after setting DC operating points. The simulated value of gain is actually what is seen in the plot (plots attached).

Following table mentions the values required to be achieved as per initial calculations and the actual values achieved from simulations :

Table 1. Calculated vs Simulated Parameter Values

Parameter	Calculated Value	Simulated Value
gm1	451 uS	443 uS
PTAIL	1.1 V	1.2 V
PCAS	0.7 V	1.19 V
NCAS	(0.5 , 1.3) V	0.700 V
NTAIL	(0.2, 1.6) V	0.533 V
Stage1 Gain	53 dB	54.98 dB
Stage2 Gain	34.9 dB	29.1 dB
Total DC Gain	87.98 dB	84.09 dB
Input Referred Noise	97.7uVrms	-

Following table mentions the parameters achieved against their expected values mentioned by specs (specs not mentioned are not addressed) :

Table 3. Achieved Results (Frequency Response parameters not addressed)

Parameter	Expected Value	Achieved Value
DC Gain	> 65 dB	84.09 dB
Input referred Noise (1k - 100 MHz)	70 uVrms	97 uVrms

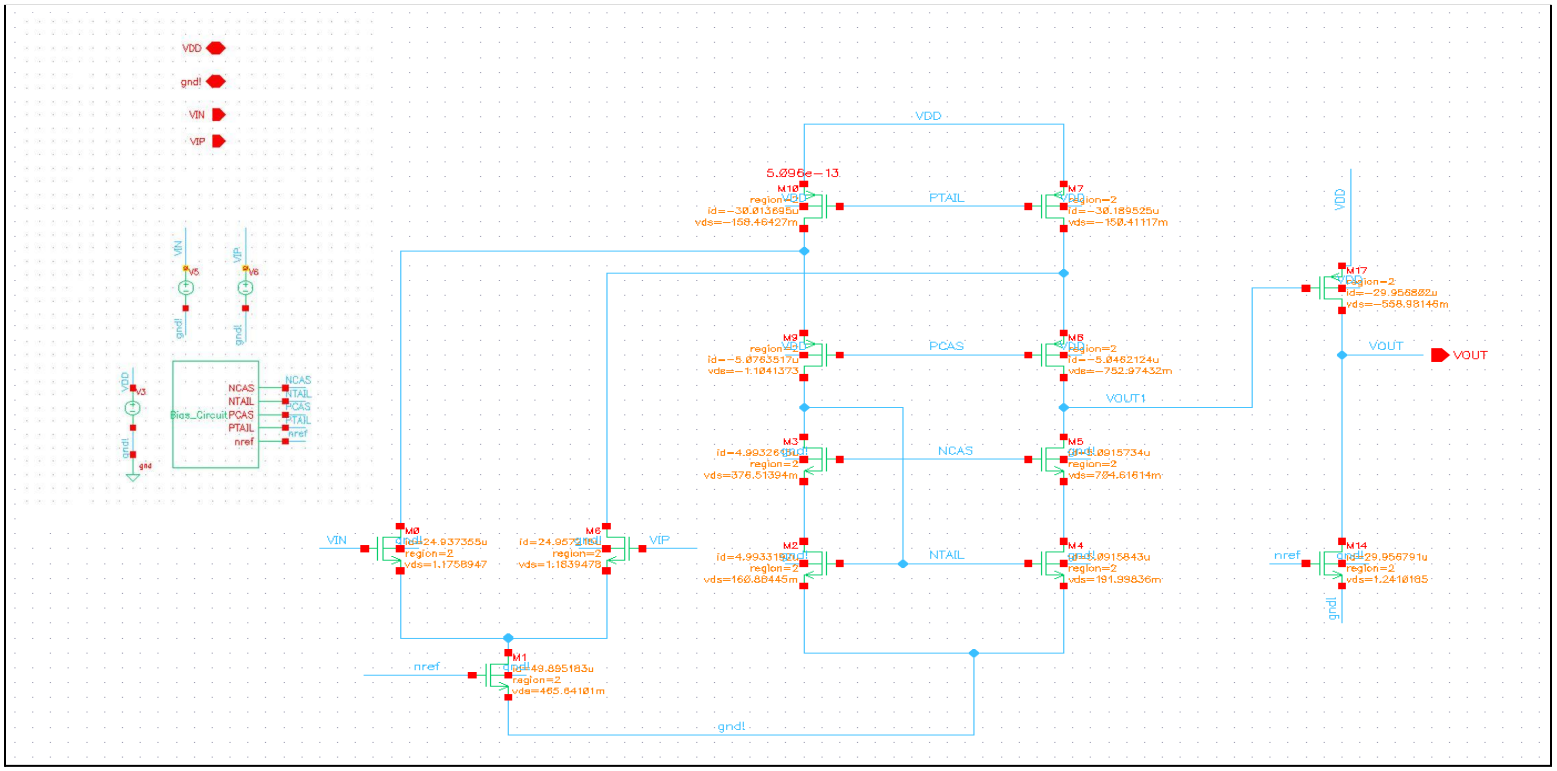

Fig 1. 2 Stage Single Ended Op-Amp using Folded Cascode OTA

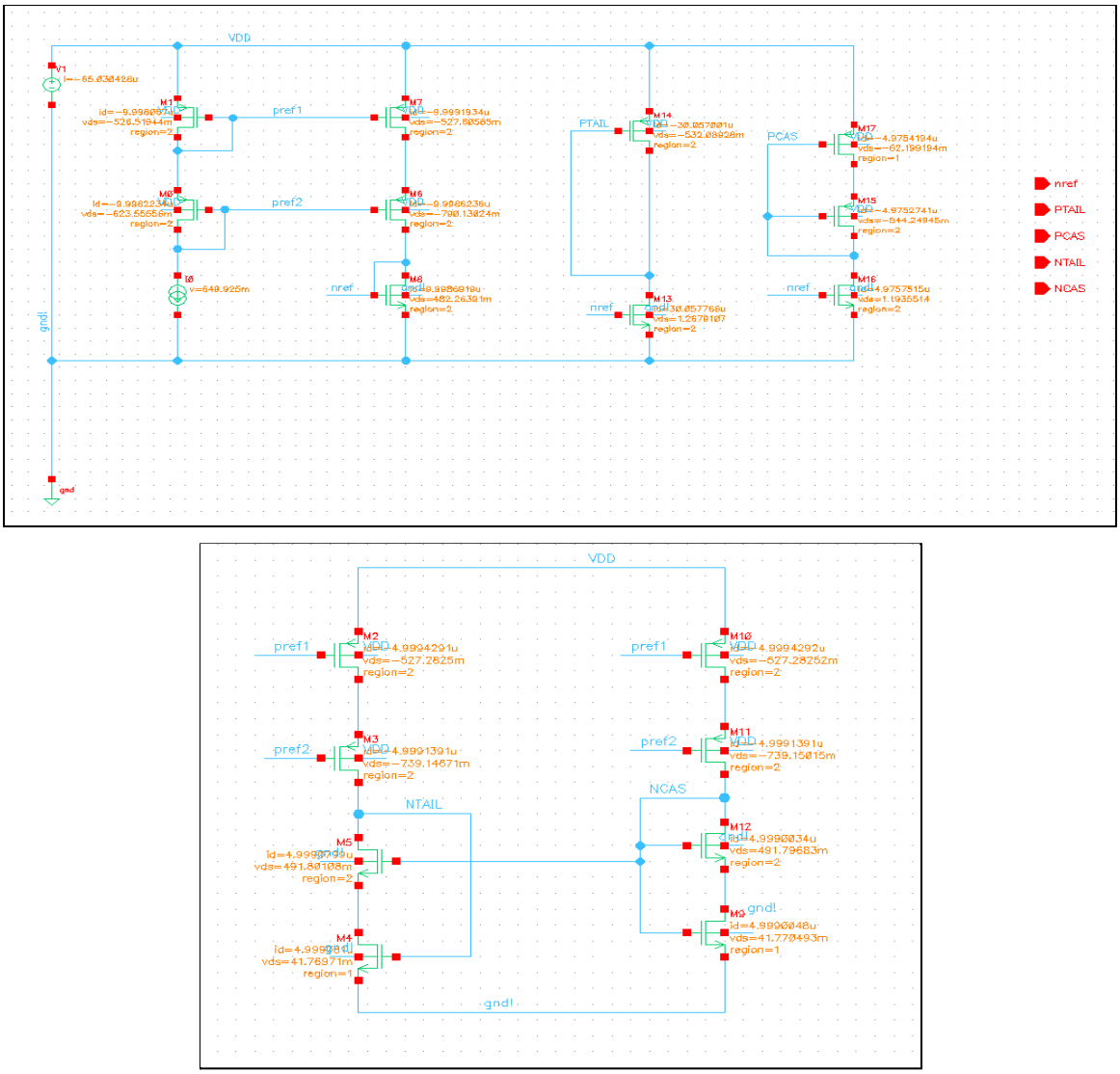

Fig 2. BIAS Generation Circuits

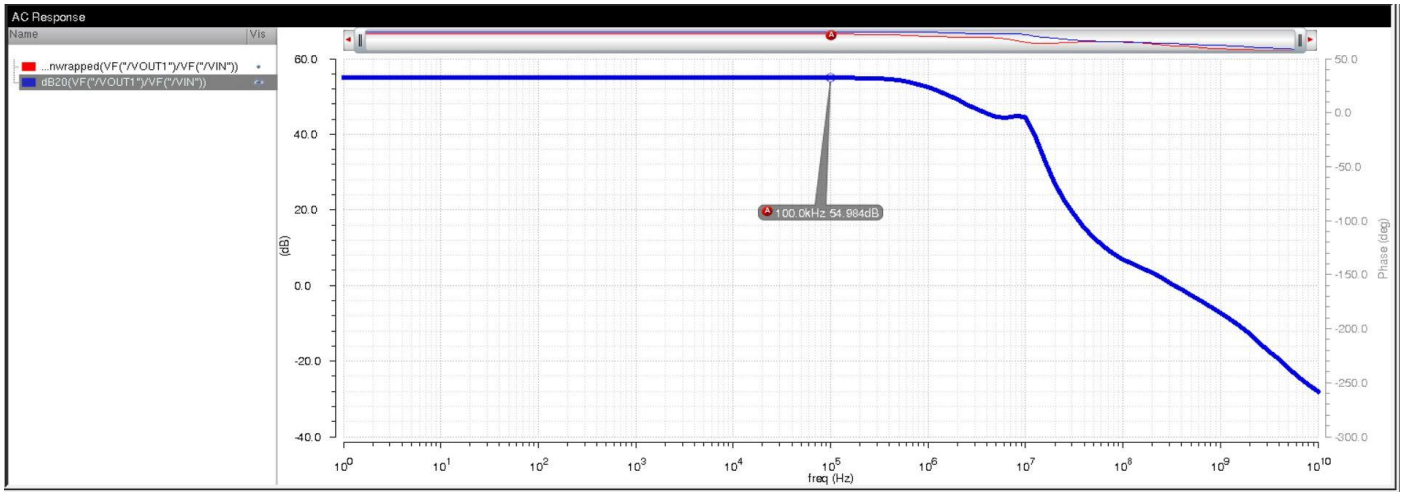

Fig 3. Stage 1(Folded Cascode OTA) Gain = 54.98 dB

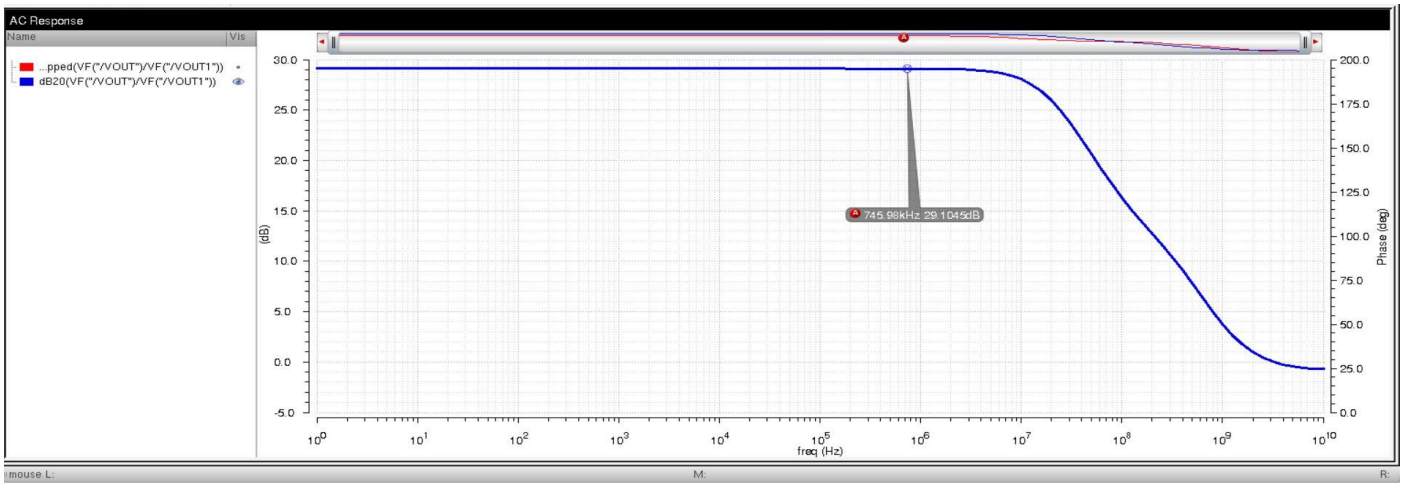

Fig 4. Stage 2(Common Source Amplifier) Gain = 29.1 dB

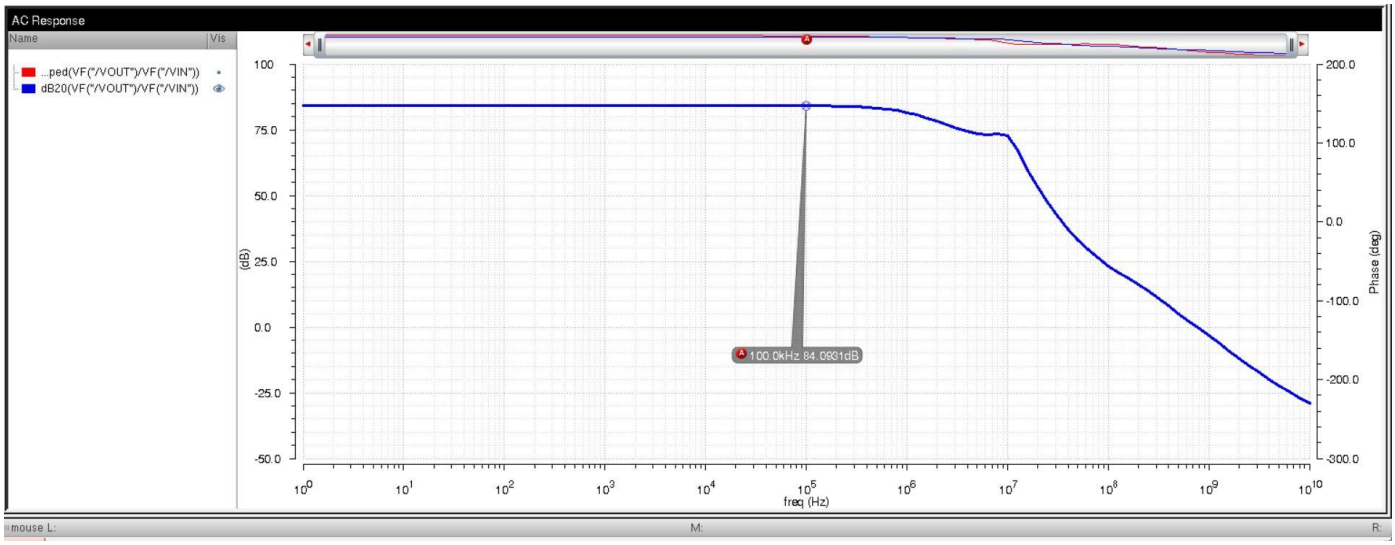

Fig 5. Total Gain of 2-Stage OTA = 84.09 dB