IECLAB (ELP831)
TASK 2 REPORT
Date : 16/10/2021

SRISHTI AGRAWAL (Entry No : 2021EEY7523)

GitHub Repository : https://github.com/srishti-1903/eey217523_Task2

AIM : Complete RTL2GDSII Flow on Mod 5 synchronous counter.
TOOLS USED : Vivado, Genus, Innovus
RESULTS:
No Setup violations reported at the end of Post Route stage.
No Hold violations reported at the end of Post Route Stage.
No DRC or connectivity violations reported at the end of Post Route Stage.
Area after Physical Implementation in Innovus = ***33.04 sq. um***
Area from hand-drawn layout using Cadence Virtuoso = ***49.65 sq. um***

Steps Followed :

Vivado : Directory = **rtl**

1. Simulated Mod5 Synchronous counter using verilog. Verilog file uploaded in github.

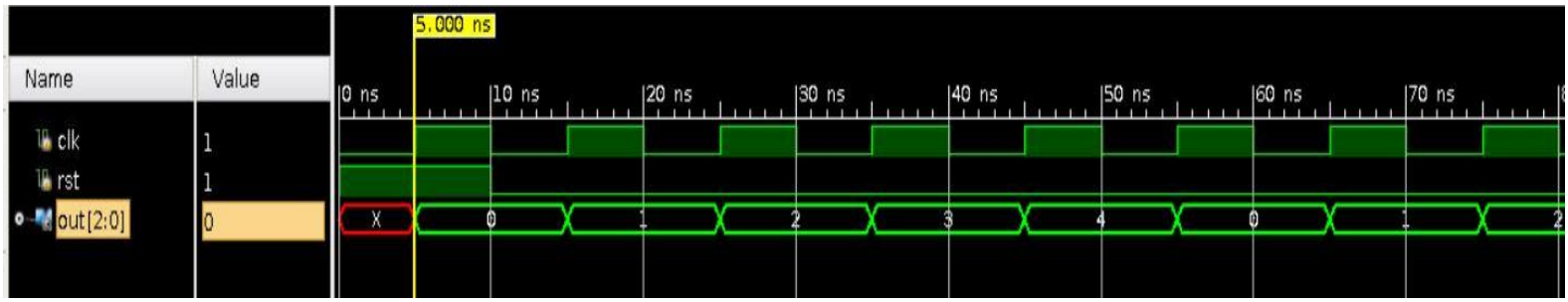


Figure 1. Mod 5 Counter Simulation Snapshot

Genus : Directory = ***synthesis***

1. Source synthesis script using command in genus shell : ***source synthesis.tcl***
2. All Generated files including timing reports as a result of synthesis are uploaded in GitHub.

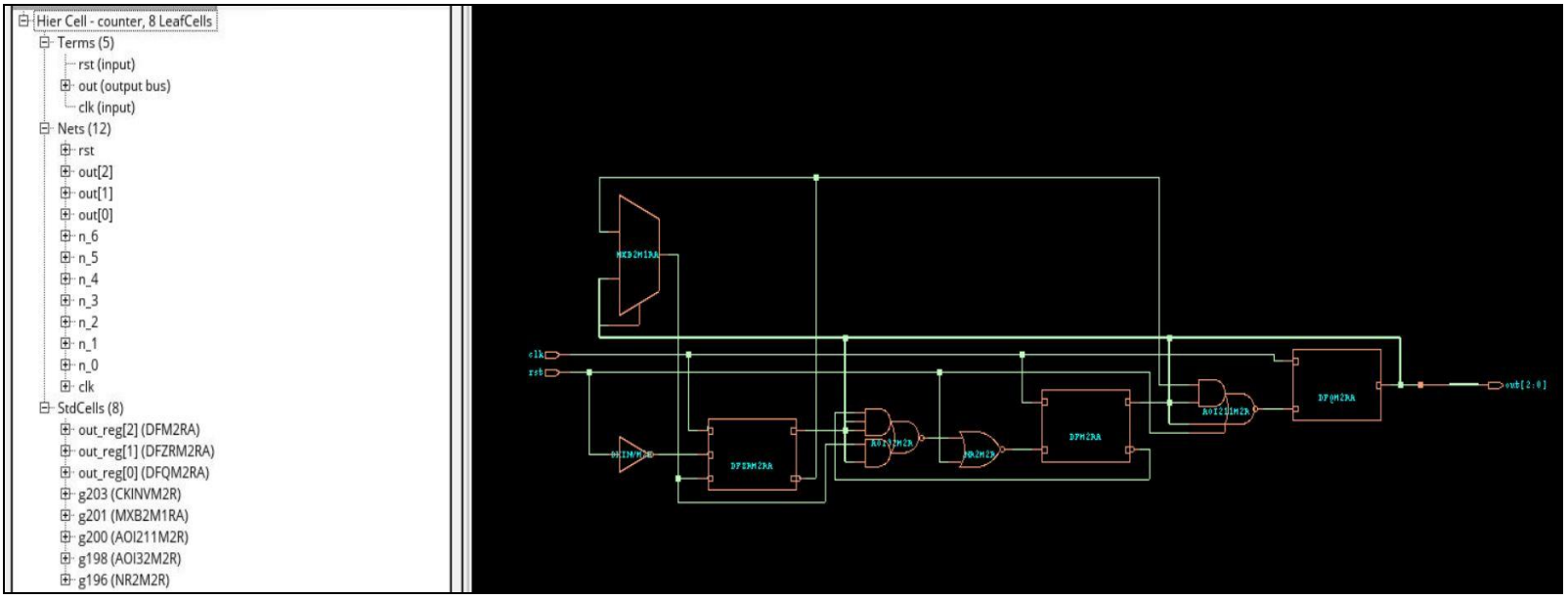
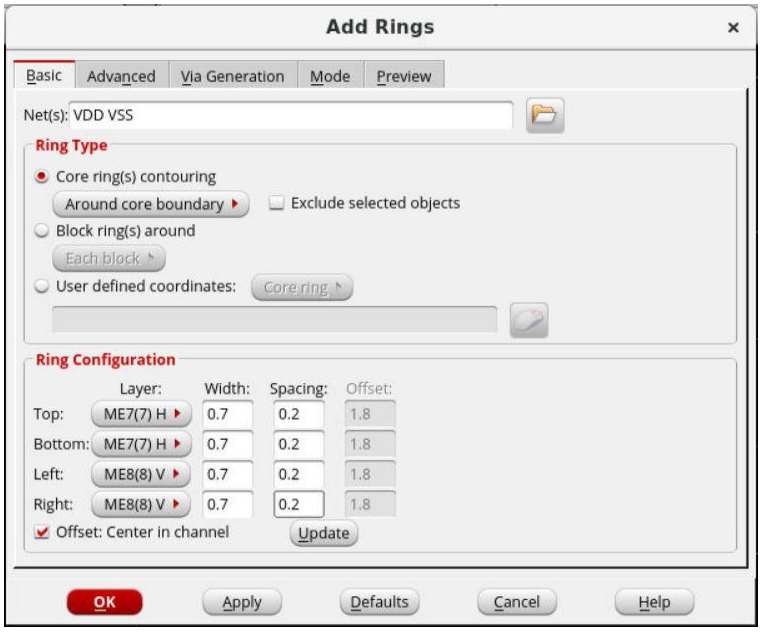


Figure 2. Mod 5 Counter Synthesized Netlist

Innovus : Directory = **physical_design**

1. In Innovus gui -> ***Import design*** (provide path to generated netlist, LEF file, best and worst case timing libraries, QRC tech file).
2. ***Floorplan -> Specify Floorplan***
3. After the module is loaded, ***Power Planning-> Add Rings and Power Planning-> Add Stripes***. Highest Metal Layers used here (M7 and M8).
4. ***saveFPlan counter.fp***



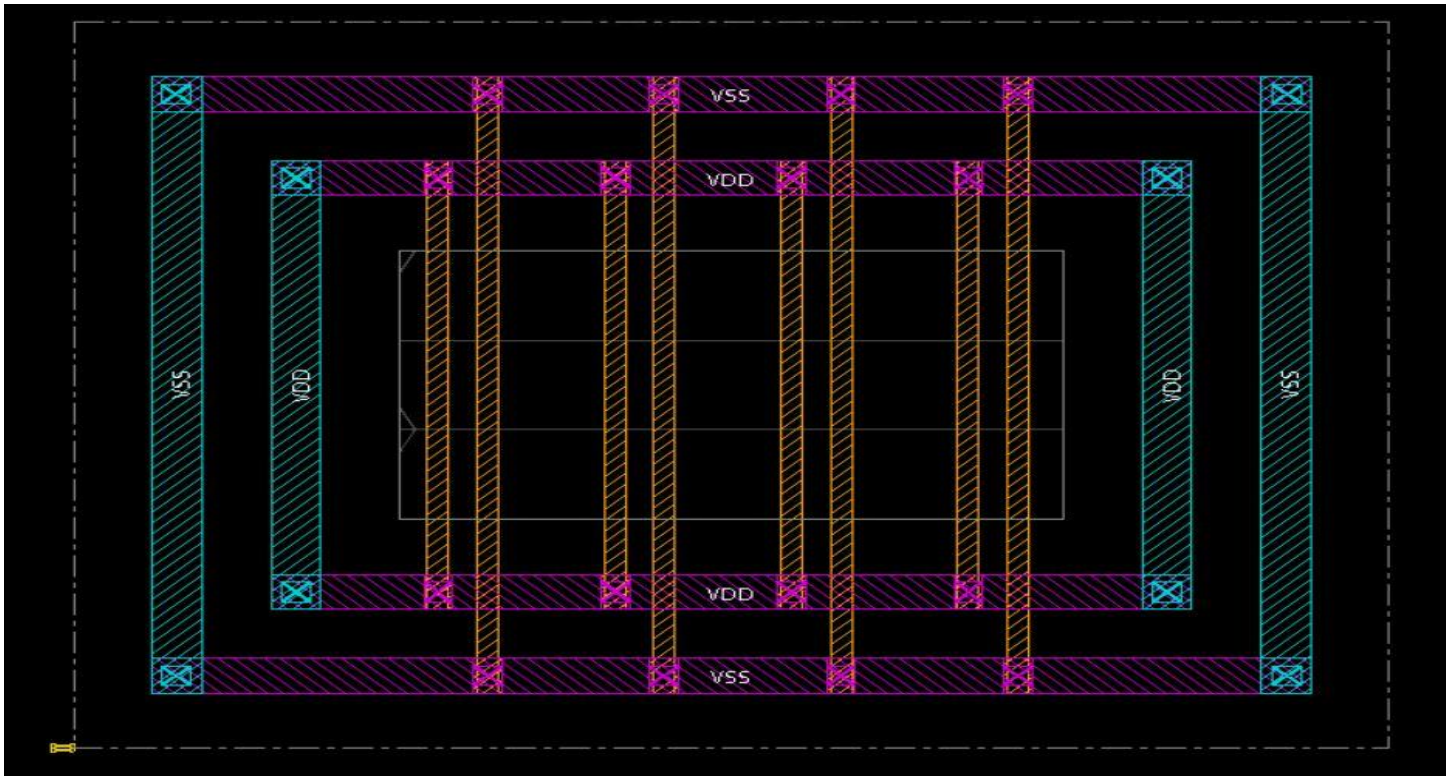


Figure 3. Power Planning Settings and Floorplan obtained snapshot

5. Before Routing connect global nets VDD and VSS with power pins of standard pins using golbalNetConnect command :
   a. ***globalNetConnect VDD -type pgpin -pin VDD -inst ****
   b. ***globalNetConnect VSS -type pgpin -pin VSS -inst ****
   c. ***globalNetConnect VDD -type tiehi***
   d. ***globalNetConnect VSS -type tielo***
   e. ***globalNetConnect VDD -type tiehi -pin VDD -inst ****
   f. ***globalNetConnect VSS -type tielo -pin VSS -inst ****

6. ***Route → Special Route.***

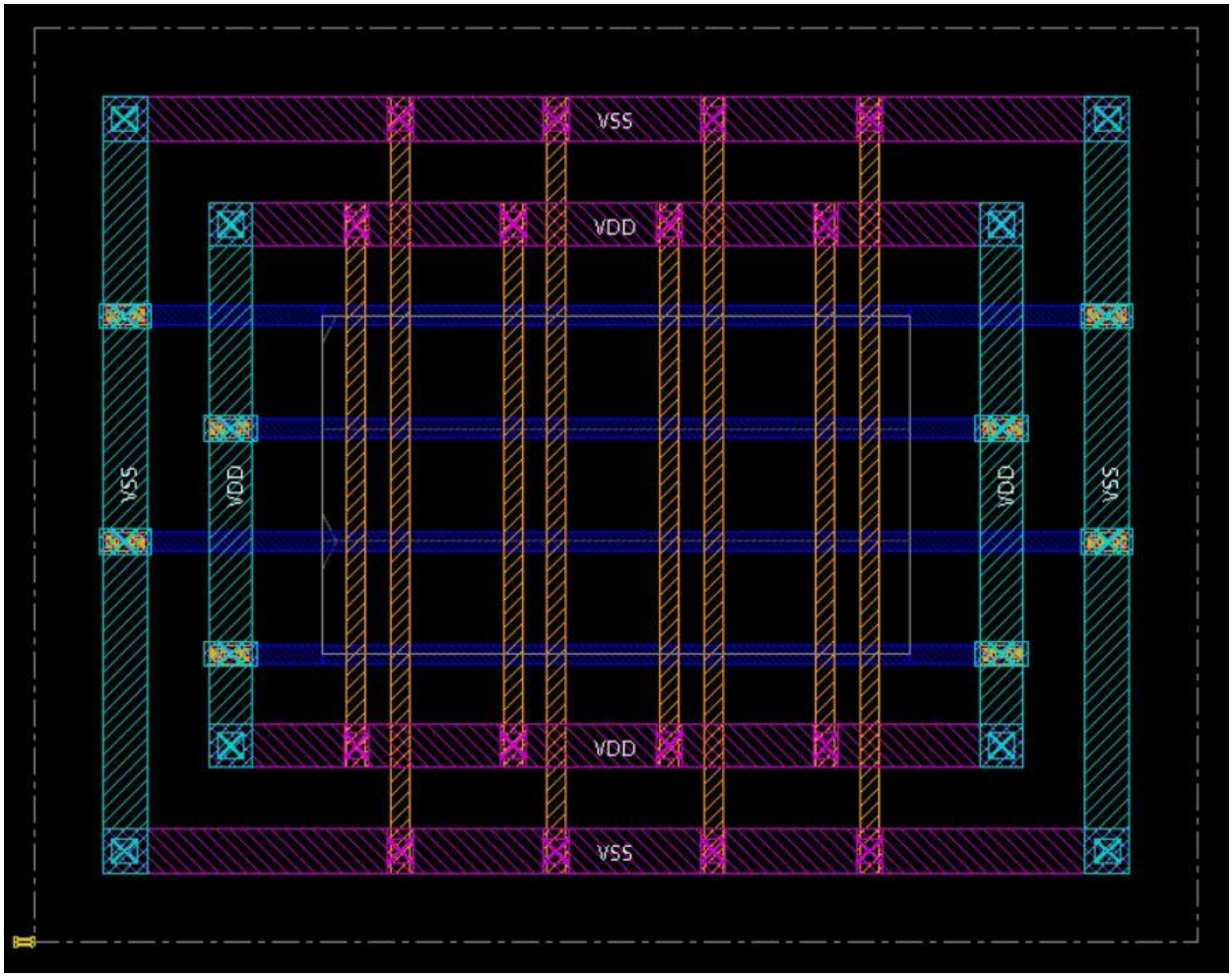


Figure 4. Design after Special Route step before place_opt

7. Run placement, generate reports and save place db *:*
    a. ***place_opt_design > placeOpt.log***
    b. ***report_timing -summary > report_timing_placeOpt.rpt***
    c. ***timeDesign -preCTS > timeDesign_preCTS.rpt*** → ***No Setup violations are reported***
    d. ***timeDesign -preCTS -hold > timeDesign_hold_preCTS.rpt*** → ***No Hold violations are reported***
    e. ***report_power > report_power > report_power_preCTS.rpt***
    f. ***report_area > report_area_preCTS.rpt*** → ***Reported Area = 33.48 sq um***
    g. ***saveDesign placeOptDesign***

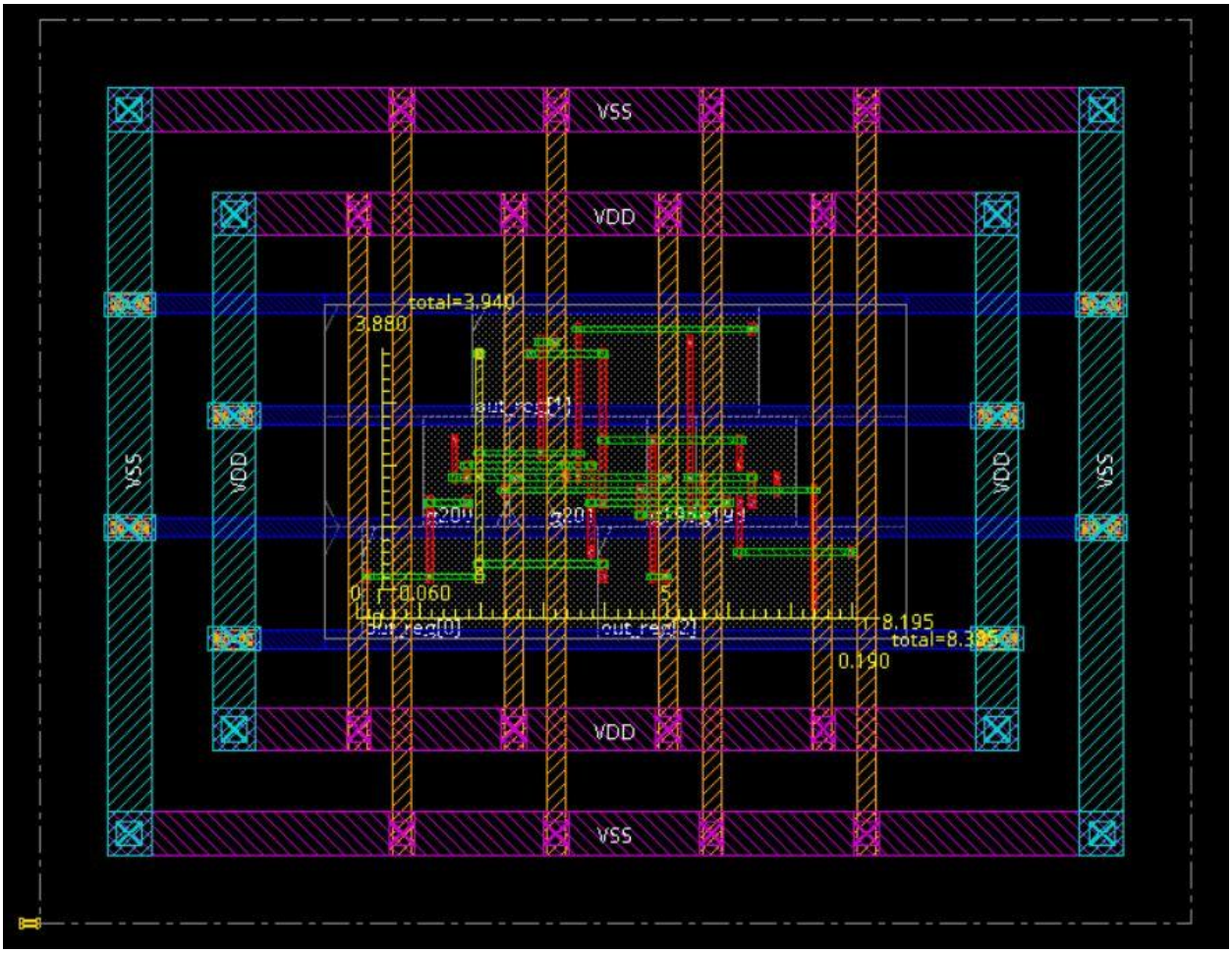


Figure 5. Design after place_opt_design command

8. Generating CTS specs :

   create_ccopt_clock_tree_spec > create_ccopt_clock_tree_spec.log

9. Running Clock tree synthesis :
   a. *ccopt_design > ccopt_design.log*
   b. *timeDesign -postCTS > timeDesign_postCTS.rpt* → *No Setup violations are reported*
   c. *timeDesign -postCTS -hold > timeDesign_hold_postCTS.rpt* → *No Hold violations are reported*
   d. *report_power > report_power_postCTS.rpt*
   e. *Report_area* → *Reported Area = 33.48 sq um*
   f. *saveDesign postCTSDesign*

10. *Route* → *Nano Route* → *Route*
    a. saveDesign routeDesign

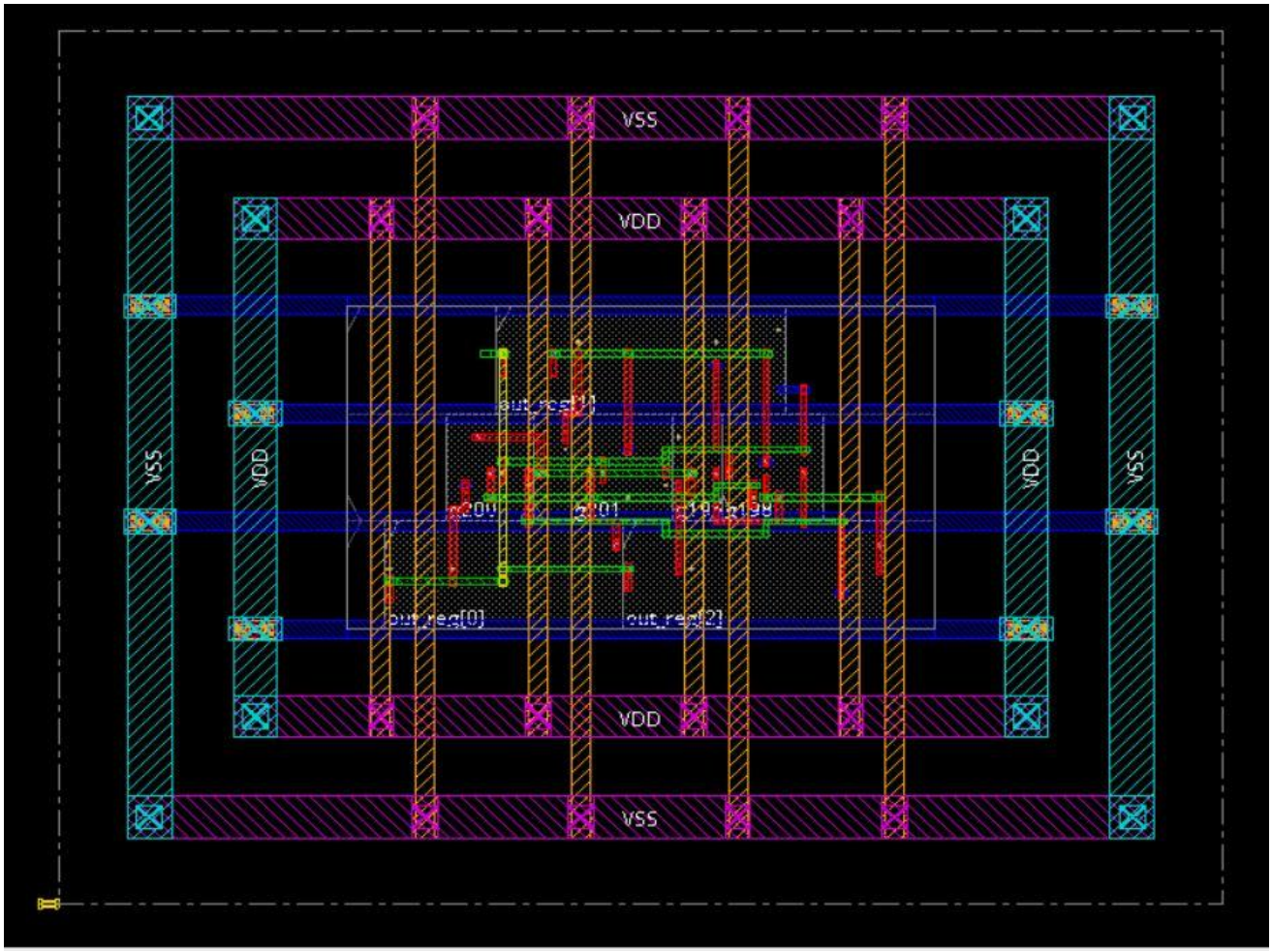


Figure 6. Final Design after Route step : PostRotue

11. Extract RC timing and generate timing reports
    a. ***extractRC***
    b. ***rcOut -spef counter.spef -rc_corner Default_rc_corner***
    c. ***setAnalysisMode -analysisType onChipVariation***
    d. ***timeDesign -postRoute > timeDesign_postRoute.rpt*** → ***No Setup violations are reported***
    e. ***timeDesign -postRoute -hold > timeDesign_hold_postRoute.rpt*** → ***No Hold violations are reported***
    f. ***report_power > report_power_postRoute.rpt***
    g. ***report_area > report_area_postRoute.rpt*** → ***Reported Area = 33.48 sq um***

12. Verify DRC violations and connectivity violations
    a. ***verify_drc > verify_drc_postRoute.rpt*** → ***No DRC violations are reported***
    b. ***verifyConnectivity > verifyConnectivity_postRoute.rpt*** → ***No connectivity violations are reported***

13. Setup Static Power Analysis for worst case and max delay corner.

14. Connect global nets
    a. ***globalNetConnect VDD -type pgpin -pin VDD -inst ****
    b. ***globalNetConnect VSS -type pgpin -pin VSS -inst ****
    c. ***globalNetConnect VDD -type tiehi***
    d. ***globalNetConnect VSS -type tielo***
    e. ***globalNetConnect VDD -type tiehi -pin VDD -inst ****
    f. ***globalNetConnect VSS -type tielo -pin VSS -inst ****

15. Run Power Analysis. Power analysis reports uploaded in github in the folder ***physical_deisgn/power_analysis.***
    a. ***Total Internal Power = 0.001626 mW***
    b. ***Total Switching Power = 0.00018 mW***
    c. ***Total Power = 0.001812 mW***
    d. ***Total Leakage Power = 6.439e-06 mW***

16. Setup Rail Analysis and run Net based Rail Analysis for power net VDD. Results uploaded in github in folder ***physical_design/rail_analysis***

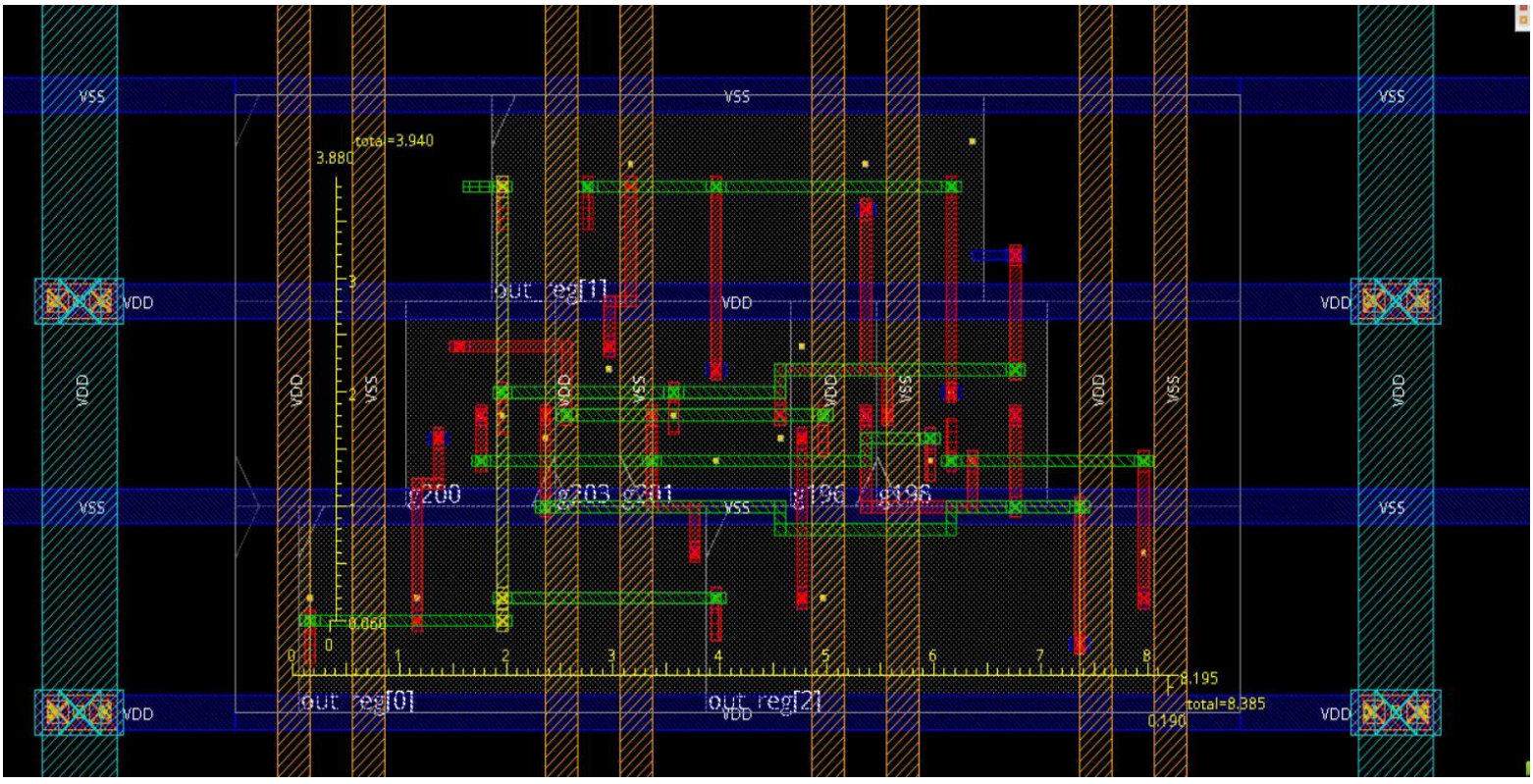


Figure 6. Height and Width measurement for area calculation : Height = 8.385 um, Width = 3.940