Siddhant Srivastava

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Location : Bengaluru, Karnataka, India

SKILL SET

Language	Python, Perl, Bash, C, C++
Familiar with	GIT, C++(11/14), VUE JS, HTML
Tools/ Framework	Makefile, MySQL, Django
OS	Linux/Unix

PROFESSIONAL EXPERIENCE

Intel Technology (India) Pvt. Ltd. (Nov 2018- Present)

As TFM Lead (Emulation & FPGA build), my responsibilities are:

- To reduce users' migration effort from simulation to emulation platform.
- To develop new methodologies to reduce TAT for emulation build.

Major Works:

- Developed and architected single handedly, an alternative build solution for emulation & fpga flows, under Intel's first ever light framework; *(Perl, Bash, Makefile)*
  - Challenged standard DV solution.
  - Customer preferred and selected this alternative solution.

  Now leading the effort to migrate whole DV space towards this solution. *(Python, Bash, Makefile)*
- Envisioned and developed "Error Reporting System"*(Perl, Bash)*
  - An auto debugger is invoked with every failure and do a root-cause-analysis, if possible.
  - Reduced design team dependency on tool/flow developers.
  - Now, we are saving this debug info for future ML solutions.

Achievements:

- Marked as "Critical Talent" from our division (globally), and recognized by Intel CEO "Pat Gelsinger".
- "Hybrid Emulation Solution" for multi-die model where different die can be in different frameworks. Received "DRA", highest engineering award in PESG division.
- Closely collaborated with customer to help them to use new framework and build emulation model in record time. Received "SEM", highest engineering award in Intel Validation Division.
- Under new framework, "Emulation & FPGA" space have:
  - Reduced "consultation" tickets by 10x.
  - Close to zero "showstopper" ticket.

Mentor Graphics (India) Pvt. Ltd. (July 2009- Oct 2018)

Our objective is to improve quality and timely delivery of emulation products.

Key Responsibilities:

- Solutions to maintain quality which can not to be tracked through regular QA-regression.
- Solutions to maximize hardware resources throughput.
- Interface for easy and efficient regression analysis.
- Provide end to end support to achieve and retain ISO 26262 certification.
- Automation of different processes required for successful completion of nightly and weekend regression.
- Provide framework for automated testing of new compilation and emulation flow.

Major Works:

- A web based solution, having services for following items: *(Python, Perl, Bash & Django framework)*
  - Tracking missed commits: Finding code-changes, not present in child branches.
  - Regression results & analysis.
  - Sign-off a release for ISO certification.
- Queuing System: Two different type of queuing mechanism: *(Perl, Bash)*
  - Emulation Queuing System
  - Simulation of SGE (basic features)
- Other major projects are live DB update; space optimization; sandbox approach for infra; automated corrective measures to save a regression run; tracking software and hardware stability for new platform; simplification and automation of regression launch in different flows.

Achievements:

- Reduced regression analysis and reporting effort by 20x.
- Increased emulation throughput by 5x.

INTERNSHIP

Mentor Graphics India Pvt Ltd	Verification of PCIe's Data Link Layer & implementation of scoreboard	May-Jun 2008
Institute of Technology, BHU	Speech Signal- analysis and sine wave synthesis	May-Jun 2007

EDUCATION

Degree	Institute	DGPA / %	Year
B.Tech (Electronics Engineering)	Indian Institute of Technology, BHU (**IIT(BHU), Varanasi**)	8.10 (Absolute Grading)	2009
Class XII (U.P.)	Mahatma Gandhi Intermediate College, Gorakhpur	76% (UP Board)	2004
Class X (U.P.)	Mahatma Gandhi Intermediate College, Gorakhpur	72% (UP Board)	2002