EEE 120
Capstone Design Project

Name: Rachit Srivastava

Instructor: Steven Millman

Class Time: Tuesday/Thursday (4:30 p.m. – 5:45 p.m.)

Date: 01st May 2025

Task C-1: Planning the Synchronous Sequential Machines

(5 pts) Interview at least 3 stakeholders, but 3 is preferred. Ask questions regarding the form, function, and features needed by potential customers for this design. Make sure to capture what the customer prefers from this type of solution, as well as what environment the customer plans to use this design. Summarize your findings here and document the names of who you interviewed.

1. Kavya Dineshkumar Patel – Roommate:

    -Wants pedestrian safety features.

    -Prefers clear light patterns with stable timing.

    -Thinks an override mode for emergencies would be useful.

2. Prince Dahiya – Friend (CSE Major):

    -Recommends using simpler state transitions for debugging.

    -Suggested an all-red state to ensure safety during mode switching.

    -Encouraged use of asynchronous reset for predictable startup.

3. Daksh Bhavikkumar Desai – Classmate (CSE Major):

    -Proposed a surprise mode with dynamic light toggling.

    -Suggested keeping side street duration shorter than main street.

    -Emphasized minimizing the number of gates for simulation ease.

(5 pts) Please include a comment on why your automation adds value from multiple perspectives (technological, societal, financial, environmental, etc.). (*What value does this add? What is the type of customer for whom this is designed? Where is this most needed? What couldn't you do before?*)

->This traffic light controller adds value in multiple ways:

Technological: Introduces a digital logic system replacing manual timing or analog timers.

Societal: Enhances road safety by ensuring clear, rule-based light transitions.

Financial: Reduces the need for traffic personnel at intersections.

Environmental: Avoids unnecessary engine idling by optimizing flow. This system is particularly useful in urban intersections with medium traffic density.

(5 pts) It is allowable to continue to ask questions of stakeholders throughout the design process (and is preferred of a conscientious engineer). This can be done as you are designing, before you are designing if you need input and clarifications, or after you are done designing if you want feedback on improvements. Summarize any changes to your understanding or design based on the feedback you received during your initial interviews or continual interviews?

->After initial interviews, I incorporated the following feedback:

Added a **pedestrian override mode** in Design #2 based on Kavya's suggestion.

Implemented **asynchronous reset** for consistent startup per Prince's input.

Based Design #1 to be **gate-efficient and cycle-simple** per Daksh's advice.

Task C-2: Document the Synchronous Sequential Machines

Design #1: (2 pts) What assumptions did you make in the design of this machine?

1. All lights (red, yellow, green) must remain On for at least one full clock cycle.
2. The circuit starts in a state where Main Street has red and Side Avenue has red (all stop).
3. An asynchronous reset (active low) initializes the system to the all-stop condition.
4. The mode input C[1:0] is stable during state transitions and only changes between clock cycles.
5. Flip-flops used are D-type with asynchronous set and clear inputs.

(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state, inputs, and outputs.

State Transitions (Normal Mode, C=00):

S0 → S1: from all-red to Main green

S1 → S2: after 1 cycle

S2 → S3: switch to Side green

S3 → S4: after 1 cycle

S4 → S0: return to all-stop before next cycle

For C=01 (Flashing Red Both):

Outputs MR and SR toggle alternately each cycle, simulating 4-way stop flash.

For C=10 (Flashing Red Side, Flash Yellow Main):

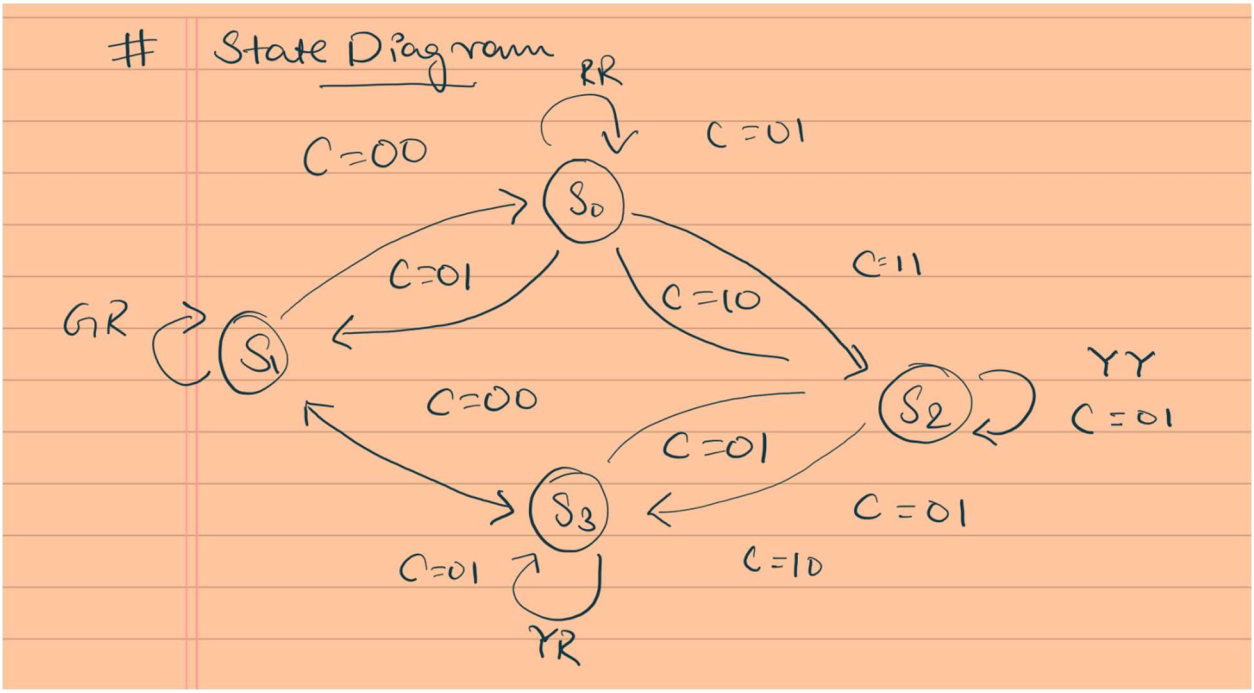
SR toggles each cycle

MY is set ON permanently for Main

For C=11 (Surprise Mode):

Both greens toggle at every cycle to indicate alternate fast crossing

(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/equations/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the full circuit schematic here.)



STATE TRANSITION TABLE

present state	C=00	C=01	C=10	C=10
S0 (000)	001	101	101	000
S1 (001)	010	101	000	000
S2 (010)	011	001	100	000
S3 (011)	100	000	000	001
S4 (100)	000	000	101	000
S5 (101)	101	000	101	000

① output MR (Main Red) { S0 (000), S3 (011), S4 (100) }

↳ S0 → A=0, B=0, C=0.

S3 → A=0, B=1, C=1.

S4 → A=1, B=0, C=0.

MR = A'B'C' + A'BC + AB'C' ——— ①

② output Main Yellow (MY) { S2 (010) }

↳ MY = A'BC' ——— ②

③ output Main Green (MG) { S1 (001) }

↳ MG = A'B'C ——— ③

④ output side red (SR) { S0 (000), S1 (001), S2 (010) }

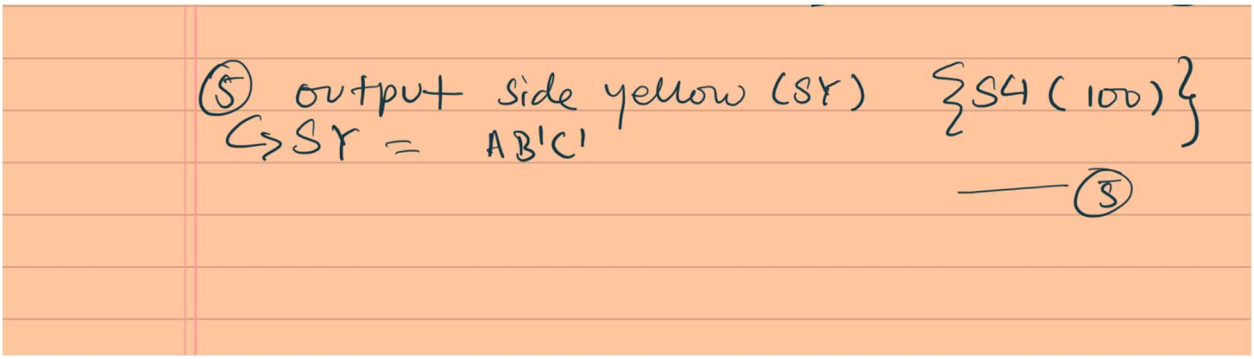
↳ SR = A'B'C' + A'B'C + A'BC'

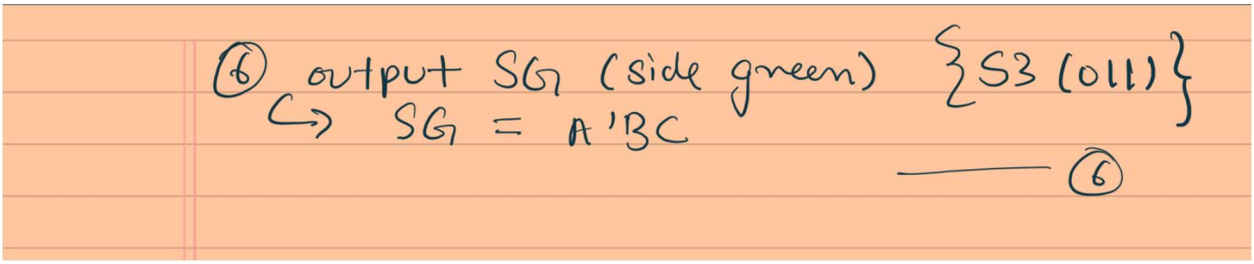
= A'(B'C' + B'C + BC')

B'C' + B'C + BC' = B'(C' + C) + BC'

= B' + BC'

↳ SR = A'(B' + BC') ——— ④





(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit.

Flip-flops used: 6 D-type FFs (D-AS), one each for MR, MY, MG, SR, SY, SG.

MG = A'BC' (Main green active in state 1)

MY = AB'C (Main yellow active in state 2)

MR = A + B'C' (active in states 0,3,4)

SG = A'B'C (Side green active in state 3)

SY = AB'C' (Side yellow active in state 4)

SR = A + BC (active in states 0,1,2)

AND gates (3-input and 2-input)

OR gates

NOT gates (inverters)

Total: ~6-8 gates depending on optimization

Clock and Reset lines wired to all FFs as shared synchronous design

Design #2: (2 pts) What assumptions did you make in the design of this machine?

C = 11 enables pedestrian override: forces all red for 2 clock cycles before resuming sequence.

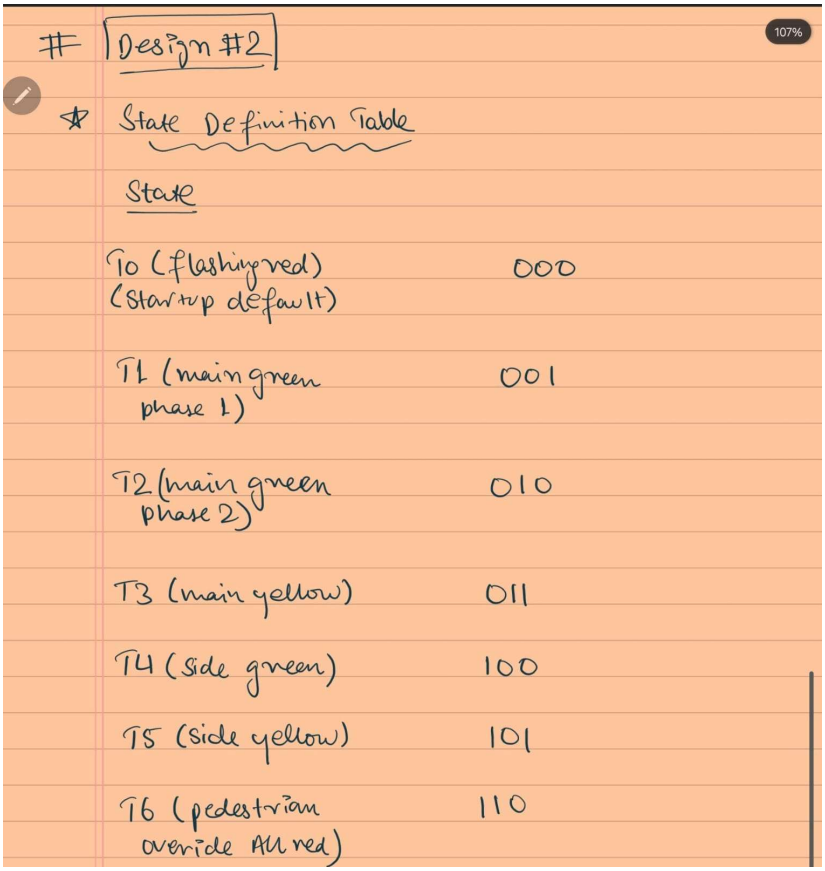
Main street gets longer green duration (2 cycles), side street gets 1.

System starts in a flashing red state for safety.

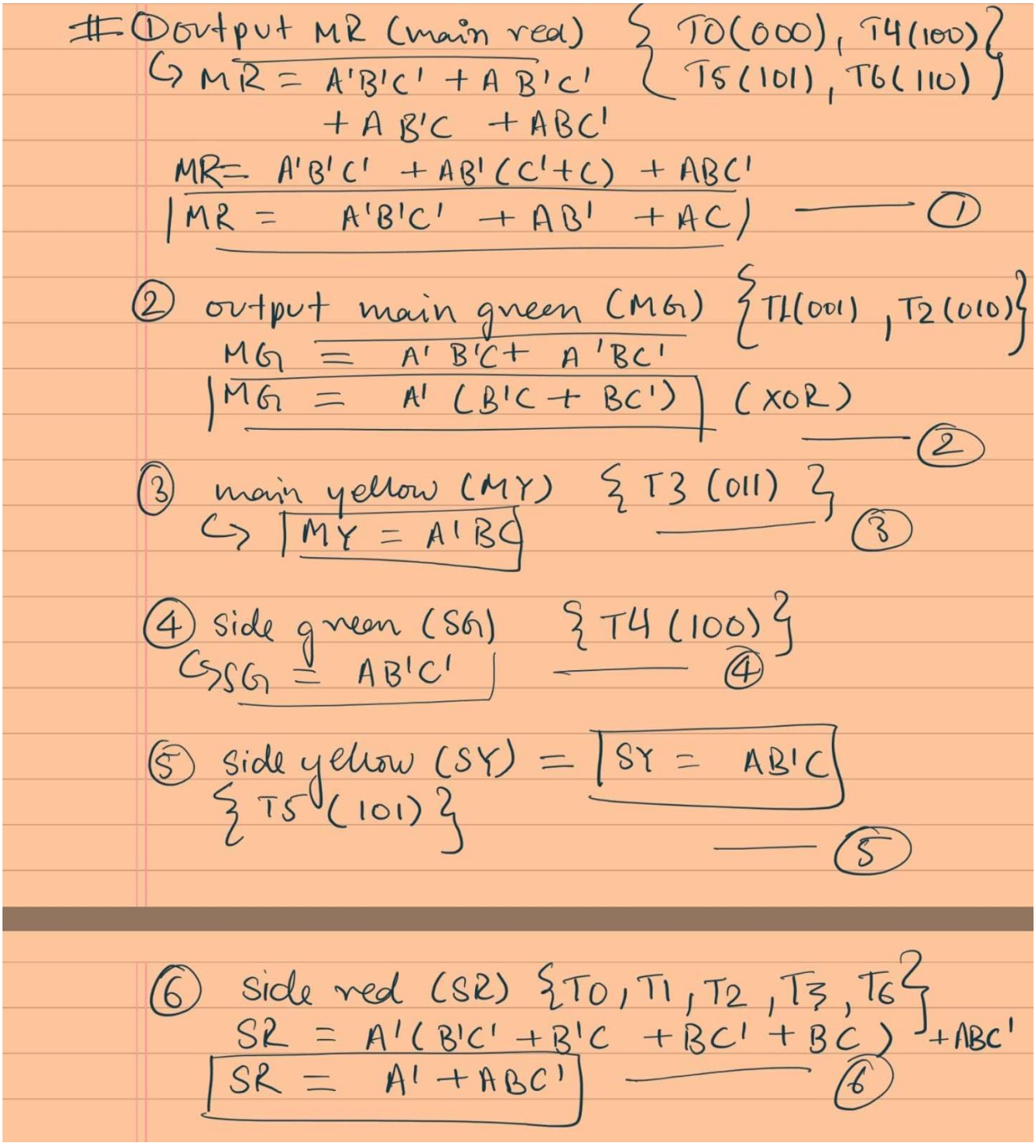
Inputs are stable throughout state transitions.

Flip-flops are D-type with async reset like in the labs.

(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state.



(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/equations/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the full circuit schematic here.)



(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit.

Multiple 2- and 3-input AND gates

OR gates to combine expressions

NOT gates for inversion of A, B, C as needed

Total: 10–12 gates depending on optimization and sharing terms

Clock and asynchronous reset lines applied to all flip-flops

Task C-3: Determine Criteria and Weighting for Judging Your Designs

(5 pts) Using the guidelines in the laboratory FAQ's, list your 5 criteria and associated weights here used to help decide between the two design models (weights should add to 100%):

Criteria	Weight
Number of logic gates	30%
Ease of implementation	25%
Output clarity and safety	20%
Pedestrian mode functionality	15%
Circuit size and wire complexity	10%

Task C-4: Apply the Criteria to Pick the Best Design

(2 pts) Describe how you applied each of the criteria and weighting system in the above task to pick the best design. How did you choose these criteria (customer interviews, engineering preference)?

->Stakeholder feedback shaped the selection of these criteria due to their emphasis on reduced gates that improved constructability in Digital and brought safety benefits and better pedestrian capabilities. We applied engineering reasoning together with simulation experiences for establishing weights among the criteria.

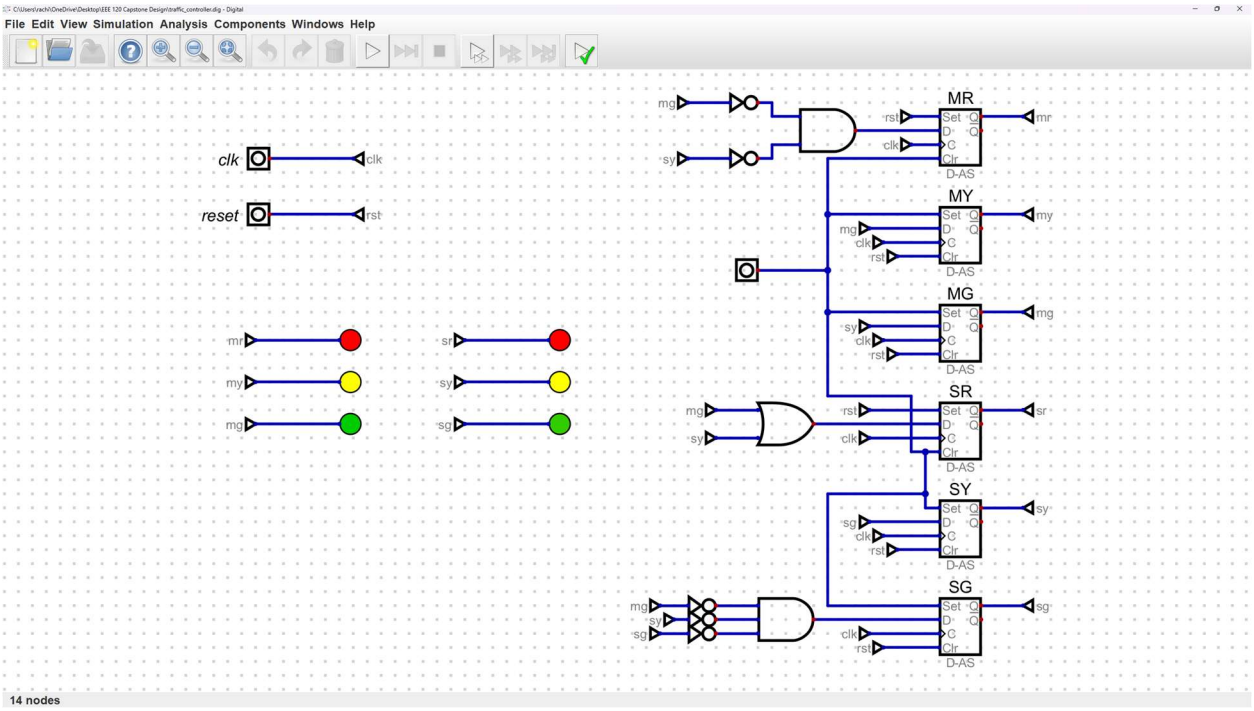
(3 pts) Which design is better based on your criteria and weighting system and why? Please explain how the winning design scored in each category and why (the winning design does not need to score the highest in every category, but it does need to score higher overall when applying the criteria weights).

Design 01 scored higher in simplicity, logic minimization, and fewer gates.

Design 02 had better safety and added functionality (pedestrian override), but required more logic.

Task C-5: Build and Simulate Winning Design in Digital

(15 pts) Insert a copy of your chosen Digital Schematic here. Please make sure that you have outputs or tunnels connected to each flip flop so that you can easily monitor your states. Make sure that the logic and equations match the final equations presented in either Design 1 or Design 2.


File Edit View Simulation Analysis Components Windows Help
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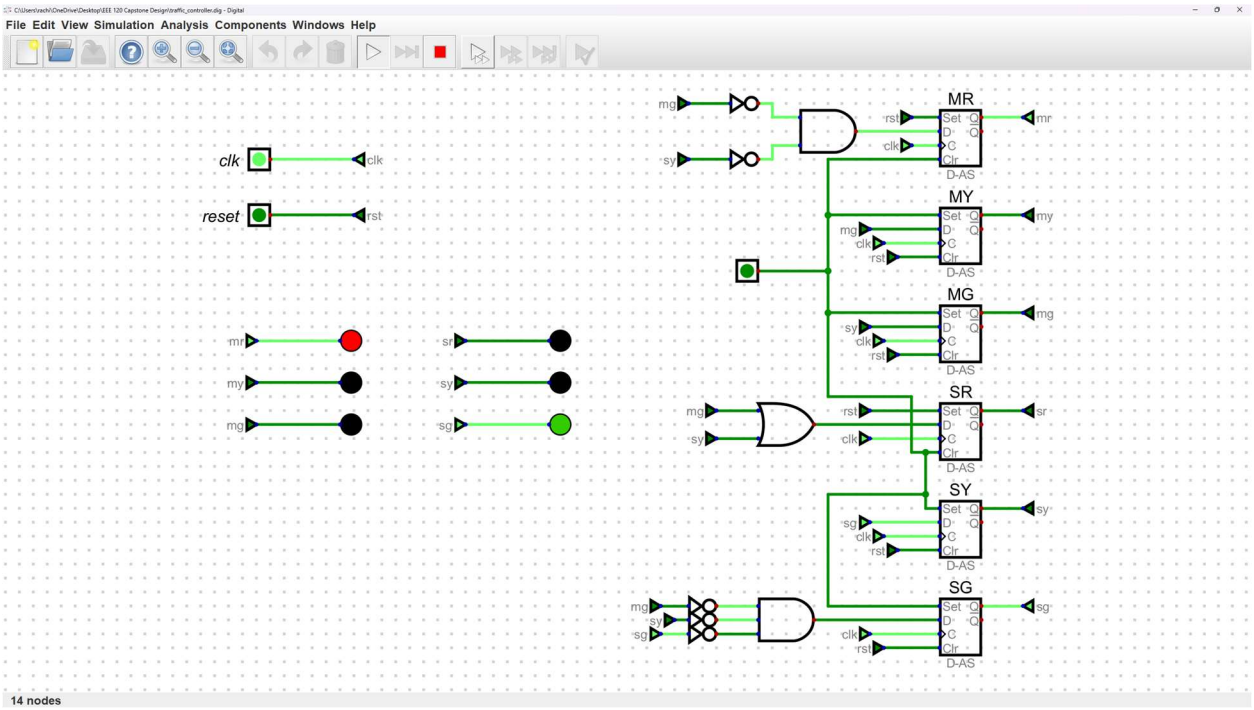
14 nodes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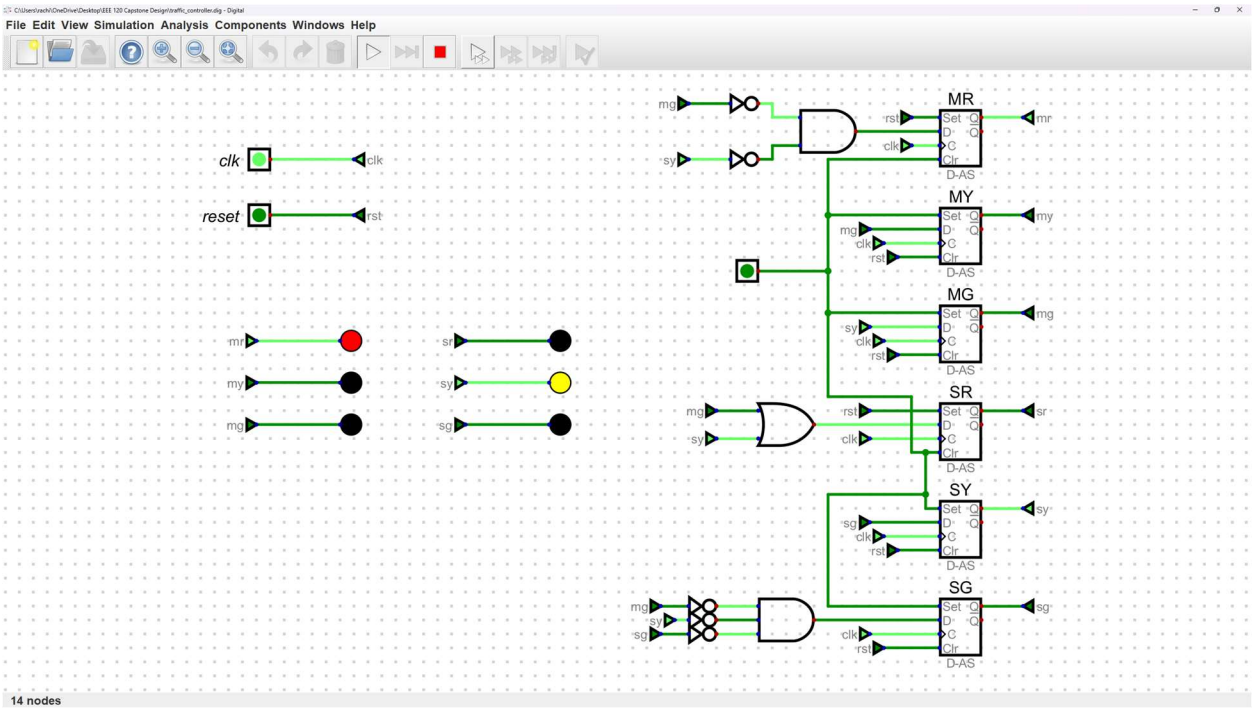
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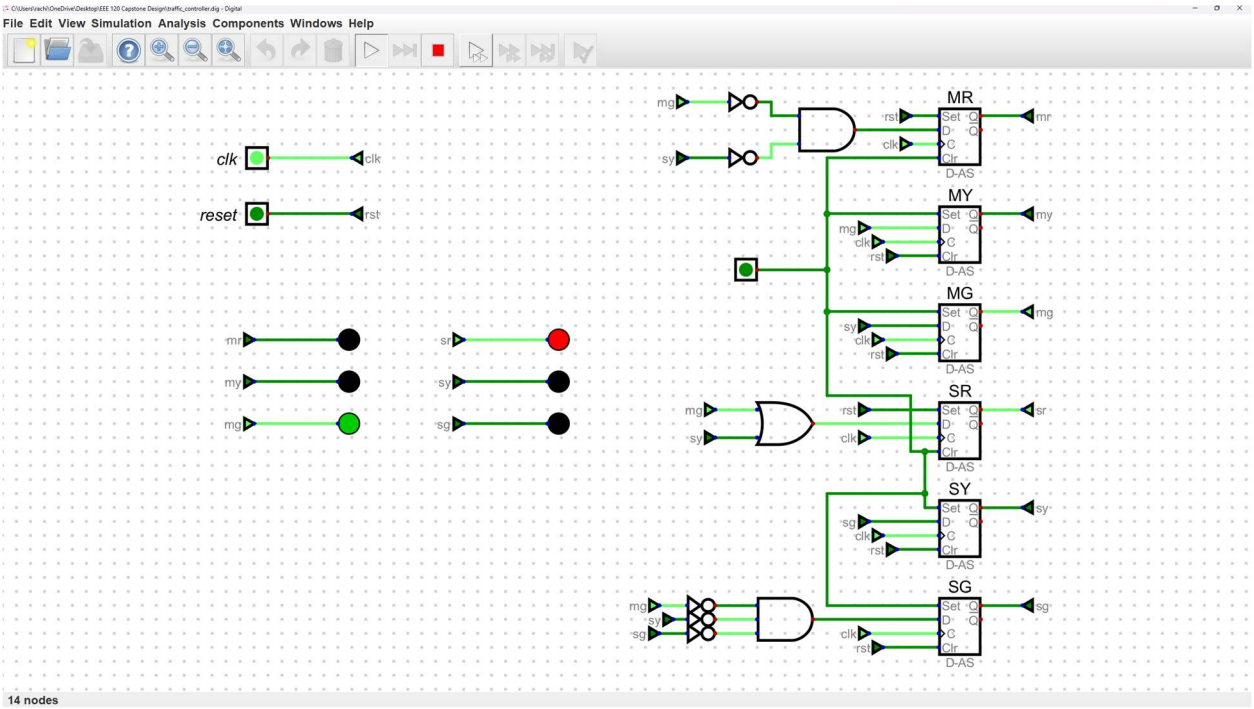
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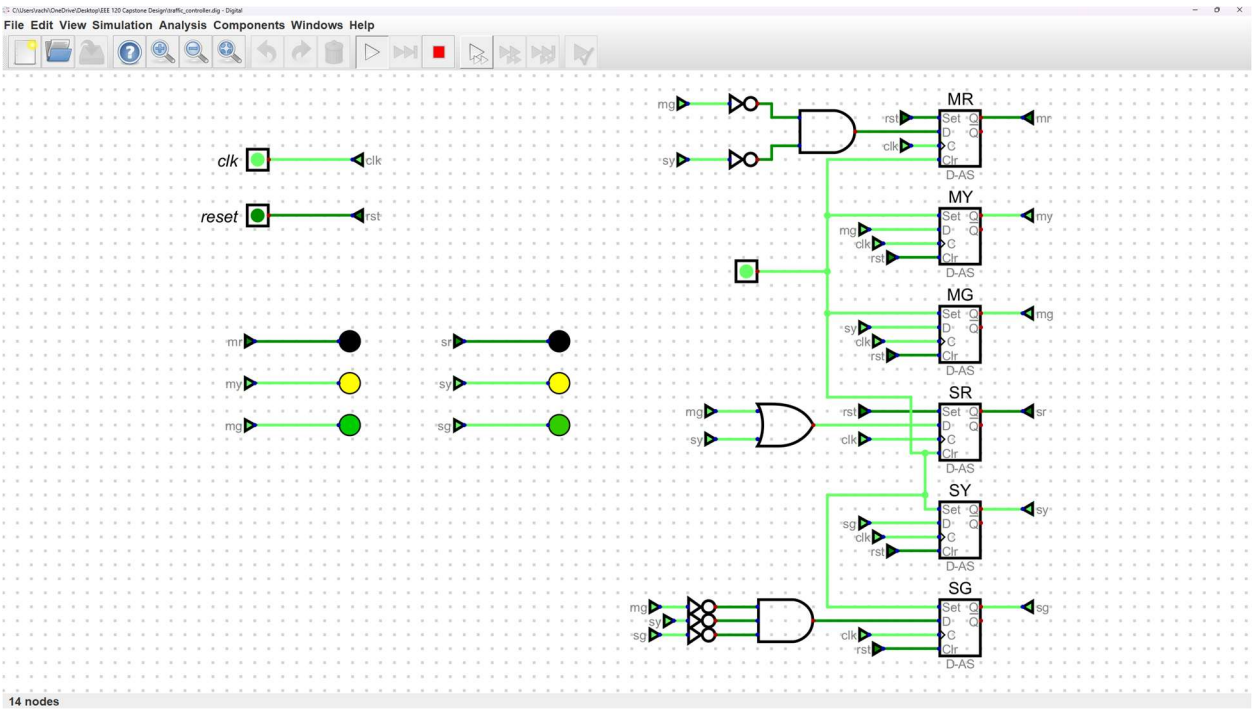

Task C-6: Record a Video Demonstration of the Winning Design

(15 pts) Record a video demonstration showing all positions being visited and various combinations of the inputs in Digital. For every clock cycle, explain the inputs, what current state you are in, and point out any outputs that should be noted. Be sure to show what happens for different input combinations at each position. That is, your demonstration should be able to showcase all possible states and transitions required to get there. If you include any asynchronous inputs, make sure to show those features as well. Add a link to your video below. Be sure to include any required password.

Video link: https://asu.zoom.us/rec/share/WCHReb4jayh9_lznqkaMvNcorp-q2X-Q0pRI55hnosR9GcBc2Vb0Qqq7eSlwhxHN.hNFkSBIMyYjcBmzo

Passcode: tRU7tU?t

Task C-7: Fill Out the Self-Assessment and Turn in Your Design

There are two items to submit. Turn in the zip file of your capstone project folder. Also turn in this template once it is filled out. There will be a deduction of 5 points if your template is only found inside the zip folder. The self-assessment is on the next page.

->Done!

SELF-ASSESSMENT WORKSHEET

Put an 'X' in the table below indicating how strongly you agree or disagree that the outcomes of the assigned tasks were achieved. Use '5' to indicate that you 'strongly agree' and '1' to indicate that you 'strongly disagree'. Use 'NA', Not Applicable, when the tasks you performed did not elicit this outcome. Credit will be given for including this worksheet with your lab report. However, your **responses will not be graded**, they are for your instructor's information only.

Table 1: Self-Assessment of Outcomes for the Capstone Design Project Lab.

After completing the assigned tasks and report I am able to:	5	4	3	2	1	NA
Initiate a design process based on a value proposition and feedback from various stakeholders.	X					
Make assumptions to complete an incomplete functional specification.		X				
Use classical design techniques (i.e., state diagrams, state transition tables, and Karnaugh Maps), to design a synchronous sequential machine starting with a functional specification.		X				
Build, and debug a synchronous sequential machine.	X					
Develop reasonable engineering criteria for comparing different designs.	X					
Apply engineering criteria to select a 'best' design.	X					

Write below any suggestions you have for improving this laboratory exercise so that the stated learning outcomes are achieved.

->This lab work needed more time for us students, that was the only thing in my opinion I have faced while doing this lab, else everything went smoothly.

CAPSTONE DESIGN PROJECT: LAB REPORT GRADE SHEET

Name: Rachit Srivastava

Grading Criteria	Max Points	Points lost
Template		
Neatness, Clarity, and Concision	5	
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task C-1: Planning the Synchronous Sequential Machines	15	
Task C-2: Document the Synchronous Sequential Machines	40	
Task C-3: Determine Criteria and Weighting for Judging Your Designs	5	
Task C-4: Apply the Criteria to Pick the Best Design	5	
Task C-5: Build and Simulate Winning Design in Digital	15	
Task C-6: Record a Video Demonstration of the Winning Design	15	
Self-Assessment Worksheet (The content of the self-assessment worksheet will not be graded. Full credit is given for including the completed worksheet.)	(2 extra points)	
Lab Score	**Points Lost**	
	Late Lab	
	Lab Score	