

EEE 120

Lab 4 Answer Sheet

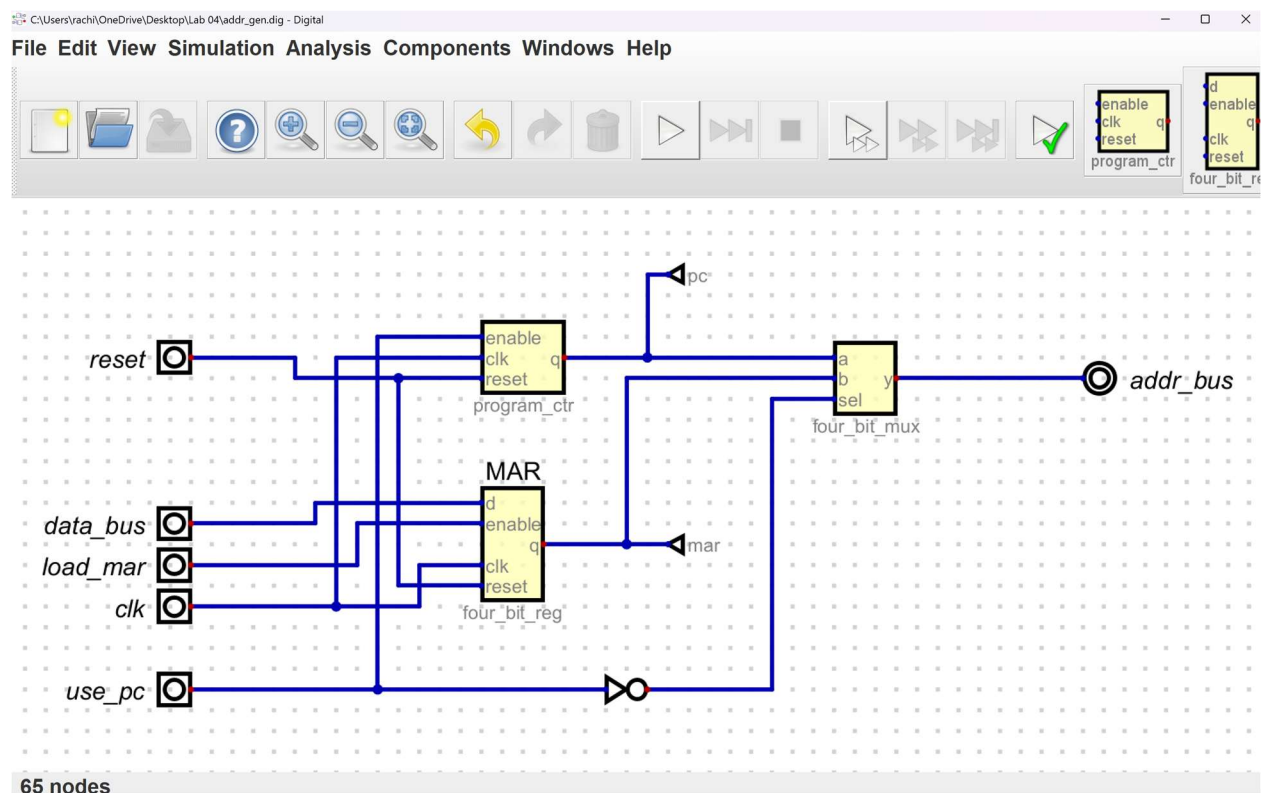
The Complete Microprocessor

Name: Rachit Srivastava **Instructor/Time:** Steven Millman (Tue,Thurs – 4:30p.m. to 5:45 p.m.)

Date: 06 April 2025

Task 4-1: Build and Test the Memory-Address-Generation Circuit

Include a picture of your Digital circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

-> When designing the circuit, no issues were faced as such.

Did the circuit behave as expected? If no, what was wrong?

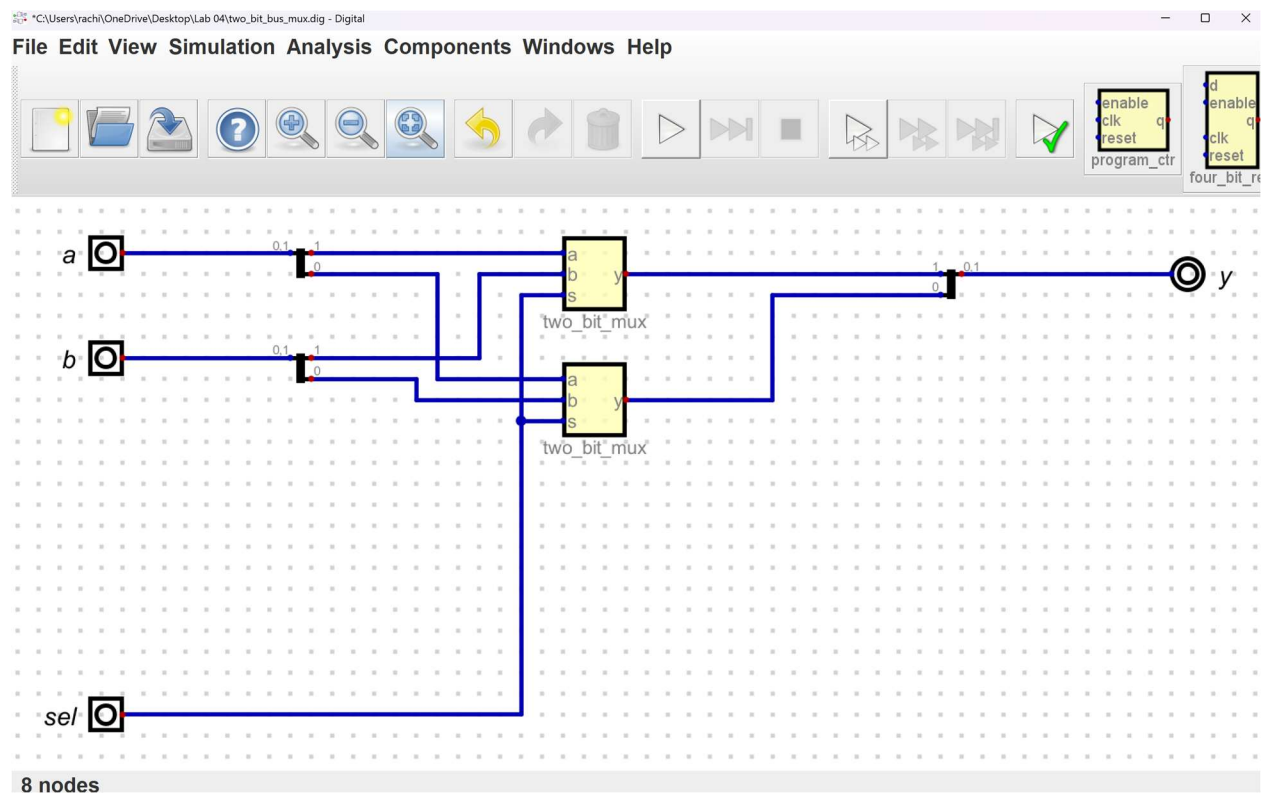
->Yes, according to the lab manual, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

->While Simulating the circuit, no issues were faced as such.

Task 4-2: Build and Test the Controller Circuit

Include a picture of your two_bit_bus_mux circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

->When designing the circuit, there were not a single issue faced as such.

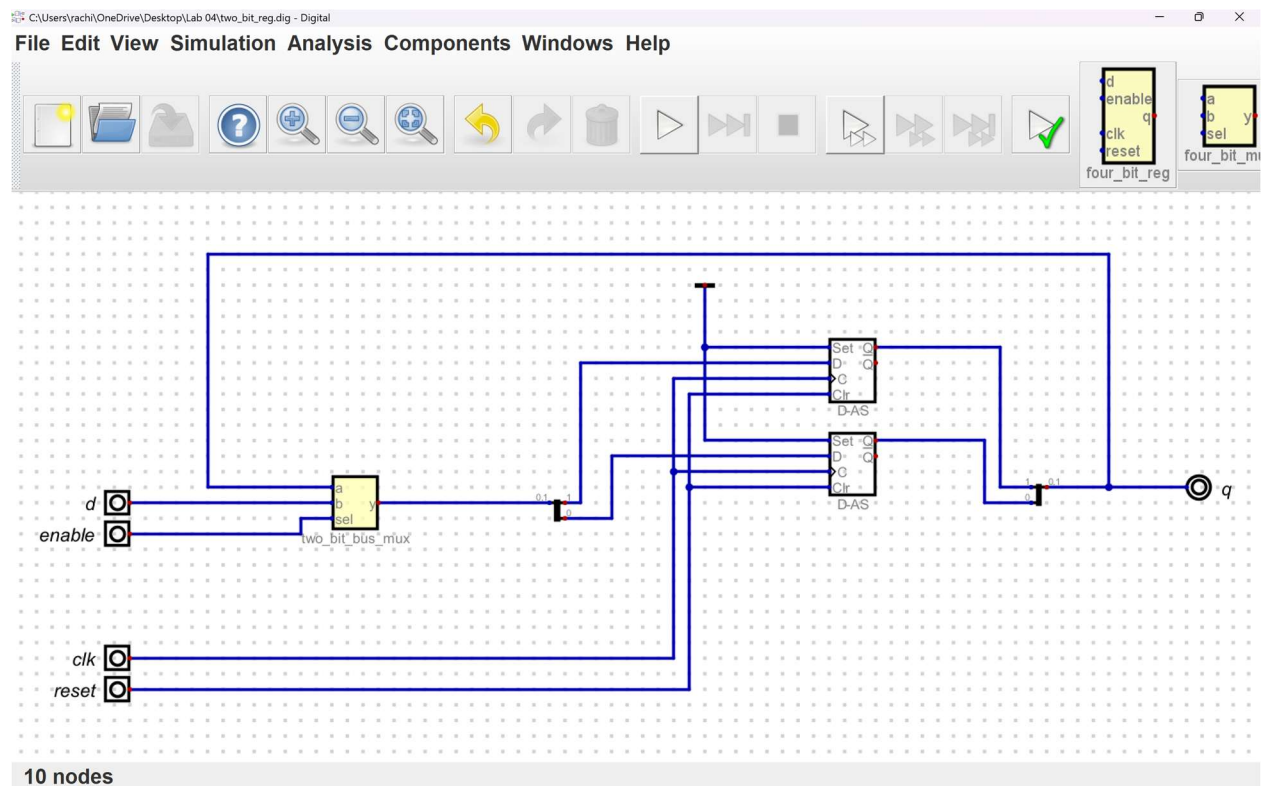
Did the circuit behave as expected? If no, what was wrong?

->Yes, the circuit behaved as expected!

Please comment on the single biggest issue you were facing when simulating the circuit.

->While simulating the circuit, all things went smoothly and not a single issue were encountered.

Include a picture of your two_bit_reg circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

->When designing the circuit, there was not a single issue faced as such. All things went smoothly. (I accidentally neglected that I have to change the two_bit_bus_mux).

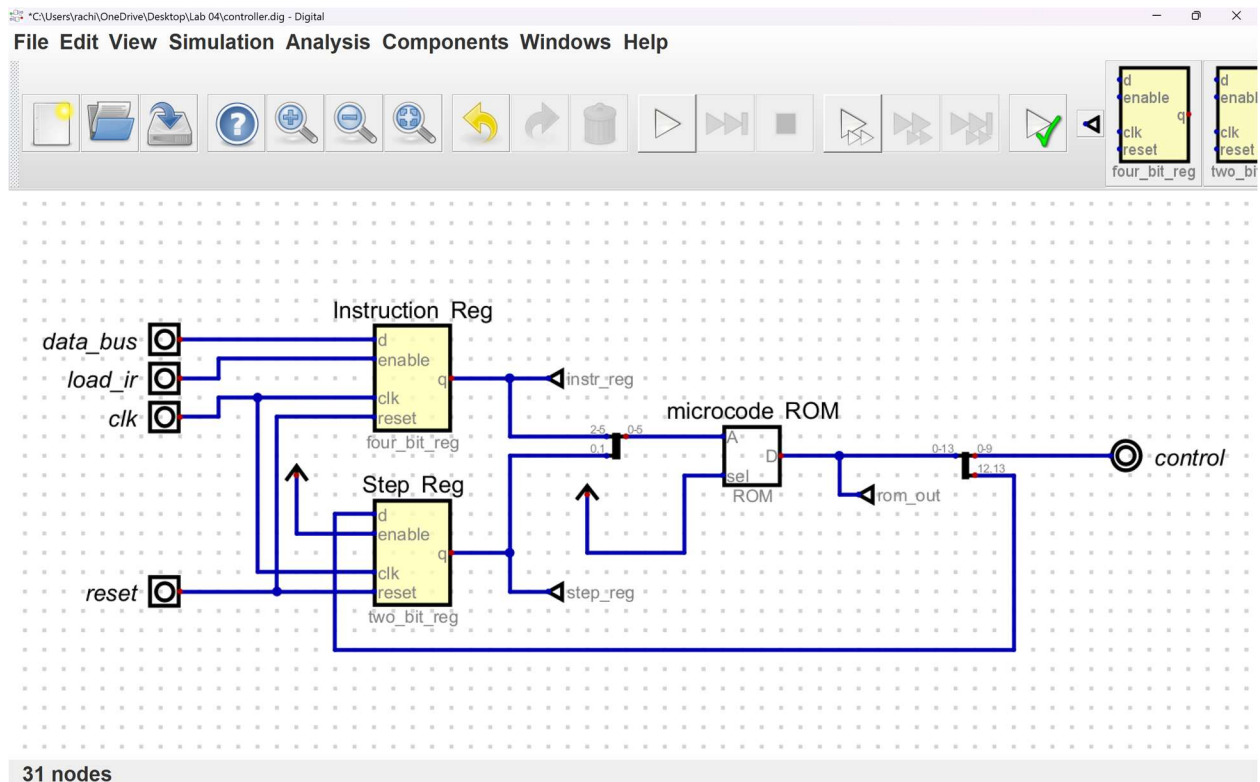
Did the circuit behave as expected? If no, what was wrong?

->Yes, the circuit behaved as expected and according to the lab manual everything went just perfect.

Please comment on the single biggest issue you were facing when simulating the circuit.

->While simulating the circuit, there was not a single issue faced, everything went smoothly.

Include a picture of your controller circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

->When designing the circuit, no issues were faced as such.

Did the circuit behave as expected? If no, what was wrong?

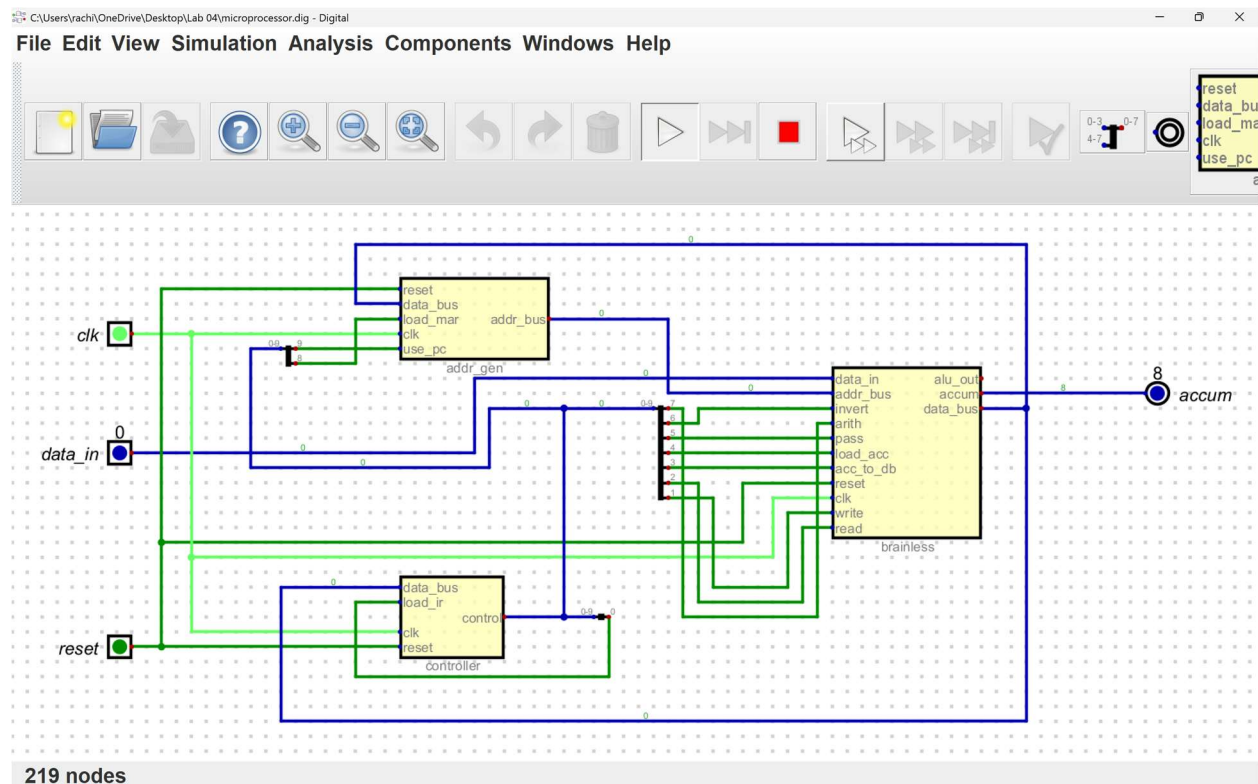
->Yes, the circuit performed smoothly and all things went perfect and matched the expectations.

Please comment on the single biggest issue you were facing when simulating the circuit.

->While simulating the circuit, there was not a single issue faced, all things went good without any issues encountered.

Task 4-3: Build the Complete Microprocessor Circuit

Include a picture of your Digital circuit here (make sure to show final values as shown in figure 17):



Please comment on the single biggest issue you were facing when designing the circuit.

->When designing the circuit, there were no major issues faced, just a few silly mistakes I made when setting bit size and naming, and eventually everything went perfect.

Did the circuit behave as expected? If no, what was wrong?

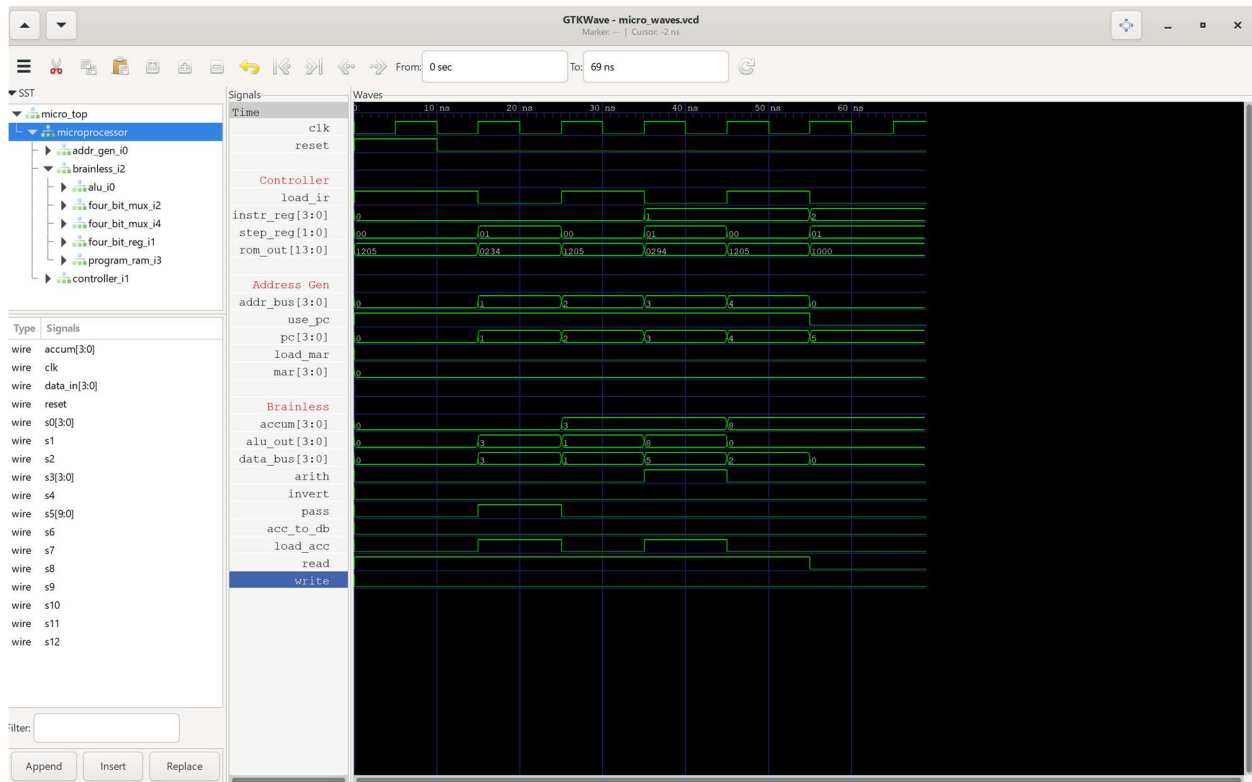
->Yes, according to the lab manual also, the circuit I have attached here behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

->While simulating the circuit, no major issues were encountered.

Task 4-4: Simulate the Design in Verilog

Include a picture of your waveforms here:



Please comment on the single biggest issue you were facing when simulating the processor.

->When simulating the processor, everything went perfectly, no issues were encountered.

Did the circuit behave as expected? If no, what was wrong?

->Yes, the circuit behaved as expected, and as per the lab manual it behaved as it is.

Please comment on the single biggest issue you were facing when simulating the circuit.

->While simulating the circuit, everything went smoothly and no issues were faced as such.

Task 4-5: Add the AND, ZERO, SUB, and STORE ACC Instructions

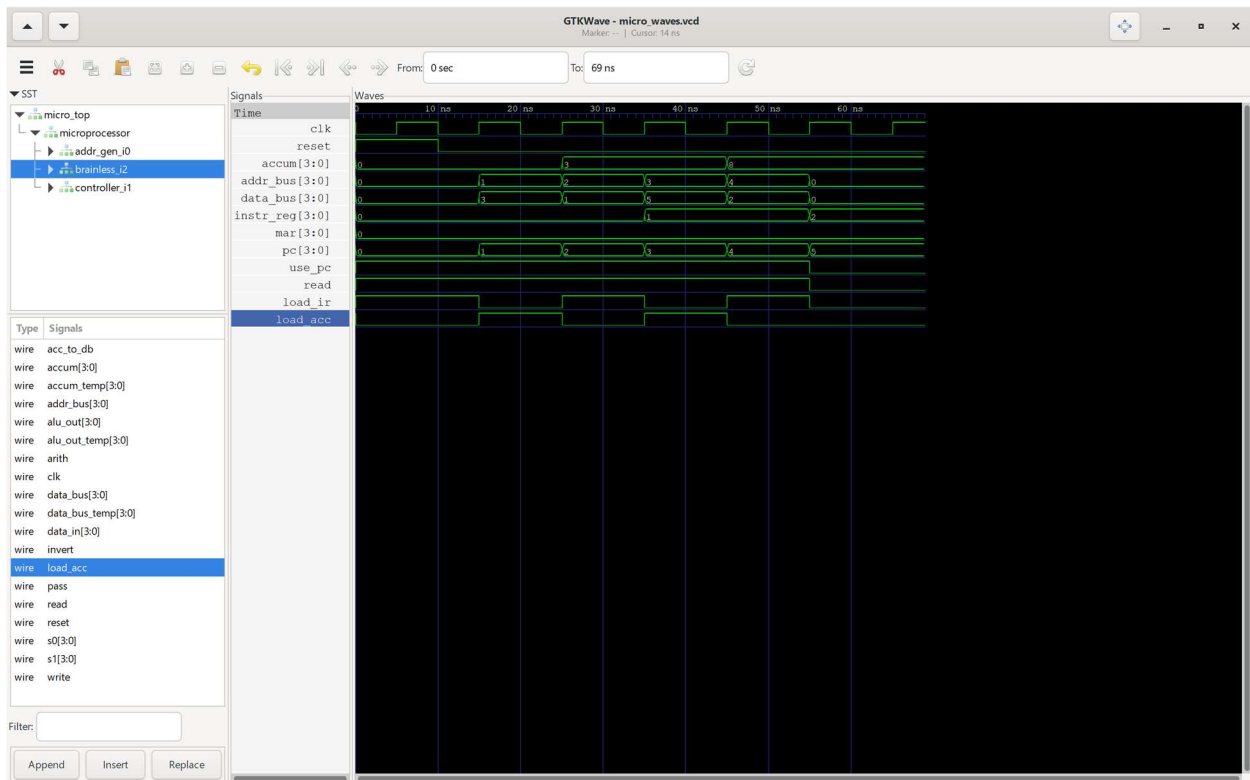
Paste the contents of your final rom_vals here:

```
rom_vals.hex
File Edit View

v2.0 raw
1205 # LOAD ACC; Load IR
0234 # Load ACC
0000 # unused
0000 # unused
1205 # ADD ACC; Load IR
0294 # ADD
0000 # unused
0000 # unused
1205 # STOP; Load IR
1000 # stay here
0000 # unused
0000 # unused
1205 # AND; Load IR
0214
0000
0000
1205 # ZERO; Load IR
00D8
0000
0000
1205 # SUB; Load IR
02D4
0000
0000
1205 # STORE ACC; Load IR
2304
000A
0000
1205 # Extra Credit; Load IR
055E
0000
3FFF
```

Test your instructions by writing and executing programs. Paste the contents of your ram_vals.txt file for each program. Note which instruction or instructions each program tests.

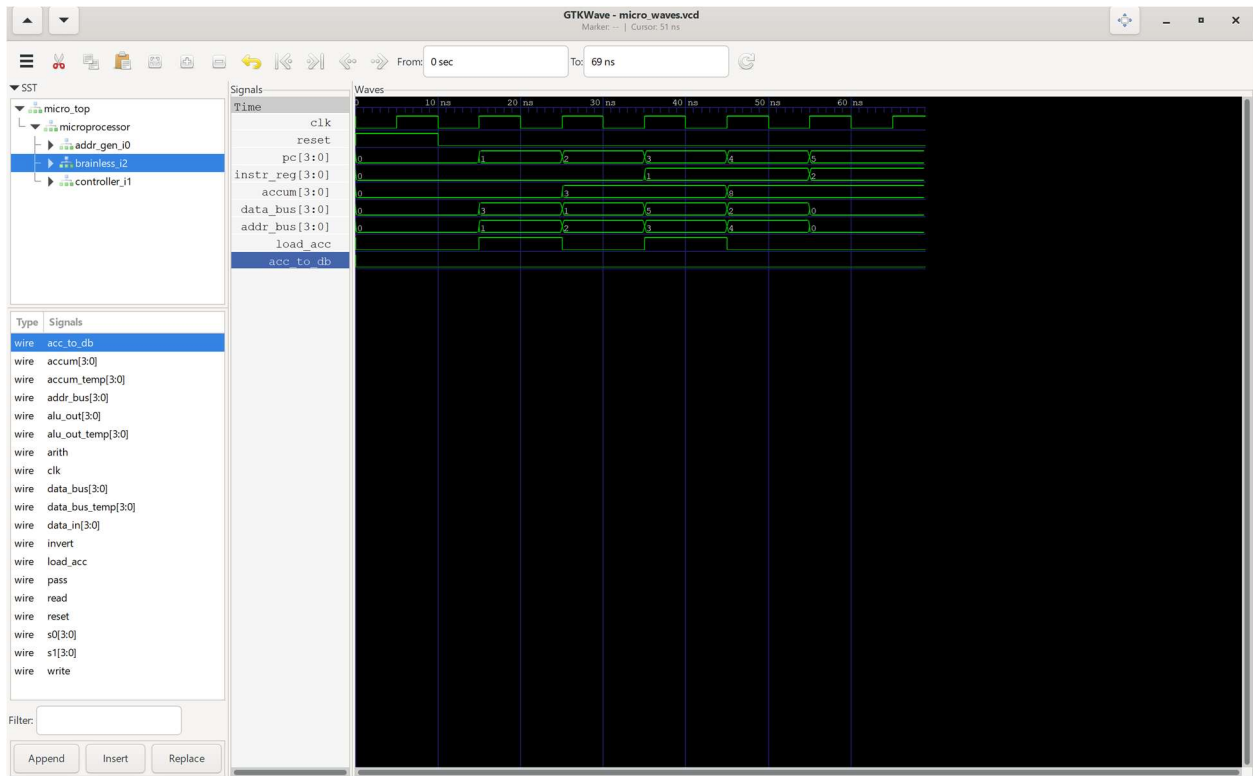
Include a picture of your AND waveforms here:



F # Value to load (ACC becomes F)

3 # AND instruction (bitwise AND ACC with next value)

Include a picture of your ZERO waveforms here:



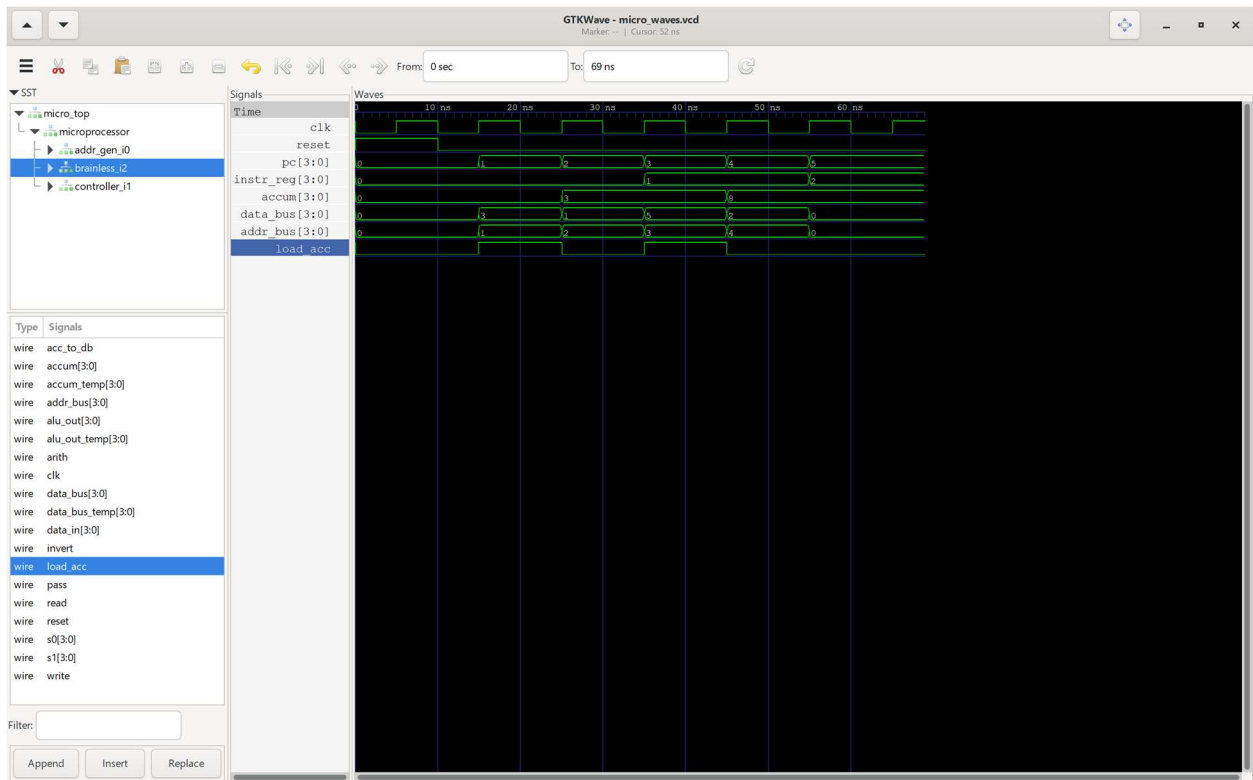
7 # Value to load (ACC becomes 7)

4 # ZERO instruction (clear ACC to 0)

0

0 # LOAD ACC

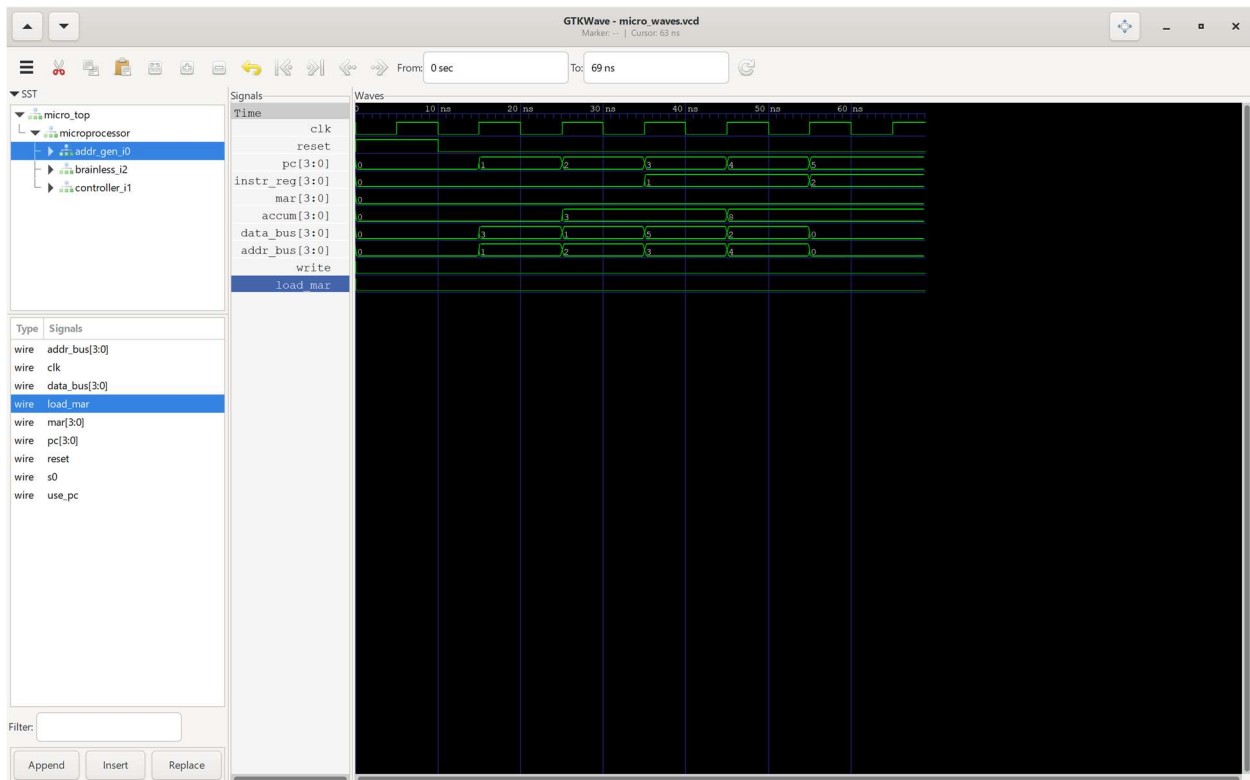
Include a picture of your SUB waveforms here:



5 # SUB instruction (subtract the next value from ACC)

1 # Operand for SUB (result becomes (F & 3) minus 1)

Include a picture of your STORE ACC waveforms here:



6 # STORE ACC (store ACC into a memory location)

E # Memory address to store into (for example, address E)

2 # STOP instruction

Did the circuit behave as expected? If no, what was wrong?

->Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

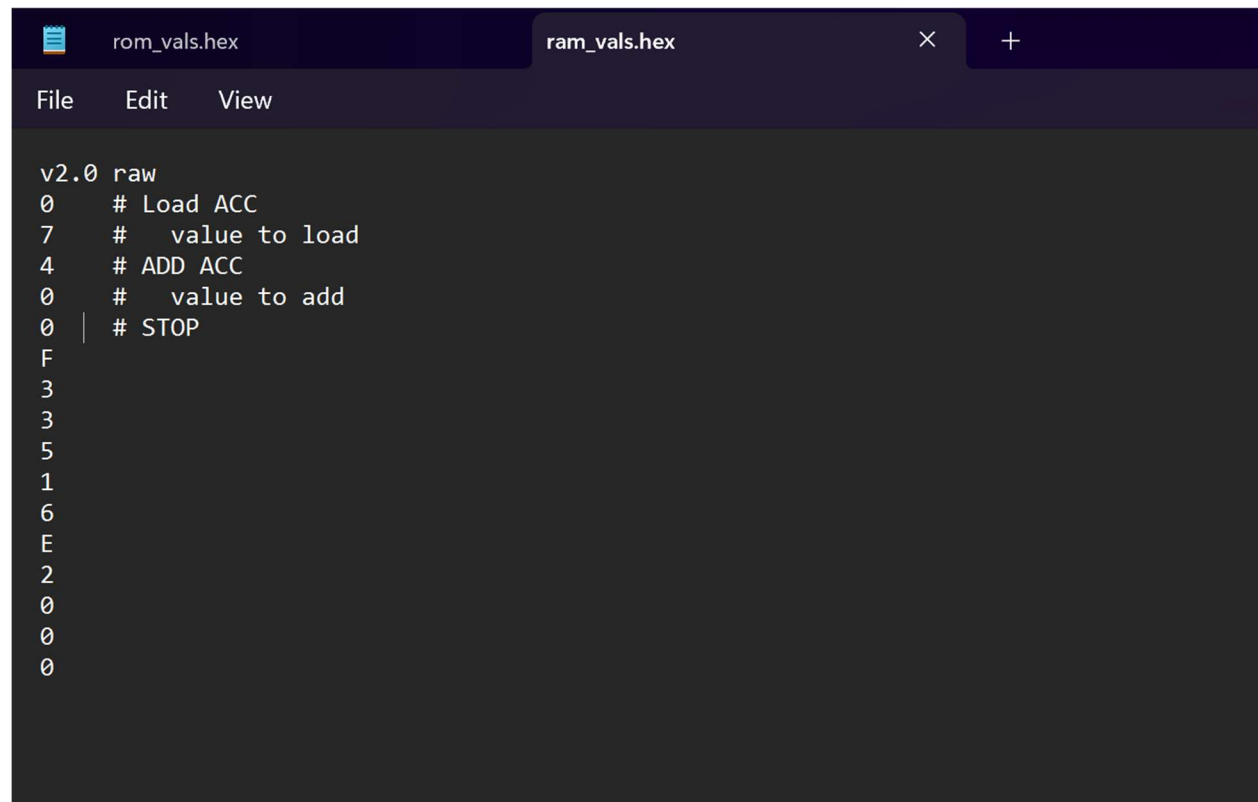
->While simulating the circuit, there was not a single issue that was encountered.

Task 4-6: Invent Your Own Instruction (Extra Credit)

Place the contents of the rom_vals for the extra credit instruction here:

```
1205 # Extra Credit; Load IR
055E
0000
3FFF
```

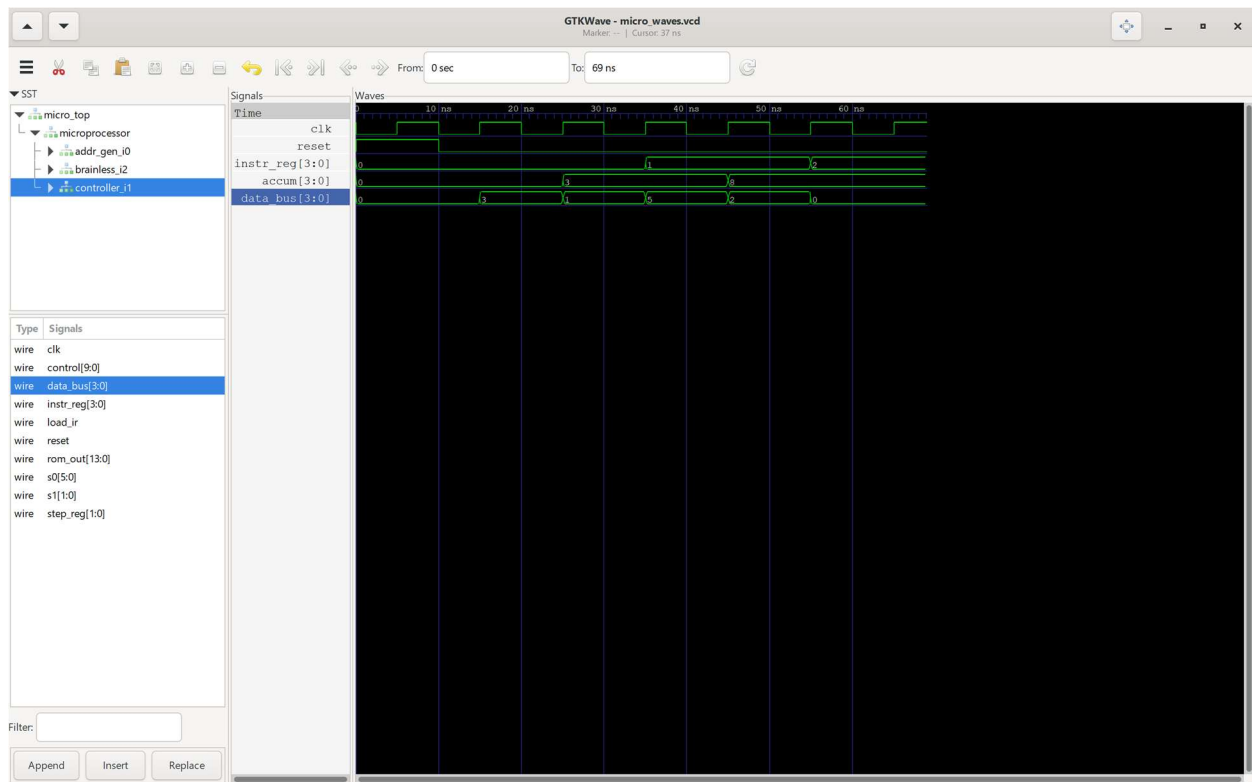
Include your Verilog ram_vals.text program used to test the extra credit instruction here:



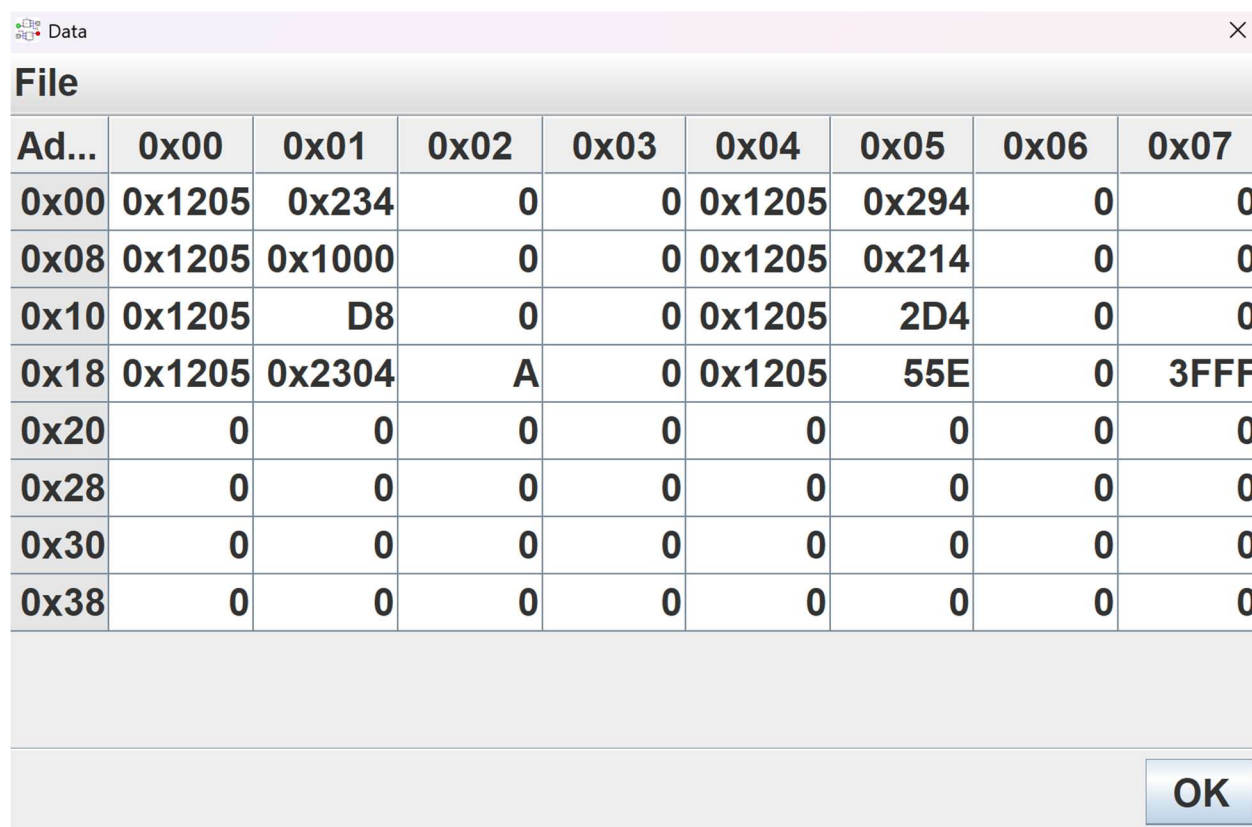
The screenshot shows a Verilog editor with two tabs: 'rom_vals.hex' and 'ram_vals.hex'. The 'ram_vals.hex' tab is active, displaying a Verilog program. The program starts with a 'v2.0 raw' header, followed by comments for 'Load ACC', 'value to load', 'ADD ACC', 'value to add', and 'STOP'. The data values are listed in a column on the left: F, 3, 3, 5, 1, 6, E, 2, 0, 0, 0.

```
v2.0 raw
0 # Load ACC
7 # value to load
4 # ADD ACC
0 # value to add
0 # STOP
F
3
3
5
1
6
E
2
0
0
0
```

Include a picture of your waveforms here:



Include a picture of your ROM contents here:



Ad...	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
0x00	0x1205	0x234	0	0	0x1205	0x294	0	0
0x08	0x1205	0x1000	0	0	0x1205	0x214	0	0
0x10	0x1205	D8	0	0	0x1205	2D4	0	0
0x18	0x1205	0x2304	A	0	0x1205	55E	0	3FFF
0x20	0	0	0	0	0	0	0	0
0x28	0	0	0	0	0	0	0	0
0x30	0	0	0	0	0	0	0	0
0x38	0	0	0	0	0	0	0	0

OK

Task 4-7: Create a video and submit your report

Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

Video Link: https://asu.zoom.us/rec/share/aOgl8s3RfWXibvWCL1kz8F-iKfzqSfB_F7v10wu0joPuTGsgKr3RhGYSeDq9kc2.YG0jZP5vB7z-GJJT?startTime=1744342868000

Passcode: B7Wj!^s2

At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab4 directory. Create a zip file of the Lab4 directory. Remember to turn in the zip file and your completed template on Canvas!

Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!

LAB 4: LAB REPORT GRADE SHEET

Name: Rachit Srivastava

NOTE: You submit the zip file in order to show your work.

If the zip file is not submitted you will receive a 0 for this lab!

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 4-1: Build and Test the Memory-Address-Generation Circuit	10	
Task 4-2: Build and Test the Controller Circuit	10	
Task 4-3: Build the Complete Microprocessor Circuit	10	
Task 4-4: Write and Execute a Simple Program for Your Microprocessor in Simulation	10	
Task 4-5: Add the 'AND', 'Zero', 'Subtract', and 'Store ACC' Instructions	30	
Task 4-6: Invent Your Own Instruction (Extra Credit)	10	
Task 4-7: Record your video	10	
Lab Score (80 points total)	Points Lost	
	Late Lab	
	Lab Score	