

Lab 3 Answer Sheet

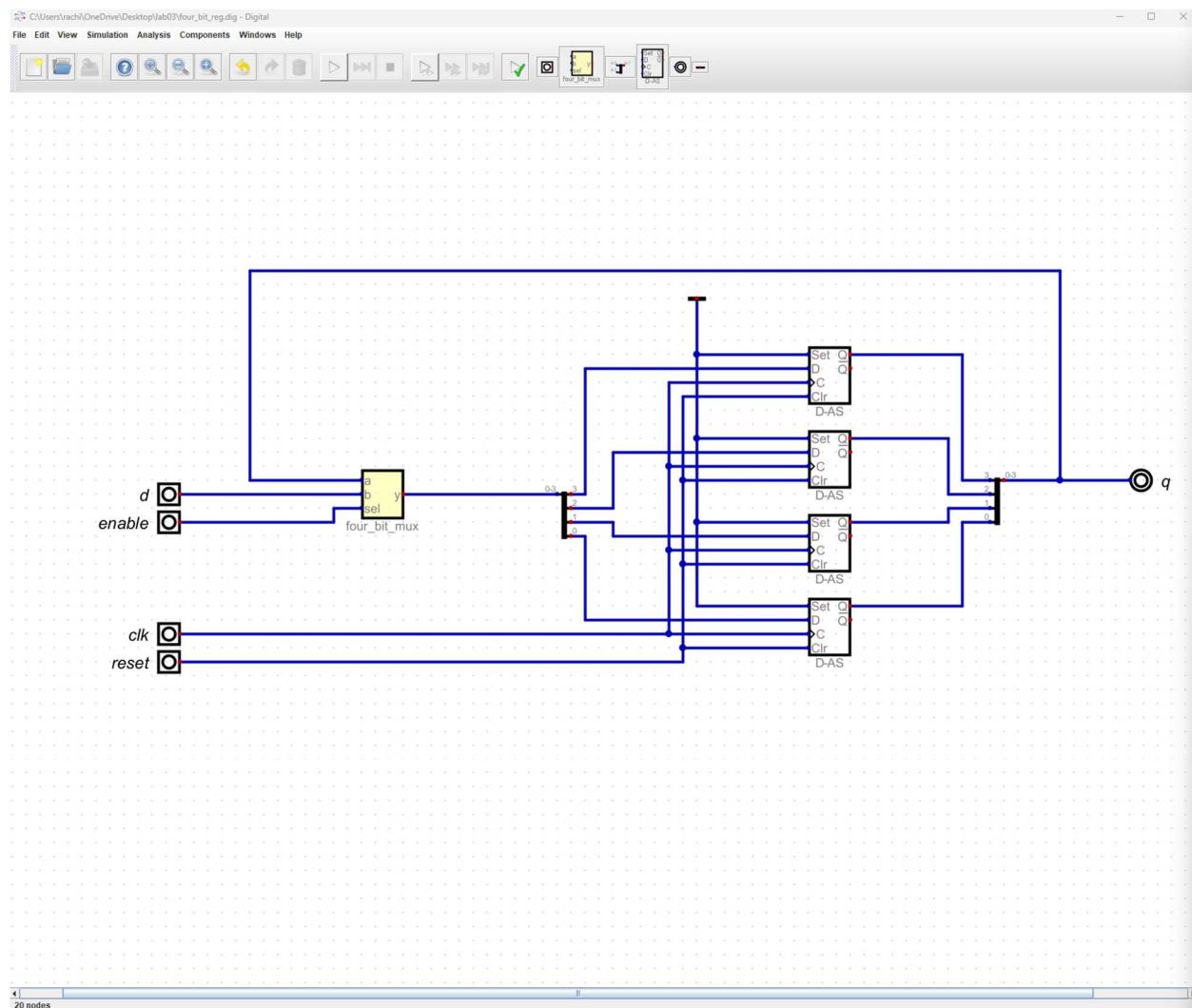
Registers, Counters and the “Brainless CPU”

Name: Rachit Srivastava **Instructor/Time:** Steven Millman (Tue,Thurs – 4:30 p.m – 5:45 p.m)

Date: 20 March, 2025

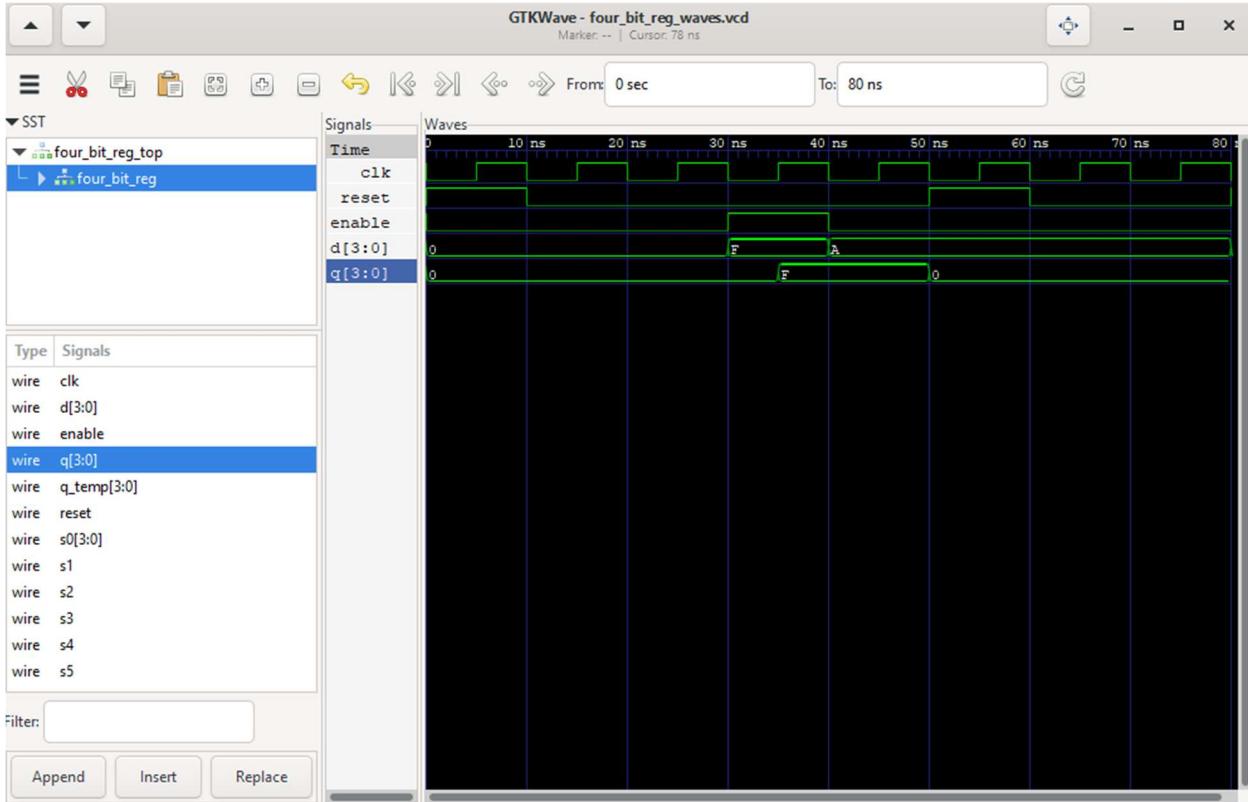
Task 3-1: Build and Test a 4-Bit D Register with Enable

Include a picture of your Digital circuit here:



Please comment on the single biggest issue you were facing when designing the circuit. No issues faced as such.

Include a picture of your GTKWave waveforms (timing diagram) here:

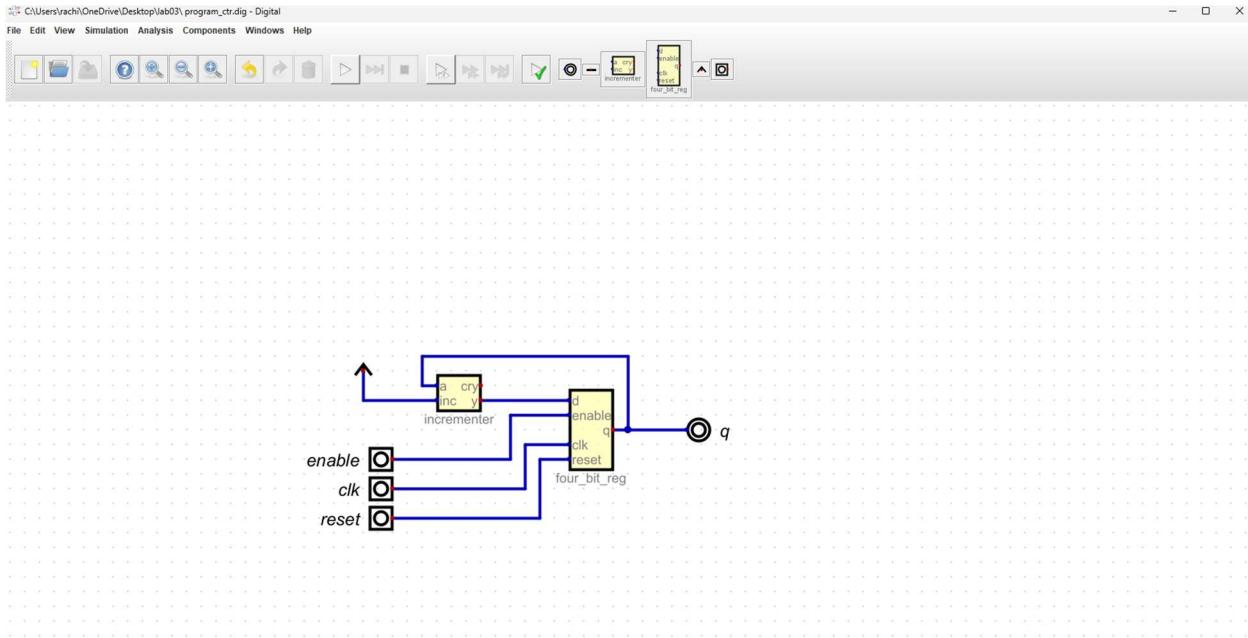


Did the circuit behave as expected? If no, what was wrong? Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. No issues faced as such.

Task 3-2: Build and Test a 4-Bit UP Counter

Include a picture of your Digital circuit here:



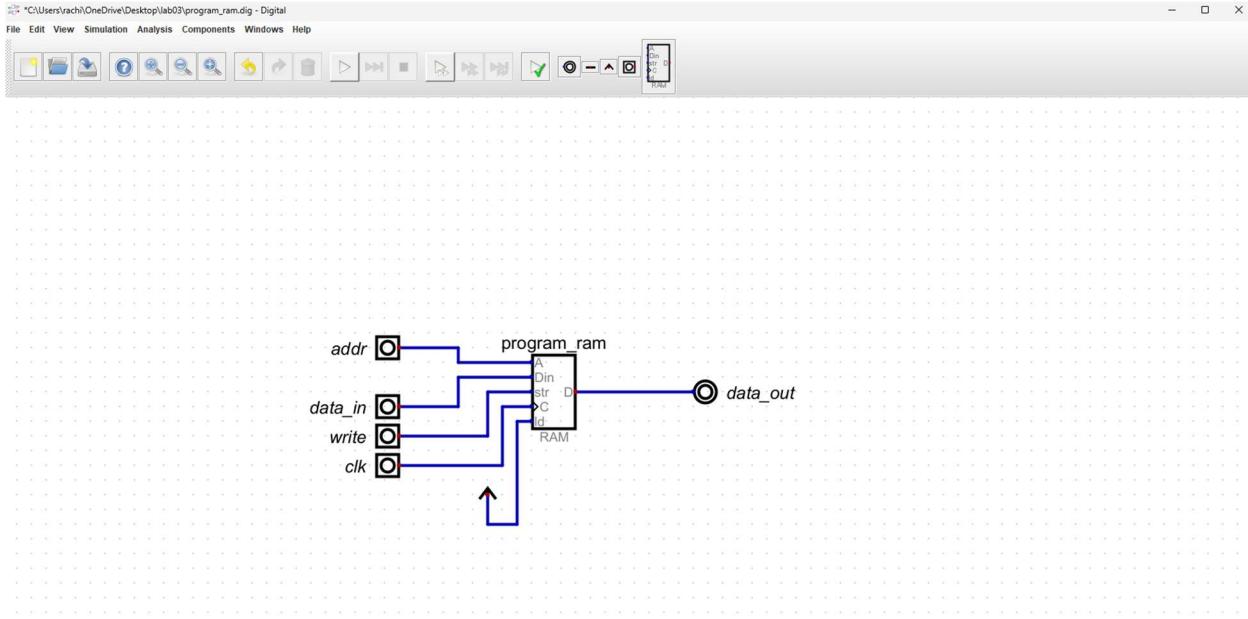
Please comment on the single biggest issue you were facing when designing the circuit. No issues faced as such.

Did the circuit behave as expected? If no, what was wrong? The circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. No issues faced as such.

Task 3-3: Create a 4-Bit RAM with 16 4-Bit Words

Include a picture of your Digital circuit here:



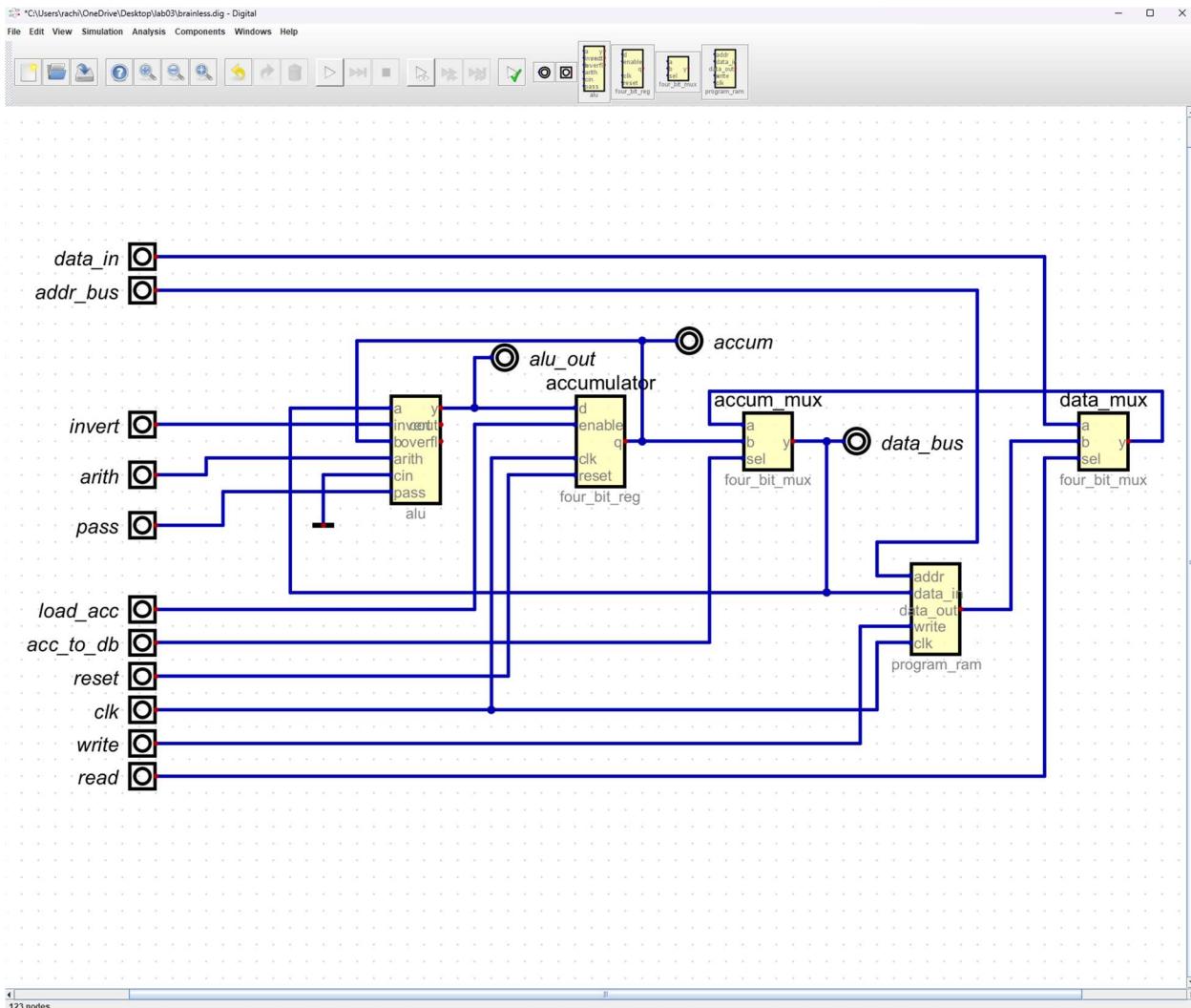
Please comment on the single biggest issue you were facing when designing the circuit. No issues faced as such.

Did the circuit behave as expected? If no, what was wrong? Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. When while simulating the circuit, no issues were faced as such.

Task 3-4: Build and Test the Brainless Central Processing Unit

Include a picture of your Digital circuit here:



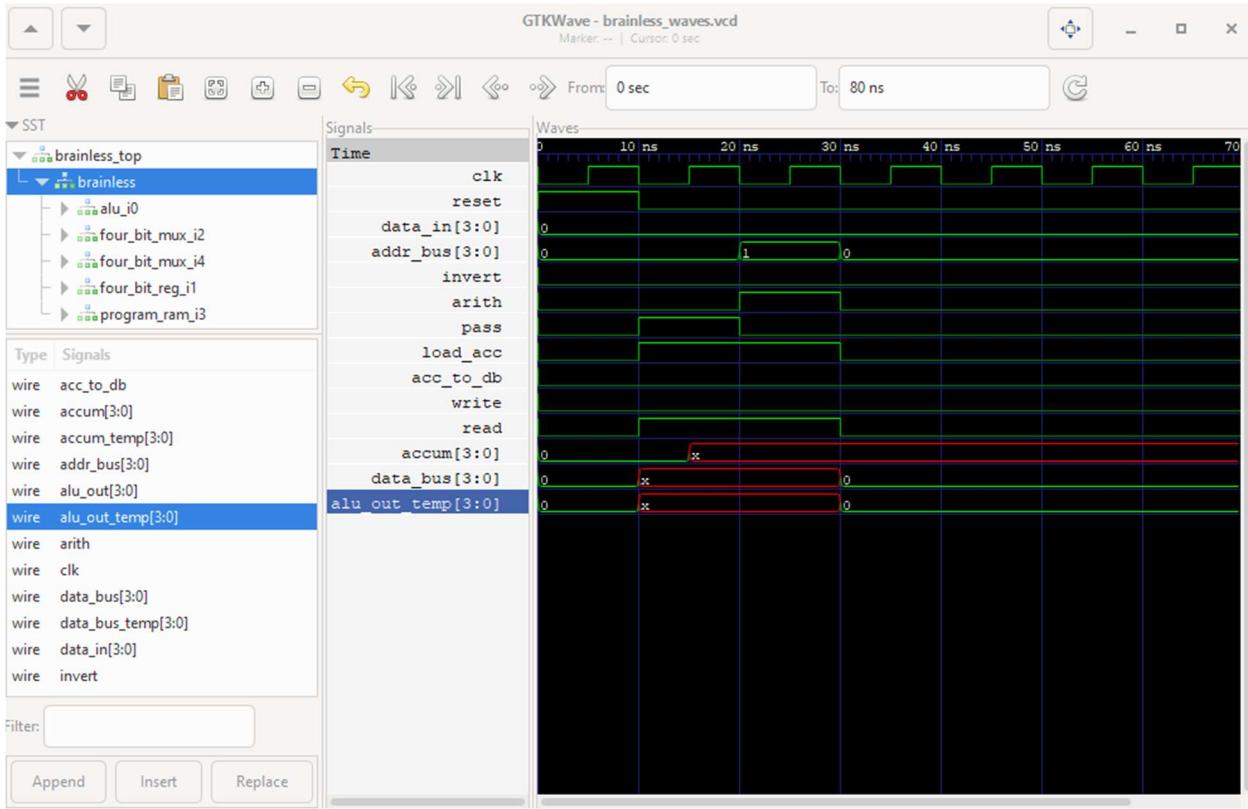
Please comment on the single biggest issue you were facing when designing the circuit. No issues faced as such.

Did the circuit behave as expected? If no, what was wrong? Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. When while simulating the circuit, no issues were faced as such.

Task 3-5: Simulate the Brainless Central Processing Unit

Include a picture of your GTKWave waveforms (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong? Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. While simulating the circuit I was quite unsure about the red waves in the output.

Task 3-6: Create Additional Tests

As shown in the manual, paste the test_vals you used for each of the tests here. Be sure to note which each set of test_vals goes with each test.

The screenshot shows a code editor window with a dark theme. The title bar has three tabs: "brainless_ext_wr" (active), "brainless_int_write.v", and "brainless_alu.v". The menu bar includes "File", "Edit", "View", and various icons for file operations and settings. The main code area contains Verilog testbench code:

```
begin
    #1 if ( num_tests > 8 )
        begin
            $display("Too many tests - the limit is 8!");
            $finish;
        end
    end

    assign values = test_vals[addr];

    // The bits of the test_vals memory are:
    // 27:23 - accum      The expected accumulator output
    // 23:20 - data_bus   The expected data_bus value
    // 19:16 - alu_out    The expected alu output
    // 15:12 - data_in    The data_in input
    // 11: 8 - addr_bus   The address bus input
    //   7   - invert      An ALU control input
    //   6   - arith       An ALU control input
    //   5   - pass        An ALU control input
    //   4   - load_acc    Load the accumulator
    //   3   - acc_to_db   Select the accumulator value
    //   2   - reset       Reset the circuit
    //   1   - write       Write a value into the RAM
    //   0   - read        Select the program_ram value

    // IMPORTANT: ONLY MODIFY BELOW THIS LINE *****
    assign num_tests = 8;                      // how many tests you want to run

    // Each assignment to test_vals[#] is one test.
    // NOTE: The maximum number of tests is 8, and they are numbered 0-7.
    // NOTE: The tests MUST be numbered consecutively starting with 0.
    // NOTE: At least the first test should be reset!
    // For the bit assignments, see the comment 14 lines above this line

initial
begin
    test_vals[0] = 28'h0_0_0_0_0_0_4; // Reset (keep this first)
    test_vals[1] = 28'h1_0_0_0_AA_5_0; // Write 0xAA to RAM address 5
    test_vals[2] = 28'h8_0_0_0_0_0_0; // Do nothing (fill remaining slots)
    test_vals[3] = 28'h8_0_0_0_0_0_0;
    test_vals[4] = 28'h8_0_0_0_0_0_0;
end

endmodule
```

The status bar at the bottom shows: Ln 55, Col 34 | 2,025 characters | 100% | Unix (LF) | UTF-8

The screenshot shows a terminal window with three tabs at the top: "brainless_ext_write.v", "brainless_int_wri", and "brainless_alu.v". The "brainless_int_wri" tab is active, displaying the following Verilog code:

```
#1 if ( num_tests > 8 )
begin
    $display("Too many tests - the limit is 8!");
    $finish;
end
end

assign values = test_vals[addr];

// The bits of the test_vals memory are:
// 27:23 - accum      The expected accumulator output
// 23:20 - data_bus   The expected data_bus value
// 19:16 - alu_out    The expected alu output
// 15:12 - data_in    The data_in input
// 11: 8 - addr_bus   The address bus input
//   7  - invert      An ALU control input
//   6  - arith       An ALU control input
//   5  - pass        An ALU control input
//   4  - load_acc    Load the accumulator
//   3  - acc_to_db   Select the accumulator value
//   2  - reset       Reset the circuit
//   1  - write       Write a value into the RAM
//   0  - read        Select the program_ram value

// IMPORTANT: ONLY MODIFY BELOW THIS LINE *****

assign num_tests = 8;                      // how many tests you want to run

// Each assignment to test_vals[#] is one test.
// NOTE: The maximum number of tests is 8, and they are numbered 0-7.
// NOTE: The tests MUST be numbered consecutively starting with 0.
// NOTE: At least the first test should be reset!
// For the bit assignments, see the comment 14 lines above this line

initial
begin
    test_vals[0] = 28'h0_0_0_0_0_0_4; // Reset
    test_vals[1] = 28'h3_0_0_0_1_55; // Load 0x55 into accumulator (from RAM
    address 1)
    test_vals[2] = 28'h2_1_0_0_0_6_55; // Store accumulator to RAM address 6
    test_vals[3] = 28'h8_0_0_0_0_0_0; // Do nothing
    test_vals[4] = 28'h8_0_0_0_0_0_0;
end

endmodule
```

The status bar at the bottom shows: Ln 55, Col 34 | 2,043 characters | 100% | Unix (LF) | UTF-8

```
brainless_ext_write.v | brainless_int_write.v | brainless_alu.v X + - □ ×
File Edit View
end
end

assign values = test_vals[addr];

// The bits of the test_vals memory are:
// 27:23 - accum      The expectedd accumulator output
// 23:20 - data_bus   The expected data_bus value
// 19:16 - alu_out    The expected alu output
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//   7   - invert      An ALU control input
//   6   - arith       An ALU control input
//   5   - pass        An ALU control input
//   4   - load_acc    Load the accumulator
//   3   - acc_to_db   Select the accumulator value
//   2   - reset       Reset the circuit
//   1   - write       Write a value into the RAM
//   0   - read        Select the program_ram value

// IMPORTANT: ONLY MODIFY BELOW THIS LINE *****

assign num_tests = 8;                                // how many tests you want to run

// Each assignment to test_vals[#] is one test.
// NOTE: The maximum number of tests is 8, and they are numbered 0-7.
// NOTE: The tests MUST be numbered consecutively starting with 0.
// NOTE: At least the first test should be reset!
// For the bit assignments, see the comment 14 lines above this line

initial
begin
    test_vals[0] = 28'h0_0_0_0_0_0_4;      // reset - this should always be the
first vector
    test_vals[0] = 28'h0_0_0_0_0_0_4; // Reset
test_vals[1] = 28'h3_0_0_0_0_2_F; // Load 0x0F (15) into accumulator (from RAM
address 2)
test_vals[2] = 28'h4_0_0_2_5_0_A; // Subtract 5 (result: 15-5=10)
test_vals[3] = 28'h3_0_0_0_0_3_3; // Load 0x03 (3) into accumulator (from RAM
address 3)
test_vals[4] = 28'h4_0_0_3_F_0_3; // AND with 0x0F (15) (result: 3 & 15 = 3)
test_vals[5] = 28'h8_0_0_0_0_0_0; // Do nothing
end

endmodule
```

If you changed your circuit since you took the screenshot for Task 3-4, take another and replace the screenshot in Task 3-4.

Include a picture of your GTKWave waveforms here (one per required test):

Please comment on the single biggest issue you were facing when designing the circuit. No issues faced as such.

Did the circuit behave as expected? If no, what was wrong? Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit. When while simulating the circuit, no issues were faced as such.

Task 3-7: Create a video and submit your report

Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

Video Link:

At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab3 directory. Create a zip file of the Lab3 directory. Remember to turn in the zip file and your completed template on Canvas!

Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!

LAB 3: LAB REPORT GRADE SHEET

Name Rachit Srivastava

NOTE: You submit the zip file in order to show your work.

If the zip file is not submitted you will receive a 0 for this lab!

Instructor Assessment

Grading Criteria	Max Points	Points Lost
<u>Description of Assigned Tasks, Work Performed & Outcomes Met</u>		
Task 3-1: Build and Test a 4-Bit D Register with Enable	10	
Task 3-2: Build and Test a 4-Bit UP Counter	10	
Task 3-4: Build and Test the Brainless Central Processing Unit	10	
Task 3-5: Simulate the Brainless Central Processing Unit	10	
Task 3-6: Create Additional Tests	10	
Task 3-7: Create a video and submit your report	10	
Lab Score (60 points total)	Points Lost	
	Late Lab	
	Lab Score	