**Week 8 Task – Post-Layout STA & Timing Graphs Across PVT Corners for Routed VSDBabySoC**

**Objective**

To perform **Post-Layout Static Timing Analysis (STA)** using the **SPEF** generated after routing in Week 7, analyze timing across all **PVT corners**, and compare post-route results with post-synthesis timing data from Week 3.

**Why This Task Is Important**

This final step closes the full ASIC flow.
You have now moved from RTL → Synthesis → Physical Design → Parasitic Extraction.
Now, by performing **post-layout STA**, you will see:

- How **routing parasitics (SPEF)** change the path delays compared to the ideal netlist.
- The **impact of PVT (Process, Voltage, Temperature)** variations on timing.
- How design optimization improves or worsens timing after layout.

Understanding these timing differences is **critical for tape-out readiness** — this is how real silicon accuracy is verified before fabrication.

**Reference Material**

- **Timing Graphs Reference:**
  📎 Day 26 – Timing Graphs Example
- **Script for Post-Route STA with SPEF Annotation:**
  📎 OpenSTA TCL Script – PVT Analysis

**Task Components**

**1. Load Post-Route Design into OpenSTA**

- Import:
  - Gate-level netlist
  - Library files for all PVT corners

    - Extracted SPEF file
    - Timing constraints (SDC)
- Use the provided TCL script to run STA across multiple corners (TT, SS, FF, etc.).

**2. Generate Post-Route Timing Reports and Graphs**

- Use report_checks with appropriate switches (-path_delay, -fields, -nosplit, etc.) to display SPEF annotation.
- Generate and plot timing graphs for each corner (similar to the examples in Day 26 repo).
- Capture key metrics for each corner:
    - Worst Negative Slack (WNS)
    - Total Negative Slack (TNS)
    - Worst Hold Slack (WHS)
    - Total Hold Slack (THS)

**3. Compare with Post-Synthesis Results (Week 3)**

- Retrieve Week 3 timing reports and graphs.
- Create a comparison table showing Week 3 vs Week 8 values for each corner:

| Corner | WNS (Week 3) | WNS (Week 8) | TNS (Week 3) | TNS (Week 8) | WHS (Week 3) | WHS (Week 8) | THS (Week 3) | THS (Week 8) |
|---|---|---|---|---|---|---|---|---|

- Highlight the improvements or regressions after routing (e.g., better setup slack but worse hold due to added RC effects).

**4. Interpret Results**

- Discuss why post-route timing differs from pre-route timing.
- Explain how SPEF annotation affects path delays.
- Comment on how physical effects (capacitance, resistance, coupling) impact timing closure.

**Deliverables**

1. **Timing Reports and Graphs**
    - Screenshots or PDFs of OpenSTA timing graphs for each corner.
    - Text files of report_checks outputs with visible SPEF annotation.
2. **Comparison Table**
    - Week 3 vs Week 8 timing summary (wns, tns, whs, ths).
3. **Documentation on GitHub**
    - Step-by-step procedure and commands used.
    - Plots comparing pre- and post-layout graphs.
    - Short write-up on key observations and learning outcomes.

✅ **By the end of Week 8**, you will:

- Perform **Post-Layout STA with SPEF annotation** across PVT corners.
- Visualize how parasitic effects alter timing characteristics.
- Gain a complete end-to-end understanding of **the SoC physical design and timing closure process** — the final step before tape-out.