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B.Tech DEGREE EXAMINATION, DECEMBER 2023

Fourth and Fifth Semester

18ECC202J - LINEAR INTEGRATED CIRCUITS

(For the candidates admitted during the academic year 2018-19 to 2021-22)

OPEN BOOK EXAMINATION

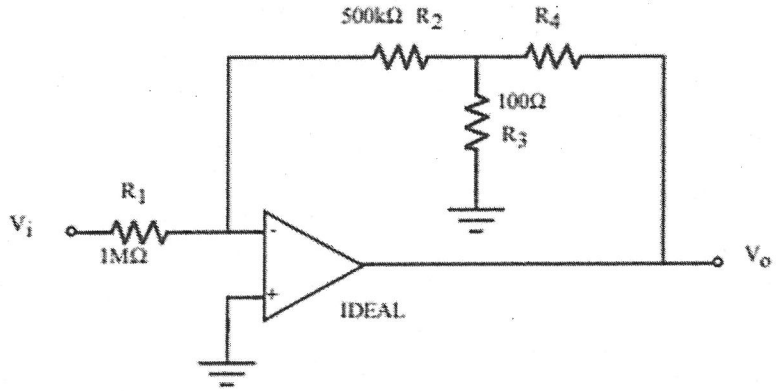
Note:

i. Specific approved THREE text books (Printed or photocopy) recommended for the course.
ii. Handwritten class notes (certified by the faculty handling the course / Head of the Department).

Time: 3 Hours **Max. Marks: 100**

Answer **FIVE** Questions (Question No. 1 is compulsory)

			Marks	BL	CO
1	i.	a. The input offset current compensated inverting amplifier shown in below figure. Determine the value of resistor R_4 in the feedback network of an amplifier to provide the voltage gain of -120 [9 Marks]	18	4	1



b. Explain the function of the circuit shown in Figure 1 and derive the output expression. Also, find the value of (i) input resistance (ii) voltage gain (iii) output voltage, where $R_1=R_3=560\Omega$, $R_f=R_2=5.6k\Omega$, $V_1=2V$ (peak to peak), $V_2=1V$ (peak to peak), Ri=2M Ω and open loop gain $A_{OL}=200000$. [9 Marks]

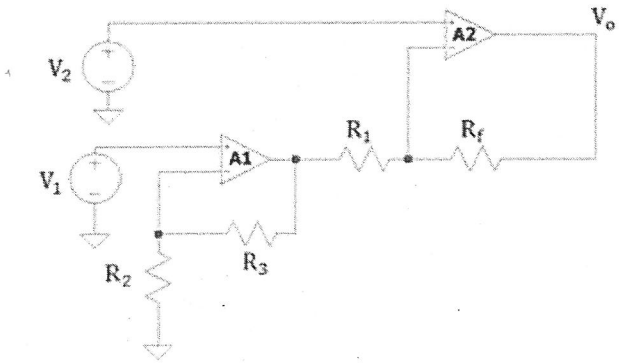
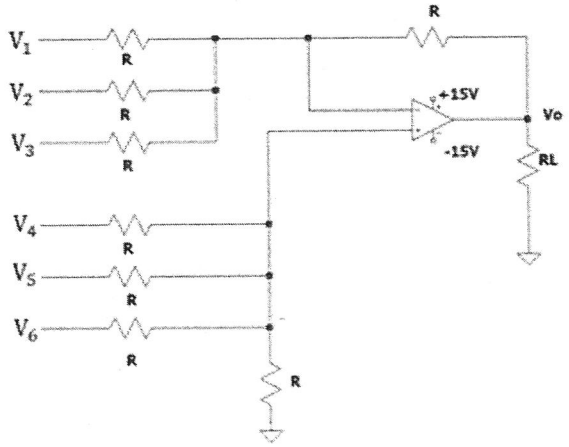


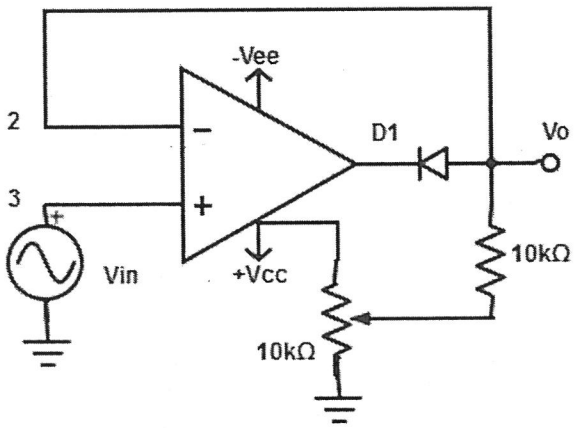
Figure 1

	ii.	What will be the emitter current in a differential amplifier, where both the transistor are biased and matched? (Assume current to be I_Q) (A) $I_E = I_Q/2$ (B) $I_E = I_Q$ (C) $I_E = (I_Q)^2/2$ (D) $I_E = (I_Q)^2$	1	1	1
	iii.	A differential amplifier has a transistor with β_0= 100, is biased at I_{CQ} = 0.48mA. Determine the value of CMRR and A_{CM}, if R_E =7.89kΩ and R_C = 5kΩ. (A) 49.54 db (B) 49.65 db (C) 49.77 db (D) 49.60 db	1	1	1

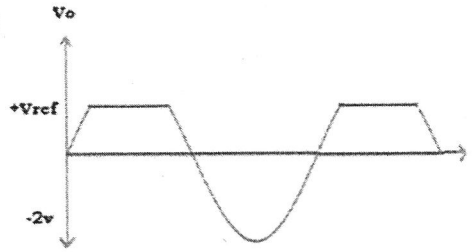
2. i. Analyze the function of the circuit shown in the Figure and derive its output voltage. Also, calculate the output voltage, where V_1=2V, V_2=5V, V_3=3V, V_4=1V, V_5=3V, V_6=2V. Assume that the op-amp is initially nulled . 18 4 2



ii. What happens if the potentiometer R_p (10 k Ohms)is connected to negative supply? 1 1 2



(A)



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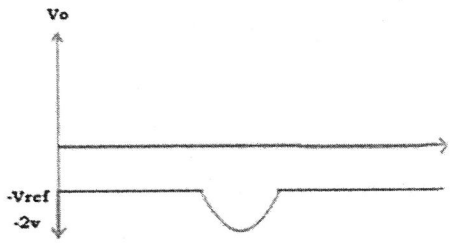

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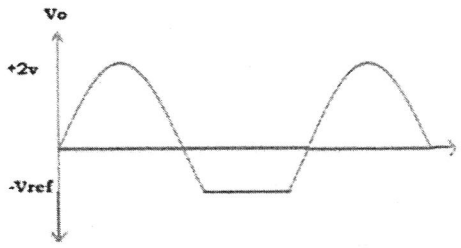
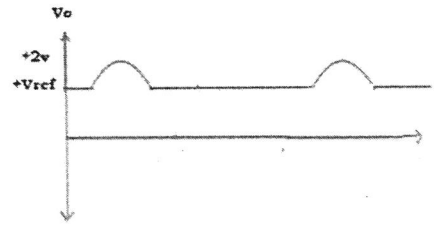


(D)



iii. How to minimize the response time and increase the operating frequency range of the op-amp? 1 1 2

(A) Positive halfwave rectifier with two diodes

(B) Positive halfwave rectifier with one diode

(C) Negative halfwave rectifier with two diodes

(D) Negative halfwave rectifier with one diode

3 i. a. Design a circuit using 555 timer, which will flash the electric bulb such that it's ON time will be 3 seconds and OFF time will be 1 second. [9 Marks] 18 4 3

b. Find the phase error necessary to produce a VCO frequency shift of Δf =10 KHz for an open loop gain of KV = 40 KHz/rad. What will be the deviation of phase error if Δf shifts to 5 KHz? [9 Marks]

ii. How to achieve 50% duty cycle in adjustable rectangular wave generator? (Assume R_1 –> Resistor connected between supply and discharge and R_2 –> Resistor connected between discharge and trigger input.) 1 1 3

(A) $R_1 < R_2$ (B) $R_1 > R_2$
(C) $R_1 = R_2$ (D) $R_1 \geq R_2$

iii. A basic feedback oscillator is satisfying the Barkhausen criterion. If the ß value is given as 0.7072, find the gain of basic amplifier? 1 1 3

(A) 2.1216 (B) 0.7072
(C) 1 (D) 1.414

4 i. a. Design an active low pass filter with a gain of 4, a corner frequency of 1 kHz, and a gain roll-off rate of −60 dB/decade. [9 Marks] 18 3 4

b. Design an active high pass filter with a gain of 10, a corner frequency of 2 kHz, and a gain roll-off rate of 40 dB/decade.[9 Marks]

ii. Find the High cut-off frequency if the pass band gain of a filter is 10. 1 1 4

(A) 70.7 Hz (B) 7.07 KHz
(C) 7.07 Hz (D) 707 Hz

iii. What happens if inductors are used in low frequency applications? 1 1 4

(A) Enhance inductor usage (B) No losses occurs
(C) Degrades inductor performance (D) Low power dissipation

5 i. a. "An ADC which uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods" - Identity a suitable ADC that will fulfill this statement and explain with an example how the input analog signal will be converted to digital output signal. [10 Marks] 18 3 5
b. A basic step of 8-Bit DAC has a resolution of 10 mV. Find the corresponding analog output voltage for the inputs 10101100.

ii. The smallest resistor in a 12 bit weighted resistor DAC is 2.5kΩ, what will be the largest resistor value? 1 1 5

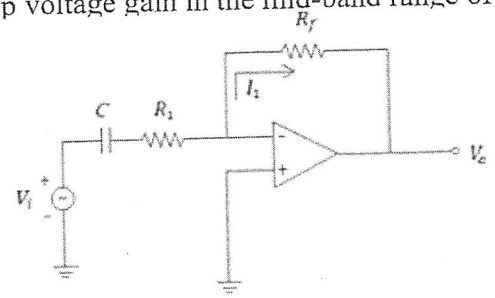
(A) 40.96MΩ (B) 10.24MΩ
(C) 61.44 MΩ (D) 18.43MΩ

iii. Find out the resolution of 8 bit DAC/ADC? 1 1 5

(A) 562 (B) 625
(C) 256 (D) 265

6 i. a. The drift parameter of an operational amplifier used in a non-inverting amplifier is given below. 18 3 2
Input offset voltage variation= ±12 µV/°C Input offset current variation= ±0.4 nA/° C Assuming R_f = 1.3 MΩ and R_i = 150KΩ and output V_o= 0 V at 25°C, find the output voltage at 60° C due to offset voltage variation and due to offset current variation. [9 Marks]

b. In the inverting AC amplifier circuit shown in Fig. below, Vi=2 V, C =0.1 µF, R1=15 KΩ, and Rf=150 KΩ. Calculate the lower 3dB frequency and the approximate closed-loop voltage gain in the mid-band range of frequencies. [9 Marks]



ii. How many equal intervals are present in a 14-bit D-A converter? 1 1 2

(A) 16383 (B) 4095
(C) 65535 (D) 1023

iii. How an AC amplifier can be powered by a single supply voltage, produces voltage swing? 1 1 2

(A) By inserting a voltage divider at the inverting input
(B) By inserting a voltage divider at the non-inverting input
(C) By inserting a voltage divider at the output
(D) By inserting a voltage divider at the feedback circuit

7 i. If an analog input of 8.3 V is given as an input to a 4 bit SAR ADC, illustrate the conversion code search sequence for a clock frequency of 100 Hz. Complete step by step search flow diagram starting from MSB with the block diagram of the 4 bit SAR ADC must be provided. Also if the full scale analog voltage is 15 V, provide the Digital VS Analog conversion chart with your assumed quantization level. 18 4 3

ii. Find the error voltage of phase comparator, whose input signal is $V_s = V_s\sin(2\pi f_s t)$ and the output signal $V_o = V_o\sin(2\pi f_o t+\varphi)$. 1 1 3

(A) $V_e=[k\times(V_s/2)]\times[\cos(-\varphi)-\cos(2\pi f_o t+\varphi)]$
(B) $V_e=[k\times V_s\times(V_o/2)]\times[\cos(-\varphi)-\cos(2\pi f_o t+\varphi)]$
(C) $V_e=[k\times V_s\times(V_o/2)]\times[\cos(-\varphi)+\cos(2\pi f_o t+\varphi)]$
(D) $V_e=[k\times V_s\times V_o]\times[\cos(-\phi)-\cos(2\pi f_o t+\phi)]$

iii. Calculate the value of external timing capacitor, if no modulating input signal is applied to VCO. Consider f_o=25 kHz and R_T=5 kΩ. 1 1 3

(A) 6nF
(B) 100μF
(C) 2nF
(D) 10nF

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