Pre-conditions:
$R_0 = 0\times00000000$
$R_1 = 0\times00005000$
$mem32[0\times00005000] = 0\times05050505$
$mem32[0\times00005004] = 0\times060060606$

(i) Instruction 1: LDR $R_0,[R_1,\#4]!$

(ii) Instruction 2: LDR $R_0,[R_1,\#4]$

(iii) Instruction 3: LDR $R_0,[R_1],\#4$

ii. Examine the updated values in the memory location and registers after the execution of SWP instruction for the given pre-condition. 5 3 1 1
Pre-condition:
$MEM32[0\times5000] = 0\times87654321$
$R_0 = 0\times00000000$
$R_1 = 0\times22221111$
$R_2 = 0\times00005000$
SWP R_0, R_1, $[R_2]$

(OR)

b.i. Explain the architecture of ARM microprocessor with a neat diagram. 5 2 1 1

ii. Draw and describe the complete register sets associated with ARM processor. 5 2 1 1

27. a. Explain the concept of relocating interrupt service routine address from interrupt vector table. 10 2 2 1

(OR)

b. Write an embedded C program to generate the time delay of 500 ms for the LED connected in port D 6th pin using timer implementation. Show the time delay calculation for the same program. 10 3 2 1

28. a. Explain the fundamental concepts of semaphores and classify the difference between binary semaphore and counting semaphore. 10 2 3 1

(OR)

b. Illustrate the concept of process management along with discuss the method of loading processes into physical memory of a microcontroller. 10 3 3 1

29. a. Explain how the threads are executed by the scheduler for five threaded implementations of blocked state. 10 3 4 1

(OR)

b. Explain the concept of fixed scheduling along with write a program to create four thread control blocks. 10 2 4 1

30. a. Explain the internal block diagram and operation of direct memory access controller with neat diagram. 10 2 5 1

(OR)

b.i. Illustrate the electrical interface between the micro-controller and the electrical cable with a neat diagram. 5 3 5 1

ii. Draw and describe the Ethernet data packet in communication systems. 5 3 5 1

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Reg. No.														

B.Tech. DEGREE EXAMINATION, DECEMBER 2022
Sixth and Seventh Semester

18ECC313J – EMBEDDED HARDWARE AND OPERATING SYSTEMS
(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

PART – A (25 × 1 = 25 Marks)
Answer **ALL** Questions

	Marks	BL	CO	PO

1. The main importance of ARM microprocessors is providing operation with _____ 1 1 1 1
(A) Low cost and low power consumption (B) High degree of multitasking
(C) Low error or glitches (D) Efficient memory management

2. Identify which of the following instruction is used to load constant vales in ARM instruction. 1 2 1 1
(A) LDR R0, # 0× FFFFFFFF (B) MOV R0, # 0×00FF0000
(C) STR R0, #0×FFFFFFFF (D) MVN R0, # 0×00FF0000

3. Each instruction in ARM machines is encoded into _____word. 1 2 1 1
(A) 2 bytes (B) 4 bytes
(C) 8 bytes (D) 10 bytes

4. The ability to shift or rotate in the same instruction along with other operation is performed with the help of _____ 1 2 1 1
(A) Barrel shifter (B) Switching circuit
(C) Arithmetic shifter unit (D) Logical switching circuit

5. For the given pre-condition, find the post-condition values after the execution of QADD instruction: 1 2 1 1
Pre-condition: CPSR = nzcvqiFt_SVC
R0 = 0×00000000
R1=0×70000000
R2=0×7FFFFFFF
QADD R0, R1, R2
Post-condition: CPSR =? And R0=?
(A) CPPSR= nZcvqiFT_SVC and R0=0×FFFFFFFF (B) CPSR=nzCvqiFt_SVC and R0=0×FFFFFFFF
(C) CPSR=nzcvQiFt_SVC and R0=0×7FFFFFFF (D) CPSR=nzcVQiFt_SVC and R0=0×7FFFFFFF

6. The interrupt vector table consists of a reset address of _____ 1 1 2 1
   (A) Stack pointer (B) Program counter
   (C) Link register (D) Instruction pointer

7. _____debug menu executes a single-step into a function, and executes the current instruction line. 1 1 2 1
   (A) Step (B) Step over
   (C) Step in (D) Step out

8. The vector interrupt controller has _____interrupt request inputs. 1 1 2 1
   (A) 8 (B) 16
   (C) 32 (D) 64

9. The systick time is used as a _____timer in cortex-M architecture. 1 1 2 1
   (A) Local (B) Global
   (C) Aperodic (D) Periodic

10. The _____register consists of bits for match and capture interrupts in LPC2124 microcontroller timer. 1 1 2 1
   (A) TOTCR (B) T1TCR
   (C) TOIR (D) TOTC

11. _____is the process of sending multiple bits of data over a single wire. 1 1 3 1
   (A) Parallel communication (B) Serial communication
   (C) I/O communication (D) Peripheral transfer

12. _____does not require to call an operating system and cause an interrupt to the kernel. 1 1 3 1
   (A) Context switching (B) Task switching
   (C) Process switching (D) Thread switching

13. The _____allows the computer to execute multiple threads at the same time. 1 1 3 1
   (A) Parallel programming (B) Serial programming
   (C) USB programming (D) Sequential programming

14. A _____thread is one that runs infrequently. 1 1 3 1
   (A) Periodic (B) Sporadic
   (C) Aperiodic (D) Independent

15. _____are integer variables that are used to solve the critical section problem. 1 1 3 1
   (A) Timers (B) Counters
   (C) Semaphores (D) Processes

16. A _____is a signaling mechanism. 1 1 4 1
   (A) Semaphore (B) Mutex
   (C) Spinlock (D) Tokens

17. To implement the sleep function, we could _____to each TCB and call it sleep. 1 1 4 1
   (A) Sub a timer (B) Add a timer
   (C) Sub a counter (D) Add a counter

18. The Little's theorem states _____ 1 1 4 1
   (A) $R = \frac{N}{T}$ (B) $T = \frac{N}{R}$
   (C) $L = N * R$ (D) $N = L * R$

19. A thread is in the _____state when it is waiting for some external event. 1 1 4 1
   (A) Ready (B) Running
   (C) Blocked (D) Suspended

20. Too make a spin-lock semaphore more efficient 1 2 4 1
   (A) Place a suspend in the while loop (B) Place a wait in the while loop
   (C) Remove the suspend from while loop (D) Remove the wait from while loop

21. _____protocol is designed to work on microcontrollers with as little as 10 KB of RAM. 1 2 5 1
   (A) MQTT (B) COAP
   (C) TCP (D) HTTP

22. A_____stands between two networks and passes frames from one network to another. 1 2 5 1
   (A) Switch (B) Connectors
   (C) Gateway (D) Router

23. The _____layer communicates with the Ethernet bus. 1 1 5 1
   (A) PHY (B) DLL
   (C) MAC (D) OSI

24. The _____is a digital output with a constant period, but variable duty cycle. 1 1 5 1
   (A) ADC (B) DAC
   (C) PWM (D) PCM

25. _____is the fraction of properly detected events. 1 1 5 1
   (A) Prevalence (B) Sensitivity
   (C) Specificity (D) Precision

PART – B (5 × 10 = 50 Marks) Marks BL CO PO
Answer **ALL** Questions

26. a.i. For the given pre-condition, illustrate and find the post-condition values after the execution of single-register transfer load instructions for various addressing modes 5 3 1 1