Reg. No.															

B.Tech/ M.Tech (Integrated) DEGREE EXAMINATION, MAY 2024

Fourth Semester

21CSE224T – COMPUTER ARCHITECTURE

(For the candidates admitted from the academic year 2022-2023 onwards)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours | Max. Marks: 75

PART – A (20 × 1 = 20Marks)

Answer **ALL** Questions

	Marks	BL	CO	PO
1. Find the BCD (Binary Coded Decimal) of number 84. (A) 1000 0100 (B) 0100 0100 (C) 1000 1001 (D) 1001 1100	1	2	1	2
2. Reflected binary code is also known as (A) Binary code (B) Gray code (C) Ascii code (D) BCD code	1	1	1	1
3. A NOR gate is logically equivalent to an OR gate followed by an (A) Invertor (B) XAND (C) AND (D) XOR	1	2	1	2
4. Find the result of adding 1101 and 1011 in binary (A) 10000 (B) 10110 (C) 11111 (D) 11000	1	3	1	2
5. Mnemonics refer to (A) Instruction (B) Program (C) Assembler (D) Machine language	1	1	2	1
6. Two important fields of an instruction are (A) Opcode and input data (B) Operand and memory (C) Only operant not opcode (D) Both opcode and operand	1	1	2	1
7. Which is the first step in the evolution of programing languages? (A) Machine learning (B) High level language (C) Assembly language (D) Coded language	1	1	2	1
8. Floating point representation is used to store (A) Boolean values (B) Real integers (C) Whole numbers (D) Integers	1	1	2	1
9. Which operation is typically not performed by the ALU? (A) Addition (B) Logical AND (C) Multiplication (D) Data Transfer	1	1	3	1

10. A group of bits that tells the computer to perform a specific operation is known as 1 1 3 2
    (A) Micro-operation (B) Accumulator
    (C) Register (D) Instruction code

11. Which type of instruction is used to alter the sequence of program execution by transferring control to another part of the program? 1 2 3 2
    (A) Arithmetic instruction (B) Logical instruction
    (C) Branch instruction (D) Data transfer instruction

12. Which of the following is not a hazard encountered in pipelined processors? 1 2 3 2
    (A) Data hazard (B) Instruction hazard
    (C) Control hazards (D) Pipeline hazards

13. Which memory has less access time? 1 2 4 2
    (A) Cache memory (B) Magnetic core memory
    (C) Random access memory (D) Auxiliary memory

14. Which of the statement refers to the associative memory? 1 1 4 1
    (A) The data are accessed sequentially (B) The data is used as an address
    (C) The address of data is generated by CPU (D) The address of data is supplied by user

15. Size of the virtual memory depends on _____. 1 2 4 1
    (A) Address line (B) Data space
    (C) Disc space (D) Memory

16. Which mechanism is used for accessing I/O (Input / Output) devices in a computer system? 1 2 4 2
    (A) Direct Memory Access (DMA) (B) Main memory
    (C) Interrupts (D) Cache memory

17. What are the basics of input / output operations in computer systems? 1 2 5 2
    (A) Loading and storing data in registers (B) Executing arithmetic and logical operations
    (C) Communicating with external device (D) Managing memory allocation

18. The number of clock cycle per second is referred as 1 2 5 2
    (A) Clock speed (B) Clock rate
    (C) Clock timing (D) Clock frequency

19. The input / output devices are also known as 1 1 5 1
    (A) Framework (B) Peripherals
    (C) Firmware (D) Software

20. Which instruction set architecture includes the thumb instruction set? 1 1 5 1
    (A) X86 (B) MIPS
    (C) Power PC (D) ARM

PART – B (5 × 8 = 40 Marks)

Answer **ALL** Questions

		Marks	BL	CO	PO
21. a.	Differentiate between BCD and XS-3 codes. Perform the operations using XS-3 codes. $(544)_{10} + (278)_{10}$	8	3	1	1
	(OR)				
b.	Explain universal gates also discuss how basic gates can be realized using NAND and NOR gate.	8	3	1	1
22. a.	Explain the various addressing modes with suitable example.	8	4	2	2
	(OR)				
b.	Describe the role of buses in any system for which purpose they are used. Explain different types of buses with suitable examples.	8	2	2	1
23. a.	Discuss the role of (IR) instruction register? Write the steps used to execute IR and also discuss the operations performed by using instruction register.	8	4	3	2
	(OR)				
b.	Compare hardwired control unit and microprogrammed control unit.	8	2	3	1
24. a.	Briefly explain about different types of pipeline hazards with suitable examples.	8	2	4	2
	(OR)				
b.	Explain mapping functions in cache memory to determine how memory blocks are placed in cache.	8	4	4	3
25. a.	Explain instruction level parallel processing and its challenges.	8	4	5	2
	(OR)				
b.	Compare Arm 5 and Arm 7 series processors with features and application.	8	3	5	2

PART – C (1 × 15 = 15 Marks)

Answer **ANY ONE** Question

		Marks	BL	CO	PO
26.	Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals.	15	4	4	3
27.	Evaluate: $X = (A - B) * \left(((-D * E) \mid F) \mid G\right)$ using all four types of addressing instructions.	15	4	2	2

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