Reg. No.															

B.Tech. DEGREE EXAMINATION, NOVEMBER 2023

Sixth Semester

18MHC205J – MICROCONTROLLERS AND EMBEDDED SYSTEMS

(For the candidates admitted from the academic year 2020-2021 & 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

	Marks	BL	CO	PO

PART – A (20 × 1 = 20 Marks)

Answer **ALL** Questions

1. AT89C2051 has RAM of — 1 1 1 1
   (A) 128 bytes (B) 256 bytes
   (C) 64 bytes (D) 512 bytes

2. When 8051 wakes up then 0X00 is loaded to which register? — 1 1 1 1
   (A) PSW (B) SP
   (C) PC (D) A register

3. On power up, the 8051 uses which RAM locations for $R_0 - R_7$. — 1 2 1 1
   (A) 00 – 2 F (B) 00 – 07
   (C) 00 – 7F (D) 00 – 0F

4. How many bytes of bit addressable memory is present in 8051 based microcontrollers? — 1 1 1 1
   (A) 8 bytes (B) 32 bytes
   (C) 16 bytes (D) 128 bytes

5. ARM processors are basically designed for — 1 1 2 1
   (A) Main frame systems (B) Distributed systems
   (C) Mobile systems (D) Super computer

6. The address space in ARM is — 1 1 2 1
   (A) 2^{24} (B) 2^{64}
   (C) 2^{16} (D) 2^{32}

7. The bank registers are used for — 1 1 2 1
   (A) Switching between supervisor and interrupt mode (B) Extended storing
   (C) Same as other general purpose register (D) Same as copied register

8. The addressing mode where the EA of the operand is the contents of R_n is — 1 1 2 1
   (A) Pre indexed mode (B) Pre indexed with write back mode
   (C) Post indexed mode (D) Switching mode

9. Which memory storage is used in embedded systems? 2 2 3 2
   (A) EEPROM (B) Flash memory
   (C) SRAM (D) DRAM

10. Which activity is concerned with identifying the task at the final embedded systems? 1 2 3 1
   (A) Scheduling (B) Task level concurrency management
   (C) High level transformation (D) Compilation

11. Which of the following helps in reducing the energy consumption of the embedded systems? 1 2 3 1
   (A) Emulator (B) Debuger
   (C) Simulator (D) Compiler

12. Which of the following is the pin efficient method of communicating between other devices?
   (A) Memory port (B) Peripheral port
   (C) Parallel port (D) Serial port

13. Identify the standard software components that can be reused in an embedded system design? 1 2 4 1
   (A) Memory (B) Application software
   (C) Application manager (D) Operating system

14. Which interrupts generate fast interrupt exception? 1 2 4 1
   (A) Software interrupt (B) Hardware interrupt
   (C) Internal interrupt (D) External interrupt

15. Which of the following is a part of RTOS kernel? 1 2 4 1
   (A) Register (B) ISR
   (C) Memory (D) Input

16. Time duration required for scheduling dispatcher to stop one process and start another is known as 1 2 4 1
   (A) Process latency (B) Dispatch latency
   (C) Execution latency (D) Interrupt latency

17. In rate monotonic scheduling 1 1 5 1
   (A) Shorter duration job has higher priority (B) Longer duration job has higher priority
   (C) Priority does not depend on the duration of the job (D) Not dependent on duration

18. In RTOS 1 1 5 1
   (A) All processes have the same priority (B) A task must be serviced by its deadline period
   (C) Process scheduling can be done only once (D) Kernel is not required

19.	Design technologies are developed to improve (A) Accuracy (B) Generation (C) Productivity (D) Time management	1	1	5	1
20.	Semaphore is a/an _____ to solve the critical section problem. (A) Hardware for a system (B) Special program for a system (C) Integer variable (D) Hardware and software combined	1	2	5	1

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

		Marks	BL	CO	PO
21.	Differentiate 8051 microcontroller and ARM controller.	4	4	1	2
22.	Explain the timer modes in 8051.	4	2	1	2
23.	Explain thumb state instruction in ARM7 controller.	4	2	2	2
24.	Develop an ALP to find the factorial of a number for implementation in ARM process.	4	4	2	4
25.	Illustrate co-design ladder with respect to embedded system.	4	3	3	1
26.	Discuss data transfer mechanism using DMA in embedded system.	4	3	4	2
27.	Explain the salient features of semaphore.	4	3	5	1

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
28. a.	Draw and explain the architecture of 8051 microcontroller.	12	2	1	2
	(OR)				
b.i	List out the various modes of operation of 8051 microcontroller and explain the mode 3 operation in detail.	6	2	1	1
ii.	Compare 8051 microcontroller and ARM microcontroller and discuss on its benefits over the other.	6	2	1	1
29. a.	Define addressing mode. Discuss the various types of addressing modes in ARM controller with appropriate examples.	12	4	2	2
	(OR)				
b.	Write an assembly language program to compute the expression (i) F=(A & B)/ (E & F)' (ii) $Z=ay^2+by+C$	12	4	2	2
30. a.	Define PLD and list out its types. Differentiate the types of PLD's with suitable examples.	12	3	3	1
	(OR)				

b.	List a pair of design metrics that may compete with one another, providing an intuitive explanation of the reason behind the competition.	12	4	3	1
31. a.i.	Draw the CDFG for the following code fragment. $x=1\ if\ (y==2)\{r=a+b;\ s=c-d;\}$ $else\{r=a-c;\}$	6	4	4	2
ii.	For the block given, write single assignment form and then draw the data flow graph $r=a+b-c;$ $s=2*r;$ $t=b-d;$ $r=d+e;$	6	4	4	2
	(OR)				
b.	For the sample C code, draw life term graphs before and after operator scheduling has been done $w=a+b;$ $x=c+d;$ $y=x+e;$ $z=a-b$	12	4	4	2
32. a.	Discuss in detail about round robin scheduling algorithm. Differentiate weighted round robin and priority driven approaches.	12	3	5	1
	(OR)				
b.	Illustrate EDF scheduling for the following process:				

Process	Execution time	Period
P_1	1	3
P_2	1	4
P_3	2	5

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