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B.Tech DEGREE EXAMINATION, NOVEMBER 2023

Seventh Semester

18ECE205J - FPGA - BASED EMBEDDED SYSTEM DESIGN

(For the candidates admitted during the academic year 2020 - 2021 & 2021 - 2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks) Marks BL CO

Answer **all** Questions

1. Which embedded design consider both the hardware and software during its design? 1 1 1
   (A) Memory Design (B) Software/ hardware code sign
   (C) Platform-based design (D) Peripheral design

2. A _____ is one in which failure could produce a catastrophic result, e.g. failure of a fire alarm system, or a pacemaker. 1 1 1
   (A) Soft Real-Time System (B) Firm Real-Time System
   (C) Hard Real-Time System (D) Continuous System

3. The maximum size of the External Data Memory space is ___ bytes. 1 1 1
   (A) 84 Bytes (B) 64 Bytes
   (C) 80 Bytes (D) 81 Bytes

4. _____ are devices that convert one or more physical parameters into digital or analog signals for processing and control applications 1 1 1
   (A) Sensor (B) Polling
   (C) FIFO (D) Looping

5. PSOC3 is a 1 1 2
   (A) True programmable embedded system-on-chip (B) . Semi-programmable embedded system-on-chip
   (C) unprogrammable embedded system-on-chip (D) programmable system-on-chip

6. The signal sent to the device from the processor to the device after receiving an interrupt is _____ 1 1 2
   (A) Interrupt-acknowledge (B) Return signal
   (C) Service signal (D) Permission signal

7. An interrupt that can be temporarily ignored is _____ 1 1 2
   (A) Vectored interrupt (B) Non-maskable interrupt
   (C) Maskable interrupt (D) High priority interrupt

8. Which interrupt can make a change in the processor mode? 1 1 2
   (A) internal interrupt (B) external interrupts
   (C) exceptions (D) software mode

9. How many logic gates can be implemented in the circuit by complex programmable logic devices (CPLDs)? 1 1 3
   (A) . 10 (B) 100
   (C) 1000 (D) 10000

10. In JTAG programming, JTAG stands for _____ 1 1 3
    (A) Joint Texture Analysis Group (B) Joint Technique Aided Group
    (C) Joint Testing Array Group (D) Joint Test Action Group

11.	_____ programming is a combination of non-volatility and re-programmability within a single chip providing a simple, secure, reliable and low-power solution for very cost-effective implementations (A) anti-fuse (B) SRAM (C) EEPROM / Flash (D) DRAM	1	1	3
12.	The _____programming technology is an old technique of producing one-time programmable devices in FPGA (A) anti-fuse (B) SRAM (C) EEPROM / Flash (D) DRAM	1	1	3
13.	SESE point Stands for _____ (A) Single End and Single Exit (B) Single Entry and Single Exit (C) Single Element Single Exit (D) Small Element and Small Entry	1	1	4
14.	A _____is a high-level language translator that runs on one platform but produces executable for another platform (A) Cross – Development (B) Cross – Compiler (C) Cross- assembler (D) Cross- Linker	1	1	4
15.	A system program that combines separately compiled modules of a program into a form suitable for execution is called _____ (A) Assembler (B) Linking Loader (C) Cross compiler (D) Debugger	1	1	4
16.	The collection of run-time information on an application during execution is referred as (A) Processing (B) Profiling (C) Partitioning (D) Planning	1	1	5
17.	Iteration-level parallelism is also known as (A) Data level parallelism (B) Bit level (C) Instruction level (D) Thread level	1	1	5
18.	The go/done model is actually a (A) Multithreaded Model (B) Network on-chip model (C) Single thread model (D) Co-processor Model	1	1	5
19.	Which mechanism can be used when the amount of time a feature runs is unknown? (A) Spin-lock (B) Coupling (C) Blocking (D) Rolling	1	1	5
20.	The co-processor model is also known as (A) Multithreaded Model (B) client/server model (C) Network on-chip model (D) Single thread model	1	1	5

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	What is an embedded system? Explain its essential components.	4	2	1
22.	List out the role of PLDs in embedded system design	4	1	1
23.	Explain any three instructions of 8051	4	2	2
24.	List out the different addressing modes of 8051	4	2	2
25.	Explain various slices used in Virtex 5	4	2	3
26.	Define the concept of Partitioning and Profiling	4	2	4
27.	Differentiate SIMD and MIMD architectures	4	4	5

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Explain in detail, the various embedded systems performance criteria with examples	12	4	1
	(OR)			
	(b) Estimate the cause of interrupt latency in embedded systems and its problems. Also, explain the measures to reduce it .			
29.	(a) Explain the functionality of PSoc3/5 architecture with 8051 implementations.	12	2	2
	(OR)			
	(b) Explain in detail about power management and clock distribution in PSoc3/5 architecture.			
30.	(a) Explain the concept of configurable logic blocks, slices, and block RAM used in Xilinx Virtex 5 with a neat diagram.	12	1	3
	(OR)			
	(b) Analyze and identify the various configuration blocks required for FPGA programming with a neat diagram			
31.	(a) Discuss the platform FPGA components (FPGA-Field Programmable Gate Array).	12	4	4
	(OR)			
	(b) Explain the Platform FPGA Components.			
32.	(a) Explain in detail the concept of on-chip and off-chip memory.	12	2	5
	(OR)			
	(b) Explain the different levels of parallelism.			

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