Reg. No.														

B.Tech. DEGREE EXAMINATION, MAY 2022
Sixth Semester

18ECC313J – EMBEDDED HARDWARE AND OPERATING SYSTEMS
(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

PART – A (25 × 1 = 25 Marks)
Answer **ALL** Questions

	Marks	BL	CO	PO
1. The address system supported by ARM systems is _____memory. (A) Little endian (B) Big endian (C) X-endian (D) Both little endian and big endian	1	1	1	1
2. The additional duplicate register used in ARM machines are called as _____ (A) Copied registers (B) Banked registers (C) Extra registers (D) Extremital registers	1	1	1	1
3. The instructions which are used to load or store multiple operands are called as _____ (A) Banked instructions (B) Coprocessor instructions (C) Block transfer instructions (D) Register/memory transfer instructions	1	2	1	1
4. Find the result upon execution of BIC instruction for the given below pre-condition: $R_1 = 0b1111$ $R_2 = 0b1010$ $BIC\ R_0, R_1, R_2$ Post-condition: R_0=? (A) $R_0 = 0b0101$ (B) $R_0 = 0b1010$ (C) $R_0 = 0b1111$ (D) $R_0 = 0b0000$	1	2	1	1
5. The registers R_{13}, R_{14} and R_{15} are sequentially used for (A) PC, LR and SP (B) LP, PC and SP (C) SP, LR and PC (D) GP, LR and SP	1	2	1	1
6. The microcontroller uses _____ to find the entry inside the interrupt vector table. (A) IVT address (B) ISR address (C) Return address (D) Interrupt number	1	1	2	1

ii. For the given pre-condition, illustrate the execution of following stack instructions: Pre – Condition: $R_1 = 0 \times 00000002$ $R_4 = 0 \times 00000003$ $SP = 0 \times 00080018$ *Instruction* 1 : $STMFD\ SP!, \{R_1, R_4\}$ *Instruction* 2 : $STMED\ SP!, \{R_1, R_4\}$	5	3	1	1
(OR)				
b. Explain the following concepts in cortex-m processor architecture. (i) Register set (ii) Stack operation	10	2	1	1
27. a. Describe the registers used in timers and discuss the step sequence involved in programming timers of ARM processor.	10	2	2	1
(OR)				
b. Explain the various ADC registers of ARM LPC2148 and write an assembly language program to read the converted value from channel 1 and channel 2 of ADC.	10	3	2	1
28. a. Illustrate the concept of establishing communication between two threads in embedded hardware operating system with necessary example.	10	2	3	1
(OR)				
b. Explain the overview of thread switching and write an assembly language program to describe thread switching.	10	3	3	1
29. a.i. Compare spin-lock and semaphore.	5	2	4	1
ii. Illustrate the various conditions for the deadlock occurrences in embedded operating system.	5	3	4	1
(OR)				
b.i. Explain the fundamental concept of deadlock using resource allocation graph.	5	2	4	1
ii. Discuss the methods to prevent deadlock in embedded operating system.	5	2	4	1
30. a.i. Illustrate the process of integrating individual components into a microcontroller based data acquisition system with neat diagram.	5	2	5	1
ii. Illustrate the performance metric attributes related to event detection in data acquisition system.	5	2	5	1
(OR)				
b. Explain the overview of application layer protocols for embedded systems.	10	3	5	1

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7. _____debug menu finishes executing the current function and stops afterwards. 1 1 2 1
(A) Step In (B) Step out
(C) Step over (D) Stop

8. The FIQ has the _____priority. 1 1 2 1
(A) Lowest (B) Medium
(C) Highest (D) Moderate

9. The _____timer is a core device on the cortex M architecture, which is commonly used as a periodic timer. 1 2 2 1
(A) Systick (B) Local
(C) Global (D) Event triggered

10. In LPC2148 microcontroller, the _____register is used to control the functions of the timer 0. 1 1 2 1
(A) TOTCR (B) TOPR
(C) TOPC (D) TOTC

11. The LPC2148 has _____inbuilt 10-bit ADC. 1 1 3 1
(A) One (B) Two
(C) Three (D) Four

12. An RTOS with a _____allows us to run multiple threads. 1 2 3 1
(A) Thread dispatcher (B) Thread kernel
(C) Thread scheduler (D) Thread swapper

13. In RTOS, if the process is an isolated means _____ 1 2 3 1
(A) It share I/O with any other process (B) It does not share I/O with any other process
(C) It share memory with any other process (D) It does not share memory with any other process

14. The _____programming allows the computer to execute multiple threads, but only one at a time. 1 1 3 1
(A) Serial (B) Parallel
(C) Concurrent (D) Sequential

15. A _____thread is one that runs at a fixed time interval. 1 1 3 1
(A) Periodic (B) Aperiodic
(C) Sporadic (D) Independent

16. The _____allows a thread to acquire it to simply wait in loop until lock is available. 1 1 4 1
(A) Semlock (B) Spin lock
(C) Mute lock (D) Wait lock

17. Another name of first-in-first-out queue is _____buffer. 1 1 4 1
(A) Serial (B) Parallel
(C) Concurrent (D) Bounded

18. In _____the threads are blocked as they are waiting on each other. 1 2 4 1
(A) Shared data problem (B) Semaphores
(C) Deadlock (D) Context switching

19. A very effective approach to deadlock is to _____timeouts to the wait function. 1 2 4 1
(A) Add (B) Remove
(C) Ignore (D) Subtract

20. The semaphore function _____will be called when it is appropriate for the blocked thread to continue. 1 1 4 1
(A) OS-event (B) OS-signal
(C) OS-continue (D) OS-run

21. _____protocol is used for communicating with low-power sensors and devices. 1 1 5 1
(A) TCP (B) HTTP
(C) MQTT (D) COAP

22. The _____layer provides transmit and receive processing for Ethernet frames. 1 1 5 1
(A) PHY (B) DLL
(C) MAC (D) Application

23. MQTT is a _____protocol. 1 1 5 1
(A) Master-slave (B) Connection less
(C) Request-response (D) Publish-subscribe

24. _____is the fraction of properly handled non-events. 1 1 5 1
(A) Sensitivity (B) Specificity
(C) Precision (D) Prevalence

25. The _____register contains the result to the most recent analog to digital conversion. 1 2 5 1
(A) ADOGDR (B) ADOCR
(C) ADGSR (D) ADOSTAT

PART – B (5 × 10 = 50 Marks)

Answer **ALL** Questions

Marks BL CO PO

26. a.i. For the given pre-condition, find the post-condition values after the execution of multiple-register store instructions for various addressing modes. 5 3 1 1

Pre – condition:

$R_0 = 0 \times 00000000$

$R_1 = 0 \times 00004000$

$R_2 = 0 \times 00005000$

$MEM32[0 \times 00004000] = 0 \times 00212121$

$MEM32[0 \times 01112122]$

(*i*) *Instruction* 1 : $STM\ R_0, [R_1, R_2]!$

(*ii*) *Instruction* 2 : $STM\ R_0, [R_1, R_2]$

(*iii*) *Instruction* 3 : $STM\ R_0, [R_1], R_2$