Reg. No															

B.Tech DEGREE EXAMINATION, NOVEMBER 2023

Fifth Semester

18EIC301J - EMBEDDED SYSTEM DESIGN

(For the candidates admitted during the academic year 2018-19 to 2021-22)

OPEN BOOK EXAMINATION

Note:

i. Specific approved THREE text books (Printed or photocopy) recommended for the course.
ii. Handwritten class notes (certified by the faculty handling the course / Head of the Department).

Time: 3 Hours **Max. Marks: 100**

Answer **FIVE** Questions
Question No. 7 is Compulsory.

		Marks	BL	CO
1 a.	i. Use 8086 microprocessor instruction to develop assembly language program for finding the factorial of a number. The number is in memory location 2000:0500H and store the result at 2000:0700H	18	6	1
b.	ii. Identify the flag manipulation instruction used in 8086 processor. (A) HLT (B) STC (C) ESC (D) NOP	1	1	1
c.	iii. Name the register which is used to hold I/O port address for I/O instruction. (A) AX (B) BX (C) CX (D) DX	1	1	1
2 a.	i. Develop an assembly language program using 8086 instruction to convert temperature in Fahrenheit to Celsius. The Fahrenheit value is in the memory 4000H: 1000H. Store the Celsius value in 5000:50H $℃ = (℉ - 32) * \frac{5}{9}$	18	6	1
b.	ii. POP instruction copies the top word from the stack to a destination specified in the instruction. After executing POP instruction in 8086 processor the stack pointer value is (A) Incremented one point (B) Incremented two points (C) Decremented one point (D) Decremented two points	1	1	1

c.	iii. MOV AX, 1234H
	MOV CL, 03
	MOV DL, AL
	ROR DL, CL
	After executing the above program in 8086 microprocessor, the result in DX register is
	(A) 1234 (B) 1286
	(C) 8246 (D) 8286
		1	1	1

3 a.	i. Develop a 8086 microprocessor based system having two 16K x 8 EPROM chips and two 8K x 8 RAM, such that the EPROM memory chip starting address assigned is FC000H and RAM memory chip starting address is AB000H. Use an address decoder made up of the 74138 IC and logic gates to interface this. Write the address decoding table and find the address range of the ROM and RAM memory. The 8086 microprocessor is in the maximum mode configuration.	18	3	2
b.	ii. _____ address lines are required to interface 32KB memory with a processor (A) 13 (B) 15 (C) 17 (D) 19	1	1	2
c.	iii. How many programmable interrupt controllers are required to interface 22 external interrupts with 8086 (A) 3 (B) 4 (C) 5 (D) 6	1	1	2

4 a.	i.	Assume that XTAL = 11.0592 MHz, write an assembly language program for 8051 microcontroller to generate a square wave of 2 kHz frequency (50% duty cycle) on pin P3.5. Timer 0 is used to generate the time delay. Analyze the program.	18	4	3
b.	ii.	To use on-chip ROM memory which signal pin is connected to Vcc (A) PSEN (B) PROG (C) EA (D) TXD	1	1	3
c.	iii.	Select the memory address for external hardware interrupt 0 (A) 0000 (B) 0003 (C) 000B (D) 001B	1	1	3
5 a.	i.	Examine the following program and find the time delay	18	4	3

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        CLR   P2.3
        MOV   TMOD,#01
HERE:   MOV   TL0,#3EH
        MOV   TH0,#0B8H
        SETB  P2.3
        SETB  TR0
AGAIN:  JNB   TF0,AGAIN
        CLR   TR0
        CLR   TF0
        CLR   P2.3
```

b.	ii.	The TMOD register value is 12H. Identify the modes of timers (A) Mode0 Timer0, Mode1 Timer1 (B) Mode1 Timer0, Mode2 Timer1 (C) Mode2 Timer0, Mode1 Timer1 (D) Mode2 Timer0, Mode2 Timer1	1	1	3
c.	iii.	Identify the TCON register value if the timer 1 over flow and timer 0 run mode. (A) A0 (B) B0 (C) 80 (D) 90	1	1	3
6 a.	i.	Develop an assembly language program for ARM processor to multiply two 32-bit numbers using MUL instruction and store a 64-bit result. Analyze the instructions used to store the higher 32-bits of the result. Also, brief the function of barrel shifter in executing ARM instructions, using a specific instruction as an example.	18	4	4
b.	ii.	In a RISC architecture, (A) The instructions are executed faster than CISC. (B) A reduced set of instructions means that the processor is unable to do some operations (C) Single instructions are available to do several operations together, namely reading data in memory, modifying it and then saving it (D) Instructions taking varying amount of cycle time	1	1	4
c.	iii.	Which of the following is false for RISC based ARM architecture? (A) It has separate Instruction cache and separate data cache (B) It has less power consumption (C) It has a Pipeline feature (D) Multiplier is not available	1	1	4
7 a.	i.	Design a micro controller-based controller for turning on and off the pump in a building, based on the water level in the over head tank. [Hint: Use 4 contact sensor to detect water level and accordingly either turn on or turn off the pump, also display the water level using 4 LEDs]	18	4	5
b.	ii.	Identify the symbol equivalent to ASCII code 63 (A) W (B) w (C) c (D) z	1	1	5

c. iii. _____ type ADC is the most versatile analog to digital convertor 1 1 5

(A) Servo tracking
(B) Counter type
(C) Dual slope
(D) Successive approximation

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