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B.Tech DEGREE EXAMINATION, MAY 2024

Third Semester

18AIS202T - DIGITAL LOGIC AND COMPUTER ARCHITECTURE

(For the candidates admitted during the academic year 2018-2019 to 2021-2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)

Answer **all** Questions

		Marks	BL	CO
1.	Find the result of multiplying the sign-magnitude numbers -12 and +8? (A) +96 (B) -4 (C) -96 (D) +4	1	1	1
2.	What is the octal equivalent of the decimal number 25? (A) 31 (B) 35 (C) 41 (D) 45	1	1	1
3.	Which of the following is not a valid hexadecimal digit? (A) A (B) B (C) F (D) G	1	1	1
4.	Find the binary representation of the hexadecimal number 2F? (A) 110111 (B) 101111 (C) 111011 (D) 111111	1	1	1
5.	What is the primary purpose of using a Karnaugh Map in simplifying Boolean expressions? (A) To complicate expressions (B) To generate larger expressions (C) To reduce the number of terms and literals (D) To increase the complexity of the circuit	1	1	2
6.	Which Boolean operation is represented by the symbol '+', indicating logical addition without carry? (A) AND (B) OR (C) XOR (D) NAND	1	1	2
7.	In a 2-to-4 demultiplexer, how many output lines are there? (A) 4 (B) 2 (C) 3 (D) 5	1	1	2
8.	What is the purpose of a priority encoder? (A) Combines multiple input lines into a single output line (B) Assigns priority to input lines based on their values (C) Expands a single input line into multiple output lines (D) Converts analog signals to digital signals	1	1	2
9.	Which of the following is NOT a common type of bus in computer architecture? (A) Data bus (B) Control bus (C) Address bus (D) Power bus	1	1	3
10.	In the instruction "SUB R4, R4, #10," what does "#10" represent? (A) An indirect addressing mode. (B) An offset value. (C) A memory address. (D) A register operand.	1	1	3

11.	Which addressing mode is often used to implement function calls and returns in assembly language? (A) Immediate (B) Register (C) Indirect (D) Stack	1	1	3
12.	During a register transfer operation, what does the Control Unit do? (A) Holds temporary data values (B) Performs arithmetic operations (C) Executes branch instructions (D) Manages the overall operation of the CPU	1	1	3
13.	In DMA operation, which component is responsible for controlling the data transfer between memory and I/O devices? (A) Central Processing Unit (CPU) (B) Memory (C) DMA controller (D) Input/Output devices	1	1	4
14.	What is the purpose of the interrupt vector table in computer architecture? (A) To map device interrupt requests to specific interrupt service routines (B) To store the addresses of all data in memory (C) To manage data transfer between the CPU and memory (D) To perform arithmetic operations	1	1	4
15.	What is the purpose of virtual memory in computer systems? (A) To store the operating system (B) To provide additional physical RAM (C) To extend the available RAM by using a portion of the hard disk (D) To cache frequently accessed data	1	1	4
16.	Which level of cache memory is typically the fastest but also the smallest in size? (A) L1 cache (B) L2 cache (C) L3 cache (D) RAM cache	1	1	4
17.	Choose the correct potential issue in pipelining can occur when one instruction depends on the result of a previous instruction, and the pipeline must stall to resolve it? (A) Pipeline hazard (B) Pipeline bubble (C) Pipeline flush (D) Pipeline segment	1	1	5
18.	What happens when a program tries to access a virtual memory address that is not currently in physical RAM? (A) The CPU executes a trap instruction. (B) The program is terminated. (C) The required page is brought in from secondary storage into RAM. (D) The CPU performs an immediate cache flush.	1	1	5
19.	In paging, what is the purpose of the page table? (A) To map virtual addresses to physical addresses (B) To store program instructions (C) To manage CPU pipeline stages (D) To hold data buffers for I/O operations	1	1	5
20.	In a fully associative cache, how are cache lines selected for replacement? (A) By using a direct-mapped technique (B) Randomly (C) Based on the memory block's address (D) Using a specific algorithm like LRU (Least Recently Used)	1	1	5

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	Illustrate the concept of binary representation and its significance in digital logic. Provide an example.	4	3	1

22.	Explain the fundamental operations of the three basic logic gates: AND, OR, and NOT. Provide truth tables for each gate and an example of their practical applications.	4	3	1
23.	Define hazard in digital logic and provide an example of a static-0 hazard and a dynamic hazard. How can hazards be minimized in digital circuits?	4	2	2
24.	Write the basic operation of a multiplexer and a demultiplexer. Provide an example of how a 4-to-1 multiplexer can be used and its truth table. How do demultiplexers complement the operation of multiplexers?	4	3	2
25.	Illustrate the concept of addressing modes in computer architecture. Provide brief descriptions of three common addressing modes and their significance in instruction execution.	4	2	3
26.	What is the concept of I/O organization in computer architecture. Provide a brief overview of why I/O organization is essential in modern computer systems.	4	3	4
27.	Explain the concept of data path and control considerations in computer architecture and their significance.	4	2	5

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Discuss the importance of various number systems (binary, decimal, octal, and hexadecimal) in digital logic and computing. Explain how conversions between these number systems are performed. Provide examples to illustrate the conversion processes.	12	3	1
	(OR)			
	(b) Analyse the concept of logical gates and discuss the fundamental types, including AND, OR, NOT, XOR, and NAND gates. Provide truth tables and practical examples for each gate to illustrate their functions and applications.			
29.	(a) Illustrate the concept of combinational logic circuits. Describe their structure, operation, and the different types of combinational logic gates. Provide examples of real-world applications and discuss their importance in digital systems.	12	3	2
	(OR)			
	(b) Explain the operation and applications of shift registers in digital circuits. Discuss different types of shift registers and their characteristics.			
30.	(a) You are working as a computer architect in a company that designs advanced microprocessors. The company has requested a report explaining the roles and interactions of the key functional units in a computer system. Provide an explanation using a practical example to illustrate how these units work together.	12	3	3
	(OR)			
	(b) Describe the different types of buses typically involved, their functions, and the advantages of using multiple buses. Additionally, discuss the trade-offs and considerations that architects face when deciding to implement multiple bus architectures in modern computer systems.			
31.	(a) Describe in detail the concept and significance of the Translation Lookaside Buffer (TLB) in computer architecture. Explain how it works, its role in memory management, and the advantages it offers in improving system performance. Provide examples of real-world scenarios where TLBs play a critical role.	12	3	4
	(OR)			
	(b) Discuss the role and importance of cache memory in the context of this mobile device, and provide insights into the design considerations, including cache size, associativity, and replacement policies. Explain how cache memory will impact the device's performance and energy efficiency.			

32. (a) Discuss the challenges and trade-offs associated with virtual memory and provide real-world examples where virtual memory plays a critical role.Describe its structure, operation, and the benefits it offers to digital systems. 12 3 5

(OR)

(b) Illustrate the concepts of cache memory mapping techniques, specifically associative and direct mapping, in computer architecture. Describe their structures, operations, advantages, and limitations.

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