Reg. No.															

MINOR CERTIFICATION EXAMINATION, MAY 2024

Third Semester

18CSC003J – COMPUTER ORGANIZATION AND ARCHITECTURE

(For the candidates admitted from the academic year 2018-2019 to 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)

Answer **ALL** Questions

	Marks	BL	CO	PO
1. When the ARM processor is running in thumb state, the size of the instructions is (A) 32 bit (B) 16 bit (C) 24 bit (D) 12 bit	1	1	1	1
2. The first phase of an interrupt phase is (A) PC ⇐ ISR address (B) POP the return address from the stack (C) CPU execute the instructions in ISR and the return (D) Save the value of PC in a stack	1	1	1	1
3. In Big Endian format, of 64-bit data, what is the starting byte address of the aligned words? (A) 0, 8, 16 (B) 0, 2, 4 (C) 0, 4, 8 (D) 2, 4, 6	1	1	1	1
4. Lower byte addresses are used for the most significant bytes of the word are used in which technique (A) Big Endian (B) Little Endian (C) Addressing mode (D) Location register	1	1	1	1
5. When we perform subtraction on –7 and –5 the answer in 2's complement form is (A) 11110 (B) 1110 (C) 1010 (D) 0010	1	2	1	1
6. The most efficient method followed by computers to multiple two unsigned numbers is _____. (A) Booth algorithm (B) Bit pair recording of multipliers (C) Restoring algorithm (D) Non restring algorithm	1	1	2	1
7. In the implementation of a multiplier circuit in the system we make use of _____. (A) Counter (B) Flip flop (C) Shift register (D) Push down stack	1	1	2	1

8. Convert hexa decimal number $(A2)_{16}$ to binary and identify it. 1 1 2 1
   (A) $(1010\ 0010)_2$ (B) $(1001\ 0001)_2$
   (C) $(1000\ 0010)_2$ (D) $(1010\ 0001)_2$

9. The disadvantages of the hardwired approach is _____. 1 1 3 1
   (A) It is less flexible (B) It cannot be used for complex instructions
   (C) It is costly (D) Less flexible and cannot be used for complete instructions

10. The situation wherein the data of operands are not available is called _____. 1 2 3 1
   (A) Data hazard (B) Stock
   (C) Dead lock (D) Structural hazard

11. _____ are caused by branch instructions and are known as control hazards in computer architecture. 1 1 3 1
   (A) Data hazard (B) Branch hazard
   (C) Structural hazard (D) Information hazard

12. Whenever the stream of instructions supplied by the instruction fetch unit is interrupted, the pipeline _____. 1 1 3 1
   (A) Stalls (B) Activated
   (C) Triggered (D) Starts

13. _____ do not have parallel processing capabilities. 1 1 4 1
   (A) Single instruction stream, single data stream (B) Single instruction stream, multiple data stream
   (C) Multiple instruction stream, multiple data stream (D) Multiple instruction stream, single data stream

14. The decision on when to execute on operation depend largely on the 1 1 4 1
   (A) Compiler (B) Hardware
   (C) Software (D) OS

15. In MIMD, each processor has a _____ program and an instruction stream in generated from _____ program. 1 1 4 1
   (A) Same, same (B) Separate, each
   (C) Same, each (D) Separate, separate

16. Instructions level parallelism achieves more than one instructions at a time through 1 1 4 1
   (A) Dynamic scheduling (B) Priority scheduling
   (C) Time-slot scheduling (D) Double scheduling

17. PCI stands for 1 1 5 1
   (A) Peripheral computer internet (B) Peripheral component interconnect
   (C) Processor computer interconnect (D) Processor cable interconnect

18. To overcome the lag in the operating speeds of the I/O device and processor we use 1 1 5 1
   (A) Buffer spaces (B) Status flags
   (C) Interrupt signals (D) Exceptions

19.	The tag bits of an address received form the processor are compared to the tag bits of each block to the cache to see if desired block is present called as (A) Direct mapping (B) Associative mapping (C) Set-associative mapping (D) Indirect mapping	1	1	5	1
20.	The device that is allowed to initiate data transfer on the bus at any given time is called (A) Bus arbiter (B) DMA controller (C) Bus master (D) Bus granter	1	1	5	1

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

		Marks	BL	CO	PO
21.	Draw and illustrate the connections between the processor and memory.	4	2	1	1
22.	Write down the steps for restoring and non-restoring division.	4	2	2	1
23.	Give the bit pair recoding for the following binary numbers (i) 1101101110 (ii) 1111101110	4	2	2	1
24.	Summarize the steps involved to process each instruction in a pipelined processors.	4	2	3	1
25.	Write down the control sequence for Move (R_1), R_2.	4	2	4	1
26.	Elaborate on software parallelism and its types.	4	2	4	1
27.	Write short note on DMA data transfer.	4	3	5	1

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
28. a.	List and explain various addressing modes, with its formats and example.	12	3	1	1
	(OR)				
b.	Represented the arithmetic statement $F = (A - B) / (C + D * E)$ in instruction formats.	12	3	1	1
29. a.	Write Booth's algorithm and perform Booth multiplication of –23×–19.	12	3	2	1
	(OR)				
b.	Write restoring division algorithm and perform restoring division of 10/3.	12	3	2	1
30. a.	What is meant by pipeline hazard? Discuss in detail about the types of hazards.	12	3	3	1
	(OR)				
b.	Describe the generation of control signals using hardwires control unit, with necessary diagram.	12	3	3	1

31. a.	Classify the different types of computer architecture proposed by Flynn's.	12	3	4	1
	(OR)				
b.	Discuss in detail the cache coherence problem and the protocol that is used to overcome cache coherence.	12	3	4	1
32. a.	Discuss on various mapping schemes used in cache design.	12	3	5	1
	(OR)				
b.	Explain how virtual memory address translation method works based on the concept of length pages? Discuss with a diagram.	12	3	5	1

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