Reg. No.															

B.Tech/ M.Tech (Integrated) DEGREE EXAMINATION, MAY 2024
Third Semester

21CSS201T – COMPUTER ORGANIZATION AND ARCHITECTURE
(For the candidates admitted from the academic year 2022-2023 onwards)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours | Max. Marks: 75

PART – A (20 × 1 = 20Marks)
Answer **ALL** Questions

	Marks	BL	CO	PO
1. The representation of hexadecimal number (6DE)H is decimal is _____. (A) $6*162+13*161+14*160$ (B) $6*162+12*161+13*160$ (C) $6*162+11*161+14*160$ (D) $6*162+14*161+15*160$	1	1	1	1
2. 1's complement of 1011101 is _____. (A) 0101110 (B) 1001101 (C) 0100010 (D) 1100101	1	1	1	1
3. Which of the following gate will give a 0 when both of its inputs are 1? (A) AND (B) OR (C) NAND (D) EXOR	1	1	1	1
4. _____ are universal gates. (A) NOT (B) NAND & NOR (C) AND (D) NOT, AND & OR	1	1	1	1
5. _____ is the sequence of operation performed by CPU in processing an instruction. (A) Execute cycle (B) Fetch cycle (C) Decode (D) Instruction cycle	1	1	2	1
6. A register capable of shifting its binary information either to the right or the left is called a _____. (A) Parallel register (B) Serial register (C) Shift register (D) Storage register	1	1	2	1
7. Which interrupt services save all the register and flags (A) Save interrupt (B) Input/ output interrupt (C) Service interrupt (D) Save and service interrupt	1	1	2	1
8. In multiple bus organization, the registers are collectively placed and referred as _____. (A) Set registers (B) Register file (C) Register block (D) Map registers	1	1	2	1

9. Which of the following is used for binary multiplication? 1 1 3 1

(A) Restoring multiplication (B) Booth's algorithm
(C) Pascal's rule (D) Digit-by-digit multiplication

10. According to De-Morgan's theorem: NAND = _____. 1 1 3 1

(A) Bubbled AND (B) Bubbled NOR
(C) Bubbled XOR (D) Bubbled OR

11. The sign followed by the string of digits is called as _____. 1 1 3 1

(A) Significant (B) Determinant
(C) Mantissa (D) Exponent

12. In 32 bit representation the scale factor as a range of _____. 1 1 3 1

(A) –128 to 127 (B) –256 to 255
(C) 0 to 255 (D) –128 to 255

13. What does the RUN signal do? 1 1 4 1

(A) It causes the termination of a signal (B) It causes a particular signal to performs its operation
(C) It causes a particular signal to end (D) It increments the step counter by one

14. The disadvantage/s of the hardwired approach is _____. 1 1 4 1

(A) It is less flexible (B) It cannot be used for complex instructions
(C) It is costly (D) Less flexile and cannot be used for complex instructions

15. In pipelining each stage is given _____ time for the operation. 1 1 4 1

(A) Equal (B) Different
(C) Infinite (D) No / zero

16. The instruction processing unit fetches and decodes _____ and _____ instructions. 1 1 4 1

(A) Vector, sub vector (B) Pipelines, parallel task
(C) Scalar, vector (D) Pipelines, scalar

17. MIMD stands for 1 1 5 1

(A) Multiple input multiple data (B) Memory input multiple data
(C) Multiple instruction multiple data (D) Memory instruction multiple data

18. When the processor is executing in ARM stage, then all instructions are _____ wide. 1 1 5 1

(A) 8 bits (B) 16 bits
(C) 32 bits (D) 64 bits

19. The frequency of load / store instruction is around _____. 1 1 5 1

(A) 20% (B) 10%
(C) 40% (D) 67%

20.	During a write operation if the required block is not present in the cache then _____ occurs (A) Write miss (B) Write latency (C) Write hit (D) Write delay	1	1	5	1

PART – B (5 × 8 = 40 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
21. a.	Differentiate between decimal, binary, octal and hexadecimal.	8	1	1	1
	(OR)				
b.i.	Subtract 111001_2 from 101011_2 using the 1's complement method.	4	1	1	1,2
ii.	Subtract 101011_2 from 111001_2 using the 2's complement method.	4	1	1	1,2
22. a.	Give the control sequence for execution of instruction.	8	2	2	1
	(OR)				
b.	Describe the importance of different addressing modes in computer architecture.	8	2	2	1
23. a.	Assume A = (+8) and B = (+5). Multiple these two numbers using booth algorithm show the step-by-step multiplication process.	8	3	3	1,2
	(OR)				
b.	Write the IEEE 754 format for representing floating point number in single precision and double precision format represent the decimal number 10.25 using IEEE 754 single precision floating point format.	8	2	3	1,2
24. a.	Find the complete control sequence for execution of the instruction Add(R3), R1 for the single bus CPU.	8	2	4	1
	(OR)				
b.	Discuss about branch prediction with example.	8	2	4	1
25. a.	Explain in detail about MESI protocol with a neat diagram.	8	2	5	1
	(OR)				
b.	The parallel computer architecture adds a new dimension in the development of computer system by using more and more number of processor. In principle, performance of a single processor at a given point of time. Justify and describe the need of parallelism. Compare which types of parallelism is need for the real time scenario.	8	1	5	1

PART – C (1 × 15 = 15 Marks)
Answer **ANY ONE** Question

		Marks	BL	CO	PO
26.	An instruction is stores at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is.	15	3	2	1

(i) direct
(ii) immediate
(iii) relative
(iv) register indirect
(v) index with R1 as the index register

27. Demonstrate the general configuration of micro programmed control unit with a neat block diagram. 15 2 4 1

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