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B.Tech DEGREE EXAMINATION, DECEMBER 2023

Fifth Semester

18ECE303T - NANOELECTRONIC DEVICES AND CIRCUITS

(For the candidates admitted during the academic year 2020 - 2021 & 2021 - 2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)

Answer **all** Questions

		Marks	BL	CO
1.	Moore's law states_____ (A) physical size (B) number of transistor per chip (C) gate length (D) Substrate size	1	1	1
2.	MOSFET has_____terminals (A) 1 (B) 2 (C) 3 (D) 4	1	1	5
3.	Lateral scaling of gate oxide thickness is (A) 1/β (B) 1/β2 (C) β2 (D) α/β2	1	1	1
4.	What is the condition of the cut-off region? (A) VGS> VTH (B) VGS (C) VGS=VTH (D) VGS= 0	1	2	3
5.	Channel length modulation in MOSFET makes the drain current (A) to decrease with drain-to-source voltage (B) independent of drain voltage (C) to increase with drain-to-source voltage (D) zero	1	1	3
6.	The chiral vector of the graphene layer determines the properties of nanotubes (A) magnetic (B) optical (C) chemical (D) electrical	1	2	5
7.	What phenomenon allows for the conversion between charge and spin currents in spintronics? (A) Hall Effect (B) Spin-Orbit Interaction (C) Ohm's Law (D) Faraday's Law	1	2	3
8.	In the negative resistance concept, an increase in the voltage of a device leads to a _____ in current quantity. (A) decrease (B) increase (C) zero (D) constant	1	4	5
9.	Which property of electrons is utilized in MRAM for data storage? (A) spin (B) charge (C) mass (D) velocity	1	1	4
10.	Tunneling is a _____ phenomenon? (A) quantum physics (B) quantum mechanical (C) quantum chemical (D) quantum maths	1	1	4

11.	The transconductance of a CNT MOSFET is_____ (A) 2321 (B) 150 (C) 260 (D) 2100	1	2	6
12.	Multi-walled CNTs are concentric nanotubes. (A) single (B) multiple (C) triple (D) double	1	2	4
13.	Which non-volatile memory type is known for its high speed and resistance to radiation-induced data loss? (A) MRAM (B) Flash Memory (C) EEPROM (D) FRAM	1	1	6
14.	What is the building block of carbon nanotubes? (A) graphene (B) Mini tubes (C) lattice (D) unit cell	1	1	4
15.	A Tunnel based FET works on _____ tunneling. (A) Band to band (B) band to Fermi (C) band to conduction (D) valence to Fermi	1	1	3
16.	The in-and-out bus lines should be in_____ (A) polysilicon (B) diffusion (C) metal (D) silicon	1	1	6
17.	Choose the correct order of increasing minimum size of feature obtained in photolithography by different lights (A) UV light > X-rays > Blue light > Red light (B) X-rays > UV light > Blue light > Red light (C) X-rays < UV light < Blue light < Red light (D) U V Light	1	1	5
18.	Which of the ceramic components is easier through nanostructuring? (A) lubrication (B) coating (C) wear (D) fabrication	1	1	2
19.	Who first used the term nanotechnology? (A) Richard Feymann (B) Norio Taniguichi (C) Eric Drexler (D) Sumio Lijima	1	1	1
20.	How many oxygen atoms lined up in a row would fit in a 1-nanometer space? (A) FIve (B) one (C) seven (D) seventy	1	1	1

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	What is the difference between high-K and low-K dielectric materials?	4	1	1
22.	What is the short-channel effect? List out the short channel effects in MOSFET.	4	1	1
23.	What is the difference between high-K and low-K dielectric materials?	4	1	1
24.	Write a short note on TMR.	4	1	3
25.	Write a short note on the Coulomb blockade.	4	1	2
26.	Explain the electrical properties of CNT.	4	1	2
27.	Discuss the metal-insulator-metal junction.	4	1	2

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO

28.	(a) What is the need of MOSFET scaling and discuss the types of scaling with necessary parameters for the scaling of MOSFET.	12	1	2
	(OR)			
	(b) Explain the MOSFET under static conditions with necessary diagrams			
29.	(a) What is SOI MOSFET? Explain the working of partially depleted SOI MOSFET?	12	1	2
	(OR)			
	(b) Explain Fin FET with structure. Also compare Fin FET and double gate MOSFET.			
30.	(a) Describe the CMOS technology scaling with performance parameters.	12	3	2
	(OR)			
	(b) (i) Write the innovations needed to continue performance scaling in nanoelectronics. (ii) Write the reliability concerns in scaling.			
31.	(a) Write a short note on (i) Decoupling (ii) Noise isolation	12	2	2
	(OR)			
	(b) Describe the guard ring structures of isolated NMOS devices.			
32.	(a) Explain single electron transistor with their structure.	12	4	5
	(OR)			
	(b) Describe the various structure of carbon nano tube.			

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