28. a.	Interpret the concept of configurable logic blocks used in Xilinx virtex 5 with neat diagram.	10	3	3	2,3 ,1
	(OR)					
b.	Develop the various slices available in XILINX virtex 5 IDE for integrated environment.	10	3	3	2,4 ,1
29. a.	Illustrate the platform FPGA components in detail.	10	2	4	2,3 ,1
	(OR)					
b.	Explain with an example to illustrate the different ways components can be combined to form large modules.	10	3	4	3,2 ,1
30. a.	Interpret the different levels of parallelism in detail.	10	2	5	2,3 ,1
	(OR)					
b.	Define profiling and explain the practical issues faced during profiling.	10	2	5	1,4 ,1

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Reg. No.														

B.Tech. DEGREE EXAMINATION, NOVEMBER 2022
Sixth and Seventh Semester

18ECE205J – FPGA-BASED EMBEDDED SYSTEM DESIGN
(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

PART – A (25 × 1 = 25 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
1.	Which design allows the reuse of software and the hardware components? (A) Memory design (B) Input design (C) Platform based design (D) Peripheral design	1	2	1	4
2.	The _____configuration has only one "zero" location for both data and memory. (A) Von Neumann memory (B) Harvard memory (C) Memory (D) CPU	1	1	1	1
3.	The maximum size of the external data memory space is _____bytes. (A) 84 (B) 64 (C) 80 (D) 81	1	1	1	1
4.	Which design can be used to reduce the energy consumption of the embedded system? (A) Simulator (B) Compiler (C) Emulator (D) Debugger	1	1	1	1
5.	The technique where by the DMA controller steals the access cycles of the processor to operate is called _____ (A) Fast conning (B) Memory con (C) Cycle stealing (D) Memory stealing	1	1	1	1
6.	FPGA device are _____types. (A) PLD (B) EPROM (C) SROM (D) SLD	1	1	2	2
7.	How many logic gates can be implemented in the circuit by complex programmable logic devices? (A) 10 (B) 100 (C) 1000 (D) 10000	1	2	2	2

8. Which among the following are used in PAL for reducing the loading on inputs? 1 1 2 2
(A) Input buffers (B) Output buffers
(C) Or matrix (D) And matrix

9. In DMA transfers, the required signals and addresses are given by the _____ 1 1 2 1
(A) Processor (B) Device drivers
(C) DMA controllers (D) The program itself

10. Which interrupt is unmaskable? 1 1 2 2
(A) RST 5.5 (B) RST 7.5
(C) TRAP (D) Both RST 5.5 and 7.5

11. Identify the variant in XILINX 5 virtex IDE that is mainly for digital signal processing applications 1 2 3 1
(A) SX (B) LX
(C) TX (D) FX

12. An embedded system has _____ 1 2 3 2
(A) Response time constraints (B) Strict deadlines
(C) Turn around time (D) Response time constraints and strict deadlines

13. Configurable logic blocks in FPGA are based on _____ 1 2 3 1
(A) Look up tables (B) Programmable interconnect
(C) Carry look ahead logic (D) Logic cell

14. In FPGA, _____ provides interface between package pins and CLBs. 1 2 3 2
(A) Input output blocks (B) Functional blocks
(C) Simulator (D) Synthesis

15. A combination PLD with a fixed array and array and a programmable OR array is called _____ 1 2 3 1
(A) PLD (B) PROM
(C) PAL (D) PLA

16. A system program that combines separately compiled modules of a program into a form suitable for execution is called _____ 1 2 4 2
(A) Assembler (B) Linking loader
(C) Cross compiler (D) Debugger

17. In VLSI design, which process deals with determination of resistance and capacitance of interconnections? 1 2 4 2
(A) Floor planning (B) Placement and routing
(C) Testing (D) Extraction

18. Which attribute in synthesis process specify the resistance by controlling the quantity of current it can source? 1 2 4 1
(A) Load attribute (B) Drive attribute
(C) Combinational attribute (D) Sequential attribute

19. Which type of simulation mode is used to check the timing performance of a design? 1 2 5 2
(A) Behavioural (B) Switch level
(C) Transistor level (D) Gate level

20. Which type of digital system exhibit the necessity for the existence of at least one feedback path from output to input? 1 2 5 1
(A) Combination system (B) Sequential system
(C) Load attribute (D) Drive attribute

21. The coprocessor model is also known as _____ 1 2 6 2
(A) Client/server model (B) Multithread model
(C) Network onchip model (D) Single thread model

22. A process network is a design abstraction in which functional components called processes communicate through data items called _____ 1 2 5 2
(A) RTL (B) Tokens
(C) FIFO (D) LIFO

23. Register transfer level description specifies all of the registers in a design and _____logic between them. 1 2 6 2
(A) Sequential (B) Combinational
(C) Spatial (D) On chip

24. The function based ESL design method uses _____model to compose different functional components into a complete system. 1 2 5 2
(A) Process (B) Computational
(C) Communication (D) Sequential

25. Hold time is defined as the time required for the data to _____after the triggering edge of clock. 1 2 5 2
(A) Increase (B) Decrease
(C) Hold (D) Remain stable

PART – B (5 × 10 = 50 Marks) Marks BL CO PO
Answer **ALL** Questions

26. a. Demonstrate and explain various types of mechanisms in interrupt service handling process and the need of DMA in embedded systems. 10 2 1 2,2,1

(OR)

b. Illustrate the sensor and its different types with real time examples. 10 2 1 2,1,2

27. a. Illustrate the $PSOC_3$ architecture with a neat block diagram. 10 3 2 1,4,1

(OR)

b. Explain in detail about power management and internal regulators. 10 3 2 2,4,1