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06DF4-18BMC205J

B.Tech. DEGREE EXAMINATION, DECEMBER 2023 Fourth Semester

18BMC205J – LINEAR AND DIGITAL INTEGRATED CIRCUITS (For the candidates admitted from the academic year 2020-2021 to 2021-2022)

	Note:	(or the candida	ates admitted from the academic INTEGRATED C	RCUITS
	(i)	Part - A should t	swered in OMR sheet within first 40 minutes and O ould be answered in answer booklet.	2021-2022)
		Over to hall invital	in ONIK sheet within fame as	2022)
	(ii)	Part - B & Part C	at the end of 40th minute	MR sheet should be
		- wratt- Csho	at the end of 40 th minute. Sould be answered in answer booklet.	should be handed
1	Time: 3	hours	wer booklet.	
/-		•		
		 .		Max. Marks: 100
		PART	$\Gamma - A (20 \times 1 = 20 \text{ Marks})$	100 viarks: 100
	1.	Voltage C. II	nswer ALL Questions	Marks BL CO PO
	-•	or on our	it acts as	co p ₀
		(A) an amplifier		1 1 1 10
		(C) an impedance mat	ching circuit (B) a multiplier	1 1,2
		Todanec mai	ching circuit (D) an inverter	,3
	2. ′	The output of a different		
	(A) image 1	tiator when applied with a step input is	
	(C) ramp	(P)	1 1 1 1,2
	(C) ramp	(B) step	,3
	3. T	ha at:	(D) sine	
	J. 1	he clipping level in op-a	amp is determined to	
				1 1 1 1 1
	(C	Reference voltage	(B) Control voltage	1 1 1,2
			(D) Input voltage	,5
	4. Th	e trans resistance ampli	£	
	(A	Crame annipit	Her is a	
	(C)	Current to voltage co	nverter (B) Vol	1 1 1,2
	(0)	controlled	current (D) Value Current converter	,3
		source	controlled on	nt
	5. The	0	Source	III
	o. The	feedback signal of basi	c sine wave oscillator is given as	
	(A)	$V_f = A\beta \times V_o$	o sine wave oscillator is given as	1 2 1 12
	(C)	$V_f = A\beta \times (V_o/V_i)$	(\sim) $V_1 \sim Ab \times V$.	1 2 1 1,2
			(D) $V_c = \Lambda D \times \sigma x = 0$	* 18
	o. The	number of RC stages at	The used in the RC phase shift oscillator is	
	(A)	Six	e used in the RC phase shift oscillator is	
	(C)	Four	(B) Two	1 2 1 1,2
	_		(D) Three	
,	· An ef	ficient oscillator operate Class A		
	(A)	Class A	es in mode	
	(C) (Class C	(B) Class B	1. 2 1 1,2
			(D) Class AD	
8.	The in	Out resistor and a	k resistor of a phase shift oscillator are	
	related	by	k resistor of a phase ship	
	(A) R	=92 R.	sinn oscillator are	1 2 1 1,2
	(C) R_{f}		(B) $R_1 < 29R_1$	~ 940
1 of 3	. ,	~71(]	(D) $R_f = 29R_1$	
			(-) 11-29K1	

	1	
	· twne	
9. The fastest analog to digital convert	er istype	
(A) Successive Approximation	(B) Flash	
		3
(C) Counter type	D/A converter with a reference	
1 sion of a 4-bit R-2R lad	(D) Dual-stope der type D/A converter with a reference 1 (D) 21 25 uA	
10. The resolution of a $R=10K\Omega$ is	- 1 0 5 · · A	
voltage of 5 v and	$(B) 31.23 \mu^2$	
(A) 62.5μ A	(D) 145 μA	3 1
		· .
(1:4)	gital-to-analog converter (DAC) is: (B) 15.6%	
11. The resolution of a 0-5 V 6-bit of	gital to the	
	(B) 15.6%	
(A) 63%	(D) 1.56%	1 3 1 2,4
(C) 64%	of each comparator is	
- 1 - log to-digital cor	everter, the output of output of	
12. In a flash analog-to-distant	(D) 1.56% Everter, the output of each comparator is	
connected to an input of a	(B) Demultiplexer	
" " 1.1 1 arror		11.2
(A) Munipieres	(D) Decodes	1,2
(C) Priority encodes	16 Ador the carry is given by	1 4 1 ,5,
12 rs A and B are the inputs of a ha	alf adder, the carry is given by	
13. If A and D are	m A OR B	
AND D	(B) A OR B	
(A) A AND B	(D) A EX-NOR B	1,2
(C) A XOR B	- an leader is	1 4 1 ,3,
-foutputs preser	it in a BCD decoder is	•,•
(C) A XOR B 14. The number of outputs preser		
	(B) \supset	
(A) 4		1,2
(C) 15	(D) 10 input lines is equal to 2 ^m then it requires	S 1 4 1 ,3,
f n selected	input lines is equal to 2 m	4,5
15. If the number of h sciences	•	
select inics.	(B) m	
(A) 2	(D) 2^n	1,2
(C) n		1 4 1 ,3,
16. Reflected binary code is also	known as	4,5
16. Reflected binary code is ans	1	
	(R) Billary Com	
(A) BCD code	(D) Gray Code	1 5 1 2,4
(C) ASCII code	(11)	1 5 1 2,1
(C) About	flip-flop cycle, the output will (B) Change (B) Toggle	
17 When both inputs of a J-K	(B) Change	
(A) Be invalid	(D) Toggle	, 5 1 2,4
(A) Not change	Goodly in n-bit bit	nary
(C) NOT OHER-B	(D) Toggle range of bit-count specifically in n-bit bin number of flip-flops is $\frac{1}{(2n+1)}$	
18. The maximum possible	range of the country of flip-flops is (B) 0 to $2^{n} + 1$	
counter consisting of 'n' I		
		1 5 1 2,
$(A) 0 \text{ to } 2^n - 1$	(D) o to -	tes or
(C) 0 to 2 1	r sequence, there are a total of now many	
19 In a 4-bit Johnson count	er sequence, there are a total of how many stat	
bit patterns?	(B) 3	*
(A) 1	(D) 8	1 5 1
(A) 1		
(C) 4 20. Ripple counters are also	(B) Asynchronous counters	
20. Ripple counters are the	(B) Asylicinological and a sylicinological a	
(A) SSI counters (C) Synchronous cour	Itoro	06DF4-18BMC205
		¥ =-

	PART – B ($5 \times 4 = 20$ Marks) Answer ANY FIVE Questions	Marks	BŁ	со	PO
21.	Classify summing and scaling amplifier.	4	1	1	1,2
	Identify the gain equation of inverting amplifier with proper circuit diagram.				,3 1,2 ,3
23	List different types of comparators.	4	2	1	1,2
	List out the advantages of inverted R-2R ladder type D/A converter over weighted resistor type.	4	3	1	2,4
25.	25. An 8-bit A/D converter is used for converting 0 to 10V input voltage. Determine the digital output for an input voltage of 4.8V.			2	2,4
26.	·				1,2 ,3, 4,5
27.	27. Explain briefly on different types of Registers.				2,4
	PART – C ($5 \times 12 = 60$ Marks) Answer ALL Questions	Marks	BL	co	PO
28. a.	Derive the output equation of full wave precision rectifier using op-amp.	12	1	2	1,2 ,3
b.	(OR) Derive the output equation of (i) Differentiator (ii) Integrator.	12	1	2	1,2 ,3
29. a.	Explain the working of RC phase shift oscillator with suitable circuit diagram.	12	2	1	1,2
b.	(OR) Design a wide band pass filter having f_L =200HZ, f_H =2 KZ and pass band gain of 4. Find the value of Q of the filter. Assume C=0.1 μ F.	12	2	2	1,2
30. a.	0. a. Design a Successive Approximation Converter for analog voltage V _a =11 V and explain the conversion procedure step by step.			2	2,4
b.	(OR) Explain the working of flash ADC with suitable circuit diagram.	12	3	1	2,4
31. a.	Design a 4-bit Gray code TO BINARY converter and implement it using logic gates.	12	4	2	1,2 ,3, 4,5
b.i.	(OR) Implement the following Boolean function using 8:1 Mux: $F(A,B,C,D)=\sum m(0,1,3,4,8,9,15)$.	12	4	2	1,2 ,3, 4,5
ii.	Design a full subtractor using half subtractors.				
32. a.	Design a Mod 5 ripple counter using T Flip Flop. (OR)	12	5	2	2,3 ,4
b.	Design a PLA for the Logic Expression. F1=AB+AC'+AB'C' F2=AC+BC+AB	12	5	2	2,4