b.	Discuss the platform FPGA components. [FPGA – Field Programmable Gate Array].	10	2	5	4
30. a.	Explain the different levels of parallelism.	10	2	5	4
	(OR)				
b.	Explain in detail the concept of on-chip and off-chip memory.	10	2	2	3

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Reg. No.														

B.Tech. DEGREE EXAMINATION, MAY 2022

Seventh Semester

18ECE205J – FPGA BASED EMBEDDED SYSTEM DESIGN

(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

PART – A (25 × 1 = 25 Marks) — Marks | BL | CO | PO

Answer **ALL** Questions

1. All interrupts are serviced by branching to the same service program by — 1 | 1 | 1 | 1
   (A) Polling (B) Daisy chaining
   (C) Scalar interrupts (D) Vector interrupts

2. The Direct Memory Access (DMA) controller has _____ register. — 1 | 1 | 1 | 1
   (A) 4 (B) 2
   (C) 3 (D) 1

3. Magnetic sensors also take advantage of the _____ point. — 1 | 1 | 2 | 1
   (A) Curie (B) Melting
   (C) Heating (D) Sublimation

4. The _____ configuration has only one "Zero" location for both data and memory. — 1 | 1 | 1 | 1
   (A) Von Neumann memory (B) Hardward memory
   (C) Memory (D) CPU

5. A _____ is one in which failure could produce a catastrophic result, example, failure of a fire alarm system or a pacemaker. — 1 | 1 | 2 | 1
   (A) Soft real-time system (B) Firm real – time system
   (C) Hard real – time system (D) Continuous system

6. The interrupt- request line is a part of the _____. — 1 | 1 | 2 | 1
   (A) Data line (B) Control line
   (C) Address line (D) Lacth

7. After the completion of the DMA transfer, the processor is notified by _____. — 1 | 1 | 2 | 1
   (A) Acknowledge signal (B) Interrupt signal
   (C) Data signal (D) Address signal

8. Programmable system on chip (SOC) devices are — 1 | 1 | 2 | 1
   (A) Dynamically configurable (B) Not configurable
   (C) Not reprogrammable (D) Not dynamically configurable

9. The time required for an input data to settle _____ the triggering edge of clock is known as 'Setup time'. 1 1 2 1
   (A) Before (B) During
   (C) After (D) Between

10. The maximum data transfer supported by USB3.0 and USB3.1 standards are respectively. 1 1 2 1
   (A) 5 MBits/ sec and 10 MBits/sec (B) 5 GBits/ sec and 10 MBits/sec
   (C) 5 GBits/ sec and 10 GBits/sec (D) 1 MBits/ sec and 10 MBits/sec

11. The first step in design flow model to figure out what the product is required to do is _____. 1 1 3 1
   (A) Specification (B) Requirements
   (C) Design (D) Integration

12. All of the components are combined, and the functionality test performed in _____ stage of design process. 1 1 3 1
   (A) Specification (B) Requirements
   (C) Design (D) Integration

13. Xlinx refers to the function generators within the FPGA fabric as _____. 1 1 4 3
   (A) Look-Up-Tables (LUT) (B) Slice
   (C) Pulse width modulation (D) Universal development board

14. The virtex5 FPGA are built from _____ input LUTs. 1 1 4 2
   (A) 2 (B) 4
   (C) 6 (D) 8

15. FPGA is a type of 1 1 5 1
   (A) Single purpose processor (B) Application specific processor
   (C) Programmable logic devices (D) General purpose processor

16. The idea of _____ is the grouping of specific sets of instructions in an application. 1 1 5 3
   (A) Partitioning (B) Composition
   (C) Decomposition (D) Functioning

17. A monitor is a primitive type of a 1 1 3 2
   (A) Debugger (B) Simulator
   (C) Compiler (D) Assembler

18. _____ is used to interfacts bus master on one bus and a bus slave on the other. 1 1 58 2
   (A) Bridge (B) Network
   (C) Router (D) Node

19. One Time Programmable (OTP) devices are 1 1 5 4
   (A) Sram and fusible link (B) Fusible link and antifuse
   (C) Fusible link and flash (D) Fusible link and EPROM

20. A system program that combines separately compiled modules of a program into a form suitable for execution is called _____. 1 1 4 4
   (A) Assembler (B) Linking loader
   (C) Cross compiler (D) Debugger

21. _____ leads to concurrency. 1 1 5 4
   (A) Serialization (B) Parallelism
   (C) Serial processing (D) Distribution

22. The on-chip memory which is local to every multithreaded Single Instruction stream, Multiple Data stream (SIMD) processor is called. 1 1 6 1
   (A) Local memory (B) Global memory
   (C) Flash memory (D) Stack

23. The co-processors operate in _____ with a processor on the same buses and with the same instruction byte stream. 1 1 6 1
   (A) Parallel (B) Series
   (C) Bit stream (D) Sequence stream

24. A program segment chosen for parallel processing is known as 1 1 6 1
   (A) Grain (B) Cluster
   (C) Work station (D) Node

25. The go/done model is actually a _____. 1 1 6 4
   (A) Multithreaded model (B) Network on chip model
   (C) Single thread model (D) Coprocessor model

PART – B (5 × 10 = 50 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
26. a.	Explain in detail on different types of embedded sensors.	10	2	1	1
	(OR)				
b.	Explain the Embedded system performance with neat diagram.	10	2	1	1
27. a.	Explain 8051 Instruction set.	10	2	1	1
	(OR)				
b.	With neat diagram explain PSOC3 (PSCO – programmable system on chip) architecture.	10	2	2	3
28. a.	Explain the concept of configurable logic blocks used in Xilinx vritex 5 with a neat diagram.	10	2	4	3
	(OR)				
b.	Explain the different configuration modes of FPGA (FPGA – Field Programmable Gate Amay).	10	2	4	3
29. a.	Explain the two major concepts and measures in system design.	10	2	5	4
	(OR)				