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B.Tech DEGREE EXAMINATION, MAY 2024

Seventh Semester

18ECE205J - FPGA - BASED EMBEDDED SYSTEM DESIGN

(For the candidates admitted during the academic year 2018-2019 to 2021-2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)

Answer **all** Questions

		Marks	BL	CO
1.	A PLD employed systems of so-called _____ consisting of simple combinations of gates and a flipflop. (A) Macrocells (B) Microcells (C) Continuous (D) Discontinuous	1	1	1
2.	_____ sense current in a small plate as a result of the Lorentz force F = q(vxB) on electrons. (A) Hall effect sensors (B) Bias magnetic field sensors (C) Magneto-inductive sensors (D) Magnetic field sensors	1	1	1
3.	_____ is a device that can transfer data to/from the embedded system directly accessing the microcontroller's memory space. (A) Mode Device (B) Memory Device (C) Sensor Device (D) I/O Device	1	1	1
4.	_____ are devices that convert one or more physical parameters into digital or analog signals for processing and control applications (A) Sensor (B) Polling (C) FIFO (D) Looping	1	1	1
5.	Interrupts form an important part of _____ systems (A) Batch processing (B) Multitasking (C) Real-time processing (D) Multi-user	1	2	2
6.	The return address from the interrupt-service routine is stored on the _____ (A) System heap (B) Processor register (C) Processor stack (D) Memory	1	1	2
7.	Which interrupt is unmaskable? (A) RST 5.5 (B) RST 7.5 (C) TRAP (D) Both RST 5.5 and 7.5	1	1	2
8.	The DMA controller has _____ registers (A) 4 (B) 3 (C) 2 (D) 1	1	1	2
9.	The Virtex 5 combines four of these logic cells to create a _____ (A) Slice (B) CLB (C) LUT (D) UDB	1	1	3
10.	A _____ is considered the highest level of abstraction for the FPGA's configurable fabric (A) Slice (B) Look Up Table (C) Configurable Logic block (D) Universal Digital blocks	1	1	3

11.	The _____can support parallel data through the use of the serialize/ deserialize (SERDES) logic, which connects to the input/output blocks. (A) slice (B) UDB (C) Transceivers (D) PWM	1	2	3
12.	FPGA is a type of (A) Single purpose processor (B) Application specific processor (C) General purpose processor (D) Programmable logic device	1	1	4
13.	The bus with the highest bandwidth that connects the processor, memory controller, and remaining high-speed devices together is referred to as (A) Data Bus (B) System Bus (C) Peripheral bus (D) control bus	1	1	4
14.	DIMM is abbreviated as _____ (A) Data In Memory Management (B) Dual in-line memory module (C) Dual Internal Memory Module (D) Data in-out Memory Module	1	1	4
15.	Which of the following is not a Bootloader? (A) SILO (B) LILO (C) MIPS PROM (D) FIFO	1	1	4
16.	A _____is a high-level language translator that runs on one platform but produces executables for another platform. (A) Cross – Development (B) Cross- assembler (C) Cross-compiler (D) Cross- Linker	1	1	5
17.	Kahn process network supports the _____flow of data from a source to a final destination (A) Bidirectional (B) Unidirectional with feedback (C) Bidirectional with feedback (D) Unidirectional	1	1	5
18.	Which process is used to communicate about the affected state that is trapped? (A) Spin-lock (B) Coupling (C) Blocking (D) Marshaling	1	1	5
19.	The on-chip memory which is local to every multithreaded SIMD processor is called (A) Global Memory (B) Local Memory (C) Flash Memory (D) Stack	1	1	5
20.	_____ leads to concurrency. (A) Serialization (B) Parallelism (C) Serial processing (D) Distribution	1	1	5

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	List out some of the performance criteria and their impact on embedded systems	4	2	1
22.	Mention some of the sensors used for communication in embedded systems and its principles	4	2	1
23.	Explain the concept of interrupt priority	4	2	2
24.	Differentiate PLA, PAL, and PROM	4	4	3
25.	Write short notes on Configurable Logic Blocks	4	2	3
26.	List the popular boot loaders	4	4	4
27.	Write the use of Spin-Lock	4	2	5

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO

28.	(a) Explain in detail, the different types of sensors used in embedded system design	12	4	1
	(OR)			
	(b) Explain in detail, the fundamentals in programmable logic and mixed-signal design of an embedded systems			
29.	(a) Explain the various instruction sets available for 8051 architectures with PSoc3/5.	12	4	2
	(OR)			
	(b) What is the need for DMA in PSoc3/5? Mention the various transaction modes available for DMA.			
30.	(a) Explain the concept of Configurable logic blocks used in Xilinx Virtex5	12	2	3
	(OR)			
	(b) Explain the different configuration modes of FPGA			
31.	(a) Explain the two major concepts and measures in system design.	12	2	4
	(OR)			
	(b) What is the analytical solution to partitioning? Explain			
32.	(a) Explain the different levels of parallelism	12	2	5
	(OR)			
	(b) Explain in detail how the affected state and trapped state concepts are used in state transfer.			

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