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B.Tech DEGREE EXAMINATION, NOVEMBER 2023

Seventh Semester

18ECC411J - FPGA BASED EMBEDDED SYSTEMS

(For the candidates admitted during the academic year 2020 - 2021 & 2021 - 2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)

Answer **all** Questions

		Marks	BL	CO
1.	Which among the following is not a type of Embedded System (A) EDM (B) CTM (C) DTM (D) FDM	1	1	1
2.	Failure of ATM machine is an example of _____Real Time System. (A) SRTS (B) HRTS (C) FRTS (D) ORTS	1	1	1
3.	Read/ Write operation of which memory has static and dynamic types (A) ROM (B) RAM (C) EPROM (D) FLASH	1	1	1
4.	the formula for BER= (A) No.of altered bits/ No of bits transmitted (B) No.of bits/ No of bits transmitted (C) No.of transmitted bits/ No of altered bits (D) bits/sec	1	1	1
5.	In PSoC, an 8-bit DAC can be configured for how many bit operations? (A) 12 (B) 8 (C) 16 (D) 32	1	1	2
6.	What is the purpose of address 0x00 0000 - 0x00 1FFF. (A) CAN (B) SRAM (C) I2C (D) ADC	1	1	2
7.	clk_usb is used for _____clock (A) IMO (B) PLL (C) USB (D) ILO	1	1	2
8.	What is the frequency of the crystal oscillator? (A) 36 MHz (B) 38 MHz (C) 34 MHz (D) 33 MHz	1	1	2
9.	Which is the intermediate step in the design life cycle (a) Specification (b) Design (c) Integration (d) Requirements (A) Specification (B) Design (C) Integration (D) Requirements	1	1	3
10.	Which among the following is not a measure of performance/success (A) Energy (B) Total Energy (C) Speed (D) Cost	1	1	3

11.	Assign statement is used in which type of Verilog program modeling? (a) switch-level (b) Behavioral (c) Structural (d) Data-flow (A) Switch -Level (B) Behavioral (C) Structural (D) Data-Flow	1	1	3
12.	Number of LUT's in Virtex-5 FPGA is____ (A) 6 (B) 5 (C) 4 (D) 7	1	1	3
13.	The term_____ refers to the ability to fix problems that arise from an unspecified behavior of the circuit. (A) Verifiability (B) maintainability (C) repairability (D) evolvability	1	1	4
14.	_____is the task of looking an existing design and managing the groupings and hierarchy without changing its functionality. (A) Reform (B) Resilience (C) Regression testing (D) Refactoring	1	1	4
15.	Which bus is used to connect on-chip memory controller and URT (A) address bus (B) data bus (C) peripheral bus (D) Universal Bus	1	1	4
16.	Speedup is defined by (A) hardware/software (B) hardware speed/software utilization (C) hardware utilization/software speed (D) hardware speed/software speed	1	1	4
17.	Coarse-grain parallelism refers to _____sub-tasks (A) large (B) small (C) medium (D) very large	1	1	5
18.	Which among the following statement(s) is not true with respect to degree of parallelism (A) the number of concurrent operations (B) time-varying functions over an entire application (C) the average of time-varying function (D) time-varying function over functional operations	1	1	5
19.	_____design uses simple FSM to read input, drive the computation, and write the outputs. (A) time-invariant (B) Time- varying (C) asynchronous (D) synchronous	1	1	5
20.	Based on the access speed of a FPGA which among the following is having least priority (A) register (B) on-chip memory (C) Off-chip memory (D) Disk	1	1	5

PART - B (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	BL	CO
21.	What is the purpose of a DMA Controller detail with a neat sketch	4	1	1
22.	Discuss about magnetic sensor	4	1	1
23.	Explain about PSW of PSoC3.	4	1	2
24.	Write a Verilog code for full-adder	4	1	3
25.	What is cohesion and its merits	4	1	4
26.	Detail the bit-level parallelism	4	1	2

27.	Give the description of the following instructions a. JNZ rel b. NOP c. CLR C d. CPL C	4	1	3

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Explain with diagram a Micro-controller subsystem	12	1	1
	(OR)			
	(b) Write a note on 1. RS232 2. USB			
29.	(a) what is an interrupt and detail interrupt handling in PSoC5.	12	1	2
	(OR)			
	(b) Discuss IMO and PLL with a neat diagram.			
30.	(a) Discuss in detail the measure of success.	12	1	3
	(OR)			
	(b) Write a Verilog code for 4-bit Ripple Carry Adder along with a logic diagram and sub-modules.			
31.	(a) List the components of Platform FPGA.	12	1	4
	(OR)			
	(b) How computer cores are customized and assembled discuss the same with a neat diagram.			
32.	(a) Explain in detail about granularity and How to choose for your design.	12	1	5
	(OR)			
	(b) List the types of spatial organization and elaborate the same.			

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