b.i.	Define control word, control variables, microinstructions and microprogram.	4	3	4	2
ii.	What is the format of a microinstruction and explain its fields briefly with diagram.	4	3	4	2
25. a.	Write in detail about any two types of software parallelism.	8	3	5	2
b.	(OR) Explain about the cache coherence problem and give solutions for this problem.	8	3	5	2
	PART – C (1 × 15 = 15 Marks) Answer ANY ONE Questions	Marks	BL	CO	PO
26.	Explain the procedure of constructing a fast adder, carry look-ahead adder with its diagram.	15	3	3	2
27.	Explain floating point arithmetic addition / subtraction with its flow chart.	15	3	3	2

Reg. No.

B.Tech. DEGREE EXAMINATION, MAY 2023 Third Semester

Note:	(For the canal	aates aamittea jrom ine	e academic year 2022-2023 onwai	(us)			
(i) (ii)	Part - A should be ans over to hall invigilator a Part - B and Part - C	it the end of 40th minute	vithin first 40 minutes and OMR e. unswer booklet.	sheet shoul	d be	han	ded
Time: 3	Max. Marks: 75						
	PAR	$AT - A (20 \times 1 = 20)$	Marks)	Marks	BL	со	PO
		Answer ALL Question	ons				
1.	The binary equivalent	, 1	1	2	2		
	(A) 10010.1101		11010.0011				
	(C) 11110.1110	(D)	01110.0011				
2.	Find the hexadecimal	value for the decima	ıl number 264	1	1	2	2
	(A) 128		108				
	(C) 2A1	(D)	761				
3.	The 2's complement	1	2	2.	2		
	(A) 011010		100010				
	(C) 001010	` '	010011				
4.	Signed 2's compleme	nt of -16 in 8-bit rep	resentation is	1	2	2	2
	(A) 10111011		10001100				
	(C) 01110000		00110101				
5.	performs	the desired operation	ns on the input information.	1	2	2	1
	(A) Arithmetic and l		Input unit				
	(7) 0 4	_	_				

(C)	001010	(D) 010011				
4. Sig	ned 2's complement of -16	in 8-bit representation is	1	2	2	2
	10111011	(B) 10001100				
	01110000	(D) 00110101				
5.	performs the desir	ed operations on the input information.	1	2	2	1
	Arithmetic and logic unit					
(C)		(D) Control unit				
6	convert the inform	oy ¹	2	2	2	
use	r.					
(A)	Input unit	(B) ALU				
(C)	Output unit	(D) Memory unit				
7.	holds the instructi	ons that is currently being executed.	1	2	2	2
(A)	Program counter	(B) Instruction register				
(C)		(D) Memory address register				
8.	operations are r	1	2	2	2	
(A)		(B) Move			30	
(C)		(D) Halt				
9.	is a combination	ut. 1	2	3	2	
(A						
(C	'	(D) Decoder				

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C. Single bit recording D. Multiple bit recording D. Single bit recording D. C. Single bit recording D. C. Single bit recording D. Single bit	10.	(A) Bit pair recoding (B)	Binary pair recoding	1	2	3	2		20.		method is used to design the control unit of ARM processor. Hardwired (B) Microprogrammed	1	3	5	2
Cache Cach	11	(-)					_			(C) S	State machine (D) Combinational circuit				
Command Foundation Command	11.			1	2	3	2								
12. How many bits are needed to represent floating point number in a single of 2 s 2 s 2 specific form? (A) 16 (B) 32 complement on the unithmetic operations indicated and verify the complement of the program of B) Command (C) Micro program (B) Command (C) Micro program (B) System files (A) Application program (B) System files (B) Subming (B) Bubbling (B) Bubbling (C) NOP (B) System files (C) NOP count forwarding (B) Bubbling			_								$PART - B (5 \times 8 = 40 Marks)$	Marks	BL	CO	PO
Second control Seco		(C) Program counter (D)	Shift register								Answer ALL Questions	-			
C	12.		loating point number in a single	1	2	3	2		21. a.	The bi	pinary numbers listed have a sign in the leftmost position and if negative	8	2	1	1
C			22												
1															
13. A set of microinstructions for a single machine instruction is called 1 2 4 2 (iii) 111001 - 001010 (iv) 101011 - 100110 (iv) 1010110 (iv) 101010 (iv) 1010110 (iv) 1010110 (iv) 1010110 (iv) 1010110 (iv) 1010110 (iv) 101010 (iv) 1010110 (iv) 1010110 (iv) 1010110 (iv) 1010110 (iv) 101010 (iv) 1010110 (iv)		(C) 04 (D)	30												
(A) Application program (B) Command (C) System files (Ny 101011 - 100110 (Ny 101011 -	13	A set of microinstructions for a single	machine instruction is called	1	2	4	2								
(A) Application program (B) Command (C) Mirro program (D) System files 14. What approach is used to identify the data dependencies when dealing with 1	15.	11 bot of informstructions for a single	machine instruction is called	-	_	,	~			` ,	,				
Cook Micro program Di System files Di System files Di System files Di Di Di Di Di Di Di D		(A) Application program (B)	Command							(1V)) 101011 – 100110				
b. Draw the graphic symbol, algebraic function and truth table for the following solitowards solitowards and the solitowards solitowards (A) Operand forwarding (B) Bubbling (C) NOP (D) Wait signal (D) Wait											(OD)				
Next approach is used to identify the data dependencies when dealing with software;		(2)	System mes						h	Deoxy		8	2	1	1
Solitoware	14.	What approach is used to identify the data	dependencies when dealing with	1	3	4	2					0	22	1	1
(a) Operand forwarding (b) Bubbling (C) NOP (D) Wait signal (ii) OR (iii) NAND (iv) EX-OR 15. Branch instruction 'IUMP IF ZERO' is an example of 1 3 4 2 (iii) NAND (iv) EX-OR 16. Instruction instruction in pipeliming to increase the memory access speed. (A) Special memory is used in pipeliming to increase the memory access special memory locations (B) Special purpose register (C) Cache (D) Buffers (1												
(C) NOP (D) Wait signal 15. Branch instruction 'TIOMP IF ZERO'' is an example of (A) Transferring the control (B) Conditional branch (D) Arithmetic branch 16		(A) Operand forwarding (B)	Bubbling												
1. 1. 1. 1. 1. 1. 1. 1.		(C) NOP (D)	Wait signal												
15. Branch instruction **IUMP** IF ZFRO** is an example of (A) Transferring the control (B) Conditional branch (C) Unconditional branch (D) Arithmetic bra										·					
(C) Unconditional branch (D) Arithmetic branch (D) Buffers (D) Buffe	15.			1	3	4	2			()					
ii. Write about the operational concepts of the following instructions. A Special memory locations (B) Special purpose register (C) Cache (D) Buffers								22	2. a.i.	Define	e instructions and data.	2	1	2	1
speed. (A) Special memory locations (B) Special purpose register (D) Buffers (C) Cache (D) Buffers (A) Processor (B) Memory (C) Control (D) Data (B) Task level parallelism (C) Instruction level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (C) Instruction and multiple data values is called (A) Single instruction would operate or execute on multiple data stream (C) Multiple instruction and multiple data stream (C) Multiple instruction and single data stream (C) Multiple		(C) Unconditional branch (D)	Arithmetic branch							7)					
speed. (A) Special memory locations (B) Special purpose register (C) Cache (D) Buffers 17. In parallelism the computer architecture has multiple nodes, multiple CPUs and multiple threads. (A) Processor (B) Memory (C) Control (D) Data 18. is a measure of how many operations can be performed in parallel at the same time. (A) Data parallelism (B) Task level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (C) Instruction and multiple (B) Single instruction and single data stream (C) Multiple instruction and single data stream (E) Multiple instruction and single data stream (E) Multiple instruction struction struction struction struction struction structions (E) Data transfer instructions (E) Data transfer instruction	16			1	2	4	2		ii.	Write	about the operational concepts of the following instructions.	6	1	2	1
(A) Special memory locations (B) Special purpose register (C) Cache (D) Buffers 7. In	10.		to increase the memory access	1	3	4	2			(i)		12			
(C) Cache (D) Buffers (III) Store (R) Store (Charial symmons assistes												
17. Inparallelism the computer architecture has multiple nodes, multiple CPUs and multiple threads. (A) Processor (B) Memory										(111)) Store R ₄ , LOC				
multiple CPUs and multiple threads. (A) Processor (B) Memory (C) Control (D) Data 18		(b)	Buriers								(OR)				
multiple CPUs and multiple threads. (A) Processor (B) Memory (C) Control (D) Data 18	17.	In parallelism the computer	architecture has multiple nodes	1	3	5	2		hi	A com	` ,	2	3	2	1
(A) Processor (B) Memory (C) Control (D) Data ii. Write about the following instruction types with an example. 6 2 2 2 1 8		multiple CPUs and multiple threads.										~	5	2	1
18 is a measure of how many operations can be performed in parallel at the same time. (A) Data parallelism (B) Task level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (D) Transaction level parallelism (D) Transaction and single data values is called (A) Single instruction and multiple (B) Single instruction and single data stream (C) Multiple instruction and single data stream (D) Multiple instruction and multiple data stream (D) Multiple data stre			Memory							arry sir	ingle byte in memory:				
is a measure of how many operations can be performed in parallel at the same time. (A) Data parallelism (B) Task level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (D) Transaction level parallelism (E) Tope of computer where a single instruction would operate or execute on multiple data values is called (A) Single instruction and multiple (B) Single instruction and single data stream (C) Multiple instruction and single data stream (D) Multiple instruction and single data stream (E) Multiple instructions (Iii) Data transfer instructions (Iiii) Data manipulation instructions (Iiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii		(C) Control (D)	Data						ii.	Write :	about the following instruction types with an example	6	2	2	1
18 is a measure of how many operations can be performed in parallel at the same time. (A) Data parallelism (B) Task level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (C) Instruction and multiple data values is called (A) Single instruction and multiple (B) Single instruction and single data stream (C) Multiple instruction and single data stream (C) Multiple instruction and single data stream (D) Multiple data stream (D) Multiple data stream (D) Multiple instruction and multiple data stream (C) Multiple instruction and single data stream (D) Multiple data stream (D) Multiple data stream (E) Multiple instruction and single data stream (D) Multiple instruction and multiple data stream (E) Multiple instruction and single data stream (E) Multiple instruction structions (iii) Data manipulation instructions (iiii) Arithmetic instructions (iii) Arithmetic instru															
parallel at the same time. (A) Data parallelism (B) Task level parallelism (C) Instruction level parallelism (D) Transaction level parallelism (E) Task level parallelism (D) Transaction level parallelism (E) Transaction level parallelism (D) Transaction level parallelism (E) Transaction level parallelism (E) Transaction level parallelism (D) Transaction level parallelism (E) Transaction leve	18.		operations can be performed in	1	3	5	2								
(C) Instruction level parallelism (D) Transaction level parallelism 23. a. Write about the 4-bit binary parallel adder/subtractor with its diagram. 8 3 3 2 19. Type of computer where a single instruction would operate or execute on multiple data values is called		2								` '					
19. Type of computer where a single instruction would operate or execute on multiple data values is called			-												
multiple data values is called		(C) Instruction level parallelism (D)	Transaction level parallelism					2	23. a.	Write	about the 4-bit binary parallel adder/subtractor with its diagram.	8	3	3	2
multiple data values is called	10	Type of computer whom a single instanct		1	2	_	2								
(A) Single instruction and multiple (B) data stream (C) Multiple instruction and single data stream (A) Single instruction and single data stream (B) Single instruction and single data stream (C) Multiple instruction and single (D) Multiple instruction and multiple data stream (B) Single instruction and single data stream (B) Multiply (+13)×(-6) by using bit pair recoding method. (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and single data stream (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and single data stream (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and single data stream (B) Single instruction and single data stream (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and single data stream (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and single data stream (B) Single instruction and single data stream (C) Multiply (+13)×(-6) by using bit pair recoding method. (B) Single instruction and	19.		on would operate or execute on	1	3	3	2								
data stream (C) Multiple instruction and single (D) Multiple instruction and data stream ii. Multiply (+13)×(-6) by using bit pair recoding method. 5 3 3 2 24. a. What are the control signals generated by control unit to execute (i) Add (R ₃), R ₁ (ii) Unconditional branching			Single instruction and single						b.i.	What a	are the advantages of bit pair recoding of multipliers?	3	2	3	2
(C) Multiple instruction and single (D) Multiple instruction and data stream multiple data stream 24. a. What are the control signals generated by control unit to execute (i) Add (R ₃), R ₁ (ii) Unconditional branching		•	_									_	2	2	
data stream multiple data stream 24. a. What are the control signals generated by control unit to execute (i) Add (R ₃), R ₁ (ii) Unconditional branching									11.	Multıp	ply $(+13)\times(-6)$ by using bit pair recoding method.	3	5	3	2
(i) Add (R ₃), R ₁ (ii) Unconditional branching		_	~	-				,	24 -	117L-4	one the control cionals conserved 11	0	2	Λ	า
(ii) Unconditional branching			T					4	44. d.			o	J	4	4
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