| Reg. No | | | | | | | | | | | | | | | |
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# B.Tech DEGREE EXAMINATION, DECEMBER 2023

Third & Fifth Semester

## 18CSC203J - COMPUTER ORGANIZATION AND ARCHITECTURE

*(For the candidates admitted during the academic year (2020-2021 & 2021-20222))*

**Note:**

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
ii. **Part - B** and **Part - C** should be answered in answer booklet.

**Time: 3 Hours** **Max. Marks: 100**

**PART - A (20 × 1 = 20 Marks)**
Answer **all** Questions

| | | Marks | BL | CO |
|---|---|---|---|---|
| 1. | A source program is usually in _____<br>(A) Assembly language (B) Machine level language<br>(C) High-level language (D) Natural language | 1 | 1 | 1 |
| 2. | The ALU makes use of _____ to store the intermediate results.<br>(A) Accumulators (B) Registers<br>(C) Heap (D) Stack | 1 | 1 | 1 |
| 3. | To reduce the memory access time we generally make use of _____<br>(A) Heaps (B) Higher capacity RAM's<br>(C) SDRAM's (D) Cache's | 1 | 1 | 1 |
| 4. | Which unit is used to measure the CPU's processing power?<br>(A) GIPS (B) LIPS<br>(C) MIPS (D) Nanoseconds | 1 | 2 | 1 |
| 5. | When we perform subtraction on -7 and 1 the answer in 2's compliment form is _____.<br>(A) 1010 (B) 1110<br>(C) 0110 (D) 1000 | 1 | 3 | 2 |
| 6. | The processor keeps track of the results of its operations using a flags called _____.<br>(A) Conditional code flags (B) Test output flags<br>(C) Type flags (D) Status flags | 1 | 1 | 2 |
| 7. | The most efficient method followed by computers to multiply two unsigned numbers is _____.<br>(A) Booth algorithm (B) Bit pair recording of multipliers<br>(C) Restoring algorithm (D) Non restoring algorithm | 1 | 1 | 2 |
| 8. | For the addition of large integers most of the systems make use of _____.<br>(A) Fast adders (B) Full adders<br>(C) Carry look-ahead adders (D) Ripple adder | 1 | 1 | 2 |
| 9. | What does the end instruction do?<br>(A) It ends the generation of a signal (B) It ends the complete generation process<br>(C) It starts a new instruction fetch cycle and resets the counter (D) It is used to shift the control to the processor | 1 | 1 | 2 |
| 10. | The disadvantage/s of the hardwired approach is _____.<br>(A) It is less flexible (B) It cannot be used for complex instructions<br>(C) It is costly (D) less flexible & cannot be used for complex instructions | 1 | 1 | 3 |

11. The contention for the usage of a hardware device is called _____. 1 1
(A) Structural hazard (B) Stalk
(C) Deadlock (D) Data Hazard

12. Each stage in pipelining should be completed within _____ cycle. 1 1
(A) 1 (B) 2
(C) 3 (D) 4

13. The average number of steps taken to execute the set of instructions can be made to be less than one by following _____. 1 1 4
(A) ISA (B) Pipe-lining
(C) Super-scaling (D) Sequential

14. The cost of a parallel processing is primarily determined by : 1 1 4
(A) time complexity (B) switching complexity
(C) circuit complexity (D) Space complexity

15. The ultimate goal of a compiler is to, 1 1 4
(A) Reduce the clock cycles for a programming task. (B) Reduce the size of the object code.
(C) be versatile. (D) be able to detect even the smallest of errors.

16. In a system with a 16 bit address bus, what is the maximum number of 1K byte memory devices it could contain 1 1 4
(A) 16 (B) 64
(C) 256 (D) 65536

17. The main purpose of having memory hierarchy is to _____ 1 1 5
(A) Reduce access time (B) Provide large capacity
(C) Reduce propagation time (D) Reduce access time & Provide large capacity

18. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster. 1 1 5
(A) A (B) B
(C) Both take the same time (D) Insufficient information

19. The counter that keeps track of how many times a block is most likely used is _____ 1 1 5
(A) Count (B) Reference counter
(C) Use counter (D) Probable counter

20. An effective way to introduce parallelism in memory access is by _____ 1 1 5
(A) Memory interleaving (B) TLB
(C) Pages (D) ILP

**PART - B (5 × 4 = 20 Marks)** Marks BL CO
Answer **any 5** Questions

21. Breakdown the connections between processor and memory with a neat sketch and explain. 4 4 1

22. Illustrate the method of storing multi-byte data types with an example. 4 2 1

23. Perform multiplication of 110*111 using shift add multiply method 4 3 2

24. Explain the process of instruction execution for the following instruction Mov R1,R2 4 4

25. Justify why instruction level parallelism is limited in practice. 4 5

| | | Marks | BL | CO |
|---|---|---|---|---|
| 26. | Explain the cause of the cache coherence problem in multi-core CPUs and offer a solution. | 4 | 5 | 4 |
| 27. | Name the structure of bistable latch made from cross-coupled inverters and access transistors. Describe its advantages and applications. | 4 | 4 | 5 |

**PART - C (5 × 12 = 60 Marks)**

Answer **all** Questions

| | | Marks | BL | CO |
|---|---|---|---|---|
| 28. | (a) Relate the various functional units of a computer and explain their significance with a neat sketch. | 12 | 3 | 1 |
| | **(OR)** | | | |
| | (b) Explain the following arithmetic function f=(L1*L2)/2+(L3/L5) in different instruction formats. | | | |
| 29. | (a) Compare and contrast the ripple carry adder with carry look ahead adder. Draw the logic circuit to perform sum of 1111+1011 using carry look ahead adder. | 12 | 4 | 2 |
| | **(OR)** | | | |
| | (b) Perform division of 1000/0011 using non-restoring division algorithm. | | | |
| 30. | (a) In the context of pipelining what is meant by a 'task'? Consider a four segment pipeline, draw the in-space time domain diagram for this pipeline, and derive a formula for speed-up. For a 4 stage pipeline, the time to perform a suboperation in each segment is 20ns for 100 tasks. What is speed-up ratio? | 12 | 5 | 3 |
| | **(OR)** | | | |
| | (b) Identify the types of hazards in pipelined architecture. Explain every type using an appropriate example. | | | |
| 31. | (a) Compare relative advantages of SIMD and MIMD architectures. Among SIMD and MIMD computers which one would be easier to program Justify. | 12 | 5 | 4 |
| | **(OR)** | | | |
| | (b) With help of schematic diagram, determine how associative memory can be realized in a computer architecture. | | | |
| 32. | (a) Relate the different methods of asynchronous data transfer ? Explain in detail. | 12 | 4 | 5 |
| | **(OR)** | | | |
| | (b) Examine the Virtual address mapping into physical address ? Explain the different methods of writing data into cache memory ? | | | |

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