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B.Tech DEGREE EXAMINATION, JUNE 2024

Third & Fifth Semester

18CSC203J - COMPUTER ORGANIZATION AND ARCHITECTURE

(For the candidates admitted during the academic year 2018-2019 to 2021-2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks) — Answer **all** Questions

		Marks	BL	CO
1.	The program counter is used to store the ___ instruction address to be executed. (A) Next (B) Previous (C) Last (D) Present	1	1	1
2.	The condition flag C is set to 1 to indicate _____ (A) There is no empty register available (B) The result does not have carry output (C) The result has a carry output (D) The operation has resulted in an error	1	2	1
3.	Which of the following contains circuitry to carry out operations such as addition, multiplication, etc? (A) Arithmetic and logic unit (B) Input / Output unit (C) Memory unit (D) Control unit	1	1	1
4.	The addressing mode/s, which uses the PC instead of a general-purpose register is _____. (A) Indirect (B) Direct (C) Relative (D) Indexed with offset	1	2	1
5.	The data 451Ah is to be represented in a byte addressable memory system starting from location 2000h using little endian format. The memory locations 2000h, 2001h are _____. (A) 54h, and A1h respectively (B) A1h, and 54h respectively (C) 1Ah, and 45h respectively (D) 45h, and 1Ah respectively	1	3	1
6.	Subtracting -5 and -2 using 2'complement method gives (A) 11001 (B) 1011 (C) 1101 (D) 1001	1	3	2
7.	Consider multiplication of two-bit numbers B1B0 and A1A0. The number of AND gates required in the circuit while implementing the design in paper pencil method are (A) 5 (B) 10 (C) 8 (D) 4	1	3	2
8.	In shift and add multiplication, consider Accumulator = 0000, Multiplier (Q) = 1100, and Multiplicand (B) = 1001. The shift right A to Q operation changes the Q as (A) 0110 (B) 1111 (C) 1100 (D) 0000	1	3	2
9.	Number of Half-adders required in the design of 2-bit ripple carry adder is (A) 4 (B) 6 (C) 2 (D) 8	1	1	2

10. In Ripple carry adder, each adder has to wait for the carry from the previous stage; this leads to — 1 2 2

(A) Low power consumption of adder (B) decreased propagation delay
(C) Increased propagation delay (D) High speed of the ripple adder

11. The two phases of executing an instruction are _____ — 1 1 3

(A) Instruction decoding and storage (B) Instruction fetch and Instruction processing
(C) Instruction execution and storage (D) Instruction fetch and instruction execution

12. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____. — 1 2 3

(A) Branch target (B) Jump instruction
(C) Forward target (D) Loop target

13. In micro-programmed approach, the signals are generated by _____. — 1 2 3

(A) Utility tools (B) Assembly language
(C) Machine instructions (D) System programs

14. _____ are the different type/s of generating control signals. — 1 1 4

(A) Micro-programmed (B) Both Micro-programmed and Hardwired
(C) Micro-instruction (D) Hardwired

15. The disadvantages of the hardwired approach is _____ — 1 1 4

(A) It is less flexible (B) less flexible & cannot be used for complex instructions
(C) It is costly (D) It cannot be used for complex instructions

16. _____ taxonomy distinguishes multi-processor computer architecture according to instruction and data stream. — 1 2 4

(A) Reader-writer classification (B) Banker's classification
(C) Philosopher's classification (D) Flynn's classification

17. SIMD represents an organization that — 1 1 5

(A) Refer to a system capable of processing single program at a same time (B) Includes many processing units under the supervision of common control unit
(C) Represents organization of single computer containing a control unit, and processor unit (D) A computer system that is capable of processing several programs at a same time

18. The access time of static RAM's are in the range of few — 1 2 5

(A) Seconds (B) Milli seconds
(C) Pico seconds (D) Nano seconds

19. The latency that measures the time taken to transfer a word or data to or from the memory is _____. — 1 2 5

(A) Data delay (B) Clock period
(C) Memory latency (D) Memory bandwidth

20. MFC is used to — 1 1 6

(A) Assign a device to perform the read operation (B) Signal the processor the memory operation is complete
(C) Signal to the device that the memory read operation is complete (D) Issue a read signal

PART - B (5 × 4 = 20 Marks) — Marks BL CO

Answer **any 5** Questions

21.	What is the role of a control unit in the execution of an instruction?	4	2	1
22.	Compute A=010111 B=101100 using fast multiplication	4	3	2
23.	Differentiate the performance of various hazards.	4	2	3
24.	List the applications of parallelism.	4	1	4
25.	Explain the significance of replacement algorithm in Cache Management System.	4	2	5
26.	Sketch the Uniform Memory Access (UMA). Also mention its use.	4	1	6
27.	Explain about the role of cache memory in pipelining	4	2	3

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Relate the various functional units of a computer and explain their significance with a neat sketch	12	2	1
	(OR)			
	(b) Explain about the bus structures in computer organization along with the diagram			
29.	(a) Compute multiplication of positive numbers for given numbers 1. B=1101 and Q=1011 (6 Mark) 2. B=0101 and Q=0100 (6 Mark)	12	3	2
	(OR)			
	(b) 1. Explain in detail about the floating point numbers and its operation (6 mark) 2. Convert the decimal number (-0.75) to single and double precision for floating point representation. (6 Mark)			
30.	(a) Explain about the execution of complete instruction with neat diagram	12	1	3
	(OR)			
	(b) Explain in detail about the multiple bus organization and a complete processor			
31.	(a) What is parallelism? What are the types of parallelism? Explain them in detail with neat diagram.	12	2	4
	(OR)			
	(b) Explain in detail about the Flynn's Classification along with its category.			
32.	(a) Explain in detail about the Internal Organization of Memory Chips with neat diagram	12	2	5
	(OR)			
	(b) Explain in detail about the Read only memory and cache memory			

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