Reg. No.														

MINOR CERTIFICATION EXAMINATION, JUNE 2023

Second & Third Semester

18CSC003J – COMPUTER ORGANIZATION AND ARCHITECTURE

(For the candidates admitted during the academic year 2021-2022 & 2022-2023)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)

Answer **ALL** Questions

	Marks	BL	CO	PO
1. A source program is usually in _____. (A) Assembly language (B) Machine level language (C) High level language (D) Natural language	1	1	1	1
2. _____ structure is usually used to connect 1/0 devices. (A) Single bus (B) Multiple bus (C) Star bus (D) Ram bus	1	1	1	1
3. The decoded instruction is stored in _____. (A) IR (B) PC (C) Registers (D) MDR	1	1	1	1
4. ISP stands for (A) Information standard processing (B) Instruction set processor (C) Interchange standard protocol (D) Interrupt service procedure	1	1	1	1
5. Convert binary to decimal $(11000)_2$ (A) $(45)_{10}$ (B) $(24)_{10}$ (C) $(25)_{10}$ (D) $(42)_{10}$	1	1	2	1
6. For the addition of large integers, most of the systems make use of (A) Fast address (B) Full address (C) Carry-look ahead address (D) Parallel address	1	1	2	1
7. When we perform subtraction on –7 and 1, the answer in 2's complement form is _____. (A) 1010 (B) 1110 (C) 0110 (D) 1000	1	1	2	1
8. Which methods of representation of numbers occupies large amount of memory than others? (A) Sign-magnitude (B) 1's compliment (C) 2's compliment (D) 10's compliment	1	1	2	1

9. In a three bus architecture, how many input and output ports are there? 1 1 3 1
   (A) 2 output and 2 input (B) 1 output and 2 input
   (C) 2 output and 1 input (D) 1 output and 1 input

10. The method used for restoring data dependency conflict by the compiler itself is 1 1 3 1
   (A) Delayed load (B) Operand forwarding
   (C) Prefect target instruction (D) Loop buffer

11. Microinstructions are stored in control memory groups, with each group specifying a 1 1 3 1
   (A) Routine (B) Subroutine
   (C) Vector (D) Address

12. Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU, we can say that 1 1 3 1
   (A) $T_1 <= T_2$ (B) $T_1 >= T_2$
   (C) $T_1 < T_2$ (D) T_1 and T_2 plus time taken for are instruction fetch cycle

13. Which one of the following is not a Flynn's classification? 1 2 4 1
   (A) MISD (B) SISD
   (C) MIMD (D) SMID

14. _____ multithreading switches threads only on costly stalls, such as last-level cache miss. 1 2 4 1
   (A) Coarse grained (B) Fine grained
   (C) Course grained (D) Tune grained

15. I = i + 1; 1 1 4 1
   J = i + 1;
   The above is example sequence logic of
   (A) Write After Write (WAW) (B) Write After Read (WAR)
   (C) Read After Write (RAW) (D) Read After Read (RAR)

16. The objective of S/W and H/W techniques, is to exploit 1 1 4 1
   (A) Parallelism (B) Scalability
   (C) Supervision (D) Computability

17. PCI stands for 1 1 4 1
   (A) Peripheral component interconnect (B) Peripheral computer internet
   (C) Processor computer interconnect (D) Processor cable interconnect

18. The device connected to USB is assigned an _____ address. 1 1 5 1
   (A) 9 bit (B) 16 bit
   (C) 4 bit (D) 7 bit

19. Once the bus is granted to a device it _____. 1 2 5 1
   (A) Activates the bus busy line (B) Performs the required operation
   (C) Raises an interrupt (D) Activates the ready line

20. In a program using subroutine call instruction, it is necessary to 1 1 5 1
   (A) Initialize program counter (B) Clear the accumulator
   (C) Reset the microprocessor (D) Clear the instruction register

PART – B (5 × 4 = 20 Marks) Marks BL CO PO
Answer **ANY FIVE** Questions

21. What are the four types of instruction set architecture you are aware of? 4 2 1 1

22. Sketch Big-Endian and Little-Endian assignment. 4 2 1 1

23. Write down the steps used for restoring and non restoring division. 4 2 2 1

24. Elaborate the different techniques for micro instruction sequencing. 4 2 3 1

25. Elaborate on branch prediction with example. 4 2 3 1

26. Elaborate on software parallelism and its types. 4 2 4 1

27. Write short notes on DMA data transfer. 4 3 5 1

PART – C (5 × 12 = 60 Marks) Marks BL CO PO
Answer **ALL** Questions

28. a. List and explain various addressing modes, with its formats and example. 12 3 1 1

(OR)

b. Outline on instruction formats with suitable examples. 12 3 1 1

29. a. Write Booth's algorithm and perform Booth multiplication of –23×–19. 12 3 2 1

(OR)

b. Write restoring division algorithm and perform restoring division of 10/3. 12 3 2 1

30. a. List and explain the steps involved in execution of complete instruction. 12 3 3 1

(OR)

b. Describe the generation of control signals using hardwire control unit, with necessary diagrams. 12 3 3 1

31. a. Explain Flynn's classification and the four architecture in detail. 12 3 4 1

(OR)

b. Discuss in detail the cache coherence problem and the protocol that is used to overcome cache coherence. 12 3 5 1

32. a. Discuss about various mapping schemes used in cache design. 12 3 5 1

(OR)

b.i. Differentiate memory mapped I/O and I/O mapped I/O. 6 3 5 1

ii. Write a note on DMA transfer. 6 3 5 1

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