Reg. No.															

B.Tech. DEGREE EXAMINATION, DECEMBER 2023

Third Semester

18CSC262J – COMPUTER ORGANIZATION AND ARCHITECTURE

(For the candidates admitted during the academic year 2018-2019 to 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks) Marks BL CO

Answer **ALL** Questions

1. The decoded instruction is stored in _____. 1 1 1
   (A) IR (B) PC
   (C) Registers (D) MDR

2. ISP stands for _____. 1 1 1
   (A) Instruction Set Processor (B) Information Standard Processing
   (C) Interchange Standard Protocol (D) Interrupt Service Procedure

3. The internal components of the processors are connected by _____. 1 1 1
   (A) Processors intra-connectivity circuity (B) Processor bus
   (C) Memory bus (D) RAM bus

4. Which circuits are used to implement logic operations? 1 1 1
   (A) Combinatorial (B) Bridge
   (C) Logical (D) Gate

5. The final result of sum of the numbers, 0110 and 0110 is _____. 1 2 2
   (A) 1100 (B) 1111
   (C) 1001 (D) 1010

6. _____ is used to implement the sum circuit using full adder. 1 2 2
   (A) AND and OR gate (B) NAND gate
   (C) XOR gate (D) XNOR

7. _____ is a name called for a decimal number when it is placed to the right of the first significant digit. 1 2 2
   (A) Orthogonal (B) De-normalized
   (C) Determinate (D) Normalized

8. _____ is a sign included after a string of digits. 1 1 2
   (A) Significant (B) Mantissa
   (C) Determinant (D) Exponent

9. The contents of the EPROM are erased by _____. 1 1 3
   (A) Overcharging the chip (B) Exposing the chip to UV rays
   (C) Exposing the chip to IR rays (D) Discharging the chip

10. The register AX is formed by grouping 1 1 3
   (A) AH and AL (B) BH and BL
   (C) CH and CL (D) DH and DL

11. The time taken to transfer a word of data to or from the memory is called as _____. 1 1 3
   (A) Access time (B) Cycle time
   (C) Memory latency (D) Recovery time

12. Which microinstruction provide next instruction from control memory 1 1 3
   (A) Microinstruction execution (B) Microinstruction buffer
   (C) Microinstruction decoder (D) Microinstruction sequencing

13. The objective of S/W and H/W techniques, is to explain, _____. 1 1 4
   (A) Parallelism (B) Scalability
   (C) Supervision (D) Compatibility

14. After the completion of the DMA transfer, the processor is notified by ____. 1 2 4
   (A) Acknowledge signal (B) Interrupt signal
   (C) WMFC signal (D) Control signal

15. The ionic feature of the RISC machine among the following is _____. 1 2 4
   (A) Reduced number of addressing modes (B) Increased memory size
   (C) Having a branch delay slot (D) Indexing registers

16. In CISC architecture most of the complex instructions are stored in _____. 1 1 4
   (A) Register (B) Diodes
   (C) CMOS (D) Transistors

17. The average time required to reach a storage location in memory and obtain its contents is called _____. 1 2 5
   (A) Latency time (B) Access time
   (C) Turnaround time (D) Response time

18. A plug and play storage device that simply plugs in the port of a computer is _____. 1 1 5
   (A) Flash drive (B) Compact disk
   (C) Hard disk (D) CD

19. The number of failed attempts to access memory, stated in the form of a fraction is called as _____. 1 1 5
   (A) Hit rate (B) Miss rate
   (C) Failure rate (D) Delay

		Marks	BL	CO
20.	The disk's surface is divided into a number of invisible concentric circles called (A) Drives (B) Tracks (C) Slits (D) References	1	1	5

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

		Marks	BL	CO
21.	Construct and explain Half Adder with an example.	4	2	1
22.	Discuss about Integer Representation with example.	4	2	2
23.	With example discuss any two assemblers.	4	1	3
24.	Write about PCI bus.	4	2	4
25.	Illustrate virtual memory along with neat diagram.	4	2	3
26.	Discuss about various types of flip-flops.	4	2	2
27.	Examine the concept of address translation.	4	2	5

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

		Marks	BL	CO
28. a.	Define addressing and list out the various types of addressing modes with examples.	12	2	1
	(OR)			
b.	Discuss in detail about Flip flops and its types.	12	2	1
29. a.	Discuss Booth's algorithm for multiplication with an example.	12	3	2
	(OR)			
b.	Explain the restoring division with suitable example.	12	3	2
30. a.	Summarize about microprogrammed control unit in detail.	12	3	3
	(OR)			
b.	Define and describe about ROM, PROM, EPROM.	12	3	3
31. a.	Discuss about various roles in interrupts in processor.	12	2	4
	(OR)			
b.	Differentiate RISC architecture from CISC architecture.	12	2	4
32. a.	Explain how the three different types of mapping techniques are operating in cache memory.	12	2	5
	(OR)			
b.	List out and explain about Secondary Storage devices.	12	2	5

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