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B.Tech DEGREE EXAMINATION, NOVEMBER 2023

Third Semester

18AIS202T - DIGITAL LOGIC AND COMPUTER ARCHITECTURE

(For the candidates admitted during the academic year 2020 - 2021 & 2021 - 2022)

Note:

i. **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

ii. **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours **Max. Marks: 100**

PART - A (20 × 1 = 20 Marks)

Answer **all** Questions

		Marks	BL	CO
1.	What is the value of the binary number 1101 in decimal? (A) 12 (B) 13 (C) 14 (D) 15	1	1	1
2.	What is the hexadecimal representation of the binary number 101110? (A) 5A (B) 9E (C) BA (D) 2E	1	1	1
3.	Convert the decimal number 49 to binary. (A) 110001 (B) 111001 (C) 100111 (D) 101001	1	1	1
4.	In sign-magnitude addition, if the signs of the numbers being added are the same, what operation is performed on their magnitudes? (A) Addition (B) Subtraction (C) Multiplication (D) Division	1	1	1
5.	What is the Boolean expression for the AND operation? (A) A + B (B) A * B (C) A / B (D) A - B	1	1	2
6.	What is a Karnaugh Map used for in digital logic? (A) Multiplication of Boolean expressions (B) Simplification of Boolean expressions (C) Division of Boolean expressions (D) Addition of Boolean expressions	1	1	2
7.	What is the function of a 2-to-1 multiplexer? (A) Combines two input lines into a single output line (B) Combines four input lines into a single output line (C) Expands a single input line into two output lines (D) Expands a single input line into four output lines	1	1	2
8.	Which gate is commonly used in the implementation of a decoder? (A) AND (B) OR (C) XOR (D) NAND	1	1	2
9.	What is a bus in computer architecture? (A) A vehicle that carries data and instructions in a computer (B) A high-speed connection that allows data to be transferred between components (C) A type of CPU used in modern computers (D) A storage device	1	1	3

10.	Which of the following instructions is typically used to change the flow of control in a program? (A) ADD (B) MOV (C) JMP (D) XOR	1	1	3
11.	Which addressing mode is used when you need to access an element of an array or structure with an offset? (A) Immediate (B) Indirect (C) Register (D) Indexed	1	1	3
12.	Which type of register is used to store the result of a computation, such as the sum of two numbers? (A) Program Counter (PC) (B) Instruction Register (IR) (C) Accumulator (ACC) (D) Memory Address Register (MAR)	1	1	3
13.	What is a non-maskable interrupt (NMI)? (A) An interrupt that cannot be ignored or disabled by the CPU (B) An interrupt generated by software (C) An interrupt that is masked by default (D) An interrupt caused by arithmetic errors	1	1	4
14.	Which of the following is an advantage of using DMA for data transfer in comparison to programmed I/O? (A) DMA is more cost-effective. (B) DMA reduces the CPU's involvement in data transfer. (C) DMA provides higher data transfer rates. (D) DMA is easier to implement in software.	1	1	4
15.	Which of the following types of memory is typically used to store the BIOS (Basic Input/Output System) in a computer? (A) RAM (B) Flash memory (C) ROM (D) Cache memory	1	1	4
16.	What is cache memory in computer architecture primarily designed to do? (A) Provide a large and inexpensive storage solution (B) Act as a temporary buffer for frequently accessed data (C) Store all user data and program files (D) Serve as non-volatile storage for the operating system	1	1	4
17.	Which cache mapping technique provides the most flexibility but also requires the most hardware? (A) Direct Mapping (B) Set-Associative Mapping (C) Fully Associative Mapping (D) N-Way Mapping	1	1	5
18.	In direct-mapped cache memory, how many lines in the cache correspond to a single block in main memory? (A) One (B) Two (C) Multiple (D) It varies depending on the cache size	1	1	5
19.	Which stage of the pipeline is responsible for writing the result of an instruction back to the register file or memory? (A) Fetch (B) Decode (C) Execute (D) Write-back	1	1	5
20.	Which component of a computer system is responsible for translating virtual addresses to physical addresses in a virtual memory system? (A) Central Processing Unit (CPU) (B) Memory Management Unit (MMU) (C) Hard Disk Drive (HDD) (D) Input/Output Controller (IOC)	1	1	5

PART - B (5 × 4 = 20 Marks) **Marks BL CO**

Answer **any 5** Questions

21.	Discuss the differences between Ripple counter and Synchronous counter.	4	2	1
22.	Explain the Excess-3 binary code and provide an example of its conversion from a decimal number.	4	3	1
23.	Explain the significance of Boolean functions in digital logic and computer science.	4	2	2
24.	Imagine a multi-processor system with four identical processor cores, each capable of executing tasks independently. Describe a condition where multi-processing can provide a significant performance advantage.	4	3	3
25.	Write about the key concept of cache memory and its primary purpose.	4	2	4
26.	Brief about the Translation Lookaside Buffer (TLB) and its function in memory management.	4	2	4
27.	Consider a computer system with a fixed physical memory size and a virtual memory system implemented using page-based memory management. The virtual memory is divided into fixed-size pages, and the physical memory consists of a limited number of frames. Explain a situation in which the page replacement mechanism is triggered and how it works.	4	3	5

PART - C (5 × 12 = 60 Marks)

Answer **all** Questions

		Marks	BL	CO
28.	(a) Discuss in detail of binary arithmetic in digital logic, covering binary addition, subtraction, multiplication, and division. Provide a detailed response.	12	3	1
	(OR)			
	(b) Explain the key concepts of Boolean algebra and provide examples to illustrate fundamental Boolean operations, identities, and laws.			
29.	(a) Explain the details of hazards, distinguishing between static-0, dynamic, and essential hazards. Provide examples for each type of hazard and discuss techniques to minimize or eliminate hazards in digital circuit design.	12	3	2
	(OR)			
	(b) Discuss the operation of multiplexers and demultiplexers. Explain how a 4-to-1 multiplexer works and provide a detailed example of its application. Additionally, clarify the role of demultiplexers and how they complement the operation of multiplexers in practical systems.			
30.	(a) Explain the significance of addressing modes in instruction execution and provide examples of three addressing modes. Additionally, describe the potential advantages and disadvantages of each addressing mode in terms of code size, execution speed, and flexibility.	12	3	3
	(OR)			
	(b) Illustrate the concept of multiprogrammed control unit and describe it. list out the advantages it offers in enhancing the efficiency of computer systems.			
31.	(a) Describe the concept of I/O organization in detail. Explain the key components and strategies involved in I/O organization.	12	3	4
	(OR)			
	(b) Explain about the Direct Memory Access (DMA) and discuss its significance in modern computer systems.			
32.	(a) Describe in detail the concepts of data path and control considerations. Explain their roles, importance, and challenges in designing efficient data paths and control units.	12	3	5
	(OR)			
	(b) Discuss the need for cache memory. Explain the following three mapping methods with examples. i). Direct. ii). Associative. iii). Set associative.			

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