

- b.i. Define control word, control variables, microinstructions and microprogram. 4 3 4 2
- ii. What is the format of a microinstruction and explain its fields briefly with diagram. 4 3 4 2
25. a. Write in detail about any two types of software parallelism. 8 3 5 2

(OR)

- b. Explain about the cache coherence problem and give solutions for this problem. 8 3 5 2

**PART – C (1 × 15 = 15 Marks)**

Answer ANY ONE Questions

26. Explain the procedure of constructing a fast adder, carry look-ahead adder with its diagram. 15 3 3 2
27. Explain floating point arithmetic addition / subtraction with its flow chart. 15 3 3 2

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Reg. No.

**B.Tech. DEGREE EXAMINATION, MAY 2023**

Third Semester

**21CSS201T – COMPUTER ORGANIZATION ARCHITECTURE**

(For the candidates admitted from the academic year 2022-2023 onwards)

Note:

- (i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40<sup>th</sup> minute.
- (ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: 3 Hours

Max. Marks: 75

**PART – A (20 × 1 = 20Marks)**

Answer ALL Questions

- |  | Marks | BL | CO | PO |
|--|-------|----|----|----|
| 1. The binary equivalent of the decimal number 26.2 is _____<br>(A) 10010.1101 (B) 11010.0011<br>(C) 11110.1110 (D) 01110.0011                                 | 1     | 1  | 2  | 2  |
| 2. Find the hexadecimal value for the decimal number 264<br>(A) 128 (B) 108<br>(C) 2A1 (D) 761   | 1     | 1  | 2  | 2  |
| 3. The 2's complement of the binary number 101101 is _____<br>(A) 011010 (B) 100010<br>(C) 001010 (D) 010011   | 1     | 2  | 2  | 2  |
| 4. Signed 2's complement of -16 in 8-bit representation is _____<br>(A) 10111011 (B) 10001100<br>(C) 01110000 (D) 00110101                                     | 1     | 2  | 2  | 2  |
| 5. _____ performs the desired operations on the input information.<br>(A) Arithmetic and logic unit (B) Input unit<br>(C) Output unit (D) Control unit         | 1     | 2  | 2  | 1  |
| 6. _____ convert the information in binary form to a form understood by user.<br>(A) Input unit (B) ALU<br>(C) Output unit (D) Memory unit                     | 1     | 2  | 2  | 2  |
| 7. _____ holds the instructions that is currently being executed.<br>(A) Program counter (B) Instruction register<br>(C) Registers (D) Memory address register | 1     | 2  | 2  | 2  |
| 8. _____ operations are required in memory access.<br>(A) Add (B) Move<br>(C) Load and store (D) Halt  | 1     | 2  | 2  | 2  |
| 9. _____ is a combinational logic circuit with two input and two output.<br>(A) Full adder (B) Half adder<br>(C) Multiplexer (D) Decoder                       | 1     | 2  | 3  | 2  |

10. \_\_\_\_\_ reduces the number of summands by a factor of 2. 1 2 3 2  
 (A) Bit pair recoding (B) Binary pair recoding  
 (C) Single bit recoding (D) Multiple bit recoding
11. Where does the multiplier operand is stored? 1 2 3 2  
 (A) Cache (B) Instruction register  
 (C) Program counter (D) Shift register
12. How many bits are needed to represent floating point number in a single precision form? 1 2 3 2  
 (A) 16 (B) 32  
 (C) 64 (D) 50
13. A set of microinstructions for a single machine instruction is called 1 2 4 2  
 (A) Application program (B) Command  
 (C) Micro program (D) System files
14. What approach is used to identify the data dependencies when dealing with software? 1 3 4 2  
 (A) Operand forwarding (B) Bubbling  
 (C) NOP (D) Wait signal
15. Branch instruction 'JUMP IF ZERO' is an example of \_\_\_\_\_ 1 3 4 2  
 (A) Transferring the control (B) Conditional branch  
 (C) Unconditional branch (D) Arithmetic branch
16. \_\_\_\_\_ memory is used in pipelining to increase the memory access speed. 1 3 4 2  
 (A) Special memory locations (B) Special purpose register  
 (C) Cache (D) Buffers
17. In \_\_\_\_\_ parallelism the computer architecture has multiple nodes, multiple CPUs and multiple threads. 1 3 5 2  
 (A) Processor (B) Memory  
 (C) Control (D) Data
18. \_\_\_\_\_ is a measure of how many operations can be performed in parallel at the same time. 1 3 5 2  
 (A) Data parallelism (B) Task level parallelism  
 (C) Instruction level parallelism (D) Transaction level parallelism
19. Type of computer where a single instruction would operate or execute on multiple data values is called \_\_\_\_\_ 1 3 5 2  
 (A) Single instruction and multiple data stream (B) Single instruction and single data stream  
 (C) Multiple instruction and single data stream (D) Multiple instruction and multiple data stream

20. \_\_\_\_\_ method is used to design the control unit of ARM processor. 1 3 5 2  
 (A) Hardwired (B) Microprogrammed  
 (C) State machine (D) Combinational circuit

**PART – B (5 × 8 = 40 Marks)**

Answer ALL Questions

21. a. The binary numbers listed have a sign in the leftmost position and if negative are in 2's complement form. Perform the arithmetic operations indicated and verify the answer.s 8 2 1 1  
 (i) 101011 + 111000  
 (ii) 001110 + 110010  
 (iii) 111001 – 001010  
 (iv) 101011 – 100110
- (OR)
- b. Draw the graphic symbol, algebraic function and truth table for the following logic gates. 8 2 1 1  
 (i) AND  
 (ii) OR  
 (iii) NAND  
 (iv) EX-OR
22. a.i. Define instructions and data. 2 1 2 1  
 ii. Write about the operational concepts of the following instructions. 6 1 2 1  
 (i) Add R<sub>0</sub>, LOCA  
 (ii) Load R<sub>2</sub>, LOC  
 (iii) Store R<sub>4</sub>, LOC
- (OR)
- b.i. A computer has 32 MB of memory. How many bits are needed to address any single byte in memory? 2 3 2 1  
 ii. Write about the following instruction types with an example. 6 2 2 1  
 (i) Data transfer instructions  
 (ii) Data manipulation instructions  
 (iii) Arithmetic instructions
23. a. Write about the 4-bit binary parallel adder/subtractor with its diagram. 8 3 3 2
- (OR)
- b.i. What are the advantages of bit pair recoding of multipliers? 3 2 3 2  
 ii. Multiply (+13)×(–6) by using bit pair recoding method. 5 3 3 2
24. a. What are the control signals generated by control unit to execute 8 3 4 2  
 (i) Add (R<sub>3</sub>), R<sub>1</sub>  
 (ii) Unconditional branching