JS^{3}Inth

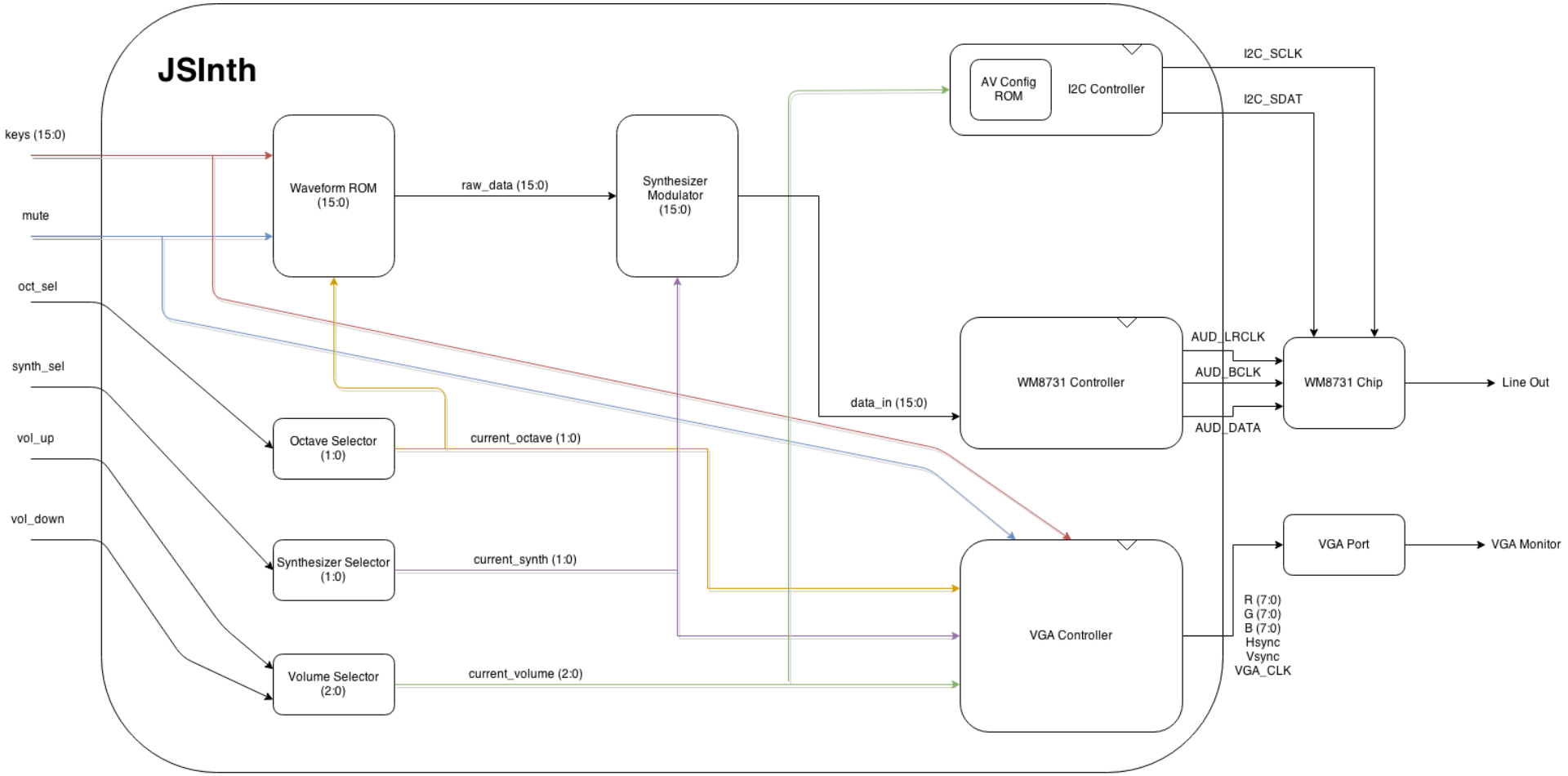
Spring 2015 - Final Presentation

Project Goal

Implement a fully working hardware synthesizer using the WM8731 chip on-board the Altera DE2-115 with a Cyclone IV E FPGA.

Background and Theory

- Every aural signal is composed by sine waves
- By combining sine waves, it is possible to replicate every sound in the universe
- Using VHDL, we stored sine waves in an FPGA to be played back to us as an analog signal. Expanding that, we have a playable musical scale


JSInth
keys (15:0)
mute
oct_sel
synth_sel
vol_up
vol_down
Waveform ROM
(15:0)
raw_data (15:0)
Synthesizer
Modulator
(15:0)
AV Config
ROM
I2C Controller
I2C_SCLK
I2C_SDAT
Octave Selector
(1:0)
current_octave (1:0)
Synthesizer Selector
(1:0)
current_synth (1:0)
Volume Selector
(2:0)
current_volume (2:0)
data_in (15:0)
WM8731 Controller
AUD_LRCLK
AUD_BCLK
AUD_DATA
WM8731 Chip
Line Out
VGA Controller
VGA Port
VGA Monitor
R (7:0)
G (7:0)
B (7:0)
Hsync
Vsync
VGA_CLK

Tasks

- Ian
  - Wave Modulation - Reverb
- Sebastian R
  - WM8731 Controller, VGA Controller, Waveform ROM
- Spencer
  - I^2C Controller and Configuration
- Sebastian W
  - Wave Modulation - Flanger

Architecture

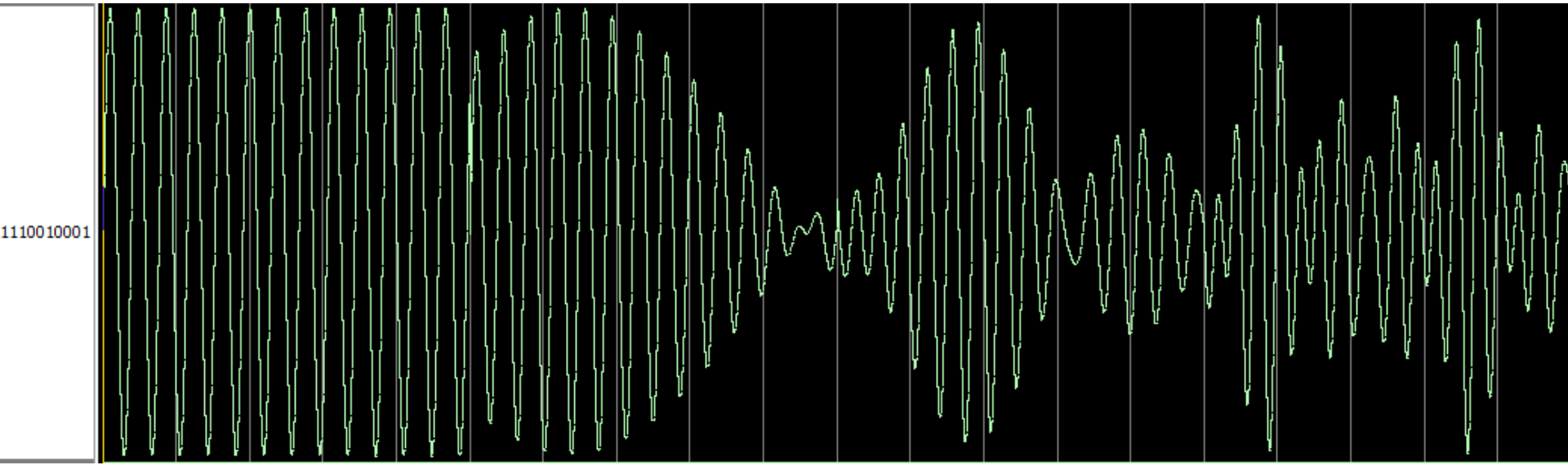
- The Cyclone IV E has 435 9k Block RAMs
  - Synthesized 41 of these as ROMs for data
- Streaming architecture using FIFOs
  - Easier to add waves, producing a cleaner sound
- WM8731 takes specific split clocks
  - Implemented a controller splits every required clock and serializes the ROM samples

Architecture

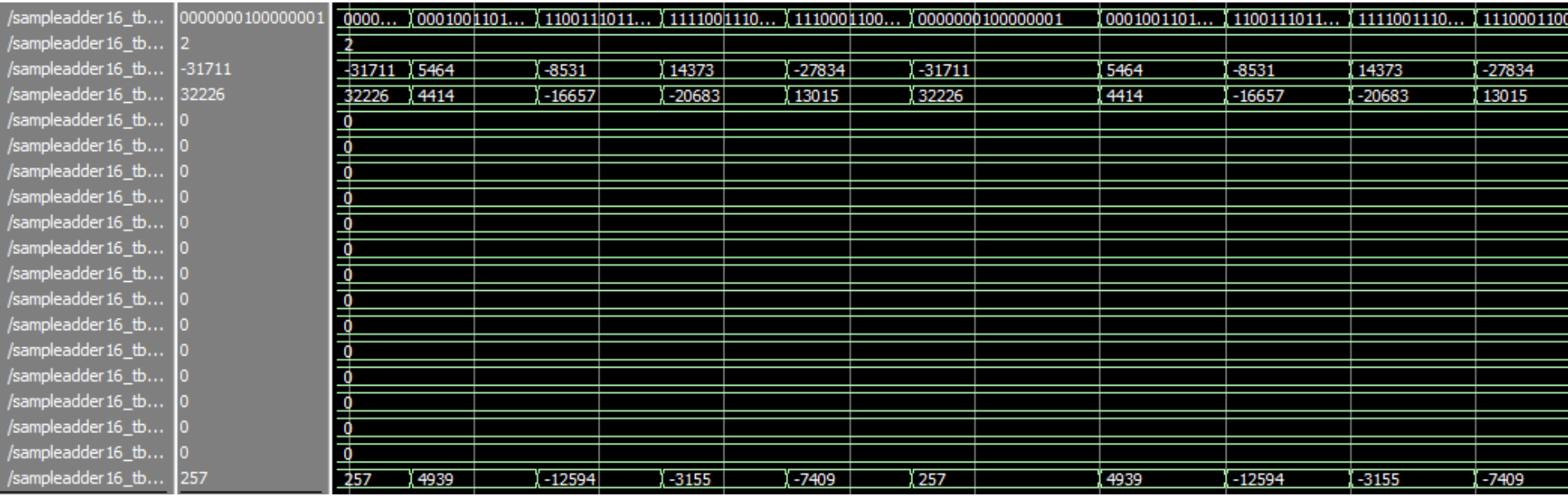
- 2 wave modulators (synthesizers) used
  - Synthesized a 2-bit multiplexer to control usage
  - Reverb
    - Used staggered FIFOs to re-add a previous sample to the current sample
  - Flanger
    - Used an FSM to control the length of the repeating sample

Simulation and Verification

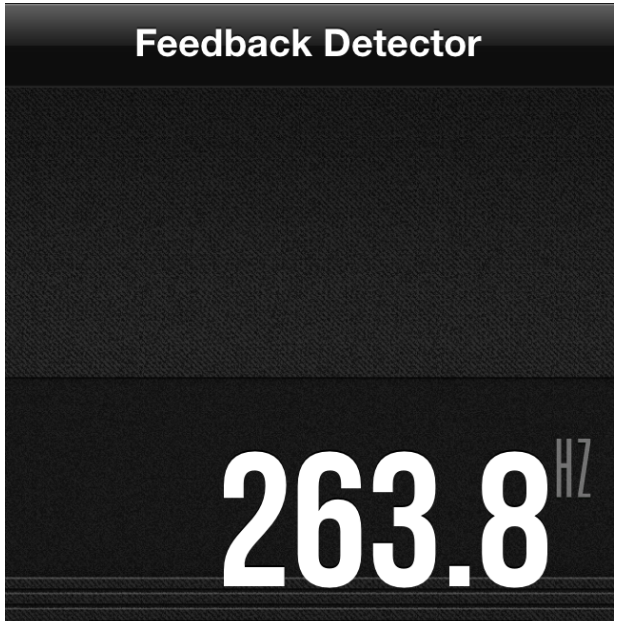
- WM8731 Controller
  - Check single and multiple keys
- Sample Adders
  - Check correct gain when adding
- Wave Modulators
  - Check correct samples are being modulated



WM8731 Controller - data_in



Sample Adders - output



C4 = 261 Hz

D5 = 587 Hz

Aural Verification

Implementation

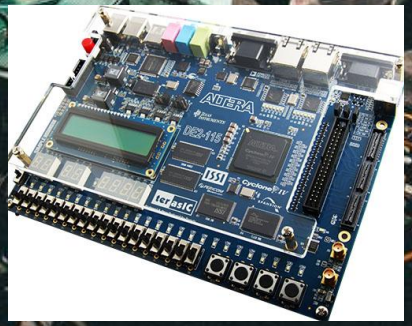
- Total logic elements - 6,782 / 114,480 (6%)
  - Total combinational functions - 6,740 / 114,480 (6%)
  - Dedicated logic registers - 531 / 114,480 (<1%)
- Total registers - 531
- Total pins - 65 / 529 (12%)
- Total memory bits - 2,288 / 3,981,312 (<1%)

- Master Clock - 50 MHz
- Audio Clock - 18.25 MHz

Results

Future Work

- ROM to hold more natural-sounding waves
- Implementation of other wave modulators (i. e. chorus, distortion, etc.)
- Audio input using the WM8731 ADC through Line In
- Implementing a PS/2 keyboard or GPIO as alternate form of input


ALTERA
DE2-115
ISSI
Cyclone IV
terasic

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